INTEGRATED CIRCUITS

DATA HANDBOOK

Linear Products

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Philips Components

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LINEAR PRODUCTS

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MC1489AN	quad line receiver	1447
MC1489D	quad line receiver	1447
MC1489F	quad line receiver	1447
MC1489N	quad line receiver	1447
MC1496F	balanced modulator/demodulator	1171
MC1496N	balanced modulator/demodulator	1171
MC1508-8F	8-bit multiplying DAC	498
MC1558N	dual general purpose operational amplifier	105
MC1596F	balanced modulator/demodulator	1171
MC1596N	balanced modulator/demodulator	1171
MC3302D	quad voltage comparator	602
MC3302F	quad voltage comparator	602
MC3302N	quad voltage comparator	602
MC3303F	quad low power operational amplifier	111
MC3303N	quad low power operational amplifier	111
MC3361D	low power FM IF system	1223
MC3361N	low power FM IF system	1223
MC3403D	quad low power operational amplifier	111
MC3403F	quad low power operational amplifier	111
MC3403N	quad low power operational amplifier	111
MC3410	10-bit high-speed multiplying DAC	504
MC3410C	10-bit high-speed multiplying DAC	504
MC3503F	quad low power operational amplifier	111
MC3510	10-bit high-speed multiplying DAC	504
MEB3000	PDV-bus interface circuit	1525
NE4558D	dual general purpose operational amplifier	138
NE4558FE	dual general purpose operational amplifier	138
NE4558N	dual general purpose operational amplifier	138
NE5018D	8-bit microprocessor-compatible DAC	512
NE5018F	8-bit microprocessor-compatible DAC	512
NE5018N	8-bit microprocessor-compatible DAC	512
NE5019F	8-bit microprocessor-compatible DAC	518
NE5019N	8-bit microprocessor-compatible DAC	518
NE5020F	10-bit microprocessor-compatible DAC	524
NE5020N	10-bit microprocessor-compatible DAC	524
NE5034F	8-bit high-speed ADC	439
NE5036D	6-bit ADC (serial output)	446
NE5036FE	6-bit ADC (serial output)	446
NE5036N	6-bit ADC (serial output)	446
NE5037D	6-bit ADC (parallel outputs)	453
NE5037F	6-bit ADC (parallel outputs)	453
NE5037N	6-bit ADC (parallel outputs)	453
NE5044D	programmable seven-channel RC encoder	879
NE5044N	programmable seven-channel RC encoder	879
NE5045D	seven-channel RC decoder	886

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NE5050D	power line modem	1469
NE5050N	power line modem	1469
NE5060F	precision high-speed sample-and-hold amplifier	398
NE5080N	high-speed FSK modem transmitter	1475
NE5081N	high-speed FSK modem receiver	1479
NE5090D	addressable relay driver	726
NE5090F	addressable relay driver	726
NE5090N	addressable relay driver	726
NE5105AD	precision high-speed comparator with latch	636
NE5105AN	precision high-speed comparator with latch	636
NE5105D	precision high-speed comparator with latch	636
NE5105N	precision high-speed comparator with latch	636
NE5118F	8-bit microprocessor-compatible DAC with current output	532
NE5118N	8-bit microprocessor-compatible DAC with current output	532
NE5119F	8-bit microprocessor-compatible DAC with current output	532
NE5119N	8-bit microprocessor-compatible DAC with current output	532
NE5150F	RGB video DAC	537
NE5151F	RGB video DAC	537
NE5152F	RGB video DAC	537
NE5170A	octal line driver	1450
NE5170D	octal line driver	1450
NE5170N	octal line driver	1450
NE5180A	octal differential line receiver	1457
NE5180N	octal differential line receiver	1457
NE5181A	octal differential line receiver	1457
NE5181N	octal differential line receiver	1457
NE5204D	wide band high frequency amplifier	229
NE5204N	wide band high frequency amplifier	229
NE5205D	wide band high frequency amplifier	239
NE5205EC	wide band high frequency amplifier	239
NE5205FE	wide band high frequency amplifier	239
NE5205N	wide band high frequency amplifier	239
NE521D	high-speed dual differential comparator/sense amplifier	615
NE521F	high-speed dual differential comparator/sense amplifier	615
NE521N	high-speed dual differential comparator/sense amplifier	615
NE5210D	transimpedance amplifier (280 MHz)	325
NE5211D	transimpedance amplifier (180 MHz)	339
NE5212D	transimpedance amplifier (140 MHz)	353
NE5212FE	transimpedance amplifier (140 MHz)	353
NE5212N	transimpedance amplifier (140 MHz)	353
NE5214D	post amplifier with link status indicator	367
NE5217D	post amplifier with link status indicator	374
NE522D	high-speed dual differential comparator/sense amplifier	620
NE522F	high-speed dual differential comparator/sense amplifier	620
NE522N	high-speed dual differential comparator/sense amplifier	620
NE5230D	low voltage operational amplifier	143
NE5230FE	low voltage operational amplifier	143
NE5230N	low voltage operational amplifier	143

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NE527F	voltage comparator	626
NE527H	voltage comparator	626
NE527N	voltage comparator	626
NE529D	voltage comparator	631
NE529F	voltage comparator	631
NE529H	voltage comparator	631
NE529N	voltage comparator	631
NE530FE	high slew rate operational amplifier	116
NE530N	high slew rate operational amplifier	116
NE531FE	high slew rate operational amplifier	123
NE531H	high slew rate operational amplifier	123
NE531N	high slew rate operational amplifier	123
NE532D	dual low power operational amplifier	98
NE532FE	dual low power operational amplifier	98
NE532N	dual low power operational amplifier	98
NE538FE	high slew rate operational amplifier	131
NE538H	high slew rate operational amplifier	131
NE538N	high slew rate operational amplifier	131
NE5410F	10-bit high-speed multiplying DAC	544
NE542N	dual low-noise preamplifier	315
NE544D	servo amplifier	873
NE544N	servo amplifier	873
NE5512D	dual high performance operational amplifier	155
NE5512FE	dual high performance operational amplifier	155
NE5512N	dual high performance operational amplifier	155
NE5514D	quad high performance operational amplifier	158
NE5514F	quad high performance operational amplifier	158
NE5514N	quad high performance operational amplifier	158
NE5517AN	dual operational transconductance amplifier	295
NE5517D	dual operational transconductance amplifier	295
NE5517N	dual operational transconductance amplifier	295
NE5520D	linear variable differential transformer (LVDT) signal conditioner	663
NE5520F	linear variable differential transformer (LVDT) signal conditioner	663
NE5520N	linear variable differential transformer (LVDT) signal conditioner	663
NE5521D	linear variable differential transformer (LVDT) signal conditioner	668
NE5521F	linear variable differential transformer (LVDT) signal conditioner	668
NE5521N	linear variable differential transformer (LVDT) signal conditioner	668
NE5532AFE	internally compensated dual low noise operational amplifier	161
NE5532AN	internally compensated dual low noise operational amplifier	161
NE5532D	internally compensated dual low noise operational amplifier	161
NE5532FE	internally compensated dual low noise operational amplifier	161
NE5532N	internally compensated dual low noise operational amplifier	161

type number	description	page
NE5533AD	dual low noise operational amplifier	167
NE5533AN	dual low noise operational amplifier	167
NE5533D	dual low noise operational amplifier	167
NE5533N	dual low noise operational amplifier	167
NE5534AD	single low noise operational amplifier	167
NE5534AFE	single low noise operational amplifier	167
NE5534AN	single low noise operational amplifier	167
NE5534D	single low noise operational amplifier	167
NE5534FE	single low noise operational amplifier	167
NE5534N	single low noise operational amplifier	167
NE5535F	dual high slew rate operational amplifier	175
NE5535N	dual high slew rate operational amplifier	175
NE5537D	low leakage sample-and-hold amplifier	403
NE5537N	low leakage sample-and-hold amplifier	403
NE5539D	ultra high frequency operational amplifier	253
NE5539F	ultra high frequency pperational amplifier	253
NE5539N	ultra high frequency operational amplifier	253
NE555D	timer	828
NE555F	timer	828
NE555FE	timer	828
NE555N	timer	828
NE556-1F	dual timer	834
NE556-1N	dual timer	834
NE556D	dual timer	834
NE556F	dual timer	834
NE556N	dual timer	834
NE5560D	SMPS controller	939
NE5560F	SMPS controller	939
NE5560N	SMPS controller	939
NE5561D	SMPS controller	954
NE5561FE	SMPS controller	954
NE5561N	SMPS controller	954
NE5562D	SMPS controller	959
NE5562F	SMPS controller	959
NE5562N	SMPS controller	959
NE5568D	SMPS controller	991
NE5568FE	SMPS controller	991
NE5568N	SMPS controller	991
NE5570D	brushless DC motor controller	892
NE5570F	brushless DC motor controller	892
NE5570N	brushless DC motor controller	892
NE558D	quad timer	840
NE558F	quad timer	840
NE558N	quad timer	840
NE5592D	video amplifier	261
NE5592N	video amplifier	261
NE564D	phase-locked loop; 5 V supply; up to 50 MHz; TTL compatible input/output	1289
NE564F	phase-locked loop; 5 V supply; up to 50 MHz; TTL compatible input/output	1289
NE564N	phase-locked loop; 5 V supply; up to 50 MHz; TTL compatible input/output	1289

type number	description	page
NE565D	phase-locked loop; ± 6 to ± 12 V supply; 0.001 Hz to 500 kHz; TTL/DTL compatible output	1298
NE565F	phase-locked loop; ± 6 to ± 12 V supply; 0.001 Hz to 500 kHz; TTL/DTL compatible output	1298
NE565N	phase-locked loop; ± 6 to ± 12 V supply; 0.001 Hz to 500 kHz; TTL/DTL compatible output	1298
NE566D	function generator	1304
NE566F	function generator	1304
NE566N	function generator	1304
NE567D	tone/frequency decoder PLL	1309
NE567F	tone/frequency decoder PLL	1309
NE567FE	tone/frequency decoder PLL	1309
NE567N	tone/frequency decoder PLL	1309
NE568D	phase-locked loop; up to 150 MHz	1321
NE568N	phase-locked loop; up to 150 MHz	1321
NE570F	compandor	1393
NE570N	compandor	1393
NE571D	compandor	1393
NE571F	compandor	1393
NE571N	compandor	1393
NE572D	programmable analogue compandor	1400
NE572N	programmable analogue compandor	1400
NE575D	low voltage dual expander/single compandor or automatic level controller	1408
NE575N	low voltage dual expander/single compandor or automatic level controller	1408
NE587D	LED decoder/driver	785
NE587F	LED decoder/driver	785
NE587N	LED decoder/driver	785
NE589D	LED decoder/driver	795
NE589N	LED decoder/driver	795
NE590F	addressable peripheral drivers	717
NE590N	addressable peripheral drivers	717
NE591F	addressable peripheral drivers	717
NE591N	addressable peripheral drivers	717
NE592D14	video amplifier	267
NE592D8	video amplifier	267
NE592F14	video amplifier	267
NE592H	video amplifier	267
NE592HD14	video amplifier	267
NE592HD8	video amplifier	267
NE592HN14	video amplifier	267
NE592HN8	video amplifier	267
NE592N14	video amplifier	267
NE592N8	video amplifier	267
NE594D	vacuum fluorescent display driver	804
NE594F	vacuum fluorescent display driver	804
NE594N	vacuum fluorescent display driver	804
NE5900	call progress decoder	1327

type no.	description	page
NE602D	double-balanced mixer and oscillator	1175
NE602FE	double-balanced mixer and oscillator	1175
NE602N	double-balanced mixer and oscillator	1175
NE604AD	low power narrow band FM IF system	1226
NE604AN	low power narrow band FM IF system	1226
NE605D	low-power FM IF system	1236
NE605F	low-power FM IF system	1236
NE605N	low-power FM IF system	1236
NE612D	double-balanced mixer and oscillator	1181
NE612N	double-balanced mixer and oscillator	1181
NE615D	high performance low power mixer FM IF system	1240
NE615N	high performance low power mixer FM IF system	1240
SAA1029	universal industrial logic and interface circuit	733
SA1458D	dual general purpose operational amplifier	105
SA1458N	dual general purpose operational amplifier	105
SA4558FE	dual general purpose operational amplifier	138
SA4558N	dual general purpose operational amplifier	138
SA5090N	addressable relay driver	726
SA5105AD	precision high-speed comparator with latch	636
SA5105AN	precision high-speed comparator with latch	636
SA5105D	precision high-speed comparator with latch	636
SA5105N	precision high-speed comparator with latch	636
SA5204D	wide band high frequency amplifier	229
SA5204N	wide band high frequency amplifier	229
SA5205D	wide band high frequency amplifier	239
SA5205FE	wide band high frequency amplifier	239
SA5205N	wide band high frequency amplifier	239
SA5211D	transimpedance amplifier (180 MHz)	339
SA5212D	transimpedance amplifier (140 MHz)	253
SA5212FE	transimpedance amplifier (140 MHz)	253
SA5212N	transimpedance amplifier (140 MHz)	253
SA5214D	post amplifier with link status indicator	367
SA5217D	post amplifier with link status indicator	374
SA5230D	low voltage operational amplifier	143
SA5230N	low voltage operational amplifier	143
SA532D	dual low power operational amplifier	98
SA532FE	dual low power operational amplifier	98
SA532N	dual low power operational amplifier	98
SA534D	quad low power operational amplifier	91
SA534F	quad low power operational amplifier	91
SA534N	quad low power operational amplifier	91
SA5512D	dual high performance operational amplifier	155
SA5521D	linear variable differential transformer (LVDT) signal conditioner	668
SA5521N	linear variable differential transformer (LVDT) signal conditioner	668
SA5534AN	single low noise operational amplifier	167
SA5534N	single low noise operational amplifier	167
SA555D	timer	828
SA555N	timer	828

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SA556-1F	dual timer	834
SA556-1N	dual timer	834
SA556N	dual timer	834
SA5570F	brushless DC motor controller	892
SA5570N	brushless DC motor controller	892
SA558F	quad timer	840
SA558N	quad timer	840
SA571F	compandor	1393
SA571N	compandor	1393
SA572D	programmable analogue compandor	1400
SA572F	programmable analogue compandor	1400
SA572N	programmable analogue compandor	1400
SA592D8	video amplifier	267
SA592N8	video amplifier	267
SA594F	vacuum fluorescent display driver	804
SA594N	vacuum fluorescent display driver	804
SA602D	double-balanced mixer and oscillator	1175
SA602FE	double-balanced mixer and oscillator	1175
SA602N	double-balanced mixer and oscillator	1175
SA604AD	low power narrow band FM IF system	1226
SA604AN	low power narrow band FM IF system	1226
SA615D	high performance low power mixer FM IF system	1240
SA615N	high performance low power mixer FM IF system	1240
SA723CN	precision voltage regulator	993
SA741CN	general purpose operational amplifier	184
SA747CN	dual operational amplifier	190
SE4558FE	dual general purpose operational amplifier	138
SE5018F	8-bit microprocessor-compatible DAC	512
SE5018N	8-bit microprocessor-compatible DAC	512
SE5019F	8-bit microprocessor-compatible DAC	518
SE5060F	precision high-speed sample-and-hold amplifier	398
SE5105AFE	precision high-speed comparator with latch	636
SE105FE	precision high-speed comparator with latch	636
SE5118F	8-bit microprocessor-compatible DAC with current output	532
SE5119F	8-bit microprocessor-compatible DAC with current output	532
SE5205FE	wide band high frequency amplifier	239
SE521F	high speed dual differential comparator/sense amplifier	615
SE5212FE	transimpedance amplifier (140 MHz)	353
SE5212N	transimpedance amplifier (140 MHz)	353
SE522F	high-speed dual differential comparator/sense amplifier	620
SE527F	voltage comparator	626
SE527H	voltage comparator	626
SE529F	voltage comparator	631
SE529H	voltage comparator	631
SE530FE	high slew rate operational amplifier	116
SE530N	high slew rate operational amplifier	116
SE531FE	high slew rate operational amplifier	123
SE531H	high slew rate operational amplifier	123
SE531N	high slew rate operational amplifier	123
SE532FE	dual low power operational amplifier	98
SE532N	dual low power operational amplifier	98

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SE538FE	high slew rate operational amplifier	131
SE538H	high slew rate operational amplifier	131
SE538N	high slew rate operational amplifier	131
SE5410F	10-bit high-speed multiplying DAC	544
SE5512FE	dual high performance operational amplifier	155
SE5512N	dual high performance operational amplifier	155
SE5514F	quad high performance operational amplifier	158
SE5514N	quad high performance operational amplifier	158
SE5521F	linear variable differential transformer (LVDT) signal conditioner	668
SE5532AFE	internally compensated dual low noise operational amplifier	161
SE5532FE	internally compensated dual low noise operational amplifier	161
SE5534AFE	single low noise operational amplifier	167
SE5534AN	single low noise operational amplifier	167
SE5534FE	single low noise operational amplifier	167
SE5534N	single low noise operational amplifier	167
SE5535F	dual high slew rate operational amplifier	175
SE5535N	dual high slew rate operational amplifier	175
SE5537N	low leakage sample-and-hold amplifier	403
SE5539F	ultra high frequency operational amplifier	253
SE5539N	ultra high frequency operational amplifier	253
SE555CF	timer	828
SE555CFE	timer	828
SE555CN	timer	828
SE555F	timer	828
SE555FE	timer	828
SE555N	timer	828
SE556CN	dual timer	834
SE556F	dual timer	834
SE556N	dual timer	834
SE556-1CF	dual timer	834
SE556-1CN	dual timer	834
SE556-1F	dual timer	834
SE556-1N	dual timer	834
SE5560F	SMPS controller	939
SE5560N	SMPS controller	939
SE5561FE	SMPS controller	954
SE5561N	SMPS controller	954
SE5562F	SMPS controller	959
SE5570F	brushless DC motor controller	892
SE5570N	brushless DC motor controller	892
SE558F	quad timer	840
SE558N	quad timer	840
SE564N	phase-locked loop; 5 V supply; up to 50 MHz; TTL compatible input/output	1289
SE565F	phase-locked loop; ± 6 to ± 12 V supply; TTL/DTL compatible output	1298
SE565N	phase-locked loop; ± 6 to ± 12 V supply; TTL/DTL compatible output	1298
SE566F	function generator	1304
SE566N	function generator	1304

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SE567F	tone/frequency decoder PLL	1309
SE567FE	tone/frequency decoder PLL	1309
SE567N	tone/frequency decoder PLL	1309
SE592F14	video amplifier	267
SE592F8	video amplifier	267
SE592H	video amplifier	267
SG1524CF	SMPS controller	999
SG1524CN	SMPS controller	999
SG2524CD	SMPS controller	999
SG2524CF	SMPS controller	999
SG2524CN	SMPS controller	999
SG3524D	SMPS controller	1006
SG3524F	SMPS controller	1006
SG3524N	SMPS controller	1006
SG3524CD	SMPS controller	999
SG3524CF	SMPS controller	999
SG3524CN	SMPS controller	999
SG3526D	SMPS controller	1012
SG3526F	SMPS controller	1012
SG3526N	SMPS controller	1012
TCA520B	low-power/low-voltage operational amplifier	197
TCA520D	low-power/low-voltage operational amplifier	197
TDA1023	proportional-control triac triggering circuit	749
TDA1060	SMPS controller	1023
TDA1060A	SMPS controller	1023
TDA1060B	SMPS controller	1023
TDA1060T	SMPS controller	1023
TDA5030A	mixer/oscillator for VHF/UHF tuners	1187
TDA5030AT	mixer/oscillator for VHF/UHF tuners	1193
TEA1017	13-bit series-parallel converter and display driver	741
TEA1039	SMPS controller	1039
TEA5500	coded locking circuit for security systems	1159
TEA5500T	coded locking circuit for security systems	1159
μA723CD	precision voltage regulator	993
μA723CF	precision voltage regulator	993
μA723CN	precision voltage regulator	993
μA723F	precision voltage regulator	993
μA723N	precision voltage regulator	993
μA733CF	differential video amplifier	276
μA733CN	differential video amplifier	276
μA733F	differential video amplifier	276
μA733N	differential video amplifier	276
μA741CD	general purpose operational amplifier	184
μA741CF	general purpose operational amplifier	184
μA741CN	general purpose operational amplifier	184
μA741F	general purpose operational amplifier	184
μA741N	general purpose operational amplifier	184

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μA747CD	dual operational amplifier	190
μA747CF	dual operational amplifier	190
μA747CN	dual operational amplifier	190
μA747F	dual operational amplifier	190
μA747N	dual operational amplifier	190
μA758	FM stereo multiplex decoder PLL	1334
UC1842N	current mode PWM controller	1051
UC2842D	current mode PWM controller	1051
UC2842N	current mode PWM controller	1051
UC3842D	current mode PWM controller	1051
UC3842N	current mode PWM controller	1051

Cross Reference Guide by Manufacturer

Pin-for-Pin Functionally-Compatible*
Cross Reference by Manufacturer

Manufacturer	Manufacturer Part Number	Signetics Part Number	Temperature Range (°C)	Package
AMD	AM26LS30PC	AM26LS30CN	0 to +70	Plastic
	AM26LS31PC	AM26LS31CN	0 to +70	Plastic
	AM26LS32PC	AM26LS32CN	0 to +70	Plastic
	AM25LS33PC	AM26LS33CN	0 to +70	Plastic
	AM6012DC	AM6012F	0 to +70	Ceramic
	DAC-08AQ	DAC-08AF	−55 to +125	Ceramic
	DAC-08CN	DAC-08CN	0 to +70	Plastic
	DAC-08CQ	DAC-08CF	0 to +70	Ceramic
	DAC-08EN	DAC-08EN	0 to +70	Plastic
	DAC-08EQ	DAC-08EF	0 to +70	Ceramic
	DAC-08HN	DAC-08HN	0 to +70	Plastic
	DAC-08HQ	DAC-08HF	0 to +70	Ceramic
	DAC-08Q	DAC-08F	−55 to +125	Ceramic
	LF198H	LF198H	−55 to +125	Metal Can
	LF198H	SE5537H	−55 to +125	Metal Can
	LF398H	LF398H	0 to +70	Metal Can
	LF398H	NE5537H	0 to +70	Metal Can
	LF398L	LF398D	0 to +70	Plastic
	LF398L	NE5537D	0 to +70	Plastic
	LF398N	LF398N	0 to +70	Plastic
	LF398N	NE5537N	0 to +70	Plastic
Datel	AM-453-2	NE5534/AF	0 to +70	Ceramic
	AM-453-2C	NE5534/AF	0 to +70	Ceramic
	AM-453-2M	SE5534/AF	−55 to +125	Ceramic
	DAC-UP10BC	NE5020N	0 to +70	Plastic
	DAC-UP8BC	NE5018N	0 to +70	Plastic
	DAC-UP8BM	SE5019F	−55 to +125	Ceramic
	DAC-UP8BQ	SE5018F	−55 to 125	Ceramic
Exar	XR-558CN	NE558F	0 to +70	Ceramic
	XR-558CP	NE558N	0 to +70	Plastic
	XR-558M	SE558F	−55 to +125	Ceramic
	XR-L567CN	NE567F	0 to +70	Ceramic
	XR-L567CP	NE567N	0 to +70	Plastic
	XR-1488CP	MC1488N	0 to +70	Plastic
	XR-1489/ACP	MC1489/AN	0 to +70	Plastic
	XR-1524N	SG3524F	0 to +70	Ceramic
	XR-1524P	SG3524N	0 to +70	Plastic
	XR-2524P	SG3524N	0 to +70	Plastic
	XR-3524N	SG3524F	0 to +70	Ceramic
	XR-3524P	SG3524N	0 to +70	Plastic
	XR-4558CP	NE4558N	0 to +70	Plastic
	XR-5532/A N	NE5532/AF	0 to +70	Ceramic
	XR-5532/A P	NE5532/AN	0 to +70	Plastic
	XR-5534/A CN	NE5534/AF	0 to +70	Ceramic
	XR-5534/A CP	NE5534/AN	0 to +70	Plastic
	XR-5534/A M	SE5534/AF	−55 to +125	Ceramic
	XR-6118CP	NE594N	0 to +70	Plastic
	XR-13600CP	NE5517N	0 to +70	Plastic
Harris	HA-2539N	NE5539N	0 to +70	Plastic
	HA-2420-2/8B	SE5060F	−55 to +125	Ceramic
	HA-2425N	NE5060N	0 to +70	Plastic
	HA-2425B	NE5060F	0 to +70	Ceramic
	HA-5320B	NE5060F	0 to +70	Ceramic

Manufacturer	Manufacturer Part Number	Signetics Part Number	Temperature Range (°C)	Package
	HA1-5102-2	SE5532/AF	−55 to +125	Ceramic
	HA1-5135-2	SE5534/AF	−55 to +125	Ceramic
	HA1-5135-5	NE5534/AF	0 to +70	Ceramic
	HA1-5202-5	NE5532/AF	0 to +70	Ceramic
	HA3-5102-5	NE5532/AN	0 to +70	Plastic
Intersil	ADC0803LCD	ADC0803-1 LCF	−40 to +85	Ceramic
	ADC0804	ADC0804-1 CN	0 to +70	Plastic
	ADC0805	ADC0805-1 LCN	−40 to +85	Plastic
	ICM7555CBA	ICM7555CD	0 to +70	Plastic
	ICM7555IPA	ICM7555IN	−40 to +85	Plastic
	ACM7555CP	ICM7555CN	0 to +70	Plastic
Motorola	AM26LS31PCD	AM26LS31CD	0 to +70	Plastic
	AM26LS31PC	AM26LS31CN	0 to +70	Plastic
	AM26LS32PC	AM26LS32CN	0 to +70	Plastic
	AM26LS32PCD	AM26LS32CD	0 to +70	Plastic
	DAC-08CD	DAC-08CN	0 to +70	Plastic
	DAC-08CQ	DAC-08CF	0 to +70	Ceramic
	DAC-08ED	DAC-08EN	0 to +70	Plastic
	DAC-08EF	DAC-08EF	0 to +70	Ceramic
	DAC-08HQ	DAC-08HF	0 to +70	Ceramic
	DAC-08Q	DAC-08F	−55 to +125	Ceramic
	LM2901N	LM2901N	−40 to +85	Plastic
	LM311J-8	LM311F	0 to +70	Ceramic
	LM311N	LM311N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM324N	LM324N	0 to +70	Plastic
	LM339/A J	LM339/AF	0 to +70	Ceramic
	LM339/A N	LM339/AN	0 to +70	Plastic
	LM358N	LM358N	0 to +70	Plastic
	LM393A/J	LM393/AF	0 to +70	Ceramic
	LM393A/N	LM393/AN	0 to +70	Plastic
	MC1408L	MC1408F	0 to +70	Ceramic
	MC1408P	MC1408N	0 to +70	Plastic
	MC1488L	MC1488F	0 to +70	Ceramic
	MC1488P	MC1488N	0 to +70	Plastic
	MC1489/A L	MC1489/AF	0 to +70	Ceramic
	MC1489/A P	MC1489/AN	0 to +70	Plastic
	MC1496L	MC1496F	0 to +70	Ceramic
	MC1496P	MC1496N	0 to +70	Plastic
	MC3302L	MC3302F	−40 to +85	Ceramic
	MC3302P	MC3302N	−40 to +85	Plastic
	MC3361D	MC3361D	0 to +70	Plastic
	MC3361P	MC3361N	0 to +70	Plastic
	MC3403L	MC3403F	0 to +70	Ceramic
	MC3403P	MC3403N	0 to +70	Plastic
	MC3410CL	MC3410CF	0 to +70	Ceramic
	MC3410L	MC3410F	0 to +70	Ceramic
		NE5410F	0 to +70	Ceramic
	MC3510L	MC5410F	−55 to +125	Ceramic
	NE565N	NE565N	0 to +70	Plastic
	NE592F	NE592F-8	0 to +70	Ceramic
	NE592F	NE592F-14	0 to +70	Ceramic
	NE592N	NE592N-14	0 to +70	Plastic

Cross Reference Guide by Manufacturer

Manufacturer	Manufacturer Part Number	Signetics Part Number	Temperature Range (°C)	Package
	SE592F	SE592F-8	−55 to +125	Ceramic
	SE592F	SE592F-14	−55 to +125	Ceramic
	SE592H	SE592H	−55 to +125	Metal Can
National	ADC0803F	ADC0803-1 LCF	−40 to +85	Ceramic
	ADC0803N	ADC0803-1 LCN	−40 to +85	Plastic
	ADC0805	ADC0805-1 LCN	−40 to +85	Plastic
	ADC0820CCN	ADC0820CNEN	0 to +70	Plastic
	ADC0820CCD	ADC0820CSAN	−40 to +85	Plastic
	ADC0820CD	ADC0820CSEF	−55 to +125	Ceramic
	DAC0800LCJ	DAC-08EF	0 to +70	Ceramic
	DAC0800LJ	DAC-08F	−55 to +125	Ceramic
	DAC0800LCN	DAC-08EN	0 to +70	Plastic
	DAC0801LCJ	DAC-08CF	0 to +70	Ceramic
	DAC0801LCN	DAC-08CN	0 to +70	Plastic
	DAC0802LJ	DAC-08AF	−55 to +125	Ceramic
	DAC0802LCJ	DAC-08HF	0 to +70	Ceramic
	DAC0802LCN	DAC-08HN	0 to +70	Plastic
	DAC0806LCJ	MC1408-6F	0 to +70	Ceramic
	DAC0806LCN	MC1408-6N	0 to +70	Plastic
	DAC0807LCJ	MC1408-7F	0 to +70	Ceramic
	DAC0807LCN	MC1408-7N	0 to +70	Plastic
	DAC0808LCJ	MC1408F	0 to +70	Ceramic
	DAC0808LCN	MC1408N	0 to +70	Plastic
	DAC0808LD	MC1408F	0 to +70	Ceramic
	DS3691N	AM26LS30CN	0 to +70	Plastic
	DS3691M	AM26LS30CD	0 to +70	Plastic
	LF198H	SE5537H	−55 to +125	Metal Can
	LF398H	NE5537H	0 to +70	Metal Can
	LF398N	NE5537N	0 to +70	Plastic
	LM13600AN	NE5517N	0 to +70	Plastic
	LM13600N	NE5517N	0 to +70	Plastic
	LM1458N	MC1458N	0 to +70	Plastic
	LM161H	SE529H	−55 to +125	Metal Can
	LM161J	SE529F	−55 to +125	Ceramic
	LM2524J	SG3524F	0 to +70	Ceramic
	LM2524N	SG3524N	0 to +70	Plastic
	LM2901N	LM2901N	−40 to +85	Plastic
	LM2903N	LM2903N	−40 to +85	Plastic
	LM3089	CA3089N	−55 to +125	Plastic
	LM319J	LM319F	0 to +70	Ceramic
	LM319N	LM319N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM324N	LM324N	0 to +70	Plastic
	LM324AD	LM324AD	0 to +70	Plastic
	LM324AN	LM324AN	0 to +70	Plastic
	LM339/AJ	LM339/AF	0 to +70	Ceramic
	LM339/AN	LM339/AN	0 to +70	Plastic
	LM3524J	SG3524F	0 to +70	Ceramic
	LM3524N	SG3524N	0 to +70	Plastic
	LM358H	LM358H	0 to +70	Metal Can
	LM358N	LM358N	0 to +70	Plastic
	LM361H	NE529H	0 to +70	Metal Can
	LM361J	NE529D	0 to +70	
	LM361N	NE529N	0 to +70	Plastic
	LM393/AN	LM393/AN	0 to +70	Plastic
	LM555J	NE555F	0 to +70	Ceramic
	LM555N	NE555N	0 to +70	Plastic
	LM556J	SE556-1F	−55 to +125	Ceramic
	LM556N	SE556-1N	−55 to +125	Plastic
	LM556CJ	NE556-1F	0 to +70	Ceramic
	LM556CN	NE556-1N	0 to +70	Plastic
	LM565CN	NE565N	0 to +70	Plastic
	LM566N	SE566N	−55 to +125	Plastic
	LM566CN	NE566N	0 to +70	Plastic
	LM567CN	NE567N	0 to +70	Plastic
	LM733CN	μA733CN	0 to +70	Plastic
	LM741CJ	μA741CF	0 to +70	Ceramic
	LM741CN	μA741CN	0 to +70	Plastic
	LM741J	μA741F	−55 to +125	Ceramic
	LM741N	μA741N	−55 to +125	Plastic
	LM747CJ	μA747CF	0 to +70	Ceramic
	LM747CN	μA747CN	0 to +70	Plastic
	LM747J	μ747F	−55 to +125	Ceramic
	LM747N	μA747N	−55 to +125	Plastic
	LMC555CN	ICM7555CN	0 to +70	Plastic
	LMC555CM	ICM7555CD	0 to +70	Plastic
	μA080/DA	DAC-08F	0 to +70	Ceramic
	μA0801CDC	MC1408F	0 to +70	Ceramic
	μA0801CPC	MC1408N	0 to +70	Plastic
	μA0801EDC	DAC-08EF	0 to +70	Ceramic
	μA0801EPC	DAC-08AF	0 to +70	Ceramic
	μA124J	LM124F	−55 to +125	Ceramic
	μA1458TC	MC1458N	0 to +70	Plastic
	μA1488DC	MC1488F	0 to +70	Ceramic
	μA1488PC	MC1488N	0 to +70	Plastic
	μA1489/A PC	MC1489/AF	0 to +70	Ceramic
	μA1489/A PC	MC1489/AN	0 to +70	Plastic
	μA198HM	NE5537H	0 to +70	Metal Can
	μA198RM	NE5537N	0 to +70	Plastic
	μA2901DC	LM2901F	−40 to +85	Ceramic
	μA2901PC	LM2901N	−40 to +85	Plastic
	μA311RC	LM311F	0 to +70	Ceramic
	μA324DC	LM324F	0 to +70	Ceramic
	μA324PC	LM324N	0 to +70	Plastic
	μA3302DC	MC3302F	−40 to +85	Ceramic
	μA3302PC	MC3302N	−40 to +85	Plastic
	μA339/ADC	LM339/AF	0 to +70	Ceramic
	μA339/APC	LM339/AN	0 to +70	Plastic
	μA3403DC	MC3403F	0 to +70	Ceramic
	μA3403PC	MC3403N	0 to +70	Plastic
	μA398HC	SE5537H	−55 to +125	Metal Can
	μA398RC	SE5537N	−55 to +125	Plastic
	μA555TC	NE555N	0 to +70	Plastic
	μA556PC	NE556-1N, NE556N	0 to +70	Plastic
	μA723DC	μA723CF	0 to +70	Ceramic
	μA723DM	μA723F	−55 to +125	Ceramic
	μA723PC	μA723CN	0 to +70	Plastic
	μA733DC	μA733F	0 to +70	Ceramic
	μA733DM	μA733F	−55 to +125	Ceramic
	μA733PC	μA733N	0 to +70	Plastic
	μA741NM	μA741N	−55 to +125	Plastic
	μA741RC	μA741CF	0 to +70	Ceramic
	μA741TC	μA741CN	0 to +70	Plastic
	μA747DC	μA747CF	0 to +70	Ceramic
	μA747PC	μA747CN	0 to +70	Plastic
	UC3842D	UC3842D	0 to +70	Plastic
	UC3842J	UC3842FE	0 to +70	Ceramic
	UC3842N	UC3842N	0 to +70	Plastic
	UC2842D	UC2842D	0 to +70	Plastic
	UC2842J	UC2842FE	0 to +70	Ceramic
	UC2842N	UC2842N	0 to +70	Plastic

Cross Reference Guide by Numeric Listing

Manufacturer	Manufacturer Part Number	Signetics Part Number	Temperature Range (°C)	Package
	UC1842J	UC1842FE	−55 to +125	Ceramic
	UC1842N	UC1842N	−55 to +125	Plastic
NEC	μPC1571C	NE571N	0 to +70	Plastic
PMI	CMP-05GP	NE5105N	0 to +70	Plastic
	CMP-05CZ	SE5105F	−55 to +125	Ceramic
	CMP-05BZ	SE5105F	−55 to +125	Ceramic
	CMP-05GZ	SA5105N	−40 to +85	Plastic
	CMP-05FZ	SA5105N	−40 to +85	Plastic
	DAC1408A-6P	MC1408-6N	0 to +70	Plastic
	DAC1408A-6Q	MC1408-6F	0 to +70	Ceramic
	DAC1408A-7N	MC1408-7N	0 to +70	Plastic
	DAC1408A-7Q	MC1408-7F	0 to +70	Ceramic
	DAC1408A-8N	MC1408-8N	0 to +70	Plastic
	DAC1408A-8Q	MC1408-8F	0 to +70	Ceramic
	DAC1508A-8Q	MC1408-8F	−55 to +125	Ceramic
	DAC312FR	AM6012F	0 to +70	Ceramic
	OP27BZ	SE5534AFE	−55 to +125	Ceramic
	OP27CZ	SE5534FE	−55 to +125	Ceramic
	PM747Y	μA747N	−55 to +125	Plastic
	SMP-10AY	SE5060F	−55 to +125	Ceramic
	SMP-10EY	NE5060N	0 to +70	Plastic
	SMP-11AY	SE5060F	−55 to +125	Ceramic
	SMP-11EY	NE5060N	0 to +70	Plastic
Raytheon	RC4805DE	NE5105N	0 to +70	Plastic
	RC4805EDE	NE5105AN	0 to +70	Plastic
	RM4805DE	SE5105F	−55 to +125	Ceramic
	RM4805ADE	SE5105AF	−55 to +125	Ceramic
	RC5532/A DE	NE5532/AF	0 to +70	Ceramic
	RC5532/A NB	NE5532/AN	0 to +70	Plastic
	RC5534/A DE	NE5534/AF	0 to +70	Ceramic
	RC5534/A NB	NE5534/AN	0 to +70	Plastic
	RM5532/A DE	SE5532/AF	−55 to +125	Ceramic
	RM5534/A DE	SE5534/AF	−55 to +125	Ceramic
Silicon General	SG3524J	SG3524F	0 to +70	Ceramic
	SG3526N	SG3526N	0 to +70	Plastic
Sprague	UDN6118A	SA594N	−40 to +85	Plastic
	UDN6118R	SA594F	−40 to +85	Ceramic
	ULN3524A	SG3524	0 to +70	Plastic
	ULN8142M	UC3842N	0 to +70	Plastic
	ULN8160A	NE5560N	0 to +70	Plastic
	ULN8160R	NE5560F	0 to +70	Ceramic
	ULN8161M	NE5561N	0 to +70	Plastic
	ULN8168M	NE5568N	0 to +70	Plastic
	ULN8564A	NE564N	0 to +70	Plastic
	ULN8564R	NE564F	0 to +70	Ceramic
	ULS8564R	SE564F	−55 to +125	Ceramic
TI	ADC0803N	ADC0803-1 LCN	−40 to +85	Plastic
	ADC0804CN	ADC0804-1 CN	0 to +70	Plastic
	ADC0805N	ADC0805-1 LCN	−40 to +85	Plastic
	LM111J	LM111F	−55 to +125	Ceramic
	LM311D	LM311D	0 to +70	Plastic
	LM311J	LM311F	0 to +70	Ceramic
	LM311JG	LM311FE	0 to +70	Ceramic
	LM324D	LM324N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM339/AJ	LM339/AF	0 to +70	Ceramic
	LM339/AN	LM339/AN	0 to +70	Plastic
	LM358P	LM358N	0 to +70	Plastic
	LM393/A P	LM393/AN	0 to +70	Plastic
	MC1458P	MC1458N	0 to +70	Plastic
	NE5532/A JG	NE5532/AF	0 to +70	Ceramic
	NE5532/A P	NE5532/AN	0 to +70	Plastic
	NE5534/A JG	NE5534/AF	0 to +70	Ceramic
	NE5534/A P	NE5534/AN	0 to +70	Plastic
	NE555JG	NE555N	0 to +70	Plastic
	NE555P	NE555N	0 to +70	Plastic
	NE556P	NE556N	0 to +70	Plastic
	NE556J	NE556-1F	0 to +70	Ceramic
	NE556N	NE556-1N	0 to +70	Plastic
	NE592	NE592N14	0 to +70	Plastic
	NE592A	NE592F14	0 to +70	Ceramic
	NE592J	NE592F	0 to +70	Ceramic
	NE592N	NE592N-14	0 to +70	Plastic
	SA556P	SA556N	−40 to +85	Plastic
	SE5534/A JG	SE5534/AF	−55 to +125	Ceramic
	SE555JG	SE555N	−55 to +125	Plastic
	SE556J	SE556-1F	−55 to +125	Ceramic
	SE556N	SE556-1N	−55 to +125	Plastic
	SE592	SE592N14	−55 to +125	Plastic
	SE592J	SE592F-14	−55 to +125	Ceramic
	SE592N	SE592N-14	−55 to +125	Plastic
	SN55107AJ	NE521F	0 to +70	Plastic
	SN55108AJ	SE522F	−55 to +125	Ceramic
	SN75107AJ	NE521F	0 to +70	Plastic
	SN75107AN	NE521N	0 to +70	Plastic
	SN75108AJ	NE522F	0 to +70	Ceramic
	SN75108AN	NE522N	0 to +70	Plastic
	SN75188J	MC1488F	0 to +70	Ceramic
	SN75188N	MC1488N	0 to +70	Plastic
	SN75189AJ	MC1489AF	0 to +70	Ceramic
	SN75189AN	MC1489AN	0 to +70	Plastic
	SN75189J	MC1489F	0 to +70	Ceramic
	SN75189N	MC1489A	0 to +70	Plastic
	TL592A	NE592F14	0 to +70	Ceramic
	TL592P	NE592NB	0 to +70	Plastic
	μA723CJ	μA723CF	0 to +70	Ceramic
	μA723CN	μA723CN	0 to +70	Plastic
	μA723MJ	μA723F	−55 to +125	Ceramic
Unitrode	UC3524J	SG3524F	0 to +70	Ceramic
	UC3524N	SG3524N	0 to +70	Plastic

*THERE MAY BE PARAMETRIC DIFFERENCES BETWEEN SIGNETICS' PARTS AND THOSE OF THE COMPETITION.

GENERAL

Product status definitions

for type numbers with prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA and UC

Ordering information

for type numbers with prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA and UC

Quality and reliability

for type numbers with prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA and UC

Type designation

for type numbers with prefixes MEB, SAA, TCA, TDA and TEA

Rating systems

for type numbers with prefixes MEB, SAA, TCA, TDA and TEA

Handling MOS devices

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Signetics' Linear integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:

$1000 per order
$250 per line item per order

Military Product:

$250 per line item per order

Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that an SE prefix (−55°C to +125°C) indicates only the operating temperature range of a device and *not* its military qualification status. The military qualification status of any Linear product can be determined by either looking in the Military Data Manual and/or contacting your local sales office.

Table 1. Part Number Description

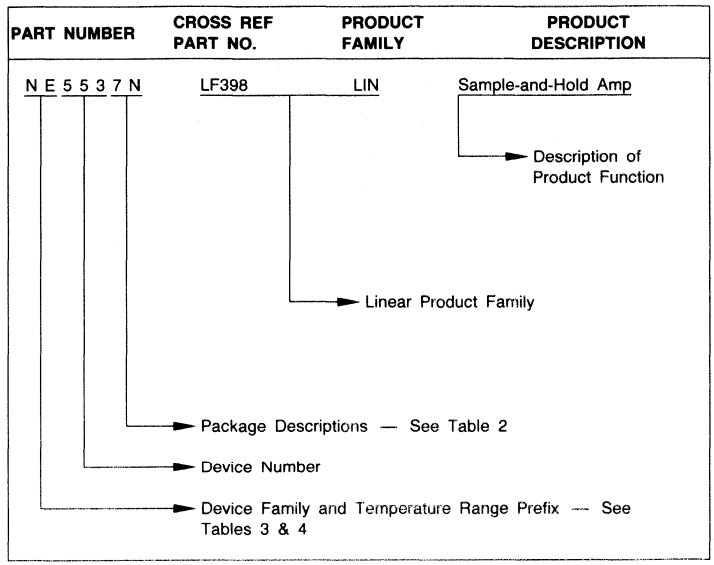


Table 2. Package Descriptions

OLD	NEW	PACKAGE DESCRIPTION
A, AA	N	14-lead plastic DIP
A	N-14	14-lead plastic DIP (selected analog products only)
B, BA	N	16-lead plastic DIP
	D	Microminiature package (SO)
F	F	14-, 16-, 18-, 22-, and 24-lead ceramic DIP (Cerdip)
I, IK	I	14-, 16-, 18-, 22-, 28-, and 4-lead ceramic DIP
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA, NX	N	24-lead plastic DIP
Q, R	Q	10-, 14-, 16-, and 24-lead ceramic flat
T, TA	H	8-lead TO-99
U	U	SIP plastic power
V	N	8-lead plastic DIP
XA	N	18-lead plastic DIP
XC	N	20-lead plastic DIP
XC	N	22-lead plastic DIP
XL, XF	N	28-lead plastic DIP
	A	PLCC
	EC	TO-46 header
	FE	8-lead ceramic DIP

Table 3. Signetics Prefix and Device Temperature

PREFIX	DEVICE TEMPERATURE RANGE
NE	0 to +70°C
SE	−55°C to +125°C
SA	−40°C to +85°C

Table 4. Industry Standard Prefix

PREFIX	DEVICE FAMILY
ADC	Linear Industry Standard
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
ICM	Linear Industry Standard
LF	Linear Industry Standard
LM	Linear Industry Standard
MC	Linear Industry Standard
NE	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
UC	Linear Industry Standard

Quality and Reliability

SIGNETICS' ZERO DEFECTS PROGRAM

In recent years, American industry has demanded increased product quality of its IC suppliers in order to meet growing international competitive pressures. As a result of this quality focus, it is becoming clear that what was once thought to be unattainable — zero defects — is, in fact, achievable.

The IC supplier committed to a standard of zero defects provides a competitive advantage to today's electronics OEM. That advantage can be summed up in four words: *reduced cost of ownership.* As IC customers look beyond purchase price to the total cost of doing business with a vendor, it is apparent that the quality-conscious supplier represents a viable cost reduction resource. Consistently high quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures.

REDUCING THE COST OF OWNERSHIP THROUGH TOTAL QUALITY PERFORMANCE

Quality involves more than just IC's that work. It also includes cost-saving advantages that come with error-free service — on-time delivery of the right quantity of the right product at the agreed-upon price. Beyond the product, you want to know you can place an order and feel confident that no administrative problems will arise to tie up your time and personnel.

Today, as a result of Signetics' growing appreciation of the concern with cost of ownership, our quality improvement efforts extend out from the traditional areas of product conformance into every administrative function, including order entry, scheduling, delivery, shipping, and invoicing. Driving this process is a Corporate Quality Improvement Team, comprised of the president and his staff, which oversees the activities of 30 other Quality Improvement Teams throughout the company.

LINEAR PRODUCT QUALITY

Signetics has put together a winning process for the manufacturing of Linear Integrated Circuits. The circuits produced by our Linear Division must meet rigid criteria as defined in our design rules and as evaluated through product characterization over the device operating temperature range.

Product conformance to specification is measured throughout the manufacturing cycle. Signetics calls the first submittal to a Product or Quality Assurance gate our Estimated Process Quality or EPQ. It is an internal measure used to drive our Quality Improvement Programs toward our goal of Zero Defects. All product acceptance sampling plans have zero as their acceptance criteria. Only shipments that demonstrate zero defects during these acceptance tests may be shipped to our customers. This is in accordance with our commitment to our Zero Defect policy.

Our standard is Zero Defects and our customers' statistics and awards for outstanding product quality demonstrate our advance toward this goal. Nowhere is this more evident than at our Electrical and Visual-Mechanical Outgoing Product Assurance inspection gates. Over the past eight years, the measured defect level at the first submission to Electrical Product Assurance for Linear products has dropped from over 4000PPM (0.4%) to under 50PPM (0.005%) (See Figure 1a). Similarly our Visual-Mechanical (body defects, lead bend, etc.) defect level has improved remarkably (see Figure 1b). The results from our Quality Improvement Program have allowed Signetics to take the industry leadership position with its Zero Defects Limited Warranty policy. No longer is it necessary to negotiate a mutually acceptable AQL between buyer and Signetics. Signetics will replace any lot in which a customer finds one verified defective part.

QUALITY DATABASE REPORTING SYSTEM — QA05

The capabilities of our manufacturing process are measured and the results are recorded through our corporate-wide QA05 database system. The QA05 system collects the results on all finished lots and feeds this data back to concerned organizations where appropriate corrective actions can be taken. The QA05 reports Estimated Process Quality (EPQ) data which are the sample inspection results for first submittal lots to Quality Assurance inspection for electrical, visual/mechanical, hermeticity, and documentation. Data from this system is available upon request and is distributed routinely to our customers who have formally adopted our Ship-to-Stock program.

CUSTOMER/VENDOR COOPERATION IS AT THE HEART OF ZERO DEFECTS AND REDUCED COSTS

Working to a zero defects standard requires that emphasis be consistently placed, not on "catching" defects, but on preventing them from ever occurring. This strong preventive focus, which demands that quality be "built-in" rather than "inspected in," includes a much greater attention to ongoing communication on quality-related issues. At Signetics, a focus on this cooperative approach has resulted in better service to all customers and the development of two innovative customer/vendor programs: Ship-to-Stock and Self-Qual.

Signetics' Ship-to-Stock Program

Ship-to-Stock is a joint program between Signetics and a customer which formally certifies specific parts to go directly into inventory or to the assembly line from the customer's receiving dock without incoming inspection. This program was developed at the request of several major customers after they had worked with us and had a chance to experience the data exchange and joint corrective action that occurs as part of our quality improvement program.

The key elements of the Ship-to-Stock program are:

- Signetics and customer agree on a list of products to be certified, complete device correlation, and sign a specification.
- The product Estimated Product Quality (EPQ) must be 300ppm or less for the past 3 months.
- Signetics will share Quality (QA05) and Reliability data on a regular basis.
- Signetics will alert Ship-to-Stock customers of any changes in quality or reliability which could adversely impact their product.

Any customer interested in the benefits of the Ship-to-Stock program should contact his local Signetics sales office for a brochure and further details.

As a result of their participation in the Ship-to-Stock Program, many of our customers have eliminated costly incoming testing on selected ICs. We will work together with any customer interested to establish a Ship-to-Stock Program, and identify the products to be included in the program and finalize all neces-

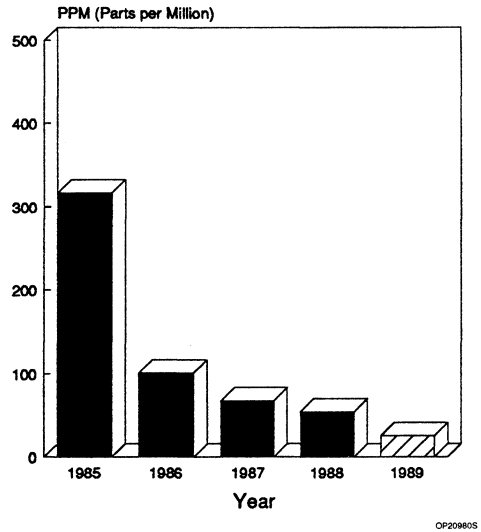


Figure 1a. Product Electrical Quality

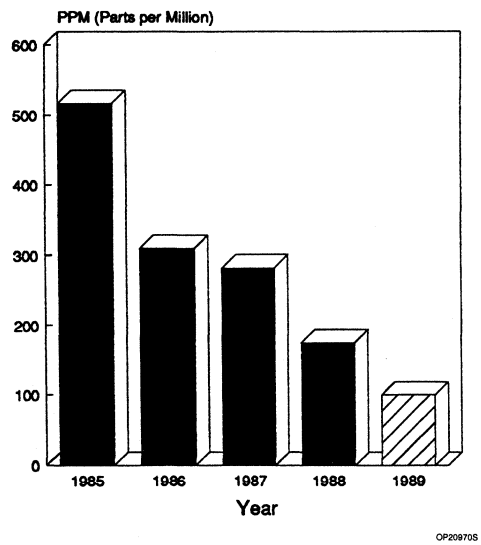


Figure 1b. Visual-Mechanical Quality

sary terms and conditions. From that point, the specified products can go directly from the receiving dock to the assembly line or into inventory. Signetics then provides, free of charge, monthly reports on those products.

In our efforts to continually reduce cost of ownership, we are now using the experience we have gained with Ship-to-Stock to begin developing a Just-in-Time Program. With Just-in-Time, products will be delivered to the receiving dock just as they are needed, permitting continuous-flow manufacturing and eliminating the need for expensive inventories.

Signetics Self-Qual Program

Like Ship-to-Stock, our Self-Qual Program employs a cooperative approach based on ongoing information exchange. At Signetics, formal qualification procedures are required for all new or changed materials, processes, products, and facilities. Prior to 1983, we created our qualification programs independently. Our major customers would then test samples to confirm our findings. Now, under the new Self-Qual Program, customers can be directly involved in the prequalification stage. When we feel we have a promising enhancement to offer, customers will be invited to participate in the development of the qualification plan. This eliminates the need to duplicate expensive qualification testing and also adds another dimension to our ongoing efforts to build in quality.

WE WANT TO WORK WITH YOU

At Signetics, we know that our success depends on our ability to support all our customers with the defect-free, higher density, higher performance products needed to compete effectively in today's demanding business environment. To achieve this goal, quality in another arena — that of communications — is vital. Here are some specific ways we can maintain an ongoing dialogue and information exchange between your company and ours on the quality issue:

- Periodical face-to-face exchanges of data and quality improvement ideas between the customer and Signetics can help prevent problems before they occur.
- Test correlation data is very useful. Line pull information and field failure reports also help us improve product performance.
- When a problem occurs, provide us as soon as possible with whatever specific data you have. This will assist us in taking prompt corrective action.

Quality products are, in large measure, the result of quality communication. By working together, by opening up channels through which we can talk openly to each other, we will insure the creation of the innovative, reliable, cost effective products that help insure a competitive edge.

QUALITY AND RELIABILITY ASSURANCE

Signetics' Linear Division Quality and Reliability Assurance Department is involved in all stages of the production of our Linear ICs:

- Product Design and Process Development
- Wafer Fabrication
- Assembly
- Inspection and Test
- Product Reliability Monitoring
- Customer liaison

The result of this continual involvement at all stages of production enables us to provide feedback to refine present and future designs, manufacturing processes, and test methodology to enhance both the quality and reliability of the products delivered to our customers.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 5×10^5 amps/cm^2. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. All circuit designs are computer-checked using the latest CAD software for adherence to design rules. Simulations are performed for functionality and parametric performance over the full operating ranges of voltage and temperature before going to production. These steps allow us to meet device specifications not only the first time, but also every time thereafter.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to insure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees.

RELIABILITY MEASUREMENT PROGRAMS

Signetics has developed comprehensive product and process qualification programs to assure that its customers are receiving highly reliable products for their critical applications. Additionally, ongoing reliability monitoring programs, SURE III and Product Monitor, sample standard production product on a regularly established basis (see Table I below).

DESCRIPTION OF STRESSES

SHTL — Static High Temperature Life: SHTL stressing applies static DC bias to the device. This has specific merit in detecting ionic contamination problems which require continuous uninterrupted bias to drive contaminants to the silicon surface. DHTL stressing is not as effective in detecting such problems because the bias continuously changes, intermittently generating and healing the problem.

HTSL — High Temperature Storage Life: This stress exposes the parts to elevated temperatures (150°C – 175°C) with no applied bias.

THBS — Biased Temperature-Humidity, Static: This accelerated temperature and humidity bias stress is performed at 85°C and 85% relative humidity (85°C/85% RH).

TMCL — Temperature Cycling, Air-to-Air: The device is cycled between the specified upper and lower temperature without power in an air or nitrogen environment. Normal temperature extremes are −65°C and +150°C with a minimum 10 minute dwell and 5 minute transition per Mil-STD-883C, Method 1010.5, Condition C. This is a good test to measure the overall package to die mechanical compatibility, because the thermal expansion coefficients of the plastic are normally very much higher than those of the die and leadframe.

PPOT — Pressure Pot: This stress exposes the devices to saturated steam at elevated temperature and pressure. The standard condition is 20 PSIG which occurs at a temperature of 127°C and 100% RH. The stress is used to test the moisture resistance of plastic encapsulated devices. Because the steam environment has an unlimited supply of moisture and ample temperature to catalyze thermally activated events, it is effective at detecting corrosion problems, contamination in-

Table I. RELIABILITY ASSURANCE PROGRAMS

RELIABILITY FUNCTION	TYPICAL STRESS	FREQUENCY
New Process Qualification	High Temperature Operating Life Biased Temperature-Humidity, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each new wafer fab process
New Product Qualification	High Temperature Operating Life Biased Temperature-Humidity, Static High Temperature Storage Life Pressure Pot Temperature Cycle Electrostatic Discharge Characterization	Each new product
SURE III	High Temperature Operating Life Biased Temperature-Humidity, Static High Temperature Storage Life Pressure Pot Temperature Cycle Thermal Shock	Each fab process family, every four weeks
Product Monitor	Pressure Pot Thermal Shock	Each package type and technology family at each assembly plant, every week

duced leakage problems, and general glassivation stability and integrity.

TMSK — Thermal Shock, Liquid-to-Liquid: Similar to TMCL, however, heating and cooling are done by immersing the units in hot and cold inert liquid. Temperature extremes are −65°C to +150°C with a minimum 5 minute dwell and less than 10 second transition per Mil-STD-883C, Method 1011.4, Condition C. Since heat transfer by conduction is generally much faster than by convection, the liquid-based thermal shock causes more rapid temperature changes in the part.

PRODUCT QUALIFICATION

Linear products are subjected to rigorous qualification procedures for all new products or redesigns to current products. Qualification testing consists of:

- High Temperature Operating Life: T_J = 150°C, 1000 hours, static bias
- High Temperature Storage Life: T_J = 175°C, 1000 hours, unbiased
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static bias
- Pressure Cooker: 20 psig, 127°C, 168 hours, unbiased
- Temperature Cycle: −65°C to +150°C, 500 cycles, 10 minute dwell, air to air, unbiased

Formal qualification procedures are required for all new or changed products, processes, and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

ONGOING RELIABILITY ASSESSMENT PROGRAMS

The SURE Program

The SURE (Systematic and Uniform Reliability Evaluation) program audits products from each of Signetics Linear Division's process families: Bipolar Junction, Single Layer Metal, Dual Layer Metal, Gold-Doped and Schottky; Oxide Isolated and ACMOS, under a variety of accelerated stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The Audit Program

Samples are selected from each process family every four weeks and are subjected to each of the following stresses:

- High Temperature Operating Life: T_J = 150°C, 1000 hours, static bias
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static bias
- Pressure Cooker: 20 psig, 127°C, 72 hours, unbiased
- Thermal Shock: −65°C to +150°C, 300 cycles, 5 minute dwell, liquid-to-liquid, unbiased
- Temperature Cycling: −65°C to +150°C, 1000 cycles, 10 minute dwell, air-to-air, unbiased

The Product Monitor Program

In addition, each Signetics assembly plant performs Pressure Cooker and Thermal Shock SURE Product Monitor stresses on a weekly basis on each molded package by pin count per the same conditions as the SURE Program.

Product Reliability Reports

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms, and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

Reliability Engineering

In addition to the product performance monitors encompassed in the Linear SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

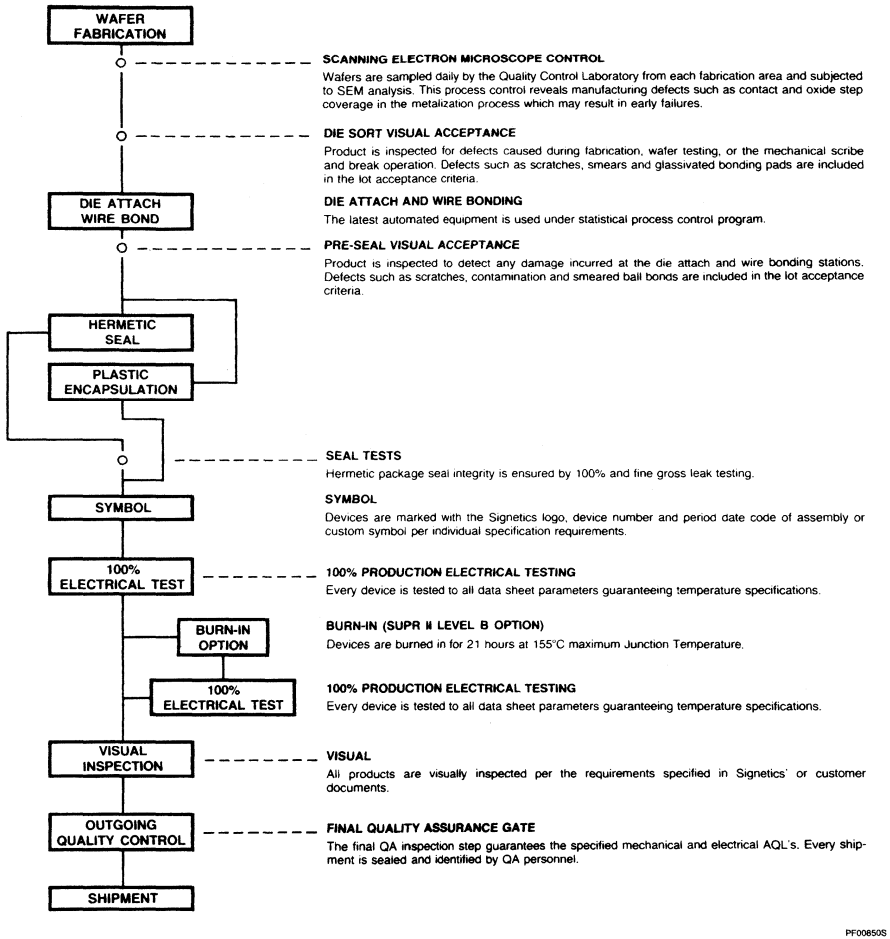
- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities, and subcontractors.
- Device or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in some evaluation programs.

Failure Analysis

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional, and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

LINEAR DIVISION LINEAR PROCESS FLOW



SIGNETICS' MANUFACTURING FACILITIES

Signetics, as part of a multinational corporation, utilizes manufacturing facilities for wafer fabrication, package assembly, and test in three states and three overseas countries as shown in Table II. All wafer fabrication is performed in Signetics operated fabs which report to the Vice President of Die Manufacturing Operations (DMO) in Sunnyvale. Similarly, Signetics Assembly operations in Utah, Korea, and Thailand, report to the Vice President of Assembly Manufacturing Operations (AMO). Assembly subcontractors, Pebei and Anam, are scheduled and controlled through the AMO organization. Assembly subcontractors process all product to Signetics' specifications and materials. Signetics has on-site quality assurance personnel at each subcontractor to audit assembly processes and procedures.

All Signetics Linear products are electrically tested in Signetics operated facilities. These facilities report to the manufacturing organization (DMO or AMO) operating the facility at which they are located.

Table II. Signetics' Linear Product Manufacturing Facilities

WAFER FABRICATION FACILITIES		
Designation	**Location**	**Process Families**
Fab 01	Sunnyvale, California	Bipolar Junction Isolated
Fab 09	Orem, Utah	Bipolar Gold Doped
Fab 16	Sunnyvale, California	Oxide Isolated
Fab 21	Orem, Utah	Bipolar Schottky
Fab 22	Albuquerque, New Mexico	ACMOS
ASSEMBLY FACILITIES		
Designation	**Location**	**Package**
SigKor	Seoul, Korea	DIP, SO, and PLCC
SigThai	Bangkok, Thailand	DIP and CERDIP
Orem	Orem, Utah	Military "Jan" Hermetic
Pebei	Kaohsiung, Taiwan	SO
Anam	Seoul, Korea	SO and Metal Can
TEST FACILITIES		
Designation	**Location**	**Package**
TA03	Sunnyvale, California	Wafer Sort, Final Test and Quality Assurance
SigKor	Seoul, Korea	Final Test and Quality Assurance
SigThai	Bangkok, Thailand	Final Test and Quality Assurance
Sacto	Sacramento, California	Military Final Test and Quality Assurance

SYMBOLIZATION INFORMATION

Signetics' Linear Division products are symboled with the following information on each package:

- Signetics' Logo
- Product Identification and Package Designator
- Traceability Code*
- Assembly Date and Plant Codes*
- Product Revision Level*
- SUPR II B Processing Code (if applicable)

* May appear on the backside of SO 8, 14 & 16 lead packages due to space limitations on topside symbol.

Example:

S NE5534N line 1
FBW5491 line 2
8901VCB line 3

Line 1:
S = Signetics' Logo
NE5534 = Product type designation
N = Package type:
N = Dual-in-Line Plastic
F = Dual-in-Line CerDip
D = Small Outline (SO) Surface Mount
A = Plastic Leaded Chip Carrier (PLCC)
E or H = Metal Header

Line 2:
FBW5491 = 7 character Traceability Code assigned to each Assembly Lot which maintains product traceability back to the Wafer Fabrication.
(May be truncated on SO-8 and metal headers.)
Line 3:
8901 = Assembly Date Code (YYWW) specifies the year (YY) (YYWW) and week number (WW) that begins the 4 week assembly period during which the product was manufactured. Thus, 8901 indicates that the product was packaged during the first four weeks of 1989. The first digit of the year may be omitted on some packages: 901.

V = Assembly Plant Code which indicates the assembly facility in which the finished product was packaged.
Assembly Plants Codes are:
V = Signetics Bangkok, Thailand
K = Signetics Seoul, Korea
B = Philips Kaohsiung, Taiwan
L = Anam Seoul, Korea
C = Product Revision Level
B = SUPR II B Burn-in Processing Code (if present)
indicates that the product was processed through 100% SUPR II B Burn-in for 21 hours under biased operation at a junction temperature (Tj) of 155°C

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and D.C. lines.

DEVICE DATA

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AN164
Explanation of Noise

Application Note

INTRODUCTION TO NOISE

Since fabrication techniques in the integrated circuit industry have improved so tremendously in the past few years, input offset voltages and bias currents are being minimized and noise parameters (whether measured at the output or referred to the input) have become a major source of concern. Reducing noise by improved process techniques and by use of peripheral component control will be the thrust of this application as a secondary effort, in understanding the noise components themselves.

An inspection of industry specifications show several methods of rating amplifier noise performance.

1. Output signal-to-noise ratio.
2. Output noise level (with specified loads and bandwidth).
3. Output noise level referenced to normal operating level.
4. Equivalent input noise (at a specified gain, source impedance and bandwidth).
5. Noise figure.

BASIC NOISE PROPERTIES

Noise, for purposes of this discussion, is defined as any signal appearing in an op amp's output that could not have been predicted by DC and AC input error analysis. Noise can be random or repetitive, internally or externally generated, current or voltage type, narrow-band or wide-band, high frequency or low frequency; whatever its nature, it can be minimized.

The first step in minimizing noise is source identification in terms of bandwidth and location in the frequency spectrum; some of the more common sources are shown in Figure 1. Some observations to be made from Figure 1 are that noise is present from DC to VHF from sources which may be identified in terms of bandwidth and frequency; noise source bandwidths overlap, making noise a composite quantity at any given frequency. Most externally-caused noise is repetitive rather than random and can be found at a definite frequency. Noise effects from external sources must be reduced to insignificant levels to realize the full performance available from a low noise op amp.

EXTERNAL NOISE SOURCES

Since noise is a composite signal, the individual sources must be identified to minimize their effects. For example, 60Hz power line pickup is a common interference noise appearing at an op amp's output as a 16ms sine wave. In this and most other situations, the basic tool for external noise source frequency characterization is the oscilloscope sweep rate setting. Recognizing the oscilloscope's potential in this area, there are several preamplifiers available with variable bandwidth and frequency which allow quick noise source frequency identification. Another basic identification tool is the simple low-pass filter, as shown in Figure 2, where the bandpass is calculated by:

$$f_O = \frac{1}{2\pi RC} \qquad (1)$$

With such a filter, measurement bandpass can be changed from 10Hz to 100Hz ($C = 4.7\mu F$ to 470pF), attenuating higher frequency components while passing frequencies of interest. Once identified, noise from an external source may be minimized by the methods outlined in Table 1, the external noise chart.

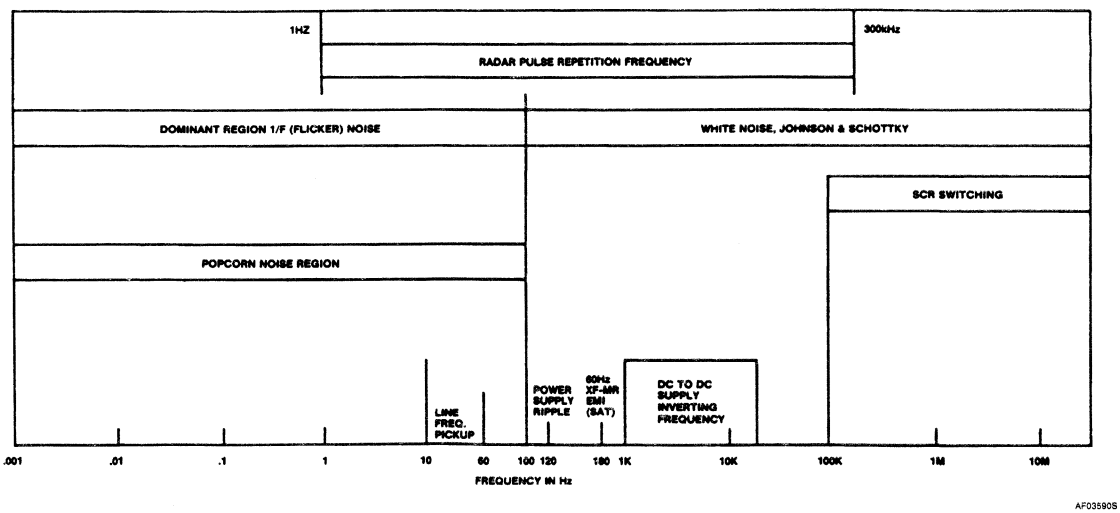


Figure 1. Frequency Spectrum of Noise Sources Affecting Operational Amplifiers and Low Noise Preamplifiers

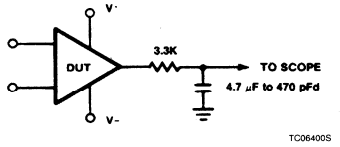


Figure 2. Noise Frequency Analysis RC Low-Pass Filter

POWER SUPPLY RIPPLE

Power supply ripple at 120Hz is not usually thought of as noise, but it should be. In an actual op amp application, it is quite possible to have a 120Hz noise component that is equal in magnitude to all other noise sources combined, and, for this reason, it deserves a special discussion.

To be negligible, 120Hz ripple noise should be between 10nV and 100nV referred to the input of an op amp. Achieving these low levels requires consideration of three factors: the op amp's 120Hz power supply rejection ratio (PSRR), the regulator's ripple rejection ratio, and, finally, the regulator's input capacitor size.

PSRR at 120Hz for a given op amp may be found in the manufacturer's data sheet curves of PSRR versus frequency as shown in Figure 3. For the amplifier shown, 120Hz PSRR is about 74dB, and to attain a goal of 100nV referred to the input, ripple at the power terminals must be less than 5mV. Today's IC regulators provide about 60dB of ripple rejection; in this case the regulator input capacitor must be made large enough to limit input ripple to 0.5V.

Externally-compensated low noise op amps can provide improved 120Hz PSRR in high close-loop gain configurations. The PSRR versus frequency curves of such an op amp are shown in Figure 5. When compensated for a closed-loop gain of 1000, 120Hz PSRR is 115dB. PSRR is still excellent at much higher frequencies, allowing low ripple noise operation in exceptionally severe environments.

POWER SUPPLY DECOUPLING

Usually, 120Hz ripple is not the only power supply associated noise. Series regulator outputs typically contain at least 150μV of noise in the 100Hz to 10kHz range, switching types contain even more. Unpredictable amounts of induced noise can also be present on power leads from many sources. Since high frequency PSRR decreases at 20dB/decade, these higher frequency supply noise components must not be allowed to reach the op amp's power terminals. RC decoupling, as shown in Figure 6, will adequately filter most wide-band noise. Some caution must be exercised with this type of decoupling, as load current changes will modulate the voltage as the op amp's supply pins.

POWER SUPPLY REGULATION

Any change in power supply voltage will have a resultant effect referred to an op amp's inputs. For the op amp of Figure 3, PSRR at DC is 110dB (3μV/V) which may be considered as a potential low frequency noise source. Power supplies for low noise op amp applications should, therefore, be both low in ripple and well-regulated. Inadequate supply regulation is often mistaken to be low frequency op amp noise.

When noise from external sources has been effectively minimized, further improvements in low noise performance are obtained by specifying the right op amp, and through careful selection and application of the peripheral components.

Noise voltage, e_n, or more properly, equivalent short-circuit input RMS noise voltage, is simply that noise voltage which would appear to originate at the input of a noiseless amplifier (referring to Figure 4) if the input terminals were shorted. It is expressed in nanovolts per root Hertz (nV/$\sqrt{Hz}$) at specified frequency, or in microvolts (μV) for a given frequency band. It is determined, or measured, by shorting the input terminals, measuring the output rms noise, dividing by amplifier gain, and referencing to the input. Hence the term, equivalent noise voltage. An output bandpass filter of known characteristics is used in

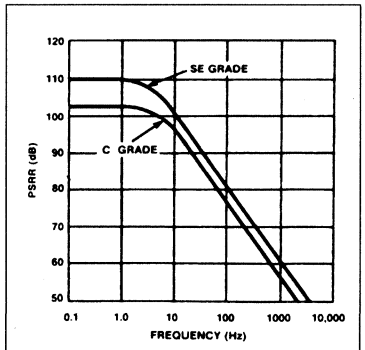


Figure 3. PSRR vs Frequency

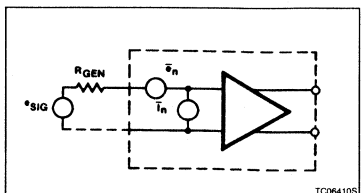


Figure 4. Noise Characterization of Amplifier

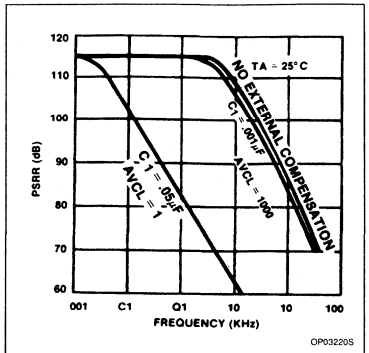


Figure 5. PSRR vs Frequency (Externally-Compensated Device)

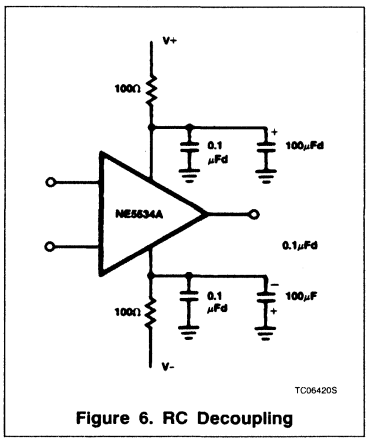


Figure 6. RC Decoupling

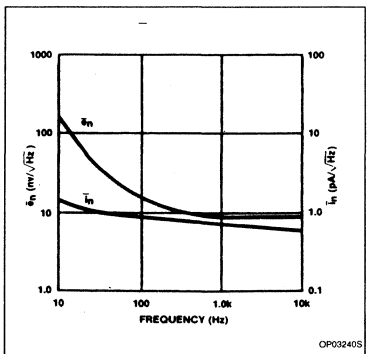


Figure 7. Noise Voltage and Current for an Op Amp

Table 1. External Noise Chart

SOURCE	NATURE	CAUSES	MINIMIZATION METHODS
60Hz Power	Repetitive Interference	Power lines physically close to op amp inputs. Poor CMRR at 60Hz.	Reorientation of power wiring. Shielded transformers.
120Hz Ripple	Repetitive	Inadequate ripple consideration. Poor RSRR at 120Hz.	Thorough design to minimize ripple. RC decoupling at the op amp.
180Hz	Repetitive EMI	180Hz radiated from saturated 60Hz transformers.	Physical reorientation of components. Shielding. Battery power.
Radio stations	Standard AM broadcast through FM	Antenna action anyplace in system.	Shielding. Output filtering. Limited circuit bandwidth.
Relay & switch arcing	High frequency burst at switching rate.	Proximity to amplifier inputs, power lines, compensation terminals, or nulling terminals.	Filtering of HF components. Shielding. Avoidance of ground loops. Arc suppressors at switching source.
Printed circuit board contamination	Random low frequency	Dirty boards or sockets.	Thorough cleaning and humidity sealant.
Radar transmitters	High frequency gated at radar pulse repetition rate.	Radar transmitters from long range surface search to short range navigational especially near airports.	Shielding. Output filtering of frequencies >>PRR.
Mechanical vibration	Random < 100Hz	Loose connections, intermittent metallic contact in mobile equipment.	Attention to connectors and cable conditions. Shock mounting in severe environments.
Chopper frequency noise	Common-mode input current at chopping frequency	Abnormally high noise chopper amplifier in system	Balanced source resistors. Use bipolar input op amps instead.

measurements, and the measured value is divided by the square root of the bandwidth $\sqrt{B}$, if data is to be expressed per unit bandwidth or per root Hertz. The level of $\bar{e}_n$ is not constant over the frequency band; typically it increases at lower frequencies as shown in Figure 7. This increase is $1/f_{NOISE}$ (flicker).

Noise current, i_n, or more properly, equivalent open-circuit RMS noise current, is that noise which occurs apparently at the input of a noiseless amplifier due only to noise currents. It is expressed in picoamps per root Hertz ($pA/\sqrt{Hz}$) at a specified frequency or in nanoamps (nA) in a given frequency band. It is measured by shunting a capacitor or resistor across the input terminals such that the noise current will give rise to an additional noise voltage which is $i_n \times R_{IN}$ (or X_{CIN}). The output is measured, divided by amplifier gain, referenced to input, and that contribution known to be due to $\bar{e}_n$ and resistor noise is appropriately subtracted from the total measured noise. If a capacitor is used at the input, there is only $\bar{e}_n$ and $\bar{i}_n$ X_{CIN}. The $\bar{i}_n$ is measured with a bandpass filter and converted to $pA/\sqrt{Hz}$, if appropriate; typically, it increases at lower frequencies for bipolar op amps and transistors, but it increases at higher frequencies for field-effect transistors and Bi-FET/Bi-MOS op amps.

Noise Figure, NF, is the logarithm of the ratio of input signal-to-noise and output signal-to-noise.

$$NF = 10 \log \frac{(S/N)_{in}}{(S/N)_{out}} \quad (2)$$

where: S and N are power or $(\text{voltage})^2$ levels

This is measured by determining the S/N at the input with no amplifier present, and then dividing by the measured S/N at the output with signal source present.

The values of R_{GEN} and any X_{GEN} as well as frequency must be known to properly express NF in meaningful terms. This is because the amplifier $i_n \times Z_{GEN}$ as well as R_{GEN} itself produces input noise. The signal source contains some noise. However, e_{SIG} is generally considered to be noise-free and input noise is present as the thermal noise of the resistive component of the signal generator impedance R_{GEN}. This thermal noise is white in nature as it contains constant noise power density per unit bandwidth. It is easily seen that the $\bar{e}_n^2$ has the units V^2/Hz and that $(\bar{e}_n)$ has the units $V/\sqrt{Hz}$

$$\bar{e}_R^2 = 4kTRB \quad (3)$$

where: T is temperature in °K
R is resistor value in Ω
B is bandwidth in Hz
k is Boltzman's constant

OPERATIONAL AMPLIFIER INTERNAL NOISE OP AMP NOISE SPECIFICATIONS

Most completely specified low noise op amp data sheets specify current and voltage noises in a 1Hz bandwidth and low frequency noise over a range of 0.1Hz to 10Hz. To minimize total noise, a knowledge of the derivation of these specifications is useful. In this section, the reader is provided with an explanation of basic op amp associated random noise mechanisms and introduced to a simplified method for calculating total input-referred noise in typical applications.

RANDOM NOISE CHARACTERISTICS

Op amp associated noise currents and voltages are random. They are aperiodic, not correlated to each other, and have Gaussian amplitude distributions; the highest noise amplitudes having the lowest probability. Gaussian amplitude distribution allows random noises to be expressed as RMS quantities;

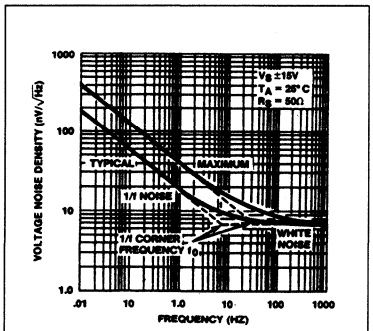


Figure 8. Noise Voltage

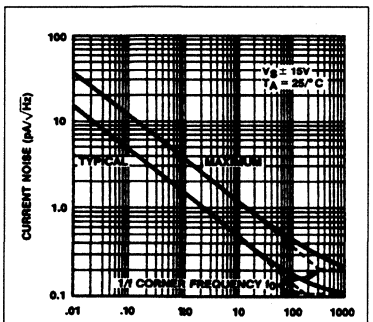


Figure 9. Noise Current

multiplying a Gaussian RMS quantity by six results in a peak-to-peak value that will not be exceeded 99.73% of the time.

The two basic types of op amp associated noises are white noise and flicker noise (I/f). White noise contains equal amounts of power in each Hertz of bandwidth. Flicker noise is different in that it contains equal amounts of power in each decade of bandwidth. This is best illustrated by spectral noise density plots such as in Figures 8 and 9. Above a certain corner frequency, white noise dominates; below that frequency, flicker (I/f) noise is dominant. Low noise corner frequencies distinguish low noise op amps from general purpose devices.

SPECTRAL NOISE DENSITY

To utilize Figures 8 and 9, let us consider the definition of spectral noise density: the square root of the rate of change of mean-square noise voltage (or current) with frequency (Equation 4a).

$$e_n^2 = \frac{d}{df}(E_n)^2 \qquad (4a)$$

$$i_n^2 = \frac{d}{df}(1_n)^2 \qquad (4b)$$

$$E_n = \sqrt{\int_{f_L}^{f_H} e_n^2\, dF} \qquad (5a)$$

$$I_N = \sqrt{\int_{f_L}^{f_H} i_n^2\, dF} \qquad (5b)$$

where e_n, i_n = Spectral noise density
E_n, I_n = Total RMS noise
f_H = Upper frequency limit
f_L = Lower frequency limit

Conversely, the RMS noise value within a given frequency band is the square root of the definite integral of the spectral noise density over the frequency band (Equation 5b). This means that three things must be known to evaluate total voltage noise (E_n) or current noise (I_n): f_H, f_L, and a knowledge of noise behavior over frequency.

WHITE NOISE

White noise sources are defined to have a noise content that is equal in each Hertz of bandwidth, and Equation 5b may be rewritten for white noise sources as:

$$E_n(\omega) = e_n\sqrt{f_H - f_L}$$
$$I_n(\omega) = i_n\sqrt{f_H - f_L} \qquad (6)$$

It is therefore convenient to express spectral noise density in $V/\sqrt{Hz}$ or $A/\sqrt{Hz}$ where $f_H - f_L = 1Hz$. When $f_H \geq 10f_L$, the white noise expressions may be further reduced to:

$$E_n(\omega) = e_n\sqrt{f_H}$$
$$I_n(\omega) = i_n\sqrt{f_H} \qquad (7)$$

FLICKER NOISE & WHITE NOISE

Since flicker noise content is equal in each decade of bandwidth, total flicker noise may be calculated if noise in one decade is known. The 0.1Hz to 1Hz decade noise content (K) is widely used for this purpose because the white noise contribution below 10Hz is usually negligible.

$$E_n(f) \cong K\sqrt{\frac{1}{f}}, \quad I_n(f) \cong K\sqrt{\frac{1}{f}} \qquad (8)$$

When substituted in Equation 3, the expressions may be rewritten to:

$$E_n(f) = K\sqrt{I_n\left(\frac{f_H}{f_L}\right)} \qquad (9)$$

$$I_n(f) = K\sqrt{I_n\left(\frac{f_H}{f_L}\right)}$$

When corner frequencies are known, simplified expressions for total voltage and current noise, (E_N and I_N), may be written:

$$E_N(f_H - f_L) = e_n\sqrt{f_{CE}\, I_n\left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \qquad (10)$$

$$I_N(f_H - f_L) = i_n\sqrt{f_{CI}\, I_n\left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \qquad (11)$$

where:

e_n = White noise voltage in a 1Hz bandwidth
i_n = White noise current in a 1Hz bandwidth
f_{CE} = Voltage noise corner frequency
f_{CI} = Current noise corner frequency
f_H = Upper frequency limit
f_L = Lower frequency limit

The two most important internally-generated noise minimization rules are: limit the circuit bandwidth, and use operational amplifiers with low corner frequencies.

NOISE SUMMATION

In the spectral density discussions, the concepts of white noise and flicker noise were introduced. In Figure 10, the complete input-referred op amp noise model, internal white and flicker noise sources are combined into three equivalent input noise generators, E_n, I_{N1} and I_{N2}. The noise current generators produce noise voltage drops across their respective source resistors, R_{S1} and R_{S2}. The source resistors themselves generate thermal noise voltages, E_{t1} and E_{t2}. Total RMS input-referred voltage noise, over a given bandwidth, is the square root of the sum of the squares of the five noise voltage sources over that bandwidth.

$$E_{NT}(f_H - f_L) = \sqrt{E_N^2 + (I_{N1}{\cdot}R_{S1})^2 + (I_{N2}{\cdot}R_{S2})^2 + E_{t1}^2 + E_{t2}^2} \qquad (12)$$

Explanation of Noise

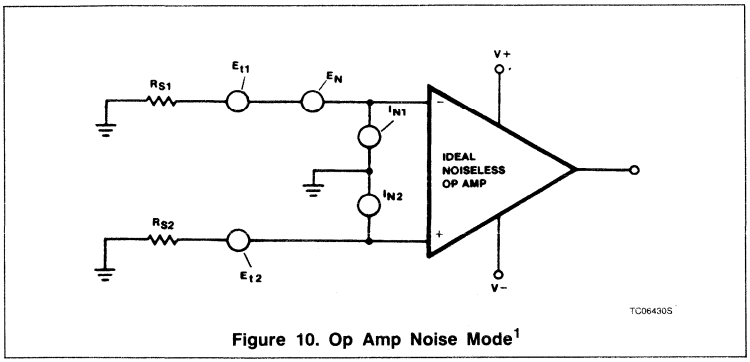


Figure 10. Op Amp Noise Mode[1]

THERMAL NOISE

Thermal (Johnson) noise is a white noise voltage generated by random movement of thermally-charged carriers in a resistance; in op amp circuits this is the type of noise produced by the source resistances in series with each input. Its RMS value over a given bandwidth is calculated by:

$$E_t = \sqrt{4kTR\,(f_H - f_L)} \qquad (13)$$

Where:

k = Boltzman's constant = 1.38×10^{-23} joules/°K
T = Absolute temperature, °K
R = Resistance in Ω
f_H = Upper frequency limit in Hz
f_L = Lower frequency limit in Hz

At room temperature, Equation 13 simplifies to:

$$E_t = 1.28 \times 10^{-10}\sqrt{R(f_H - f_L)} \qquad (14)$$

To minimize thermal noise (E_{t1} and E_{t2}) from R_{S1} and R_{S2}, large source resistors and excessive system bandwidth should be avoided.

Thermal noise is also generated inside the op amp, principally from r_{bb}, the base-spreading resistances in the input stage transistors. These noises are included in E_N, the total equivalent input voltage noise generator.

SHOT NOISE

Shot noise (Shottky noise) is a white noise current associated with the fact that current flow is actually a movement of discrete charged particles (electrons). In Figure 10, I_{N1} and I_{N2} above the 1/f frequency are shot noise currents which are related to the amplifier's DC input bias currents:

$$I_{SH} = \sqrt{2qI_{BIAS}\,(f_H - f_L)} \qquad (15)$$

where:

I_{SH} = RMS shot noise value in amps
q = charge of an electron
= 1.602×10^{-19} Coulombs
I_{BIAS} = Bias current in amps
f_H = Upper frequency limit in Hz
f_L = Lower frequency limit in Hz

At room temperature, Equation 15 simplifies to:

$$I_{SH} = 5.64 \times 10^{-10}\sqrt{I_{BIAS}\,(f_h - f_L)} \qquad (16)$$

Shot noise currents also flow in the input stage emitter dynamic resistances, (r_e), producing input noise voltages. These voltages, along with the r_{bb}, thermal noise, make up the white noise portion of E_N, the total equivalent input noise voltage generator.

FLICKER NOISE

In limited bandwidth applications, flicker (1/f) noise is the most critical noise source. An op amp designer minimizes flicker noise by keeping current noise components in the input and second stages from contributing to input voltages noise. Equation 17 illustrates this relationship:

$$\frac{i_n \text{ second stage}}{g_M \text{ first stage}} = e_n \text{ input} \qquad (17)$$

Another critical factor is corner frequency. For minimum noise, the current and voltage noise corner frequencies must be low; this is crucial. As shown in Figure 11, low noise corner frequencies distinguish low noise op amps from ordinary industry-standard 741 types.

POPCORN NOISE

Popcorn noise (burst noise) is a momentary change in input bias current usually occurring below 100Hz, and is caused by imperfect semiconductor surface conditions incurred during wafer processing. Minimization of this problem can be accomplished through careful surface treatment, general cleanliness, and a special three-step process known as "Triple Passivation".

Op amp manufacturers face a difficult decision in dealing with popcorn noise. Through careful low noise processing, it can be significantly reduced in almost all devices; alternatively, the processing may be relaxed, and finished devices must be individually tested for this parameter. Special noise testing takes valuable labor time, adds significant amounts to manufacturing cost, and ultimately increases the price a customer has to pay.

TOTAL NOISE CALCULATION

With data sheet curves and specifications, and a knowledge of source resistance values, total input-referred noise may be calculated

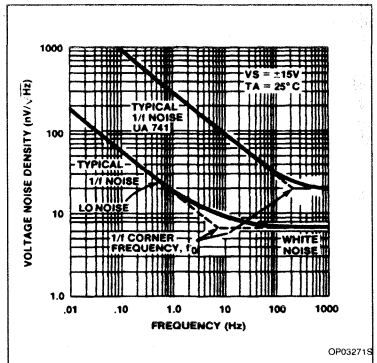


Figure 11. Noise Voltage Comparison

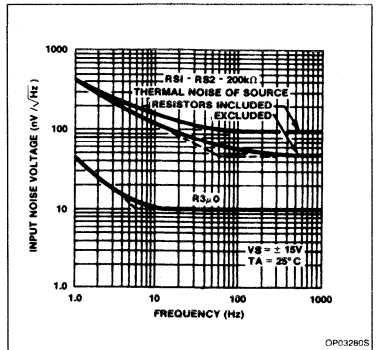


Figure 12. Input Noise Voltage vs Frequency

for a given application. To illustrate the method, noise information from a data sheet is reproduced in Figure 12. The first step is to determine the current and voltage noise corner frequencies so that the E_N and I_N terms of Equation 12 may be calculated using Equations 10 and 11.

CORNER FREQUENCY DETERMINATION

In the input shot noise versus frequency curves of Figure 12, it may be seen that voltage noise ($R_S = 0$) begins to rise at about 10Hz. Lines projected from the horizontal (white noise) portion and sloped (flicker noise) portion intersect at 6Hz, the voltage noise corner frequency (f_{CE}). In the center curve, excluding thermal noise multiplied by 200Ω is plotted as a voltage noise. Lines projected from the horizontal portion and sloped portions intersect at 60Hz, the current noise corner frequency (f_{CI}). Equations 10 and 11 also require e_n and i_n for calculation of E_N and I_N. To find e_n and i_n, use the data sheet specification a decade or more above the respective corner frequencies; in this case e_n is 9.6 $nV/\sqrt{Hz}$ (1000Hz), and i_n is 0.12 $pA/\sqrt{Hz}$ (1000Hz).

BANDWIDTH OF INTEREST

To be summed correctly, each of the five noise quantities must be expressed over the same bandwidth, $(f_H - f_L)$. At this time, assume f_H to be the highest frequency component that must be amplified without distortion. Note that e_n, i_n, corner frequencies and bandwidth are independent of actual circuit component values. When doing noise calculations for a large number of circuits using the same op amp, these numbers only have to be calculated once.

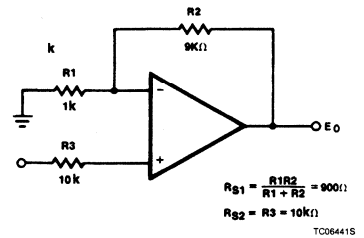
TYPICAL APPLICATION EXAMPLE

Figure 13a shows a typical ×10 gain stage with a 10kΩ source resistance. In Figure 13b, the circuit is redrawn to show five noise voltage sources. To evaluate total input-referred noise, the values of each of the five sources must be determined.

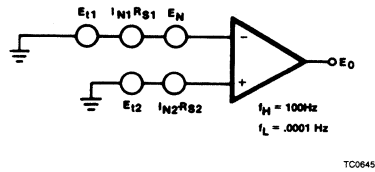
$e_n = 9.6nV/\sqrt{Hz}$
$I_n = 0.12pA/\sqrt{Hz}$
$f_{CE} = 6Hz$
$f_{CI} = 60Hz$

Using Equation 14: $E_t = \sqrt{4kTR(f_H - f_L)}$

$E_{t1} = 1.28 \times 10^{10}\sqrt{(900\Omega)(100Hz)}$
$= 0.4\mu V_{RMS}$
$E_{t2} = 1.28 \times 10^{10}\sqrt{(10k\Omega)(100Hz)}$
$= 0.128\mu V_{RMS}$



a. Noise Analysis Circuit



b. Noise Analysis Equivalent Circuit

Figure 13

Next, Calculate I_N Using Equation 11

$$I_N = i_n\sqrt{f_{CI}\ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$$

$$= 0.12pA\sqrt{60\ln\left(\frac{100Hz}{0.01Hz}\right) + (100 - 0.01)}$$

$$= 3.066pA_{RMS}$$

and:

$I_{N1} \cdot R_{S1} \geq 3.066pA\ (900\Omega) = 0.0027\mu V_{RMS}$

$I_{N2} \cdot R_{S2} = 3.066pA\ (10k\Omega) = 0.0306\mu V_{RMS}$

Finally, E_N from Equation 10

$$E_N = e_n\sqrt{f_{CE}\ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$$

$$= 9.6nV\sqrt{6\ln\left(\frac{100Hz}{0.01Hz}\right) + (100 - 0.01)}$$

$$= 0.120\mu V_{RMS}$$

Substituting in Equation 12

$$E_{NT}\ (f_H - f_L) =$$

$$\sqrt{E_N^2 + I_{N1}^2R_{S1}^2 + (I_{N2}R_{S2})^2 + E_{t1}^2 + E_{t2}^2}$$

$$= \sqrt{(0.120\mu V)^2 + (0.0027\mu V)^2 + (0.0306\mu V)^2 + (0.04\mu V)^2 + (0.128\mu V)^2}$$

$$= 0.183\mu V_{RMS}$$

Using the factor of 6, total input-referred noise = $1.1\mu V_{P-P}$ (0.01Hz to 100Hz).

741 CALCULATION EXAMPLE

The preceding calculation determined total noise in a given bandwidth using a low noise op amp. To place this level of performance into perspective, a calculation using the industry-standard 741 op amp in the circuit of Figure 13 is useful. Once again the starting point is corner frequency determination, using the data sheet curves:

$f_{CE} = 200Hz$; $f_{CI} = 2kHz$;

$e_n = 20nV/\sqrt{Hz}$; $i_n = 0.5pA/\sqrt{Hz}$.

Using these corner frequencies and noise magnitudes, E_N and I_N are calculated to be $0.88\mu V_{RMS}$ and $68pA_{RMS}$, respectively. Multiplying this noise current by the source resistance gives terms 2 and 3 of Equation 12 as shown below.

$$E_{NT}\ (f_H - f_L) =$$

$$\sqrt{E_N^2 + I_{N1}^2R_{S1}^2 + I_{N2}^2R_{S2}^2 + E_{t1}^2 + E_{t2}^2} \quad (12)$$

Substituting in Equation 12

$$= \sqrt{(0.88\mu V)^2 + (0.061\mu V)^2 + (0.68\mu V)^2 + (0.4\mu V)^2 + (0.128\mu V)^2}$$

$$= 1.12\mu V_{RMS}$$

Total input-referred noise = $6.7\mu V_{P-P}$ (0.01Hz to 100Hz).

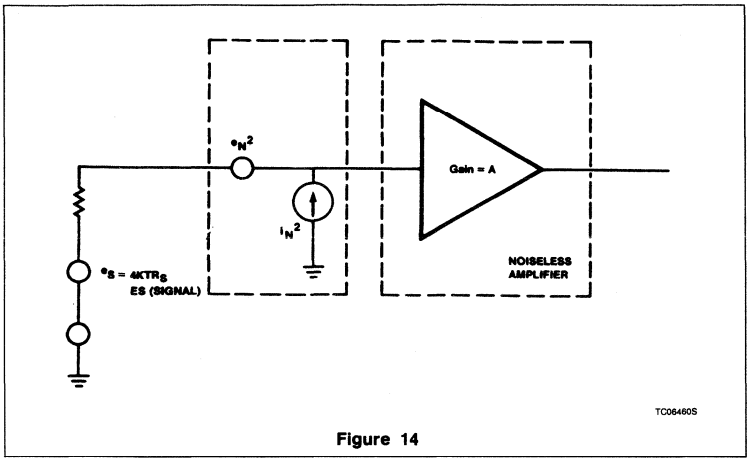


Figure 14

This is 5.9 times that of the low noise op amp example.

The calculation examples illustrate three rules for minimizing noise in operational amplifier applications:

RULE 1. Use an op amp with low corner frequencies.

RULE 2. Keep source resistances as low as possible.

RULE 3. Limit circuit bandwidth to signal bandwidth.

NOISE PERFORMANCE

This segment shall be concerned with determining the signal-to-noise characteristics and the noise figure of amplifiers.

The amplifier noise is composed of thermal noise generated in the base resistance shot noise caused by the arrival of discrete charges at diode junction and 1/f noise.

For simplification, these noise sources can be combined and the amplifier modeled by a noise source and a noiseless amplifier as in Figure 14.

e_n = Amplifier's equivalent mean square noise voltage/$\sqrt{Hz}$

i_n = Amplifier's equivalent mean square noise current/$\sqrt{Hz}$

The total output noise can now be computed by Equation 8:

$$e_t = (e_n^2 + i_n^2 R_S^2 + 4kTR_S)^{1/2} B^{1/2} A_{RMS} \text{Volts} \quad (8)$$

Assuming R_S small compared to amplifier input.

* See Note 1.

If we now compare the total output noise to the output signal, A – E_S, we find the output signal-to-noise ratio.

$$S/N = \frac{E_s}{(e_n^2 + i_n^2 R_S^2 + 4kTR_S)^{1/2} B^{1/2}} \quad (13)$$

The denominator of the S/N ratio is the total output noise divided by the midband gain or the equivalent input noise as shown on the NE542 specification sheet.

$$E_{IN} = (e_n^2 + i_n^2 R_S^2 + 4kTR_S)^{1/2} B^{1/2} \text{RMS Volts} \quad (14)$$

The S/N ratio may now be computed independently of the amplifier gain. However, the gain should be chosen to maintain linear operation of the amplifier. For example, if the input signal to the NE542 is 400μV_{RMS} from a source resistance of 680Ω with a bandwidth of 100Hz to 10kHz, the S/N ratio becomes, in dB:

$$S/N = 20 \log \frac{400\mu V}{0.77\mu V} = 54.3dB$$

An amplifier gain of 68dB yields an output signal voltage of $1V_{RMS}$.

For an input signal of $10mV_{RMS}$, 40dB of gain, and $1V_{RMS}$ output, the NE542 gives a S/N ratio:

$$S/N = 20 \log \frac{10{,}000}{0.77} = 82.3dB$$

Another popular figure of merit for measuring the noise performance of an amplifier is noise figure. We first define noise factor (F) as

$$F = \frac{\text{Noise power input (Total)}}{\text{Thermal noise power}}$$

In terms of voltage this can be expressed as:

$$F = \frac{4kTR_S + (e_n^2 + i_n^2 R_S^2)}{4kTR_S} = 5.34, \quad R_S = 680\Omega \quad (15)$$

The noise figure is now defined as:

$$NF = 10 \log F \text{ (dB)}$$

or

$$NF = 10 \log \frac{4kTR_S + e_n^2 + i_n^2 R_S^2}{4kTR_S} \text{(dB)} \quad (16)$$

Table 2. Spectral Voltage and Current Noise Densities

	μA741	5534	LF357	NE542	LM387
e_n (nV/$\sqrt{Hz}$)	40	4	12	7	9
i_n (pA/$\sqrt{Hz}$)	0.25	0.6	0.01	0.25	0.7
e_n f_{CE} (Hz)	200	90	50	800	850
i_n f_{CI} (Hz)	1.5k	200	1	700	2

NOTES:

1. The current spectral noise is omitted for the LF series since current noise levels in JFET devices are insignificant.
2. The spectral current noise for the LM387 is relatively linear over the frequency spectrum of 100Hz to 10kHz and is not specified below 100Hz.

A noiseless amplifier will, therefore, have a noise figure of "0" dB. Although the bandwidth has been eliminated from this calculation, it is still an influencing factor on the noise figure since the value of e_n and i_n will be dependent on the bandwidth of interest. This is especially true if I/f or high frequency noise is in this bandwidth.

From Figures 15 and 16 we can calculate the noise figure. For the NE542, the noise figure for 100Hz to 10Hz, 3dB bandwidth (15.7kHz equivalent noise bandwidth) and a source resistance of 5kΩ is:

$$NF = 10 \log \left(1 + \frac{e_n^2 + i_n^2 R_S^2}{4kTR_S} \right) \quad (17)$$

$$NF = 10 \log \left(1 + \frac{(7)^2 \times 10^{-18} + (0.25)^2 \times 10^{-24} \times R_S^2}{75 \times 10^{-18}} \right)$$

$$= 10 \log \frac{4 \times 1.38 \times 10^{-23} \times 300^\circ K \times R_S}{}$$

$= 7.27$ @ $R_S = 680\Omega$

$= 2.07$ @ $R_S = 5k\Omega$

$= 1.25$ @ $R_S = 10k\Omega$

To this point, the discussion has been limited to flat band response and no mention of the effect of equalization networks has been made. In instances where the gain of the amplifier is changing significantly across the frequency band of interest, as is the case for NAB and RIAA equalization, the noise performance is significantly improved.

The following table lists the spectral voltage and current noise densities and the respective corner frequencies for several different operational amplifiers and low noise preamplifiers.

where

I_N = total current noise over a specified bandwidth.

E_N = total voltage noise over a specified bandwidth.

E_{ti} = thermal (Johnson) noise of the source resistance.

*R_S = equivalent input source (or generator) resistance.

NOTE:

1. If R_S is a complex function, Z_S, then this function must be calculated for the R_{SS} mean of each bandwidth considered. For example, the input is a capacitor in parallel with a resistor; the input impedance is therefore:

$$Z_{IN} = \frac{R}{1 + jwCR}$$

Therefore as the frequency varies, the absolute value of Z_{IN} will vary and will affect the $I_N R_S$*, input noise value.

GENERAL EQUATIONS

Total Spectral Voltage Noise

$$E_N (f_H - f_L) = e_n \sqrt{f_{CE} I_n \left(\frac{f_H}{f_L} \right) + (f_H - f_L)} \quad (18)$$

Total Spectral Noise Current

$$I_N (f_H - f_L) = i_n \sqrt{f_{CI} I_n \left(\frac{f_H}{f_L} \right) + (f_H - f_L)} \quad (19)$$

Thermal

$E_t = 4\ kTR\ (f_H - f_L)$

$k = 1.38 \times 10^{-23}$ joules/°K

T = absolute temp in °K

R = Ω

$f_t = 1.28 \times 10^{-10} \sqrt{R(f_H - f_L)}$ at room temperature (20)

Shot at Room Temperature

$$I_{SH} = 5.64 \times 10^{-10} \sqrt{I_{BIAS} (f_H - f_L)} \quad (21)$$

Total Noise*

$$\left| ENT \right|_{f_L}^{f_H} = \sqrt{E_n^2 + (I_N R_{S1})^2 + I_{N2} R_{S2}^2 + E_{t1}^2 + E_{t2}^2}$$

Example:

In order to determine the total noise of any device the following basic procedures can be used:

1. Determine the spectral voltage noise value $\bar{e}_n$ and the 3dB corner frequency. (If the value is not listed, but a curve given, the spectral noise value will be that value above the 3dB corner frequency on the flat portion of the curve.)

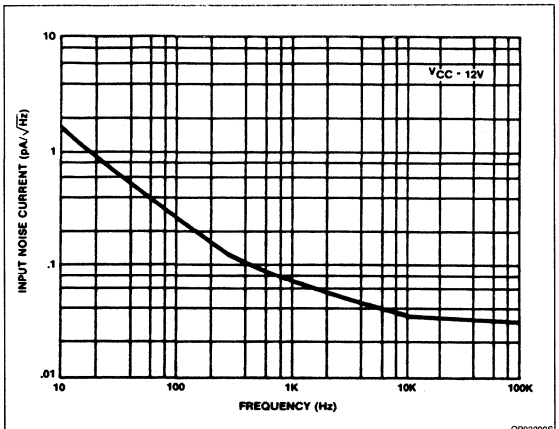


Figure 15. Input Noise Current vs Frequency

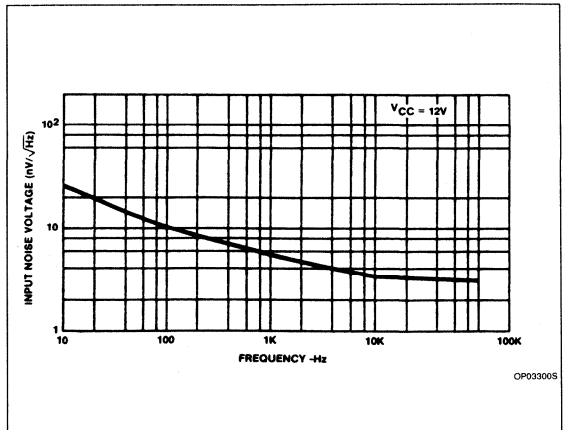


Figure 16. Input Noise Voltage vs Frequency

2. Determine the spectral current noise value $\overline{i_n}$ and the 3dB corner frequency. (The same note holds true as for the spectral voltage noise, except that the corner frequencies are generally not the same.)
3. Determine the thermal noise of the input port source resistances by using the basic equal at room temperature of $E_T = 1.28 \times 10^{-10} \sqrt{R}/\sqrt{Hz}$
4. Using Equations 1, 2, and 4 and using Figure 1 as a basic block, we then can determine the total current and voltage noise at the input ports.
5. Employing Equation 5 we can then determine the total R_{SS} voltage noise referred to the input of the amplifier.
6. If the closed-loop gain of the system is known, then the total output noise is then $E_{Nout} = E_{Nin} \times A_{CL}$

Given: From Table 2, the NE5534 operating over the range of 10Hz to 1kHz and 1kHz to 10kHz, with R_S = 10kΩ: determine total input noise over each bandwidth.

$$E_N(f_H - f_L) = e_n \sqrt{f_{CE} \ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \quad (18)$$

$$I_N(f_H - f_L) = i_n \sqrt{f_{CI} \ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \quad (19)$$

$$E_t = 1.28 \times 10^{-10} \sqrt{R\,(f_H - f_L)} \quad (20)$$

$$\left| \text{ENT} \right|_{f_L}^{f_H} = \sqrt{(E_n)^2 + (I_{N1} R_{S1})^2 + (E_t)^2} \quad (21)$$

For the first band (10Hz to 1kHz):

$$E_n = 4 \times 10^{-9} \sqrt{90\ 1n\ (100) + (990)}$$
$$= 0.15\mu V_{RMS}$$

$$I_N R_S = 0.6 \times 10^{-12} \sqrt{200\ 1n\ (100) + (990) \times (10^4)}$$
$$= 0.26\mu V_{RMS}$$

$$E_T = 1.28 \times 10^{-8} \sqrt{990} = 0.4\mu V_{RMS}$$

$$E_{TH}{}_{10}^{1000} = \sqrt{(E_N)^2 + (I_N R_S)^2 + E_T{}^2}$$
$$= 0.50\mu V_{RMS}$$

Using the factor of 6:

$f_{NOISE\ P\text{-}P}$ = 3.00$\mu V_{P\text{-}P}$ will never be exceeded in 99.73% of all cases.

For the second band (1kHz to 10kHz):

$$*E_N = 4 \times 10^{-9} \sqrt{9000} = 0.38\mu V_{RMS}$$

$$*I_N R_S = 0.6 \times 10^{-12} \sqrt{9000 \times (10^4)}$$
$$= 0.58\mu V_{RMS}$$

$$E_T = 1.28 \times 10^{-10} \sqrt{10^4 (9000)}$$
$$= 1.21\mu V_{RMS}$$

NOTE:
* For frequencies above 1kHz only WHITE noise is a consideration.

$$\left| E_{TH} \right|_{f_{1kHz}}^{f_{10kHz}} = \sqrt{(0.38)^2 + (0.57)^2 + (1.21)^2 \mu V_{RMS}}$$

$$\text{RSS} \left| E_{TH} \right|_{f_{1kHz}}^{f_{10kHz}} = \sqrt{1.39\mu V_{RMS}}$$

E_{THmax} = 8.34$\mu V_{P\text{-}P}$

CONCLUSION

The designer should look at the previous application note as a reasonable approach to determine system noise levels. The variations of parameters, such as resistance values, temperature and bandwidth, are controllable by design procedure; however, the parametric variations of the monolithic op amps are controlled by the IC manufacturer. Signetics manufactures a wide variety of operational amplifiers designed to meet all contingencies.

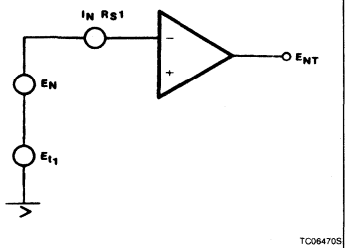


Figure 17. Total Noise Configuration

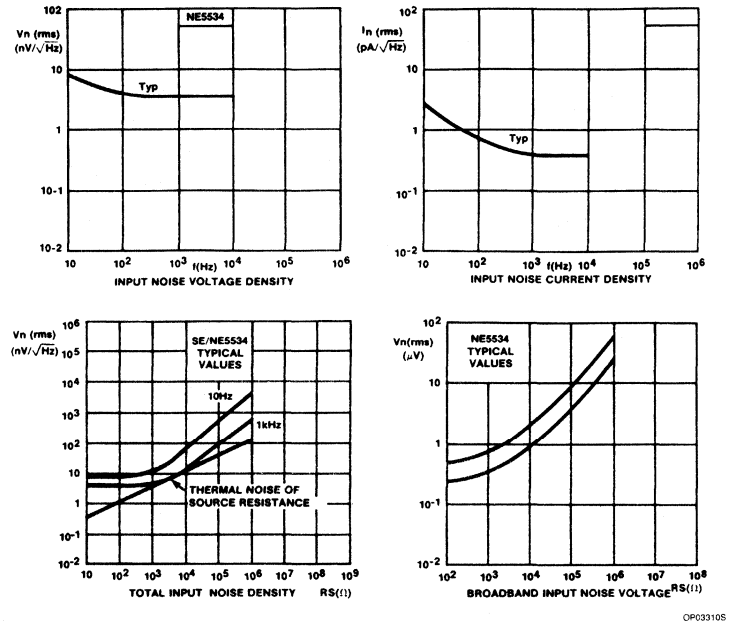


Figure 18. NE5534 Noise Characteristics

AN165
Integrated Operational Amplifier Theory

Application Note

INTRODUCTION

The operational amplifier was first introduced in the early 1940s. Primary usage of these vacuum tube forerunners of the ideal gain block was in computational circuits. They were fed back in such a way as to accomplish addition, subtraction, and other mathematical functions.

Expensive and extremely bulky, the operational amplifier found limited use until new technology brought about the integrated version, solving both size and cost drawbacks.

Volumes upon volumes have been and could be written on the subject of op amps. In the interest of brevity, this application note will cover the basic op amp as it is defined, along with test methods and suggestive applications. Also, included is a basic coverage of the feedback theory from which all configurations can be analyzed.

THE PERFECT AMPLIFIER

The ideal operational amplifier possesses several unique characteristics. Since the device will be used as a gain block, the ideal amplifier should have infinite gain. By definition also, the gain block should have an infinite input impedance in order not to draw any power from the driving source. Additionally, the output impedance would be zero in order to supply infinite current to the load being driven. These ideal definitions are illustrated by the ideal amplifier model of Figure 1.

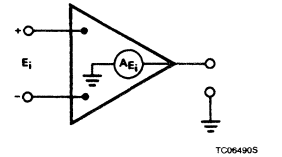


Figure 1. Ideal Operational Amplifier

Further desirable attributes would include infinite bandwidth, zero offset voltage, and complete insensitivity to temperature, power supply variations, and common-mode input signals.

Keeping these parameters in mind, further contemplation produces two very powerful analysis tools. Since the input impedance is infinite, there will be no current flowing at the amplifier input nodes. In addition, when feedback is employed, the differential input voltage reduces to zero. These two statements are used universally as beginning points for any network analysis and will be explored in detail later on.

THE PRACTICAL AMPLIFIER

Tremendous strides have been made by modern technology with respect to the ideal amplifier. Integrated circuits are coming closer and closer to the ideal gain block. In bipolar devices, for instance, input bias currents are in the pA range for FET input amplifiers while offset voltages have been reduced to less than 1mV in many cases.

Any device has limitations however, and the integrated circuit is no exception. Modern op amps have both voltage and current limitations. Peak-to-peak output voltage, for instance, is generally limited to one or two base-emitter voltage drops below the supply voltage, while output current is internally limited to approximately 25mA. Other limitations such as bandwidth and slew rates are also present, although each generation of devices improves over the previous one.

DEFINITION OF TERMS

Earlier, the ideal operational amplifier was defined. No circuit is ideal, of course, so practical realizations contain some sources of error. Most sources of error are very small and therefore can usually be ignored. It should be noted that some applications require special attention to specific sources of error.

Before the internal circuitry of the op amp is further explored, it would be beneficial to define those parameters commonly referenced.

INPUT OFFSET VOLTAGE

Ideal amplifiers produce 0V out for 0V input. But, since the practical case is not perfect, a small DC voltage will appear at the output, even though no differential voltage is applied. This DC voltage is called the input offset voltage, with the majority of its magnitude being generated by the differential input stage pictured in Figure 2.

An operational amplifier's performance is, in large part, dependent upon the first stage. It is the very high gain of the first stage that amplifies small signal levels to drive remaining circuitry. Coincidentally, the input current, a function of beta, must be as small as possible. Collector current levels are thus made very low in the input stage in order to gain low bias currents. It is this input stage which also determines DC parameters such as offset voltage, since the amplified output of this stage is of sufficient voltage levels to eclipse most subsequent error terms added by the remaining circuitry. Under balanced conditions, the collector currents of Q1 and Q2 are perfectly matched, hence we may say:

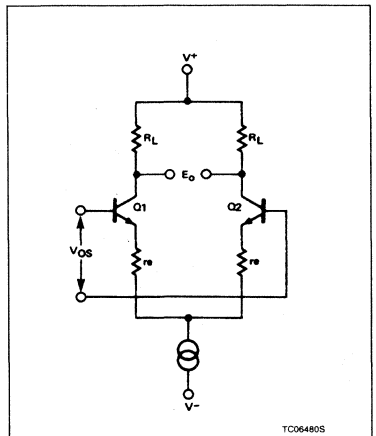


Figure 2. Differential Input Stage

$$E_{OS} = I_{C2}R_L - I_{C1}R_L = 0 \qquad (1)$$

In practice, small differences in geometries of the base-emitter regions of Q1 and Q2 will cause E_{OS} not to equal 0. Thus, for balance to be restored, a small DC voltage must be added to one V_{BE} or

$$V_{OS} = V_{BE}1 - V_{BE}2 \qquad (2)$$

where the V_{BE} of the transistor is found by

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_E}{I_s}\right) \qquad (3)$$

Reference is made to the input when talking of offset voltage. Thus, the classic definition of input offset voltage is 'that differential DC voltage required between inputs of an amplifier to force its output to zero volts.'

Offset voltage becomes a very useful quantity for the designer because many other sources of error can be expressed in terms of V_{OS}. For instance, the error contribution of input bias current can be expressed as offset voltages appearing across the input resistors.

INPUT OFFSET VOLTAGE DRIFT

Another related parameter to offset voltage is V_{OS} drift with temperature. Present-day amplifiers usually possess V_{OS} drift levels in the range of 5μV/°C to 40μV/°C. The magnitude of V_{OS} drift is directly related to the initial offset voltage at room temperature. Amplifiers exhibiting larger initial offset voltages will also possess higher drift rates with temperature. A rule of thumb often applied is that the drift per °C will be 3.3μV for each millivolt of initial offset. Thus, for tighter control of thermal drift, a low offset amplifier would be selected.

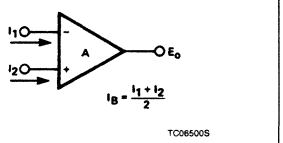


Figure 3. Input Bias Current

INPUT BIAS CURRENT

Referring to Figure 3, it is apparent that the input pins of this op amp are base inputs. They must, therefore, possess a DC current path to ground in order for the input to function. Input bias current, then, is 'the DC current required by the inputs of the amplifier to properly drive the first stage.'

The magnitude of I_{BIAS} is calculated as the average of both currents flowing into the inputs and is calculated from

$$I_B = \frac{I_1 + I_2}{2} \quad (4)$$

Bias current requirements are made as small as possible by using high beta input transistors and very low collector currents in the first stage. The trade-off for bias current is lower stage gain due to low collector current levels and lower slew rates. The effect upon slew rate is covered in detail under the compensation section.

INPUT OFFSET CURRENT

The ideal case of the differential amplifier and its associated bias current does not possess an input offset current. Circuit realizations always have a small difference in bias currents from one input to the other, however. This difference is called the input offset current. Actual magnitudes of offset current are usually at least an order of magnitude below the bias current. For many applications this offset may be ignored but very high gain, high input impedance amplifiers should possess as little I_{OS} as possible because the difference in currents flowing across large impedances develops substantial offset voltages. Output voltage offset due to I_{OS} can be calculated by

$$V_{OUT} = A_{CL}(I_{OS}R_S) \quad (5)$$

Hence, high gain and high input impedances magnify directly to the output, the error created by offset current. Circuits capable of nulling the input voltage and current errors are available and will be covered later in this chapter.

INPUT OFFSET CURRENT DRIFT

Of considerable importance is the temperature coefficient of input offset current. Even though the effects of offset are nulled at room temperature, the output will drift due to changes in offset current over temperature. Many popular models now include a typical specification for I_{OS} drift with values ranging in the 0.5nA/°C area. Obviously, those applications requiring low input offset currents also require low drift with temperature.

INPUT IMPEDANCE

Differential and common-mode impedances looking into the input are often specified for integrated op amps. The differential impedance is the total resistance looking from one input to the other, while common-mode is the common impedance as measured to ground. Differential impedances are calculated by measuring the change of bias current caused by a change in the input voltage.

COMMON-MODE RANGE

All input structures have limitations as to the range of voltages over which they will operate properly. This range of voltages impressed upon *both inputs* which will not cause the output to misbehave is called the common-mode range. Most amplifiers possess common-mode ranges of ± 12V with supplies of ± 15V.

COMMON-MODE REJECTION RATIO

The ideal operational amplifier should have no gain for an input signal common to both inputs. Practical amplifiers do have some gain to common-mode signals. The classic definition for common-mode rejection ratio of an amplifier is the ratio of the differential signal gain to the common-mode signal gain expressed in dB as shown in equation 6a.

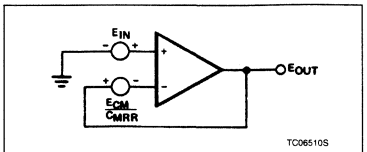


Figure 4. Effects of CMRR on Voltage-Follower

$$CMRR(dB) = 20 \log \frac{e_O/e_I}{e_O/e_{CM}} \quad (6a)$$

The measurement CMRR as in 6a requires 2 sets of measurements. However, note that if e_o in equation 6a is held constant, CMRR becomes:

$$CMRR(dB) = 20 \log \frac{e_{CM}}{e_I} \quad (6b)$$

A new alternate definition of CMRR based on 6b is the ratio of the change of input offset voltage to the input common-mode voltage change producing it.

Figure 4 illustrates the application of the equivalent common-mode error generator to the voltage-follower circuit. The gain of the voltage-follower with error contributions caused by both finite gain and finite common-mode rejection ratio is shown in equation 7.

$$\frac{e_O}{e_{IN}} = \frac{1 \pm 1/CMRR}{1 + 1/A} \quad (7)$$

where A equals open-loop gain and is frequency-dependent.

AC PARAMETERS

Parameter definition has, up to this point, been dealing primarily with DC quantities of voltages currents, etc. Several important AC, or frequency-dependent parameters will now be discussed.

An ideal gain block was defined earlier as one which would provide infinite gain and bandwidth. Real circuits approximate infinite open-loop gain with low frequency gains in excess of 100dB. The very high gains achieved with present designs are possible only by cascading stages. Although providing very high open-loop gain, the cascading of stages results in the need for frequency compensation in closed-loop configurations and reduces the open-loop.

LARGE-SIGNAL BANDWIDTH

The large-signal or power bandwidth of an amplifier refers to its ability to provide its maximum output voltage swing with increasing frequency. At some frequency the output will become slew rate limited and the output will begin to degrade. This point is defined by

$$f_{PL} = \frac{\text{Slew Rate}}{2\pi \cdot E_{OUT}} \quad (8)$$

where f_{PL} is the upper power bandwidth frequency and E_{OUT} is the peak output swing of the amplifier.

SLEW RATE

The maximum rate of change of the output in response to a step input signal is termed slew rate. Deviation from the ideal is caused by the limitation in frequency response of the amplifier stages and the phase compensation technique used. Summing node and amplifier output capacitances must be kept to a minimum to guarantee getting the maximum slew rate of the operational amplifier. Circuit board layout must also be of high frequency quality. Power supplies should be adequately bypassed at the pins, with both low and high frequency components, to avoid possible ringing. A selection of a proper capacitor in parallel with the feedback resistor may be necessary. Too small a value could result in excessive ringing and too large a value will decrease frequency response. In general, the worst case slew rate is in the unity gain noninverting mode (see Figure 5a). Specifications of slew rate should always reflect this worst case condition with the maximum required compensation network.

FREQUENCY RESPONSE

Distributed capacitances and transit times in semiconductors cause an upper frequency limit or pole for each gain stage. Monolithic PNP transistors, used for level shifting, possess poor upper frequency characteristics. Cascaded gain stages, used to approach the highest gain, subtract from the maximum frequency response. As shown in Figure 6, the open-loop frequency response of the op amps shown crosses unity gain at approximately 10MHz. Closed-loop response is unstable without compensation, however, so typical unity gain frequencies are readjusted by the effects of phase compensation, in this case 1MHz.

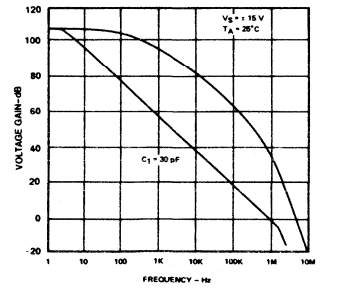


Figure 6. Open-Loop Voltage Gain as a Function of Frequency

From Figure 6, it is also apparent that an amplifier has a trade-off between gain and bandwidth. Higher gains are achieved at the expense of bandwidth. This trade-off is a constant figure called the gain bandwidth product.

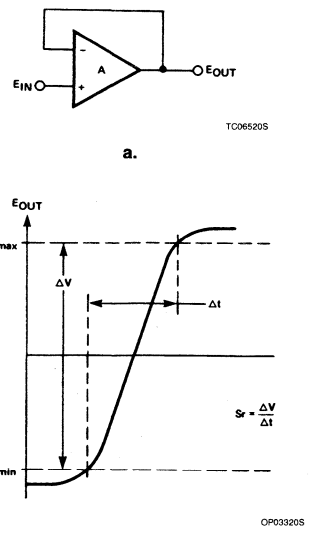
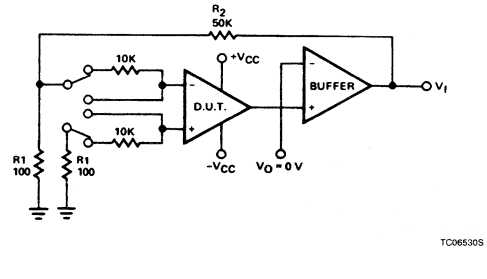
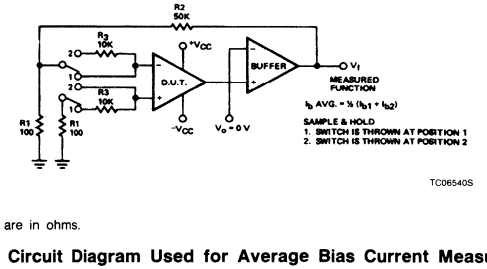


Figure 5. Amplifier Slew Rate Limitations



NOTE:
All resistor values are in ohms.

Figure 7. Circuit Diagram Used for CMRR Measurement



NOTE:
All resistor values are in ohms.

Figure 8. Circuit Diagram Used for Average Bias Current Measurement

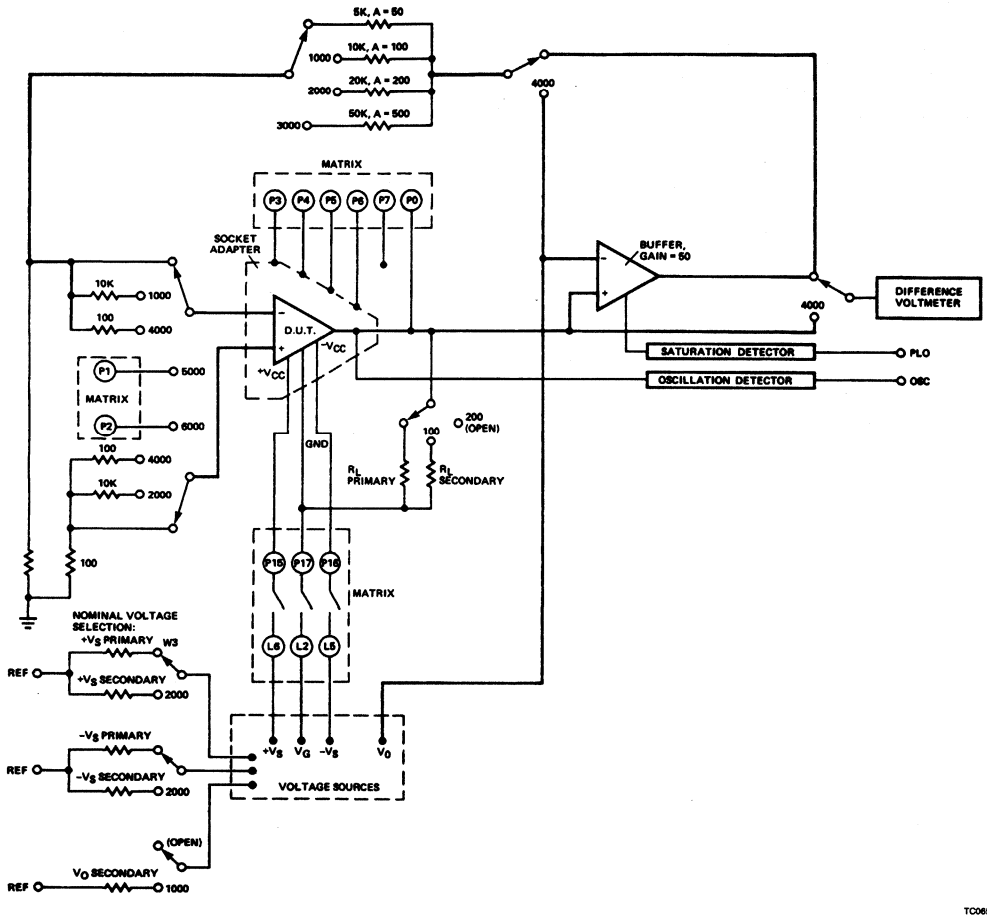
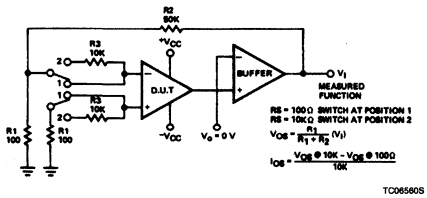
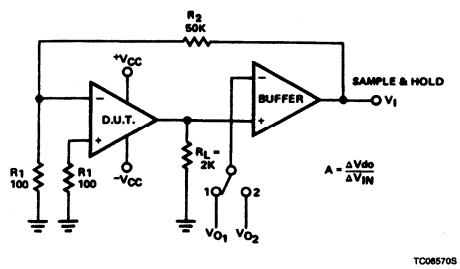


Figure 9. A Typical Op Amp Test Circuit (Simplified)



NOTE:
All resistor values are in ohms.

Figure 10. Circuit Diagram Used for Offset Voltage and Offset Current



NOTE:
All resistor values are in ohms.

Figure 11. Circuit Diagram Used for Large-Signal Open-Loop Gain Measurement

TEST METHODS

Product testing of integrated circuits uses automatic test equipment. Large computer-controlled test decks test all data sheet limits in a matter of milliseconds. Each parameter is tested in a specific circuit configuration defined by the test hardware.

A typical simplified op amp test configuration is depicted by Figure 9. Units may be classed in several categories according to selected parameters. Even failures may be classified categorically, depending upon their mode of failure.

Figures 7, 8, 10 and 11 illustrate the general test setups commonly used to measure CMRR, average bias current, offset voltage and current, and open-loop gain, respectively.

In general, the following parameters are tested under the following conditions.

COMMON-MODE REJECTION

The test setup for CMRR is given in Figure 7. Resistor values are chosen to provide sufficient sensitivity and accuracy for the device type being tested and the voltage measuring equipment being used.

The positive common-mode input voltage within the range V_{CM1} is algebraically subtracted from all supply voltages and from V_O. Then V_1 is measured (V_{11}). The most negative common-mode voltage within the range, V_{CM2}, is then subtracted from all the supply voltages and V_O, and V_1 is again measured (V_{12}).

Then

$$CMRR = (R1 + R2)/R1(V_{CM1} - V_{CM2})/V_{11} - V_{12} \quad (9)$$

This operation is equivalent to swinging both inputs over the full common-mode range, and holding the output voltage constant, but it makes the V_1 measurement much simpler.

BIAS CURRENT

Bias current is measured in the configuration of Figure 8.

With switches at position 1 and $V_O = 0V$, measure V_{11}. Move switches to position 2 and again measure V_{12}. Calculate I_{BIAS} (average), by

$$I_{B1} = \frac{R1}{R1 + R2}\left(\frac{V1}{R3}\right) \quad (10a)$$

$$I_{B2} = \frac{R1}{R1 + R2}\left(\frac{V1}{R3}\right) \quad (10b)$$

$$I_{BIAS(avg)} = \frac{I_{B1} + I_{B2}}{2} = \frac{R1}{R1 + R2}\,\frac{V_{11} - V_{12}}{2R3} \quad (10c)$$

OFFSET VOLTAGE

Figure 10 is used for both offset voltage and current. With V_O at 0V and the switches selecting the source impedance of 100Ω, the offset voltage is measured at V_1 and is equal to

$$V_{OS} = \frac{R1V_1}{R1 + R2} \quad (11)$$

OFFSET CURRENT

Offset current is measured by calculation of offset voltage change with a change in source impedance. With switches in position 1, measure V_{12}. Calculate the contribution of I_{OS} by

$$I_{OS} = \frac{V_{12} - V_I}{R3} \quad (12)$$

SIGNAL GAIN

The signal gain of operational amplifiers is most commonly specified for the full output swing.

This is referred to as large signal voltage gain and can be measured by the circuit of Figure 11. Usually specified under a specific load determined by R_L, a signal equal to the maximum swing of the output voltage is applied to V_O in both positive and negative directions. V_{11} and V_{12} are measured values of V_1 and V_O = maximum positive and maximum negative signals, respectively. The gain of the device under test then becomes

$$A_{VO} = \left(\frac{R1 + R2}{R1}\right)\left(\frac{V_{O1} - V_{O2}}{V_{11} - V_{12}}\right) \quad (13)$$

SLEW RATE

Many other parameters are checked automatically by similar means. Only the most important ones have been covered here. Of great interest to the designer are other parameters which do not necessarily carry minimum or maximum limits. One such parameter is slew rate. The configuration used to measure slew rate depends upon the intended application. Worst case conditions arise in the unity gain non-inverting mode.

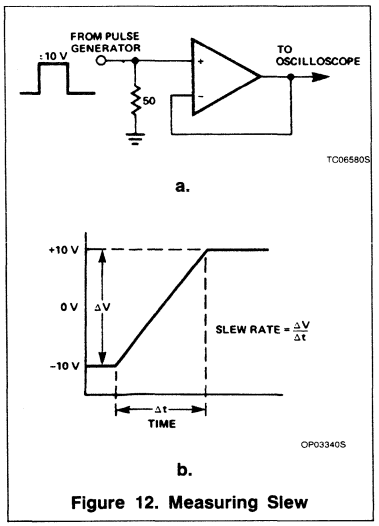


Figure 12. Measuring Slew

Figure 12 shows a typical bench setup for measuring the response of the output to a step input. The input step frequency should be of a frequency low enough for the output of the op amp to have sufficient time to slew from limit to limit. In addition, V_{IN} must be less

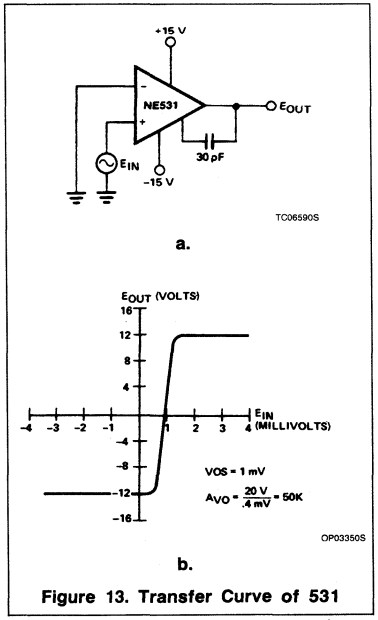


Figure 13. Transfer Curve of 531

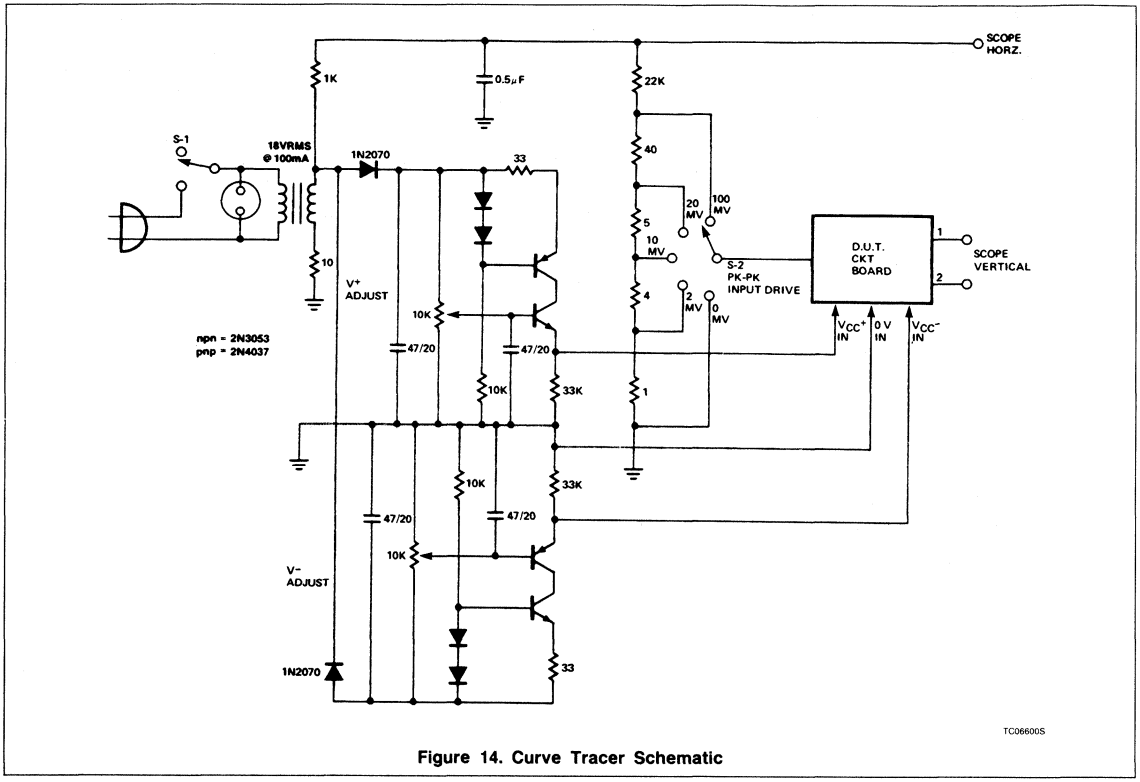


Figure 14. Curve Tracer Schematic

than absolute maximum input voltage and the waveform should have good rise and fall times. The slew rate is then calculated from the slope of the output voltage versus time or

$$SR = \frac{\Delta V_{OUT}}{\Delta T} \text{ in } V/\mu s \qquad (14)$$

OP AMP CURVE TRACER

Two of the most important parameters of linear integrated circuits having differential inputs are voltage gain and input offset voltage. These parameters may be read directly from a plot of the transfer characteristic of the device. This memo will describe a very simple curve tracer which, when used with an oscilloscope, will display the transfer characteristic of most Signetics linear devices.

Figure 13 shows the transfer characteristics of a typical linear device, the Signetics NE531. Note that the unit saturates at approximately +12V and −12V and exhibits a linear transfer characteristic between −10V and +10V.

From the slope of this linear portion of the transfer characteristic, and from the point and +10V where it crosses the E_{IN} axis, the voltage gain and offset voltage may be determined. It can be seen that the voltage gain of the device under test, (DUT), is 50,000 and its input offset voltage is 1.0mV.

A simple circuit to display the curves of Figure 13 on an oscilloscope is shown in Figure 14. A 60Hz, $44V_{P-P}$ sinewave is applied to the horizontal input of oscilloscope and an attenuated version of the sinewave is applied to the input of the DUT.

The output of the DUT drives the vertical input of the scope. For providing V+ and V− to the DUT, the tester uses two simple adjustable regulators, both current-limited at 25mA. Input drive to the DUT may be selected by means of S-2 as shown.

To use the curve tracer, first preset the V+ and V− supplies with an accurate meter. The supply voltages are somewhat dependent on AC line regulation and should be checked periodically. The horizontal gain of the scope may be set to give a convenient readout of the peak-to-peak DUT input signal corresponding to the setting of S-2. As some devices have two outputs, a second output line (vertical 2) has been provided for these devices. The transfer function of such devices will be inverted to that of Figure 13.

Simplicity and low cost are the two major attributes of this tester. It is not intended to perform highly rigorous tests for all devices. It is, however, a reasonably accurate means of determining the gains and offset voltages of most amplifiers. It will, in addition, indicate the transfer curves of comparators and sense amplifiers with equivalent accuracies.

AMPLIFIER DESIGN

Linear operational amplifier ICs were introduced soon after the appearance of the first digital integrated circuits. The performance of these early devices, however, left much to be desired until the introduction of the 709 device. Even with its lack of short-circuit protection and its complicated compensation requirements, the 709 gained real acceptance for the IC op amp. The 709 was designed using a three-stage approach requiring both input and output stage compensation. In addition, the output stage was not short-circuit proof and the input stage latched-up under certain conditions, requiring external protection.

Much better designs soon were introduced. Among the contenders were the 741, 748, 101, and 107 devices. All were general purpose devices with single capacitor compensation, (some were internally-compensated), and all heralded input and output overstress protection. The basic design has two gain stages. By rolling off the frequency response of one of these (the second stage), so that the overall gain is unity at a frequency below the point where excess phase becomes significant, the device can be stabilized for all feedback configurations. Further, by making the first stage a voltage-to-current converter, with a small g_M and the second stage a current-to-voltage converter with a high r_M, the second stage can be rolled off at 6dB octave with a small value capacitor in the order of 30pF, which can then be built into the device itself. This concept is shown in Figure 15.

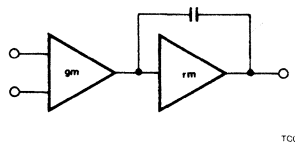


Figure 15. Basic Two-Stage Op Amp Design

The frequency and phase response of the PNP devices in the first stage dictate a roll-off in the second stage to give a loop gain of unity at about 1.0MHz. For the unity gain feedback configuration, this implies an open-loop gain of unity at this frequency. The capacitor C_C controls this parameter by looking much smaller than r_M at frequencies above a few cycles, giving a clean 6dB/octave roll-off over 5 decades.

The overall gain at frequencies where the impedance of C_C dominates r_m is given by

$$A_{V(\omega)} = \frac{qI_{S1}}{4kT} \cdot \frac{1}{\omega C_C} \qquad (15)$$

Substituting the value given, we find that a capacitance of C_C = 30pF gives a unity gain frequency of about 1.0MHz.

First-stage large signal current also defines the slew rate for a specific compensation technique. It is this current which must charge and discharge the C_C by the expression

$$SR = \frac{dV}{dT} = \frac{I_{LS}}{C_C} \qquad (16)$$

where I_{LS} is the largest signal current of the input stage. Obviously, the slew rate can be improved by increasing the first-stage collector current. This would, however, reflect directly upon the bias current by increasing it.

Two serious limitations, then, of these devices for diverse applications are input bias current and slew rate. Both may be overcome with small changes of the input structure to yield higher performance devices.

Reducing the input bias current becomes a matter of raising the transistor beta of the first stage. Several current designs boasting very low input currents use what is termed super beta input devices. These transistors have betas of 1,500 to 7,000. Bias currents under 2nA can be achieved in this way. Even though the B_{VCEO} of such transistors can be as low as 1V, the lower breakdowns are accounted for in the input stage by rearranging the bias technique. Bandwidths and slew rates suffer only slightly as a result of the lower current levels.

The second limitation of 741 devices is slew rate. As previously mentioned, the rate of change is dictated by the compensation capacitance as charged by the large signal current of the first stage. By altering the large signal g_M of the first stage as depicted by Figure 18, the slew rate can be dramatically increased.

The additional current supplied during large signal swings by current source I_4 causes the first-stage transfer function to change as shown in Figure 19. The compensation capacitor is returned to the output of the NE531 structure because the output driving source must be capable of supplying the increased current to charge the capacitor.

Large-signal bandwidths with this input structure will be essentially the same as the small-signal response. Full bandwidth possibilities of this configuration are still limited by the beta and f_t of the lateral PNP devices used for collector loads in the first stage. Even so, the slew rate of the NE531 and NE538 is a factor of 40 better than general purpose devices.

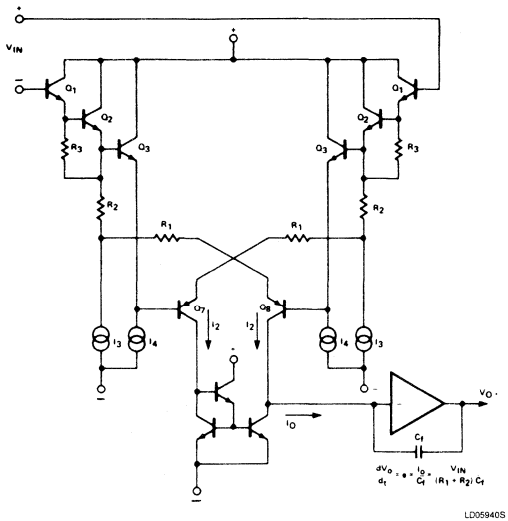


Figure 18. Input Structure of 531

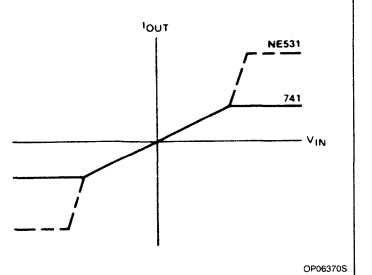


Figure 19. Voltage/Current Curves of First Stage

AN166
Basic Feedback Theory

Application Note

BASIC FEEDBACK THEORY

In AN165, the ideal op amp was defined. The ideal parameters are never fully realized but they present a very convenient method for the preliminary analysis of circuitry. So important are these ideal definitions that they are repeated here. The ideal amplifier possesses

1. Infinite gain
2. Infinite input impedance
3. Infinite bandwidth
4. Zero output impedance

From these definitions two important theorems are developed.

1. No current flows into or out of the input terminals.
2. When negative feedback is applied, the differential input voltage is reduced to zero.

Keeping these rules in mind, the basic concept of feedback can be explored.

VOLTAGE-FOLLOWER

Perhaps the most often used and simplest circuit is that of a voltage-follower. The circuit of Figure 1 illustrates the simplicity.

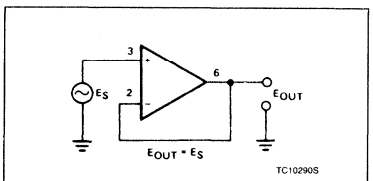


Figure 1. Voltage-Follower

Applying the zero differential input theorem, the voltages of Pins 2 and 3 are equal, and since Pins 2 and 6 are tied together, their voltage is equal; hence, $E_{OUT} = E_{IN}$. Trivial to analyze, the circuit nevertheless does illustrate the power of the zero differential voltage theorem. Because the input impedance is multiplied and the output impedance divided by the loop gain, the voltage-follower is extremely useful for buffering voltage sources and for impedance transformation.

The basic configuration in Figure 1 has a gain of 1 with extremely high input impedance. Setting the feedback resistor equal to the source impedance will cancel the effects of bias current if desired.

However, for most applications, a direct connection from output to input will suffice. Errors arise from offset voltage, common-mode rejection ratio, and gain. The circuit can be used with any op amp with the required unity gain compensation, if it is required.

NON-INVERTING AMPLIFIER

Only slightly more complicated is the non-inverting amplifier of Figure 2.

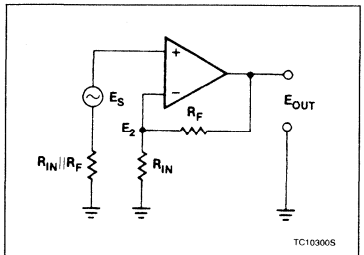


Figure 2. Non-Inverting Amplifier

The voltage appearing at the inverting input is defined by

$$E_2 = \frac{E_{OUT} \cdot R_{IN}}{R_F + R_{IN}} \qquad (1a)$$

Since the differential voltage is zero, $E_2 = E_S$, and the output voltage becomes

$$E_{OUT} = E_S\left(1 + \frac{R_F}{R_{IN}}\right) \qquad (1b)$$

It should be noted that as long as the gain of the closed-loop is small compared to open-loop gain, the output will be accurate, but as the closed-loop gain approaches the open-loop value more error will be introduced.

The signal source is shown in Figure 2 in series with a resistor equal in size to the parallel combination of R_{IN} and R_F. This is desirable because the voltage drops due to bias currents to the inputs are equal and cancel out even over temperature. Thus overall performance is much improved.

The amplifier does not phase-invert and possesses high input impedance. Again the impedances of the two inputs should be equal to reduce offsets due to bias currents.

INVERTING AMPLIFIER

By slightly rearranging the circuit of Figure 2, the non-inverting amplifier is changed to an inverting amplifier. The circuit gain is found by applying both theorems; hence, the voltage at the inverting input is 0 and no current flows into the input. Thus the following relationships hold:

$$\frac{E_S}{R_{IN}} + \frac{E_O}{R_F} = 0 \qquad (2a)$$

Solving for the output E_O

$$E_O = -E_S\frac{R_F}{R_{IN}} \qquad (2b)$$

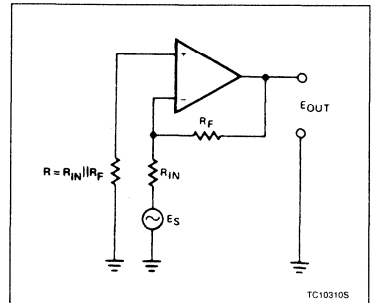


Figure 3. Inverting Amplifier

As opposed to the non-inverting circuits the input impedance of the inverting amplifier is not infinite but becomes essentially equal to R_{IN}. This circuit has found widespread acceptance because of the ease with which input impedance and gain can be controlled to advantage, as in the case of the summing amplifier.

With the inverting amplifier of Figure 3, the gain can be set to any desired value defined by R divided by R_{IN}. Input impedance is defined by the value of R_{IN} and R should equal the parallel combination of R_{IN} and R to cancel the effect of bias current. Offset voltage, offset current, and gain contribute most of the errors. The ground may be set anywhere within the common-mode range and any op amp will provide satisfactory response.

CURRENT-TO-VOLTAGE CONVERTER

The transfer function of the current-to-voltage converter is

$$V_{OUT} = I_{IN} R_1 \qquad (3)$$

Evaluation of the circuit depends upon the virtual ground theorem developed earlier. The current flowing into the input must be the same as that flowing across R1, hence, the output voltage is the IR drop of R1.

Limitations, of course, are output saturation voltage and output current capability. The inputs may be biased anywhere within the common-mode range.

DIFFERENTIAL AMPLIFIER

This circuit of Figure 5 has a gain with respect to differential signals of R2/R1.

The common-mode rejection is dominated by the accuracy of the resistors. Other errors arise from the offset voltage, input offset current, gain and common-mode rejection. The circuit can be used with any op amp discussed in this chapter with the proper compensation.

SUMMING AMPLIFIER

The summing amplifier is a variation of the inverting amplifier. The output is the sum of the input voltages, each being weighed by R_F/R_{IN}.

The value of R4 may be chosen to cancel the effects of bias current and is selected equal to the parallel combination of R_F and all the input resistors.

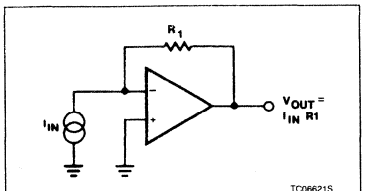


Figure 4. Current-to-Voltage Converter

INTEGRATOR

Integration can be performed with a variation of the inverting amplifier by replacing the feedback resistor with a capacitance. The transfer function is defined by

$$V_{OUT} = -\frac{1}{RC}\int_{o}^{t} V_{IN} \cdot dt \qquad (4)$$

The gain of the circuit falls at 6dB per octave over the range in which strays and leakages are small.

Since the gain at DC is very high a method for resetting initial conditions is necessary. Switch S1 removes the charge on the capacitor. A relay or FET may be used in the practical circuit. Bias and offset currents and offset voltage of the switch should be low in such an application.

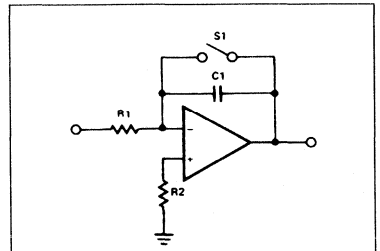


Figure 7. Integrator

DIFFERENTIATOR

The differentiator of Figure 8 is another variation of the inverting amplifier. The gain increases at 6dB per octave until it intersects the amplifier open-loop gain, then decreases because of the amplifier bandwidth. This characteristic can lead to instability and high frequency noise sensitivity.

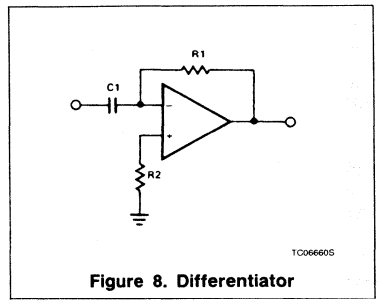


Figure 8. Differentiator

A more practical circuit is shown in Figure 9. The gain has been reduced by R3 and the high frequency gain reduced by C2, allowing better phase control and less high frequency noise. Compensation should be for unity gain.

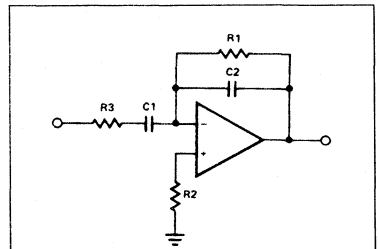


Figure 9. Practical Differentiator

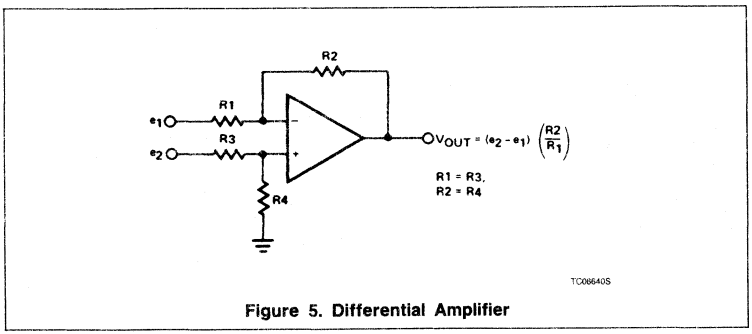


Figure 5. Differential Amplifier

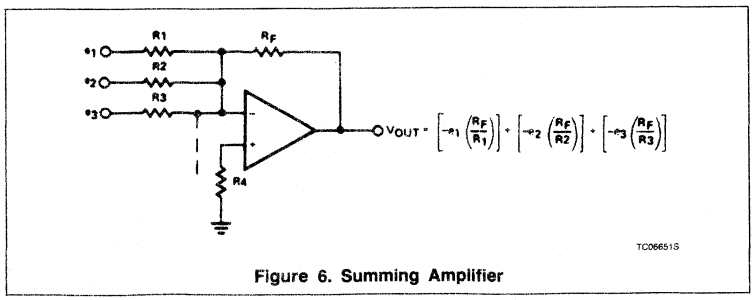


Figure 6. Summing Amplifier

COMPENSATION

Present-day operational amplifiers are comprised of multiple stages, each of which has a 3dB point or pole associated with it. Referring to Figure 10, the 3dB breakpoints of a two-stage amplifier are approximated by the Bode plot.

As with any feedback loop, the op amp must be protected from phase shifts in excess of 360°. A steady 180° phase shift is developed by the amplifier from output to inverting input. In addition, the sum of all additional shifts due to amplifier poles or feedback component poles will cause the necessary additional 180° to sustain oscillation if the gain of the amplifier is greater than one for the frequency at which the 180° phase shift is reached. By adding poles and zeros to the amplifier response externally, the phase shift can be controlled to insure stability.

Many op amps now include internal compensation. These are single capacitors of 30pF, typically, and the amplifier will remain stable for all gains. However, since they are unconditionally stable, the compensation is larger than required for most applications. The resultant loss of bandwidth and slew rate may be acceptable in the general case, but selection of an externally-compensated device can add a great deal to the amplifier response if the compensation is handled properly.

In order to fully develop the point at which instability occurs, a fuller understanding of phase response is necessary.

The diagram of Figure 11 depicts the phase shift of a single pole. Note that at the pole position the phase shift is 45° and that phase shift becomes 0° for a decade below the pole and −90° for a decade above the pole location. This is a Bode approximation which possesses a 5.7° error at 0° and 90°, but this error is usually considered small enough to be ignored. The single pole produces a maximum of 90° phase shift and also produces a frequency roll-off of 20dB per decade. The addition of the second pole of Figure 12 produces an additional 90° phase shift and increases the roll-off slope to −40dB per decade.

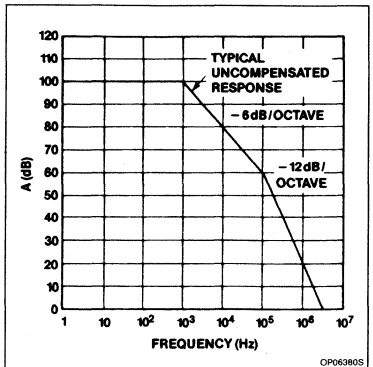


Figure 10. Frequency Compensation

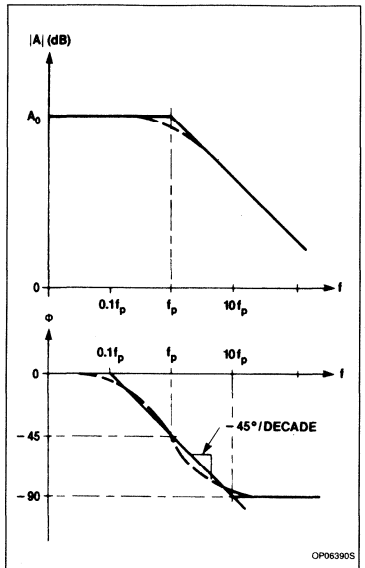


Figure 11. Single-Pole Amplitude and Phase Response

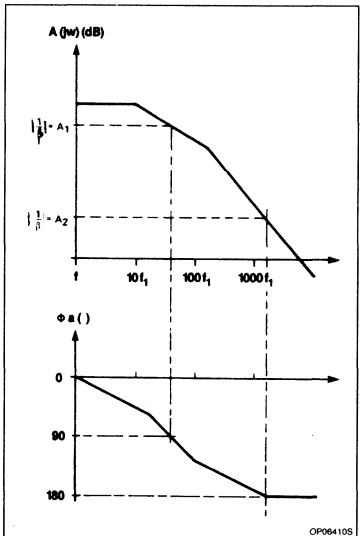


Figure 12. Two-Pole Closed-Loop Response

At this point, phase shift could exceed 180° because unity gain is reached, causing stability. For gain levels equal to A1 or $1/\beta$, the phase shift is only 90° and the amplifier is stable. However, the gain of A2 the phase shift is 180° and the loop is unstable. Gains in between A1 and A2 are marginally stable.

However, as shown in Figure 13, the phase shift as it approaches 180° causes increasing frequency peaking and overshoot until sustained oscillations occur.

It is generally accepted in the interest of minimized frequency peaking to limit the phase shift of the amplifier to 135° or a phase margin of 45°. At this margin the second-order response of the system is critically damped and oscillation is prevented.

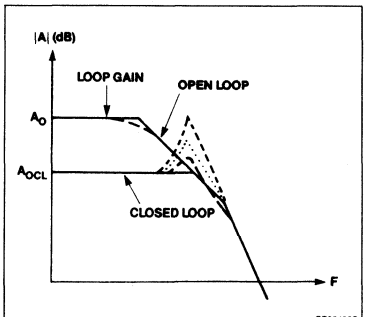


Figure 13. Frequency Peaking Due to Insufficient Phase Margin

Referring to Figure 14, the required compensation can be determined. Given the open-loop response of the amplifier, the desired gain is plotted until it intercepts the open-loop curve as shown.

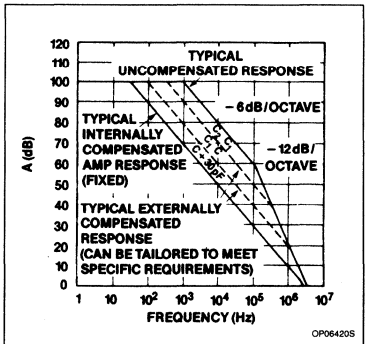


Figure 14. Frequency Compensation

The phase shift for minimum peaking is 135°. Remembering that phase shift is 45° at the frequency pole, the example of Figure 14 will be unstable at gains less than 20dB where phase shift exceeds 180°, and will possess excessive overshoot and ringing at gains I_{SS} than 60dB where phase shift exceeds 135°. Thus, the desired compensation will move the second pole of the amplifier out in frequency until the closed-loop gain intersects the open-loop response before the second break of the amplifier occurs. Selecting only enough compensation to do the job assures the maximum

bandwidths and slew rates of the amplifier. Additional in-depth information on compensation can be found in the reference material.

FEED-FORWARD COMPENSATION

External compensation has been shown to improve amplifier bandwidth over internal compensation in the preceding section. Additional bandwidth can be realized if feed-forward compensation is used. Bandwidth is limited in monolithic design by the poor frequency response of the PNP level shifters of the first stage.

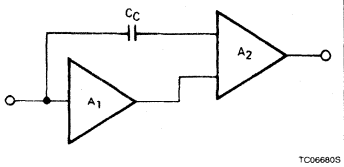


Figure 15. Technique of Feed-Forward Around 1st Stage

The concept of feed-forward compensation bypasses the input stage at high frequencies driving the higher frequency second stage directly as pictured by Figure 15. The Bode plot of Figure 16 shows the additional response added by the feed-forward technique. The response of the original amplifier requires less compensation at lower frequencies allowing an order of magnitude improvement in bandwidth. Standard compensation and feed-forward are both plotted to illustrate the bandwidth improvement. Unfortunately, the use of feed-forward compensation is restricted to the inverting amplifier mode.

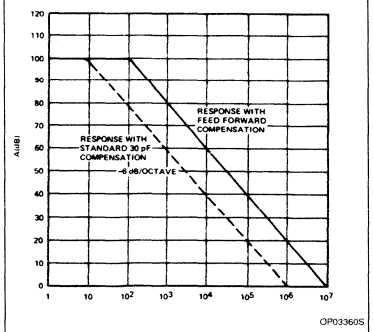


Figure 16. Frequency Response With Feed-Forward Compensation

REFERENCES

1. OPERATIONAL AMPLIFIERS-*Design & Applications*, Jerald Graeme and Gene Tobey, McGraw Hill Book Company.

AU2902
Low Power Quad Operational Amplifier

Preliminary Specification

DESCRIPTION

The AU2902 consists of four independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

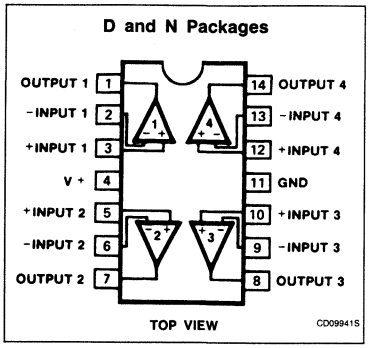
In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain crossover frequency and the input bias current are temperature-compensated.

FEATURES

- **Internally frequency-compensated for unity gain**
- **Large DC voltage gain: 100dB**
- **Wide bandwidth (unity gain): 1MHz (temperature-compensated)**
- **Wide power supply range Single supply: $3V_{DC}$ to $30V_{DC}$ or dual supplies: $\pm 1.5V_{DC}$ to $\pm 15V_{DC}$**
- **Very low supply current drain: essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)**
- **Low input bias current: $45nA_{DC}$ (temperature-compensated)**
- **Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage: $0V_{DC}$ to $V_{CC} - 1.5V_{DC}$ swing**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	−40°C to +125°C	AU2902N
14-Pin Plastic SO	−40°C to +125°C	AU2902D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	32 or ±16	V_{DC}
V_{IN}	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	−0.3 to +32	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[1] N package D package	 1420 1040	 mW mW
	Output short-circuit to GND one amplifier[2] V_{CC} < 15V_{DC} and T_A = 25°C	Continuous	
I_{IN}	Input current (V_{IN} < −0.3V)[3]	50	mA
T_A	Operating ambient temperature range AU2902	 −40 to +125	 °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   N package at 11.4mW/°C
   D package at 8.3mW/°C
2. Short-circuits from the output to V_{CC}+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15V_{DC} continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input bias clamps. In addition, there is also lateral NPN parasitic transistor action on the IC chip. This action can cause the output voltages of the op amps to go to the V+ rail (or to ground for a large overdrive) during the time that the input is driven negative.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V, T_A = 25°C, unless otherwise specified.

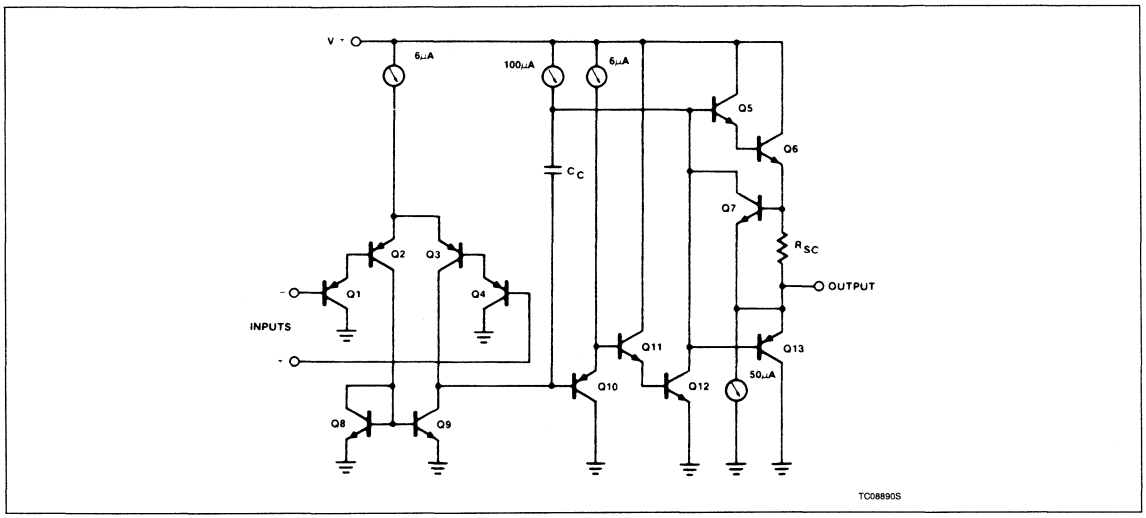
SYMBOL	PARAMETER	TEST CONDITIONS	AU2902			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S = 0\Omega$		±2	±7	mV
		$R_S = 0\Omega$, over temp.			±9	mV
$\Delta V_{OS}/\Delta T$	Temperature drift	$R_S = 0\Omega$, over temp.		7		μV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	250	nA
		$I_{IN}(+)$ or $I_{IN}(-)$, over temp.		40	500	nA
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50		pA/°C
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$		±5	±50	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.			±150	nA
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10		pA/°C
V_{CM}	Common-mode voltage range[3]	$V_{CC} \leqslant 30V$	0		$V_{CC} - 1.5$	V
		$V_{CC} \leqslant 30V$, over temp.	0		$V_{CC} - 2$	V
CMRR	Common-mode rejection ratio	$V_{CC} = 30V$	65	70		dB
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $V_{CC} = 30V$, over temp.	26			V
V_{OH}	Output voltage high	$R_L \geqslant 10k\Omega$, $V_{CC} = 30V$, over temp.	27	28		V
V_{OL}	Output voltage low	$R_L \leqslant 10k\Omega$, $V_{CC} = 5V$, over temp.		5	20	mV
I_{CC}	Supply current	$R_L = \infty$, $V_{CC} = 30V$, over temp.		1.5	3	mA
		$R_L = \infty$, $V_{CC} = 5V$, over temp.		0.7	1.2	mA
A_{VOL}	Large-signal voltage gain	$V_{CC} = 15V$ (for large V_O swing), $R_L \geqslant 2k\Omega$	25	100		V/mV
		$V_{CC} = 15V$ (for large V_O swing), $R_L \geqslant 2k\Omega$, over temp.	15			V/mV
	Amplifier-to-amplifier coupling[5]	f = 1kHz to 20kHz, input referred		−120		dB
PSRR	Power supply rejection ratio	$R_S = 0\Omega$	65	100		dB
I_{OUT}	Output current Source	$V_{IN}+ = +1V$, $V_{IN}- = 0V$, $V_{CC} = 15V$	20	40		mA
		$V_{IN}+ = +1V$, $V_{IN}- = 0V$, $V_{CC} = 15V$, over temp.	10	20		mA
	Sink	$V_{IN}- = +1V$, $V_{IN}+ = 0V$, $V+ = 15V$	10	20		mA
		$V_{IN}- = +1V$, $V_{IN}+ = 0V$, $V_{CC} = 15V$, over temp.	5	8		mA
		$V_{IN}- = +1V$, $V_{IN}+ = 0V$, $V_O = 200mV$	12	50		μA
I_{SC}	Short-circuit current[4]		10	40	60	mA
V_{DIFF}	Differential input voltage[3]				V_{CC}	V
GBW	Unity gain bandwidth			1		MHz
SR	Slew rate			0.3		V/μs
V_{NOISE}	Input noise voltage	f = 1kHz		40		nV/√Hz

See notes on next page.

NOTES:

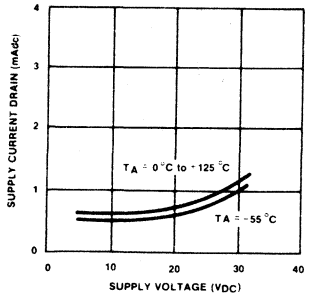
1. $V_O \cong 1.4V_{DC}$, $R_S = 0\Omega$ with V_{CC} from 5V to 30V and over full input common-mode range ($0V_{DC}$+ to V_{CC} – 1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC} –1.5, but either or both inputs can go to +32V without damage.
4. Short-circuits from the output to V_{CC} can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.

EQUIVALENT SCHEMATIC



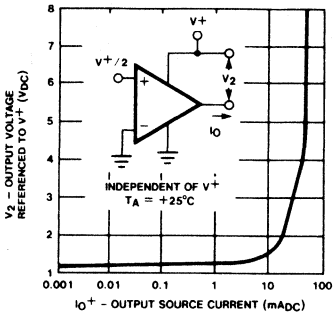
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current



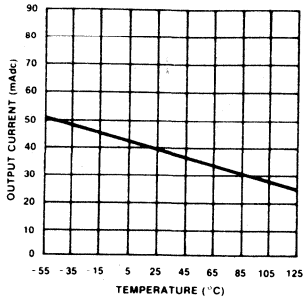
OP05450S

Output Characteristics Current Sourcing



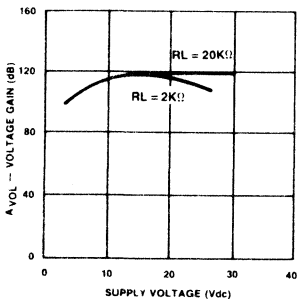
OP05461S

Current Limiting



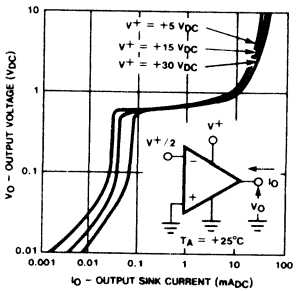
OP05470S

Voltage Gain



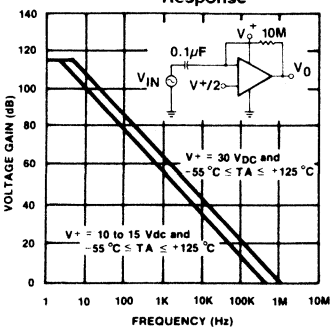
OP05480S

Output Characteristics Current Sinking



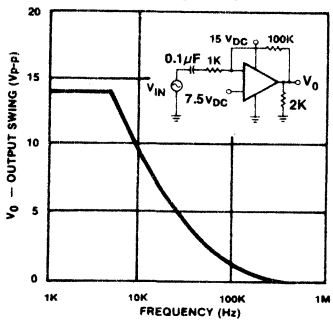
OP05490S

Open-Loop Frequency Response



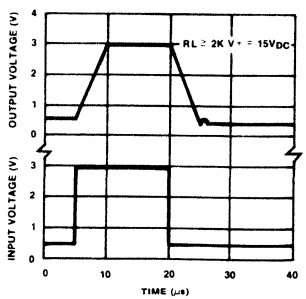
OP05500S

Large-Signal Frequency Response



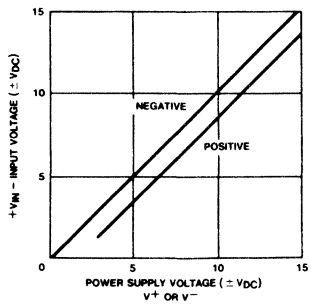
OP05511S

Voltage-Follower Pulse Response



OP05520S

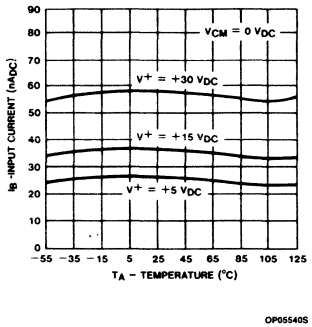
Input Voltage Range



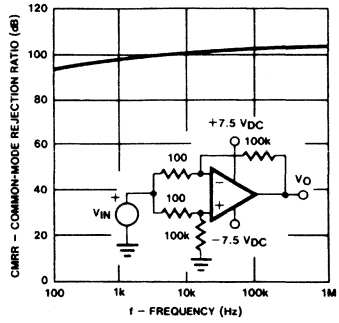
OP05530S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

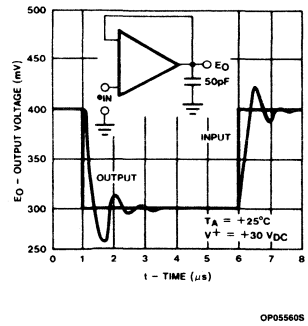
Input Current



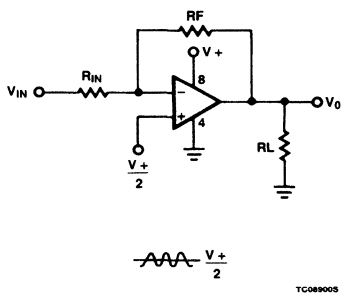
Common-Mode Rejection Ratio



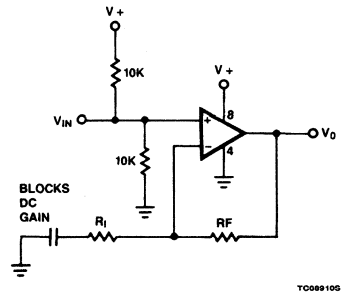
Voltage-Follower Pulse Response (Small-Signal)



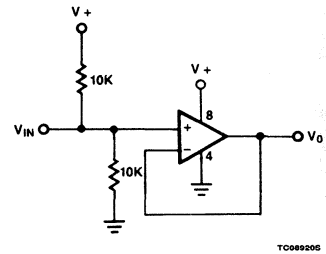
TYPICAL APPLICATIONS



Single Supply Inverting Amplifier



Non-Inverting Amplifier



Input Biasing Voltage-Follower

AU2904

Low Power Dual Operational Amplifier

Preliminary Specification

DESCRIPTION

The AU2904 consists of two independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage.

UNIQUE FEATURES

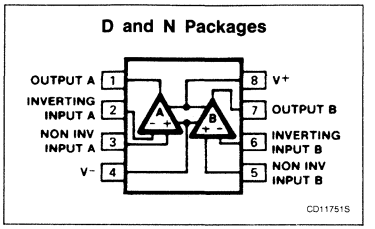
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain crossover frequency and the input bias current are temperature-compensated.

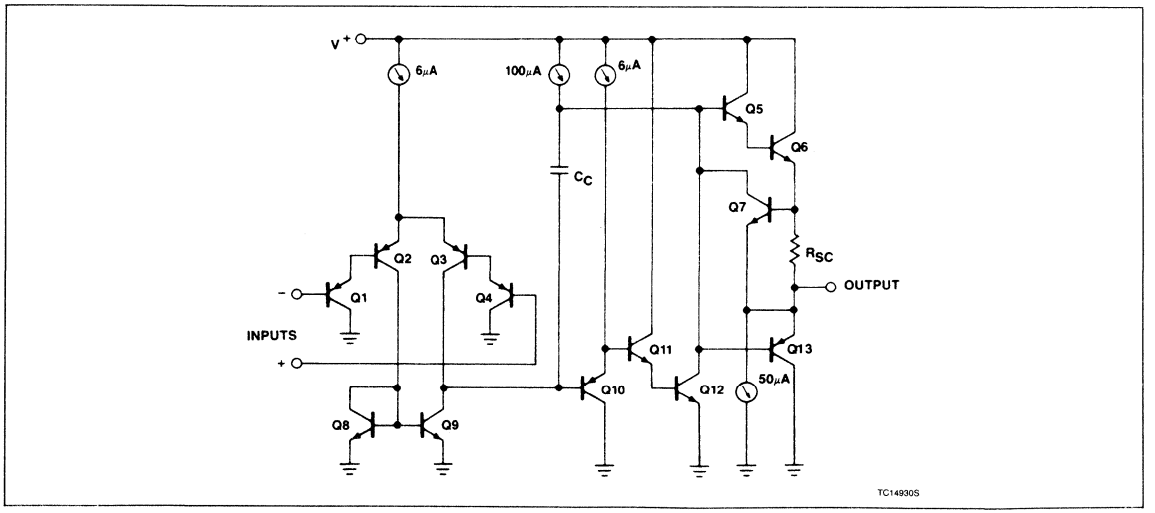
FEATURES

- **Internally frequency-compensated for unity gain**
- **Large DC voltage gain: 100dB**
- **Wide bandwidth (unity gain): 1MHz (temperature-compensated)**
- **Wide power supply range**
  Single supply: $3V_{DC}$ to $30V_{DC}$
  or dual supplies: $\pm 1.5V_{DC}$ to $\pm 15V_{DC}$
- **Very low supply current drain (400μA): essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)**
- **Low input bias current: $45nA_{DC}$ (temperature-compensated)**
- **Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage: $0V_{DC}$ to $V+ - 1.5V_{DC}$ swing**

PIN CONFIGURATION



EQUIVALENT CIRCUIT



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	−40°C to +125°C	AU2904N
8-Pin Plastic SO	−40°C to +125°C	AU2904D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage V+	32 or ±16	V_{DC}
	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	−0.3 to +32	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[1] N package D package	 1160 780	 mW mW
	Output short-circuit to GND[5] V+ < $15V_{DC}$ and T_A = 25°C	 Continuous	
T_A	Operating ambient temperature range AU2904	 −40 to +125	 °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, V+ = +5V, unless otherwise specified.

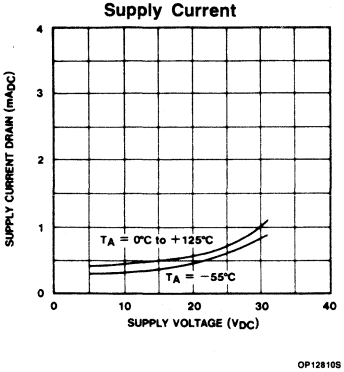
SYMBOL	PARAMETER	TEST CONDITIONS	AU2904			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S = 0\Omega$		±2	±7	mV
		$R_S = 0\Omega$, over temp.			±9	mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		7		μV/°C
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$		±5	±50	nA
		Over temp.			±150	nA
I_{OS}	Drift	Over temp.		10		pA/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	250	nA
		Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	500	nA
I_{BIAS}	Drift	Over temp.		50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+ = 30V	0		V+ – 1.5	V
		Over temp., V+ = 30V	0		V+ – 2.0	V
CMRR	Common-mode rejection ratio	V+ = 30V	65	70		dB
V_{OH}	Output voltage swing	$R_L \geq 2k\Omega$, V+ = 30V, over temp.	26			V
		$R_L \geq 10k\Omega$, V+ = 30V, over temp.	27	26		V
V_{OL}	Output voltage swing	$R_L \geq 10k\Omega$, Over temp.		5	20	mV
I_{CC}	Supply current	$R_L = \infty$, V+ = 30V		0.5	1.0	mA
		$R_L = \infty$ on all amplifiers, Over temp., V+ = 30V		0.6	1.2	mA
A_{VOL}	Large-signal voltage gain	$R_L \geq 2k\Omega$, V_{OUT} ±10V, V+ = 15V	25	100		V/mV
		Over temp.	15			V/mV
PSRR	Supply voltage rejection ratio	$R_S = 0\Omega$	65	100		dB
	Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		–120		dB
I_{OUT}	Output current Source	$V_{IN+} = +1V_{DC}$, $V_{IN-} = 0V_{DC}$, V+ = $15V_{DC}$	20	40		mA
		$V_{IN+} = +1V_{DC}$, $V_{IN-} = 0V_{DC}$, V+ = $15V_{DC}$, over temp.	10	20		mA
	Sink	$V_{IN-} = +1V_{DC}$, $V_{IN+} = 0V_{DC}$, V+ = $15V_{DC}$	10	20		mA
		$V_{IN-} = +1V_{DC}$, $V_{IN+} = 0V_{DC}$, V+ = $15V_{DC}$, over temp.	5	8		mA
		$V_{IN+} = 0V$, $V_{IN-} = +1V_{DC}$, $V_O = 200mV$	12	50		μA
I_{SC}	Short circuit current[5]			40	60	mA
	Differential input voltage[3]				V+	V
GBW	Unity gain bandwidth	$T_A = 25°C$		1		MHz
SR	Slew rate	$T_A = 25°C$		0.3		V/μs
V_{NOISE}	Input noise voltage	$T_A = 25°C$, f = 1kHz		40		$nV/\sqrt{Hz}$

NOTES:

1. $V_O \cong 1.4V$, $R_S = 0\Omega$ with V_{CC} from 5V to 30V and over full input common-mode range ($0V_{DC}$+ to V_{CC} – 1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ – 1.5, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.
5. Short-circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.

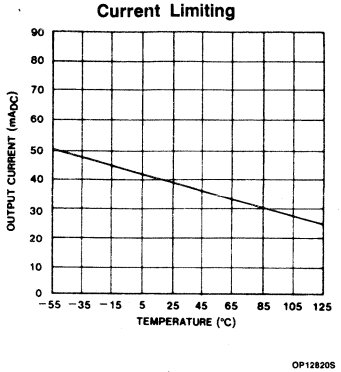
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current



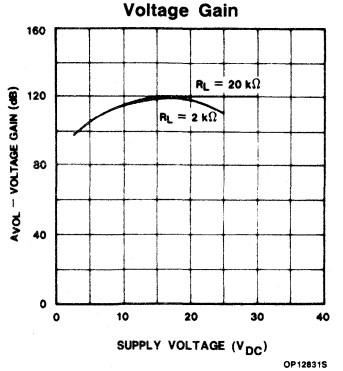
OP12810S

Current Limiting



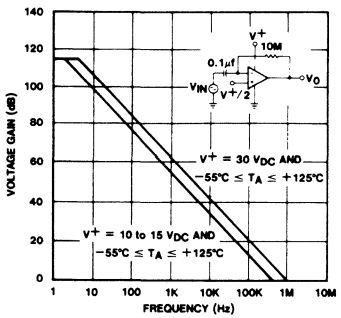
OP12820S

Voltage Gain



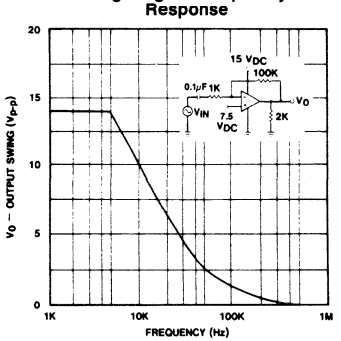
OP12831S

Open-Loop Frequency Response



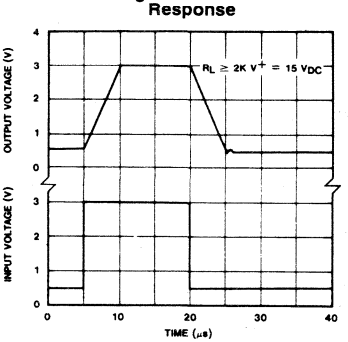
OP12840S

Large-Signal Frequency Response



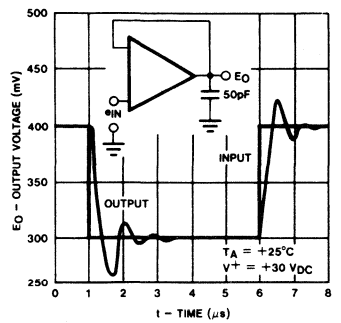
OP12851S

Voltage-Follower Pulse Response



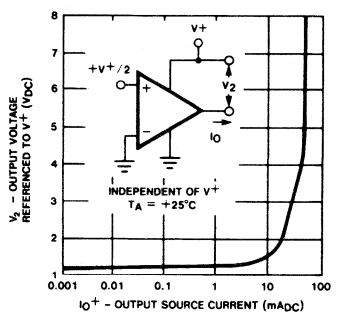
OP12860S

Voltage-Follower Pulse Response (Small-Signal)



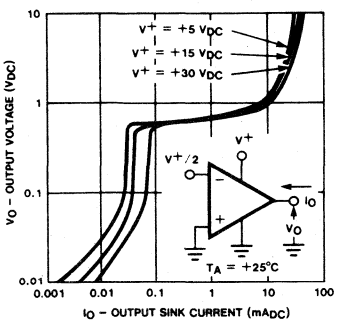
OP12870S

Output Characteristics Current Sourcing



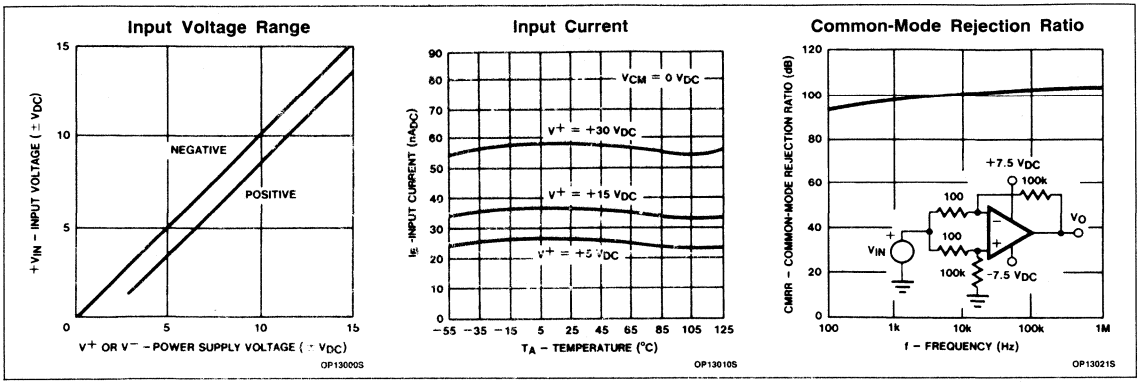
OP12881S

Output Characteristics Current Sinking

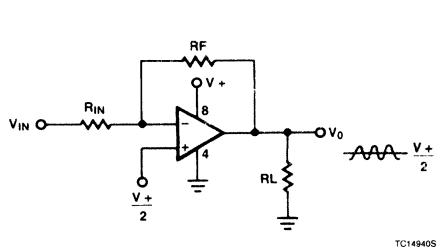


OP12890S

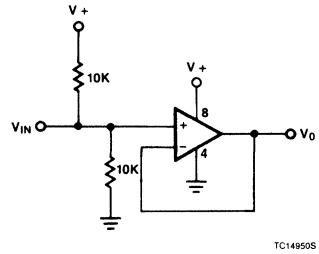
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



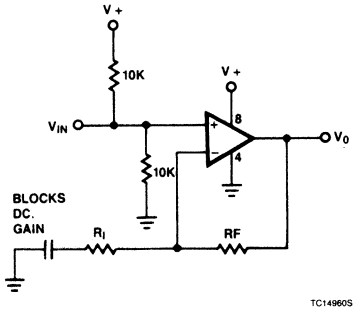
TYPICAL APPLICATIONS



Single Supply Inverting Amplifier



Input Biasing Voltage-Follower



Non-Inverting Amplifier

LM124/224/324/324A/ SA534/LM2902
Low Power Quad Op Amps

Product Specification

DESCRIPTION

The LM124/SA534/LM2902 series consists of four independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

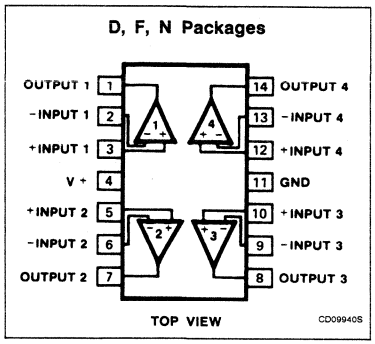
In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain crossover frequency and the input bias current are temperature-compensated.

FEATURES

- **Internally frequency-compensated for unity gain**
- **Large DC voltage gain: 100dB**
- **Wide bandwidth (unity gain): 1MHz (temperature-compensated)**
- **Wide power supply range Single supply: $3V_{DC}$ to $30V_{DC}$ or dual supplies: $\pm 1.5V_{DC}$ to $\pm 15V_{DC}$**
- **Very low supply current drain: essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)**
- **Low input biasing current: $45nA_{DC}$ (temperature-compensated)**
- **Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage: $0V_{DC}$ to $V_{CC} - 1.5V_{DC}$ swing**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	−55°C to +125°C	LM124N
14-Pin Ceramic DIP	−55°C to +125°C	LM124F
14-Pin Plastic DIP	−25°C to +85°C	LM224N
14-Pin Ceramic DIP	−25°C to +85°C	LM224F
14-Pin Plastic DIP	0 to +70°C	LM324N
14-Pin Ceramic DIP	0 to +70°C	LM324F
14-Pin Plastic SO	0 to +70°C	LM324D
14-Pin Plastic DIP	0 to +70°C	LM324AN
14-Pin Plastic SO	0 to +70°C	LM324AD
14-Pin Plastic DIP	−40°C to +85°C	SA534N
14-Pin Ceramic DIP	−40°C to +85°C	SA534F
14-Pin Plastic SO	−40°C to +85°C	SA534D
14-Pin Plastic SO	−40°C to +85°C	LM2902D
14-Pin Plastic DIP	−40°C to +85°C	LM2902N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	32 or ±16	V_{DC}
V_{IN}	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	−0.3 to +32	V_{DC}
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] N package F package D package	 1420 1190 1040	 mW mW mW
	Output short-circuit to GND one amplifier[2] $V_{CC} < 15V_{DC}$ and $T_A = 25°C$	Continuous	
I_{IN}	Input current ($V_{IN} < -0.3V$)[3]	50	mA
T_A	Operating ambient temperature range LM324/A LM224 SA534/LM2902 LM124	 0 to +70 −25 to +85 −40 to +85 −55 to +125	 °C °C °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C
2. Short-circuits from the output to V_{CC}+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC}. At values of supply voltage in excess of $+15V_{DC}$ continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input bias clamps. In addition, there is also lateral NPN parasitic transistor action on the IC chip. This action can cause the output voltages of the op amps to go to the V+ rail (or to ground for a large overdrive) during the time that the input is driven negative.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM124/LM224			LM324/SA534/LM2902			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S = 0\Omega$		±2	±5		±2	±7	mV
		$R_S = 0\Omega$, over temp.			±7			±9	mV
$\Delta V_{OS}/\Delta T$	Temperature drift	$R_S = 0\Omega$, over temp.		7			7		μV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	150		45	250	nA
		$I_{IN}(+)$ or $I_{IN}(-)$, over temp.		40	300		40	500	nA
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50			50		pA/°C
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$		±3	±30		±5	±50	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.			±100			±150	nA
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10			10		pA/°C
V_{CM}	Common-mode voltage range[3]	$V_{CC} \leq 30V$	0		$V_{CC} - 1.5$	0		$V_{CC} - 1.5$	V
		$V_{CC} \leq 30V$, over temp.	0		$V_{CC} - 2$	0		$V_{CC} - 2$	V
CMRR	Common-mode rejection ratio	$V_{CC} = 30V$	70	85		65	70		dB
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $V_{CC} = 30V$, over temp.	26			26			V
V_{OH}	Output voltage high	$R_L \leq 10k\Omega$, $V_{CC} = 30V$, over temp.	27	28		27	28		V
V_{OL}	Output voltage low	$R_L \leq 10k\Omega$, $V_{CC} = 5V$, over temp.		5	20		5	20	mV
I_{CC}	Supply current	$R_L = \infty$, $V_{CC} = 30V$, over temp.		1.5	3		1.5	3	mA
		$R_L = \infty$, $V_{CC} = 5V$, over temp.		0.7	1.2		0.7	1.2	mA
A_{VOL}	Large-signal voltage gain	$V_{CC} = 15V$ (for large V_O swing), $R_L \geq 2k\Omega$	50	100		25	100		V/mV
		$V_{CC} = 15V$ (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	25			15			V/mV
	Amplifier-to-amplifier coupling[5]	f = 1kHz to 20kHz, input referred		−120			−120		dB
PSRR	Power supply rejection ratio	$R_S \leq 0\Omega$	65	100		65	100		dB
I_{OUT}	Output current source	$V_{IN}+ = +1V$, $V_{IN}- = 0V$, $V_{CC} = 15V$	20	40		20	40		mA
		$V_{IN}+ = +1V$, $V_{IN}- = 0V$, $V_{CC} = 15V$, over temp.	10	20		10	20		mA
	sink	$V_{IN}- = +1V$, $V_{IN}+ = 0V$, $V+ = 15V$	10	20		10	20		mA
		$V_{IN}- = +1V$, $V_{IN}+ = 0V$, $V_{CC} = 15V$, over temp.	5	8		5	8		mA
		$V_{IN}- = +1V$, $V_{IN}+ = 0V$, $V_O = 200mV$	12	50		12	50		μA
I_{SC}	Short-circuit current[4]		10	40	60	10	40	60	mA
V_{DIFF}	Differential input voltage[3]				V_{CC}			V_{CC}	V
GBW	Unity gain bandwidth			1			1		MHz
SR	Slew rate			0.3			0.3		V/μs
V_{NOISE}	Input noise voltage	f = 1kHz		40			40		$nV/\sqrt{Hz}$

DC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 5V, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM324A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S = 0\Omega$		±2	±3	mV
		$R_S = 0\Omega$, over temp.			±5	mV
$\Delta V_{OS}/\Delta T$	Temperature drift	$R_S = 0\Omega$, over temp.		7	30	μV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	100	nA
		$I_{IN}(+)$ or $I_{IN}(-)$, over temp.		40	200	nA
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50		pA/°C
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$		±5	±30	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.			±75	nA
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10	300	pA/°C
V_{CM}	Common-mode voltage range[3]	$V_{CC} \leq 30V$	0		$V_{CC} - 1.5$	V
		$V_{CC} \leq 30V$, over temp.	0		$V_{CC} - 2$	V
CMRR	Common-mode rejection ratio	$V_{CC} = 30V$	65	85		dB
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $V_{CC} = 30V$, over temp.	26			V
V_{OH}	Output voltage high	$R_L \leq 10k\Omega$, $V_{CC} = 30V$, over temp.	27	28		V
V_{OL}	Output voltage low	$R_L \leq 10k\Omega$, $V_{CC} = 5V$, over temp.		5	20	mV
I_{CC}	Supply current	$R_L = \infty$, $V_{CC} = 30V$, over temp.		1.5	3	mA
		$R_L = \infty$, $V_{CC} = 5V$, over temp.		0.7	1.2	mA
A_{VOL}	Large-signal voltage gain	$V_{CC} = 15V$ (for large V_O swing), $R_L \geq 2k\Omega$	25	100		V/mV
		$V_{CC} = 15V$ (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	15			V/mV
	Amplifier-to-amplifier coupling[5]	f = 1kHz to 20kHz, input referred		−120		dB
PSRR	Power supply rejection ratio	$R_S \leq 0\Omega$	65	100		dB
I_{OUT}	Output current source	$V_{IN}+ = +1V$, $V_{IN}- = 0V$, $V_{CC} = 15V$	20	40		mA
		$V_{IN}+ = +1V$, $V_{IN}- = 0V$, $V_{CC} = 15V$, over temp.	10	20		mA
	sink	$V_{IN}- = +1V$, $V_{IN}+ = 0V$, $V+ = 15V$	10	20		mA
		$V_{IN}- = +1V$, $V_{IN}+ = 0V$, $V_{CC} = 15V$, over temp.	5	8		mA
		$V_{IN}- = +1V$, $V_{IN}+ = 0V$, $V_O = 200mV$	12	50		μA
I_{SC}	Short-circuit current[4]		10	40	60	mA
V_{DIFF}	Differential input voltage[3]				V_{CC}	V

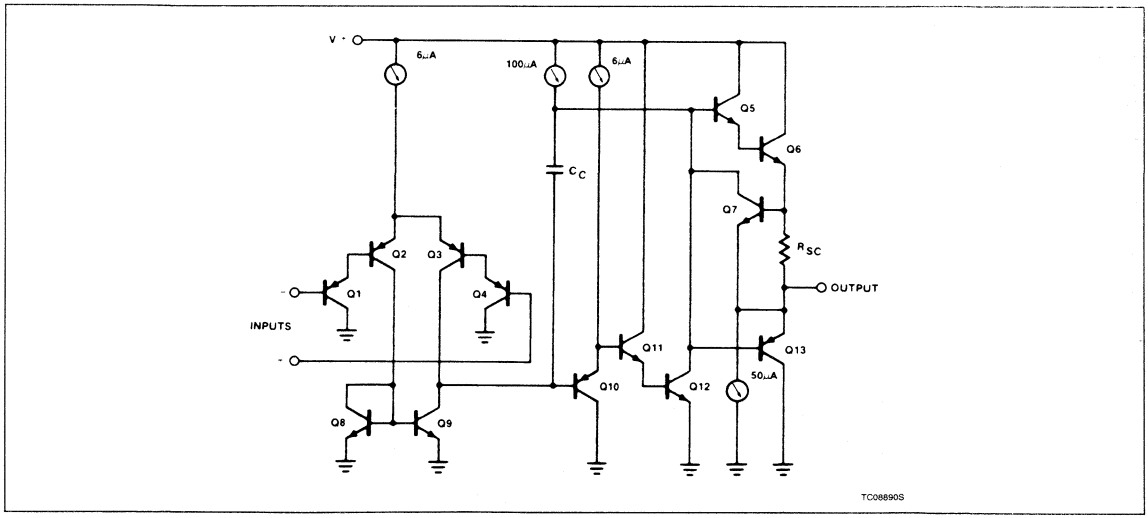
DC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 5V, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM324A			UNIT
			Min	Typ	Max	
GBW	Unity gain bandwidth			1		MHz
SR	Slew rate			0.3		V/μs
V_{NOISE}	Input noise voltage	f = 1kHz		40		nV/√Hz

NOTES:

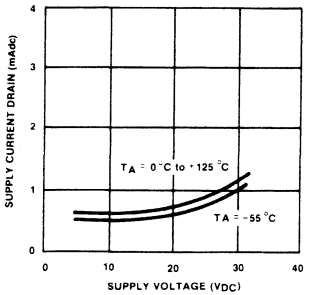
1. $V_O \cong 1.4V_{DC}$, $R_S = 0\Omega$ with V_{CC} from 5V to 30V and over full input common-mode range ($0V_{DC}$+ to V_{CC} − 1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC} − 1.5, but either or both inputs can go to +32V without damage.
4. Short-circuits from the output to V_{CC} can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.

EQUIVALENT SCHEMATIC



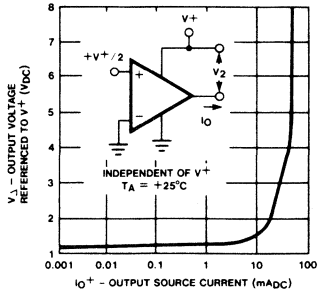
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current



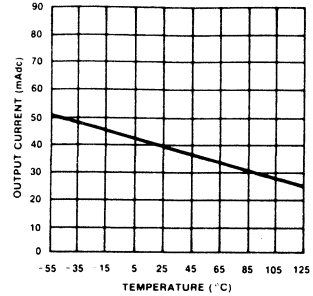
OP05450S

Output Characteristics Current Sourcing



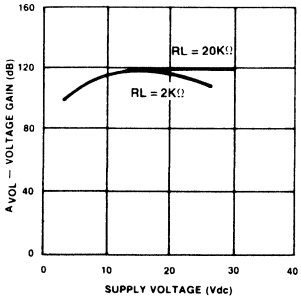
OP05460S

Current Limiting



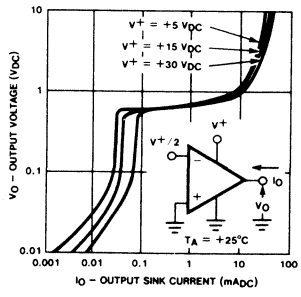
OP05470S

Voltage Gain



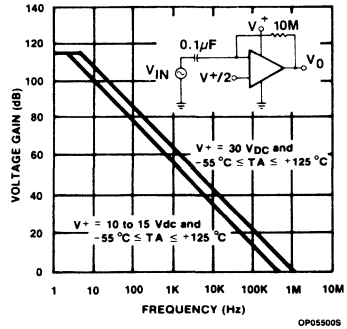
OP05480S

Output Characteristics Current Sinking



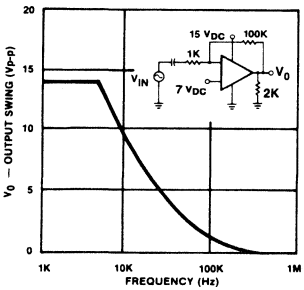
OP05490S

Open-Loop Frequency Response



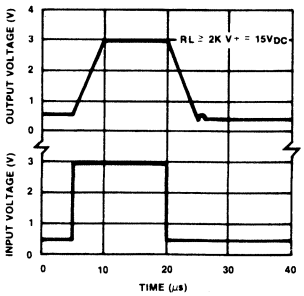
OP05500S

Large-Signal Frequency Response



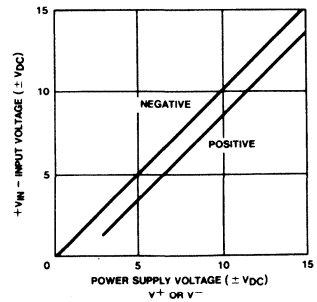
OP05510S

Voltage-Follower Pulse Response



OP05520S

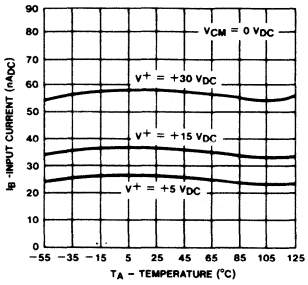
Input Voltage Range



OP05530S

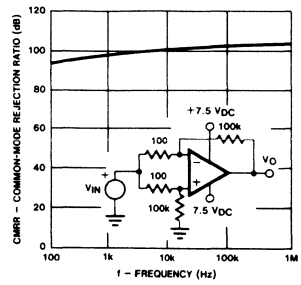
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Input Current



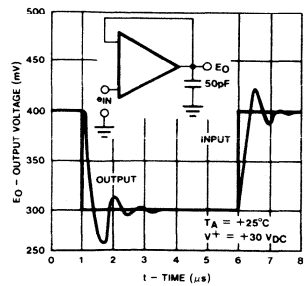
OP05540S

Common-Mode Rejection Ratio



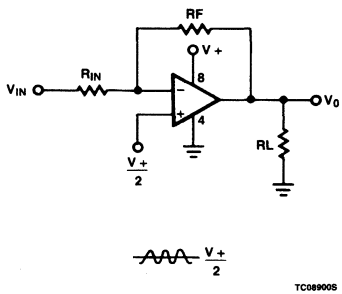
OP05550S

Voltage-Follower Pulse Response (Small-Signal)



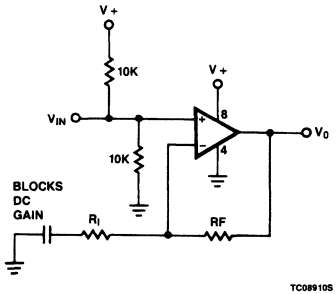
OP05560S

TYPICAL APPLICATIONS



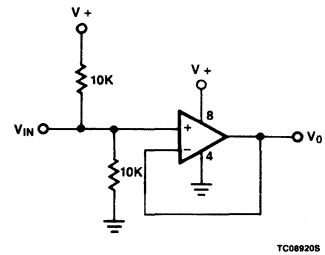
TC08900S

Single Supply Inverting Amplifier



TC08910S

Non-Inverting Amplifier



TC08920S

Input Biasing Voltage-Follower

NE/SA/SE532/ LM158/258/358/A/2904

Low Power Dual Operational Amplifiers

Product Specification

DESCRIPTION

The 532/358/LM2904 consists of two independent, high gain, internally frequency-compensated operational amplifiers internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage.

UNIQUE FEATURES

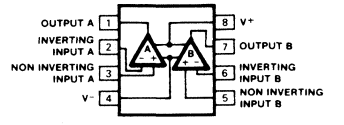
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature-compensated. The input bias current is also temperature-compensated.

FEATURES

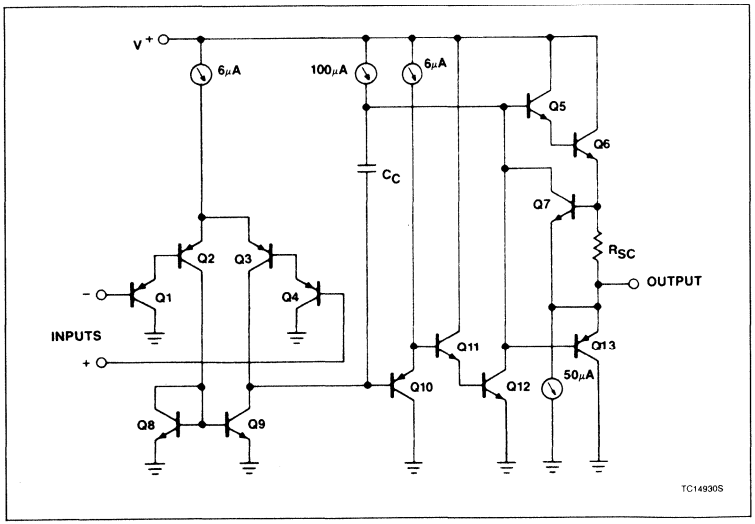
- **Internally frequency-compensated for unity gain**
- **Large DC voltage gain — 100dB**
- **Wide bandwidth (unity gain) — 1MHz (temperature-compensated)**
- **Wide power supply range single supply — $3V_{DC}$ to $30V_{DC}$ or dual supplies — $\pm 1.5V_{DC}$ to $\pm 15V_{DC}$**
- **Very low supply current drain ($400\mu A$) — essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)**
- **Low input biasing current — $45nA_{DC}$ temperature-compensated**
- **Low input offset voltage — $2mV_{DC}$ and offset current — $5nA_{DC}$**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage — $0V_{DC}$ to V+ $1.5V_{DC}$ swing**

PIN CONFIGURATIONS

D, FE, N Packages



EQUIVALENT CIRCUIT



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE532D
8-Pin Plastic DIP	0 to +70°C	NE532N
8-Pin Ceramic DIP	0 to +70°C	NE532FE
8-Pin Plastic SO	−40°C to +85°C	SA532D
8-Pin Plastic DIP	−40°C to +85°C	SA532N
8-Pin Ceramic DIP	−40°C to +85°C	SA532FE
8-Pin Plastic SO	−40°C to +85°C	LM2904D
8-Pin Plastic DIP	−40°C to +85°C	LM2904N
8-Pin Ceramic DIP	−55°C to +125°C	LM158FE
8-Pin Plastic DIP	−25°C to +85°C	LM258N
8-Pin Plastic SO	−25°C to +85°C	LM258D
8-Pin Plastic SO	0 to +70°C	LM358D
8-Pin Plastic DIP	0 to +70°C	LM358N
8-Pin Plastic DIP	0 to +70°C	LM358AN
8-Pin Plastic SO	0 to +70°C	LM358AD
8-Pin Plastic DIP	−55°C to +125°C	SE532N
8-Pin Ceramic DIP	−55°C to +125°C	SE532FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage, V+	32 or ±16	V_{DC}
	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	−0.3 to +32	V_{DC}
P_D	Maximum power dissipation T_A = 25°C (Still air)[1] FE package N package D package	 780 1160 780	 mW mW mW
	Output short-circuit to GND[5] V+ < 15 V_{DC} and T_A = 25°C	 Continuous	
T_A	Operating ambient temperature range NE532/LM358/LM358A LM258 SA532/LM2904 SE532/LM158	 0 to +70 −25 to +85 −40 to +85 −55 to +125	 °C °C °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:
1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V+ = +5V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE/SA532/LM358/ LM2904			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S = 0\Omega$ $R_S = 0\Omega$, over temp.		±2	±5 ±7		±2	±7 ±9	mV mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		7			7		µV/°C
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$ Over temp.		±3	±30 ±100		±5	±50 ±150	nA nA
I_{OS}	Drift	Over temp.		10			10		pA/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$ Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		45 40	150 300		45 40	250 500	nA nA
I_B	Drift	Over temp.		50			50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+ = 30V Over temp., V+ = 30V	0 0		V+ – 1.5 V+ – 2.0	0 0		V+ – 1.5 V+ – 2.0	V V
CMRR	Common-mode rejection ratio	V+ = 30V	70	85		65	70		dB
V_{OH}	Output voltage swing	$R_L \geq 2k\Omega$, V+ = 30V, over temp. $R_L \geq 10k\Omega$, V+ = 30V, over temp.	26 27	28		26 27	28		V V
V_{OL}	Output voltage swing	$R_L \geq 10k\Omega$, over temp.		5	20		5	20	mV
I_{CC}	Supply current	$R_L = \infty$, V+ = 30V $R_L = \infty$ on all amplifiers, over temp., V+ = 30V		0.5 0.6	1.0 1.2		0.5 0.6	1.0 1.2	mA mA
A_{VOL}	Large-signal voltage gain	$R_L \geq 2k\Omega$, V_{OUT} ±10V, V+ = 15V (for large V_O swing) over temp.	50 25	100		25 15	100		V/mV V/mV
PSRR	Supply voltage rejection ratio	$R_S = 0\Omega$	65	100		65	100		dB
	Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		–120			–120		dB
I_{OUT}	Output current Source	$V_{IN+} = +1V_{DC}$, $V_{IN-} = 0V_{DC}$, $V+ = 15V_{DC}$	20	40		20	40		mA
		$V_{IN+} = +1V_{DC}$, $V_{IN-} = 0V_{DC}$, $V+ = 15V_{DC}$, over temp.	10	20		10	20		mA
	Sink	$V_{IN-} = +1V_{DC}$, $V_{IN+} = 0V_{DC}$, $V+ = 15V_{DC}$	10	20		10	20		mA
		$V_{IN-} = +1V_{DC}$, $V_{IN+} = 0V_{DC}$, $V+ = 15V_{DC}$, over temp.	5	8		5	8		mA
		$V_{IN+} = 0V$, $V_{IN-} = +1V_{DC}$, $V_O = 200mV$	12	50		12	50		µA
I_{SC}	Short circuit current[5]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V
GBW	Unity gain bandwidth	$T_A = 25°C$		1			1		MHz
SR	Slew rate	$T_A = 25°C$		0.3			0.3		V/µs
V_{NOISE}	Input noise voltage	$T_A = 25°C$, f = 1kHz		40			40		$nV/\sqrt{Hz}$

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V+ = +5V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM358A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S = 0\Omega$ $R_S = 0\Omega$, over temp.		±2	±3 ±5	mV mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		7	20	μV/°C
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$ Over temp.		5	±30 ±75	nA nA
I_{OS}	Drift	Over temp.		10	300	pA/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$ Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		45 40	100 200	nA nA
I_B	Drift	Over temp.		50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+ = 30V Over temp., V+ = 30V	0 0		V+ – 1.5 V+ – 2.0	V V
CMRR	Common-mode rejection ratio	V+ = 30V	65	85		dB
V_{OH}	Output voltage swing	$R_L \geq 2k\Omega$, V+ = 30V, over temp. $R_L \geq 10k\Omega$, V+ = 30V, over temp.	26 27	 28		V V
V_{OL}	Output voltage swing	$R_L \geq 10k\Omega$, over temp.		5	20	mV
I_{CC}	Supply current	$R_L = \infty$, V+ = 30V $R_L = \infty$ on all amplifiers, over temp., V+ = 30V		0.5 0.6	1.0 1.2	mA mA
A_{VOL}	Large-signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} \pm 10V$, V+ = 15V (for large V_O swing) over temp.	25 15	100		V/mV V/mV
PSRR	Supply voltage rejection ratio	$R_S = 0\Omega$	65	100		dB
	Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		–120		dB
I_{OUT}	Output current Source	$V_{IN+} = +1V_{DC}$, $V_{IN-} = 0V_{DC}$, $V+ = 15V_{DC}$ $V_{IN+} = +1V_{DC}$, $V_{IN-} = 0V_{DC}$, $V+ = 15V_{DC}$, over temp.	20 10	40 20		mA mA
	Sink	$V_{IN-} = +1V_{DC}$, $V_{IN+} = 0V_{DC}$, $V+ = 15V_{DC}$ $V_{IN-} = +1V_{DC}$, $V_{IN+} = 0V_{DC}$, $V+ = 15V_{DC}$, over temp. $V_{IN+} = 0V$, $V_{IN-} = +1V_{DC}$, $V_O = 200mV$	10 5 12	20 8 50		mA mA μA

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$, V+ = +5V, unless otherwise specified.

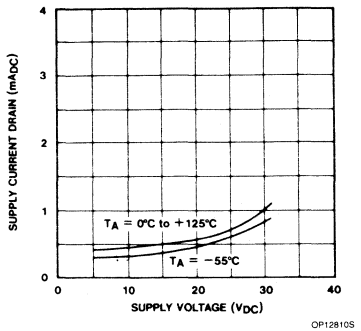
SYMBOL	PARAMETER	TEST CONDITIONS	LM358A			UNIT
			Min	Typ	Max	
I_{SC}	Short circuit current[5]			40	60	mA
	Differential input voltage[6]				V+	V
GBW	Unity gain bandwidth	$T_A = 25°C$		1		MHz
SR	Slew rate	$T_A = 25°C$		0.3		V/μs
V_{NOISE}	Input noise voltage	$T_A = 25°C$, f = 1kHz		40		nV/√Hz

NOTES:

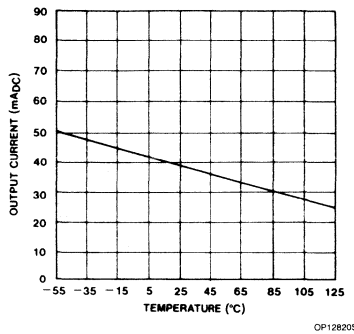
1. $V_O \cong 1.4V$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common-mode range (0V to V+ −1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance coupling increases at higher frequencies.
5. Short-circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to $+32V_{DC}$ without damage.

TYPICAL PERFORMANCE CHARACTERISTICS

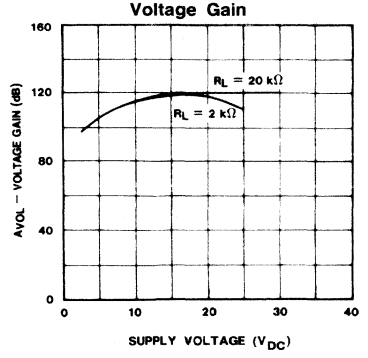
Supply Current



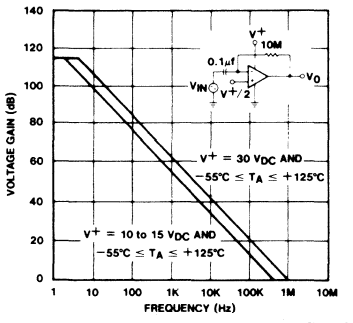
Current Limiting



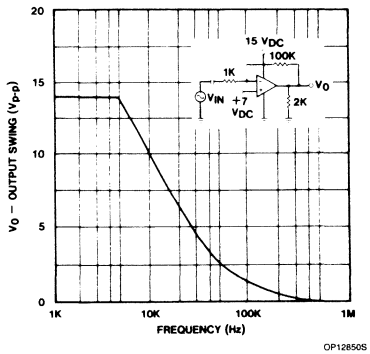
Voltage Gain



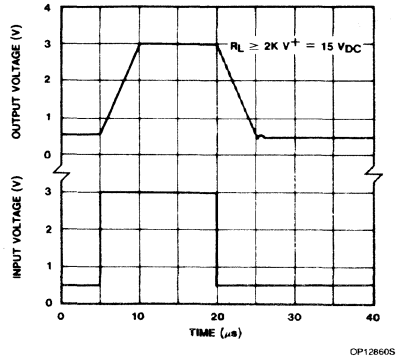
Open-Loop Frequency Response



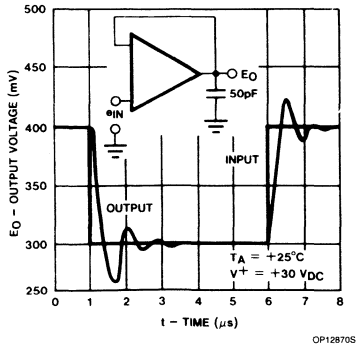
Large-Signal Frequency Response



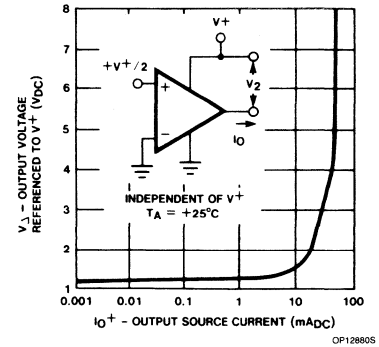
Voltage-Follower Pulse Response



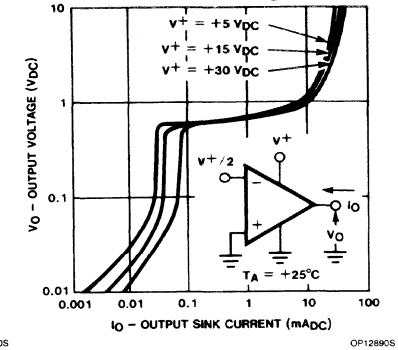
Voltage-Follower Pulse Response (Small-Signal)



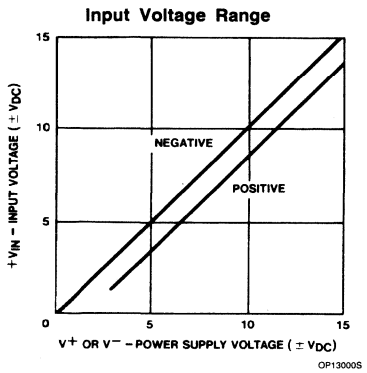
Output Characteristics Current Sourcing

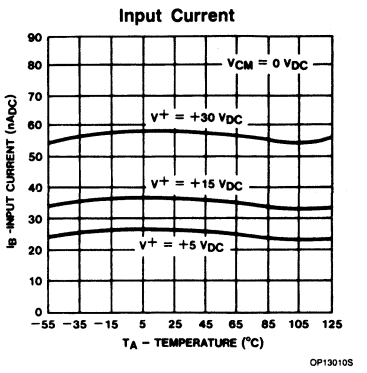


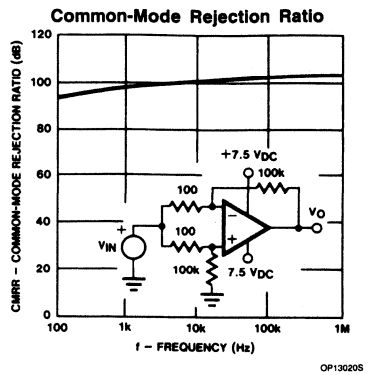
Output Characteristics Current Sinking



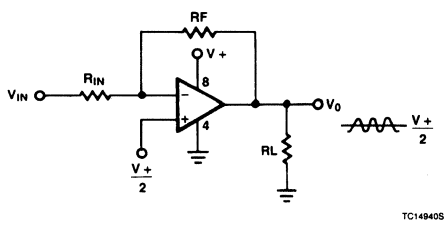
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



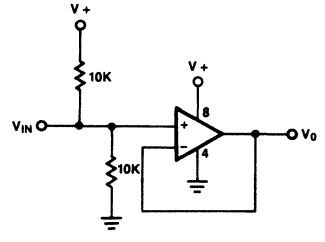




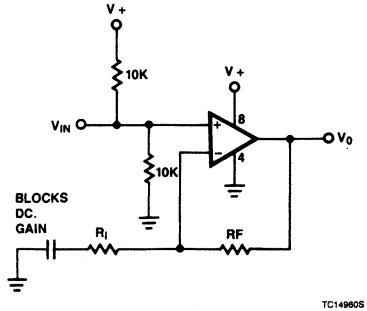
TYPICAL APPLICATIONS



Single Supply Inverting Amplifier



Input Biasing Voltage Follower



Non-Inverting Amplifier

MC/SA1458/MC1558
General-Purpose Operational Amplifier

Product Specification

DESCRIPTION

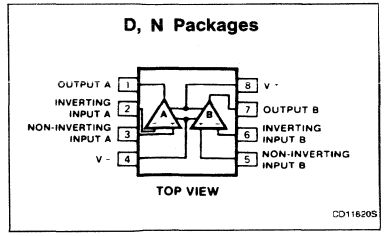
The MC1458 is a high-performance operational amplifier with high open-loop gain, internal compensation, high common-mode range and exceptional temperature stability. The MC1458 is short-circuit protected.

The MC1458/SA1458/MC1558 consists of a pair of 741 operational amplifiers on a single chip.

FEATURES

- **Internal frequency compensation**
- **Short-circuit protection**
- **Excellent temperature stability**
- **High input voltage range**
- **No latch-up**
- **1558/1458 are 2 "op amps" in space of one 741 package**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	MC1458D
8-Pin Plastic DIP	0 to +70°C	MC1458N
8-Pin Plastic SO	−40°C to +85°C	SA1458D
8-Pin Plastic DIP	−40°C to +85°C	SA1458N
8-Pin Plastic DIP	−55°C to +125°C	MC1558N

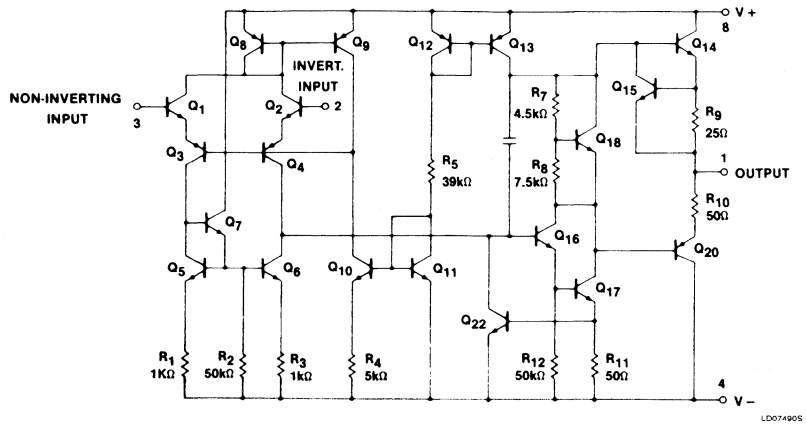
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage		
	MC1458	±18	V
	SA1458	±18	V
	MC1558	±22	V
T_J	Junction temperature	+150	°C
$P_{D\ MAX}$	Maximum power dissipation, T_A = 25°C (still-air)[1]		
	N package	1160	mW
	D package	780	mW
V_{DIFF}	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
	Output short-circuit duration	Continuous	
T_A	Operating ambient temperature range		
	MC1458	0 to +70	°C
	SA1458	−40 to +85	°C
	MC1558	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. The following derating factors should be applied above 25°C:
   N package at 9.3mW/°C
   D package at 6.2mW/°C.
2. For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC



Amplifier "A" of MC1458, SA1458, MC1558

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1558			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		1.0	5.0	mV
		$R_S = 10k\Omega$, over temperature			6.0	mV
ΔV_{OS}	Offset voltage	Over temperature		10		$\mu V/°C$
I_{OS}	Offset current			20	200	nA
		Over temperature			500	nA
ΔI_{OS}	Offset current	Over temperature		0.10		nA/°C
I_{BIAS}	Input bias current			80	500	nA
		Over temperature			1500	nA
ΔI_{BIAS}	Bias current	Over temperature		1.0		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$, over temperature	±12	±14		V
		$R_L = 2k\Omega$, over temperature	±10	±13		V
A_{VOL}	Large-signal voltage gain	$R_L = 2k\Omega, V_O = \pm 10V$	50	100		V/mV
		$R_L = 2k\Omega$, $V_O = \pm$ temperature	20			V/mV
	Offset voltage adjustment range			±30		mV
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$		30	150	$\mu V/V$
CMRR	Common mode rejection ratio		70	90		dB
I_{CC}	Supply current			2.3	5.0	mA
V_{IN}	Input voltage range		±12	±13		V
P_D	Power consumption			70	150	mW
	Channel separation			120		dB
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current		10	25	60	mA

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified.

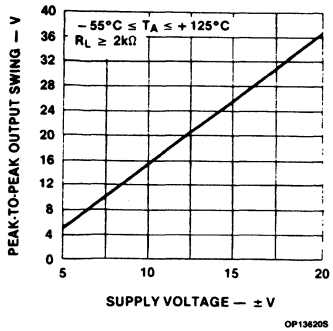
SYMBOL	PARAMETER	TEST CONDITIONS	MC1458			SA1458			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		2.0	6.0		2.0	6.0	mV
		$R_S = 10k\Omega$, over temp.			7.5			7.5	mV
ΔV_{OS}	Offset voltage	Over temperature		12			12		$\mu V/°C$
I_{OS}	Offset current			20	200		20	200	nA
		Over temperature			300			500	nA
ΔI_{OS}	Offset current	Over temperature		0.10			0.10		nA/°C
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temperature			800			1500	nA
ΔI_{BIAS}	Bias current	Over temperature		1.0			1.0		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$, over temp.	± 12	± 14		± 12	± 14		V
		$R_L = 2k\Omega$, over temp.	± 10	± 13		± 10	± 13		V
A_{VOL}	Large-signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	25	200		20	200		V/mV
		$R_L = 2k\Omega$, $V_O = \pm 10V$, Over temperature	15			15			V/mV
	Offset voltage adjustment range			± 30			± 30		mV
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$		30	150		30	150	$\mu V/V$
CMRR	Common-mode rejection ratio		70	90		70	90		dB
I_{CC}	Supply current			2.3	5.6		2.3	5.6	mA
V_{IN}	Input voltage range		± 12	± 13		± 12	± 13		V
R_{IN}	Input resistance		0.3	1		0.3	1		MΩ
P_D	Power consumption			70	170		70	170	mW
	Channel separation			120			120		dB
I_{SC}	Output short-circuit current			25			25		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

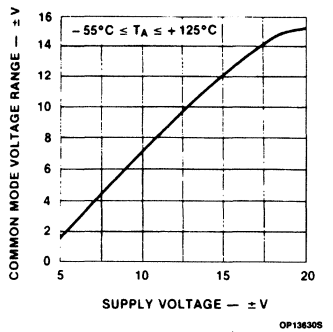
SYMBOL	PARAMETER	TEST CONDITIONS	MC1458, SA1458, MC1558			UNIT
			Min	Typ	Max	
R_{IN}	Parallel input resistance	Open-loop, f = 20Hz	0.3			MΩ
	Common-mode input impedance	f = 20Hz		200		MΩ
	Equivalent input noise voltage	$A_V = 100$, $R_S = 10k\Omega$, BW = 1.0kHz, f = 1.0kHz		30		$nV/\sqrt{Hz}$
BW	Power bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, THD $\leq 5\%$, $V_{OUT} = 20V_{P-P}$		14		kHz
	Phase margin			65		degrees
A_V	Gain margin			11		dB
	Unity gain crossover frequency	Open loop		1.0		MHz
	Transient response unity gain	$V_{IN} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$				
t_R	Rise time			0.3		μs
	Overshoot			5.0		%
SR	Slew rate	$C_L \leq 100pF$, $R_L \geq 2k\Omega$, $V_{IN} = \pm 10V$		0.8		$V/\mu s$

TYPICAL PERFORMANCE CHARACTERISTICS

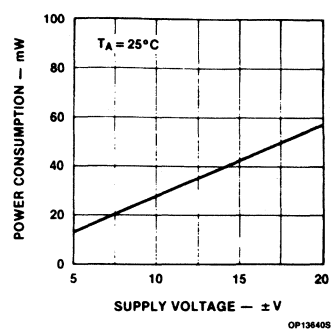
Output Voltage Swing as a Function of Supply Voltage



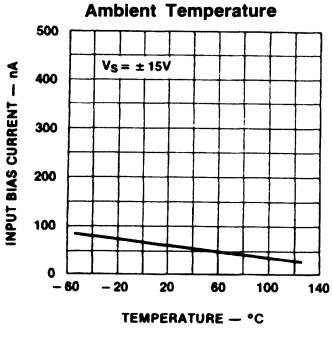
Input Common-Mode Voltage Range as a Function of Supply Voltage



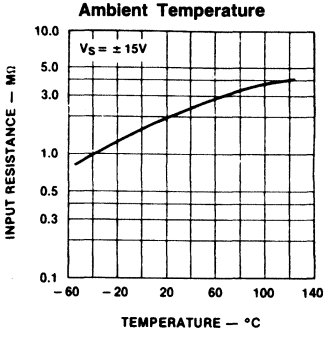
Power Consumption as a Function of Supply Voltage



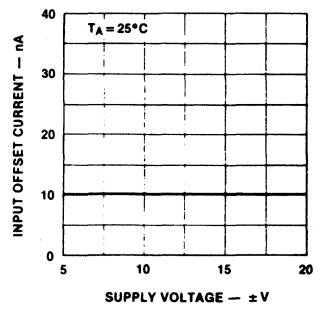
Input Bias Current as a Function of Ambient Temperature



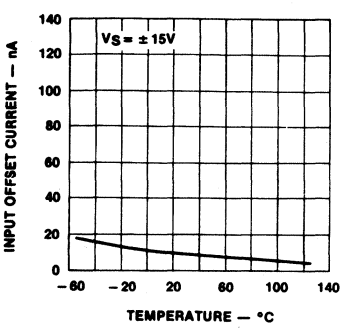
Input Resistance as a Function of Ambient Temperature



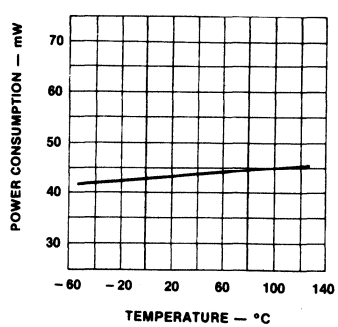
Input Offset Current as a Function of Supply Voltage



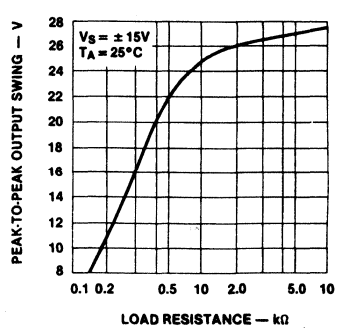
Input Offset Current as a Function of Ambient Temperature



Power Consumption as a Function of Ambient Temperature

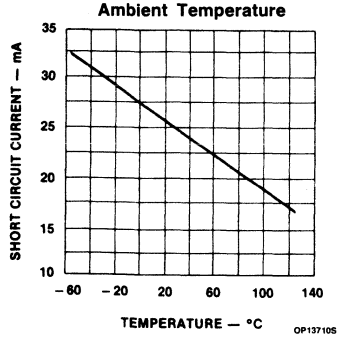


Output Voltage Swing as a Function of Load Resistance

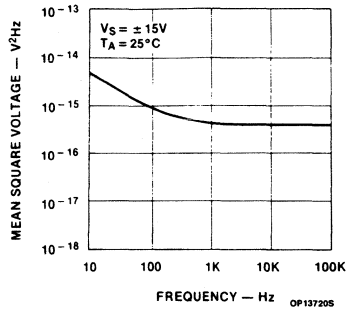


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

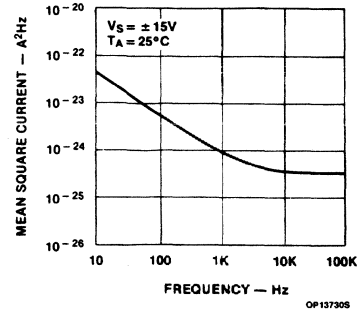
Output Short-Circuit Current as a Function of Ambient Temperature



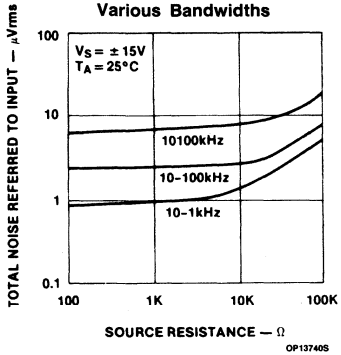
Input Noise Voltage as a Function of Frequency



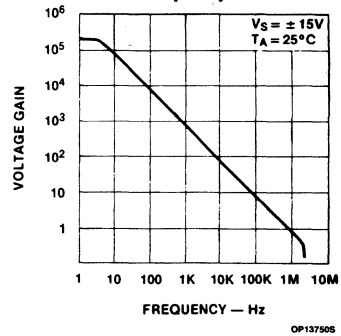
Input Noise Current as a Function of Frequency



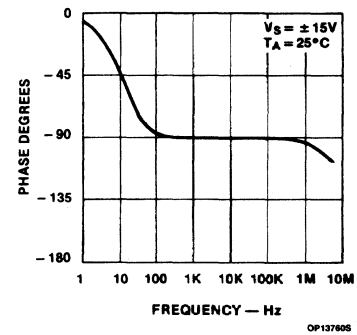
Broadband Noise for Various Bandwidths



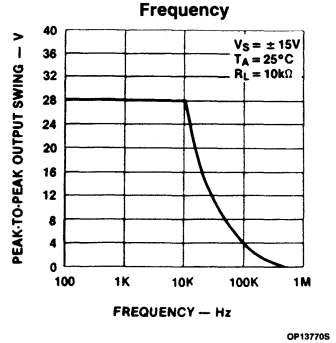
Open-Loop Voltage Gain as a Function of Frequency



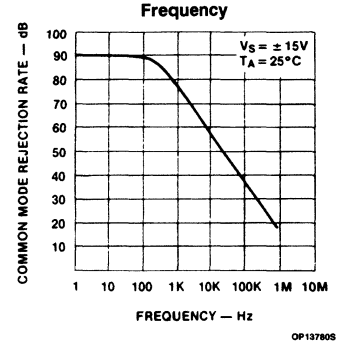
Open-Loop Phase Response as a Function of Frequency



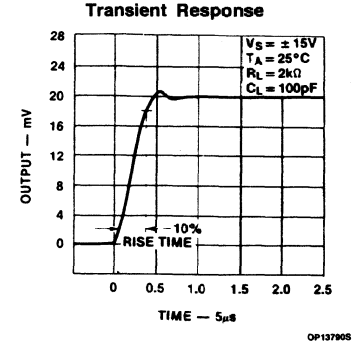
Output Voltage Swing as a Function of Frequency



Common-Mode Rejection Ratio as a Function of Frequency

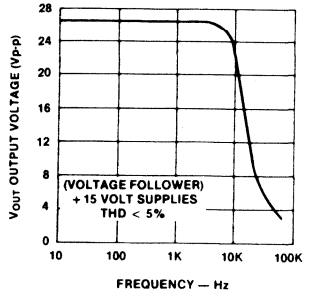


Transient Response



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Power Bandwidth
(Large-Signal Swing vs Frequency)



MC3303/3403/3503
Quad Low Power Operational Amplifiers

Product Specification

DESCRIPTION

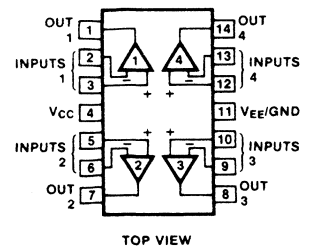
The MC3403 is a quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular μA741. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The MC3403 can operate at supply voltages as low as 3.0V or as high as 32V. The common-mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

FEATURES

- **Short-circuit protected outputs**
- **Class AB output stage for minimal crossover distortion**
- **True differential input stage**
- **Single supply operation: 3.0 to 32V**
- **Split supply operation: ± 1.5 to ± 16V**
- **Low input bias currents: 500nA max**
- **Four amplifiers per package**
- **Internally compensated**

PIN CONFIGURATION

D, F, N, Packages



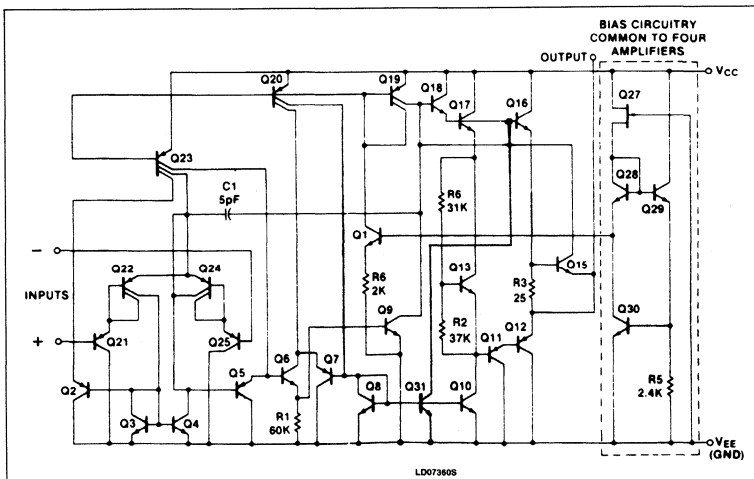
TOP VIEW

CD11580S

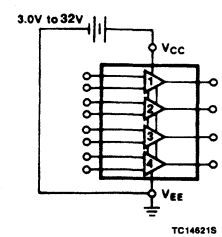
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	−40°C to +85°C	MC3303D
14-Pin Ceramic DIP	−40°C to +85°C	MC3303F
14-Pin Plastic DIP	−40°C to +85°C	MC3303N
14-Pin Plastic SO	0 to +70°C	MC3403D
14-Pin Ceramic DIP	0 to +70°C	MC3403F
14-Pin Plastic DIP	0 to +70°C	MC3403N
14-Pin Ceramic DIP	−55°C to +125°C	MC3503F

CIRCUIT SCHEMATIC (¼ Shown)

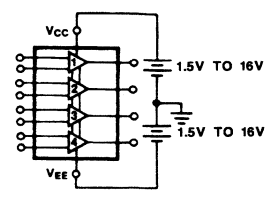


LD07360S



TC14621S

Single Supply



TC14631S

Split Supplies

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Power supply voltage[3]		
V_{CC}	Single supply	36	V_{DC}
V_{CC}	Split supplies	+18	V_{DC}
V_{EE}		−18	V_{DC}
V_{IDR}	Input differential voltage range[1]	±36	V_{DC}
V_{ICR}	Input common-mode voltage range[1, 2]	±18	V_{DC}
$P_{D\ MAX}$	Maximum power dissipation, T_A = 25°C (still-air)[4]		
	F package	1.20	W
	D package	1.04	W
	N package	1.45	W
T_{STG}	Storage temperature range		
	Ceramic	−65 to +150	°C
	Plastic	−55 to +125	
T_A	Operating ambient temperature range		
	MC3503	−55 to +125	°C
	MC3403	0 to +70	°C
	MC3303	−40 to +85	°C
T_J	Junction temperature	150	°C

NOTES:
1. Split power supplies.
2. For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
3. Device not functional for single supply > 32V or split supply > ± 16V.
4. Derate above 25°C at the following rates:
   F package at 9.5mW/°C
   D package at 8.7mW/°C
   N package at 11.6mW/°C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = +15V, V_{EE} = −15V for MC3503, MC3403; V_{CC} = +14V, V_{EE} = GND for MC3303. T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input offset voltage	$T_A = T_{HIGH}$ to T_{LOW}		2.0 6.0	5.0 6.0		2.0	10 12		2.0	8.0 10	mV
I_{IO}	Input offset current	$T_A = T_{HIGH}$ to T_{LOW}		10	50 200		10	50 200		30	75 250	nA
A_{VOL}	Large-signal open-loop voltage gain	V_O = ±10V, V_O = ±10V R_L = 2.0kΩ $T_A = T_{HIGH}$ to T_{LOW}	50 50 25	200 200 300		20 20 15	200 200		20 20 15	200 200		V/mV
I_{BIAS}	Input bias current	$T_A = T_{HIGH}$ to T_{LOW}		−30 −40	−500 −1200		−30	−500 −800		−30	−500 −1000	nA
Z_O	Output impedance	f = 20Hz		75			75			75		Ω
Z_I	Input impedance	f = 20Hz	0.3	1.0		0.3	1.0		0.3	1.0		MΩ
V_{OR}	Output voltage range	R_L = 10kΩ R_L = 2.0kΩ R_L = 2.0kΩ $T_A = T_{HIGH}$ to T_{LOW}	±12 ±10 ±10	±13.5 ±13		±12 ±10 ±10	±13.5 ±13		+12 +10 +10	+12.5 +12		V

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = +15V, V_{EE} = −15V for MC3503, MC3403; V_{CC} = +14V, V_{EE} = GND for MC3303. T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{ICR}	Input common-mode voltage range		+13 $-V_{EE}$	+13.5 $-V_{EE}$		+13 $-V_{EE}$	+13.5 $-V_{EE}$		+12 $-V_{EE}$	+12.5 $-V_{EE}$		V
CMRR	Common-mode rejection ratio	$R_S \leq 10k\Omega$	70	90		70	90		70	90		dB
I_{CC}, I_{EE}	Power supply current (V_O = 0)	$R_L = \infty$		2.5	4.0		2.5	7.0		2.5	7.0	mA
		$T_A = T_{HIGH}$ to T_{LOW}		3.5	5.0		3.5	7.0		3.5	7.0	mA
$I_{OS}\pm$	Individual output short-circuit current[1]		±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
PSSR+	Positive power supply rejection ratio			30	150		30	150		30	150	μV/V
PSSR−	Negative power supply rejection ratio			30	150		30	150				μV/V
$\Delta I_B/\Delta T$	Average temperature coefficient of input bias current	$T_A = T_{HIGH}$ to T_{LOW}		50			50			50		pA/°C
$\Delta I_{IO}/\Delta T$	Average temperature coefficient of input offset current	$T_A = T_{HIGH}$ to T_{LOW}		50			50			50		pA/°C
$\Delta V_{IO}/\Delta T$	Average temperature coefficient of input offset voltage	$T_A = T_{HIGH}$ to T_{LOW}		10			10			10		μV/°C
BW_P	Power bandwidth	A_V = 1, R_L = 2.0kΩ, V_O = $20V_{P-P}$ THD = 5%		9.0			9.0			9.0		kHz
BW	Small-signal bandwidth	A_V = 1, R_L = 10kΩ, V_O = 50mV		1.0			1.0			1.0		MHz
SR	Slew rate	A_V = 1, V_I = −10V to +10V		0.6			0.6			0.6		V/μs
t_{TLH}	Rise time	A_V = 1, R_L = 10kΩ, V_O = 50mV		0.35			0.35			0.35		μs
t_{THL}	Fall time	A_V = 1, R_L = 10kΩ, V_O = 50mV		0.35			0.35			0.35		μs
OS	Overshoot	A_V = 1, R_L = 10kΩ, V_O = 50mV		20			20			20		%
θm	Phase margin	A_V − 1, R_L − 2.0kΩ, C_L = 200pF		50			50			50		Deg
	Crossover distortion	V_{IN} = $30mV_{P-P}$, V_{OUT} = $2.0V_{P-P}$, f = 10kHz		1.0			1.0			1.0		%

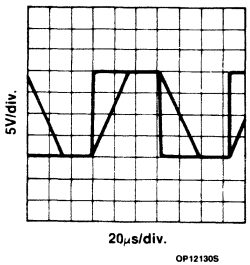
DC AND AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V, V_E = GND, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input offset voltage			2.0	5.0		2.0	10.0			10.0	mV
I_{IO}	Input offset current			30	50		30	50			75	nA
I_{BIAS}	Input bias current			−200	−500		−200	−500			−500	nA
A_{VOL}	Large-signal open-loop voltage gain	R_L = 2.0kΩ	10	200		10	200		10	200		V/mV
PSRR	Power supply rejection ratio				150			150			150	μV/V
V_{OR}	Output voltage range[2]	R_L = 10kΩ, V_{CC} = 5.0V	3.3	3.5		3.3	3.5		3.3	3.5		V_p
		R_L = 10kΩ, 5.0V ≤ V_{CC} ≤ 30V	V_{CC} −1.7	V_{CC} −1.5		V_{CC} −1.7	V_{CC} −1.5		V_{CC} −1.7	V_{CC} −1.5		
I_{CC}	Power supply current			2.5	4.0		2.5	7.0		2.5	7.0	mA
	Channel separation	f = 1.0kHz to 20kHz (input referenced)		−120			−120			−120		dB

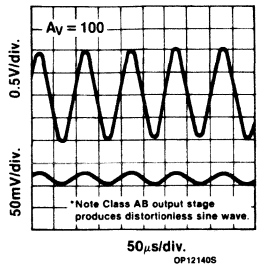
NOTES:
1. Not to exceed maximum package power dissipation.
2. Output will swing to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

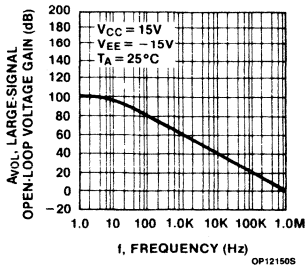
Inverter Pulse Response



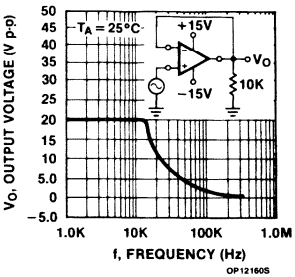
Sine Wave Response



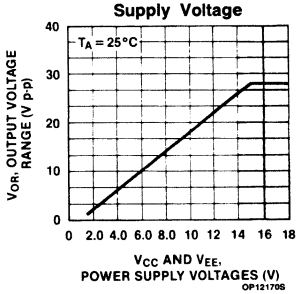
Open-Loop Frequency Response



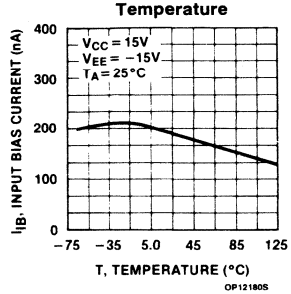
Power Bandwidth



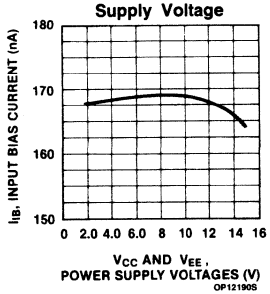
Output Swing vs Supply Voltage



Input Bias Current vs Temperature



Input Bias Current vs Supply Voltage



NE/SE530
High Slew Rate Operational Amplifier

Product Specification

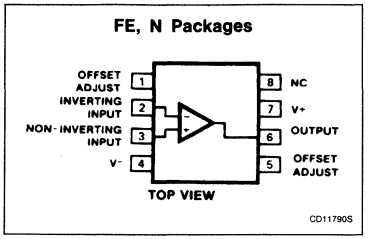
DESCRIPTION

The 530 is a new generation operational amplifier featuring a high slew rate combined with improved input characteristics. Internally compensated, the SE530 guarantees slew rates of 25V/μs with 2mV typical offset voltage. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers such as the 741 and LF356 types.

FEATURES

- **Gain bandwidth product — 3MHz**
- **35V/μs slew rate (gain = −1)**
- **Internal frequency compensation**
- **Low input offset voltage 2mV typical**
- **Low input bias current — 65nA typical**
- **Short-circuit protection**
- **Offset null capability**
- **Large common-mode and differential voltage ranges**

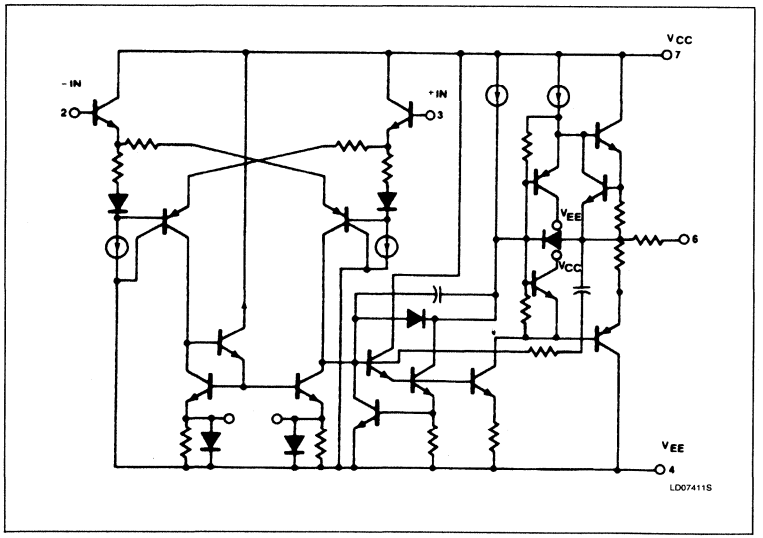
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE530N
8-Pin Ceramic DIP	0 to +70°C	NE530FE
8-Pin Plastic DIP	−55°C to +125°C	SE530N
8-Pin Ceramic DIP	−55°C to +125°C	SE530FE

EQUIVALENT SCHEMATIC EACH AMPLIFIER



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage SE530 NE530	 ±22 ±18	 V V
$P_{D\ MAX}$	Maximum power dissipation T_A = 25°C (still air)[1] F package N package	 830 1200	 mW mW
V_{DIFF}	Differential input voltage	±30	V
V_{IN}	Input voltage	±15	V
T_A	Operating temperature range SE530 NE530	 −55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
I_{SC}	Output short circuit	Indefinite	

NOTE:
1. Derate above 25°C, at the following rates:
   F package at 6.7mW/°C
   N package at 9.6mW/°C

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = ±15V, unless otherwise specified.

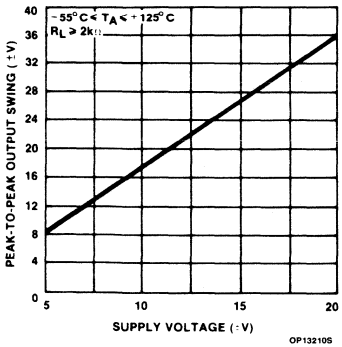
SYMBOL	PARAMETER	TEST CONDITIONS	SE530			NE530			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$ Over temperature		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
ΔV_{OS}	Temperature coefficient of input offset voltage	Over temperature		3	15		6		µV/°C
I_{OS}	Input offset current	 Over temperature		5	20 40		15	40 80	nA nA
ΔI_{OS}	Input offset current	Over temperature		25			40		pA/°C
I_{BIAS}	Input bias current	 Over temperature		45	80 200		65	150 200	nA nA
ΔI_{BIAS}	Input current	Over temperature		50			80		pA/°C
R_{IN}	Input resistance		3	10		1	6		MΩ
V_{CM}	Input common mode voltage range		±12	±13		±12	±13		V
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, V_O = ±10V Over temperature	50 25	200		50 25	200		V/mV V/mV
V_{OUT}	Output voltage swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
I_{SC}	Output short-circuit current		10	25	50	10	25	50	mA
R_{OUT}	Output resistance			100			100		Ω
I_{CC}	Supply current	 Over temperature		2.0 2.2	3.0 3.6		2.0 2.2	3.0	mA mA
CMRR	Common-mode rejection ratio	$R_S \leq 10k\Omega$ Over temperature	70	90		70	90		dB
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$ Over temperature		30	150		30	150	µV/V

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified.

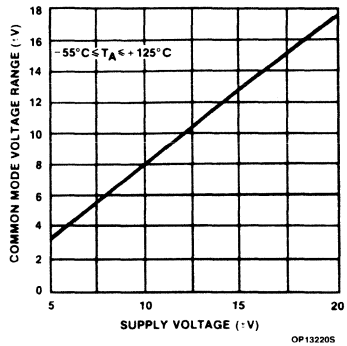
SYMBOL	PARAMETER	TEST CONDITIONS	SE530			NE530			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Transient Response								
t_R	Small-signal rise time			0.06			0.06		μs
	Small-signal overshoot			13			13		%
t_S	Settling time	To 0.1% (10V step)		0.9			0.9		μs
SR	Slew rate	$\pm 15V$ supply, $V_O = \pm 10V$, $R_L \geq 2k\Omega$							
	Unity gain inverting		25	35		20	35		V/μs
	Unity gain non-inverting		18	25		12	25		V/μs
BW	Power bandwidth	5% THD, $V_O = \pm 10V$, $R_L \geq 2k\Omega$	360	500		280	500		kHz
	Small-signal bandwidth	Open-loop		3			3		MHz
V_{NOISE}	Input noise voltage	f = 1kHz		30			30		$nV/\sqrt{Hz}$

TYPICAL PERFORMANCE CHARACTERISTICS

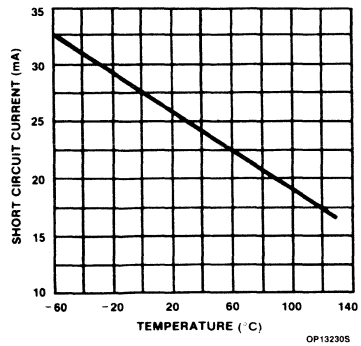
Output Voltage Swing as a Function of Supply Voltage



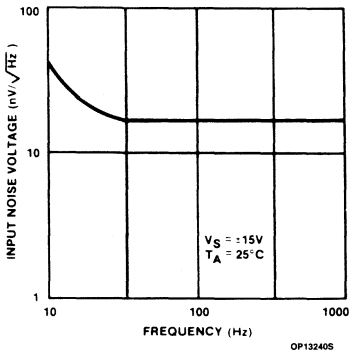
Input Common-Mode Voltage Range as a Function of Supply Voltage



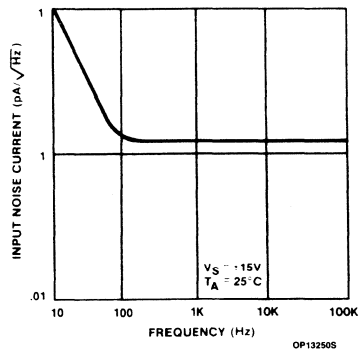
Output Short-Circuit Current as a Function of Ambient Temperature



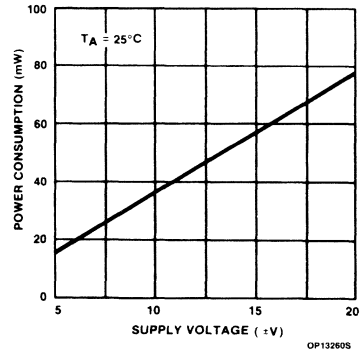
Input Noise Voltage as a Function of Frequency



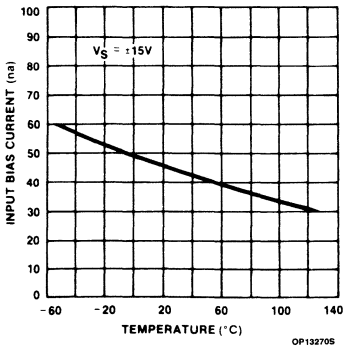
Input Noise Current as a Function of Frequency



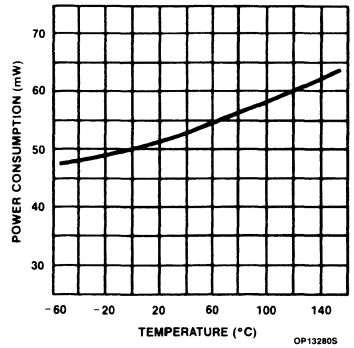
Power Consumption as a Function of Supply Voltage (Each Amplifier)



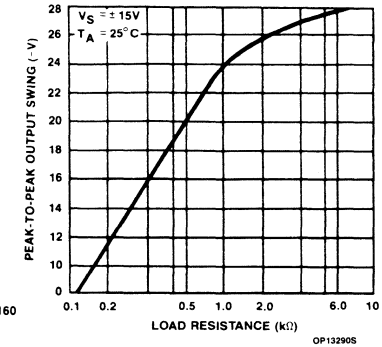
Input Bias Current as a Function of Ambient Temperature



Power Consumption as a Function of Ambient Temperature (Each Amplifier)

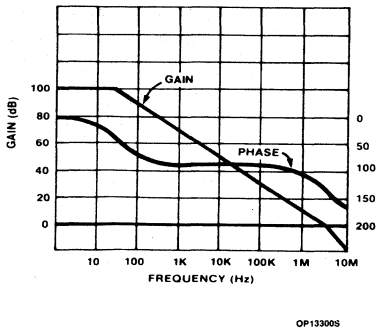


Output Voltage Swing as a Function of Load Resistance



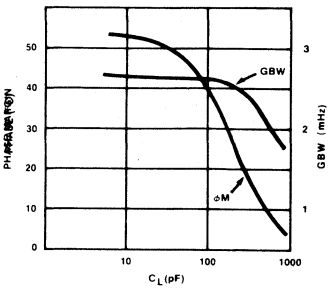
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

NE530 Open-Loop Gain and Phase vs Frequency



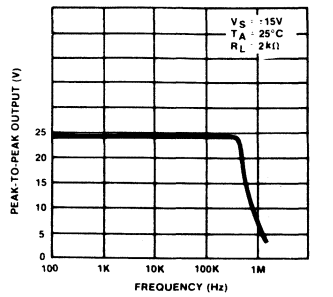
OP13300S

Gain Bandwidth Product and Phase Margin vs Load Capacity



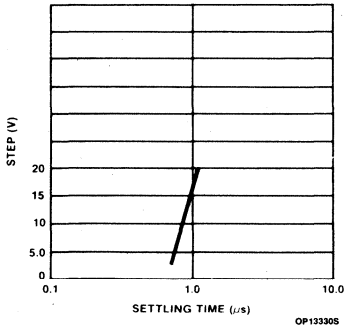
OP13310S

Power Bandwidth



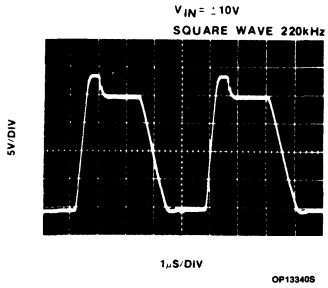
OP13320S

Input Voltage Step vs Settling Time to 10mV



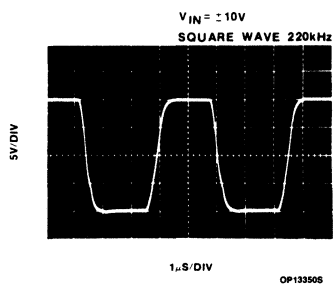
OP13330S

Slew Rate — Voltage-Follower



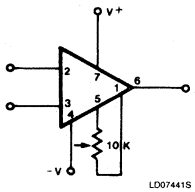
OP13340S

Slew Rate (−1 Amplifier)



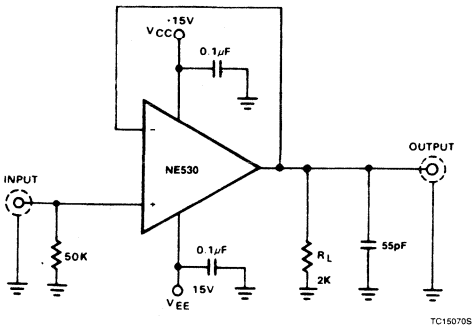
OP13350S

TYPICAL CIRCUIT CONNECTION

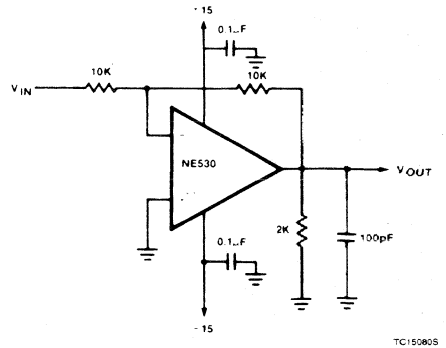


Offset Adjust Circuit

TEST LOAD CIRCUITS

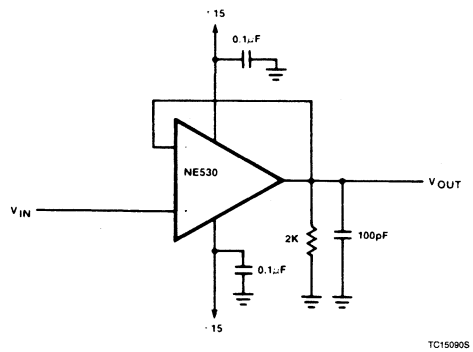


Slew Rate and Settling Time

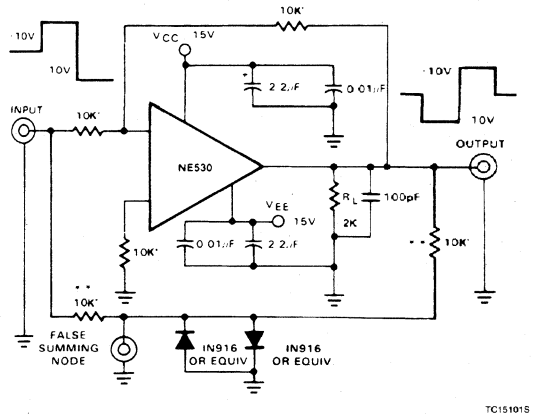


High Slew Rate — Inverting Amplifier

NOTES:
Pins not shown are not connected.
All resistor values are typical and in ohms.



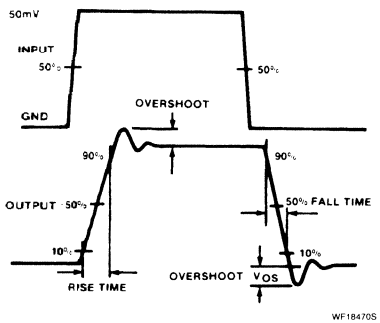
High Slew Rate — Voltage-Follower



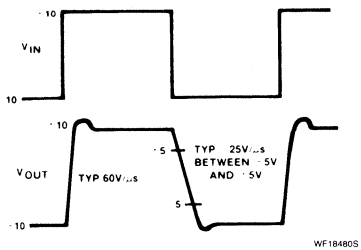
NOTES:
Pins not shown are not connected.
All resistor values are typical and in ohms.
*Match to within 0.01%.
**Open for slew rate.

Testing Slew Rate and Settling Time

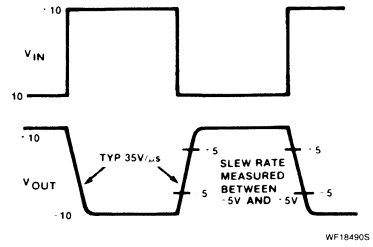
VOLTAGE WAVEFORMS



Small-Signal Transient Response Definitions



Slew Rate — Voltage-Follower



Slew Rate — Inverting Amplifier

NE/SE531
High Slew Rate Operational Amplifier

Product Specification

DESCRIPTION

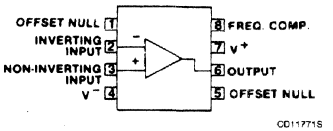
The 531 is a fast slewing high performance operational amplifier which retains DC performance equal to the best general purpose types while providing far superior large-signal AC performance. A unique input stage design allows the amplifier to have a large-signal response nearly identical to its small-signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large-signal bandwidths are required, the amplifier out-performs conventional designs which have much better small-signal response. Also, because the small-signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation, and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

FEATURES

- **35V/μs slew rate at unity gain**
- **Pin-for-pin replacement for μA709, μA748, or LM101**
- **Compensated with a single capacitor**
- **Same low drift offset null circuitry as μA741**
- **Small-signal bandwidth 1MHz**
- **Large-signal bandwidth 500kHz**
- **True op amp DC characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications**

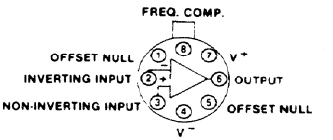
PIN CONFIGURATIONS

N, FE Packages



CD11771S

H Package[1]



CD11780S

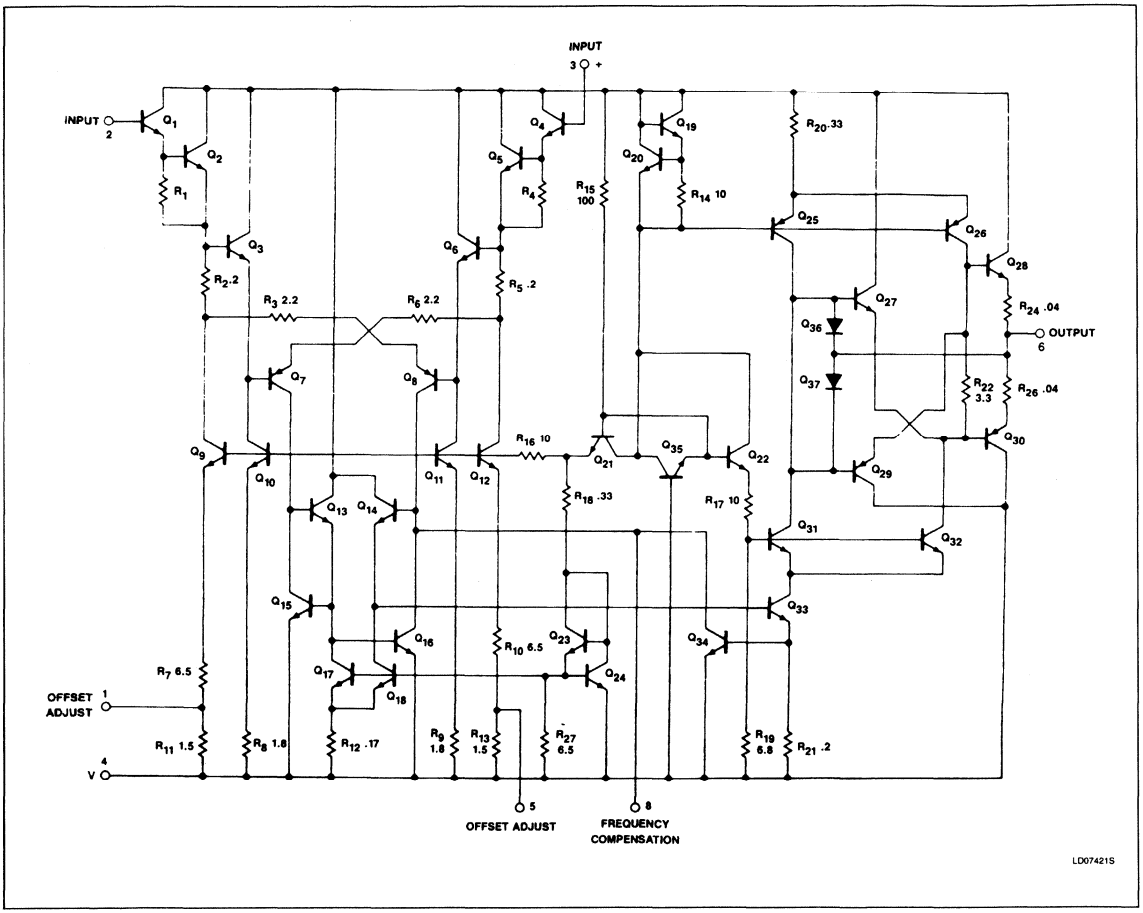
NOTE:
1. Metal cans (H) not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
$P_{D\ MAX}$	Maximum power dissipation T_A = 25°C (still-air)[1] FE package N package H package	 780 1160 830	 mW mW mW
	Differential input voltage	±15	V
V_{CM}	Common-mode input voltage[2]	±15	V
	Voltage between offset null and V–	±0.5	V
T_A	Operating ambient temperature range NE531 SE531	 0 to +70 –55 to +125	 °C °C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
	Output short-circuit duration[3]	indefinite	

NOTES:
1. The following derating factors should be applied above 25°C:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   H package at 6.7mW/°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to +125°C case temperature or to +75°C ambient temperature.

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE531N
8-Pin Ceramic DIP	0 to +70°C	NE531FE
8-Pin Metal Can	0 to +70°C	NE531H
8-Pin Ceramic DIP	−55°C to +125°C	SE531FE
8-Pin Metal Can	−55°C to +125°C	SE531H

DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, unless otherwise specified.

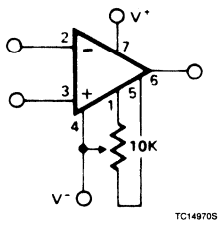
SYMBOL	PARAMETER	TEST CONDITIONS	SE531			NE531			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$, $T_A = 25°C$		2.0	5.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp			6.0			7.5	mV
ΔV_{OS}		Over temp		10			10		μV/°C
I_{OS}	Offset current	$T_A = 25°C$		30	200		50	200	nA
		T_A = High			200			200	nA
		T_A = Low			500			300	nA
ΔI_{OS}		Over temp		0.4			0.4		nA/°C
I_{BIAS}	Input bias current	T = 25°C		300	500		400	1500	nA
		T_A = High			500			1500	nA
		T_A = Low			1500			2000	nA
ΔI_{BIAS}		Over temp		2			2		nA/°C
V_{CM}	Common-mode voltage range	$T_A = 25°C$	±10			±10			V
CMRR	Common-mode rejection ratio	$T_A = 25°C$, $R_S \leq 10k\Omega$				70	100		dB
		Over temp $R_S \leq 10k\Omega$	70	90					dB
R_{IN}	Input resistance	$T_A = 25°C$		20			20		MΩ
V_{OUT}	Output voltage swing	$R_L \geq 10k\Omega$, over temp	±10	±13		±10	±13		V
I_{CC}	Supply current	$T_A = 25°C$			7.0			10	mA
		T_{MAX}			7.0			10	mA
P_D	Power consumption	$T_A = 25°C$			210			300	mW
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$, $T_A = 25°C$					10	150	μV/V
		$R_S \leq 10k\Omega$, over temp		10	150				μV/V
R_{OUT}	Output resistance	$T_A = 25°C$		75			75		Ω
A_{VOL}	Large-signal voltage gain	$T_A = 25°C$, $R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$	50	100		20	60		V/mV
		$R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$, over temp	25			15			V/mV
V_{INN}	Input noise voltage	25°C, f = 1kHz		20			20		$nV/\sqrt{Hz}$
I_{SC}	Short-circuit current	25°C	5	15	45	5	15	45	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.[1]

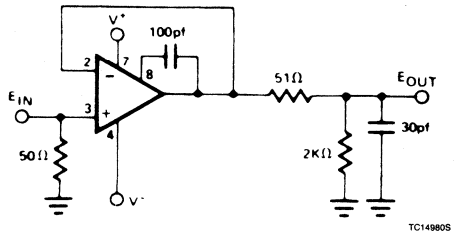
SYMBOL	PARAMETER	TEST CONDITIONS	NE531			SE531			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Full power bandwidth			500			500		kHz
t_S	Settling time (1%)	$A_V = +1$, $V_{IN} = \pm 10V$		1.5			1.5		μs
	(0.1%)			2.5			2.5		μs
	Large-signal overshoot	$A_V = +1$, $V_{IN} = \pm 10V$		2			2		%
	Small-signal overshoot	$A_V = +1$, $V_{IN} = 400mV$		5			5		%
t_R	Small-signal rise time	$A_V = +1$, $V_{IN} = 400mV$		300			300		ns
SR	Slew rate	$A_V = 100$		35			35		V/μs
		$A_V = 10$		35			35		V/μs
		$A_V = 1$ (non-inverting)		30		20	30		V/μs
		$A_V = 1$ (inverting)		35		25	35		V/μs

NOTE:
1. All AC testing is performed in the transient response test circuit.

TEST LOAD CIRCUITS



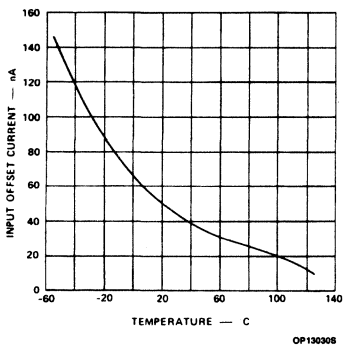
Offset Null Circuit



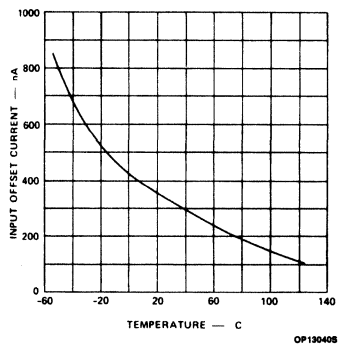
Transient Response Circuit

TYPICAL PERFORMANCE CHARACTERISTICS $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise specified.

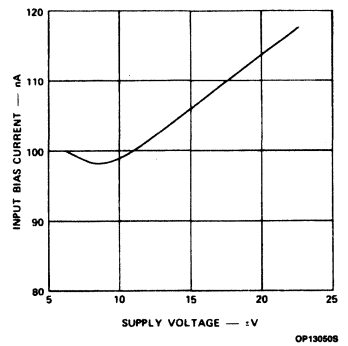
Input Offset Current as a Function of Ambient Temperature



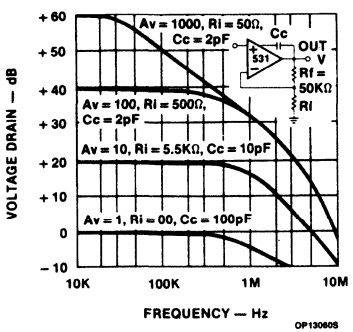
Input Bias Current as a Function of Ambient Temperature



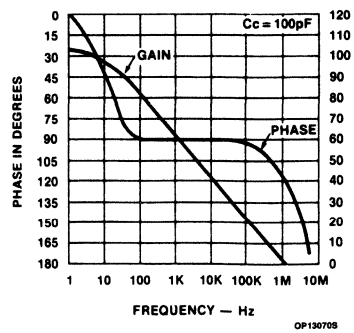
Input Bias Current as a Function of Supply Voltage



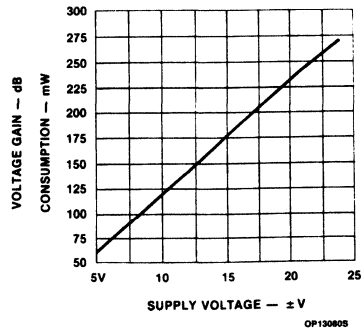
Closed-Loop Non-Inverting Voltage Gain as a Function of Frequency



Open-Loop Phase Response and Voltage Gain as a Function of Frequency

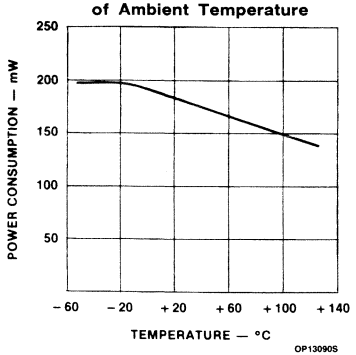


Power Consumption as a Function of Supply Voltage

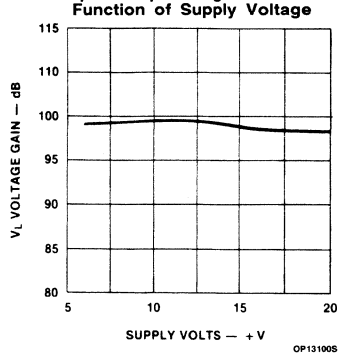


TYPICAL PERFORMANCE CHARACTERISTICS (Continued) $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise specified.

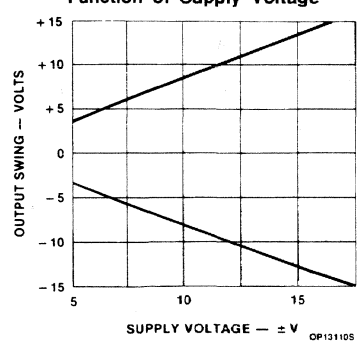
Power Consumption as a Function of Ambient Temperature



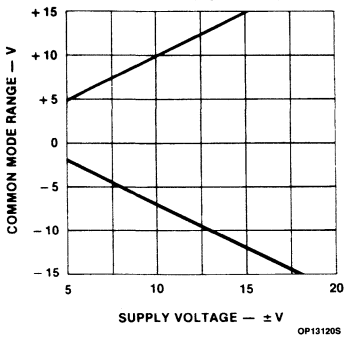
Open-Loop Voltage Gain as a Function of Supply Voltage



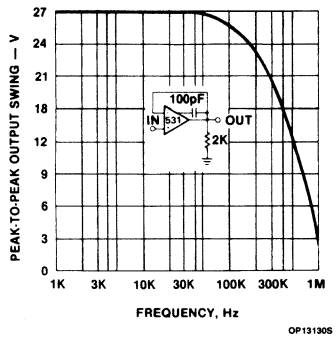
Output Voltage Swing as a Function of Supply Voltage



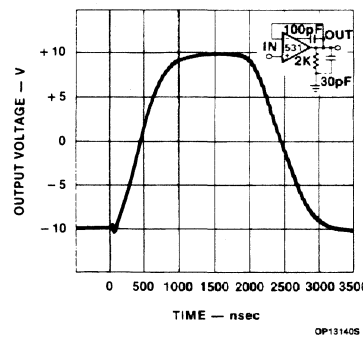
Input Voltage Range as a Function of Supply Voltage



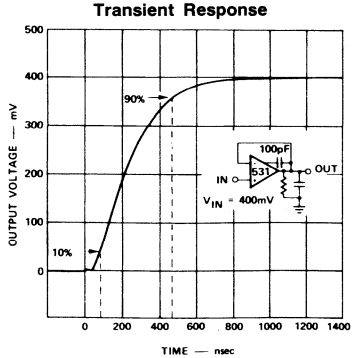
Output Voltage Swing as a Function of Frequency



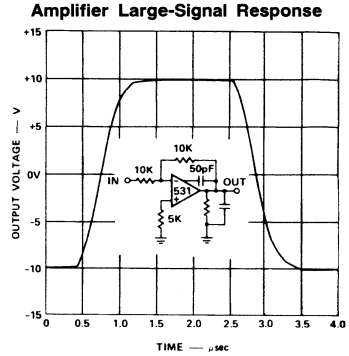
Voltage-Follower Large-Signal Response



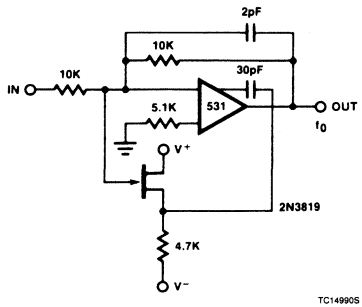
Voltage-Follower Transient Response



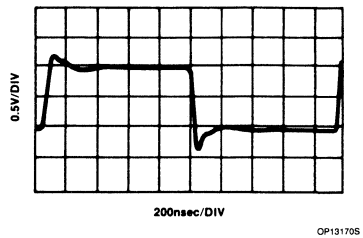
Unity Gain Inverting Amplifier Large-Signal Response



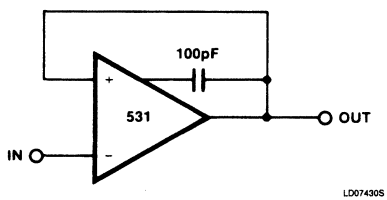
TYPICAL APPLICATIONS



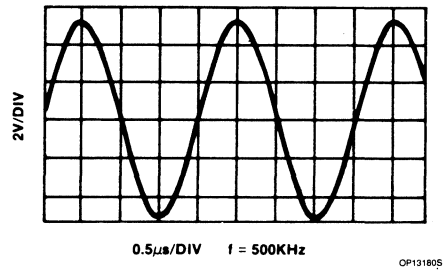
High-Speed Inverter (10MHz Bandwidth)



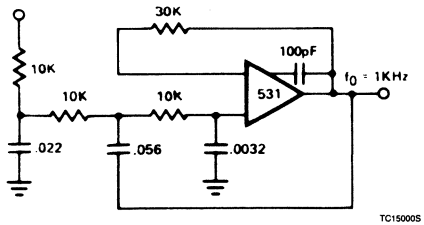
Pulse Response High-Speed Inverter



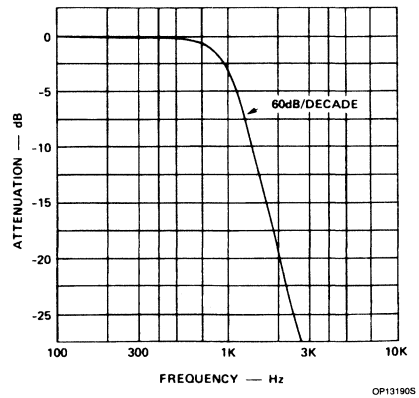
Fast Settling Voltage-Follower



Large-Signal Response Voltage-Follower



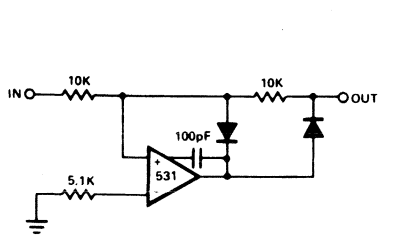
Three-Pole Active Low-Pass Filter Butterworth Maximally Flat Response[1]



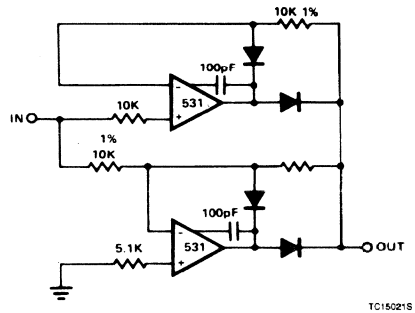
Response of 3-Pole Active Butterworth Maximally Flat Filter

NOTES:
1. Reference — EDN Dec. 15, 1970
   Simplify 3-pole active filter design
   A. Paul Brokow

TYPICAL APPLICATIONS (Continued)

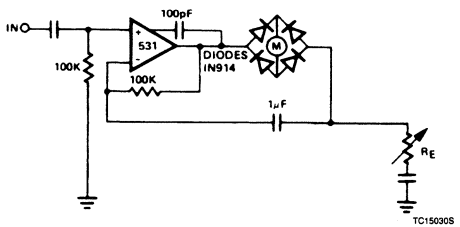


a. Half-Wave

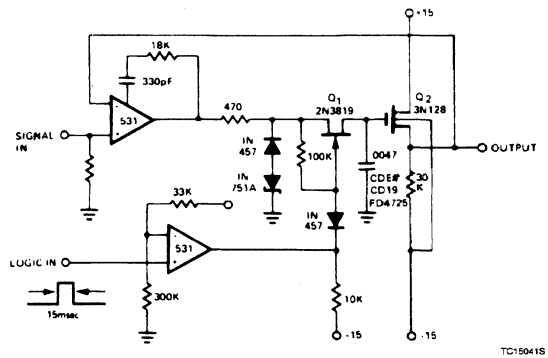


b. Full-Wave

Precision Rectifiers



AC Millivoltmeter



AC Millivoltmeter Sample-and-Hold

CYCLIC A-TO-D CONVERTER

One interesting, but much ignored, A/D converter is the cyclic converter. This consists of a chain of identical stages, each of which senses the polarity of the input. The stage then subtracts V_{REF} from the input and doubles the remainder if the polarity was correct. In Figure 1, the signal is full-wave rectified and the remainder of $V_{IN} - V_{REF}$ is doubled. A chain of these stages gives the gray code equivalent of the input voltage in digitized form related to the magnitude of V_{REF}. Possessing high potential accuracy, the circuit using NE531 devices settles in 5μs.

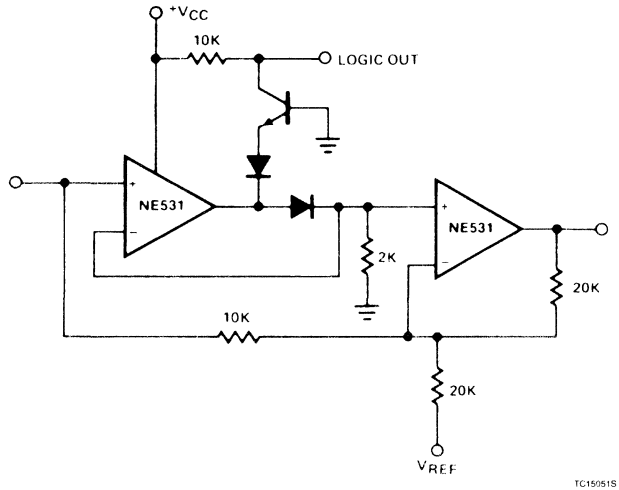
TRIANGLE AND SQUARE WAVE GENERATOR

The circuit in Figure 2 will generate precision triangle and square waves. The output amplitude of the square wave is set by the output swing of op amp A-1, and R1/R2 sets the triangle amplitude. The frequency of oscillation in either case is:

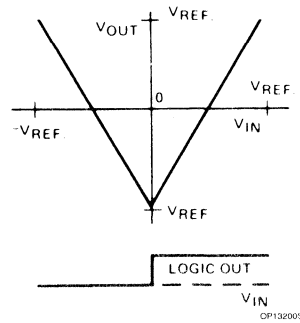
$$f = \frac{1}{4RC} \cdot \frac{R2}{R1} \quad (1)$$

The square wave will maintain 50% duty cycle even if the amplitude of the oscillation is not symmetrical.

The use of the NE531 in this circuit will allow good square waves to be generated to quite high frequencies. Since the amplifier A1 runs open-loop, there is no need for compensation. The triangle-generating amplifier must be compensated. The NE5535 device can be used as well, except for the lower frequency response.



a.



b.

Figure 1. Cyclic A-to-D Converter

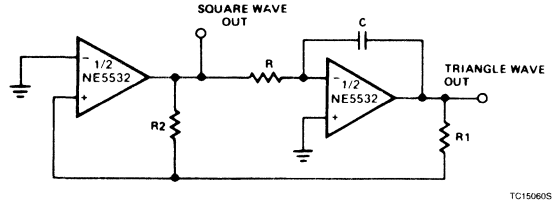


Figure 2. Triangle and Square Wave Generator

NE/SE538
High Slew Rate Op Amp

Product Specification

DESCRIPTION

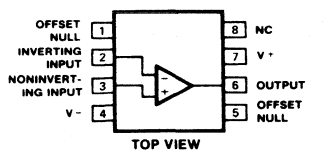
The NE/SE538 is a new generation operational amplifier featuring high slew rates combined with improved input characteristics. Internally-compensated for gains of 5 or larger, the SE538 offers guaranteed minimum slew rates of 40V/μs or larger. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 748, 101A and 741.

FEATURES

- **2mV typical input offset voltage**
- **80nA max input offset current**
- **Short-circuit protected**
- **Offset null capability**
- **Large common-mode and differential voltage ranges**
- **60V/μs typical slew rate (gain of +5, −4 min)**
- **6MHz typical gain bandwidth product (gain +5, −4 minimum)**
- **Internal frequency compensation (gain of +5, −4 minimum)**
- **Pinout: standard single op amp (748, 101A, 741, etc).**

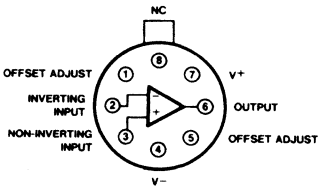
PIN CONFIGURATIONS

D, FE, N Packages



CD11720S

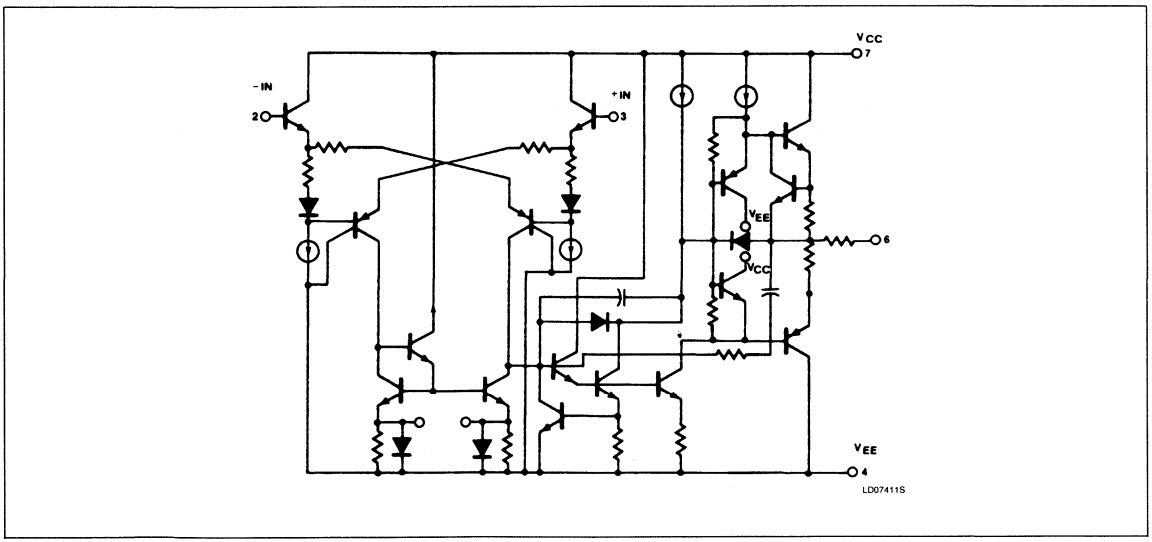
H Package[1]



CD11730S

NOTE:
1. Metal cans no longer available.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE538D
8-Pin Plastic DIP	0 to +70°C	NE538N
8-Pin Ceramic DIP	0 to +70°C	NE538FE
8-Pin Plastic DIP	−55°C to +125°C	SE538N
8-Pin Ceramic DIP	−55°C to +125°C	SE538FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage SE military grade NE commercial grade	 ±22 ±18	 V V
P_D	Maximum power dissipation, T_A=25°C (still air)[1] D package F package N package	 790 830 1200	 mW mW mW
V_{DIFF}	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
T_A	Operating ambient temperature range SE military grade NE commercial grade	 −55 to +125 0 to 70	 °C °C
	Output short-circuit[3]	indefinite	
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   D package at 6.3mW/°C
   F package at 6.7mW/°C
   N package at 9.6mW/°C
2. For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

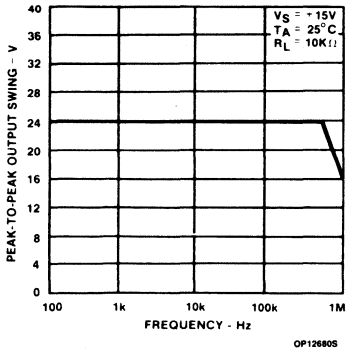
SYMBOL	PARAMETER	TEST CONDITIONS	SE538			NE538			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$ $R_S \leq 10k\Omega$, over temp.		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		4.0			6.0		µV/°C
I_{OS}	Input offset current	 Over temp.		5	20 40		15	40 80	nA nA
ΔI_{OS}	Input offset current	Over temp.		25			40		pA/°C
I_B	Input current	 Over temp.		45	80 200		65	150 200	nA nA
ΔI_B	Input current	Over temp.		50			80		pA/°C
V_{CM}	Input common-mode voltage range		±12	±13		±12	±13		V
CMRR	Common-mode rejection ratio	$R_S \leq 10k\Omega$, over temp.	70	90		70	90		dB
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	µV/V
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large-signal voltage gain	$R_L \geq 2k\Omega$, , $V_{OUT} = \pm 10V$ Over temp., $R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	50 25	200		50 25	200		V/mV V/mV
V_{OUT}	Output voltage swing	Over temp., $R_L \geq 2k\Omega$ Over temp., $R_L \geq 10k\Omega$	±10 ±12	±13 ±14		±10 ±12	±13 ±14		V V
I_{CC}	Supply current	 Over temp.		2 2.2	3 3.6		2 2.2	3 3.6	mA mA
P_D	Power dissipation	 Over temp.		60 66	90 108		60 66	90 108	mW mW
I_{SC}	Output short-circuit current		10	25	50	10	25	50	mA
R_{OUT}	Output resistance			100			100		Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified.

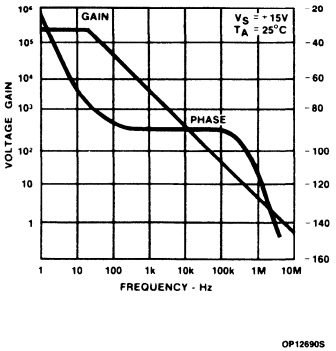
SYMBOL	PARAMETER	TEST CONDITIONS	SE538			NE538			UNIT
			Min	Typ	Max	Min	Typ	Max	
GBW	Gain bandwidth product (Gain +5, −4 minimum)			6			6		MHz
t_R	Transient response Small-signal rise time Small-signal overshoot			 0.25 6			 0.25 6		 µs %
t_S	Settling time	To 0.1%		1.2			1.2		µs
SR	Slew rate	Minimum gain = 5 Noninverting $R_L \geq 2k\Omega$	40	60			60		V/µs
V_{NOISE}	Input noise voltage	f = 1kHz, T_A = 25°C		30			30		$nV/\sqrt{Hz}$

TYPICAL PERFORMANCE CHARACTERISTICS

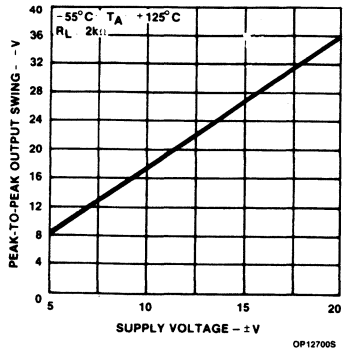
Output Voltage Swing as a Function of Frequency



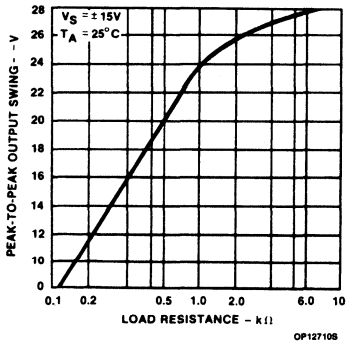
Open Loop Voltage Gain as a Function of Frequency



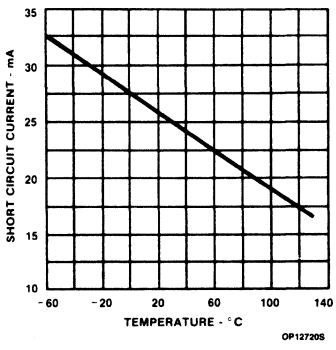
Output Voltage Swing as a Function of Supply Voltage



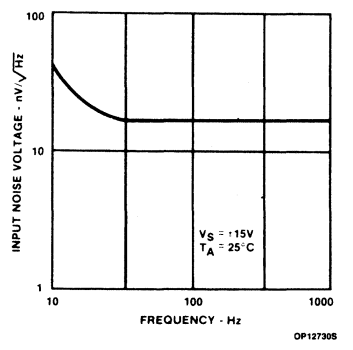
Output Voltage Swing as a Function of Load Resistance



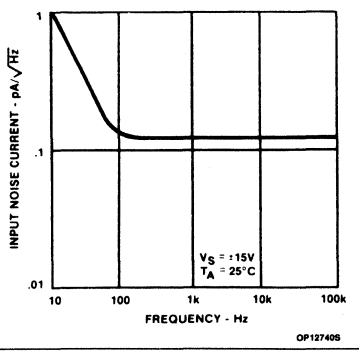
Output Short-Circuit Current as a Function of Ambient Temperature



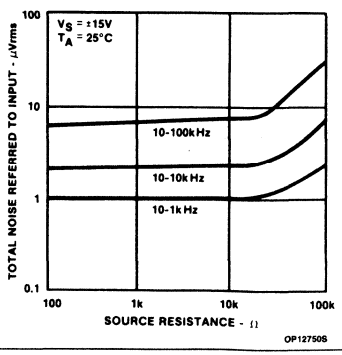
Input Noise Voltage as a Function of Frequency



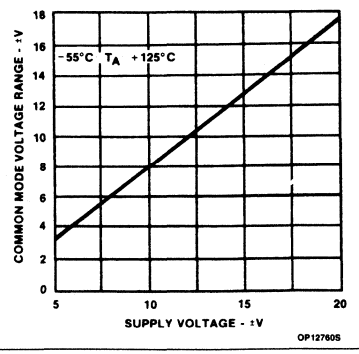
Input Noise Current as a Function of Frequency



Broadband Noise for Various Bandwidths

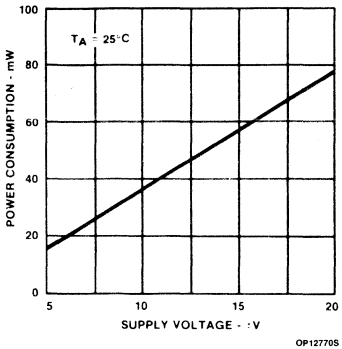


Input Common-Mode Voltage Range as a Function of Supply Voltage

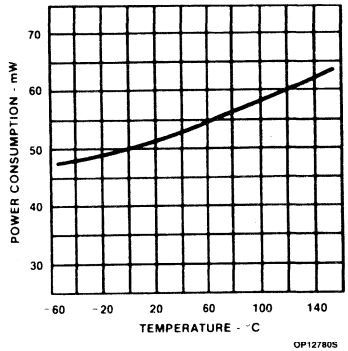


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

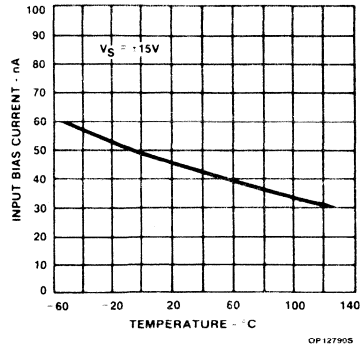
Power Consumption as a Function of Supply Voltage



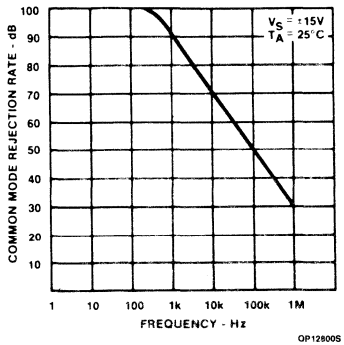
Power Consumption as a Function of Ambient Temperature



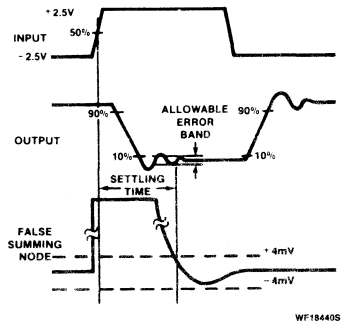
Input Bias Current as a Function of Ambient Temperature



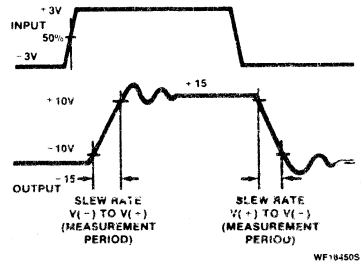
Common-Mode Rejection Ratio as a Function of Frequency



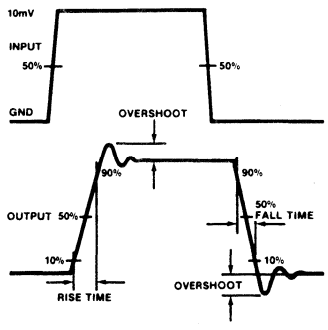
Settling Time Measurement Waveforms



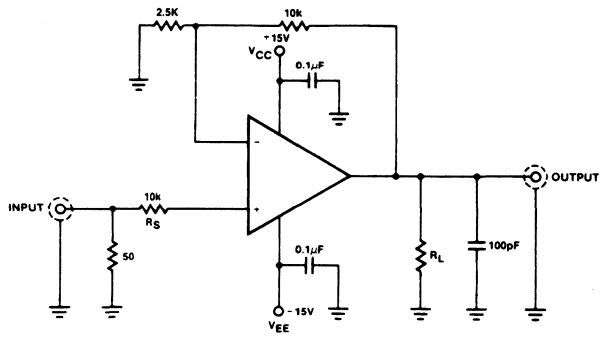
Slew Rate Measurement $V_{CC} = \pm 20V$



Small-Signal Transient Response Definitions

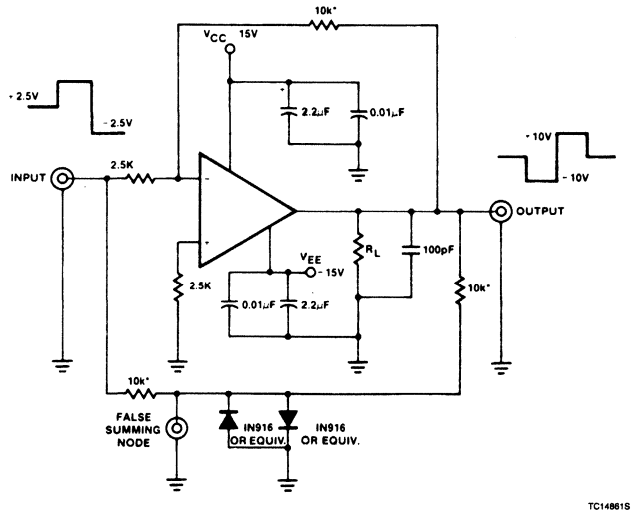


TEST LOAD CIRCUITS



NOTES:
Pins not shown are not connected.
All resistor values are typical and in ohms.

Slew Rate and Small-Signal Transient Response Test Circuit



NOTES:
*Match to within 0.01%.
Pins not shown are not connected.
All resistor values are typical and in ohms.

Settling Time Test Circuit

APPLICATIONS

The internal frequency compensation is designed for a minimum inverting gain of 4 and a minimum non-inverting gain of 5. Below these gains the NE538 will be unstable and will need external compensation (see Figures 1 and 2).

The higher slew rate of the NE538 has made this device quite appealing for high-speed designs, and the fact that it has a standard pinout will allow it to be used to upgrade existing systems that now use the μA741 or μ748.

Equations:

$$f_{LAG} = \frac{1\ (6MHz)}{10} = \frac{1}{2\pi R_L C_L}$$

$$f_{LEAD} = 6MHz = \frac{1}{2\pi R_F C_F}$$

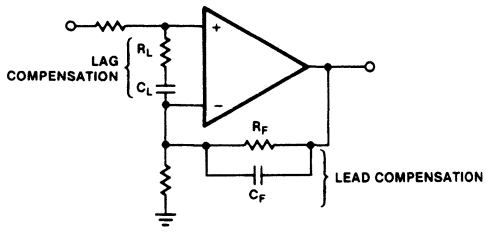


Figure 1. Non-Inverting Configuration

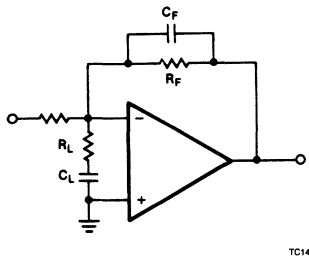


Figure 2. Inverting Configuration

VOLTAGE COMPARATOR

Inexpensive voltage comparators with only modest parameters are often needed. The op amp is often used in the configuration because the high gain provides good selectivity. Figure 6 shows a circuit usable with most any op amp. The zener is selected for the output voltage required (5.1 volt for TTL), and the resistor provides some current protection to the op amp output structure. V_{REF} can be any voltage within the wide common-mode range of the amplifier — another advantage of using op amps for comparators.

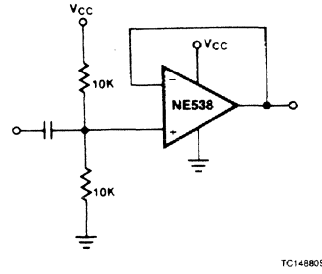


Figure 3. Voltage-Follower With Single Power Source

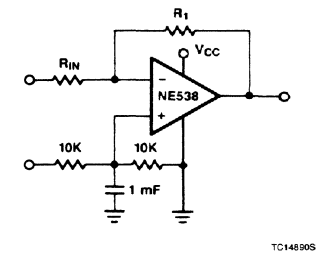


Figure 4. Inverting Amp With Single Power Supply

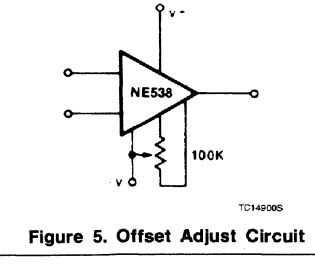
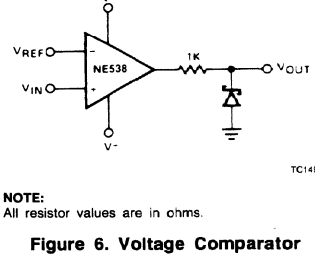


Figure 5. Offset Adjust Circuit



NOTE:
All resistor values are in ohms.

Figure 6. Voltage Comparator

NE/SA/SE4558
Dual General-Purpose Operational Amplifier

Product Specification

DESCRIPTION

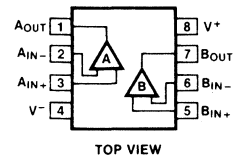
The 4558 is a dual operational amplifier that is internally compensated. Excellent channel separation allows the use of a dual device in a single amp application, providing the highest packaging density. The NE/SA/SE4558 is a pin-for-pin replacement for the RC/RM/RV4558.

FEATURES

- **2MHz unity gain bandwidth guaranteed**
- **Supply voltage ±22V for SE4558 and ±18V for NE4558**
- **Short-circuit protection**
- **No frequency compensation required**
- **No latch-up**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**

PIN CONFIGURATIONS

D, FE, N Packages



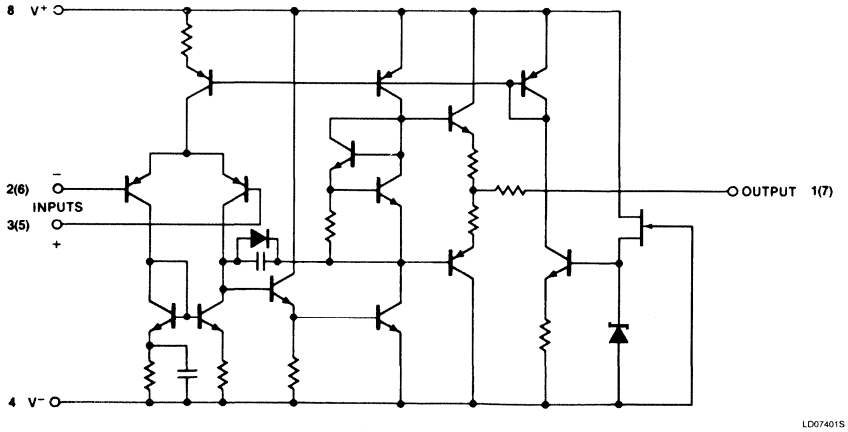
TOP VIEW

CD11700S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE4558D
8-Pin Ceramic DIP	0 to +70°C	NE4558FE
8-Pin Plastic DIP	0 to +70°C	NE4558N
8-Pin Plastic DIP	-40°C to +85°C	SA4558N
8-Pin Ceramic DIP	-40°C to +85°C	SA4558FE
8-Pin Plastic DIP	-55°C to +125°C	SE4558N
8-Pin Ceramic DIP	-55°C to +125°C	SE4558FE

EQUIVALENT SCHEMATIC



LD07401S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage SE4558 NE4558, SA4558	 ±22 ±18	 V V
$P_{D\ MAX}$	Maximum power dissipation, T_A = 25°C (Still air)[1] FE package N package D package	 780 1160 780	 mW mW mW
	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range SE4558 SA4558 NE4558	 −55 to +125 −40 to +85 0 to +70	 °C °C °C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
	Output short-circuit duration[3]	Indefinite	

NOTES:

1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground on one amp only. Rating applies to +125°C case temperature or +75°C ambient temperature for NE4558 and to +85°C ambient temperature for SA4558.

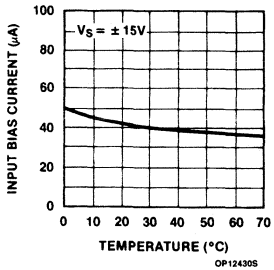
DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE4558			SA/NE4558			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
	$\Delta V_{OS}/\Delta T$	Over temp.		4			4		$\mu V/°C$
I_{OS}	Input offset current			50	200		30	200	nA
	$\Delta I_{OS}/\Delta T$	Over temp.		20			20		pA/°C
I_{BIAS}	Input bias current			40	500		200	500	nA
	$\Delta I_B/\Delta T$	Over temp.		40			40		pA/°C
R_{IN}	Input resistance		0.3	1.0		0.3	1.0		MΩ
A_V	Large-signal voltage gain	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	50,000	300,000		20,000	300,000		V/V
	Output voltage swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
V_{IN}	Input voltage range		±12	±13		±12	±13		V
CMRR	Common-mode rejection ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$		10	150		10	150	$\mu V/V$
I_{SC}	Short-circuit current		5	25	60	5	25	60	mA
	Power consumption (all amplifiers)	$R_L = \infty$		120	170		120	170	mW
	Transient response (unity gain)	$V_{IN} = 20mV$ $R_L = 2k\Omega$ $C_L \leq 100pF$							
t_R	Rise time Overshoot			100 15.0			100 15.0		ns %
SR	Slew rate (unity gain)	$R_L \geq 2k\Omega$		1.0			1.0		$V/\mu s$
	Channel separation (gain = 100)	f = 10kHz $R_S = 1k\Omega$		90			90		dB
GBW	Unity gain bandwidth (gain = 1)		2.0	3.0		2.0	3.0		MHz
θ_M	Phase margin			45			45		Degree
V_{NOISE}	Input noise voltage	f = 1kΩ		25			25		$nV/\sqrt{Hz}$
NOTE: The following specifications apply over operating temperature range.									
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
I_{OS}	Input offset current				500			300/500[1]	nA
I_{BIAS}	Input bias current				1500			800/1500[1]	nA
A_V	Large-signal voltage gain	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	25,000			15,000			V/V
	Output voltage swing	$R_L \geq 2k\Omega$	±10			±10			V
P_C	Power consumption	T_A = HIGH T_A = LOW		105 125	150 200		115 120	150 200	mW mW

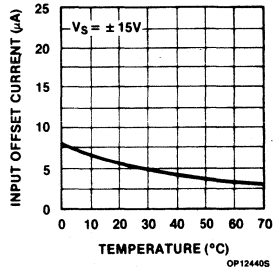
NOTE:
1. SA4558 only.

TYPICAL PERFORMANCE CURVES

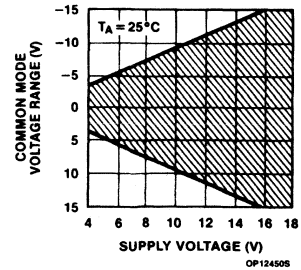
Input Bias Current as a Function of Ambient Temperature



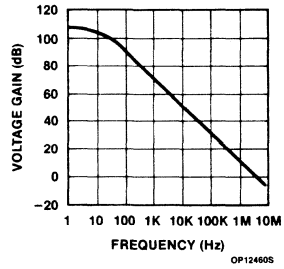
Input Offset Current as a Function of Ambient Temperature



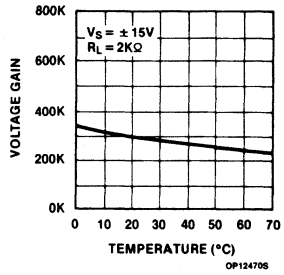
Common-Mode Range as a Function of Supply Voltage



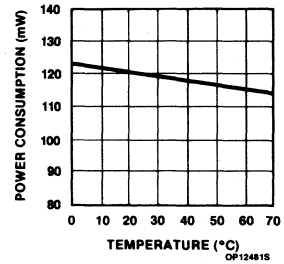
Open-Loop Voltage Gain as a Function of Frequency



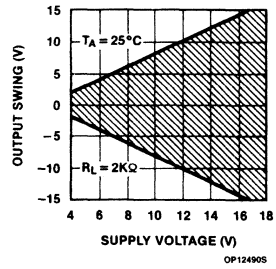
Open-Loop Gain as a Function of Temperature



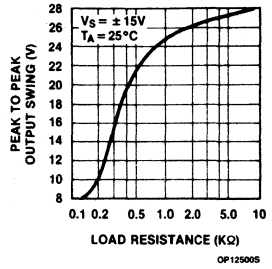
Power Consumption as a Function of Ambient Temperature



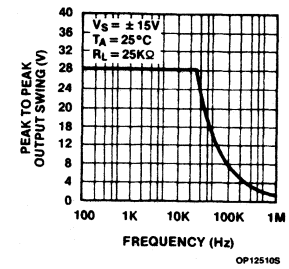
Typical Output Voltage as a Function of Supply Voltage



Output Voltage Swing as a Function of Load Resistance

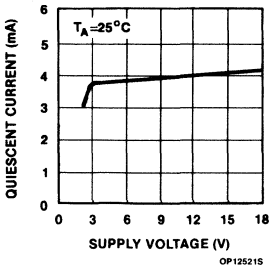


Output Voltage Swing as a Function of Frequency

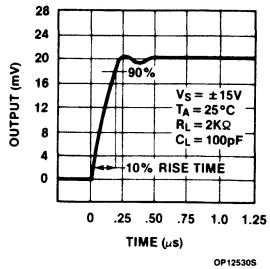


TYPICAL PERFORMANCE CURVES (Continued)

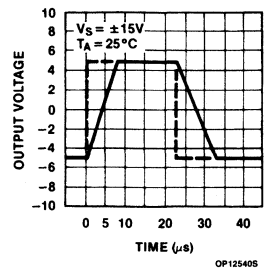
Quiescent Current as a Function of Supply Voltage



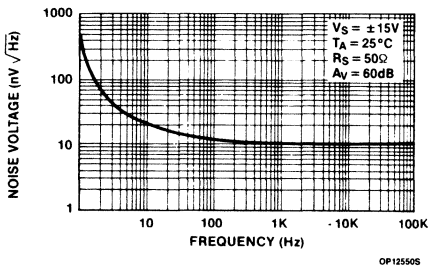
Transient Response



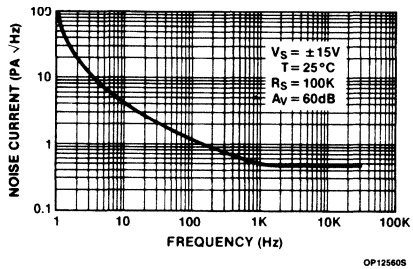
Voltage-Follower Large-Signal Pulse Response



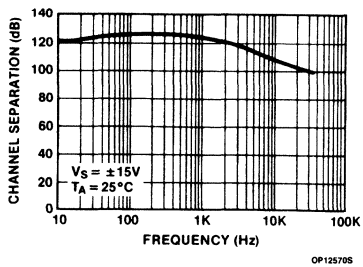
Input Noise Voltage as a Function of Frequency



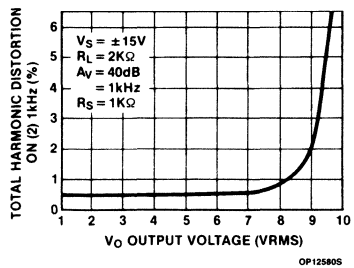
Input Noise Current as a Function of Frequency



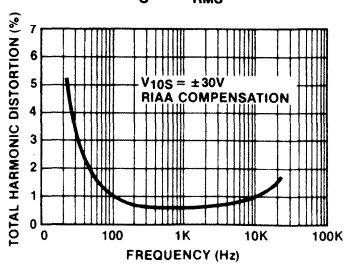
Channel Separation



Total Harmonic Distortion vs Output Voltage



Distortion vs Frequency $V_O = 1V_{RMS}$



NE/SA5230
Low Voltage Operational Amplifier

Product Specification

DESCRIPTION

The NE5230 is a very low voltage operational amplifier that can perform with a voltage supply as low as 1.8V or as high as 15V. In addition, split or single supplies can be used, and the output will swing to ground when applying the latter. There is a bias adjusting pin which controls the supply current required by the device and thereby controls its power consumption. If the part is operated at ±0.9V supply voltages, the current required is only 110μA when the current control pin is left open. Even with this low power consumption, the device obtains a typical unity gain bandwidth of 180kHz. When the bias adjusting pin is connected to the negative supply, the unity gain bandwidth is typically 600kHz while the supply current is increased to 600μA. In this mode, the part will supply full power output beyond the audio range.

The NE5230 also has a unique input stage that allows the common-mode input range to go above the positive and below the negative supply voltages by 250mV. This provides for the largest possible input voltages for low voltage applications. The part is also internally-compensated to reduce external component count.

The NE5230 has a low input bias current of typically ±40nA, and a large open-loop gain of 125dB. These two specifications are beneficial when using the device in transducer applications. The large open-loop gain gives very accurate signal processing because of the large "excess" loop gain in a closed-loop system.

The output stage is a class AB type that can swing to within 100mV of the supply voltages for the largest dynamic range that is needed in many applications. The NE5230 is ideal for portable audio equipment and remote transducers because of its low power consumption, unity gain bandwidth, and 30nV/$\sqrt{Hz}$ noise specification.

FEATURES

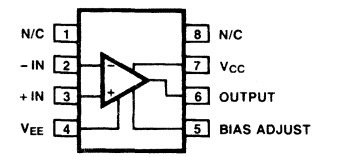
- **Works down to 1.8V supply voltages**
- **Adjustable supply current**
- **Low noise**
- **Common-mode includes both rails**
- **V_{OUT} within 100mV of both rails**

APPLICATIONS

- **Portable precision instruments**
- **Remote transducer amplifier**
- **Portable audio equipment**
- **Rail-to-rail comparators**
- **Half-wave rectification without diodes**
- **Remote temperature transducer with 4 to 20mA output transmission**

PIN CONFIGURATION

N, FE and D Packages



TOP VIEW

CD11071S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5230D
8-Pin Ceramic DIP	0 to +70°C	NE5230FE
8-Pin Plastic DIP	0 to +70°C	NE5230N
8-Pin Plastic SO	−40°C to +85°C	SA5230D
8-Pin Ceramic DIP	−40°C to +85°C	SA5230FE
8-Pin Plastic DIP	−40°C to +85°C	SA5230N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Single supply voltage	18	V
V_S	Dual supply voltage	±9	V
V_{IN}	Input voltage[1]	±9 (18)	V
	Differential input voltage[1]	$\pm V_S$	V
V_{CM}	Common-mode voltage (positive)	V_{CC} + 0.5	V
V_{CM}	Common-mode voltage (negative)	V_{EE} − 0.5	V
P_D	Power dissipation[2]	500	mW
T_J	Operating junction temperature[2]	150	°C
	Output short-circuit duration to either power supply pin[2, 3]	Indefinite	s
T_{STG}	Storage temperature	−65 to 150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Can exceed the supply voltages when $V_S \leqslant \pm 7.5V$ (15V).
2. The maximum operating junction temperature is 150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions.
   Derate above 25°C at the following rates:
   FE package at 6.7mW/°C
   N package at 9.5mW/°C
   D package at 6.25mW/°C
3. Momentary shorts to either supply are permitted in accordance to transient thermal impedance limitations determined by the package and device mounting conditions.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNIT
Single supply voltage	1.8 to 15	V
Dual supply voltage	±0.9 to ±7.5	V
Common-mode voltage (positive)	V_{CC} + 0.25	V
Common-mode voltage (negative)	V_{EE} − 0.25	V
Temperature		
NE grade	0 to 70	°C
SA grade	−40 to 85	°C

DC AND AC ELECTRICAL CHARACTERISTICS Unless otherwise specified, $\pm 0.9V \leq V_S \leq \pm 7.5V$ or equivalent single supply, $R_L = 10k\Omega$, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER		TEST CONDITIONS		BIAS	NE/SA5230			UNIT
						Min	Typ	Max	
V_{OS}	Offset voltage		$T_A = 25°C$		Any		0.4	3	mV
					Any		3	4	mV
V_{OS}	Drift				Any		2	5	µV/°C
I_{OS}	Offset current		$T_A = 25°C$		High		3	50	nA
			$T_A = 25°C$		Low		3	30	nA
					High			100	nA
					Low			60	nA
I_{OS}	Drift				High		0.5	1.4	nA/°C
					Low		0.3	1.4	nA/°C
I_B	Bias current		$T_A = 25°C$		High		40	150	nA
			$T_A = 25°C$		Low		20	60	nA
					High			200	nA
					Low			150	nA
I_B	Drift				High		2	4	nA/°C
					Low		2	4	nA/°C
I_S	Supply current		$V_S = \pm 0.9V$	$T_A = 25°C$	Low		110	160	µA
				$T_A = 25°C$	High		600	750	µA
					Low			250	µA
					High			800	µA
			$V_S = \pm 7.5V$	$T_A = 25°C$	Low		320	550	µA
				$T_A = 25°C$	High		1.1	1.6	mA
					Low			600	µA
					High			1.7	mA
V_{CM}	Common-mode input range		$V_{OS} \leq 6mV$, $T_A = 25°C$		Any	$V^- - 0.25$		$V^+ + 0.25$	V
					Any	V^-		V^+	V
CMRR	Common-mode rejection ratio		$V_S = \pm 7.5V$	$R_S = 10k\Omega$, $V_{CM} = \pm 7.5V$, $T_A = 25°C$	Any	85	95		dB
				$R_S = 10k\Omega$, $V_{CM} = \pm 7.5V$	Any	80			dB
PSRR	Power supply rejection ratio		$T_A = 25°C$		High	90	105		dB
			$T_A = 25°C$		Low	85	95		dB
					High	75			dB
					Low	80			dB
I_L	Load current	source	$V_S = \pm 7.5V$		Any	4	10		mA
		sink	$V_S = \pm 7.5V$		Any	5	15		mA
		source	$V_S = \pm 0.9V$		Any	1	5		mA
		sink	$V_S = \pm 0.9V$		Any	2	6		mA
		source	$V_S = \pm 0.9V$, $T_A = 25°C$		High	4	6		mA
		sink	$V_S = \pm 0.9V$, $T_A = 25°C$		High	5	7		mA
		source	$V_S = \pm 7.5V$, $T_A = 25°C$		High		16		mA
		sink	$V_S = \pm 7.5V$, $T_A = 25°C$		High		32		mA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) Unless otherwise specified, $\pm 0.9V \leq V_S \leq \pm 7.5V$ or equivalent single supply, $R_L = 10k\Omega$, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS		BIAS	NE/SA5230			UNIT
					Min	Typ	Max	
A_{VOL}	Large-signal open-loop gain	$V_S = \pm 7.5V$	$R_L = 10k\Omega$, $T_A = 25°C$	High	120	2000		V/mV
			$R_L = 10k\Omega$, $T_A = 25°C$	Low	60	750		V/mV
				High	100			V/mV
				Low	50			V/mV
V_{OUT}	Output voltage swing	$V_S = \pm 0.9V$	$T_A = 25°C$, +SW	Any	750	800		mV
			$T_A = 25°C$, -SW	Any	750	800		mV
			+SW	Any	700			mV
			-SW	Any	700			mV
		$V_S = \pm 7.5V$	$T_A = 25°C$, +SW	Any	7.30	7.35		V
			$T_A = 25°C$, -SW	Any	-7.32	-7.35		V
			+SW	Any	7.25	7.30		V
			-SW	Any	-7.30	-7.35		V
SR	Slew rate	$T_A = 25°C$		High		0.25		V/μs
		$T_A = 25°C$		Low		0.09		V/μs
BW	Inverting unity gain bandwidth	$C_L = 100pF$, $T_A = 25°C$		High		0.6		MHz
		$C_L = 100pF$, $T_A = 25°C$		Low		0.25		MHz
θ_M	Phase margin	$C_L = 100pF$, $T_A = 25°C$		Any		70		Deg.
t_S	Settling time	$C_L = 100pF$, 0.1%		High		2		μs
		$C_L = 100pF$, 0.1%		Low		5		μs
V_{INN}	Input noise	$R_S = 0\Omega$, f = 1kHz		High		30		nV/$\sqrt{Hz}$
		$R_S = 0\Omega$, f = 1kHz		Low		60		nV/$\sqrt{Hz}$
THD	Total Harmonic Distortion	$V_S = \pm 7.5V$ $A_V = 1$, $V_{IN} = 500mV$, f = 1kHz		High		0.003		%
		$V_S = \pm 0.9V$ $A_V = 1$, $V_{IN} = 500mV$, f = 1kHz		High		0.002		%

THEORY OF OPERATION

Input Stage

Operational amplifiers which are able to function at minimum supply voltages should have input and output stage swings capable of reaching both supply voltages within a few millivolts in order to achieve ease of quiescent biasing and to have maximum input/output signal handling capability. The input stage of the NE5230 has a common-mode voltage range that not only includes the entire supply voltage range, but also allows either supply to be exceeded by 250mV without increasing the input offset voltage by more than 6mV. This is unequalled by any other operational amplifier today.

In order to accomplish the feat of rail-to-rail input common-mode range, two emitter-coupled differential pairs are placed in parallel so that the common-mode voltage of one can reach the positive supply rail and the other can reach the negative supply rail. The simplified schematic of Figure 1 shows how the complementary emitter-coupler transistors are configured to form the basic input stage cell. Common-mode input signal voltages in the range from 0.8V above V_{EE} to V_{CC} are handled completely by the NPN pair, Q3 and Q4, while common-mode input signal voltages in the range of V_{EE} to 0.8V above V_{EE} are processed only by the PNP pair, Q1 and Q2. The intermediate range of input voltages requires that both the NPN and PNP pairs are operating. The collector currents of the input transistors are summed by the current combiner circuit composed of transistors Q8 through Q11 into one output current. Transistor Q8 is connected as a diode to ensure that the outputs of Q2 and Q4 are properly subtracted from those of Q1 and Q3.

The input stage was designed to overcome two important problems for rail-to-rail capability. As the common-mode voltage moves from the range where only the NPN pair was operating to where both of the input pairs were operating, the effective transconductance would change by a factor of two. Frequency compensation for the ranges where one input pair was operating would, of course, not be optimal for the range where both pairs were operating. Secondly, fast changes in the common-mode voltage would abruptly saturate and restore the emitter current sources, causing transient distortion. These problems were overcome by assuring that only the input transistor pair which is able to function properly is active. The NPN pair is normally activated by the current source I_{B1} through Q5 and the current mirror Q6 and Q7, assuming the PNP pair is non-conducting. When the common-mode input voltage passes below the reference voltage, V_{B1} = 0.8V at the base of Q5, the emitter current is gradually steered toward the PNP pair, away from the NPN pair. The transfer of the emitter currents between the complementary input pairs occurs in a voltage range of about 120mV around the reference voltage V_{B1}. In this way the sum of the emitter currents for each of the NPN and PNP transistor pairs is kept constant; this ensures that the transconductance of the parallel combination will be constant, since the transconductance of bipolar transistors is proportional to their emitter currents.

An essential requirement of this kind of input stage is to minimize the changes in input offset voltage between that of the NPN and PNP transistor pair which occurs when the input common-mode voltage crosses the internal reference voltage, V_{B1}. Careful circuit layout with a cross-coupled quad for each input pair has yielded a typical input offset voltage of less than 0.3mV and a change in the input offset voltage of less than 0.1mV.

Output Stage

Processing output voltage swings that nominally reach to less than 100mV of either supply voltage can only be achieved by a pair of complementary common-emitter connected transistors. Normally, such a configuration causes complex feed-forward signal paths that develop by combining biasing and driving which can be found in previous low supply voltage designs. The unique output stage of the NE5230 separates the functions of driving and biasing, as shown in the simplified schematic of Figure 2, and has the advantage of a shorter signal path which leads to increasing the effective bandwidth.

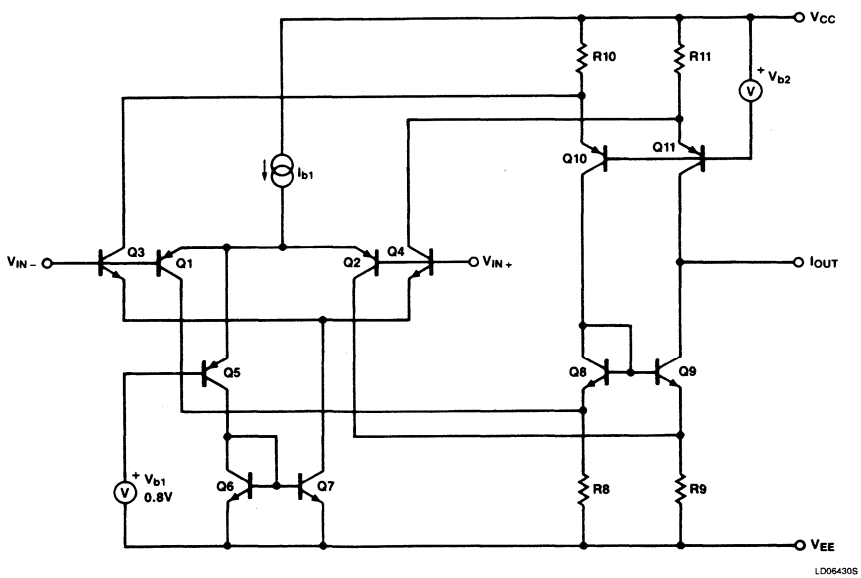


Figure 1. Input Stage

This output stage consists of two parts: the Darlington output transistors and the class AB control regulator. The output transistor Q3 connected with the Darlington transistors Q4 and Q5 can source up to 10mA to an output load. The output of NPN Darlington connected transistors Q1 and Q2 together are able to sink an output current of 10mA. Accurate and efficient class AB control is necessary to insure that none of the output transistors are ever completely cut off. This is accomplished by the differential amplifier (formed by Q8 and Q9) which controls the biasing of the output transistors. The differential amplifier compares the summed voltages across two diodes, D1 and D2, at the base of Q8 with the summed voltages across the base-emitter diodes of the output transistors Q1 and Q3. The base-emitter voltage of Q3 is converted into a current by Q6 and R6 and reconverted into a voltage across the base-emitter diode of Q7 and R7. The summed voltage across the base-emitter diodes of the output transistors Q3 and Q1 is proportional to the logarithm of the product of the push and pull currents I_{OP} and I_{ON}, respectively. The combined voltages across diodes D1 and D2 are proportional to the logarithm of the square of the reference current I_{B1}. When the diode characteristics and temperatures of the pairs Q1, D1 and Q3, Q2 are equal, the relation $I_{OP} \times I_{ON} = I_{B1} \times I_{B1}$ is satisfied.

Separating the functions of biasing and driving prevents the driving signals from becoming delayed by the biasing circuit. The output Darlington transistors are directly accessible for in-phase driving signals on the bases of Q5 and Q2. This is very important for simple high-frequency compensation. The output transistors can be high-frequency compensated by Miller capacitors CM1A and CM1B connected from the collectors to the bases of the output Darlington transistors.

A general-purpose op amp of this type must have enough open-loop gain for applications when the output is driving a low resistance load. The NE5230 accomplishes this by inserting an intermediate common-emitter stage between the input and output stages. The three stages provide a very large gain, but the op amp now has three natural dominant poles — one at the output of each common-emitter stage. Frequency compensation is implemented with a simple scheme of nested, pole-splitting Miller integrators. The Miller capacitors CM1A and CM1B are the first part of the nested structure, and provide compensation for the output and intermediate stages. A second pair of Miller integrators provide pole-splitting compensation for the pole from the input stage and the pole resulting from the compensated combination of poles from the intermediate and output stages. The result is a stable, internally-compensated op amp with a phase margin of 70 degrees.

THERMAL CONSIDERATIONS

When using the NE5230, the internal power dissipation capabilities of each package should be considered. Signetics does not recommend operation at die temperatures above 110°C in the SO package because of its inherently smaller package mass. Die temperatures of 150°C can be tolerated in all the other packages. With this in mind, the following equation can be used to estimate the die temperature:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

Where $T_A \equiv$ Ambient Temperature
T_J = Die Temperature
$P_D \equiv$ Power Dissipation
$= (I_{CC} \times V_{CC})$
$\theta_{JA} \equiv$ Package thermal resistance
$= 270°C/W$ for SO-8 in PC board mounting

See the packaging section for information regarding other methods of mounting.

$\theta_{JA} = 100°C/W$ for the plastic DIP;
$\theta_{JA} = 110°C/W$ for the ceramic DIP.

The maximum supply voltage for the part is 15V and the typical supply current is 1.1mA (1.6mA max). For operation at supply voltages other than the maximum, see the data

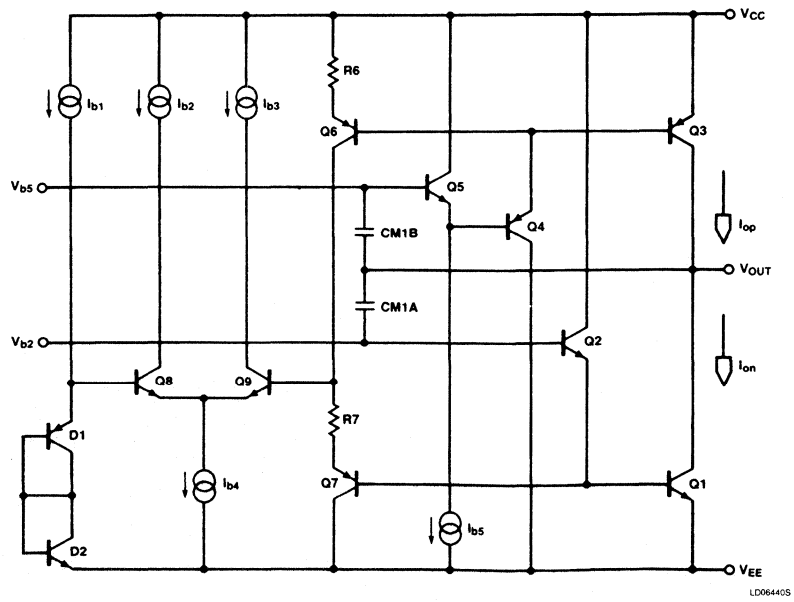


Figure 2. Output Stage

sheet for I_{CC} versus V_{CC} curves. The supply current is somewhat proportional to temperature and varies no more than 100μA between 25°C and either temperature extreme.

Operation at higher junction temperatures than that recommended is possible but will result in lower MTBF (Mean Time Between Failures). This should be considered before operating beyond recommended die temperature because of the overall reliability degradation.

DESIGN TECHNIQUES AND APPLICATIONS

The NE5230 is a very user-friendly amplifier for an engineer to design into any type of system. The supply current adjust pin (Pin 5) can be left open or tied through a pot or fixed resistor to the most negative supply (i.e., ground for single supply or to the negative supply for split supplies). The minimum supply current is achieved by leaving this pin open. In this state it will also decrease the bandwidth and slew rate. When tied directly to the most negative supply, the device has full bandwidth, slew rate and I_{CC}. The programming of the current-control pin depends on the trade-offs which can be made in the designer's application. The graph in Figure 3 will help by showing bandwidth versus I_{CC}. As can be seen, the supply current can be varied anywhere over the range of 100μA to 600μA for a supply voltage of 1.8V. An external resistor can be inserted between the current control pin and the most negative supply. The resistor can be selected between 1Ω to 100kΩ to provide any required supply current over the indicated range. In addition, a small varying voltage on the bias current control pin could be used for such exotic things as changing the gain-bandwidth for voltage controlled low pass filters or amplitude modulation. Furthermore, control over the slew rate and the rise time of the amplifier can be obtained in the same manner. This control over the slew rate also changes the settling time and overshoot in pulse response applications. The settling time to 0.1% changes from 5μs at low bias to 2μs at high bias. The supply current control can also be utilized for wave-shaping applications such as for pulse or triangular waveforms. The gain-bandwidth can be varied from between 250kHz at low bias to 600kHz at high bias current. The slew rate range is 0.08V/μs at low bias and 0.25V/μs at high bias.

The full output power bandwidth range for V_{CC} equals 2V, is above 40kHz for the maximum bias current setting and greater than 10kHz at the minimum bias current setting.

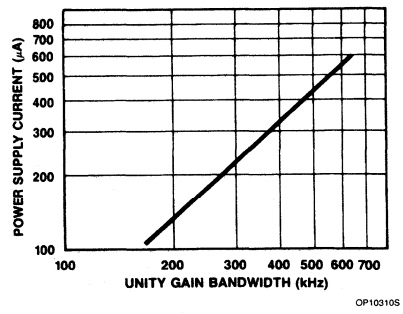
If extremely low signal distortion (< 0.05%) is required at low supply voltages, exclude the common-mode crossover point (V_{B1}) from the common-mode signal range. This can be accomplished by proper bias selection or by using an inverting amplifier configuration.

Most single supply designs necessitate that the inputs to the op amp be biased between V_{CC} and ground. This is to assure that the input signal swing is within the working common-mode range of the amplifier. This leads to another helpful and unique property of the NE5230 that other CMOS and bipolar low voltage parts cannot achieve. It is the simple fact that the input common-mode voltage can go beyond either the positive or negative supply voltages. This benefit is made very clear in a non-inverting voltage-follower configuration. This is shown in Figure 4 where the input sine wave allows an undistorted output sine wave which will swing less than 100mV of either supply voltage. Many competitive parts will show severe clipping caused by input common-mode limitations. The NE5230 in this configuration offers more freedom for quiescent biasing of the inputs close to the positive supply rail where similar op amps would not allow signal processing.

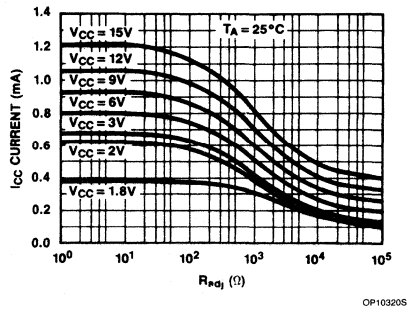
There are not as many considerations when designing with the NE5230 as with other devices. Since the NE5230 is internally-compensated and has a unity gain-bandwidth of 600kHz, board layout is not so stringent as for very high frequency devices such as the NE5205. The output capability of the NE5230 allows it to drive relatively high capacitive loads and small resistive loads. The power supply pins should be decoupled with a low-pass RC network as close to the supply pins as possible to eliminate 60Hz and other external power line noise, although the power supply rejection ratio (PSRR) for the part is very high. The pinout for the NE5230 is the same as the standard single op amp pinout with the exception of the bias current adjusting pin.

REMOTE TRANSDUCER WITH CURRENT TRANSMISSION

There are many ways to transmit information along two wires, but current transmission is



a. Unity Gain Bandwidth vs Power Supply Current for $V_{CC} = \pm 0.9V$



b. I_{CC} Current vs Bias Current Adjusting Resistor for Several Supply Voltages

Figure 3

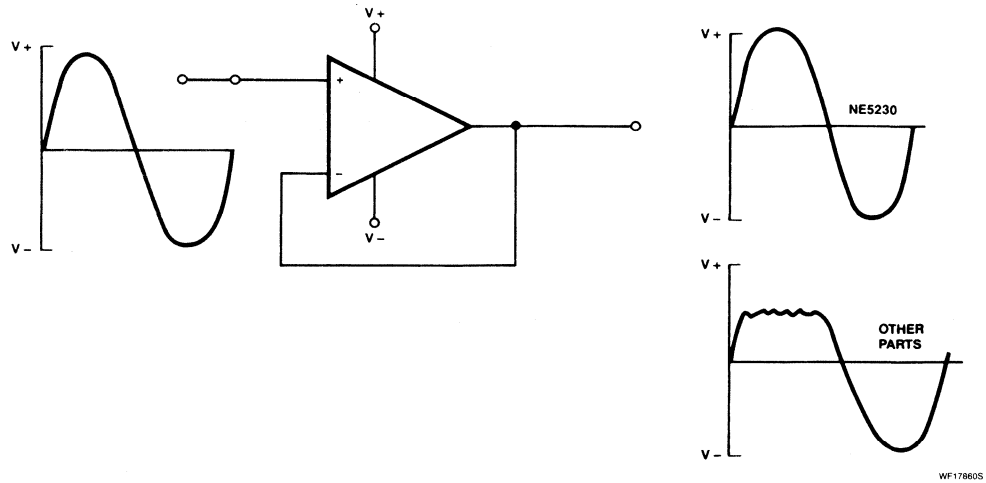


Figure 4. In a Non-Inverting Voltage-Follower Configuration, the NE5230 will Give Full Rail-to-Rail Swing. Other Low Voltage Amplifiers will not Because they are Limited by their Input Common-Mode Range and Output Swing Capability

the most beneficial when the sensing of remote signals is the aim. It is further enhanced in the form of 4 to 20mA information which is used in many control-type systems. This method of transmission provides immunity from line voltage drops, large load resistance variations, and voltage noise pickup. The zero reference of 4mA not only can show if there is a break in the line when no current is flowing, but also can power the transducer at the remote location. Usually the transducer itself is not equipped to provide for the current transmission. The unique features of the NE5230 can provide high output current capability coupled with low power consumption. It can be remotely connected to the transducer to create a current loop with minimal external components. The circuit for this is shown in Figure 5. Here, the part is configured as a voltage-to-current, or transconductance amplifier. This is a novel circuit that takes advantage of the NE5230's large open-loop gain. In AC applications, the load current will decrease as the open-loop gain rolls off in magnitude. The low offset voltage and current sinking capabilities of the NE5230 must also be considered in this application.

The NE5230 circuit shown in Figure 5 is a pseudo transistor configuration. The inverting input is equivalent to the "base," the point where V_{EE} and the non-inverting input meet is the "emitter," and the connection after the output diode meets the V_{CC} pin is the collector. The output diode is essential to keep the output from saturating in this configuration. From here it can be seen that the base and emitter form a voltage-follower and the voltage present at R_C must equal the input voltage present at the inverting input. Also, the emitter and collector form a current-follower and the current flowing through R_C is equivalent to the current through R_L and the amplifier. This sets up the current loop. Therefore, the following equation can be formulated for the working current transmission line. The load current is:

$$I_L = V_{IN} / R_C \quad (2)$$

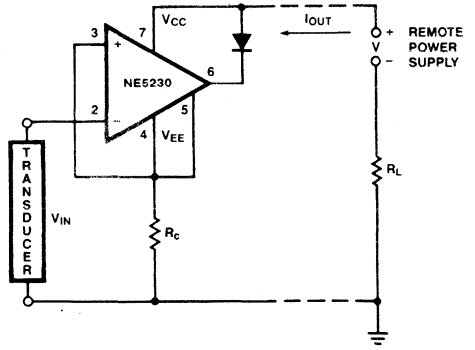
and proportional to the input voltage for a set R_C. Also, the current is constant no matter what load resistance is used while within the operating bandwidth range of the op amp. When the NE5230's supply voltage falls past a certain point, the current cannot remain constant. This is the "voltage compliance" and is very good for this application because of the near rail output voltage. The equation that determines the voltage compliance as well as the largest possible load resistor for the NE5230 is as follows:

$$R_{L\ max} = [V_{remote\ supply}) - V_{CC\ min} - V_{IN\ max}] / I_L \quad (3)$$

Where $V_{CC\ min}$ is the worst-case power supply voltage (approximately 1.8V) that will still keep the part operational. As an example, when using a 15V remote power supply, a current sensing resistor of 1Ω, and an input voltage (V_{IN}) of 20mV, the output current (I_L) is 20mA. Furthermore, a load resistance of zero to approximately 650Ω can be inserted in the loop without any change in current when the bias current-control pin is tied to the negative supply pin. The voltage drop across the load and line resistance will not affect the NE5230 because it will operate down to 1.8V. With a 15V remote supply, the voltage available at the amplifier is still enough to power it with the maximum 20mA output into the 650Ω load.

What this means is that several instruments, such as a chart recorder, a meter, or a controller, as well as a long cable, can be connected in series on the loop and still obtain accurate readings if the total resistance does not exceed 650Ω. Furthermore, any variation of resistance in this range will not change the output current.

Any voltage output type transducer can be used, but one that does not need external DC voltage or current excitation to limit the maximum possible load resistance is preferable. Even this problem can be surmounted if the supply power needed by the transducer is compatible with the NE5230. The power goes up the line to the transducer and amplifier while the transducer signal is sent back via the current output of the NE5230 transconductance configuration. The voltage range on the input can be changed for transducers that produce a large output by simply increasing the current sense resistor to get the corresponding 4 to 20mA output current. If a very long line is used which causes high line resistance, a current repeater could be inserted into the line. The same configuration of Figure 5 can be used

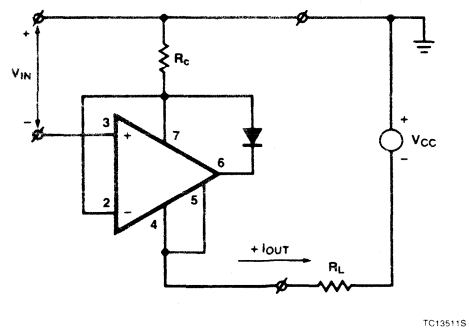


NOTES:
1. $I_{OUT} = V_{IN}/R_C$
2. $R_{L\ max} \simeq \frac{V_{REMOTE} - 1.8V - V_{IN\ max}}{I_{OUT}}$

For $R_C = 1\Omega$

I_{OUT}	V_{IN}
4mA	4mV
20mA	20mV

a. The NE5230 as a Remote Transducer Transconductance Amp With 4 – 20mA Current Transmission Output Capability



b. The Same Type of Circuit as Figure 5a, but for Sourcing Current to the Load

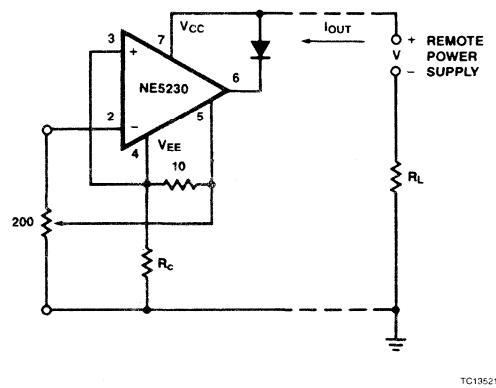
Figure 5

with exception of a resistor across the input and line ground to convert the current back to voltage. Again, the current sensing resistor will set up the transconductance and the part will receive power from the line.

TEMPERATURE TRANSDUCER

A variation on the previous circuit makes use of the supply current control pin. The voltage present at this pin is proportional to absolute temperature (PTAT) because it is produced by the amplifier bias current through an internal resistor divider in a PTAT cell. If the control pin is connected to the input pin, the NE5230 itself can be used as a temperature transducer. If the center tap of a resistive pot is connected to the control pin with one side to ground and the other to the inverting input, the voltage can be changed to give different temperature versus output current conditions (see Figure 6). For additional control, the output current is still proportional to the input voltage differential divided by the current sense resistor.

When using the NE5230 as a temperature transducer, the thermal considerations in the previous section must be kept in mind.



NOTES:
1. $I_{OUT} = V_{IN}/R_C$
2. $R_L Max \simeq \frac{V_{REMOTE} - 1.8V - V_{IN}Max}{I_{OUT}}$

For $RC = 1\Omega$

I_{OUT}	V_{IN}
4mA	4mV
20mA	20mV

Figure 6. NE5230 Remote Temperature Transducer Utilizing 4 – 20mA Current Transmission. This Application Shows the use of the Accessibility of the PTAT Cell in the Device to Make the Part, Itself, a Transducer

HALF-WAVE RECTIFIER WITH RAIL-TO-GROUND OUTPUT SWING

Since the NE5230 input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction becomes a simple task. All that is needed are two external resistors; there is no need for diodes or matched resistors. Moreover, it can have either positive- or negative-going outputs, depending on the way the bias is arranged. This can be seen in Figure 7. Circuit (a) is biased to ground, while circuit (b) is biased to the positive supply. This rather unusual biasing does not cause any problems with the NE5230 because of the unique internal saturation detectors incorporated into the part to keep the PNP and NPN output transistors out of "hard" saturation. It is therefore relatively quick to recover from a saturated output condition. Furthermore, the device does not have parasitic current draw when the output is biased to either rail. This makes it possible to bias the NE5230 into "saturation" and obtain half-wave rectification with good recovery. The simplicity of biasing and the rail-to-ground half-sine wave swing are unique to this device. The circuit gain can be changed by the standard op amp gain equations for an inverting configuration.

It can be seen in these configurations that the op amp cannot respond to one-half of the incoming waveform. It cannot respond because the waveform forces the amplifier to swing the output beyond either ground or the positive supply rail, depending on the biasing, and, also, the output cannot disengage during this half cycle. During the other half cycle, however, the amplifier achieves a half-wave that can have a peak equal to the total supply voltage. The photographs in Figure 8 show the effect of the different biasing schemes, as well as the wide bandwidth (it works over the full audio range), that the NE5230 can achieve in this configuration.

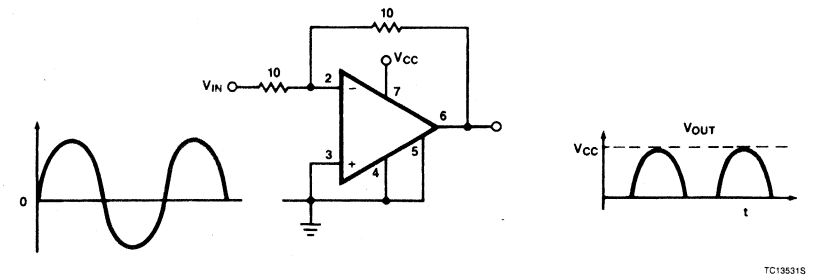
By adding another NE5230 in an inverting summer configuration at the output of the half-wave rectifier, a full-wave can be realized. The values for the input and feedback resistors must be chosen so that each peak will have equal amplitudes. A table for calculating values is included in Figure 9. The summing network combines the input signal at the half-wave and adds it to double the half-wave's output, resulting in the full-wave. The output waveform can be referenced to the supply or ground, depending on the half-wave configuration. Again, no diodes are needed to achieve the rectification.

This circuit could be used in conjunction with the remote transducer to convert a received AC output signal into a DC level at the full-wave output for meters or chart recorders that need DC levels.

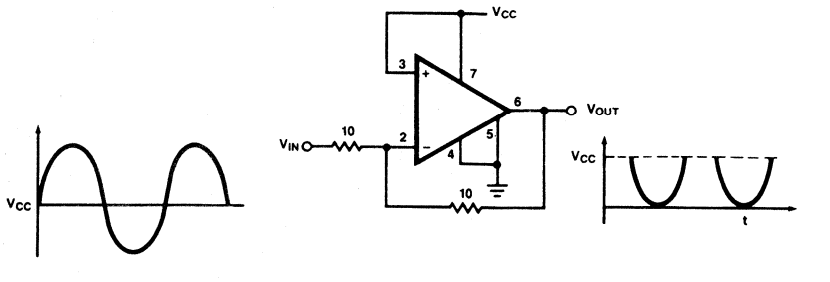
CONCLUSION

The NE5230 is a versatile op amp in its own right. The part was designed to give low voltage and low power operation without the limitations of previously available amplifiers that had a multitude of problems. The previous application examples are unique to this amplifier and save the user money by excluding various passive components that would have been needed if not for the NE5230's special input and output stages.

The NE5230 has a combination of novel specifications which allows the designer to implement it easily into existing low-supply voltage designs and to enhance their performance. It also offers the engineer the freedom to achieve greater amplifier system design goals. The low input referenced noise voltage eases the restrictions on designs



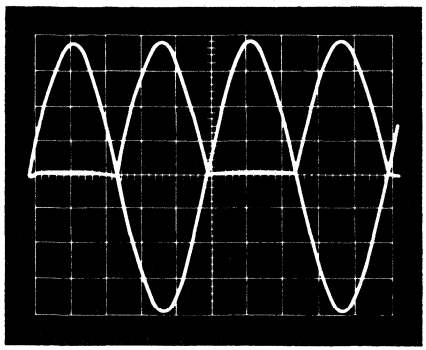
a. Rail-to-Ground Output Swing Referenced to Ground



b. Negative-Going Output Referenced to V_{CC}

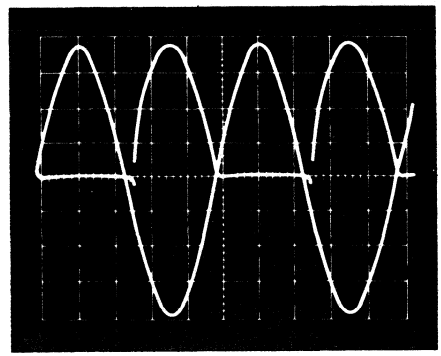
Figure 7. Half-Wave Rectifier With Positive-Going Output Swings

where S/N ratios are important. The wide full-power bandwidth and output load handling capability allow it to fit into portable audio applications. The truly ample open-loop gain and low power consumption easily lend themselves to the requirements of remote transducer applications. The low, untrimmed typical offset voltage and low offset currents help to reduce errors in signal processing designs. The amplifier is well isolated from changes on the supply lines by its typical power supply rejection ratio of 105dB.



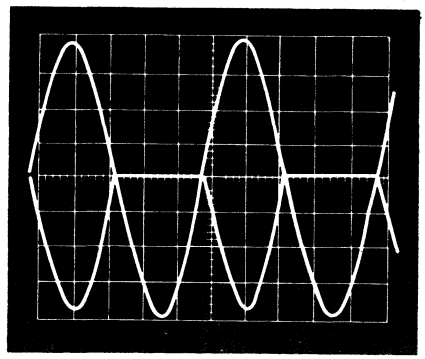
WF17870S

500mV/DIV 200μS/DIV
Biased to Ground



WF17880S

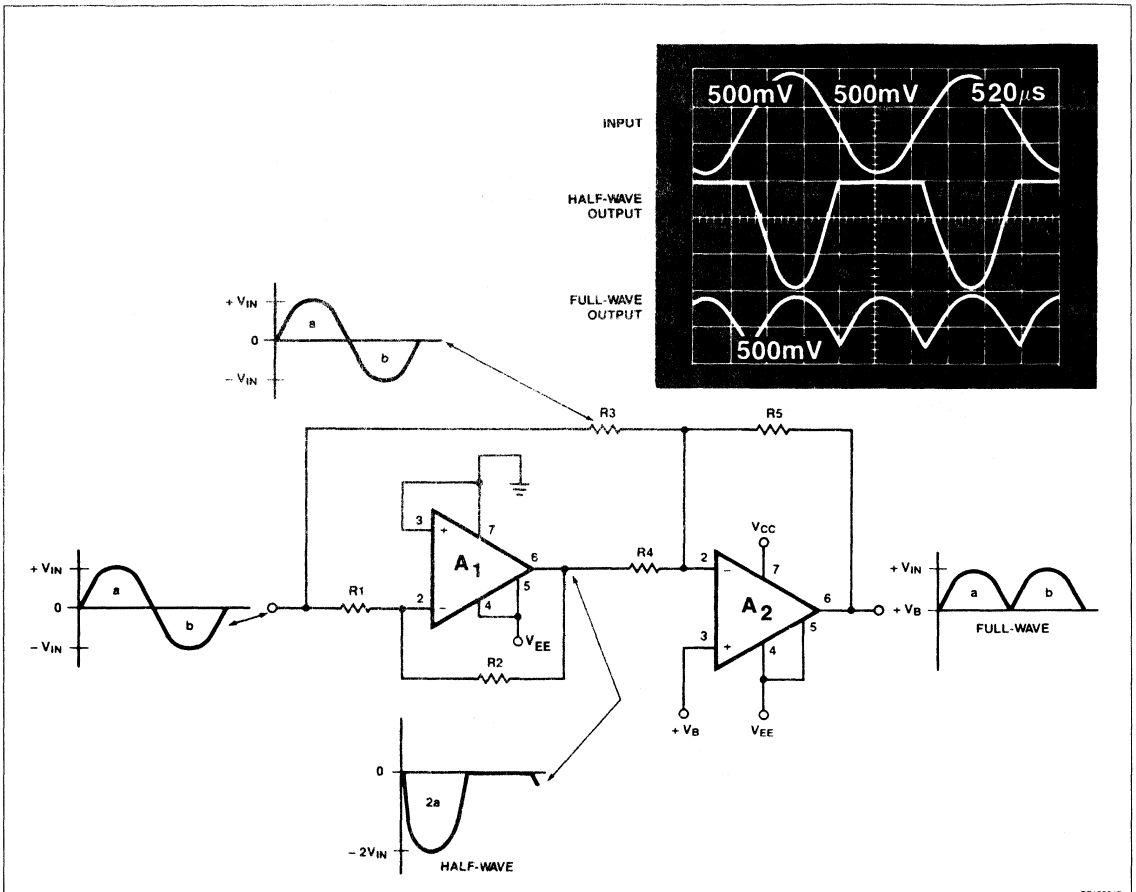
500mV/DIV 20μS/DIV
Biased to Ground



WF17890S

500mV/DIV 20μS/DIV
Biased to Positive Rail

Figure 8. Performance Waveforms for the Circuits in Figure 7. Good Response is Shown at 1 and 10kHz for Both Circuits Under Full Swing With a 2V Supply



NOTES:
R2 = 2 R1
R4 = R5 = R3
+ V_B will vary output reference.
For single supply operation V_{EE} can be grounded on A2.

Figure 9. Adding an Inverting Summer to the Input and Output of the Half-Wave Rectifier will Result in Full-Wave

REFERENCES

Johan H. Huijsing, "Multi-stage Amplifier with Capacitive Nesting for Frequency Compensation," U.S. Patent Application Serial No. 602.234, filed April 19, 1984.

Bob Blauschild, "Differential Amplifier with Rail-to-Rail Capability," U.S. Patent Application Serial No. 525.181, filed August 23, 1983.

Operational Amplifiers — Characteristics and Applications, Robert G. Irvine, Prentice-Hall, Inc., Englewood Cliffs, NJ 07632, 1981.

Transducer Interface Handbook — A Guide to Analog Signal Conditioning, Edited by Daniel H. Sheingold, Analog Devices, Inc., Norwood, MA 02062, 1981.

NE/SA/SE5512
Dual High-Performance Operational Amplifier

Product Specification

DESCRIPTION

The 5512 series of high-performance operational amplifiers provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector-to-emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability, yet have low supply quiescent current.

APPLICATIONS

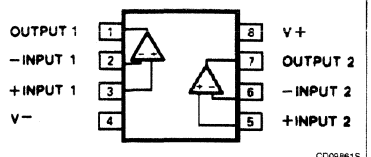
- **AC amplifiers**
- **RC active filters**
- **Transducer amplifiers**
- **DC gain block**
- **Battery operation**
- **Instrumentation amplifiers**

FEATURES

- **Low input bias $< \pm 20$nA**
- **Low input offset current $< \pm 20$nA**
- **Low input offset voltage < 1mV**
- **Low V_{OS} temperature drift $5\mu V/°C$**
- **Low input bias temperature drift 40pA/°C**
- **Low input voltage noise 30nV/$\sqrt{Hz}$**
- **Low supply current 1.5mA/amp**
- **High slew rate 1.0V/μs**
- **High CMRR 100dB**
- **High input impedance 100MΩ**
- **High PSRR 110dB**
- **High differential input voltage limit**
- **No crossover distortion**
- **Indefinite output short circuit protection**
- **Internally-compensated for unity gain**
- **600Ω drive capability**
- **MIL-STD processing available**

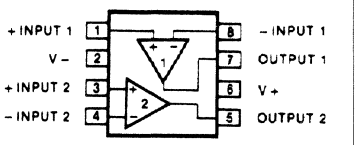
PIN CONFIGURATIONS

FE, N Packages



TOP VIEW

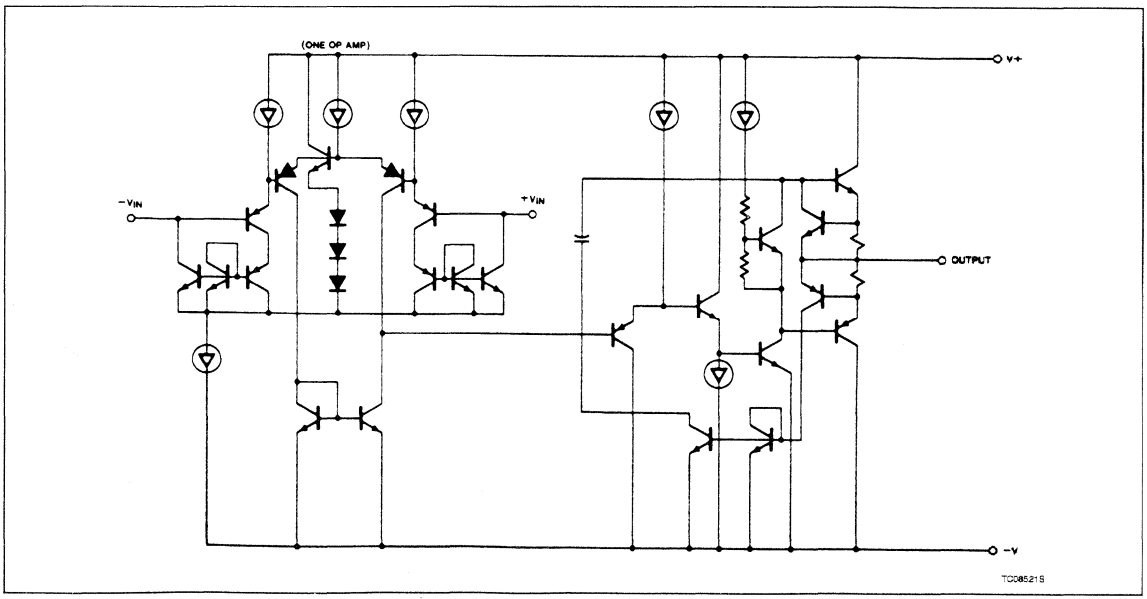
D Package[1]



TOP VIEW

NOTE:
1. The D package pinout is not functionally identical to the FE or N pinout.

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0°C to +70°C	NE5512D
8-Pin Ceramic DIP	0°C to +70°C	NE5512FE
8-Pin Plastic DIP	0°C to +70°C	NE5512N
8-Pin Plastic SO	−40°C to +85°C	SA5512D
8-Pin Plastic DIP	−40°C to +85°C	SA5512N
8-Pin Ceramic DIP	−55°C to +125°C	SE5512FE
8-Pin Plastic DIP	−55°C to +125°C	SE5512N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±16	V
$P_{D\ MAX}$	Maximum power dissipation, T_A = 25°C (still air)[1]		
	FE package	850	mW
	N package	1212	mW
	D package	800	mW
T_A	Operating ambient temperature range		
	NE5512	0 to +70	°C
	SA5512	−40 to +85	°C
	SE5512	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. The following derating factors should be applied above 25°C:
   FE package at 6.8mW/°C
   N package at 9.7mW/°C
   D package at 6.4mW/°C

ELECTRICAL PERFORMANCE CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25°C$ over temperature range, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5512			NE/SA5512			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS} $\Delta V_{OS}/\Delta T$	Input offset voltage	$R_S = 100\Omega$ $T_A = +25°C$ Over temp.		0.7 1 4	2 3		1 1.5 5	5 6	mV $\mu V/°C$
I_{OS} $\Delta I_{OS}/\Delta T$	Input offset current	$R_S = 100k\Omega$ $T_A = +25°C$ Over temp.		3 4 30	10 20		6 8 40	20 30	nA pA/°C
I_{BIAS} $\Delta I_{BIAS}/\Delta T$	Input bias current	$R_S = 100k\Omega$ $T = +25°C$ Over temp.		3 4 30	10 20		6 8 40	20 30	nA pA/°C
R_{IN}	Input resistance differential	$T_A = 25°C$		100			100		MΩ
V_{CM}	Input common mode range	$T_A = 25°C$ Over temp.	±13.5 ±13	±13.7 ±13.2		±13.5 ±13	±13.7 ±13.2		V
CMRR	Input common-mode rejection ratio	$V_{CC} = \pm 15V$ $V_{IN} = \pm 13.5V$ $T_A = 25°C$ $V_{IN} = \pm 13V$ Over temp.	70	100		70	100		dB
A_V	Large-signal voltage gain	$R_L = 2k\Omega$ $T_A = 25°C$ $V_O = \pm 10V$ over temp.	50 25	200		50 25	200		V/mV
SR	Slew rate	$T_A = 25°C$	0.6	1			1		$V/\mu s$
GBW	Small-signal unity gain bandwidth	$T_A = 25°C$		3			3		MHz
θ_M	Phase margin	$T_A = 25°C$		45			45		degree
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ $T_A = 25°C$ Over temp.	±13 ±12.5	±13.5 ±13		±13 ±12.5	±13.5 ±13		V
V_{OUT}	Output voltage swing	$R_L = 600\Omega$[1] $T_A = 25°C$ Over temp.	±10 ±7.5	±11.5 ±9		±10 ±8	±11.5 ±9		V
I_{CC}	Power supply current	R_L = Open $T_A = 25°C$ Over temp.		3.4 3.6	5 5.5		3.4 3.6	5 5.5	mA
PSRR	Power supply rejection ratio	$T_A = 25°C$ Over temp.	80 80	110 100		80 80	110 100		dB
AA	Amplifier-to-amplifier coupling	f = 1kHz to 20kHz, $T_A = 25°C$		−120			−120		dB
THD	Total harmonic distortion	f = 10kHz $T_A = 25°C$ $V_O = 7V_{RMS}$		0.01			0.01		%
V_{NOISE}	Input noise voltage	f = 1kHz $T_A = 25°C$		30			30		$nV/\sqrt{Hz}$
I_{NOISE}	Input noise current	f = 1kHz $T_A = 25°C$		0.2			0.2		$pA/\sqrt{Hz}$
I_{SC}	Short-circuit current	$\pm 15V$, $T_A = 25°C$		40			40		mA

NOTE:
1. Not to exceed maximum package power dissipation.

NE/SE5514
Quad High-Performance Operational Amplifier

Product Specification

DESCRIPTION

The NE/SE5514 family of quad operational amplifiers sets new standards in bipolar quad amplifier performance. The amplifiers feature low input bias current and low offset voltages. Pinout is identical to LM324/LM348 which facilitates direct product substitution for improved system performance. Output characteristics are similar to a μA741 with improved slew and drive capability.

FEATURES

- **Low input bias current: < ± 3nA**
- **Low input offset current: < ± 3nA**
- **Low input offset voltage: < 1mV**
- **Low supply current: 1.5mA/A**
- **1V/μs slew rate**
- **High input impedance: 100MΩ**
- **High common-mode impedance: 10GΩ**
- **Internal compensation for unity gain**
- **600Ω drive capability ($7V_{RMS}$)**

APPLICATIONS

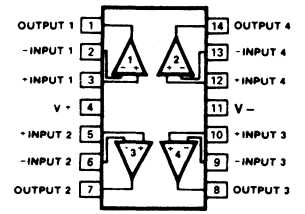
- **AC amplifiers**
- **RC active filters**
- **Transducer amplifiers**
- **DC gain block**
- **Instrumentation amplifier**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL package	0 to +70°C	NE5514D
14-Pin Ceramic DIP	0 to +70°C	NE5514F
14-Pin Plastic DIP	0 to +70°C	NE5514N
14-Pin Ceramic DIP	−55°C to +125°C	SE5514F
14-Pin Plastic DIP	−55°C to +125°C	SE5514N

PIN CONFIGURATIONS

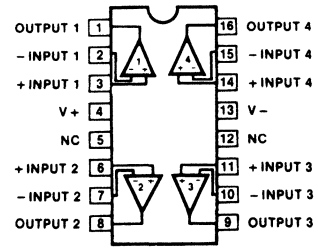
F, N Packages



TOP VIEW

CD11660S

D Package[1]

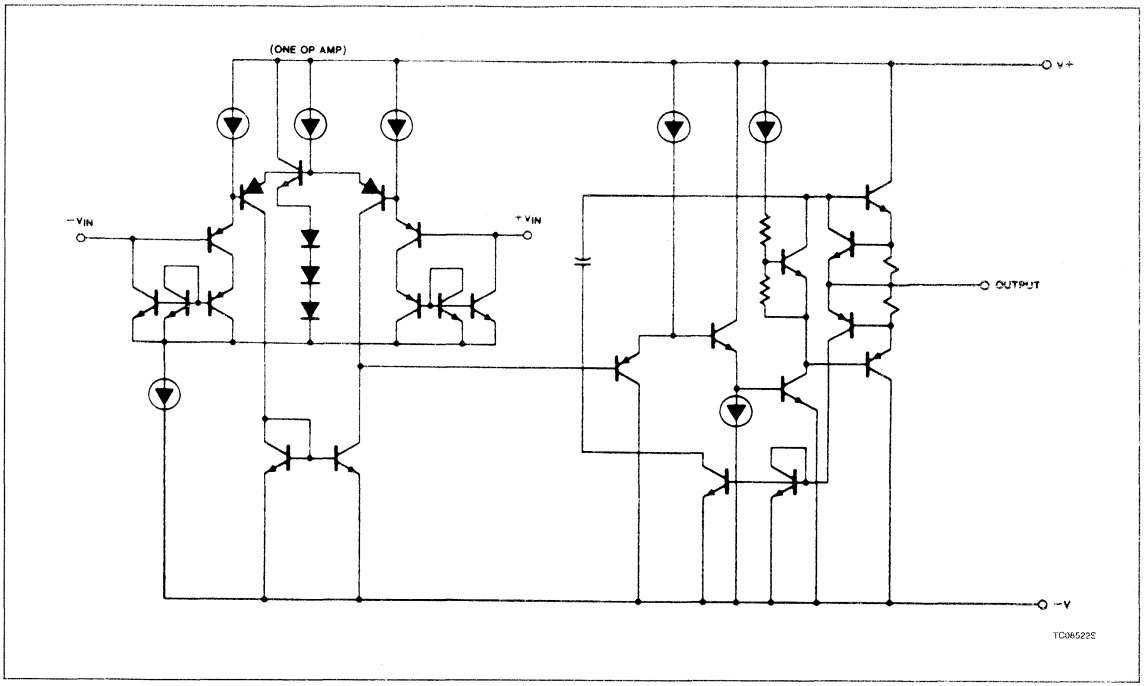


TOP VIEW

CD11670S

NOTE:
1. SOL – Released in 16-lead large SO package only. Pinout is different than F, N packages.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±16	V
V_{DIFF}	Differential input voltage	32	V
V_{IN}	Input voltage	0 to 32	V
	Output short to ground	Continuous	
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
T_A	Operating ambient temperature range		
	NE5514	0 to 70	°C
	SE5514	−55 to +125	°C
P_{MAX}	Maximum power disspation T_A = 25°C (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1250	mW

NOTE:

1. The following derating factors should be applied above 25°C:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 10.0mW/°C.

ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5514			NE5514			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 100\Omega$, $T_A = +25°C$,		0.7	2		1	5	mV
		Over temp.		1	3		1.5	6	
ΔV_{OS}		Over temp.		4			5		$\mu V/°C$
I_{OS}	Input offset current	$R_S = 100k\Omega$, $T_A = +25°C$,		3	10		6	20	nA
		Over temp.		4	20		8	30	
ΔI_{OS}		Over temp.		30			40		pA/°C
I_{BIAS}	Input bias current	$R_S = 100k\Omega$, $T_A = +25°C$,		3	10		6	20	nA
		Over temp.		4	20		8	30	
ΔI_{BIAS}		Over temp.		30			40		pA/°C
R_{IN}	Input resistance differential	$T_A = 25°C$		100			100		MΩ
V_{CM}	Input common mode range	$T_A = 25°C$,	±13.5	±13.7		±13.5	±13.7		V
		Over temp.	±13	±13.2		±13	±13.2		
CMRR	Input common-mode rejection ratio	$V_{CC} = \pm 15V$, c, $V_{IN} = \pm 13.5V$ @ $T_A = 25°C$, $V_{IN} = \pm 13V$ @ Over temp.	70	100		70	100		dB
A_V	Large-signal voltage gain	$R_L = 2k\Omega$, $T_A = 25°C$	50	200		50	200		V/mV
		$V_C = \pm 10V$, Over temp.	25			25			
SR	Slew rate	$T_A = 25°C$	0.6	1		0.6	1		$V/\mu s$
GBW	Small-signal unity gain bandwidth	$T_A = 25°C$		3			3		MHz
θ_M	Phase margin	$T_A = 25°C$		45			45		Degr
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $T_A = 25°C$,	±13	±13.5		±13	±13.5		V
		Over temp.	±12.5	±13		±12.5	±13		
V_{OUT}	Output voltage swing	$R_L = 600\Omega$, $T_A = 25°C$,	±10	±11.5		±10	±11.5		V
		Over temp.	±7.5	±9		±8	±9		
I_{CC}	Power supply current	R_L = Open, $T_A = 25°C$,		6	10		6	10	mA
		Over temp.		7	12		7	12	
PSRR	Power supply rejection ratio	Over temp.	80	110		80	110		dB
AA	Amplifier to amplifier coupling	f = 1kHz to 20kHz, $T_A = 25°C$		−120			−120		dB
THD	Total harmonic distortion	f = 10kHz, $T_A = 25°C$,		0.01			0.01		%
		$V_O = 7V_{RMS}$							
V_{NOISE}	Input noise voltage	f = 1kHz, $T_A = 25°C$		30			30		$nV/\sqrt{Hz}$
I_{SC}	Short-circuit current	$T_A = 25°C$	10	40	60	10	40	60	mA

NE/SE5532/5532A

Internally-Compensated Dual Low Noise Operational Amplifier

Product Specification

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

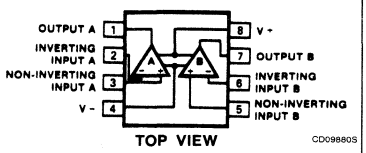
This makes the device especially suitable for application in high-quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used because it has guaranteed noise voltage specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, $10V_{RMS}$**
- **Input noise voltage: $5nV/\sqrt{Hz}$ (typical)**
- **DC voltage gain: 50000**
- **AC voltage gain: 2200 at 10kHz**
- **Power bandwidth: 140kHz**
- **Slew rate: $9V/\mu s$**
- **Large supply voltage range: ±3 to ±20V**
- **Compensated for unity gain**

PIN CONFIGURATIONS

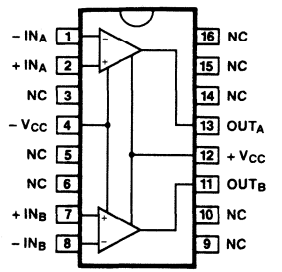
FE, N Packages



TOP VIEW

CD09880S

D Package[1]

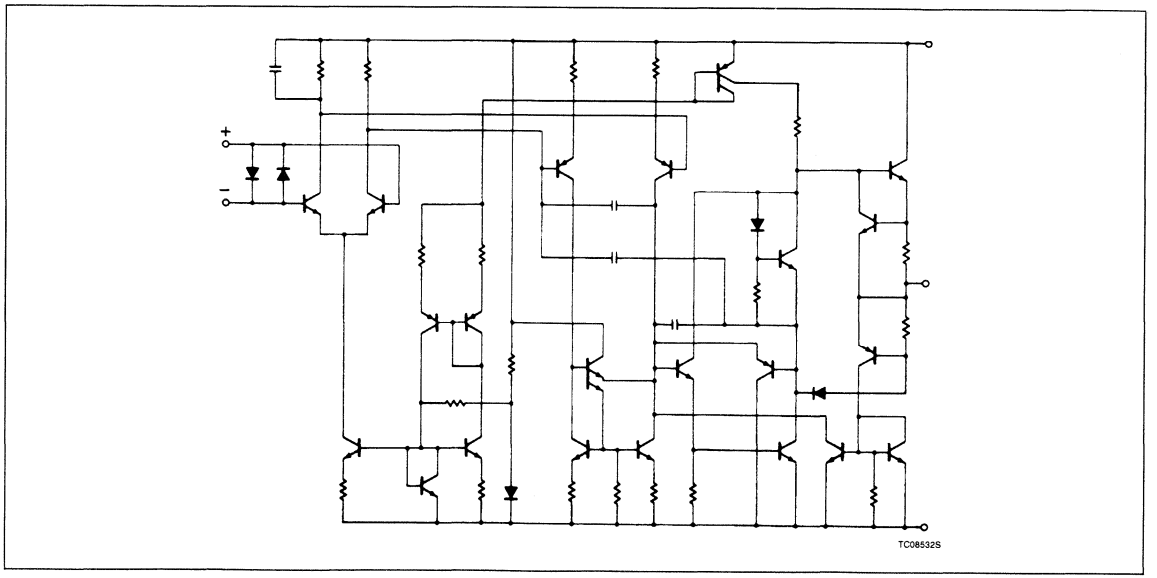


TOP VIEW

CD09891S

NOTE:
1. SOL and *non-standard* pinout.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



Internally-Compensated Dual Low Noise Operational Amplifier

NE/SE5532/5532A

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to 70°C	NE5532N
8-Pin Ceramic DIP	0 to 70°C	NE5532FE
8-Pin Plastic DIP	0 to 70°C	NE5532AN
8-Pin Ceramic DIP	0 to 70°C	NE5532AFE
8-Pin Ceramic DIP	−55°C to +125°C	SE5532FE
8-Pin Ceramic DIP	−55°C to +125°C	SE5532AFE
16-Pin Plastic SOL	0 to 70°C	NE5532D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	$\pm V_{SUPPLY}$	V
V_{DIFF}	Differential input voltage[1]	±0.5	V
T_A	Operating temperature range NE5532/A SE5532/A	 0 to 70 −55 to +125	 °C °C
T_{STG}	Storage temperature	−65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Maximum power dissipation, T_A = 25°C, (still-air)[2] N package F package D package	 1200 1000 1200	 mW mW mW
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. Thermal resistances of the above packages are as follows:
   N package at 100°C/W.
   F package at 135°C/W.
   D package at 105°C/W.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	SE5532/5532A			NE5532/5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Offset current				100		10	150	nA
		Over temperature			200			200	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			200	400		200	800	nA
		Over temperature			700			1000	nA
$\Delta I_B/\Delta T$				5			5		nA/°C
I_{CC}	Supply current			8	10.5		8	16	mA
		Over temperature			13				mA
V_{CM}	Common-mode input range		±12	±13		±12	±13		V
CMRR	Common-mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	µV/V
A_{VOL}	Large-signal voltage gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	40	50		15	50		V/mV
		Over temperature	20			10			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
		Over temperature	±10	±12		±10	±12		V
		$R_L \geq 600\Omega$, $V_S = \pm 18V$	±15	±16		±15	±16		V
		Over temperature	±12	±14		±12	±14		V
		$R_L \geq 2k\Omega$	±13	±13.5		±13	±13.5		V
		Over temperature	±12	±12.5		±10	±12.5		V
R_{IN}	Input resistance		30	300		30	300		kΩ
I_{SC}	Output short circuit current		10	38	60	10	38	60	mA

NOTES:

1. Diodes protect the inputs against overvoltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the package thermal resistance.
3. Output may be shorted to ground at $V_S = \pm 15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

Internally-Compensated Dual Low Noise Operational Amplifier

NE/SE5532/5532A

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

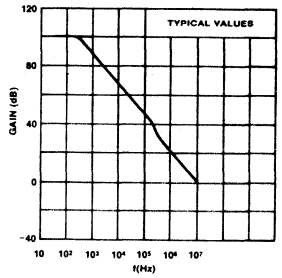
SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5532/5532A			UNIT
			Min	Typ	Max	
R_{OUT}	Output resistance	A_V = 30dB Closed-loop f = 10kHz, $R_L = 600\Omega$		0.3		Ω
	Overshoot	Voltage-follower $V_{IN} = 100mV_{P-P}$ C_L = 100pF, $R_L = 600\Omega$		10		%
A_V	Gain	f = 10kHz		2.2		V/mV
GBW	Gain bandwidth product	C_L = 100pF, $R_L = 600\Omega$		10		MHz
SR	Slew rate			9		V/μs
	Power bandwidth	$V_{OUT} = \pm 10V$ $V_{OUT} = \pm 14V$, $R_L = 600\Omega$, $V_{CC} = \pm 18V$		140 100		kHz kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5532			NE/SE5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{NOISE}	Input noise voltage	f_O = 30Hz f_O = 1kHz		8 5			8 5	12 6	nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$
I_{NOISE}	Input noise current	f_O = 30Hz f_O = 1kHz		2.7 0.7			2.7 0.7		pA/$\sqrt{Hz}$ pA/$\sqrt{Hz}$
	Channel separation	f = 1kHz, $R_S = 5k\Omega$		110			110		dB

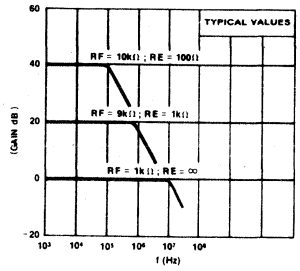
TYPICAL PERFORMANCE CHARACTERISTICS

Open-Loop Frequency Response



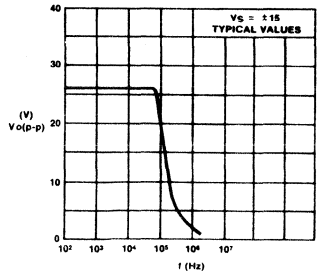
OP04870S

Closed-Loop Frequency Response



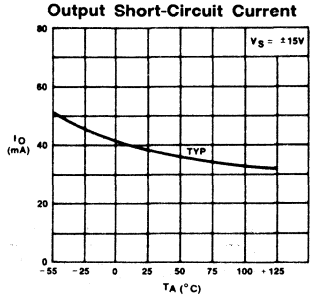
OPT4880S

Large-Signal Frequency Response



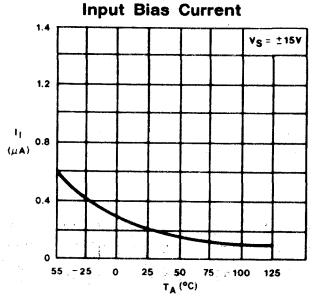
OPT4890S

Output Short-Circuit Current



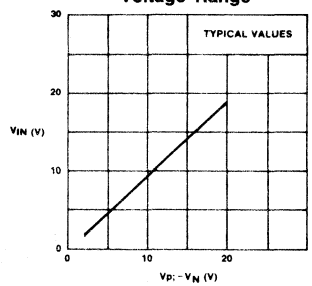
OP04900S

Input Bias Current



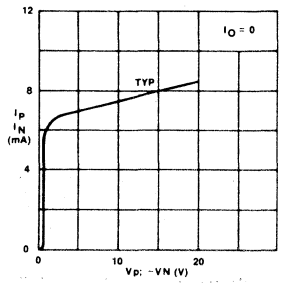
OP04910S

Input Common-Mode Voltage Range



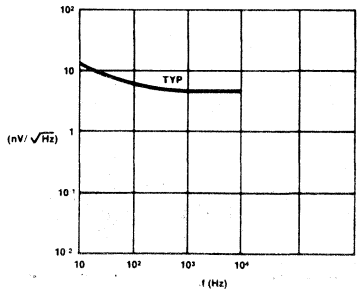
OP04920S

Supply Current



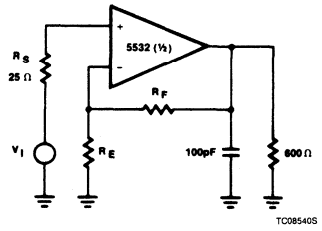
OP04930S

Input Noise Voltage Density

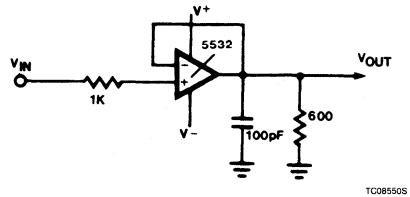


OP04940S

TEST CIRCUITS



Closed-Loop Frequency Response



Voltage-Follower

NE5533/5533A
NE/SA/SE5534/5534A
Dual and Single Low Noise Op Amp

Product Specification

DESCRIPTION

The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, $10V_{RMS}$ at $V_S = \pm 18V$**
- **Input noise voltage: $4nV/\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwith: 200kHz**
- **Slew rate: $13V/\mu s$**
- **Large supply voltage range: ±3 to ±20V**
- **5534 MIL-STD processing available**

APPLICATIONS

- **Audio equipment**
- **Instrumentation and control circuits**
- **Telephone channel amplifiers**
- **Medical equipment**

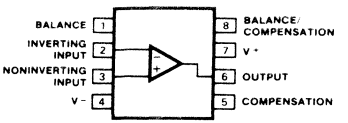
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5533N
16-Pin Plastic SO package	0 to +70°C	NE5533AD
14-Pin Plastic DIP	0 to +70°C	NE5533AN
16-Pin Plastic SO package	0 to +70°C	NE5533D
8-Pin Plastic SO package	0 to +70°C	NE5534D
8-Pin Hermetic Cerdip	0 to +70°C	NE5534FE
8-Pin Plastic DIP	0 to +70°C	NE5534N
8-Pin Plastic SO package	0 to +70°C	NE5534AD
8-Pin Hermetic Cerdip	0 to +70°C	NE5534AFE
8-Pin Plastic DIP	0 to +70°C	NE5534AN
8-Pin Plastic DIP	-40°C to +85°C	SA5534N
8-Pin Plastic SO package	-40°C to +85°C	SA5534AD
8-Pin Plastic DIP	-40°C to +85°C	SA5534AN
8-Pin Hermetic Cerdip	-55°C to +125°C	SE5534AFE
8-Pin Plastic DIP	-55°C to +125°C	SE5534N
8-Pin Hermetic Cerdip	-55°C to +125°C	SE5534FE
8-Pin Plastic DIP	-55°C to +125°C	SE5534AN

PIN CONFIGURATIONS

NE/SA/SE5534/5534A

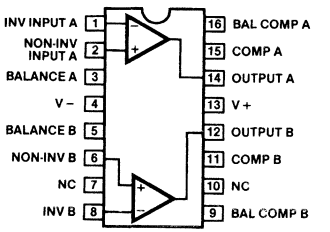
D, FE, N Packages



CD09900S

NE5533/5533A

N Package



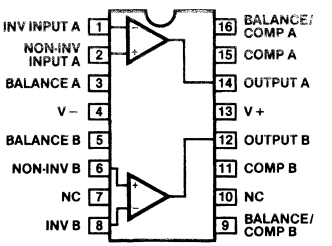
TOP VIEW

CD13740S

NE5533/5533A

D Package

D²

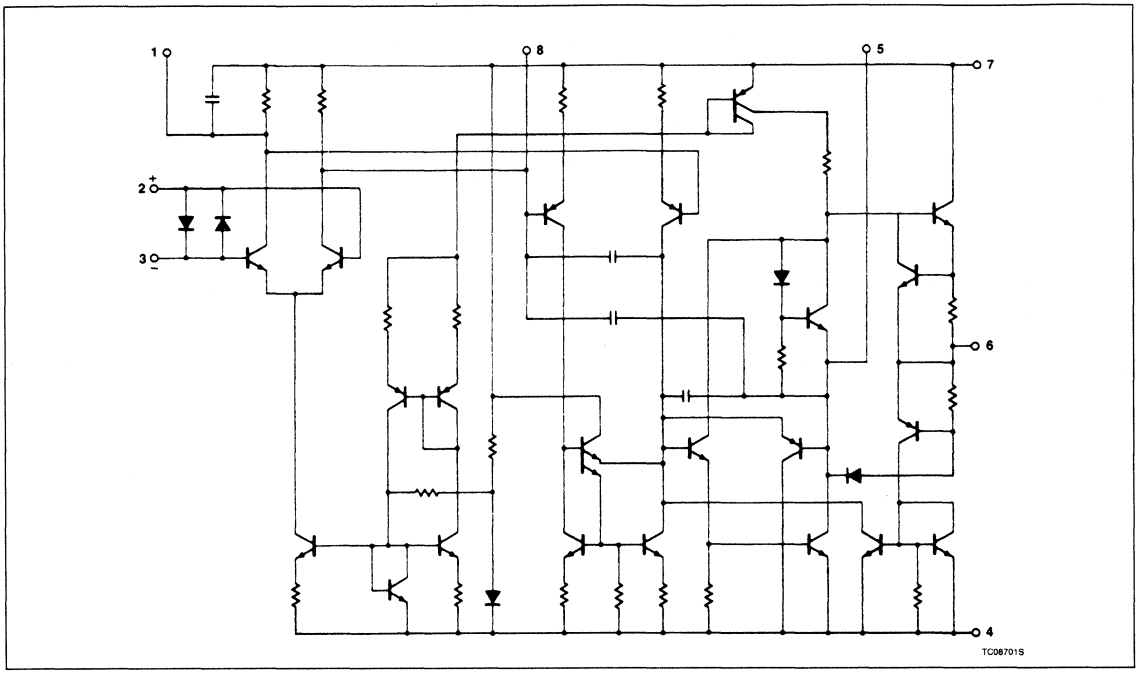


TOP VIEW

CD11390S

NOTE:
This device may not be symboled in standard format.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±0.5	V
T_A	Operating temperature range		
	SE	−55 to +125	°C
	SA	−40 to +85	°C
	NE	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation at 25°C[2]		
	5533D	1350	mW
	5533N	1500	mW
	5534D	750	mW
	5534FE	800	mW
	5534N	1150	mW
	Output short-circuit duration[3]	Indefinite	
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Diodes protect the inputs against over voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the following junction-to-ambient thermal resistance:
   - 8-pin ceramic DIP 150°C/W
   - 8-pin plastic DIP 105°C/W
   - 8-pin plastic SO 160°C/W
   - 14-pin plastic DIP 80°C/W
   - 16-pin plastic SO 90°C/W
3. Output may be shorted to ground at $V_S = \pm 15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A NE/SA5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Offset current			10	200		20	300	nA
		Over temperature			500			400	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			400	800		500	1500	nA
		Over temperature			1500			2000	nA
$\Delta I_B/\Delta T$				5			5		nA/°C
I_{CC}	Supply current per op amp			4	6 5		4	8	mA
		Over temperature			9			10	mA
V_{CM}	Common mode input range		± 12	± 13		± 12	± 13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	µV/V
A_{VOL}	Large-signal voltage gain	$R_L \geq 600\Omega$, $V_O = \pm 10V$	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$	± 12	± 13		± 12	± 13		V
		Over temperature	± 10	± 12		± 10	± 12		V
		$R_L \geq 600\Omega$, $V_S = \pm 18V$	± 15	± 16		± 15	± 16		V
		$R_L \geq 2k\Omega$	± 13	± 13.5		± 13	± 13.5		V
		Over temperature	± 12	± 12.5		± 12	± 12.5		V
R_{IN}	Input resistance		50	100		30	100		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES:
1. For NE5533/5533A/5534/5534A, $T_{MIN} = 0°C$, $T_{MAX} = 70°C$.
2. For SE5534/5534A, $T_{MIN} = -55°C$, $T_{MAX} = +125°C$.
3. For SA5534/5534A, $T_{MIN} = -40°C$, $T_{MAX} = +125°C$.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

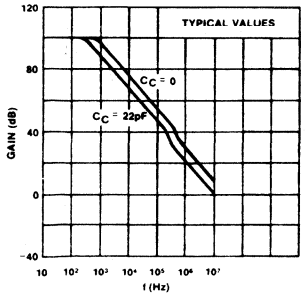
SYMBOL	PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A NESA5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_{OUT}	Output resistance	$A_V = 30dB$ closed-loop $f = 10kHz$, $R_L = 600\Omega$, $C_C = 22pF$		0.3			0.3		Ω
	Transient response	Voltage-follower, $V_{IN} = 50mV$ $R_L = 600\Omega$, $C_C = 22pF$, $C_L = 100pF$							
t_R	Rise time			20			20		ns
	Overshoot			20			20		%
	Transient response	$V_{IN} = 50mV$, $R_L = 600\Omega$ $C_C = 47pF$, $C_L = 500pF$							
t_R	Rise time			50			50		ns
	Overshoot			35			35		%
A_V	Gain	$f = 10kHz$, $C_C = 0$ $f = 10kHz$, $C_C = 22pF$		6 2.2			6 2.2		V/mV V/mV
GBW	Gain bandwidth product	$C_C = 22pF$, $C_L = 100pF$		10			10		MHz
SR	Slew rate	$C_C = 0$ $C_C = 22pF$		13 6			13 6		V/μs V/μs
	Power bandwidth	$V_{OUT} = \pm 10V$, $C_C = 0$ $V_{OUT} = \pm 10V$, $C_C = 22pF$ $V_{OUT} = \pm 14V$, $R_L = 600\Omega$ $C_C = 22pF$, $V_{CC} = \pm 18V$		200 95 70			200 95 70		kHz kHz kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = 15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{NOISE}	Input noise voltage	$f_O = 30Hz$ $f_O = 1kHz$		7 4			5.5 3.5	7 4.5	nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$
I_{NOISE}	Input noise current	$f_O = 30Hz$ $f_O = 1kHz$		2.5 0.6			1.5 0.4		pA/$\sqrt{Hz}$ pA/$\sqrt{Hz}$
	Broadband noise figure	$f = 10Hz - 20kHz$, $R_S = 5k\Omega$					0.9		dB
	Channel separation	$f = 1kHz$, $R_S = 5k\Omega$		110			110		dB

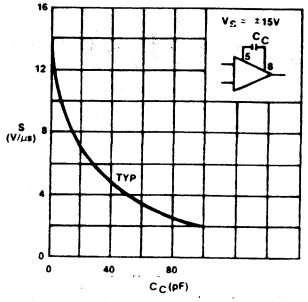
TYPICAL PERFORMANCE CHARACTERISTICS

Open-Loop Frequency Response



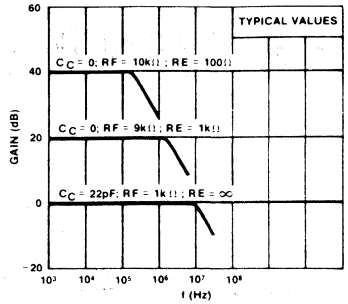
OP05060S

Slew Rate as a Function of Compensation Capacitance



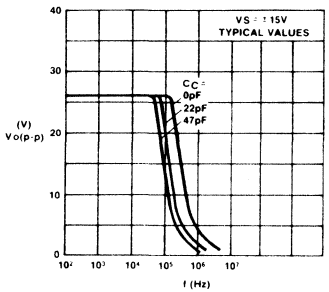
OP05070S

Closed-Loop Frequency Response



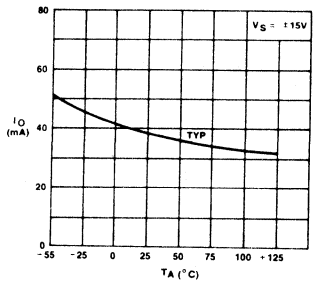
OP05090S

Large-Signal Frequency Response



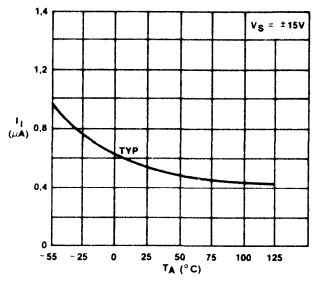
OP05080S

Output Short-Circuit Current



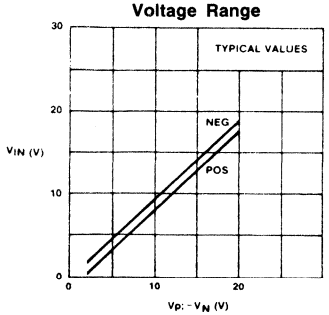
OP05100S

Input Bias Current



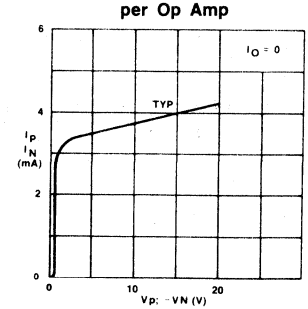
OP05110S

Input Common-Mode Voltage Range



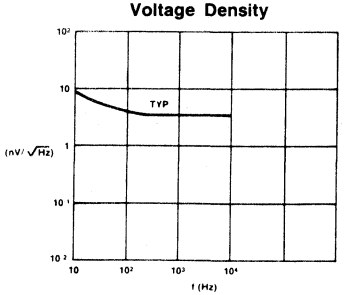
OP05120S

Supply Current per Op Amp



OP05130S

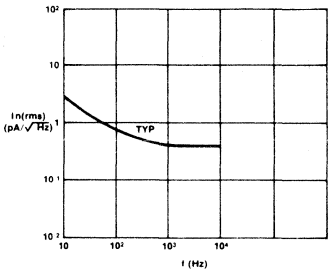
Input Noise Voltage Density



OP05140S

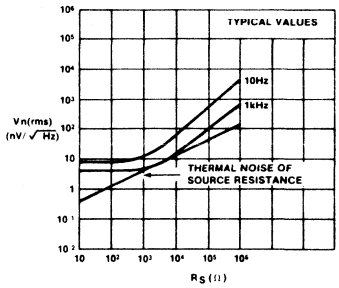
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Input Noise Current Density



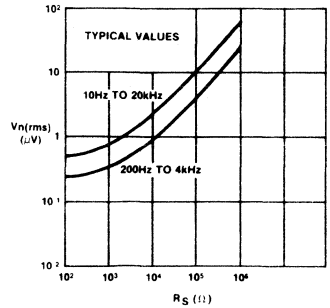
OP05150S

Total Input Noise Density



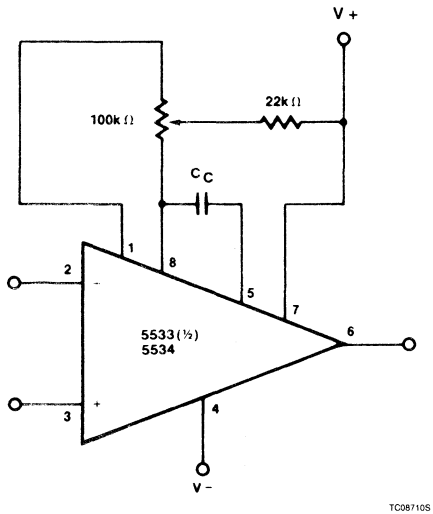
OP05160S

Broadband Input Noise Voltage



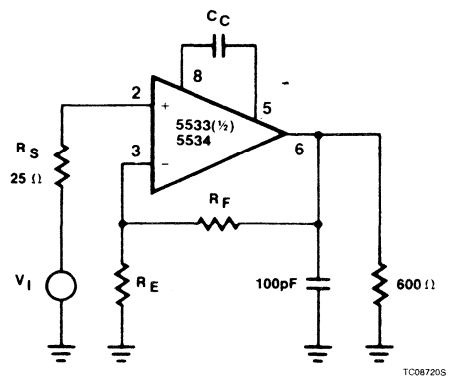
OP05170S

TEST LOAD CIRCUITS



TC08710S

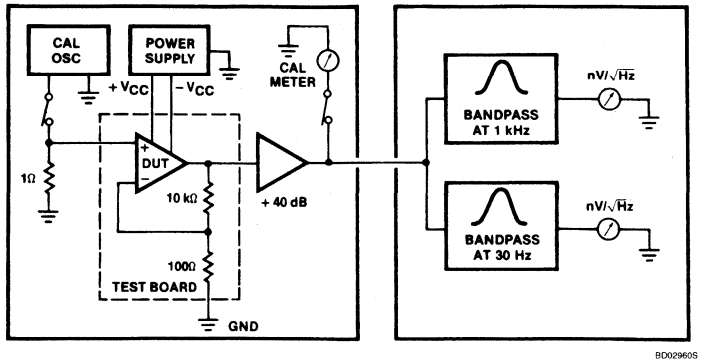
Frequency Compensation and Offset Voltage Adjustment Circuit



TC08720S

Closed-Loop Frequency Response

NOISE TEST BLOCK DIAGRAM



NE/SE5535
Dual High Slew Rate Op Amp

Product Specification

DESCRIPTION

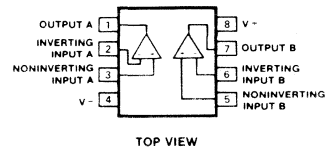
The NE/SE5535 is a new generation operational amplifier featuring high slew rates combined with improved input characteristics. The 5535 is a dual configuration. Internally compensated for unity gain, the SE5535 features a guaranteed unity gain slew rate of 10V/μs with 4mV maximum offset voltage. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 747 and 1558.

FEATURES

- **15V/μs unity gain slew rate**
- **Internal frequency compensation**
- **Low input offset voltage — 2mV**
- **Low input bias current 80nA max**
- **Short-circuit protected**
- **Large common-mode and differential voltage ranges**
- **Pin compatibility** $\frac{5535}{747,1558}$
- **Dual configuration**
- **Low noise current 0.15pA/$\sqrt{\text{Hz}}$ typ.**

PIN CONFIGURATION

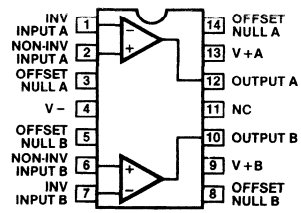
N Package



TOP VIEW

CD10099S

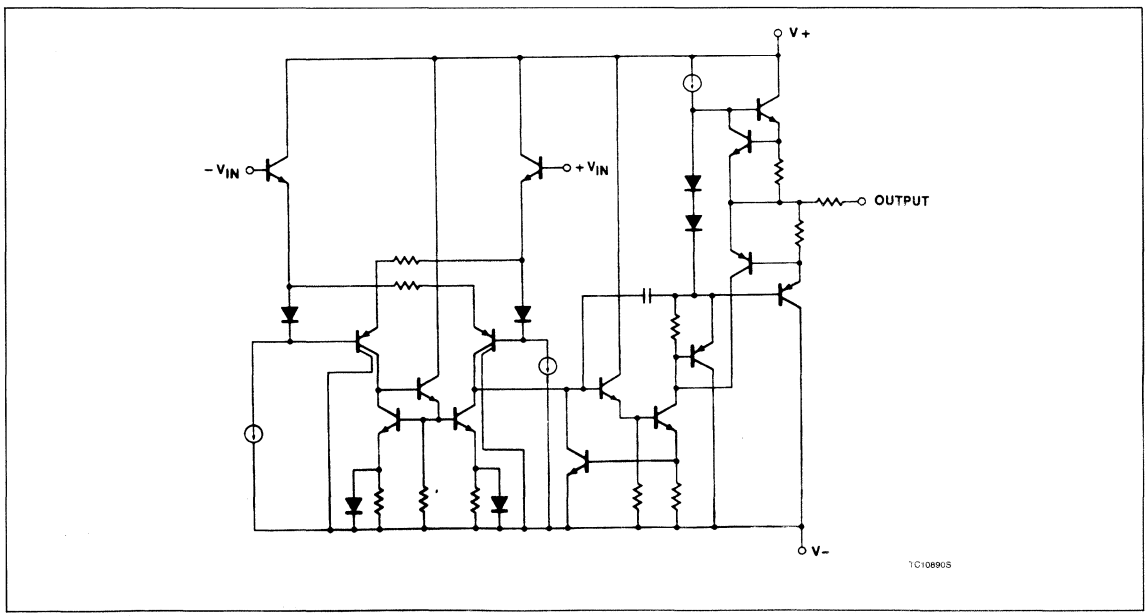
F Package



TOP VIEW

CD13780S

EQUIVALENT SCHEMATIC (one amplifier)



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5535N
8-Pin Plastic DIP	−55°C to +125°C	SE5535N
14-Pin Cerdip	0 to +70°C	NE5535F
14-Pin Cerdip	−55 to +125°C	SE5535F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	SE5535	NE5535	UNIT
V_S	Supply voltage	±22	±18	V
P_D	Internal power dissipation[1] N package F package	 1275 1250	 1275 1250	 mW mW
V_{IN}	Differential input voltage	±30	±30	V
V_{IN}	Input voltage[2]	±15	±15	V
T_A	Operating temperature range	−55 to +125	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	300	°C
I_{SC}	Output short-circuit[3]	Indefinite	Indefinite	

NOTES:

1. Rating applies at $T_A = 25°C$ for thermal resistances junction to ambient of 98°C/W and 100°C/W for N and F packages, respectively. Maximum junction temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.*

SYMBOL	PARAMETER	TEST CONDITIONS	SE5535			NE5535			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$ $R_S \leq 10k\Omega$, over temp.		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
$\Delta V_{OS}/\Delta T$		$R_S = 0\Omega$, over temp.		4.0			6.0		$\mu V/°C$
I_{OS}	Input offset current	 Over temp.		5	20 40		15	40 80	nA nA
$\Delta I_{OS}/\Delta T$		Over temp.		25			40		pA/°C
I_B	Input bias current	 Over temp.		45	80 200		65	150 200	nA nA
$\Delta I_B/\Delta T$		Over temp.		50			80		pA/°C
V_{CM}	Common-mode voltage range		±12	±13		±12	±13		V
CMRR	Common-mode rejection ratio	$R_S \leq 10k\Omega$, over temp.	70	90		70	90		dB
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	$\mu V/V$
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large-signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$ $R_L = 2k\Omega$, $V_{OUT} = \pm 10V$, over temp.	50 25	500		50 25	500		V/mV V/mV
V_{OUT}	Output voltage	$R_L \geq 2k\Omega$, over temp. $R_L \geq 10k\Omega$, over temp.	±10 ±12	±13 ±14		±10 ±12	±13 ±14		V V
I_{CC}	Supply current	Per amplifier Per amplifier, over temp.		1.8 2	2.8 3.3		1.8 2	2.8	mA mA
P_D	Power dissipation	Per amplifier Per amplifier, over temp.		54 60	84 99		54 60	84	mW mW
I_{SC}	Output short-circuit current		10	25	50	10	25	50	mA
R_{OUT}	Output resistance			100			100		Ω

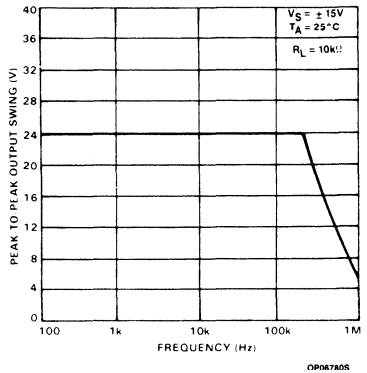
NOTE:
* Temperature range:
SE types $-55°C \leq T_A \leq 125°C$
NE types $0°C \leq T_A \leq 70°C$

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified.

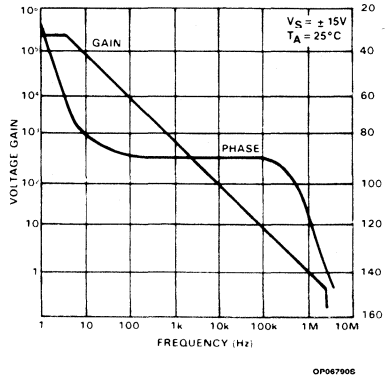
SYMBOL	PARAMETER	TEST CONDITIONS	SE5535			NE5535			UNIT
			Min	Typ	Max	Min	Typ	Max	
GBW	Gain bandwidth product			1			1		MHz
	Transient response								
t_R	Small-signal rise time			0.25			0.25		μs
	Small-signal overshoot			6			6		%
t_S	Settling time	To 0.1%		3			3		μs
SR	Slew rate	$R_L \geq 10k\Omega$, unity gain, non-inverting	10	15		10	15		V/μs
	Input noise voltage	f = 1kHz, $T_A = 25°C$		30			30		$nV/\sqrt{Hz}$

TYPICAL PERFORMANCE CHARACTERISTICS

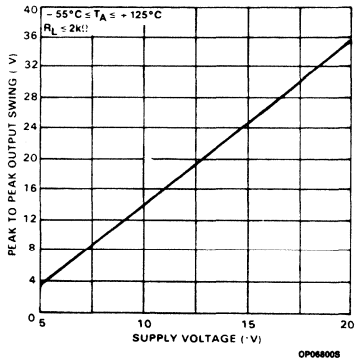
Output Voltage Swing as a Function of Frequency



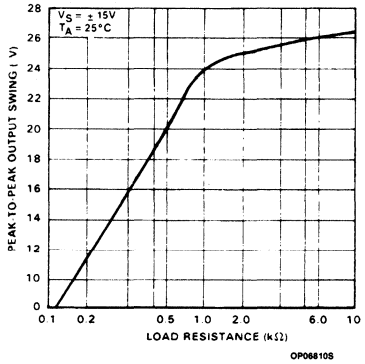
Open-Loop Voltage Gain as a Function of Frequency



Output Voltage Swing as a Function of Supply Voltage

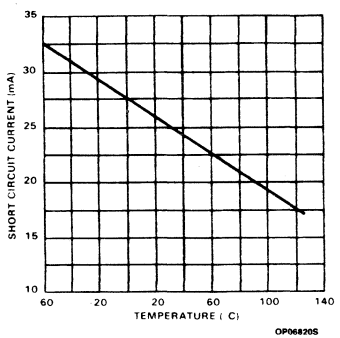


Output Voltage Swing as a Function of Load Resistance

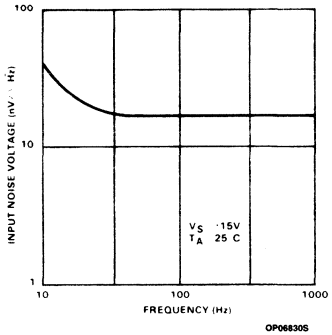


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

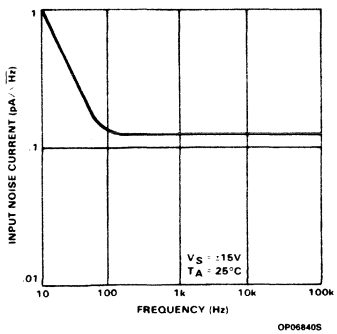
Output Short-Circuit Current as a Function of Ambient Temperature



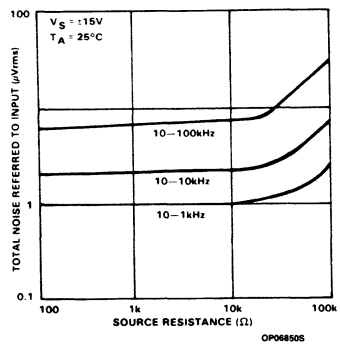
Input Noise Voltage as a Function of Frequency



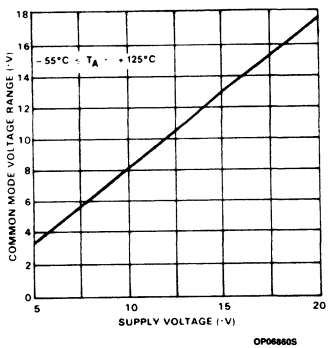
Input Noise Current as a Function of Frequency



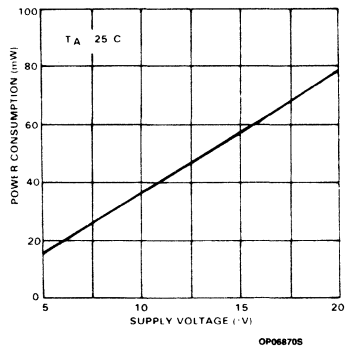
Broadband Noise for Various Bandwidths



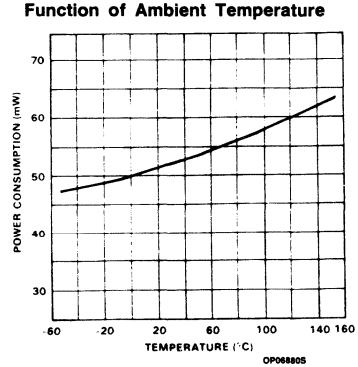
Input Common-Mode Voltage Range as a Function of Supply Voltage



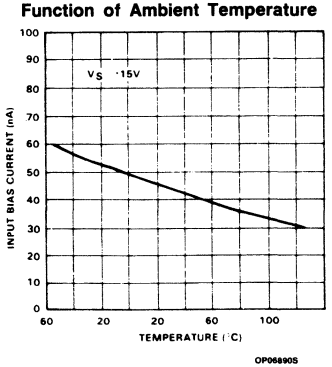
Power Consumption as a Function of Supply Voltage



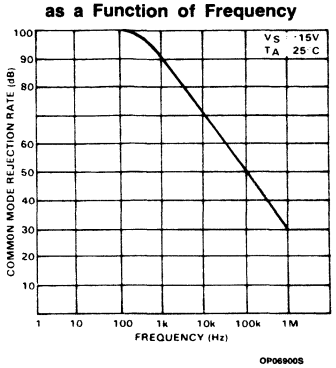
Power Consumption as a Function of Ambient Temperature



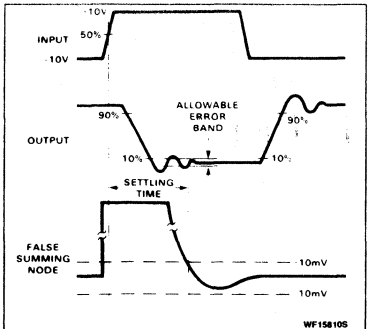
Input Bias Current as a Function of Ambient Temperature



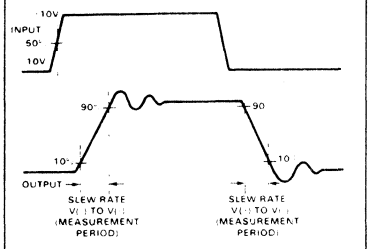
Common-Mode Rejection Ratio as a Function of Frequency



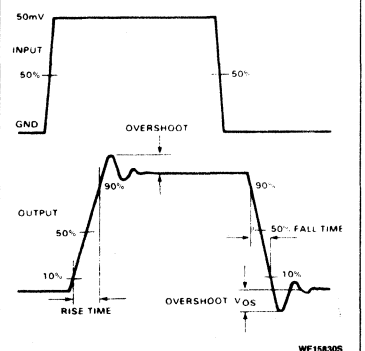
VOLTAGE WAVEFORMS



Settling Time Measurement

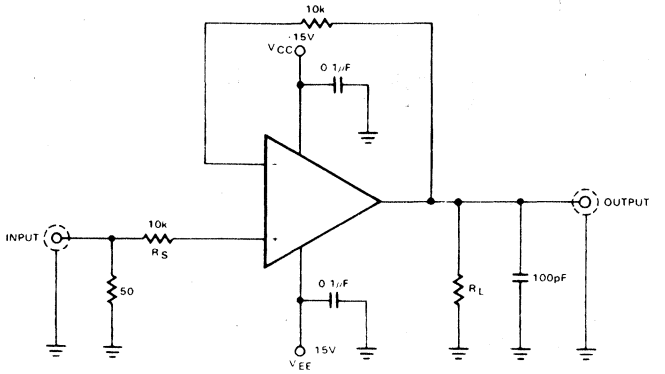


Slew Rate Measurement



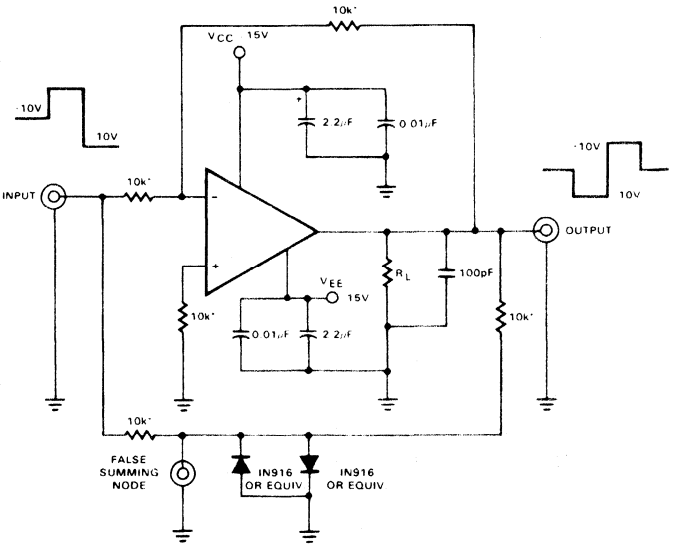
Small-Signal Transient Response Definitions

TEST CIRCUITS



NOTES:
1. Pins not shown are not connected.
2. All resistor values are typical and in ohms.

Slew Rate and Small-Signal Transient Response

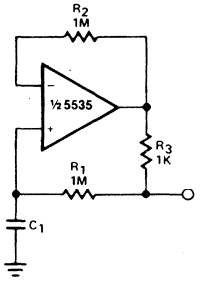


NOTES:
1. Pins not shown are not connected.
2. All resistor values are typical and in ohms.
   *Match to within 0.01%.

Settling Time

INTRODUCTION

The NE5535 is a new generation monolithic op amp which features improved input characteristics. The device is compensated to unity gain and has a minimum guaranteed unity gain slew rate of 10Vμs. This is achieved by employing a clamped super beta input stage which has lower input bias current.



NOTE:
All resistor values are in ohms.

Figure 1. Capacitance Multiplier

APPLICATIONS

These improved parameters can be put to good use in applications such as sample and hold circuits which require low input current and in voltage-follower circuits which require high slew rates. The circuit that follows will yield maximum small-signal transient response and slew rate for the NE5535 at unity gain.

It is always good practice in designing a system to use dual tracking regulators to power the dual-supply op amps. This will guarantee the positive and negative supply voltage will be equal during power-up. With the NE5535, it is possible to degrade the input circuit characteristics by not applying the power supplies simultaneously. The NE5535 is capable of directly replacing the μA741 with higher input resistance which will improve such designs as active filters, sample and hold, as well as voltage-followers.

The NE5535 can be used either with single or split power supplies.

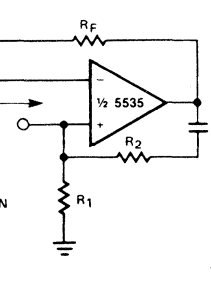


Figure 2. Virtual Inductor

Capacitance Multiplier

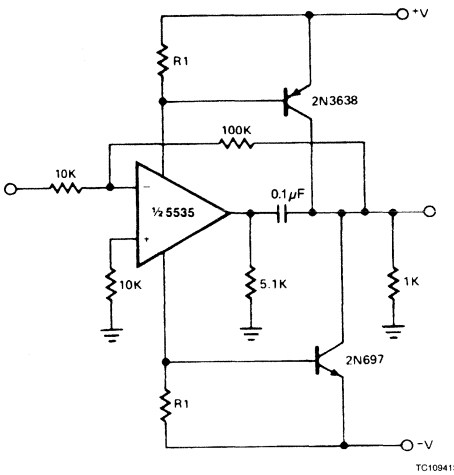
The circuit in Figure 1 can be used to simulate large capacitances using small value components. With the values shown and C = 10μF, an effective capacitance of 10,000μF was obtained. The Q available is limited by the effective series resistance. So R1 should be as large as practical.

Simulated Inductor

With a constant current excitation, the voltage dropped across an inductance increases with frequency. Thus, an active device whose output increases with frequency can be characterized as an inductance. The circuit of Figure 2 yields such a response with the effective inductance being equal to:

$L = R_1R_2C$

The Q of this inductance depends upon R_1 being equal to R_2. At the same time, however, the positive and negative feedback paths of the amplifier are equal leading to the distinct possibility of instability at high frequencies. R_1 should therefore always be slightly smaller than R_2 to assure stable operation.



NOTE:
All resistor values are in ohms.

Figure 3. Power Booster

Power Amplifier

For most applications, the available power from op amps is sufficient. There are times when more power handling capability is necessary. A simple power booster capable of driving moderate loads is offered in Figure 3.

The circuit as shown uses an NE5535 device. Other amplifiers may be substituted only if R_1 values are changed because of the I_{CC} current required by the amplifier. R_1 should be calculated from the expression

$$R_1 = \frac{600mV}{I_{CC}}$$

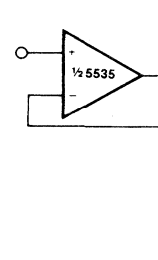
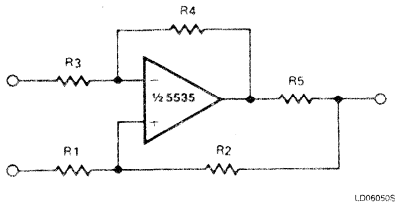


Figure 4. Voltage-to-Current Converter



NOTES:

$$\frac{R_2}{R_1} = \frac{R_4}{R_3}$$

$$I_{OUT} = \frac{V_{IN} \cdot R_2}{R_5 \cdot R_1}$$

Figure 5. Voltage-to-Current Converter

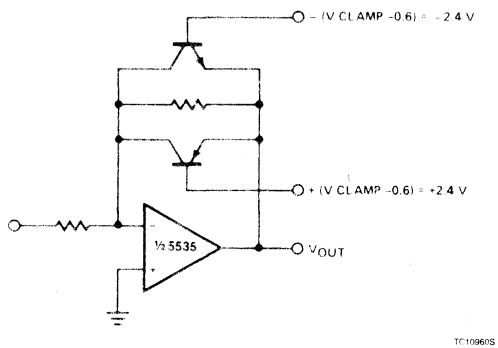
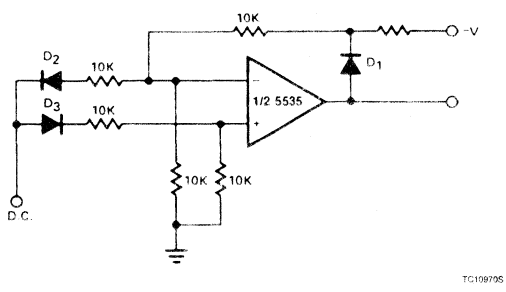


Figure 6. Active Clamp-Limiting Amplifier



NOTE:
All resistor values are in ohms.

Figure 7. Absolute Value Amplifier

Voltage-to-Current Converters

A simple voltage-to-current converter is shown in Figure 4. The current out is $I_{OUT} \cong V_{IN}/R$. For negative currents, a PNP can be used and, for better accuracy, a Darlington pair can be substituted for the transistor. With careful design, this circuit can be used to control currents of many amps. Unity gain compensation is necessary.

The circuit in Figure 5 has a different input and will produce either polarity of output current. The main disadvantages are the error current flowing in R_2 and the limited current available.

Active Clamp-Limiting Amplifier

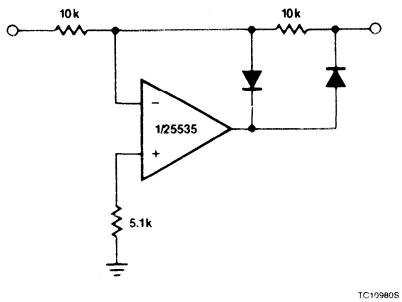
The modified inverting amplifier in Figure 6 uses an active clamp to limit the output swing with precision. Allowance must be made for the V_{BE} of the transistors. The swing is limited by the base-emitter breakdown of the transistors. A simple circuit uses two back-to-back zener diodes across the feedback resistor, but tends to give less precise limiting and cannot be easily controlled.

Absolute Value Amplifier

The circuit in Figure 7 generates a positive output voltage for either polarity of input. For positive signals, it acts as a noninverting amplifier and for negative signals, as an inverting amplifier. The accuracy is poor for input voltages under 1V, but for less stringent applications, it can be effective.

Half-Wave Rectifier

Figure 8 provides a circuit for accurate half-wave rectification of the incoming signal. For positive signals, the gain is 0; for negative signals, the gain is −1. By reversing both diodes, the polarity can be inverted. This circuit provides an accurate output, but the output impedance differs for the two input polarities and buffering may be needed. The output must slew through two diode drops when the input polarity reverses. The NE5535 device will work up to 10kHz with less than 5% distortion.



NOTE:
All resistor values are in ohms.

Figure 8. Half-Wave Rectifier

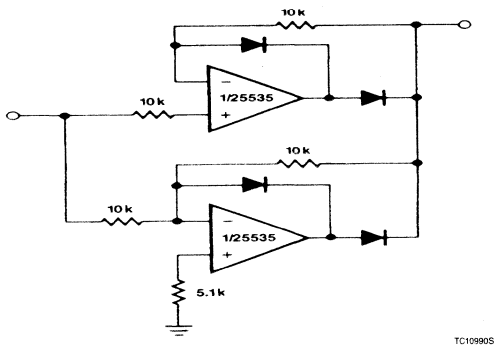
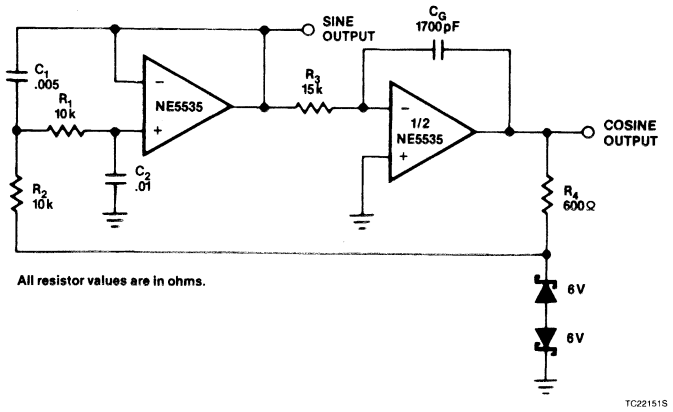


Figure 9. Precision Full-Wave Rectifier



NOTE:
All resistor values are in ohms.

Figure 10. Two-Phase Sine Wave Oscillator

Precision Full-Wave Rectifier

The circuit in Figure 9 provides accurate full-wave rectification. The output impedance is low for both input polarities, and the errors are small at all signal levels. Note that the output will not sink heavy currents, except a small amount through the 10kΩ resistors. Therefore, the load applied should be referenced to ground or a negative voltage. Reversal of all diode polarities will reverse the polarity of the output. Since the outputs of the amplifiers must slew through two diode drops when the input polarity changes, 741 type devices give 5% distortion at about 300Hz.

Two-Phase Sine Wave Oscillator

The circuit (refer to Figure 10) uses a 2-pole pass Butterworth, followed by a phase-shifting single-pole stage, fed back through a voltage limiter to achieve sine and cosine outputs. The values shown using the μA741 amplifiers give about 1.5% distortion at the sine output and about 3% distortion at the cosine output. By careful trimming of C_G and/or the limiting network, better distortion figures are possible. The component values shown give a frequency of oscillation of about 2kHz. The values can be readily selected for other frequencies. The NE5535 should be used at higher frequencies to reduce distortion due to slew limiting.

μA741/μA741C/SA741C General Purpose Operational Amplifier

Product Specification

DESCRIPTION

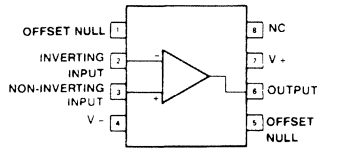
The μA741 is a high performance operational amplifier with high open-loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit-protected and allows for nulling of offset voltage.

FEATURES

- **Internal frequency compensation**
- **Short circuit protection**
- **Excellent temperature stability**
- **High input voltage range**

PIN CONFIGURATION

D, F, N Packages



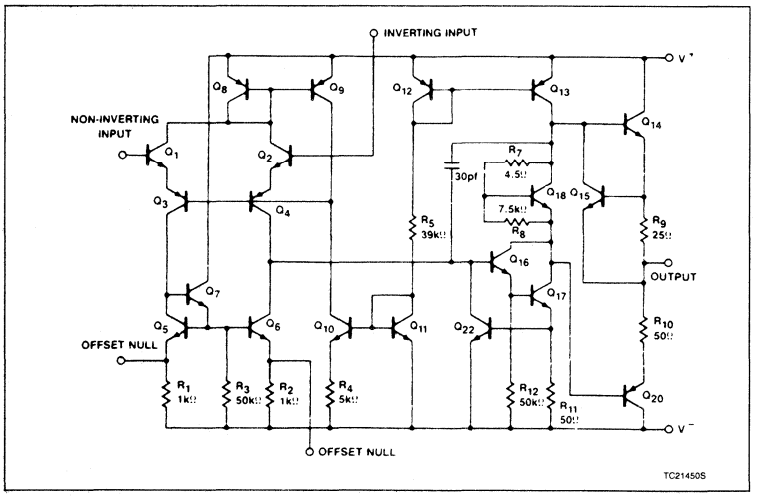
TOP VIEW

CD10181S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	−55°C to +125°C	μA741N
8-Pin Plastic DIP	0 to +70°C	μA741CN
8-Pin Plastic DIP	−40°C to +85°C	SA741CN
8-Pin Cerdip	−55°C to +125°C	μA741F
8-Pin Cerdip	0 to +70°C	μA741CF
8-Pin SO	0 to +70°C	μA741CD

EQUIVALENT SCHEMATIC



TC21450S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage μA741C μA741	 ±18 ±22	 V V
P_D	Internal power dissipation D package N package F package	 780 1170 800	 mW mW mW
V_{IN}	Differential input voltage	±30	V
V_{IN}	Input voltage[1]	±15	V
I_{SC}	Output short-circuit duration	Continuous	
T_A	Operating temperature range μA741C SA741C μA741	 0 to +70 −40 to +85 −55 to +125	 °C °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS (μA741, μA741C) $T_A = 25°C$, $V_S = ±15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	μA741			μA741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		1.0	5.0		2.0	6.0	mV
		$R_S = 10k\Omega$, over temp.		1.0	6.0			7.5	mV
$\Delta V_{OS}/\Delta T$				10			10		μV/°C
I_{OS}	Offset current			20	200		20	200	nA
		Over temp.						300	nA
		$T_A = +125°C$		7.0	200				nA
		$T_A = -55°C$		20	500				nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temp.						800	nA
		$T_A = +125°C$		30	500				nA
		$T_A = -55°C$		300	1500				nA
$\Delta I_B/\Delta T$				1			1		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$	±12	±14		±12	±14		V
		$R_L = 2k\Omega$, over temp.	±10	±13		±10	±13		V
A_{VOL}	Large-signal voltage gain	$R_L = 2k\Omega$, $V_O = ±10V$	50	200		20	200		V/mV
		$R_L = 2k\Omega$, $V_O = ±10V$, over temp.	25			15			V/mV
	Offset voltage adjustment range			±30			±30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$					10	150	μV/V
		$R_S \leq 10k\Omega$, over temp.		10	150				μV/V
CMRR	Common-mode rejection ratio					70	90		dB
		Over temp.	70	90					dB
I_{CC}	Supply current			1.4	2.8		1.4	2.8	mA
		$T_A = +125°C$		1.5	2.5				mA
		$T_A = -55°C$		2.0	3.3				mA

DC ELECTRICAL CHARACTERISTICS (Continued) (μA741, μA741C) $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	μA741			μA741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN} R_{IN}	Input voltage range Input resistance	(μA741, over temp.)	± 12 0.3	± 13 2.0		± 12 0.3	± 13 2.0		V MΩ
P_D	Power consumption	$T_A = +125°C$ $T_A = -55°C$		50 45 45	85 75 100		50	85	mW mW mW
R_{OUT}	Output resistance			75			75		Ω
I_{SC}	Output short-circuit current		10	25	60	10	25	60	mA

DC ELECTRICAL CHARACTERISTICS (SA741C) $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

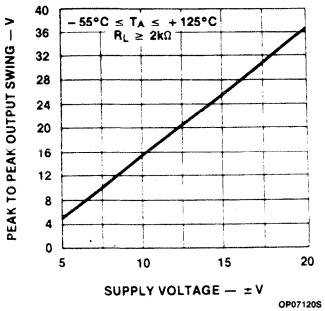
SYMBOL	PARAMETER	TEST CONDITIONS	SA741C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		2.0	6.0	mV
		$R_S = 10k\Omega$, over temp.			7.5	mV
$\Delta V_{OS}/\Delta T$				10		μV/°C
I_{OS}	Offset current	Over temp.		20	200	nA
					500	nA
$\Delta I_{OS}/\Delta T$				200		pA/°C
I_{BIAS}	Input bias current	Over temp.		80	500	nA
					1500	nA
$\Delta I_B/\Delta T$				1		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$	± 12	± 14		V
		$R_L = 2k\Omega$, over temp.	± 10	± 13		V
A_{VOL}	Large-signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	20	200		V/mV
		$R_L = 2k\Omega$, $V_O = \pm 10V$, over temp.	15			V/mV
	Offset voltage adjustment range			± 30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		10	150	μV/V
CMRR	Common mode rejection ration		70	90		dB
V_{IN}	Input voltage range	Over temp.	± 12	± 13		V
R_{IN}	Input resistance		0.3	2.0		MΩ
P_d	Power consumption			50	85	mW
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current			25		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

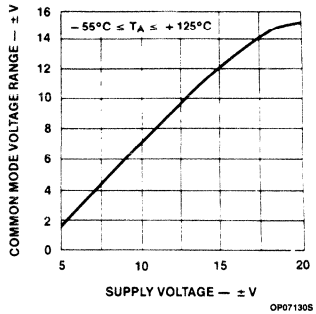
SYMBOL	PARAMETER	TEST CONDITIONS	μA741, μA741C			UNIT
			Min	Typ	Max	
R_{IN}	Parallel input resistance	Open-loop, f = 20Hz	0.3			MΩ
C_{IN}	Parallel input capacitance	Open-loop, f = 20Hz		1.4		pF
	Unity gain crossover frequency	Open-loop		1.0		MHz
	Transient response unity gain	$V_{IN} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$				
t_R	Rise time			0.3		μs
	Overshoot			5.0		%
SR	Slew rate	$C \leq 100pF$, $R_L \geq 2k\Omega$, $V_{IN} = \pm 10V$		0.5		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

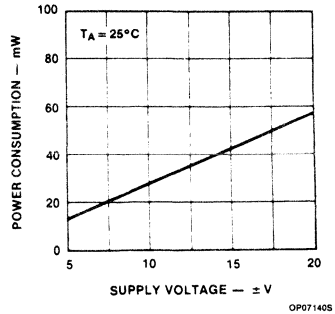
Output Voltage Swing as a Function of Supply Voltage



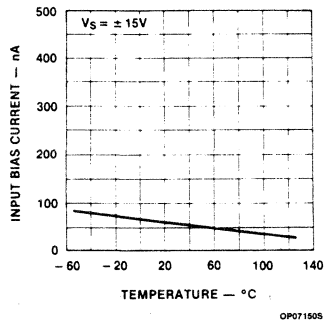
Input Common-Mode Voltage Range as a Function of Supply Voltage



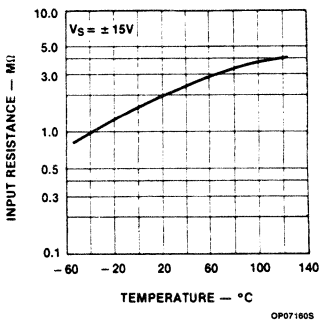
Power Consumption as a Function of Supply Voltage



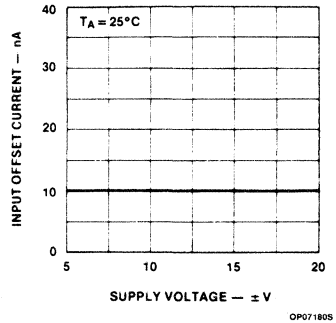
Input Bias Current as a Function of Ambient Temperature



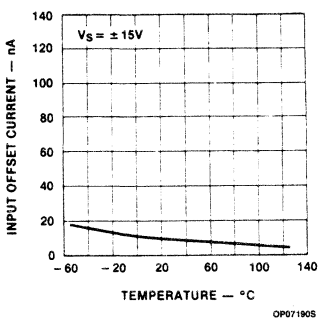
Input Resistance as a Function of Ambient Temperature



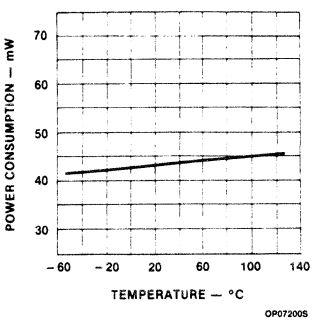
Input Offset Current as a Function of Supply Voltage



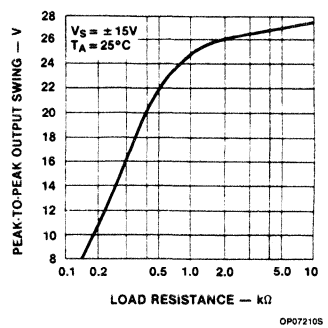
Input Offset Current as a Function of Ambient Temperature



Power Consumption as a Function of Ambient Temperature

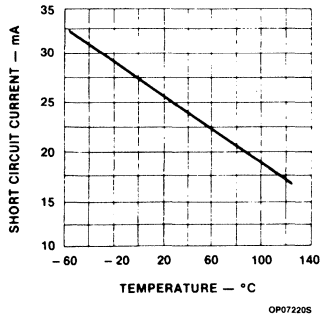


Output Voltage Swing as a Function of Load Resistance

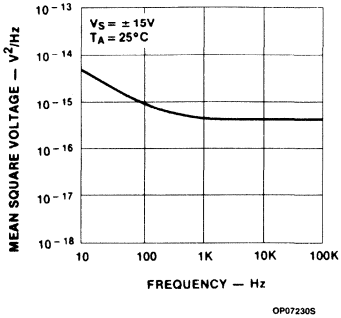


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

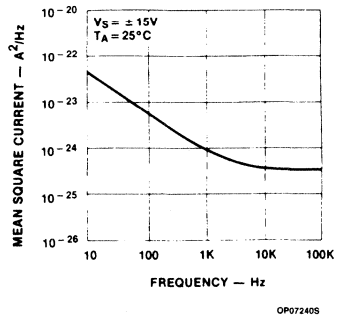
Output Short-Circuit Current as a Function of Ambient Temperature



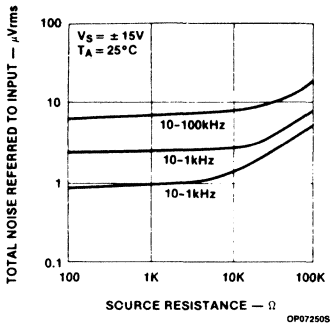
Input Noise Voltage as a Function of Frequency



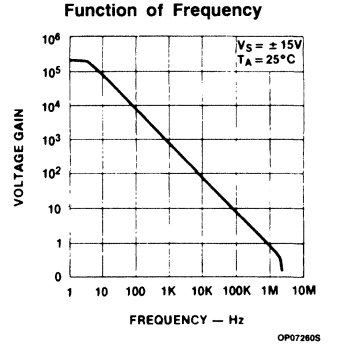
Input Noise Current as a Function of Frequency



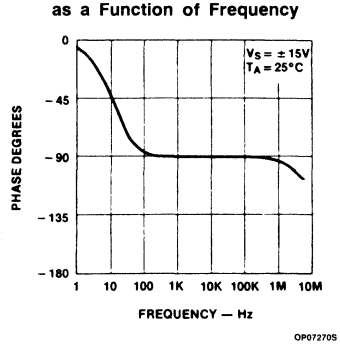
Broadband Noise for Various Bandwidths



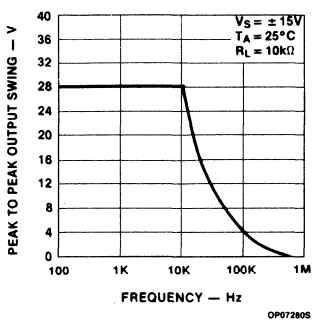
Open-Loop Voltage Gain as a Function of Frequency



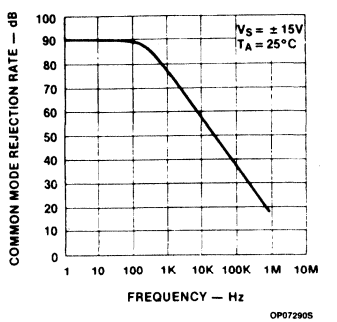
Open-Loop Phase Response as a Function of Frequency



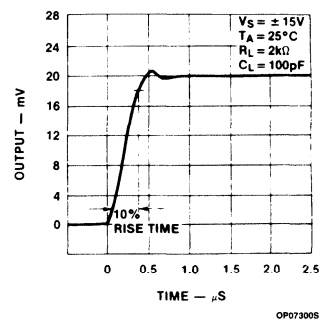
Output Voltage Swing as a Function of Frequency



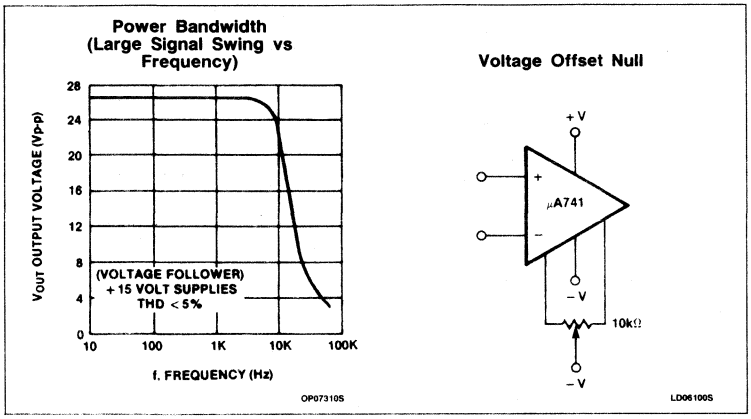
Common-Mode Rejection Ratio as a Function of Frequency



Transient Response



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



μA747/747C/SA747C
Dual Operational Amplifier

Product Specification

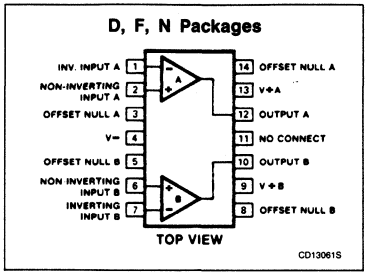
DESCRIPTION

The 747 is a pair of high-performance monolithic operational amplifiers constructed on a single silicon chip. High common-mode voltage range and absence of "latch-up" make the 747 ideal for use as a voltage-follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The 747 is short-circuit protected and requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed-loop applications. For single amplifier performance, see μA741 data sheet.

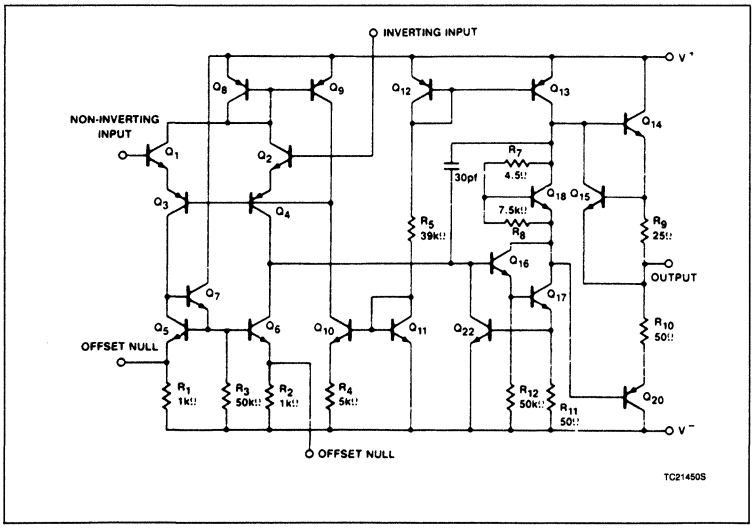
FEATURES

- **No frequency compensation required**
- **Short-circuit protection**
- **Offset voltage null capability**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**
- **No latch-up**

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	−55°C to +125°C	μA747N
14-Pin Plastic DIP	0 to +70°C	μA747CN
14-Pin Plastic DIP	−45°C to +85°C	SA747CN
14-Pin Cerdip	−55°C to +125°C	μA747F
14-Pin Cerdip	0 to +70°C	μA747CF
14-Pin SO	0 to +70°C	μA747CD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage μA747 μA747C SA747C	 ±22 ±18 ±18	 V V V
$P_{D\ MAX}$	Maximum power dissipation T_A = 25°C (still air)[1] D package F package N package	 1000 1200 1500	 mW mW mW
V_{IN}	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
	Voltage between offset null and V−	±0.5	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating temperature range μA747 μA747C SA747C	 −55 to +125 0 to +70 −40 to +85	 °C °C °C
T_{SOLD}	Lead temperature (soldering, 10sec)	 300	 °C
I_{SC}	Output short-circuit duration	Indefinite	

NOTES:
1. Derate above 25°C at the following rates:
   D package at 8.3mW/°C
   F package at 9.7mW/°C
   N package at 12mW/°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS (μA747, μ747C) $T_A = 25°C$, $V_{CC} = \pm 15V$ unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	μA747			μA747C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$ $R_S \leq 10k\Omega$, over temp.		2.0 3.0	5.0 6.0		2.0 3.0	6.0 7.5	mV mV
$\Delta V_{OS}/\Delta T$				10			10		μV/°C
I_{OS}	Offset current	 $T_A = +125°C$ $T_A = -55°C$ Over temperature		20 7.0 85	200 200 500		20 7.0	200 300	nA nA nA nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_{BIAS}	Input current	 $T_A = +125°C$ $T_A = -55°C$ Over temperature		80 30 300	500 500 1500		80 30	500 800	nA nA nA nA
$\Delta I_B/\Delta T$				1			1		nA/°C
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temp. $R_L \geq 10k\Omega$, over temp.	±10 ±12	±13 ±14		±10 ±12	±13 ±14		V V
I_{CC}	Supply current each side	 $T_A = +125°C$ $T_A = -55°C$ Over temperature		1.7 1.5 2.0	2.8 2.5 3.3		1.7 2.0	2.8 3.3	mA mA mA mA
P_d	Power consumption	 $T_A = +125°C$ $T_A = -55°C$ Over temperature		50 45 60	85 75 100		50 60	85 100	mW mW mW mW
C_{IN}	Input capacitance			1.4			1.4		pF
	Offset voltage adjustment range			±15			±15		mV
R_{OUT}	Output resistance			75			75		Ω
	Channel separation			120			120		dB
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	μV/V
A_{VOL}	Large-signal voltage gain (DC)	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$ Over temperature	50,000 25,000			25,000 15,000			V/V V/V
CMRR	Common-mode rejection ratio	$R_S \leq 10k\Omega$, $V_{CM} = \pm 12V$ Over temperature	70			70			dB

DC ELECTRICAL CHARACTERISTICS (SA747C) $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

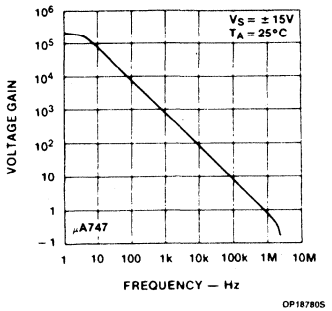
SYMBOL	PARAMETER	TEST CONDITIONS	SA747C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10\Omega$ $R \leq 10k\Omega$, over temperature		2.0 3.0	6.0 7.5	mV mV
$\Delta V_{OS}/\Delta T$				10		μV/°C
I_{OS}	Offset current	Over temperature		20	200 500	mA mA
$\Delta I_{OS}/\Delta T$				300		pA/°C
I_{BIAS}	Input bias current	Over temperature		80	500 1500	mA mA
$\Delta I_B/\Delta T$				1		mA/°C
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temperature $R_L \geq 10k\Omega$, over temperature	±10 ±12	±13 ±14		V V
I_{CC}	Supply current, each side	Over temperature		1.7 2.0	2.8 3.3	mA mA
P_d	Power consumption	Over temperature		50 60	85 100	mW mW
C_{IN}	Input capacitance			1.4		pF
	Offset voltage adjustment range			±15		mV
R_{OUT}	Output resistance			75		Ω
	Channel separation			120		dB
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temperature		30	150	μV/V
A_{VOL}	Large signal voltage gain (DC)	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	25,000			V/V
CMRR	Common-mode rejection ratio	$R_S \leq 10k\Omega$, $V_{CM} = \pm 12V$ Over temperature	70			dB
I_{SC}	Output short-circuit current		10	25	60	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

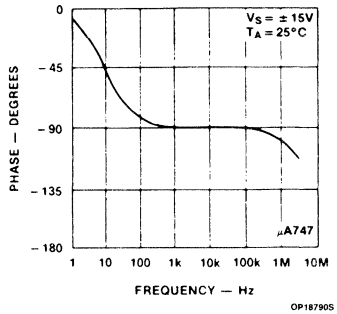
SYMBOL	PARAMETER	TEST CONDITIONS	μA747/μA747C/SA747C			UNIT
			Min	Typ	Max	
t_R	Transient response Rise time Overshoot	$V_{IN} = 20mV$, $R_L = 2k\Omega$, $C_L < 100pF$ Unity gain $C_L \leq 100pF$ Unity gain $C_L \leq 100pF$		 0.3 5.0		 μs %
SR	Slew rate	$R_L > 2k\Omega$		0.5		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

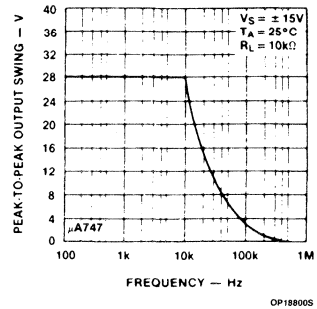
Open-Loop Voltage Gain as a Function of Frequency



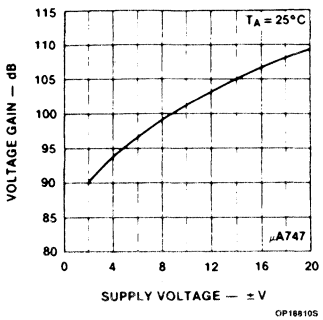
Open-Loop Phase Response as a Function of Frequency



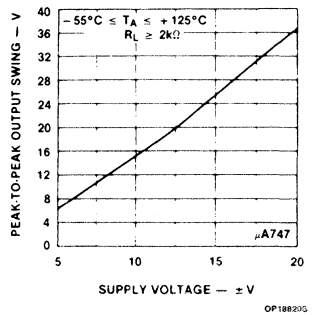
Output Voltage Swing as a Function of Frequency



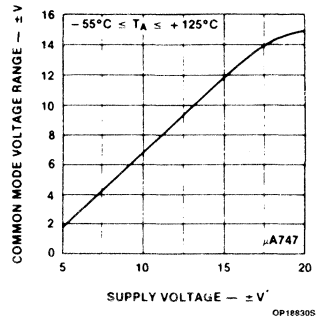
Open-Loop Voltage Gain as a Function of Supply Voltage



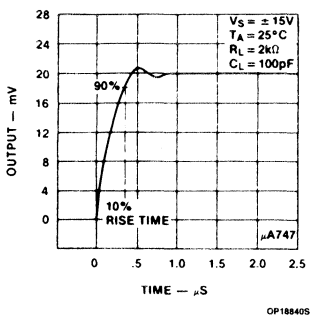
Output Voltage Swing as a Function of Supply Voltage



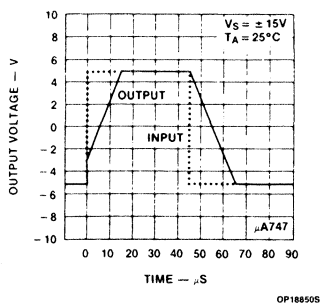
Input Common-Mode Voltage Range as a Function of Supply Voltage



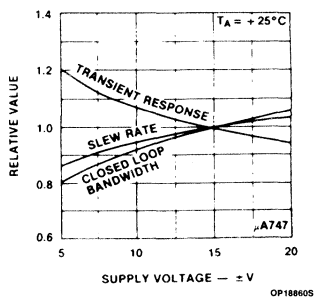
Transient Response



Voltage-Follower Large-Signal Pulse Response

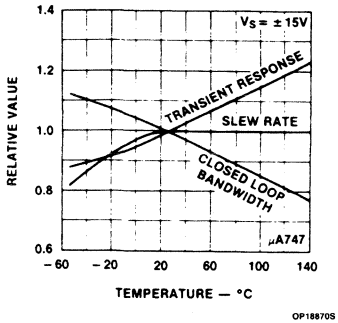


Frequency Characteristics as a Function of Supply Voltage



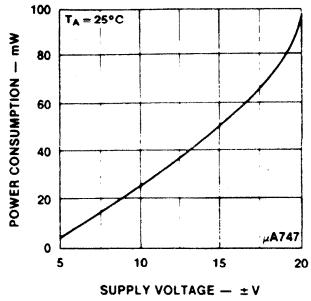
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Frequency Characteristics as a Function of Ambient Temperature



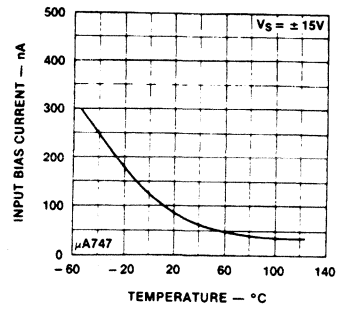
OP18870S

Power Consumption as a Function of Supply Voltage



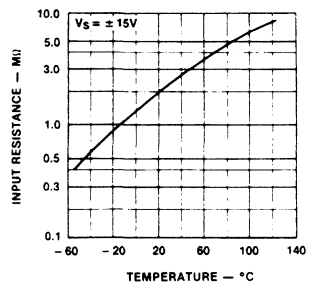
OP18880S

Input Bias Current as a Function of Ambient Temperature



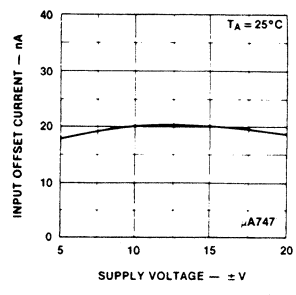
OP18890S

Input Resistance as a Function of Ambient Temperature



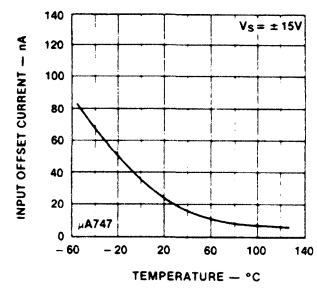
OP18900S

Input Offset Current as a Function of Supply Voltage



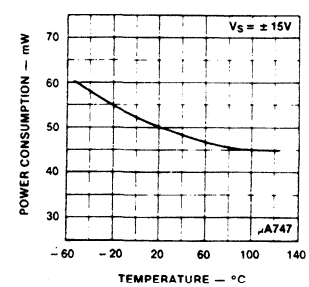
OP18910S

Input Offset Current as a Function of Ambient Temperature



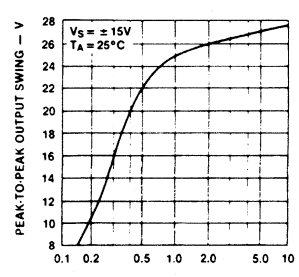
OP18920S

Power Consumption as a Function of Ambient Temperature



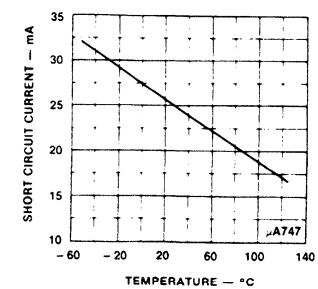
OP18930S

Output Voltage Swing as a Function of Load Resistance



OP18940S

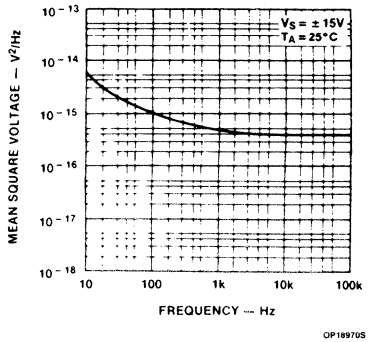
Output Short-Circuit Current as a Function of Ambient Temperature



OP18950S

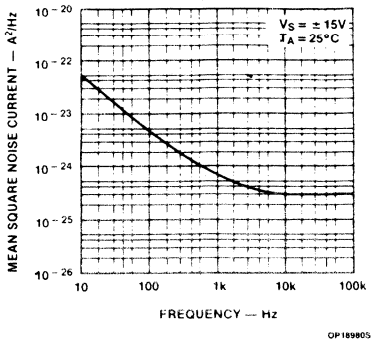
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Input Noise Voltage as a Function of Frequency



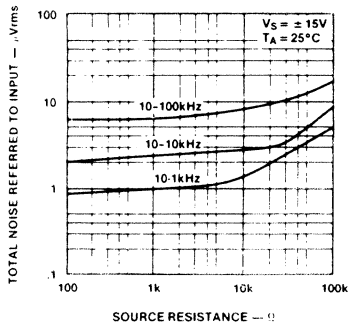
OP18970S

Input Noise Current as a Function of Frequency



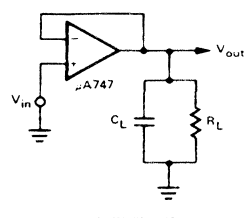
OP18980S

Broadband Noise for Various Bandwidths



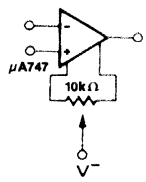
OP18990S

TEST CIRCUITS



sfc1030>TC21460S

Transient Response Test Circuit



TC21471S

Voltage Offset Null Circuit

OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The TCA520 is a bipolar integrated operational amplifier primarily intended for low-power, low-voltage applications and as a comparator in digital systems.

Features

- Wide supply voltage range
- Low supply voltage operation
- Low power consumption
- Low input bias current
- Offset compensation facility
- Frequency compensation facility
- High slew rate
- Large output voltage swing
- TTL compatible output

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		2 to 20	V
Supply current	I_{CC}	typ.	0,8	mA
Input bias current	I_{IB}	typ.	60	nA
Output voltage range	V_O		0,1 to V_{CC}–0,1	V
D.C. differential voltage amplification	A_{VD}	typ.	15 000	
Slew rate	S_{VOAV}	typ.	25	V/μs
Operating ambient temperature range	T_{amb}		–25 to + 85	°C

PACKAGE OUTLINES

TCA520B : 8-lead DIL; plastic (SOT97).
TCA520D: 8-lead mini-pack; plastic (SO8; SOT96A).

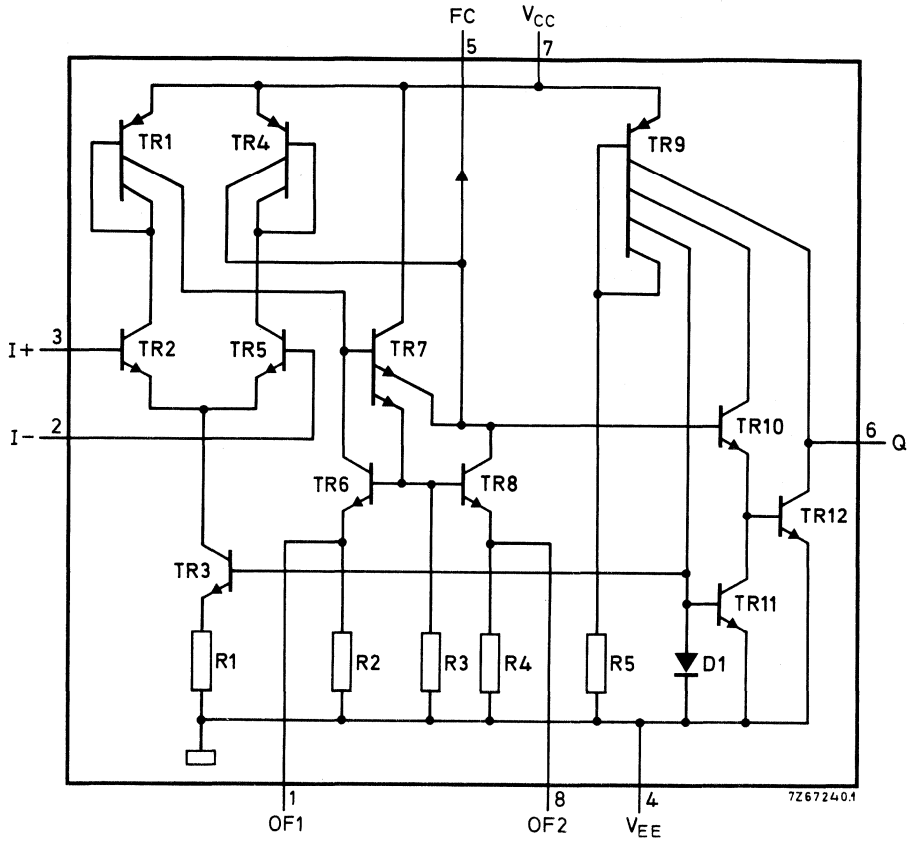


Fig. 1 Circuit diagram.

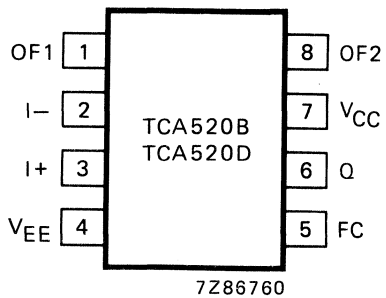


Fig. 2 Pinning diagram.

PINNING

1	OF1	offset compensation connection
2	I−	inverting input
3	I+	non-inverting input
4	V_{EE}	ground connection
5	FC	frequency compensation connection
6	Q	output
7	V_{CC}	positive supply connection
8	OF2	offset compensation connection

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC}	max.	22	V
Input voltage	V_I	max.	V_{CC}	V
	$-V_I$	max.	0	V
Differential input voltage	$\pm V_{ID}$	max.	2	V
Power dissipation at T_{amb} = 85 °C	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−55 to + 125		°C
Operating ambient temperature range	T_{amb}	−25 to + 85		°C

CHARACTERISTICS

V_{CC} = 5 V; V_{EE} = 0 V; T_{amb} = 25 °C; R_L from Q to V_{CC} unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC}; pin 7					
Supply current, unloaded	I_{CC}	0,5	0,8	1,2	mA
Inputs I+ and I−; pins 3 and 2					
Input voltage	V_I	0,9	–	V_{CC}−0,5	V
Input bias current	I_{IB}	–	60	250	nA
Input offset voltage	V_{IO}	–	1	6	mV
Variation with temperature	ΔV_{IO}	–	5	–	μV/K
Input offset current	I_{IO}	–	10	75	nA
Common-mode rejection ratio	k_{CMR}	70	100	–	dB
Input noise voltage at f = 1 kHz	$V_{n(rms)}$	–	15	–	$nV/\sqrt{Hz}$
Input noise current at f = 1 kHz	$I_{n(rms)}$	–	0,4	–	$pA/\sqrt{Hz}$
Input noise angular frequency	f_c	–	300	–	Hz
Output Q; pin 6					
Output voltage range at R_L = 5 kΩ	V_Q	0,1	–	V_{CC}−0,1	V
Output current					
HIGH at $V_Q = V_{CC} - 0,4$ V	$-I_{OH}$	100	200	–	μA
LOW at V_Q = 0,4 V	I_{OL}	6	12	–	mA
D.C. voltage amplification at R_L = 5 kΩ	A_{VD}	10 000	15 000	–	
A.C. voltage amplification at f = 1 kHz; C_{FC} = 100 pF	A_{vd}	–	58	–	dB
Slew rate (average rate of change of the output voltage) at R_L = 1 kΩ					
C_{FC} = 0 pF	S_{VOAV}	–	25	–	V/μs
C_{FC} = 100 pF	S_{VOAV}	–	500	–	mV/μs

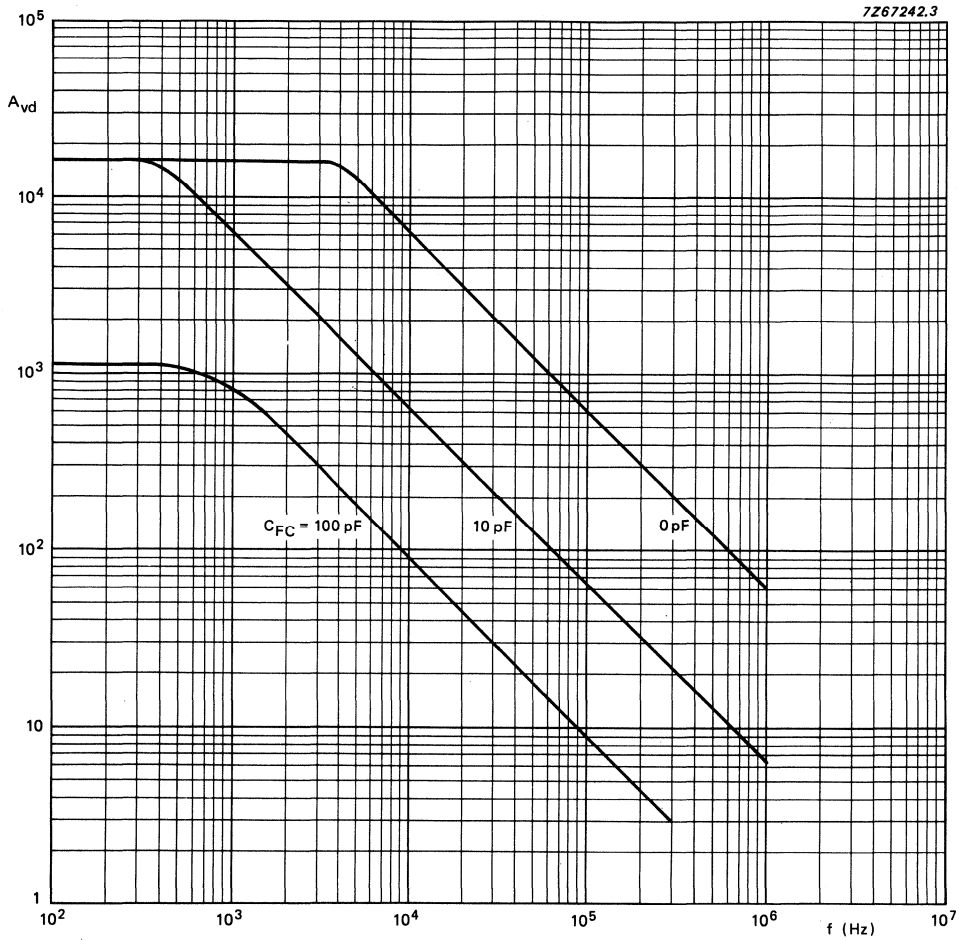


Fig. 3 Typical values of the open-loop voltage amplification as a function of frequency.

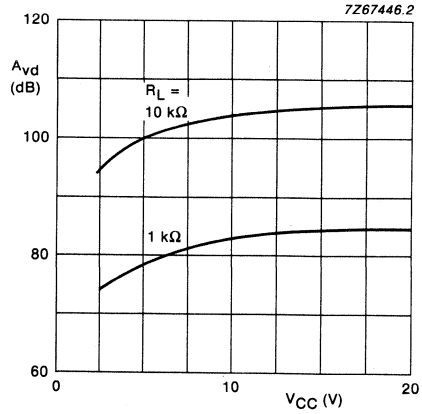


Fig. 4 Typical values of the open-loop voltage amplification as a function of supply voltage.

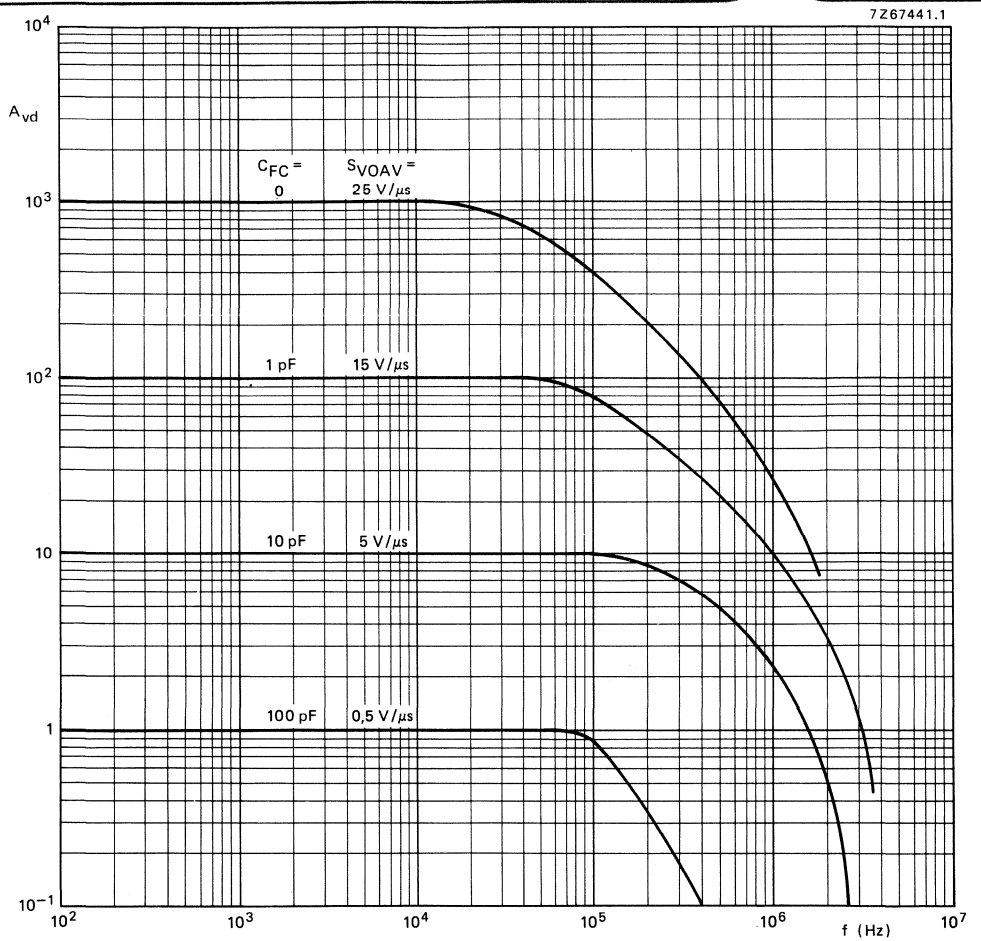


Fig. 5 Typical frequency response and slew rate for various closed-loop gains.

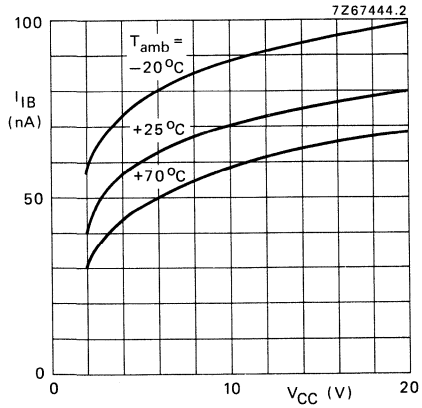


Fig. 6 Typical values of the input bias current as a function of supply voltage, with ambient temperature as a parameter.

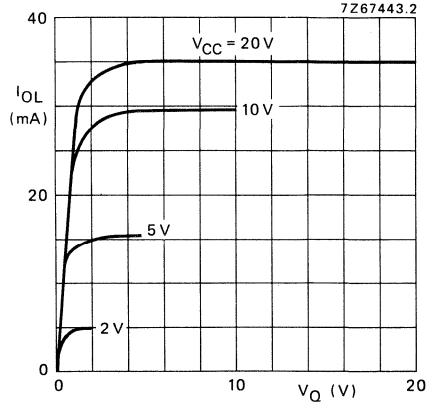


Fig.7 Typical output current LOW as a function of output voltage, with supply voltage as a parameter.

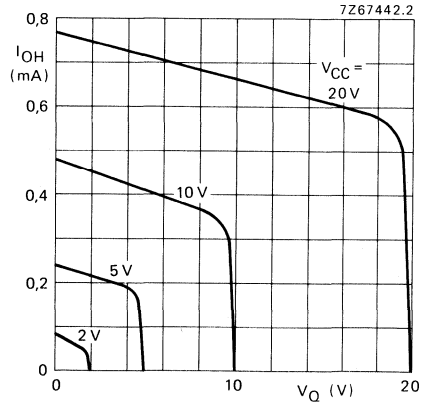


Fig.8 Typical output current HIGH as a function of ouput voltage, with supply voltage as a parameter.

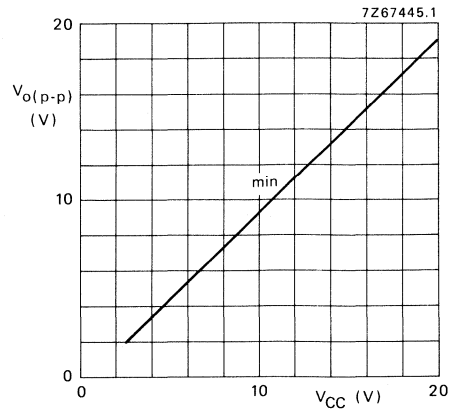


Fig. 9 Minimum values of the output voltage swing as a function of supply voltage for R_L = 1 kΩ.

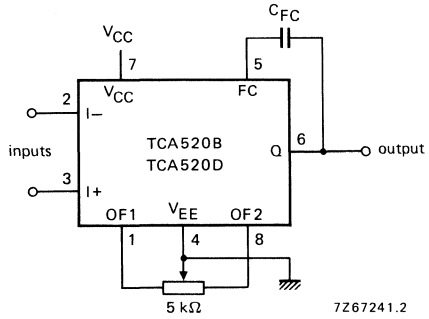


Fig. 10 Typical arrangement of the TCA520 with frequency and offset compensation.

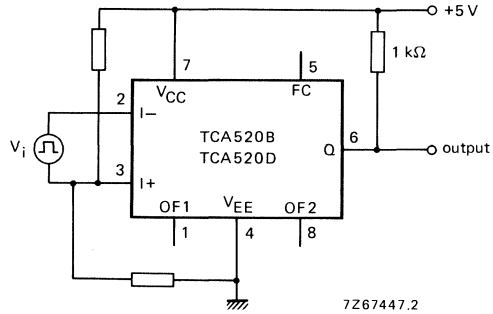


Fig. 11 Typical application of the TCA520 as a comparator; $|V_{2\text{-}3}|$ maximum 2 V.

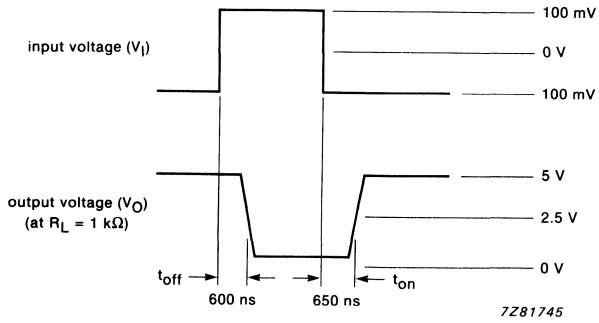


Fig. 12 Typical propagation delay time.

AN142
Audio Circuits Using the NE5532/33/34

Application Note

AUDIO CIRCUITS USING THE NE5532/33/34

The following will explain some of Signetics' low noise op amps and show their use in some audio applications.

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally-compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise voltage specifications.

APPLICATIONS

The Signetics 5532 High-Performance Op Amp is an ideal amplifier for use in high quality and professional audio equipment which requires low noise and low distortion.

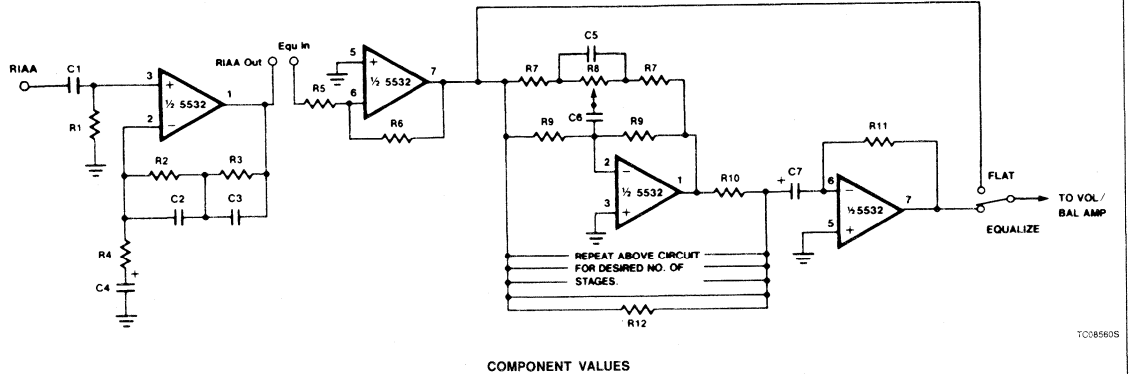
The circuit included in this application note has been assembled on a PC board, and tested with actual audio input devices (Tuner and Turntable). It consists of an RIAA (Recording Industry Association of America) preamp, input buffer, 5-band equalizer, and mixer. Although the circuit design is not new, its performance using the 5532 has been improved.

The RIAA preamp section is a standard compensation configuration with low frequency boost provided by the Magnetic cartridge and the RC network in the op amp feedback loop. Cartridge loading is accomplished via R1. 47k was chosen as a typical value, and may differ from cartridge to cartridge.

The Equalizer section consists of an input buffer, 5 active variable band pass/notch (depending on R9's setting) filters, and an output summing amplifier. The input buffer is a standard unity gain design providing impedance matching between the preamplifier and the equalizer section. Because the 5532 is internally-compensated, no external compensation is required. The 5-band active filter section is actually five individual active filters with the same feedback design for all five. The main difference in all five stages is the values of C5 and C6, which are responsible for setting the center frequency of each stage. Linear pots are recommended for R9. To simplify use of this circuit, a component value table is provided, which lists center frequencies and their associated capacitor values. Notice that C5 equals (10) C6, and that the Value of R8 and R10 are related to R9 by a factor of 10 as well. The values listed in the table are common and easily found standard values.

RIAA EQUALIZATION AUDIO PREAMPLIFIER USING NE5532A

With the onset of new recording techniques with sophisticated playback equipment, a new breed of low noise operational amplifiers was developed to complement the state-of-the-art in audio reproduction. The first ultra-low noise op amp introduced by Signetics was called the NE5534A. This is a single operational amplifier with less than $4nV/\sqrt{Hz}$ input noise voltage. The NE5534A is internally-compensated at a gain of three. This device has been used in many audio preamp and equalizer (active filter) applications since its introduction early last year.



COMPONENT VALUES

R1	1meg	C1	0.22μF	R5	100k	C5	SEE TABLE
R2	100k	C2	750pF	R6	100k	C6	SEE TABLE
R3	1meg	C3	0.0033μF	R7	SEE TABLE	C7	2.2μF
R4	1.1k	C4	33μF	R8	(pot) SEE TABLE		

R9	SEE TABLE
R10	100k
R11	100k
R12	20k (5 STAGES)

Figure 1. RIAA — Equalizer Schematic

COMPONENT VALUES FOR FIGURE 1

R8 = 25k R7 = 2.4k R9 = 240k			R8 = 50k R7 = 5.1k R9 = 510k			R8 = 100k R7 = 10k R9 = 1meg		
f_O	C5	C6	f_O	C5	C6	f_O	C5	C6
23Hz	1μF	0.1μF	25Hz	0.47μF	0.047μF	12Hz	0.47μF	0.047μF
50Hz	0.47μF	0.047μF	36Hz	0.33μF	0.033μF	18Hz	0.33μF	0.033μF
72Hz	0.33μF	0.033μF	54Hz	0.22μF	0.022μF	27Hz	0.22μF	0.022μF
108Hz	0.22μF	0.022μF	79Hz	0.15μF	0.015μF	39Hz	0.15μF	0.015μF
158Hz	0.15μF	0.015μF	119Hz	0.1μF	0.01μF	59Hz	0.1μF	0.01μF
238Hz	0.1μF	0.01μF	145Hz	0.082μF	0.0082μF	72Hz	0.082μF	0.0082μF
290Hz	0.082μF	0.0082μF	175Hz	0.068μF	0.0068μF	87Hz	0.068μF	0.0068μF
350Hz	0.068μF	0.0068μF	212Hz	0.056μF	0.0056 μF	106Hz	0.056μF	0.0056μF
425Hz	0.056μF	0.0056μF	253Hz	0.047μF	0.0047μF	126Hz	0.047μF	0.0047μF
506Hz	0.047μF	0.0047μF	360Hz	0.033μF	0.0033μF	180Hz	0.033μF	0.0033μF
721Hz	0.033μF	0.0033μF	541Hz	0.022μF	0.0022μF	270Hz	0.022μF	0.0022μF
1082Hz	0.022μF	0.0022μF	794Hz	0.015μF	0.0015μF	397Hz	0.015μF	0.0015μF
1588Hz	0.015μF	0.0015μF	1191Hz	0.01μF	0.001μF	595Hz	0.01μF	0.001μF
2382Hz	0.01μF	0.001μF	1452Hz	0.0082μF	820pF	726Hz	0.0082μF	820pF
2904Hz	0.0082μF	820pF	1751Hz	0.0068μF	680pF	875Hz	0.0068μF	680pF
3502Hz	0.0068μF	680pF	2126Hz	0.0056μF	560pF	1063Hz	0.0056μF	560pF
4253Hz	0.0056μF	560pF	2534Hz	0.0047μF	470pF	1267Hz	0.0047μF	470pF
5068Hz	0.0047μF	470pF	3609Hz	0.0033μF	330pF	1804Hz	0.0033μF	330pF
7218Hz	0.0033μF	330pF	5413Hz	0.0022μF	220pF	2706Hz	0.0022μF	220pF
10827Hz	0.0022μF	220pF	7940Hz	0.0015μF	150pF	3970Hz	0.0015μF	150pF
15880Hz	0.0015μF	150pF	11910Hz	0.001μF	100pF	5955Hz	0.001μF	100pF
23820Hz	0.001μF	100pF	14524Hz	820pF	82pF	7262Hz	820pF	82pF
			17514Hz	680pF	68pF	8757Hz	680pF	68pF
			21267Hz	560pF	56pF	10633Hz	560pF	56pF
						12670Hz	470pF	47pF
						18045Hz	330pF	33pF

Many of the amplifiers that are being designed today are DC-coupled. This means that very low frequencies (2 – 15Hz) are being amplified. These low frequencies are common to turntables because of rumble and tone arm resonancies. Since the amplifiers can reproduce these sub-audible tones, they become quite objectionable because the speakers try to reproduce these tones. This causes non-linearities when the actual recorded material is amplified and converted to sound waves.

The RIAA has proposed a change in its standard playback response curve in order to alleviate some of the problems that were previously discussed. The changes occur primarily at the low frequency range with a slight modification to the high frequency range (See Figure 2). Note that the response peak for the bass section of the playback curve now occurs at 31.5Hz and begins to roll off below that frequency. The roll-off occurs by introducing a fourth RC network with a 7950μs time constant to the three existing networks that make up the equalization circuit. The high end of the equalization curve is extended to 20kHz, because recordings at these frequencies are achievable on many current discs.

NE5533/34 DESCRIPTION

the 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers.

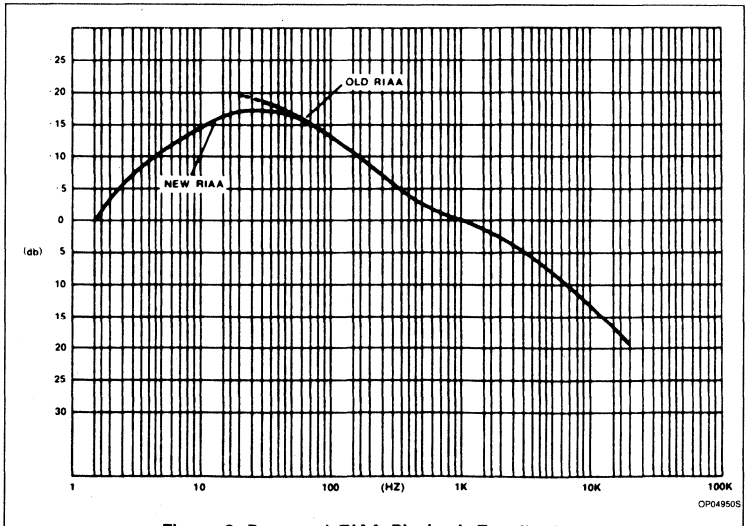
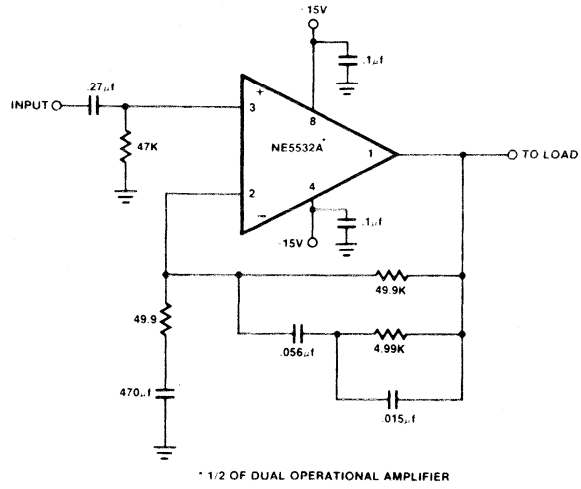


Figure 2. Proposed RIAA Playback Equalization

Audio Circuits Using the NE5532/33/34



NOTE:
All resistors are 1% metal film

Figure 3. RIAA Phonograph Preamplifier Using the NE5532A

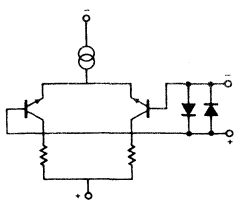
The op amps are internally-compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

APPLICATIONS

Diode Protection of Input

The input leads of the device are protected from differential transients above ±0.6V by internal back-to-back diodes. Their presence imposes certain limitations on the amplifier dynamic characteristics related to closed-loop gain and slew rate.

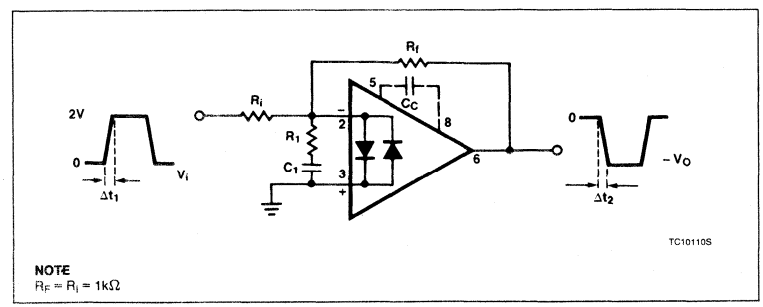
Consider the unity gain follower as an example:



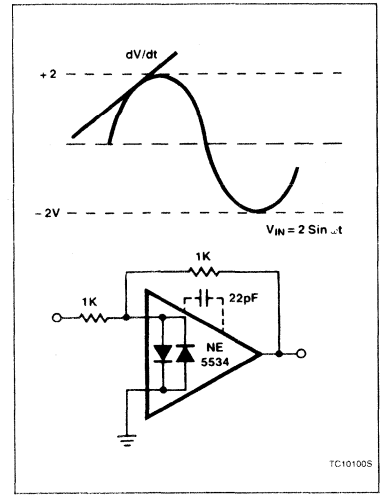
Assume a signal input square wave with dV/dt of 250V/μs and 2V peak amplitude as shown. If a 22pF compensation capacitor is inserted and the R_1 C_1 circuit deleted, the device slew rate falls to approximately 7V/μs. The input waveform will reach 2V/250V/μs or 8ns, while the output will have changed (8×10^{-3}) only 56mV. The differential input signal is then $(V_{IN} - V_O)$ $R_I/R_I + R_F$ or approximately 1V.

The diode limiter will definitely be active and output distortion will occur; therefore, $V_{IN} < 1V$ as indicated.

Next, a sine wave input is used with a similar circuit.



NOTE
$R_F = R_I = 1k\Omega$



The slew rate of the input waveform now depends on frequency and the exact expression is

$$\frac{dv}{dt} = 2\omega \cos \omega t$$

The upper limit before slew rate distortion occurs for *small-signal* ($V_{IN} < 100mV$) conditions is found by setting the slew rate to 7V/μs. That is:

$$7 \times 10^6 V/\mu s = 2\omega \cos \omega t$$

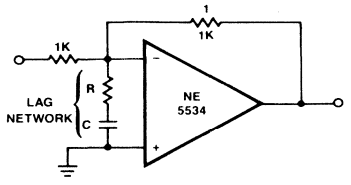
at $\omega t = 0$

$$\omega_{LIMIT} = \frac{7 \times 10^6}{2} = 3.5 \times 10^6 \text{ rad/s}$$

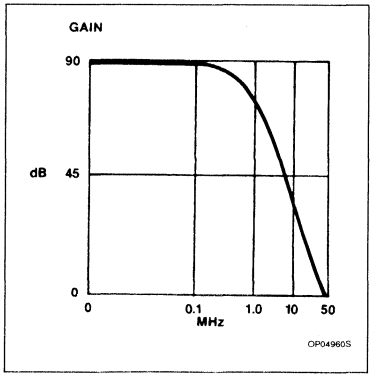
$$f_{LIMIT} = \frac{3.5 \times 10^6}{2\pi} \cong 560kHz$$

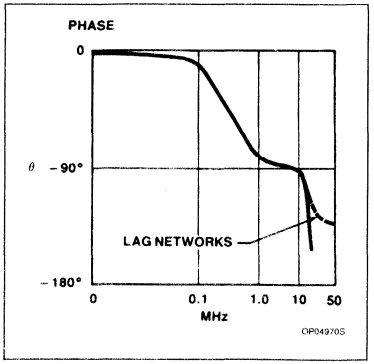
External Compensation Network Improves Bandwidth

By using an external lead-lag network, the follower circuit slew rate and small-signal bandwidth can be increased. This may be useful in situations where a closed-loop gain less than 3 to 5 is indicated. A number of examples are shown in subsequent figures. The principle benefit of using the network approach is that the full slew rate and bandwidth of the device is retained, while impulse-related parameters such as damping and phase margin are controlled by choosing the appropriate circuit constants. For example, consider the following configuration:



The major problem to be overcome is poor phase margin leading to instability.





By choosing the lag network break frequency one decade below the unity gain crossover frequency (30 – 50MHz), the phase and gain margin are improved. An appropriate value for R is 270Ω. Setting the lag network break frequency at 5MHz, C may be calculated

$$C = \frac{1}{2\pi \cdot 270 \cdot 5 \times 10^6}$$
$$= 118\text{pF}$$

RULES AND EXAMPLES

Compensation Using Pins 5 and 8 (Limited Bandwidth and Slew Rate)

A single-pole and zero inserted in the transfer function will give an added 45° of phase margin, depending on the network values.

Calculating the Lead-Lag Network

$$C_1 = \frac{1}{2\pi F_1 R_1} \quad \text{Let } R_1 = \frac{R_{IN}}{10}$$

where

$$F_1 = \frac{1}{10}\,(\text{UGBW})$$

UGBW = 30MHz

External Compensation for Wide-Band Voltage-Follower

Shunt Capacitance Compensation

$$C_F = \frac{1}{2\pi F_F R_F}, \quad F_F \cong 30\text{MHz}$$

or

$$C_F \cong \frac{C_{DIST}}{A_{CL}}$$

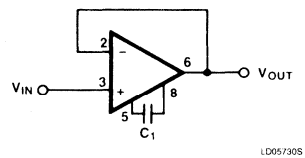
$C_{DIST} \cong$ Distributed Capacitance $\cong$ 2 – 3pF

Many audio circuits involve carefully-tailored frequency responses. Pre-emphasis is used in all recording mediums to reduce noise and produce flat frequency response. The most often used de-emphasis curves for broadcast and home entertainment systems are shown in Figure 7. Operational amplifiers are well suited to these applications because of their high gain and easily-tailored frequency response.

RIAA PREAMP USING THE NE5534

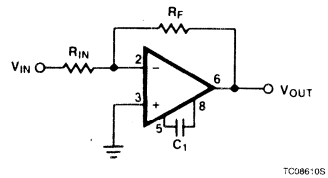
The preamplifier for phono equalization is shown in Figure 8 with the theoretical and actual circuit response.

Low frequency boost is provided by the inductance of the magnetic cartridge with the



NOTES:
$C_1 = C_C(1)$
C_C = 22pF for NE5533/34
C_C = 22pF [See graph under typical performance characteristics]

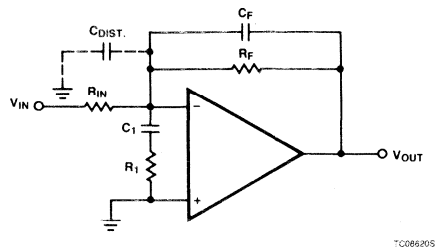
Figure 4. Unity Gain Non-Inverting Confliguration



NOTES:
$R_F = R_{IN}$

$$C_1 = C_C \left[\frac{R_{IN}}{R_F + R_{IN}}\right] = \frac{C_C}{2} \text{ therefore, } C_1 \simeq 11\text{pF}$$

Figure 5. Unity Gain Inverting Confliguration



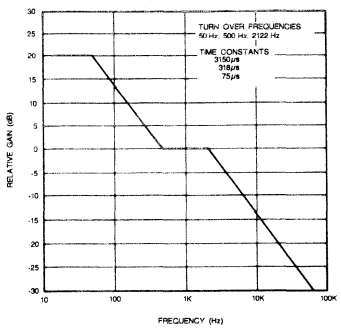
NOTE:
Input diodes limit differential to < 0.5V

Figure 6. External Compensation for Wideband Voltage Follower

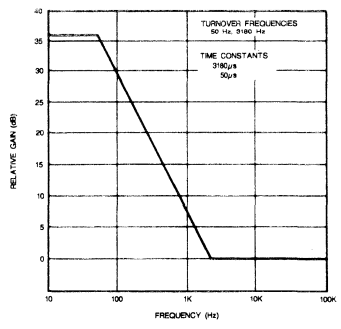
RC network providing the necessary break points to approximate the theoretical RIAA curve.

RUMBLE FILTER

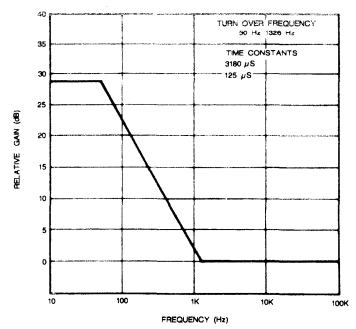
Following the amplifier stage, rumble and scratch filters are often used to improve overall quality. Such a filter designed with op amps uses the 2-pole Butterworth approach and features switchable break points. With the circuit of Figure 9, any degree of filtering from fairly sharp to none at all is switch-selectable.



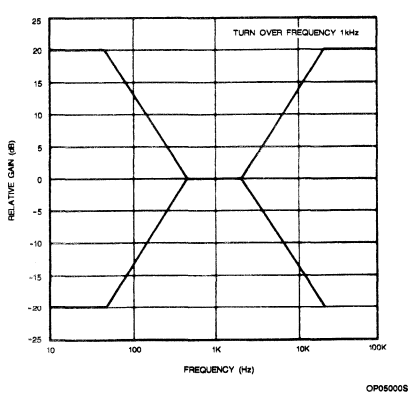
a. RIAA Equalization



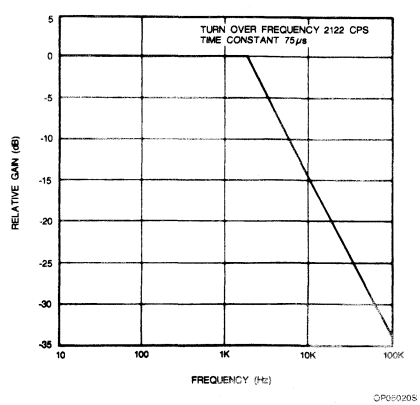
b. NAB Standard Playback 7½ IPS



c. 3.75 IPS Tape Equalization

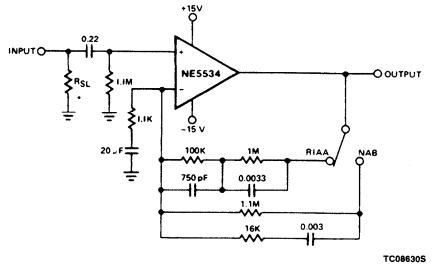


d. Base Treble Control Curve



e. Standard FM Broadcast Equalization

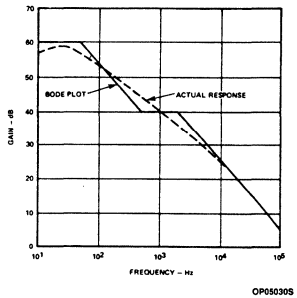
Figure 7



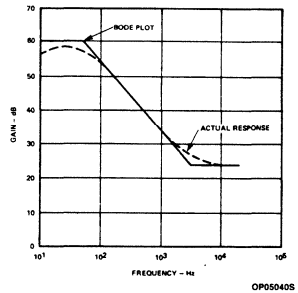
NOTES:
*Select to provide specified transducer loading.
Output Noise ≅ 0.8mV$_{RMS}$ (with input shorted)

All resistor values are in ohms.

a.

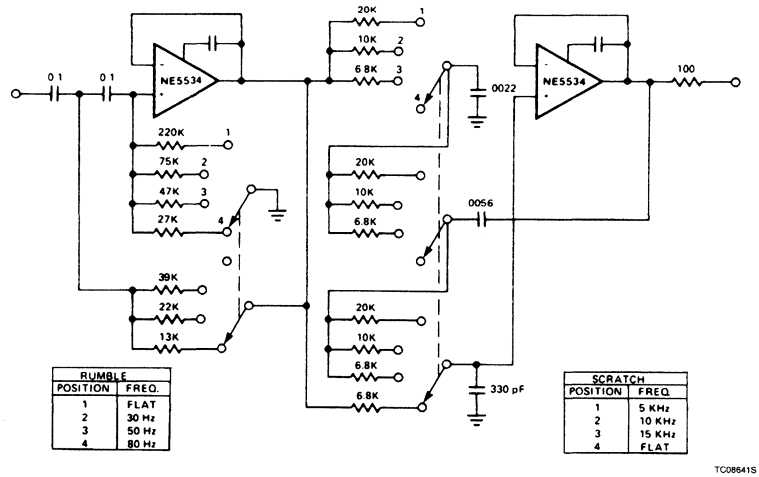


b. Bode Plot of RIAA Equalization and the Response Realized in an Actual Circuit Using the 531.



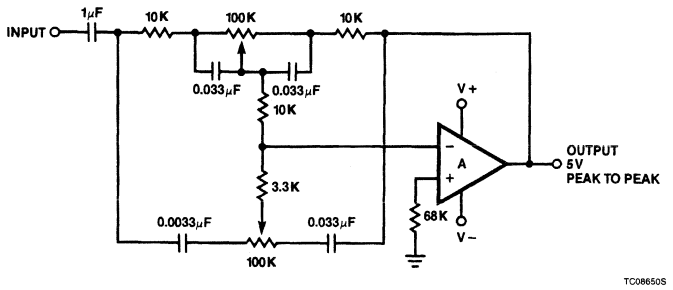
c. Bode Plot of NAB Equalization and the Response Realized in the Actual Circuit Using the 531.

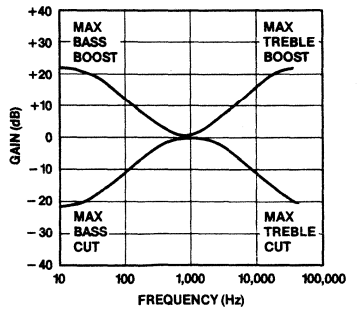
Figure 8. Preamplifier — RIAA/NAB Compensation



NOTE:
All resistor values are in ohms.

Figure 9. Rumble/Scratch Filter

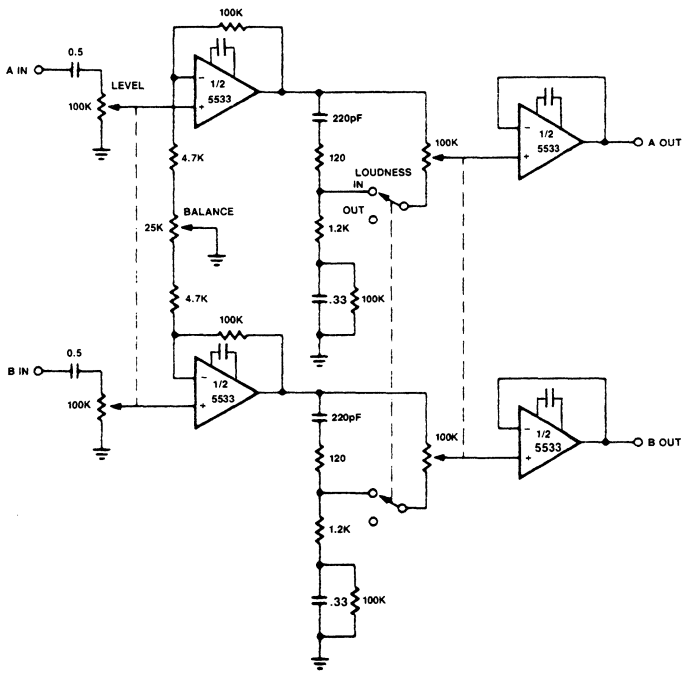




NOTES:
1. Amplifier A may be a NE531 or 301. Frequency compensation, as for unity gain non-inverting amplifiers, must be used.
2. Turn-over frequency — 1kHz.
3. Bass boost + 20dB at 20Hz, bass cut − 20dB at 20Hz, treble boost + 19dB at 20Hz, treble cut − 19dB at 20Hz.

All resistor values are in ohms.

Figure 10. Tone Control Circuit for Operational Amplifiers



NOTE:
All resistor values are in ohms.

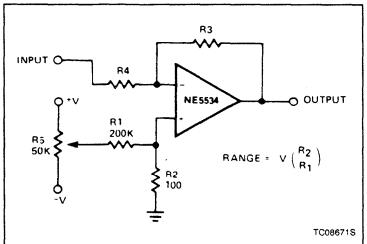
Figure 11. Balance Amplifier with Loudness Control

TONE CONTROL

Tone control of audio systems involves altering the flat response in order to attain more low frequencies or more high ones, dependent upon listener preference. The circuit of Figure 10 provides 20dB of bass or treble boost or cut as set by the variable resistance. The actual response of the circuit is shown also.

BALANCE AND LOUDNESS AMPLIFIER

Figure 11 shows a combination of balance and loudness controls. Due to the non-linearity of the human hearing system, the low frequencies must be boosted at low listening levels. Balance, level, and loudness controls provide all the listening controls to produce the desired music response.

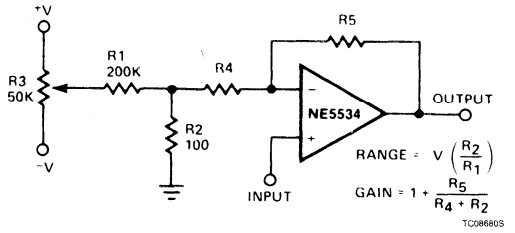


NOTE:
All resistor values are in ohms.

Figure 12. Universal Offset Null for Inverting Amplifiers

VOLTAGE AND CURRENT OFFSET ADJUSTMENTS

Many IC amplifiers include the necessary pin connections to provide external offset adjustments. Many times, however, it becomes necessary to select a device not possessing external adjustments. Figures 12, 13, and 14 suggest some possible arrangements for offset voltage adjust and bias current nulling circuitry. The circuitry of Figure 14 provides sufficient current into the input to cancel the bias current requirement. Although more simplified arrangements are possible, the addition of Q2 and Q3 provide a fixed current level to Q1, thus, bias cancellation can be provided without regard to input voltage level.



NOTE:
All resistor values are in ohms.

Figure 13. Universal Offset Null for Non-Inverting Amplifiers

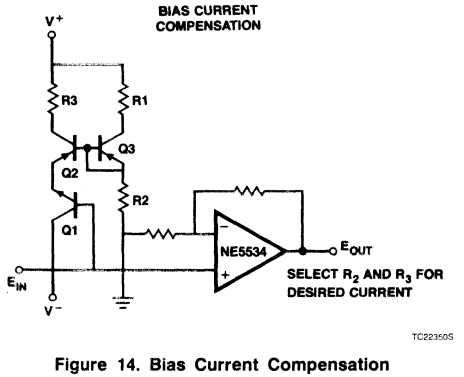


Figure 14. Bias Current Compensation

AN144
Applications for the NE/SA/SE5512

Application Note

DESCRIPTION

The NE/SA/SE5512 series of high-performance operational amplifiers provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector-to-emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability, yet have low supply quiescent current.

BRIDGE TRANSDUCER AMPLIFIER

In applications involving strain gauges, accelerometers and thermal sensors, a bridge transducer is often used. Frequently the sensor elements are high resistance units requiring equally high bridge resistance for good sensitivity. This type of circuit then demands an amplifier with high input impedance, low bias current and low drift. The circuit shown represents a solution to these general requirements (Figure 1).

For V_S = 10V, the common-mode voltage is approximately +5V, well within the common-mode limits of the NE5512.

The sensitivity of the input stage is approximately

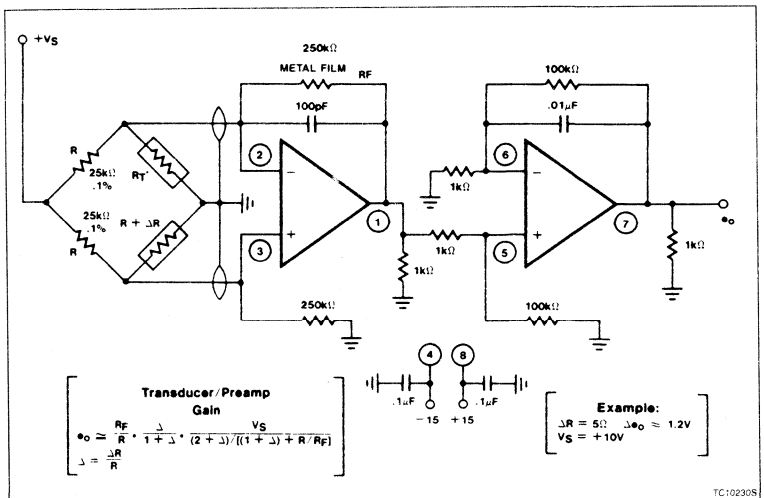
$$\frac{R_F \cdot V_S}{2R}$$

to a change in transducer resistance ΔR. This gives a gain factor of ≅50 for V_S = 10V and R = 25kΩ. The second stage gain is ×100 giving a total gain of ≅5000.

Noise is minimized by shielding the transducer leads and taking special care to determine a good signal ground. Common-mode noise rejection is particularly important, making matched differential impedance critical. The NE5512 typically provides 100dB of common-mode rejection and will considerably reduce this undesirable effect.

The following are sensitivity figures for the transducer circuits.

	ΔR / 10Ω	ΔE_{OUT}
Leg 1		−2.6V
	5Ω	−1.3V
Leg 2	10Ω	+2.4V
	5Ω	+1.2V



NOTE:
Thermal compensation transducer (non-active)

Figure 1. NE/SE5512 Bridge Transducer Amplifier

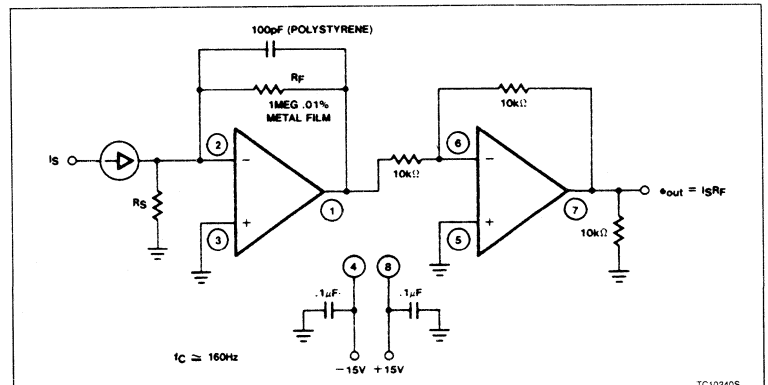


Figure 2. NE/SE5512 Current-to-Voltage Converter With 1% Accuracy [Sensitivity: 1V/μA]

Temperature compensation of the bridge element is accomplished by using low drift metal film resistors and also by providing a complimentary non-active sensor element to thermally track the offset in the active element.

High frequency roll-off provides attenuation of unwanted noise above the pass band of the transducer. The shunt capacitors across both stage feedback resistors are for this purpose.

CURRENT-TO-VOLTAGE CONVERTER

Taking advantage of the very low bias current and offset of the NE5512 is demonstrated in its adaptation to a current-to-voltage converter as shown in Figure 2.

The lower limit of measuring accuracy is determined by I_B (inverting), which is typically

6nA. In order to attain a measurement accuracy of 1%, the following inequality must hold:

$I_B \leq (0.01)\ I_{Smin}$

Where I_B = input bias current and I_{Smin} = minimum measured current. For I_B = 6nA and I_{Smin} = 1μA,

6nA ≤ (0.01) 1μA = 10nA and the inequality hold.

DC offset and current noise gain is determined by

$$\frac{R_F + R_S}{R_S}$$

which ≅ 1 for $R_S >> R_F$.

The measured results for this circuit appear below (V_{CC} = ±15V).

INPUT CURRENT	OUTPUT VOLTAGE
1μA	1.008V
5μA	5.00V
10.00μA	10.00V

NE5512 OPERATIONAL DIFFERENTIATOR

By utilizing the very high input impedance characteristic of the NE5512, an excellent active differentiator can be realized. Using the circuit shown (Figure 3), good results were obtained as shown by the waveforms in Figures 4, 5 and 6. One of the primary problems with such circuits is the tendency towards instability and distortion either due to loading caused by input bias currents or amplifier non-linearity. In addition, gain increases with frequency, requiring low input noise in the amplifier.

The relative stability is shown by the output signal waveforms mentioned above. Adding R_1 provides added compensation in the form of a zero near the amplifier unity gain frequency. Frequency range is 100Hz to 10kHz.

In order to obtain good differentiation, the network time constant, RC, must be small relative to the period of the highest frequency present at the input. Since the differentiator will attenuate the signal by a factor of ωRC, which may be 100:1 in the operating region, the second amplifier stage is used to compensate for this loss. Various circuits are easily interfaced with the differentiator block due to the inherently low output impedance of the NE5512.

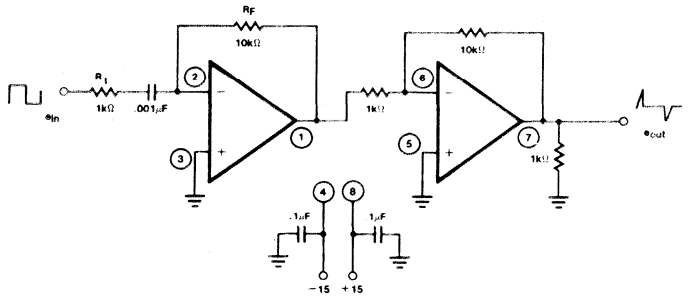


Figure 3. NE/SE5512 Active Differentiator With Inverting × 10 Buffer

DIFFERENTIATOR WAVEFORMS

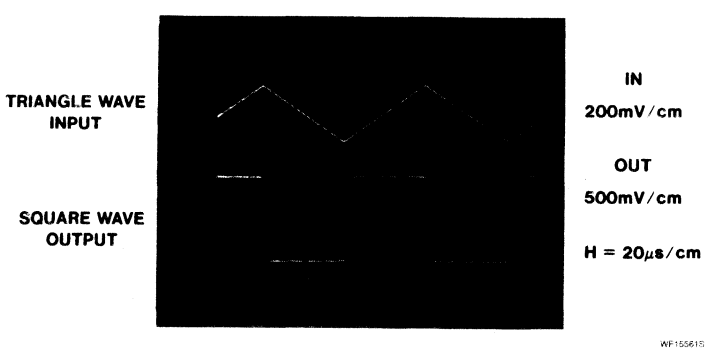


Figure 4

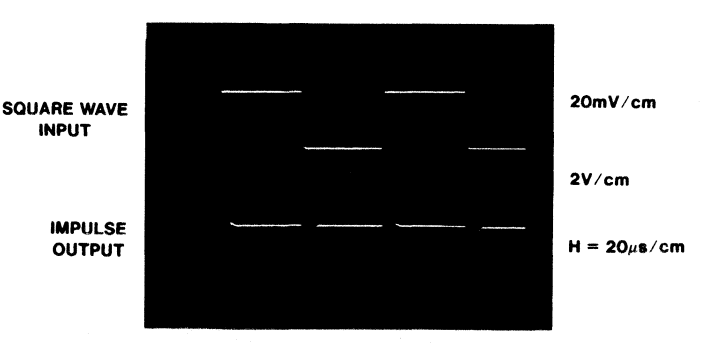


Figure 5

THE OPERATIONAL INTEGRATOR

The operational complement of the active differentiator is the active integrator. The NE5512 is easily adapted to this function as shown in the circuit below (Figure 7). To obtain satisfactory integration, the time constant must fulfill the following requirement:

$RC \geq 15T$

Where T is the period of the input waveform.

For the ideal integrator

$$e_{out} = \frac{1}{RC}\int e_{in}\, dt$$

The factor 1/RC represents an attenuation of the input signal. The low signal level is increased by using the second half of the NE5512 as a gain stage following the operational integration. The waveforms in Figures 8 and 9 show the input-output relationship for both a sine wave and a square wave function. A good integrator must exhibit a phase shift of $\geq 89°$ for sine wave input over the active frequency range. For a square wave, the resultant output must be a linear ramp. The circuit shown fulfills this requirement (see Figure 7). No external compensation is required since the amplifier is unity gain stable.

DIFFERENTIATOR WAVEFORMS

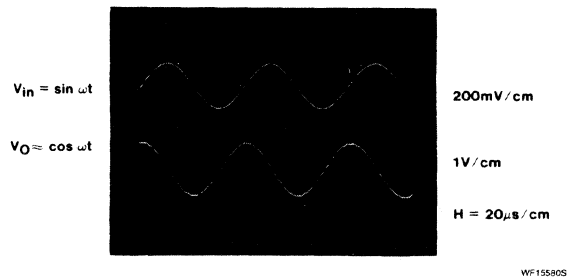


Figure 6

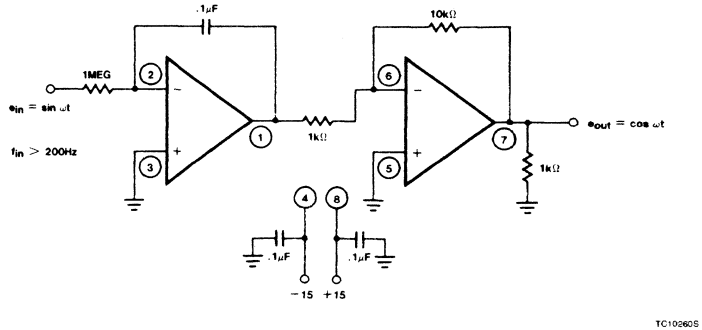


Figure 7. NE/SE5512 Active Integrator

INTEGRATOR WAVEFORMS

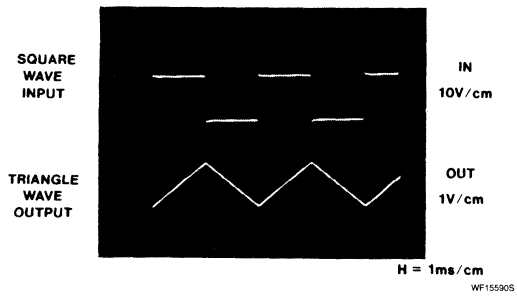


Figure 8

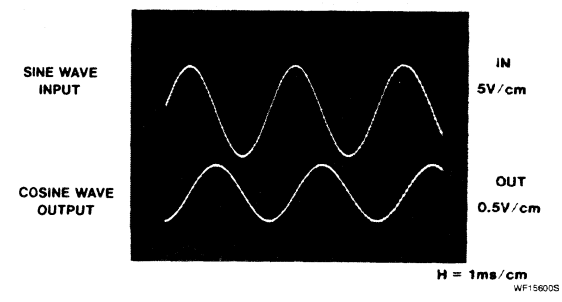


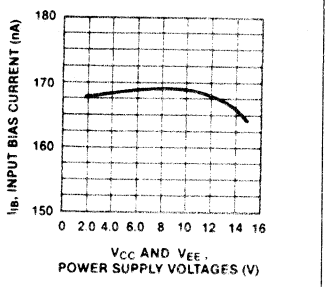
Figure 9

AN160
Applications for the MC3403

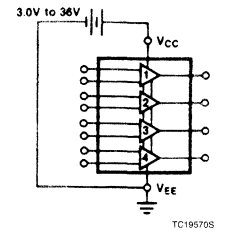
Application Note

MC3403 DESCRIPTION

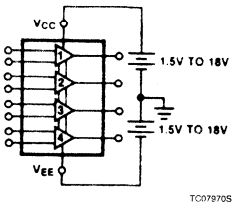
The MC3403 is a quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular μA741. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The MC3403 can operate at supply voltages as low as 3.0V or as high as 36V. The common-mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.



Input Bias Current vs Supply Voltage

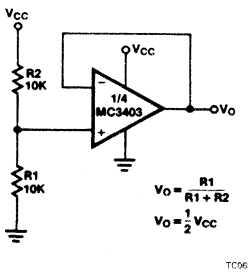


Single Supply

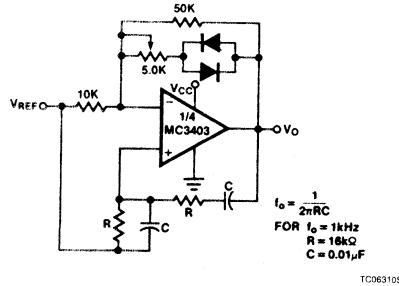


Split Supplies

APPLICATIONS

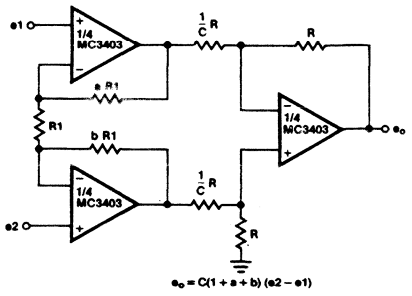


Voltage Reference

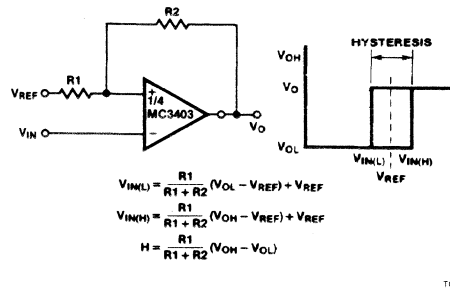


Wein Bridge Oscillator

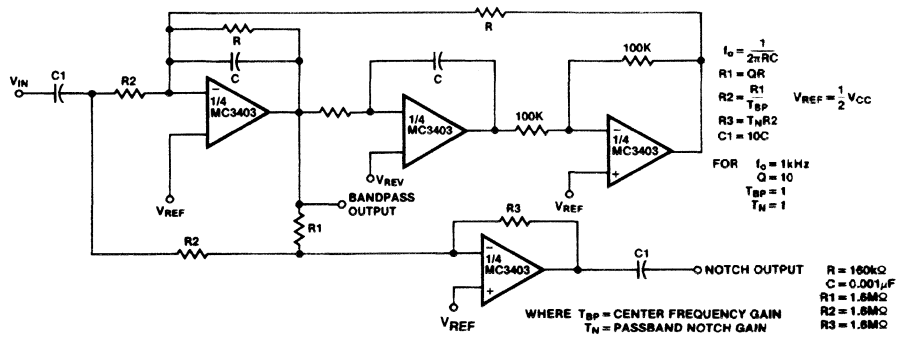
APPLICATIONS (Continued)



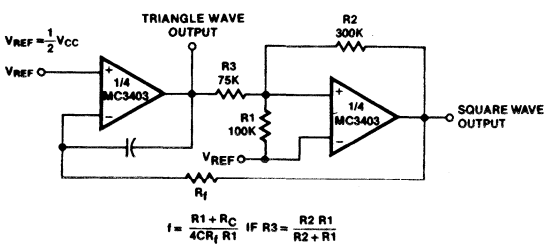
High Impedance Differential Amplifier



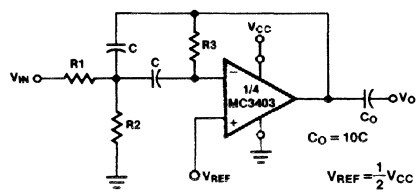
Comparator With Hysteresis



Bi-Quad Filter



Function Generator



GIVEN f_o = CENTER FREQUENCY
$A(f_o)$ = GAIN AT CENTER FREQUENCY

CHOOSE VALUE f_o, C

THEN:

$R3 = \frac{Q}{\pi f_o C}$

$R1 = \frac{R3}{2A(f_o)}$

$R2 = \frac{R1\,R5}{4Q^2 R1 - R5}$

FOR LESS THAN 10% ERROR FROM OPERATIONAL AMPLIFIER

$\frac{Q_o f_o}{BW} < 0.1$ WHERE f_o AND BW ARE EXPRESSED IN Hz.

IF SOURCE IMPEDANCE VARIES, FILTER MAY BE PRECEDED WITH VOLTAGE FOLLOWER BUFFER TO STABILIZE FILTER PARAMETERS.

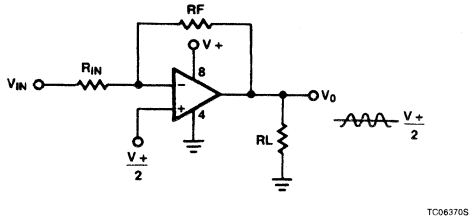
TC06360S

Multiple Feedback Bandpass Filter

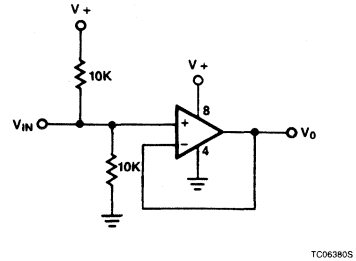
Applications for the MC3403

AN160

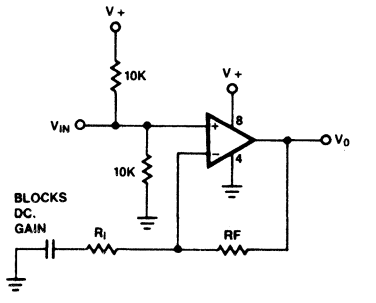
TYPICAL APPLICATIONS



Single Supply Inverting Amplifier



Input Biasing Voltage-Follower



Non-Inverting Amplifier

AN1441
Applications for the NE5514

Application Note

NE5514 DESCRIPTION

The SE/NE5514 family of Quad Operational Amplifiers sets new standards in Bipolar Quad Amplifier Performance. The amplifiers feature low input bias current and low offset voltages. Pinout is identical to LM324/ LM348, which facilitates direct product substitution for improved system performance. Output characteristics are similar to a μA741 with improved slew and drive capability.

FOUR-QUADRANT PHOTO-CONDUCTIVE DETECTOR AMPLIFIER

When operating a photo diode in the photo-conductive mode (reverse-biased) very small currents in the microampere range must be sensed in the photo active operating region. Dark currents in the nanoamperes are common. Generally, for this reason, JFET input preamps are used to prevent interaction and accuracy degradation due to input bias currents.

The 5514 has sufficiently low input bias current (6nA) to allow its use under these circuit constraints as shown in a possible design used to sense four-quadrant motion of a light source. By proper summing of the signals from the X and Y axes, four-quadrant output may be fed to an X-Y plotter, oscilloscope or computer for simulation (see Figure 1).

The wide input common-mode voltage range of the device allows a +10V supply to be used to drive the signal bridge giving high sensitivity and improved signal-to-noise. Obviously, input balancing is critical to achieving common-mode signal rejection in addition to adequate shielding of the sensor leads. The sensor head itself must be shielded and the shield grounded to signal common to avoid unwanted noise pick-up from power line and other local noise sources. Amplifier response may be shaped to aid in noise reduction by more complex filter configurations. If possible the 5514 should be located in close proximity to the sensor head.

System balance may be done under dark field conditions if adequate photo detector tracking results. However, for high accuracy systems, a bipolar balance adjust added to the non-inverting output stage is more desirable. With this latter method, the signal bridge is balanced for a null output under uniform light field conditions using the bridge balance pot as shown. DC offset is then adjusted using the balance pot on the output amplifier under dark field conditions.

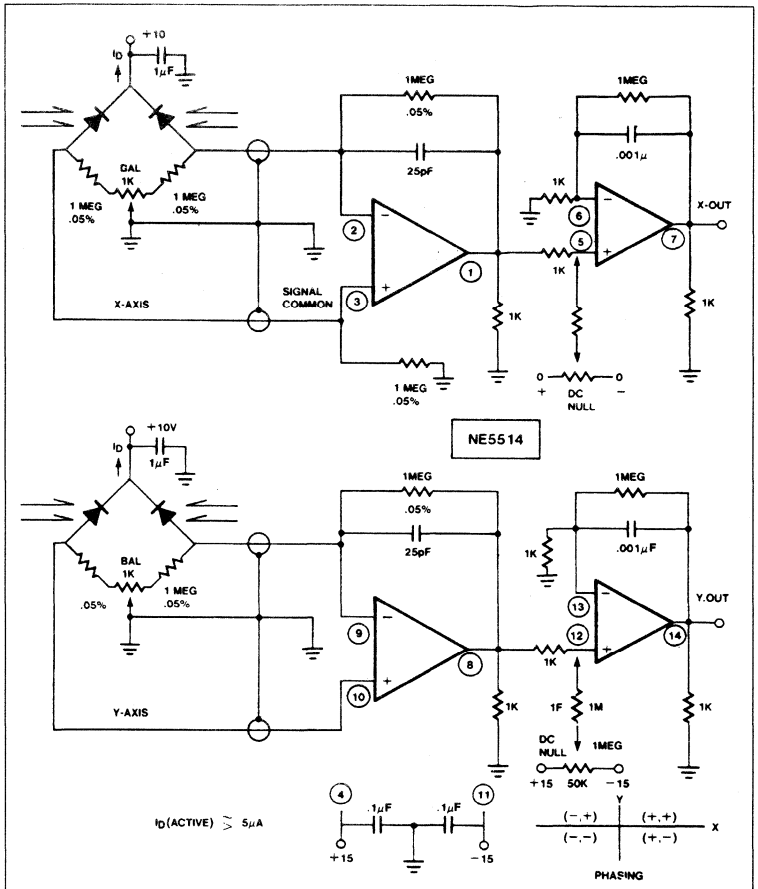


Figure 1. Four-Quadrant Photo Detector

MULTI-TONE BANDPASS FILTER FOR PLL TONE DECODER

In the design of a multiple tone signaling system, particularly where signals are transmitted over long lines, noise and adjacent channel interference may be a significant barrier to reliable communications. By the use of narrow-band active pre-filters to attain selectivity and gain, the effective signal to noise ratio is greatly improved. The NE/ SE5514 is easily adapted to such filter configurations due to its inherent stability. In addition, its very high input impedance drastically reduces loading to the passive networks and allows for increased "Q" and large value resistors.

The circuit in Figure 2 demonstrates multiple feedback filters operating at four of the standard signaling frequencies. More channels may be added to increase the capacity of the system.

Test results obtained from the filter configuration were as follows:

Wide-band signal-to-noise	63dB
Gain (Mid band)	30dB
Q (effective)	≈ 30
Output	0dBM (0.775V_{RMS})

Note that the amplifiers are operated from a single +12V supply and are biased to half V_{CC} by a simple resistive divider at point B which connects to all non-inverting inputs.

4-STATION 0 – 50° TEMPERATURE SENSOR

By using an NPN transistor as a temperature sensing element, the NE5514 forms the basis for a multi-station temperature sensor as shown in Figure 3. The principle used is fundamental to the current voltage relationship of a forward-biased junction. The current flow across the base-emitter junction is determined by absolute temperature in the following way:

$$I_E = -(I_C + I_B)$$

and $I_E \propto I_S \exp(V_{BE}/V_T)$; $V_T = \frac{kt}{q}$

therefore, $V_{BE} \propto V_T \ln I_E/I_S$

Where I_E is the forward current and I_S is the saturation current inherent in the junction, I_E must be high enough such that the I_S variation with temperature is small relative to I_E ($I_E >> I_S$). I_S is typically 0.05pA, therefore, setting I_E to 1 or 2μA gives the desired condition.

Diode D_1 serves to substantially reduce error due to power supply variation by giving a fixed voltage reference. To calibrate the sensor adjust R_4 for "0" volts output from the NE5514 at 0°C. Adjust R_6 tracking resistor for a scale factor of 100mV/°C output.

Only the transistor need be placed in the temperature-controlled environment. Figure 4 shows the addition of an A/D converter and display to give a digital thermometer.

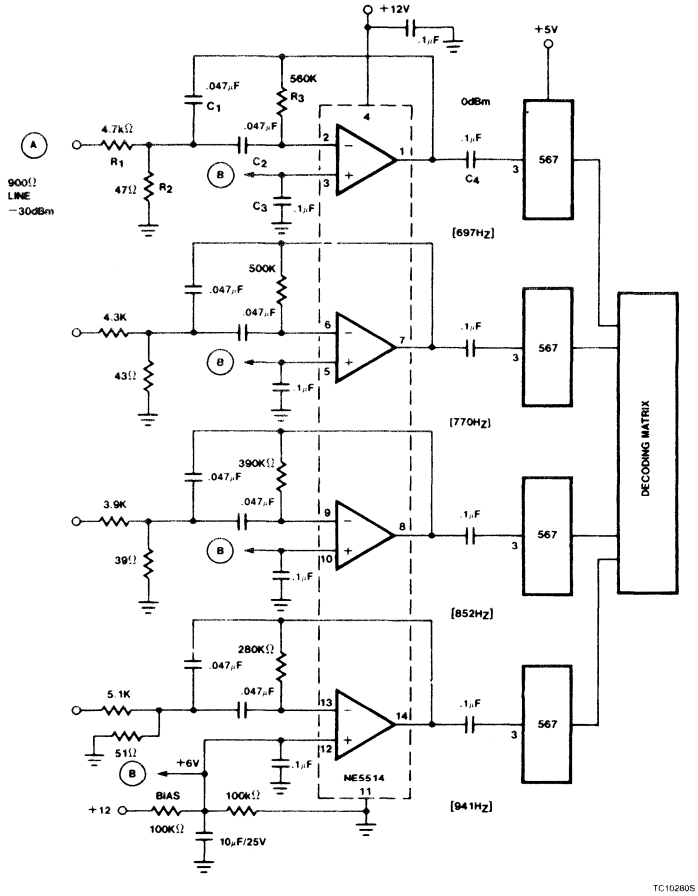


Figure 2. NE5514 MFB Bandpass Filter for Multi-Channel Tone Decoder

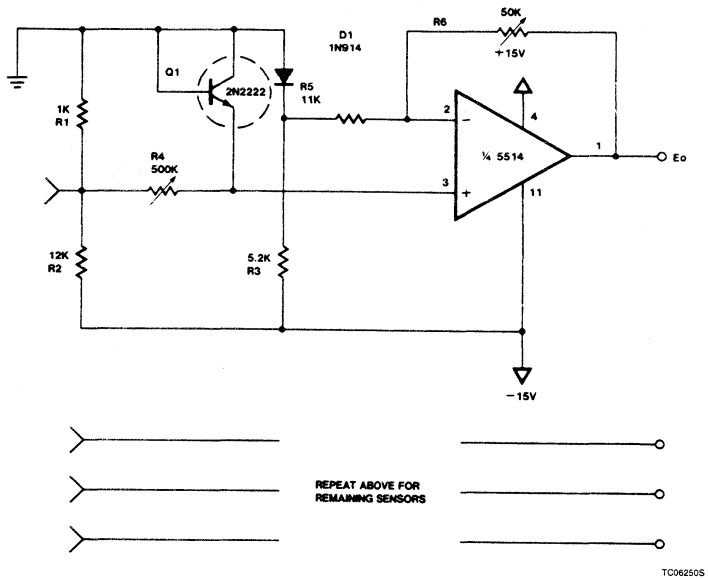


Figure 3. 4-Channel Temperature Sensor (0 – 50°C)

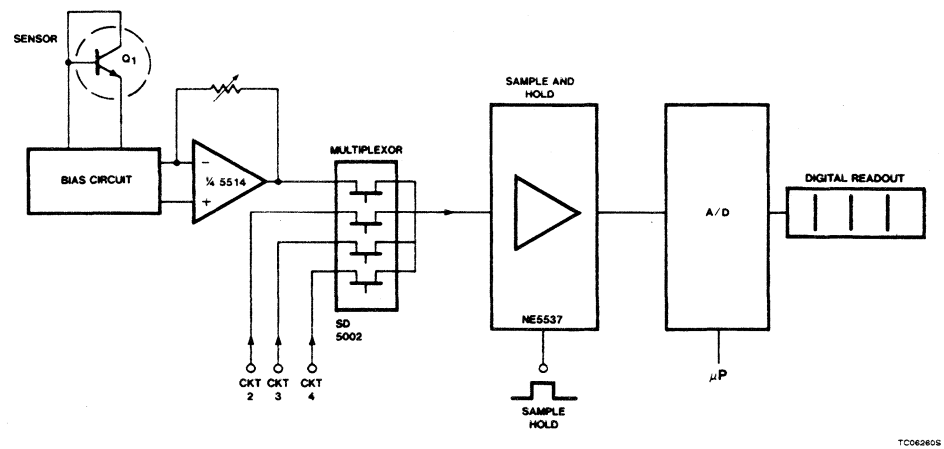


Figure 4. Microprocessor-Controlled Digital Thermometer

AN1511
Low-Voltage Gated Function Generator: NE5230

Application Note

INTRODUCTION

Described herein is a low-voltage, gated function generator using the NE5230 and two AA batteries. The outputs are a square, triangular and sine wave. The sine wave-generating circuit and the square and triangular circuits are independent. Some ideas for refinement of the circuits are also presented.

APPLICATIONS

The use of signal sources is universal. Over the years, a great many practical circuits have been developed which have numerous desirable features. These circuits are typified by high power outputs, or speed, or precision, or combinations of these. They are housed in rugged, handsome cases and are available for a few hundred dollars. Most require AC line cords and are somewhat cumbersome to use. With the advent of low-voltage op amps such as the NE5230, it is now possible to design good, stable, battery-operated signal sources.

SINE WAVE GENERATOR

The circuit used is a Wien bridge sine wave oscillator. This circuit has been used since the days of vacuum tubes (see Figure 1). It is simple, stable and requires few components. The circuit utilizes both positive and negative feedback to achieve balanced operation. The oscillator will stop working if too much negative feedback is used and will saturate in both states if too much positive feedback is used. In the practical implementation, some non-linear element must be employed to realize this stable condition. The gain of the amplifier must be large enough at the frequency of oscillation to make the input excursions small enough to be compensable by this non-linear element. Among others, diodes and FETs have been used to accomplish this. One of the most popular is the lamp; small, inexpensive and readily available, its voltage variable resistance makes it an ideal candidate for this application. It works like this: as the negative feedback voltage increases across the lamp, its resistance increases, and thereby reduces the output voltage. When the output voltage decreases, the amount of negative feedback voltage across the lamp decreases and thereby increases the resistance of the lamp. This balancing act continues until a stable condition is achieved. It is important to note that the lamp resistance is changing due to the thermal effects caused by the changing voltage across it. The frequency of oscillation is determined by:

$$f_{OSC} = \frac{1}{2\pi RC}$$

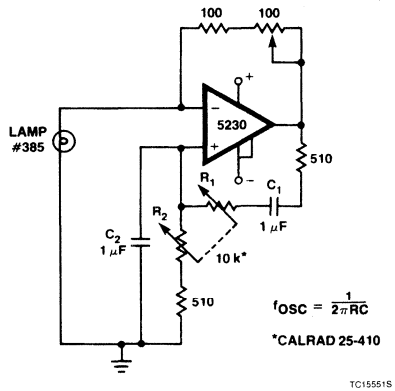


Figure 1. Sine Wave Generator

VCO

Another classic oscillator circuit uses a comparator and an integrator. The output of the comparator is fed back to the input of the integrator. The output of the integrator is connected to the input of the comparator. Upon application of power, the comparator output goes into one state or the other. This comparator output voltage is fed back into the input of the integrator which begins ramping up or down, depending on the polarity of the first pulse from the comparator. When the voltage threshold of the comparator is reached, the output changes state. The cycle then repeats.

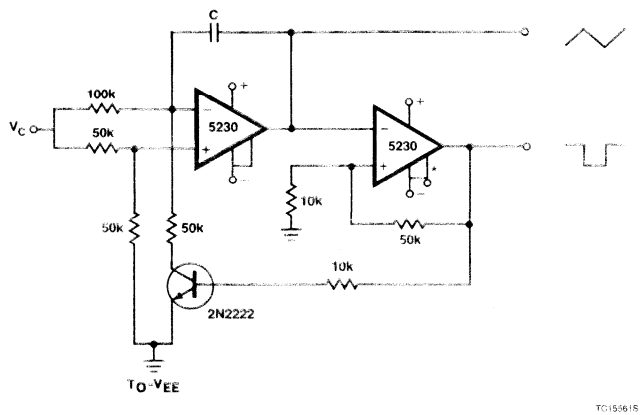
If an inversion in the feedback loop can be achieved, and external energy can be introduced at the right time, some interesting modifications of the previously described circuit will result — namely, a voltage-controlled oscillator. It works as follows: the transistor inverts the output of the comparator. This voltage is presented to the inverting input of the integrator to begin the cycle. When the comparator threshold is reached, the comparator changes state as before. This time, however, because the external applied voltage to the same inverting input is present, the amount of current available to the input is controlled by the external voltage and not by the feedback voltage. Once the component values are selected, the applied voltage, V_C, sets the frequency of oscillation because the current available to the integrating capacitor determines the charging time constant and, therefore, the frequency. The more positive the V_C, the more current that is available and the higher the frequency of oscillation. The converse is also true with minor differences. It is interesting to note here that other low-voltage amplifiers are not able to perform as well as the NE5230 in this circuit. One reason is that the NE5230 input voltage swing is able to exceed the rails by 250mV and still operate within its linear region. For a given set of conditions, then, the frequency range of the NE5230 is wider than conventional low-voltage op amps. The frequency of this circuit can also be changed by changing the value of the integrating capacitor. The smaller the capacitor, the higher the frequency for a given set of conditions.

PERFORMANCE

The circuit in Figure 2 is the complete low-voltage function generator. The measurements were taken at room temperature with

Low-Voltage Gated Function Generator: NE5230

AN1511



NOTE:
*See text.

Figure 2. Function Generator

only two AA batteries supplying the power. The outputs were loaded with 200Ω for the sine and triangular wave outputs and 50Ω for the square wave output. The output voltage for the sine wave was ± 1V. The square wave output swung from rail to rail while the output voltage of the triangular wave varied with the input voltage, V_C. This was due, of course, to the collector-emitter voltage requirements of the transistor.

The distortion of the Wien bridge was 0.015% at the lowest frequency and 0.09% at the highest. Using the different capacitor values, the frequency was varied from minimum to maximum using the ganged 10kΩ pot. The frequencies could be changed from 20Hz to 2.5kHz. It was necessary to include a 500Ω resistor in each leg of the bridge to prevent the complete saturation of the amplifier when the potentiometer was in one extreme of its travel. In addition, a small adjustment resistor was used in the negative feedback loop to adjust the gain and to compensate for the slow thermal time constant of the lamp.

The maximum frequency obtained by the VCO was 9.7kHz with V_C = 1.65V with ± 1.4V batteries. The frequency varied from 8.4kHz to 1.6kHz with ± 1 (V_C) applied with a 0.001μF integrating capacitor.

CONCLUSIONS

Some things could have been done differently to improve the operation of these circuits. The thermal time constant of the non-linear elements was an inhibiting factor in the low-frequency operation of the Wien bridge. A diode or FET will work better here. Extreme ambient temperature will change the operating point of the lamp and, therefore, the output amplitude. Some non-symmetrical output was seen when operating the VCO at the lower frequencies. This is due to the influence of the transistor, as described previously.

Finally, the NE5230 has yet another feature: the bias adjust pin. This pin is intended to be used to control the power supply current. The power supply current is controlled by decreasing the internal bias current of the op amp. When the bias current is decreased, the transconductance, g_M, of the input stage is reduced; this, in turn, lowers the –3dB bandwidth. In addition, this pin can be used to turn the op amp on or off. If the voltage at the bias adjust pin is moved to 50mV above the voltage at the V_{EE} pin, the output becomes severely attenuated. The op amp, for all intents and purpose, is off. If, on the other hand, the bias adjust pin is moved to 50mV below the voltage at the V_{EE} pin, the bandwidth and the slew rate are increased. The user should exercise care when doing this.

The NE5230 is a versatile, low-voltage op amp. It has been demonstrated that the device can be used in a variety of different ways. Its ability to swing within 100mV of the output, its input voltage which can exceed the power supply voltage, and its programmable power supply current, make it a leader of low-voltage op amps.

REFERENCES:

Modern Electronic Circuit Reference Manual, John Markus

Raytheon 1984 Data Manual

AN1512
All in One: NE5230

Application Note

ABSTRACT

Recent improvements in low voltage operational amplifier design have resulted in novel applications formerly thought impossible. Design improvements include rail-to-rail operation at both the input and output, programmable bandwidth, full swing capability to ±0.8V with ±9V V_{CC} and availability in surface mount packages. These unique features combine to make possible applications such as voltage-to-current conversion down to zero; a low voltage, full-swing, instrumentation amplifier; a solar-powered, gated function generator; active filters and many more applications. A circuit for increased output power is also presented.

INTRODUCTION

The name of the game in low voltage op amps is: MAX HEADROOM. For a given range of voltage, how much of that voltage can be utilized by the op amp's output? Traditionally, not very much, especially on the positive side. Among other important concerns are input voltage range, drive capability, speed, input bias current and power supply current. Trade-offs are part of every design. But with each new design, fewer trade-offs are tolerated. For example, drive capability and speed were not available in the same amplifier. Now, they are not only offered together but expected in precision designs. And so it is with low voltage and input and output rail-to-rail operation. The NE5230 is the first to offer this combination. Moreover, the device offers power supply current programmability. This feature allows variable bandwidth, slew rate and, to some degree, input bias current. This unique combination of features makes the device useful in a great many applications. What this means to the user is outlined below.

INPUT AND OUTPUT RAIL-TO-RAIL OPERATION

Figure 1 illustrates input and output rail-to-rail operation. The amplifier's common-mode voltage includes both input rails, and its output swings up to both rails. The NE5230 is unique in this regard. Figure 1 demonstrates the usefulness of this feature. The voltage-to-current converter shown in Figure 2 can deliver current down to zero for a zero input voltage. With minor changes, this circuit can also be configured to sink as well as source current by simply using an NPN connected to the negative supply instead of the PNP connected to the positive supply. The output current is a function of the input voltage divided by the value of the load resistor. Selection of the resistor value is limited, on the one hand, by the maximum power capability of the amplifier, which is outlined in the data sheet. While many amplifiers can swing to the negative rail, no other can accomplish this at both output rails under load. Applications range from transducer interfaces to level-shift circuits.

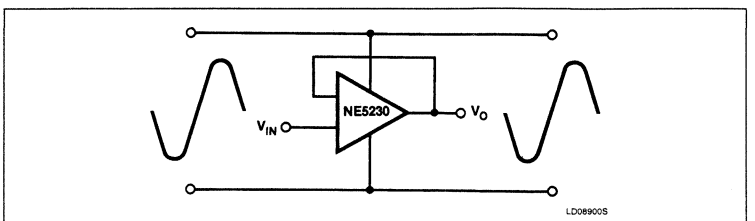


Figure 1. Rail-to-Rail Operation

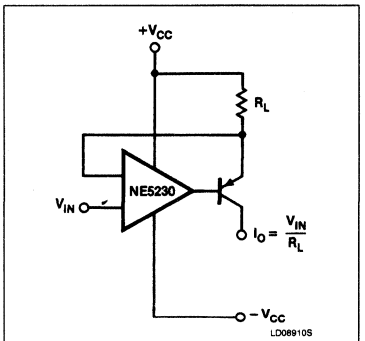


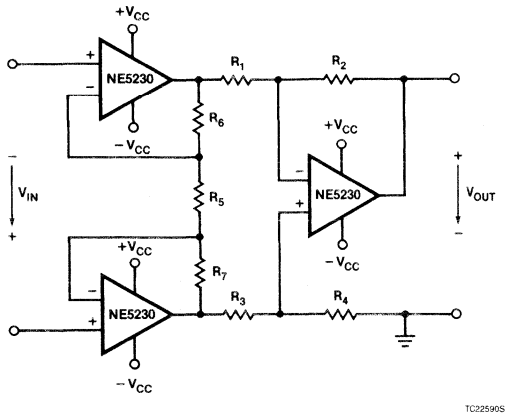
Figure 2. Voltage-to-Current Converter

INSTRUMENTATION AMPLIFIER

Another useful application for rail-to-rail operation is the instrumentation amplifier shown in Figure 3. Along with its other practical features of high common-mode rejection ratio, high input impedance, and low offset drift, this familiar amplifier's capability has now been enhanced. Signal swing beyond both input rails and swing up to both output rails is now possible. With equal value resistors, the gain configuration is a non-inverting gain of three. With the power supply voltage of ±2.00V, with no load at room temperature, the performance was predictable. The photographs in Figure 4 show the input and output of the waveforms of the circuit used. Among its other applications, remote transducers, portable precision instrumentation and any low voltage, low power application are included in this amplifier's repertoire.

LOW VOLTAGE, GATED FUNCTION GENERATOR

Another useful application is as solar-powered, gated function generator. Although it can be powered conventionally, circuit performance is not significantly different with solar cells. This circuit uses a Wien Bridge sine wave oscillator. The Wien Bridge has been used since the vacuum tube era. It is simple, stable, and requires few external components. The circuit utilizes both positive and negative feedback to achieve balanced operation. The oscillator will stop working if too much negative feedback is used and will saturate in both states if too much positive feedback is used. In a practical implementation, some non-linear element must be employed to realize this stable condition. The gain of the amplifier must be large enough at the frequency of oscillation to make the input excursions small enough to be compensatable by this non-linear element. Diodes and FETs have been used to accomplish this. One of the most popular is the lamp; small, inexpensive and readily available, its voltage variable resistance makes it an ideal candidate for this application. It works like this: as the negative feedback voltage increases



$$A_V = \frac{R_2}{R_1}\left(1 + \frac{2R_6}{R_5}\right), \quad \begin{matrix} R_1 = R_3 \\ R_2 = R_4 \\ R_6 = R_7 \end{matrix}$$

Figure 3. Rail-to-Rail Instrumentation Amplifier

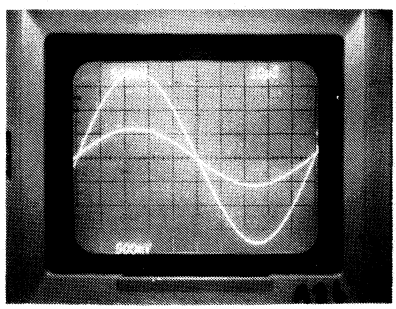


Figure 4. Input and Output Waveforms

across the lamp, its resistance increases, and thereby reduces the output voltage. When the output voltage decreases, the amount of negative feedback voltage across the lamp decreases, thereby decreasing the resistance of the lamp. This balancing act continues until a stable oscillation is achieved. It is important to note that the lamp resistance is changing due to the thermal effects caused by the changing voltage across it. The frequency of oscillation is determined by

$$f_{OSC} = \frac{1}{2\pi RC}$$

Another classic oscillator uses a comparator and an integrator. The output of the comparator is fed back to the input of the integrator. The output of the integrator is connected to the input of the comparator. Upon application of power, the comparator goes into one state or the other. This comparator output voltage is fed back into the input of the integrator which begins ramping up or down, depending on the polarity of the first pulse from the comparator. When the voltage threshold of the comparator is reached, the output changes state. The cycle then repeats.

VCO

If an inversion in the feedback loop can be introduced and external energy applied at the right time, some interesting modifications of the previously described circuit will result — namely, a voltage-controlled oscillator. It works like this: the transistor inverts the output of the comparator. This voltage is presented to the inverting input of the integrator to begin the ramp cycle. When the comparator threshold is reached, the comparator changes state as before. This time, however, because the external applied voltage to the same inverting input is present, the amount of current available to the input is controlled by the external voltage and not by the feedback voltage. Once the component values are selected, the applied voltage, V_C, sets the frequency of oscillation because the current available to the integrating capacitor determines the charging time constant and, therefore, the frequency. The more positive the V_C, the more current is available and the higher the frequency of oscillation. The converse is also true with minor differences. It is interesting to note here that other low voltage op amps are not able to perform as well as the NE5230 in this circuit. This is because the NE5230 input voltage swing is able to exceed the rails by 250mV and still operate within its linear region. For a given set of conditions, then, the frequency range of the NE5230 is wider than conventional low voltage amplifiers. The frequency range of this circuit can also be changed by changing the value of the integrating capacitor. The smaller the value, the higher the frequency of oscillation for a given set of conditions.

The circuit in Figure 5 is the complete function generator. The measurements were taken at room temperature with only two AA batteries supplying the power. The outputs were loaded with 200Ω for the sine and triangular wave outputs and 50Ω for the square wave output. The output voltage for the sine wave was ±1V. The square wave output swung from rail-to-rail while the output voltage of the triangular wave varied with the input voltage, V_C. This was due, of course, to the voltage requirements of the transistor.

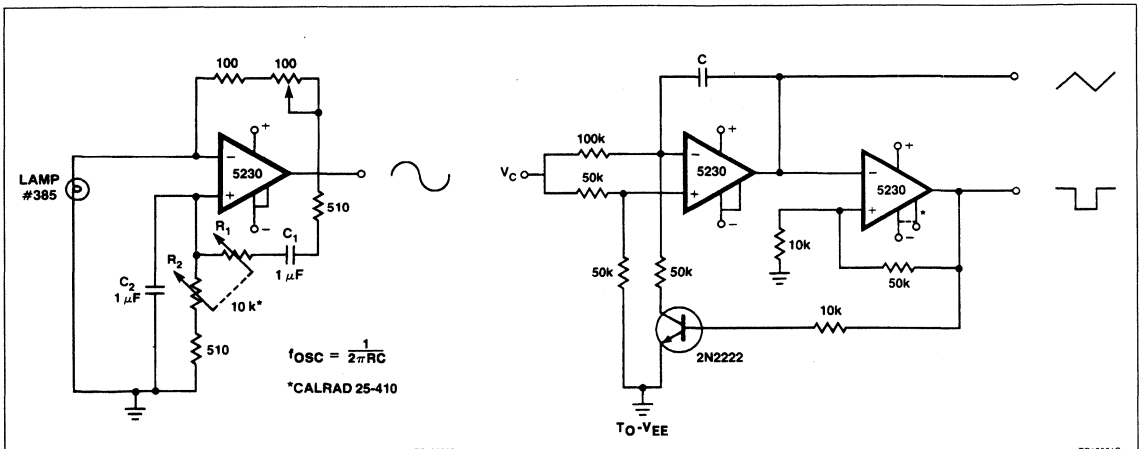


Figure 5. Gated Function Generator

PERFORMANCE

The distortion of the Wien Bridge output was 0.015% at the lowest frequency and 0.09% at the highest. Using the different capacitor values, the frequency was varied from minimum to maximum using the ganged 10kΩ pot. The frequencies could be changed from 20Hz to 2.5kHz. It was necessary to include a 500Ω resistor in the positive feedback loop to prevent the complete saturation of the amplifier when the potentiometer was in one extreme of its travel. In addition, a small adjustment resistor was used in the negative feedback loop to adjust the gain and to compensate for the slow response of the lamp.

The maximum frequency obtained by the VCO was 9.7kHz with a V_C of 1.65V with +1.4V batteries. The frequency varied from 8.4kHz to 1.6kHz with ±1V (V_C) applied with 0.001μF integrating capacitor.

CONCLUSIONS: FUNCTION GENERATOR

The thermal time constant of the lamp was an inhibiting factor in the low frequency operation of the Wien Bridge. A diode or a FET will work better here. Extreme ambient temperature will change the operating point of the lamp and, therefore, the output amplitude. Some non-symmetrical output was seen when operating the VCO at the lower frequencies. This was due to influence of the transistor as described previously.

BIAS ADJUST PIN

The NE5230 has another feature: the bias adjust pin. This pin is intended to control the power supply current. The power supply current is controlled by decreasing the internal bias current of the op amp. When the bias current is decreased, the transconductance (g_M) of the input stage is reduced; this, in turn, lowers the -3dB bandwidth. In addition, this pin can be used to turn the op amp on or off. If the voltage at the bias adjust pin is moved to 50mV above the voltage at the V_{EE} pin, the output becomes severely attenuated. The op amp, for all intents and purposes, is off. If, on the other hand, the bias adjust pin is moved to 50mV below the voltage at the V_{EE} pin, the bandwidth and slew rate are increased. The user should exercise care when doing this.

Utilized as a frequency-controlling element, this pin can be employed as a filter for upper band suppression. By carefully selecting the value, a single resistor connected to the $+V_{CC}$ pin can be used to determine the upper cutoff frequency of this filter. Values below 1.0MΩ should not be used because the total power supply current is too low for useful operation. The drive capability of the output is limited to approximately 100kΩ. This is an unconventional way to use this pin and this method of using the pin is not characterized. The user is cautioned to use care when employing the pin as outlined. The portion of the band which lends itself to this use is approximately the top half of the audio range. Below and beyond that range some problems become apparent. For the lower frequencies, the amplifier is operating far below its designed operating values and is not optimum in its performance. See Figure 6. For example, the drive capability of the amplifier is severely limited. The common-mode rejection ratio, power supply rejection ratio, as well as the input parameters go out of the data sheet-specified values at the higher frequencies; the slope of the suppression is less than desirable. At the frequencies in question, however, the method is unsurpassed in simplicity and ease of use.

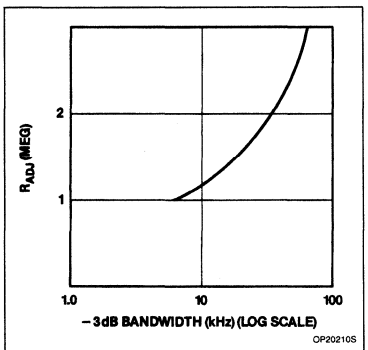


Figure 6. R_{ADJ} vs Bandwidth

AUDIO EQUALIZER

A useful application which takes advantage of the bias adjust pin is an audio equalizer circuit in Figure 7. An audio equalizer is a circuit which divides the audio frequency spectrum into equal parts. Adjustments of the frequency response of each band are possible. The equalizer circuit replaces a tone control in conventional audio equipment. Used in conjunction with a series capacitor filter, the NE5230 can be configured as a band pass filter. With one amplifier for each band, significant cost savings can be realized. The RC network in front of the circuit is used to remove the out-of-band response beyond the audio spectrum.

LOW FREQUENCY

These circuits are unity gain Sallen-Key filters. For the lower frequency band, the NE5230 can be configured to attenuate all but the lowest frequencies. Because the input parameters are compromised to the point where system performance is severely affected, the aforementioned unconventional method of upper band suppression is not used for the lowest frequency range of the equalizer. Instead, the upper end of this frequency band is attenuated using a second-order unity gain low-pass filter. The lower end is DC. The upper end cutoff was chosen to be about 1000Hz.

MIDBAND FREQUENCY

The midband frequencies can be selected as described earlier. The upper frequency of this band can be determined by connecting a resistor from Pin 5 to Pin 4. The value of this resistor can be determined by using the graph shown as Figure 6. The lower end of this frequency is selected by using a second-order high-pass filter with the upper band suppression done by using the bias adjust pin. The lower end frequency was chosen to be about 500Hz and the upper band was selected to be about 7.6kHz.

UPPER BAND FREQUENCY

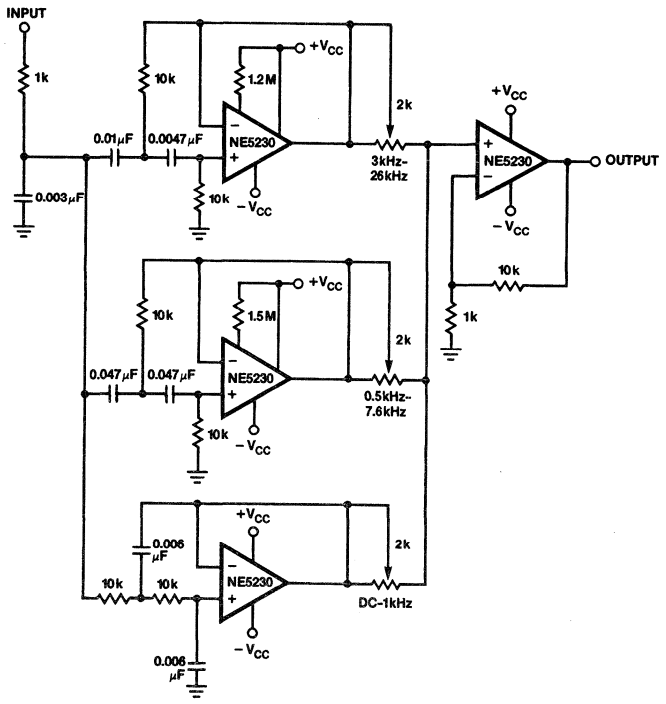
The upper band lower frequencies were tailored using the same filters. The upper band upper frequencies can be tailored by using the bias adjust pin in the unconventional manner described earlier. The lower end cutoff frequency was chosen to be about 3kHz and the upper end band was selected to be about 26kHz.

PERFORMANCE

Clearly one other band could have been used to bolster the response between the lowest and midband frequencies. See Figure 8. The outputs of each of the circuits were fed into a summing amplifier. The photograph shows the composite bandwidth of the three circuits. The potentiometers are intended to serve as an interfacing adjustment element and not as a gain adjustment. However, some interaction was seen when adjusting these potentiometers. Adjustment of one changes the relative attenuation of the other bands. Because of this, it may be desirable to include a buffer with gain for each band. Certainly more than three bands can be designed using this technique. In this case, cascading would be required to increase the slope of each band to provide better separation.

BRIDGE-TIED LOAD

One of the concerns found when using low voltage op amps is deliverable power to the load. Although the NE5230 has excellent drive capability, the Bridge-Tied Load (BTL) configuration can be used to increase the output power of the NE5230. Figure 9 shows the outputs arranged in a push-pull configuration; output power can thereby be doubled. This circuit finds applications in the audio field where low distortion power is critical. A 0.1%



NOTES:
All resistors in Ω
All capacitors in μF

Figure 7. Audio Equalizer

THD was measured with a 1kΩ load at 10kHz at room temperature. The single NE5230 amplifier is specified to drive a 10kΩ load. While a lighter load will improve the distortion figures, the intention here is to demonstrate the concept.

CONCLUSIONS

The NE5230 is a versatile precision, low voltage op amp. Its rail-to-rail capabilities coupled with its low voltage operating range and power supply current programmability make this op amp stand out among the competition. While other op amps have individual features which, on paper, seem to be better, the NE5230 shines on its combined merits. Its unique combination of features makes it the new leader in low voltage op amps.

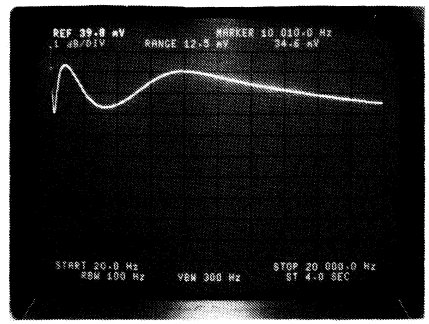
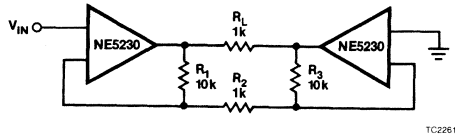


Figure 8. Equalizer Bandwidth



$$A_V = 2\frac{R_3}{R_2}\ ,\ R_1 = R_3\ ,\ 2\frac{R_3}{R_2} >> 1$$

Figure 9. Bridge-Tied Load

REFERENCES:

Lancaster, Don, Active Filter Cook Book, 1985

Markus, John, Modern Electronic Circuits Reference Manual, 1980

Pelser, F. A., Car Radio Audio Power Amplifiers up to 24 Watts with the TDA1015; Philips, Elcoma Applications Laboratory, Philips, The Netherlands.

Sheingold, Daniel H., Transducer Interfacing Handbook, 1980

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High frequency amplifiers

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NE/SA5204
Wide-band High-Frequency Amplifier

Product Specification

DESCRIPTION

The NE/SA5204 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ± 0.5dB from DC to 200MHz. The −3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204 operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204 is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC-coupling capacitors because the NE/SA5204 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

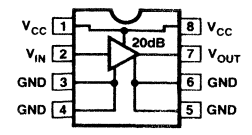
The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204s in series as required, without any degradation in amplifier stability.

FEATURES

- **Bandwidth (min.)**
  200 MHz, ± 0.5dB
  350 MHz, − 3dB
- **20dB insertion gain**
- **4.8dB (6dB) noise figure**
  Z_O = 75Ω (Z_O = 50Ω)
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface-mount package available**
- **Cascadable**

PIN CONFIGURATION

N, D Packages



TOP VIEW

CD12760S

APPLICATIONS

- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broadband LANs**
- **Networks**
- **Modems**
- **Mobile radio**
- **Security systems**
- **Telecommunications**

ORDERING INFORMATION

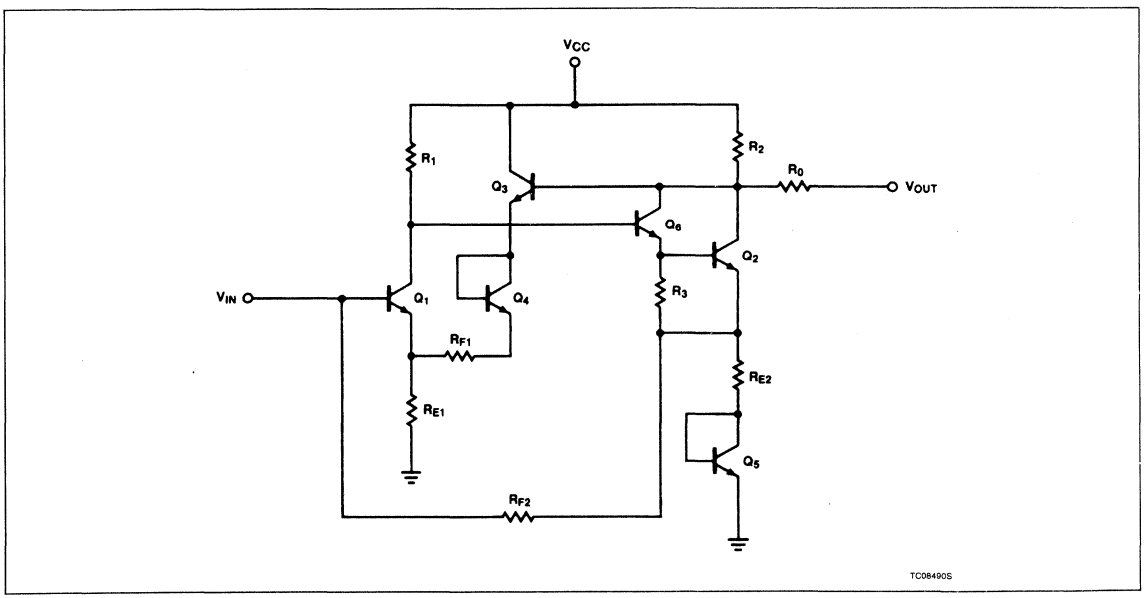
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5204N
	−40 to +85°C	SA5204N
8-Pin Plastic SO package	0 to +70°C	NE5204D
	−40 to +85°C	SA5204D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range NE grade SA grade	 0 to +70 −40 to +85	 °C °C
P_{DMAX}	Maximum power dissipation[1, 2] T_A = 25°C (still-air) N package D package	 1160 780	 mW mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C.
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	24	31	mA
S21	Insertion gain	f = 100MHz, over temperature	16	19	22	dB
S11	Input return loss	f = 100MHz		25		dB
		DC -550MHz		12		dB
S22	Output return loss	f = 100MHz		27		dB
		DC -550MHz		12		dB
S12	Isolation	f = 100MHz		-25		dB
		DC -550MHz		-18		dB
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	-3dB	350	550		MHz
	Noise figure (75Ω)	f = 100MHz		4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0		dB
	Saturated output power	f = 100MHz		+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24		dBm
t_R	Rise time			5		ps
	Propagation delay			5		ps

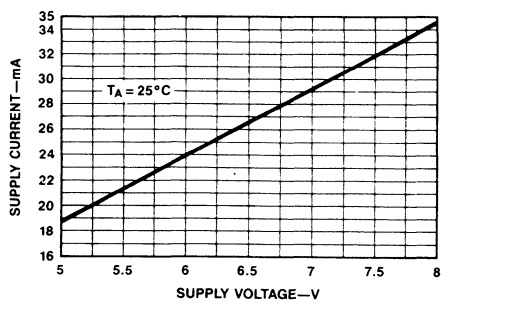


Figure 1. Supply Current vs Supply Voltage

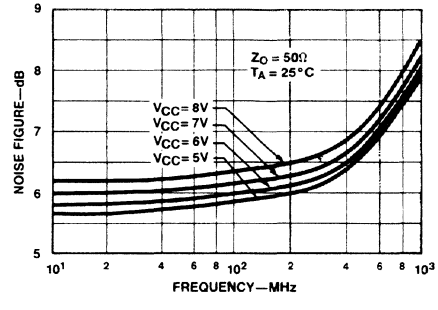


Figure 2. Noise Figure vs Frequency

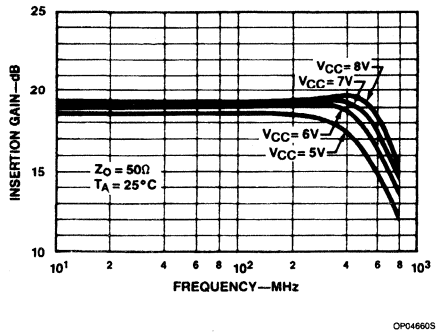


Figure 3. Insertion Gain vs Frequency (S_{21})

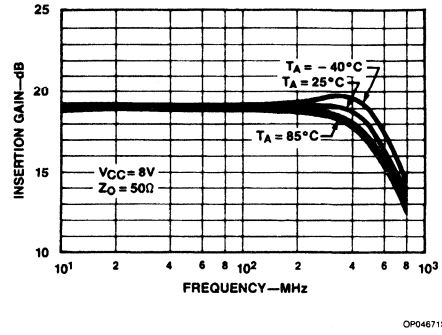


Figure 4. Insertion Gain vs Frequency (S_{21})

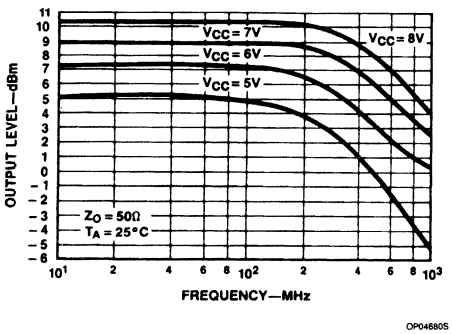


Figure 5. Saturated Output Power vs Frequency

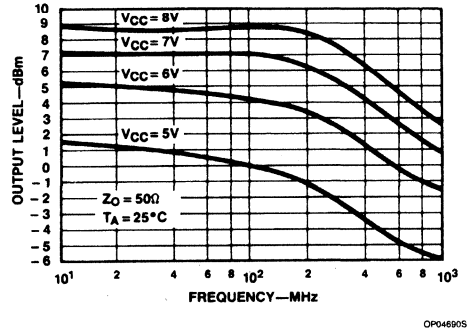


Figure 6. 1dB Gain Compression vs Frequency

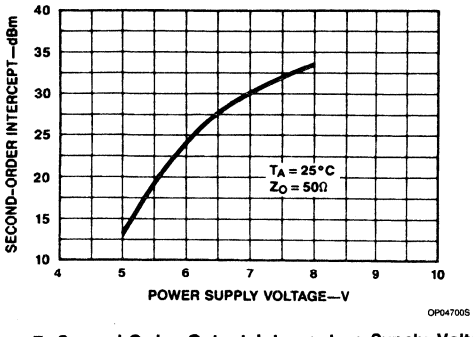


Figure 7. Second-Order Output Intercept vs Supply Voltage

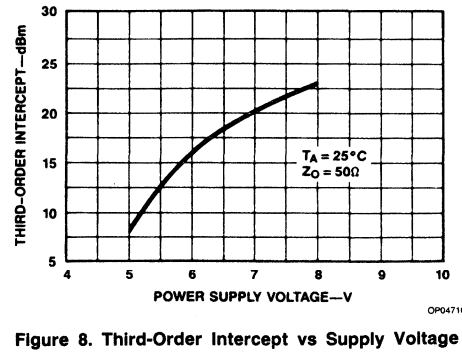


Figure 8. Third-Order Intercept vs Supply Voltage

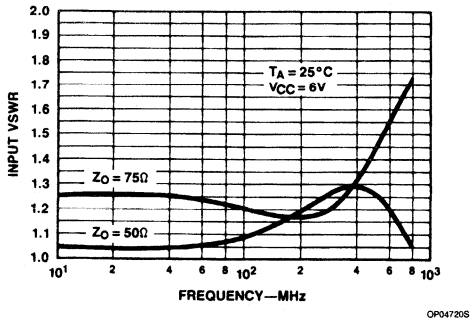


Figure 9. Input VSWR vs Frequency

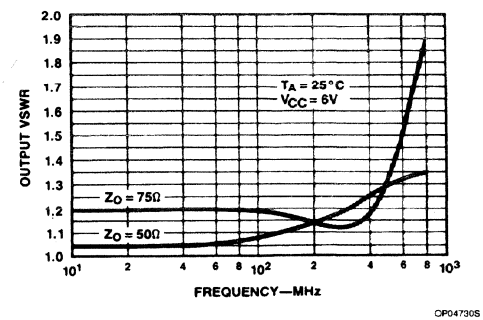


Figure 10. Output VSWR vs Frequency

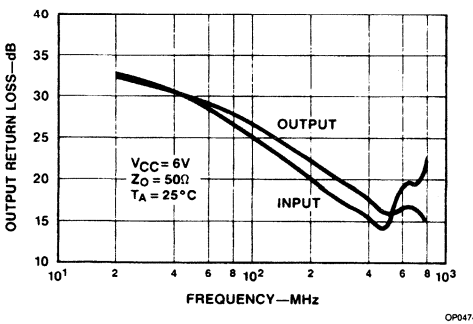


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

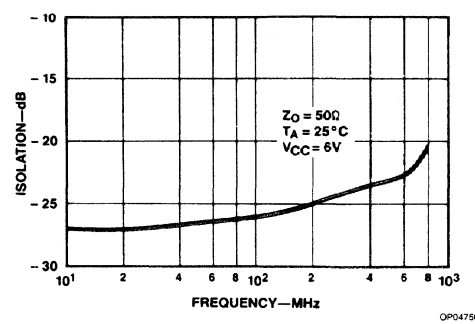


Figure 12. Isolation vs Frequency (S_{12})

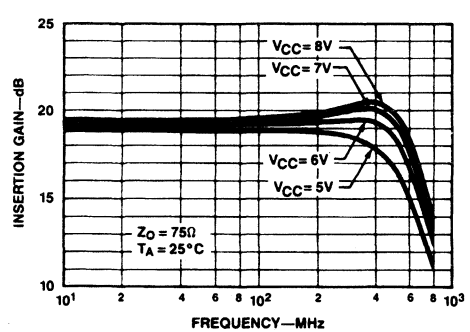


Figure 13. Insertion Gain vs Frequency (S_{21})

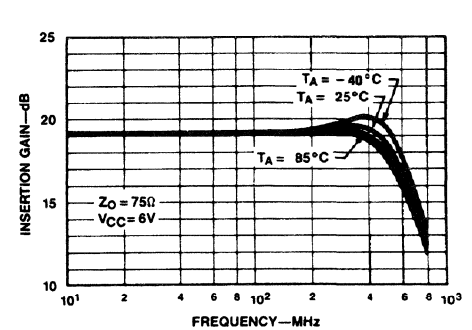


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10\text{Log}\left\{1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_0}\right\} \text{dB} \quad (2)$$

where I_{C1} = 5.5mA, R_{E1} = 12Ω, r_b = 130Ω, KT/q = 26mV at 25°C and R_0 = 50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\,R_{E1} \quad (3)$$

where R_{E1} = 12Ω, V_{BE} = 0.8V, I_{C1} = 5mA and I_{C3} = 7mA (currents rated at V_{CC} = 6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of R_{F1} = 140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \quad (4)$$

where V_{CC} = 6V, R_2 = 225Ω, I_{C2} = 7mA and I_{C6} = 5mA.

From here, it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

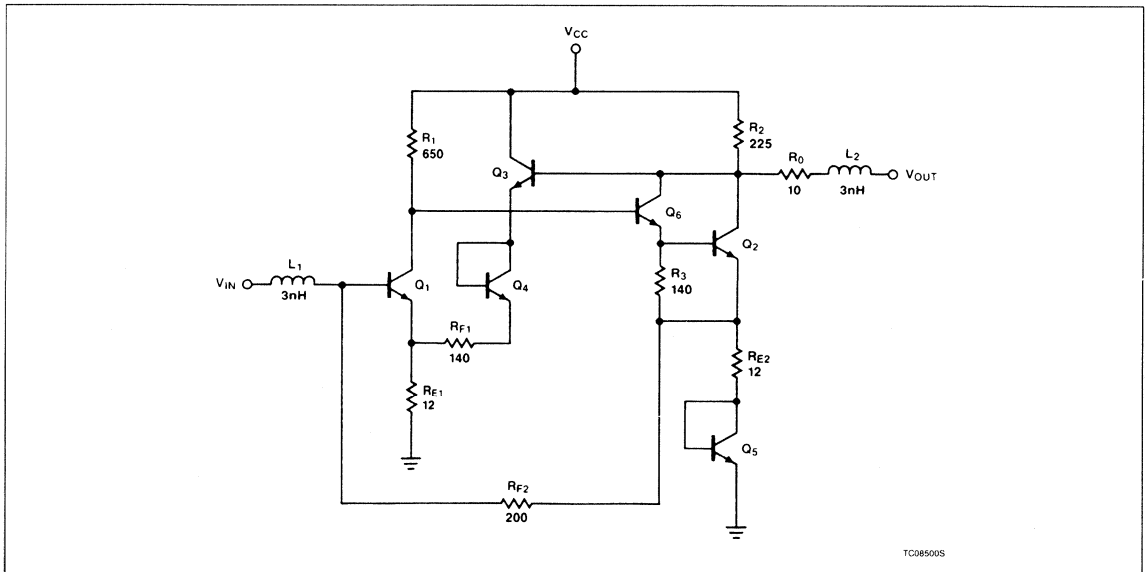


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at $V_{CC} = 6V$, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

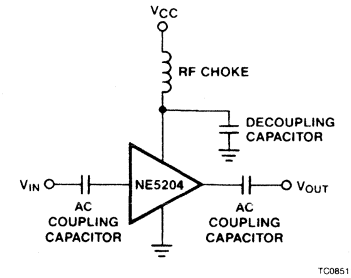
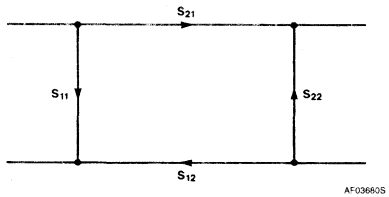


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

SCATTERING PARAMETERS

The primary specifications for the NE5204 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

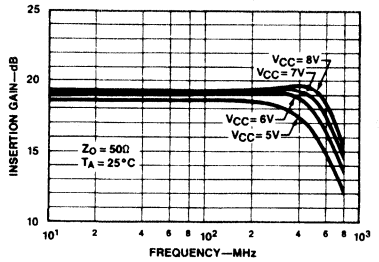
$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

AF03690S

b.

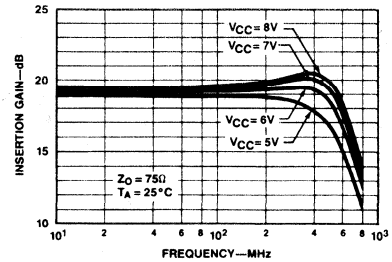
Figure 17

50Ω System

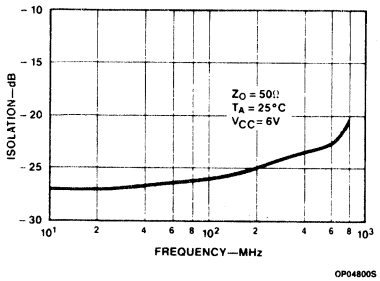


a. Insertion Gain vs Frequency (S_{21})

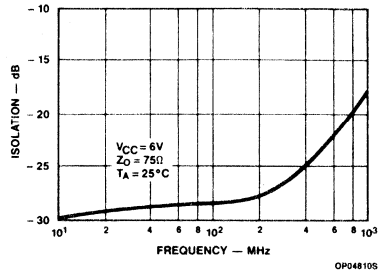
75Ω System



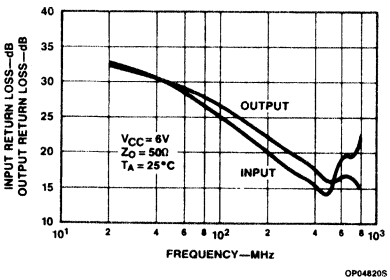
b. Insertion Gain vs Frequency (S_{21})



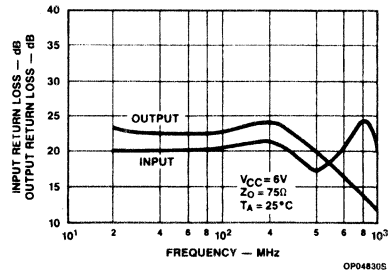
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency



f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18

Actual S-parameter measurements, using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B), are shown in Figure 18.

Values for Figure 20 are measured and specified in the data sheet to ease adaptation and comparison of the NE5204 to other high-frequency amplifiers. The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE5204

$$P_{IN} = \frac{V_{IN}^2}{Z_D} \quad \boxed{\text{NE5204}\ Z_D} \quad P_{OUT} = \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain
V_I = Insertion Voltage Gain

Measured value for the NE5204 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10\text{Log}\ |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20\text{Log}\ S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing-wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = S_{11}dB
$S_{11}\text{dB} = 20\text{Log}\ |S_{11}|$

OUTPUT RETURN LOSS = S_{22}dB
$S_{22}\text{dB} = 20\text{Log}\ |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leq 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leq 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to non-linearities in the amplifier, an indication of the point of transition between small-signal operation and the large-signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

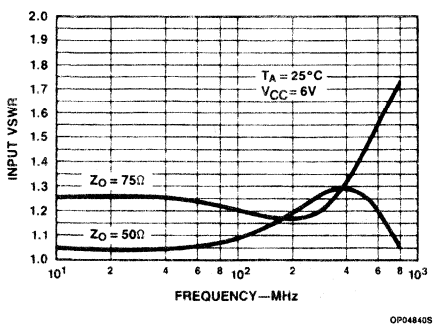
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second-order IMR is equal to the difference between the second-order intercept and the fundamental output level. The third-order IMR is equal to twice the difference between the third-order intercept and the fundamental output level. These are expressed as:

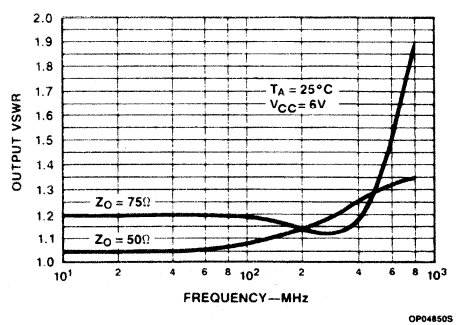
$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second- and third-order output intercepts in dBm, and IMR_2 and IMR_3 are the second- and third- order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small-signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point, the intermodulation products no longer follow the straight-line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be care-



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ful, however, not to select levels which are too low, because the test equipment may not be able to recover the signal from the noise. For the NE5204, an output level of −10.5dBm was chosen with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers*; by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985, published by John Wiley & Sons, Inc.

S-Parameter Techniques for Faster, More Accurate Network Design, HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

S-Parameter Design, HP App Note 154, 1972.

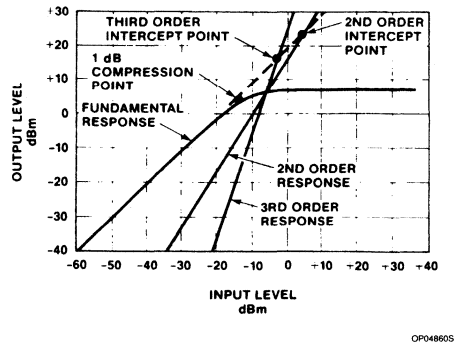


Figure 20

NE/SA/SE5205
Wide-band High-Frequency Amplifier

Product Specification

DESCRIPTION

The NE/SA/SE5205 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ± 0.5dB from DC to 450MHz, and the −3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205 operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205 solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the −3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the −3dB frequency to 600MHz. The Cerdip package is hermetically sealed, and can operate over the full −55°C to +125°C range.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205s in series as required, without any degradation in amplifier stability.

FEATURES

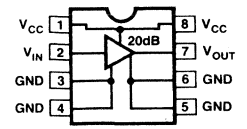
- **600MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface mount package available**
- **MIL-STD processing available**

APPLICATIONS

- **75Ω cable TV decoder boxes**
- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broad-band LANs**
- **Fiber-optics**
- **Modems**
- **Mobile radio**
- **Security systems**
- **Telecommunications**

PIN CONFIGURATIONS

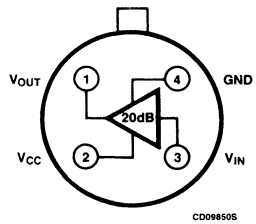
N, FE, D Packages



TOP VIEW

CD12760S

EC Package



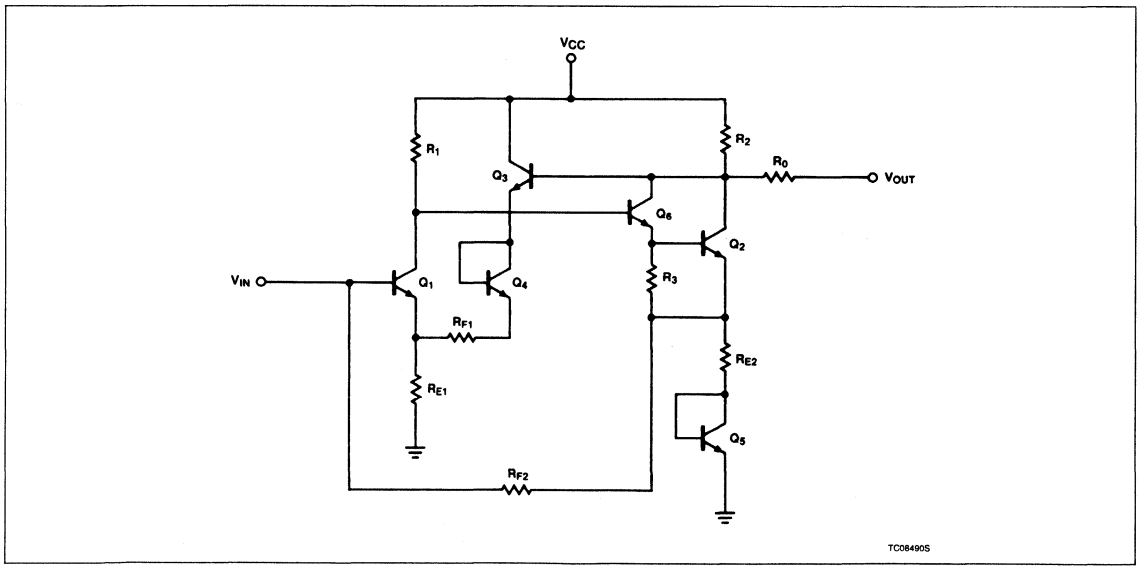
CD09850S

NOTE:
Tab denotes Pin 1.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5205D
4-Pin Metal can	0 to +70°C	NE5205EC
8-Pin Cerdip	0 to +70°C	NE5205FE
8-Pin Plastic DIP	0 to +70°C	NE5205N
8-Pin Plastic SO	−40°C to +85°C	SA5205D
8-Pin Plastic DIP	−40°C to +85°C	SA5205N
8-Pin Cerdip	−40°C to +85°C	SA5205FE
8-Pin Cerdip	−55°C to +125°C	SE5205FE
8-Pin Plastic DIP	−55°C to +125°C	SE5205N

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	−40 to +85	°C
	SE grade	−55 to +125	°C
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[1, 2]		
	FE package	780	mW
	N package	1160	mW
	D package	780	mW
	EC package	1250	mW

NOTES:
1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
   EC package at 10.0mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS

at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Operating supply voltage range	Over temperature	5 5		6.5 6.5	5 5		8 8	V V
I_{CC}	Supply current	Over temperature	20 19	24	30 31	20 19	24	30 31	mA mA
S21	Insertion gain	f = 100MHz Over temperature	17 16.5	19	21 21.5	17 16.5	19	21 21.5	dB
S11	Input return loss	f = 100MHz D, N, FE		25			25		dB
		DC − f_{MAX} D, N, FE	12			12			dB
S11	Input return loss	f = 100MHz EC package					24		dB
		DC − f_{MAX} EC				10			dB
S22	Output return loss	f = 100MHz D, N, FE		27			27		dB
		DC − f_{MAX}	12			12			dB
S22	Output return loss	f = 100MHz EC package					26		dB
		DC − F_{MAX}				10			dB
S12	Isolation	f = 100MHz		−25			−25		dB
		DC − f_{MAX}	−18			−18			dB
t_R	Rise time			5			5		ps
	Propagation delay			5			5		ps

DC ELECTRICAL CHARACTERISTICS at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth	±0.5dB D, N					450		MHz
f_{MAX}	Bandwidth	±0.5dB EC					500		MHz
f_{MAX}	Bandwidth	±0.5dB FE		300			300		MHz
f_{MAX}	Bandwidth	-3dB D, N				550			MHz
f_{MAX}	Bandwidth	-3dB EC				600			MHz
f_{MAX}	Bandwidth	-3dB FE	400			400			MHz
	Noise figure (75Ω)	f = 100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0			6.0		dB
	Saturated output power	f = 100MHz		+7.0			+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24			+24		dBm

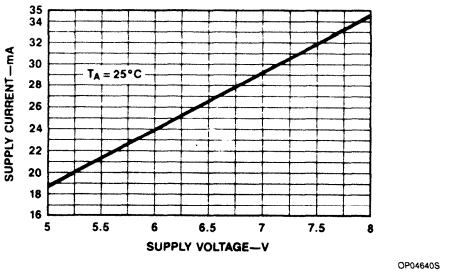


Figure 1. Supply Current vs Supply Voltage

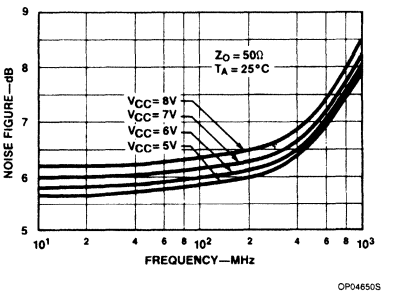


Figure 2. Noise Figure vs Frequency

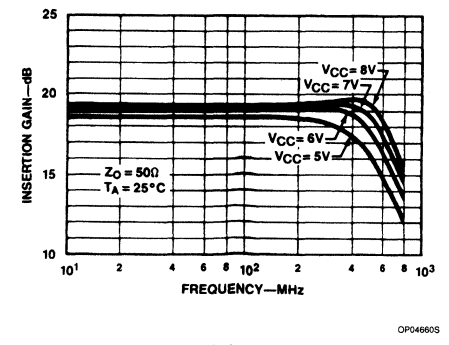


Figure 3. Insertion Gain vs Frequency (S_{21})

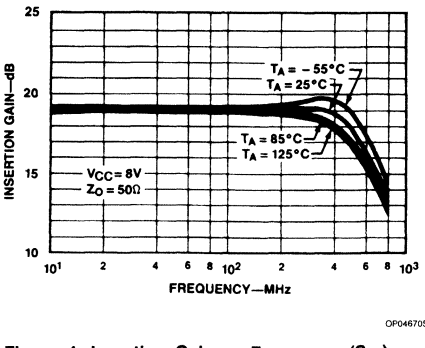


Figure 4. Insertion Gain vs Frequency (S_{21})

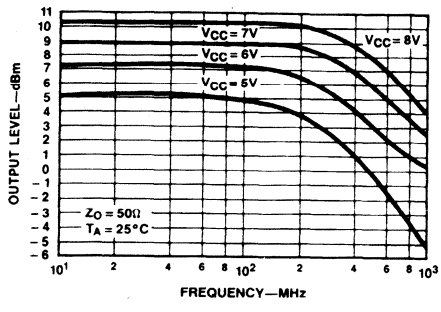


Figure 5. Saturated Output Power vs Frequency

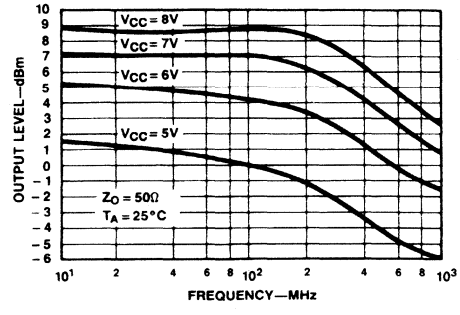


Figure 6. 1dB Gain Compression vs Frequency

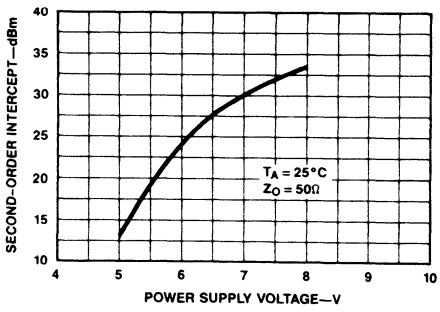


Figure 7. Second-Order Output Intercept vs Supply Voltage

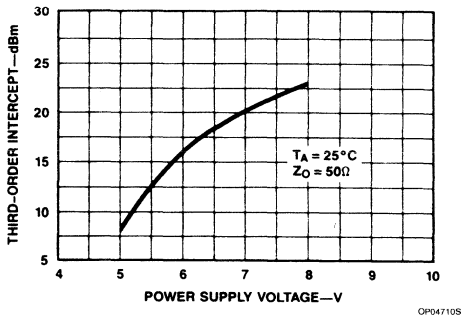


Figure 8. Third-Order Intercept vs Supply Voltage

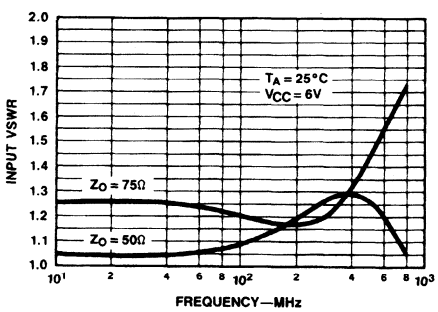


Figure 9. Input VSWR vs Frequency

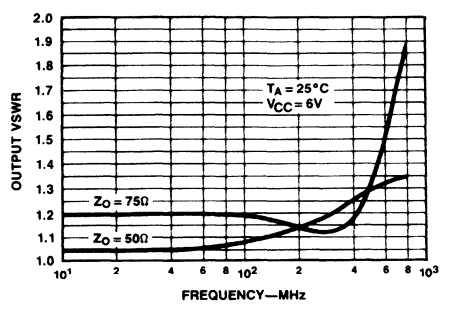


Figure 10. Output VSWR vs Frequency

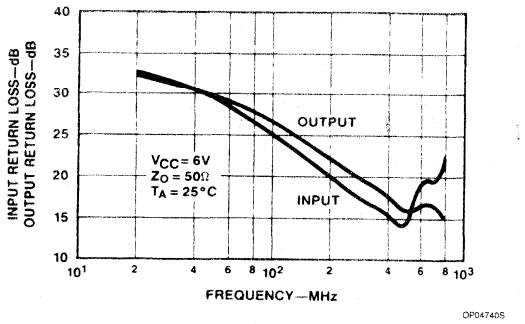


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

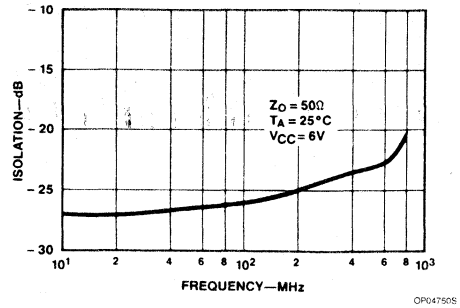


Figure 12. Isolation vs Frequency (S_{12})

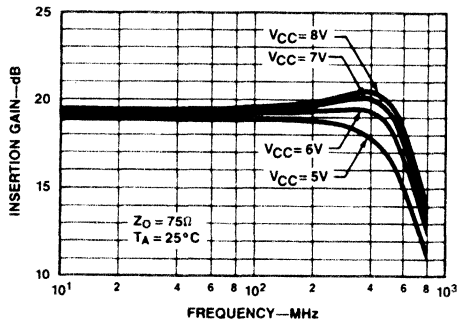


Figure 13. Insertion Gain vs Frequency (S_{21})

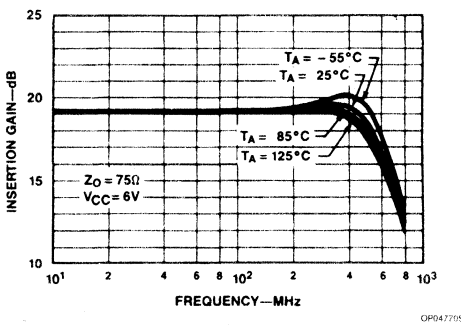


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10 \text{ Log} \left\{ 1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2q I_{C1}} \right]}{R_0} \right\} \text{ dB} \quad (2)$$

where $I_{C1} = 5.5mA$, $R_{E1} = 12\Omega$, $r_b = 130\Omega$, $KT/q = 26mV$ at 25°C and $R_0 = 50$ for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\ R_{E1}$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8V$, $I_{C1} = 5mA$ and $I_{C3} = 7mA$ (currents rated at $V_{CC} = 6V$).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of $R_{F1} = 140\Omega$ is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \quad (4)$$

where $V_{CC} = 6V$, $R_2 = 225\Omega$, $I_{C2} = 7mA$ and $I_{C6} = 5mA$.

From here it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D and EC package body against the PC board plane.

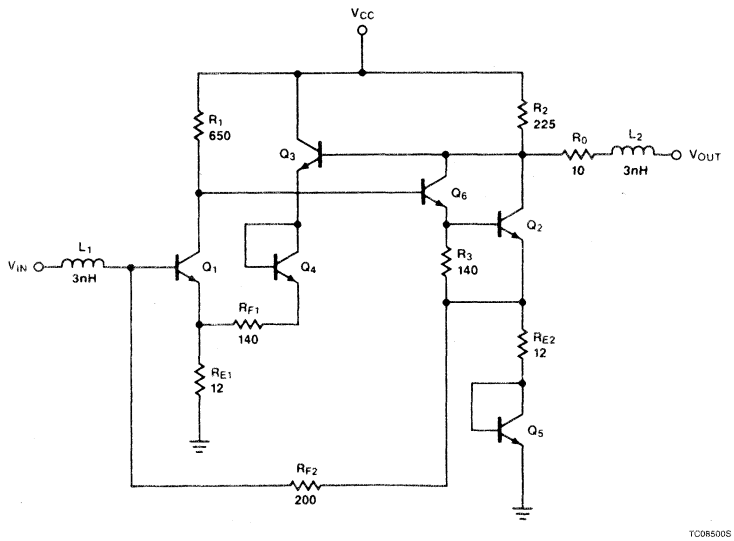


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). In addition, if the EC package is used, the case should be soldered to the ground plane. The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at V_{CC} = 6V, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

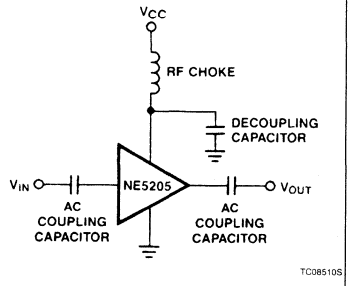


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

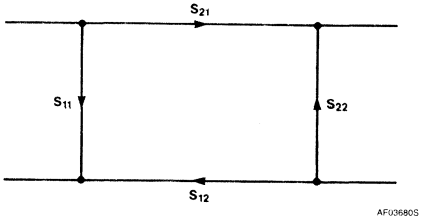


Figure 17a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

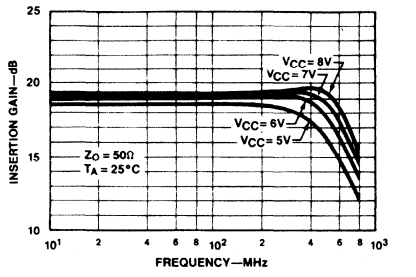
AF03690S

Figure 17b

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

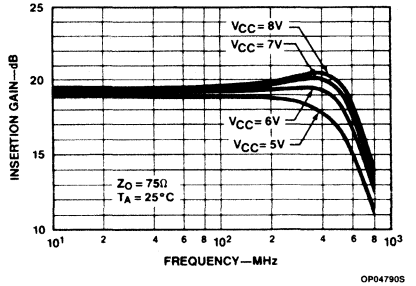
Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205 to other high-frequency amplifiers.

50Ω System

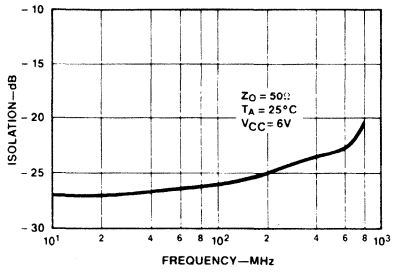


a. Insertion Gain vs Frequency (S_{21})

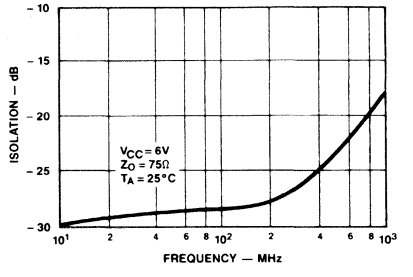
75Ω System



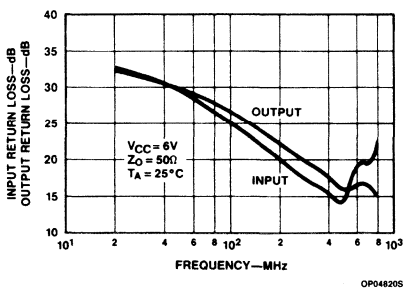
b. Insertion Gain vs Frequency (S_{21})



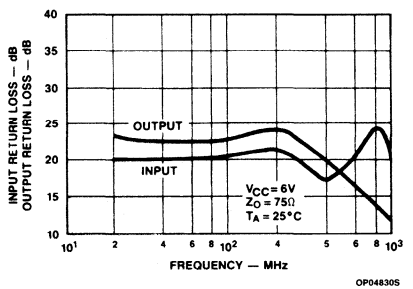
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

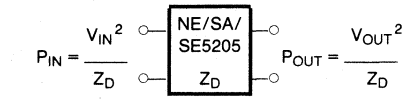


f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE/SA/SE5205



$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain

V_I = Insertion Voltage Gain

Measured value for the NE/SA/SE5205 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20dB$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20dB$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20dB$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = $S_{11}dB$

$S_{11}dB = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS = $S_{22}dB$

$S_{22}dB = 20 \text{ Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leq 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leq 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

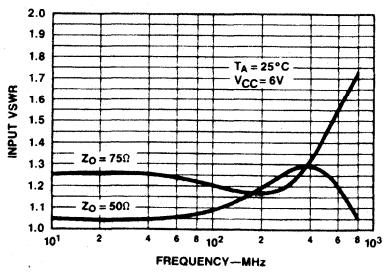
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

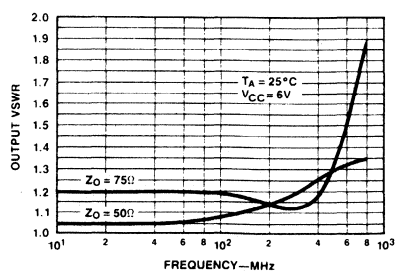
$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205 we have chosen an output level of −10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers* by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

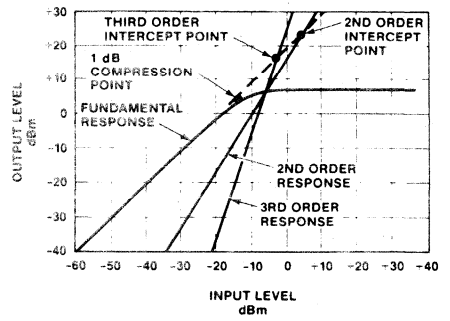


Figure 20

Video amplifiers

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NE5539	ultra high frequency operational amplifier	253
NE5592	video amplifier	261
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SA592	video amplifier	267
SE5539	ultra high frequency operational amplifier	253
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NE/SE5539
High Frequency Operational Amplifier

Product Specification

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

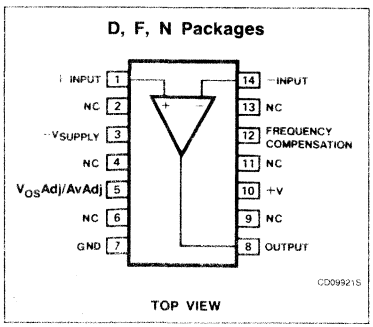
FEATURES

- **Bandwidth**
  - **Unity gain – 350MHz**
  - **Full power – 48MHz**
  - **GBW – 1.2 GHz at 17dB**
- **Slew rate: 600/Vμs**
- **A_{VOL}: 52dB typical**
- **Low noise – 4nV/$\sqrt{Hz}$ typical**
- **MIL-STD processing available**

APPLICATIONS

- **High speed datacomm**
- **Video monitors & TV**
- **Satellite communications**
- **Image processing**
- **RF instrumentation & oscillators**
- **Magnetic storage**
- **Military communications**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5539N
14-Pin Plastic SO	0 to +70°C	NE5539D
14-Pin Cerdip	0 to +70°C	NE5539F
14-Pin Plastic DIP	–55°C to +125°C	SE5539N
14-Pin Cerdip	–55°C to +125°C	SE5539F

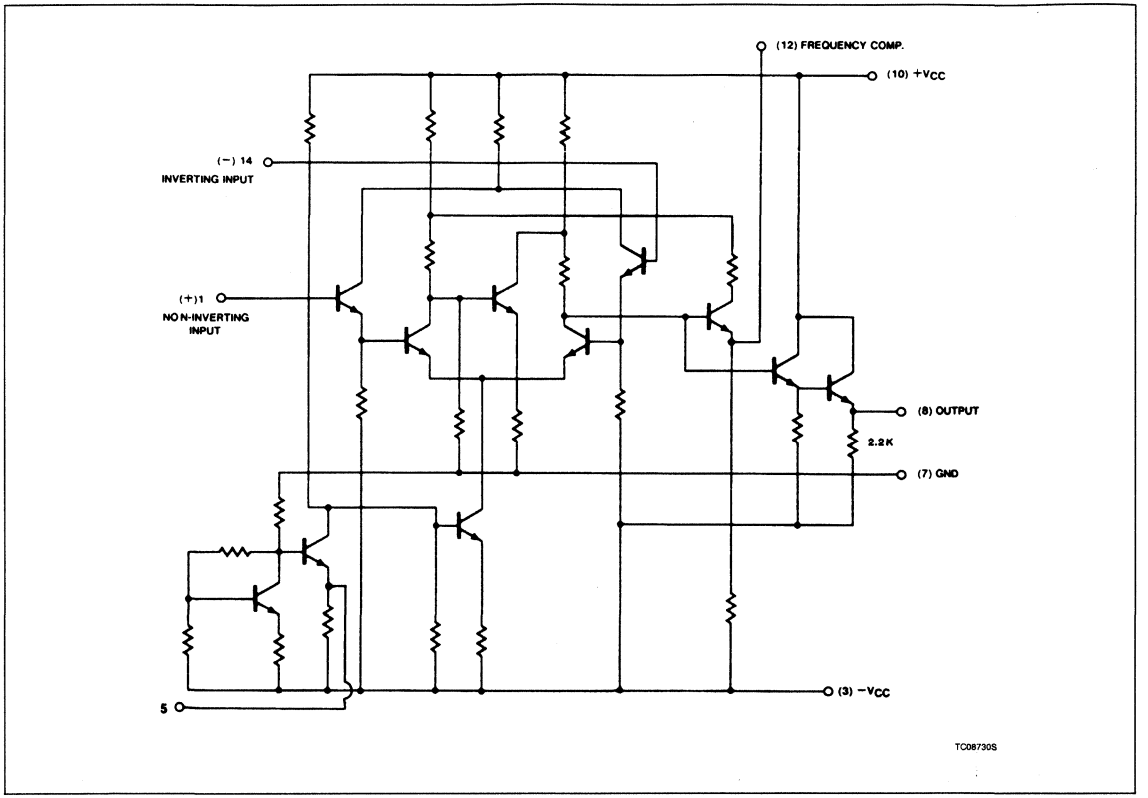
ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±12	V
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2]		
	F package	1.17	W
	N package	1.45	W
	D package	0.99	W
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	–55 to +125	°C
T_{SOLD}	Lead temperature (10sec max)	300	°C

NOTES:

1. Differential input voltage should not exceed 0.25V to prevent excessive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3 mW/°C
   N package at 11.6 mW/°C
   D package at 7.9 mW/°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
	$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Input offset current		Over temp		0.1	3				µA
			$T_A = 25°C$		0.1	1			2	
	$\Delta I_{OS}/\Delta T$				0.5			0.5		nA/°C
I_B	Input bias current		Over temp		6	25				µA
			$T_A = 25°C$		5	13		5	20	
	$\Delta I_B/\Delta T$				10			10		nA/°C
CMRR	Common-mode rejection ratio	F = 1kHz, $R_S = 100\Omega$, $V_{CM} \pm 1.7V$		70	80		70	80		dB
			Over temp	70	80					dB
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			NE5539			UNIT
					Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$		+Swing				+2.3	+2.7		V
				−Swing				−1.7	−2.2		
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ to GND	Over temp	+Swing	+2.3	+3.0					V
				−Swing	−1.5	−2.1					
			$T_A = 25°C$	+Swing	+2.5	+3.1					V
				−Swing	−2.0	−2.7					
$I_{CC}+$	Positive supply current	$V_O = 0$, $R_1 = \infty$		Over temp		14	18				mA
				$T_A = 25°C$		14	17		14	18	
$I_{CC}-$	Negative supply current	$V_O = 0$, $R_1 = \infty$		Over temp		11	15				mA
				$T_A = 25°C$		11	14		11	15	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000				μV/V
				$T_A = 25°C$					200	1000	
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$						47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2\Omega$ to GND									dB
				$T_A = 25°C$				47	52	57	
A_{VOL}	Large signal voltage gain	$V_O = +2.5V, -2.0V$ $R_L = 2k\Omega$ to GND		Over temp	46		60				dB
				$T_A = 25°C$	48	53	58				

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			UNIT
					Min	Typ	Max	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				$T_A = 25°C$		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	μA
				$T_A = 25°C$		0.1	1	
I_B	Input bias current			Over temp		5	20	μA
				$T_A = 25°C$		4	10	
CMRR	Common-mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85		dB
$I_{CC}+$	Positive supply current			Over temp		11	14	mA
				$T_A = 25°C$		11	13	
$I_{CC}-$	Negative supply current			Over temp		8	11	mA
				$T_A = 25°C$		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	μV/V
				$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+Swing	+1.4	+2.0		V
				−Swing	−1.1	−1.7		
			$T_A = 25°C$	+Swing	+1.5	+2.0		
				−Swing	−1.4	−1.8		

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 470Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$, $V_0 = 0.1\ V_{P-P}$		1200			1200		MHz
	Small-signal bandwidth	$A_{CL} = 2$, $R_L = 150\Omega$[1]		110			110		MHz
t_S	Settling time	$A_{CL} = 2$, $R_L = 150\Omega$[1]		15			15		ns
SR	Slew rate	$A_{CL} = 2$, $R_L = 150\Omega$[1]		600			600		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$, $R_L = 150\Omega$[1]		7			7		ns
	Full power response	$A_{CL} = 2$, $R_L = 150\Omega$[1]		48			48		MHz
	Full power response	$A_V = 7$, $R_L = 150\Omega$[1]		20			20		MHz
	Input noise voltage	$R_S = 50\Omega$, 1MHz		4			4		$nV/\sqrt{Hz}$
	Input noise current	1MHz		6			6		$pA/\sqrt{Hz}$

NOTE:
1. External compensation.

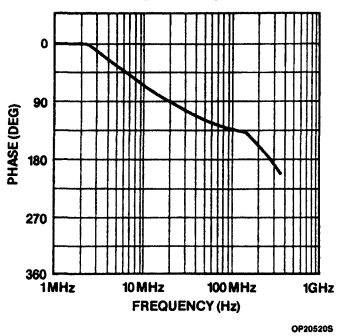
AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNIT
			Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$		700		MHz
	Small-signal bandwidth	$A_{CL} = 2$[1]		120		MHz
t_S	Settling time	$A_{CL} = 2$[1]		23		ns
SR	Slew rate	$A_{CL} = 2$[1]		330		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$[1]		4.5		ns
	Full power response	$A_{CL} = 2$[1]		20		MHz

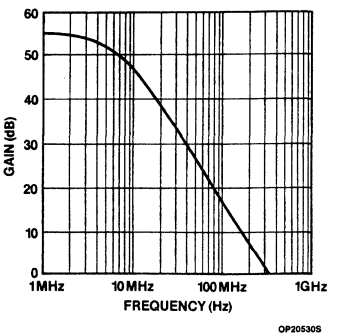
NOTE:
1. External compensation.

TYPICAL PERFORMANCE CURVES

NE5539 Open-Loop Phase

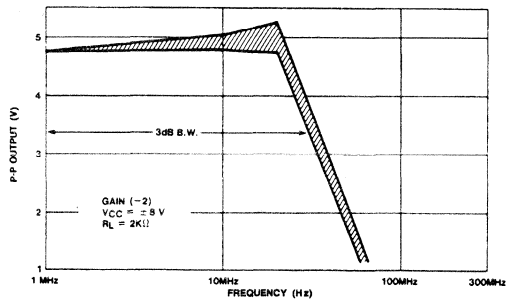


NE5539 Open-Loop Gain



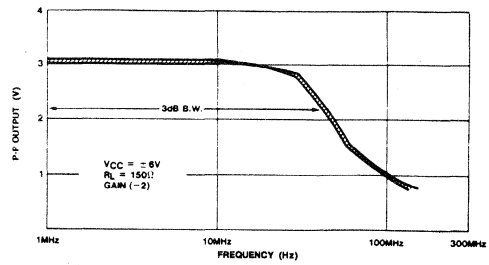
TYPICAL PERFORMANCE CURVES (Continued)

Power Bandwidth (SE)



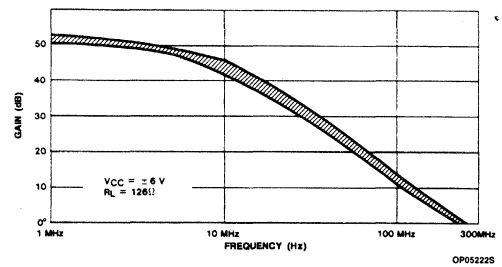
OP05202S

Power Bandwidth (NE)



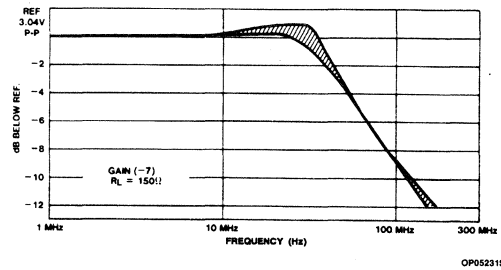
OP05212S

SE5539 Open-Loop Gain vs Frequency



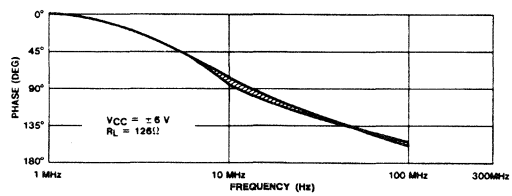
OP05222S

Power Bandwidth

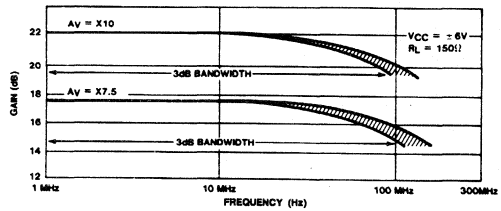


OP05231S

SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency



OP05251S

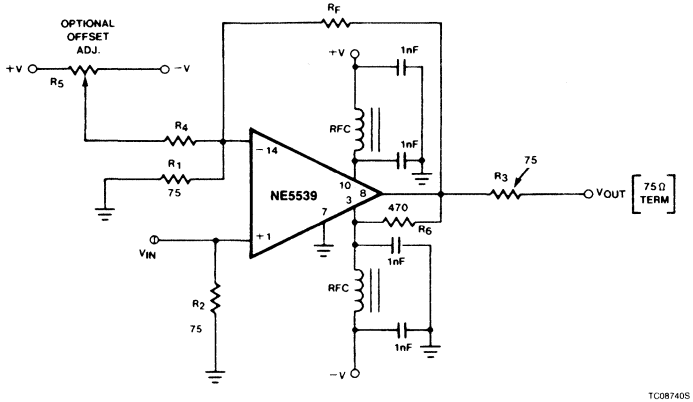
NOTE

Indicates typical distribution $-55°C \leq T_A \leq 125°C$

OP05241S

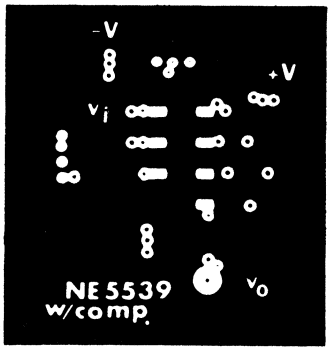
CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the physical circuit layout is extremely critical. Breadboarding is not recommended. A double-sided copper-clad printed cirucit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.

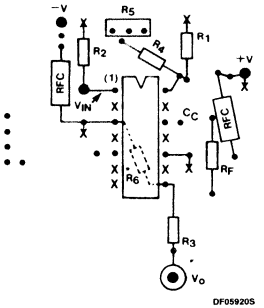


NOTES:
R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36k 5% CARBON
R_5 = 20k TRIMPOT (CERMET)
R_F = 1.5k (28dB GAIN)
R_6 = 470Ω 5% CARBON
RFC 3T # 26 BUSS WIRE ON FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

Top Plane Copper[1] (Component Side)

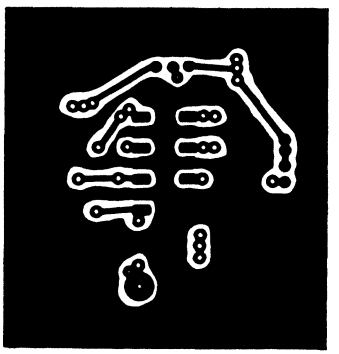


Component Side (Component Layout)



NOTES:
(X) indicates ground connection to top plane.
*R_6 is on bottom side.

Bottom Plane Copper[1]



NOTE:
1. Bond edges of top and bottom ground plane copper.

Figure 1. 28dB Non-Inverting Amp Sample PC Layout

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in Figure 2 along with vector-scope[1] photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of approximately 10 (20dB).

NOTE:

1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.

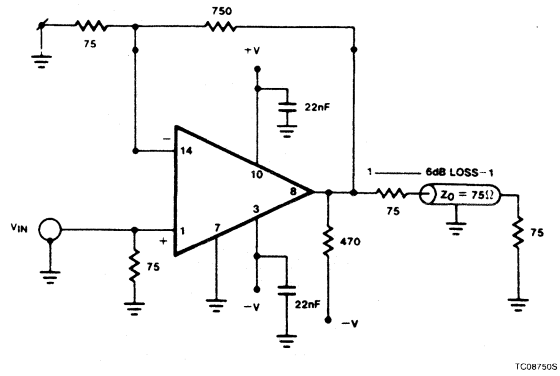


Figure 2. NE5539 Video Amplifier

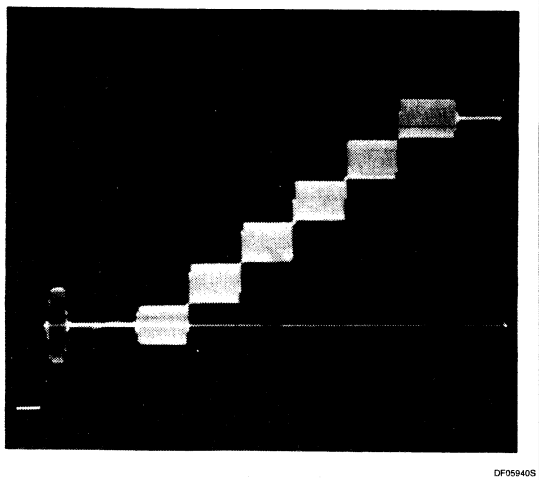


Figure 3. Input Signal

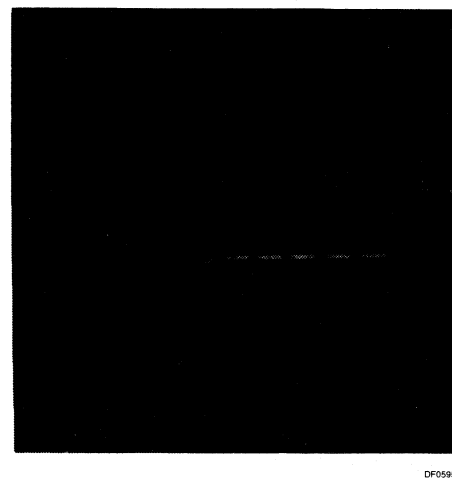


Figure 4. Differential Gain < 0.5%

NOTE:

Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

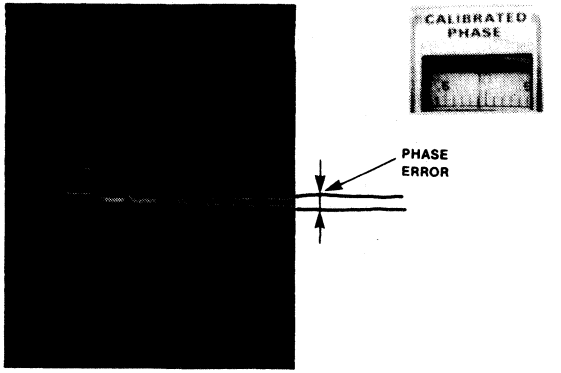


Figure 5. Differential Phase +0.1°

APPLICATIONS

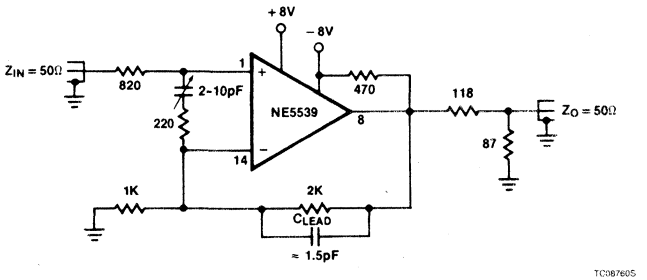


Figure 6. Non-Inverting Follower

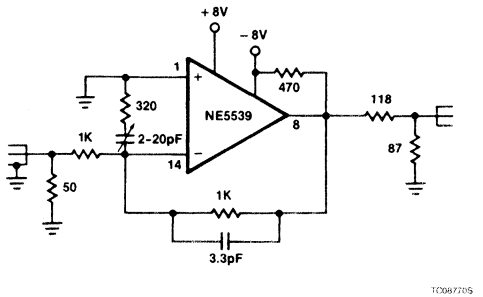


Figure 7. Inverting Follower

NE5592
Video Amplifier

Product Specification

DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers a fixed gain of 400 without external components and an adjustable gain from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

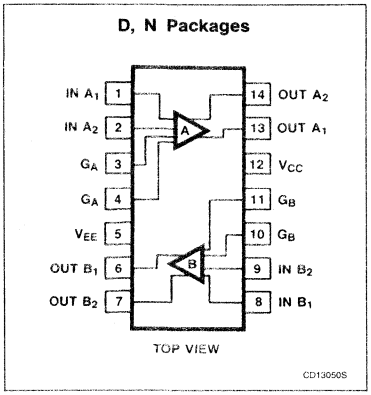
FEATURES

- **110MHz unity gain bandwidth**
- **Adjustable gain from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

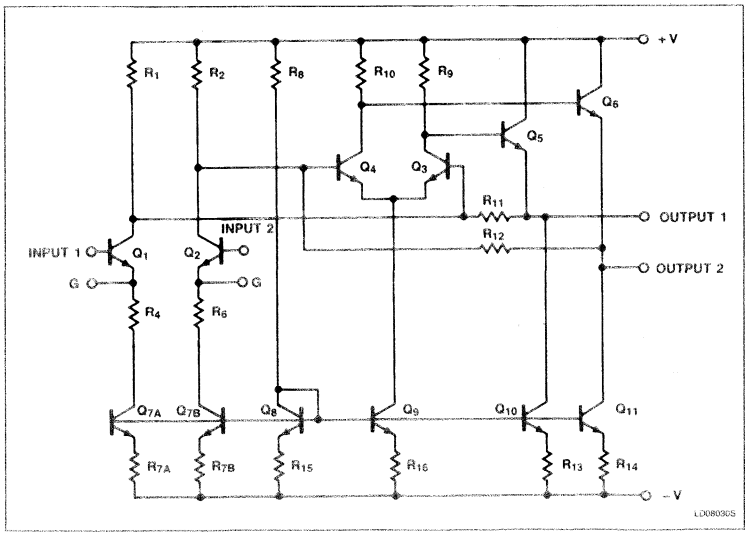
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to 70°C	NE5592N
14-Pin SO package	0 to 70°C	NE5592D

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common mode Input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range NE5592	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, $T_A = 25°C$ (still air)[1] D package N package	 1.03 1.48	 W W

NOTE:
1. Derate above 25°C at the following rates:
   D package 8.3mW/°C
   N package 11.9mW/°C

DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltage is $V_S = \pm 6.0V$, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	400	480	600	V/V
R_{IN}	Input resistance		3	14		kΩ
C_{IN}	Input capacitance			2.5		pF
I_{OS}	Input offset current			0.3	3	μA
I_{BIAS}	Input bias current			5	20	μA
	Input noise voltage	BW 1kHz to 10MHz		4		$nV/\sqrt{Hz}$
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	$V_{CM} \pm 1V$, f < 100kHz $V_{CM} \pm 1V$, f = 5MHz	60	93 87		dB dB
PSRR	Supply voltage rejection ratio	$\Delta V_S = \pm 0.5V$	50	85		dB
	Channel separation	$V_{OUT} = 1V_{P-P}$; f = 100kHz (output referenced) $R_L = 1k\Omega$	65	70		dB
V_{OS}	Output offset voltage gain select pins open	$R_L = \infty$ $R_L = \infty$		0.5 0.25	1.5 0.75	V V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	3.1	3.4	V
V_{OUT}	Output differential voltage swing	$R_L = 2k\Omega$	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current (total for both sides)	$R_L = \infty$		35	44	mA

DC ELECTRICAL CHARACTERISTICS $V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leq T_A \leq 70°C$, unless otherwise specified. Recommended operating supply voltage is $V_S = \pm 6.0V$, and gain select pins are connected together.

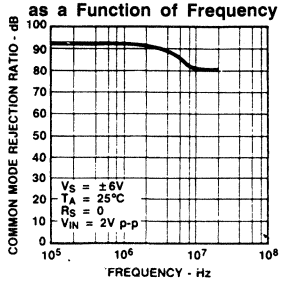
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	350	430	600	V/V
R_{IN}	Input resistance		1	11		kΩ
I_{OS}	Input offset current				5	μA
I_{BIAS}	Input bias current				30	μA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	$V_{CM} \pm 1V$, $f < 100kHz$ $R_S = \phi$	55			dB
PSRR	Supply voltage rejection ratio	$\Delta V_S = \pm 0.5V$	50			dB
	Channel separation	$V_{OUT} = 1V_{P-P}$; $f = 100kHz$ (output referenced) $R_L = 1k\Omega$		70		dB
V_{OS}	Output offset voltage gain select pins connected together	$R_L = \infty$			1.5	V
	gain select pins open	$R_L = \infty$			1.0	V
V_{OUT}	Output differential voltage swing	$R_L = 2k\Omega$	2.8			V
I_{CC}	Power supply current (total for both sides)	$R_L = \infty$			47	mA

AC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltage $V_S = \pm 6.0V$. Gain select pins connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
BW	Bandwidth	$V_{OUT} = 1V_{P-P}$		25		MHz
t_R	Rise time			15	20	ns
t_{PD}	Propagation delay	$V_{OUT} = 1V_{P-P}$		7.5	12	ns

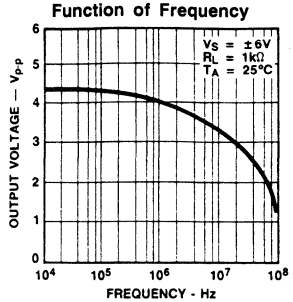
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



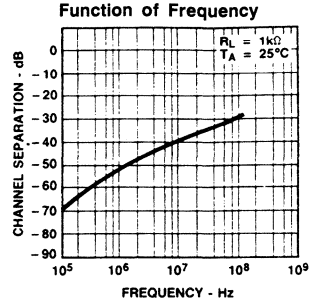
OP18580S

Output Voltage Swing as a Function of Frequency



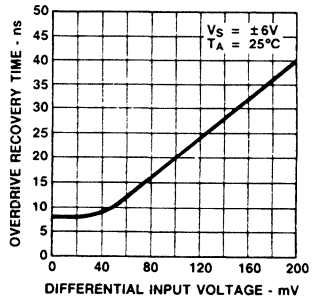
OP18590S

Channel Separation as a Function of Frequency



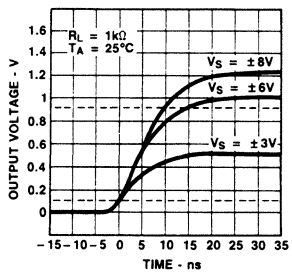
OP18600S

Differential Overdrive Recovery Time



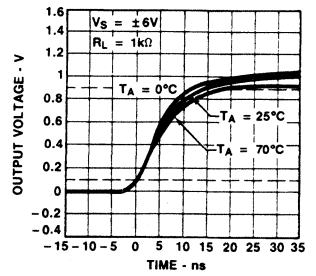
OP18610S

Pulse Response as a Function of Supply Voltage



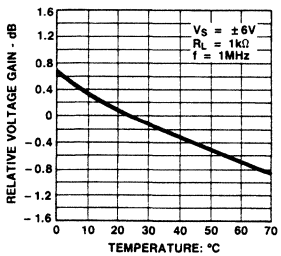
OP18620S

Pulse Response as a Function of Temperature



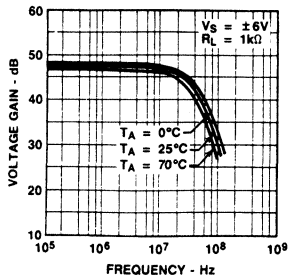
OP18630S

Voltage Gain as a Function of Temperature



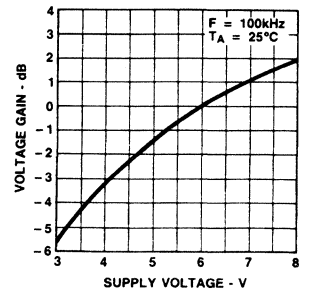
OP18640S

Gain vs Frequency as a Function of Temperature



OP18650S

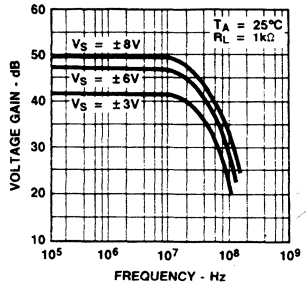
Voltage Gain as a Function of Supply Voltage



OP18660S

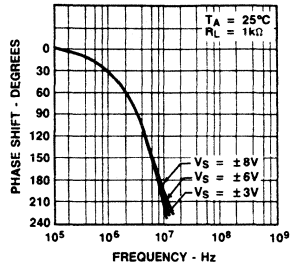
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage



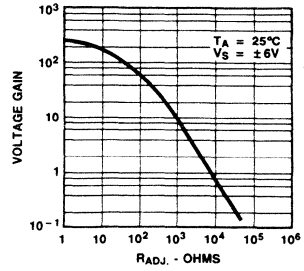
OP18670S

Phase vs Frequency as a Function of Supply Voltage



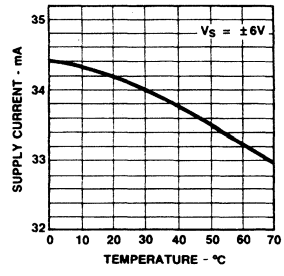
OP18680S

Voltage Gain as a Function of R_{ADJ}



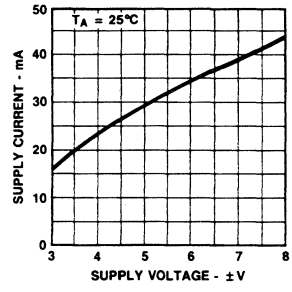
OP18690S

Supply Current as a Function of Temperature



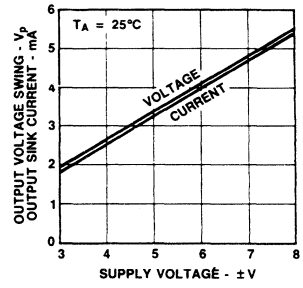
OP18700S

Supply Current as a Function of Supply Voltage



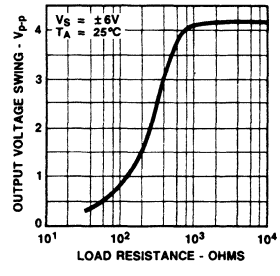
OP18710S

Output Voltage Swing and Sink Current as a Function of Supply Voltage



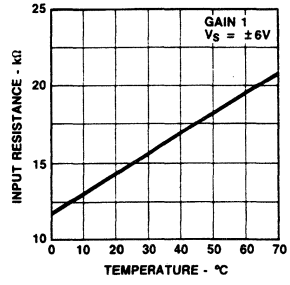
OP18720S

Output Voltage Swing as a Function of Load Resistance



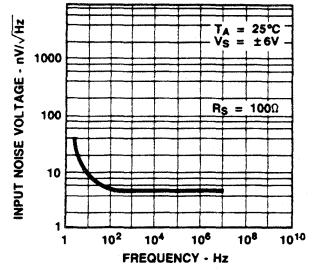
OP18730S

Input Resistance as a Function of Temperature



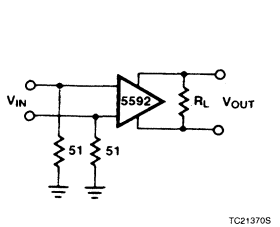
OP18740S

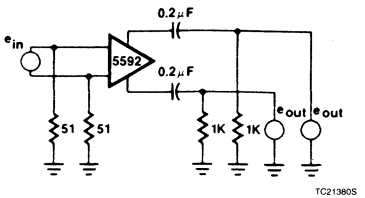
Input Noise Voltage as a Function of Frequency

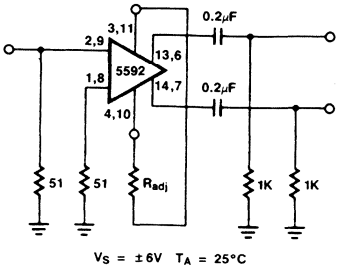


OP18750S

TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.







NE/SA/SE592
Video Amplifier

Product Specification

DESCRIPTION

The NE/SA/SE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

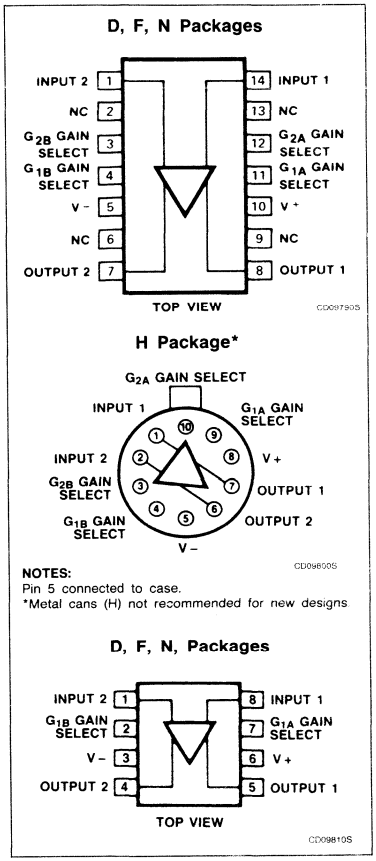
FEATURES

- **120MHz unity gain bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**
- **MIL-STD processing available**

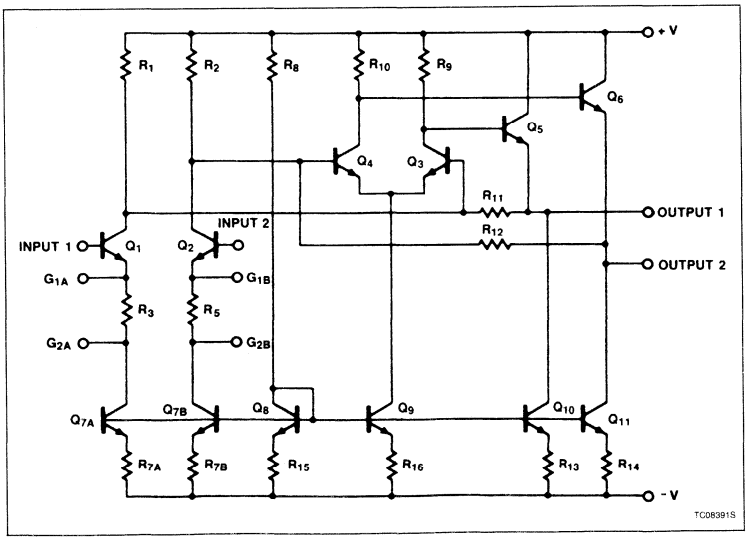
APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

PIN CONFIGURATIONS



EQUIVALENT CIRCUIT



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE592N14
14-Pin Cerdip	0 to +70°C	NE592F14
14-Pin Cerdip	−55°C to +125°C	SE592F14
14-Pin SO	0 to +70°C	NE592D14
8-Pin Plastic DIP	0 to +70°C	NE592N8
8-Pin Cerdip	−55°C to +125°C	SE592F8
8-Pin Plastic DIP	−40°C to +85°C	SA592N8
8-Pin SO	0 to +70°C	NE592D8
8-Pin SO	−40°C to +85°C	SA592D8
10-Lead Metal Can	0 to +70°C	NE592H
10-Lead Metal Can	−55°C to +125°C	SE592H

NOTE:
N8, N14, D8 and D14 package parts also available in "High" gain version by adding "H" before package designation, i.e., NE592HD8.

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating ambient temperature range		
	SE592	−40 to +85	°C
	NE592	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, $T_A = 25°C$ (still air)[1]		
	F-14 package	1.17	W
	F-8 package	0.79	W
	D-14 package	0.98	W
	D-8 package	0.79	W
	H package	0.83	W
	N-14 package	1.44	W
	N-8 package	1.17	W

NOTE:
1. Derate above 25°C at the following rates:
   F-14 package at 9.3mW/°C
   F-8 package at 6.3mW/°C
   D-14 package at 7.8mW/°C
   D-8 package at 6.3mW/°C
   H package at 6.7mW/°C
   N-14 package at 11.5mW/°C
   N-8 package at 9.3mW/°C

DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	250	400	600	300	400	500	V/V
	Gain 2[2, 4]		80	100	120	90	100	110	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 1[1]			4.0			4.0		kΩ
	Gain 2[2, 4]		10	30		20	30		kΩ
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	$V_{CM} \pm 1V$, $f < 100kHz$	60	86		60	86		dB
	Gain 2[4]	$V_{CM} \pm 1V$, $f = 5MHz$		60			60		dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.0	V
	Gain 3[3]	$R_L = \infty$		0.35	0.75		0.35	0.75	V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

DC ELECTRICAL CHARACTERISTICS

$V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leq T_A \leq 70°C$ for NE592; $-40°C \leq T_A \leq 85°C$ for SA592, $-55°C \leq T_A \leq 125°C$ for SE592, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	250		600	200		600	V/V
	Gain 2[2, 4]		80		120	80		120	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 2[2, 4]		8.0			8.0			kΩ
I_{OS}	Input offset current				6.0			5.0	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		± 1.0			± 1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	$V_{CM} \pm 1V$, $f < 100kHz$	50			50			dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	$\Delta V_S = \pm 0.5V$	50			50			dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.2	V
	Gain 3[3]	$R_L = \infty$			1.0			1.0	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	2.8			2.5			V
I_{CC}	Power supply current	$R_L = \infty$			27			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

AC ELECTRICAL CHARACTERISTICS

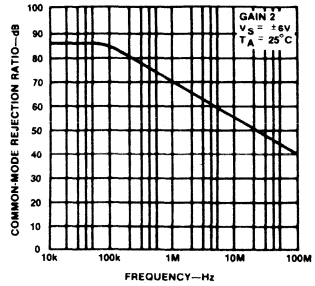
$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth								
	Gain 1[1]			40			40		MHz
	Gain 2[2, 4]			90			90		MHz
t_R	Rise time								
	Gain 1[1]	$V_{OUT} = 1V_{P-P}$		10.5			10.5		ns
	Gain 2[2, 4]			4.5	12		4.5	10	ns
t_{PD}	Propagation delay								
	Gain 1[1]	$V_{OUT} = 1V_{P-P}$		7.5			7.5		ns
	Gain 2[2, 4]			6.0	10		6.0	10	ns

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

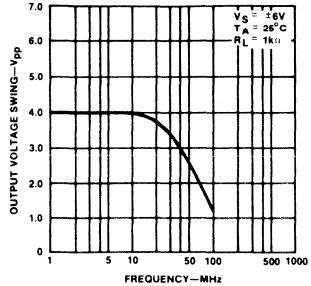
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



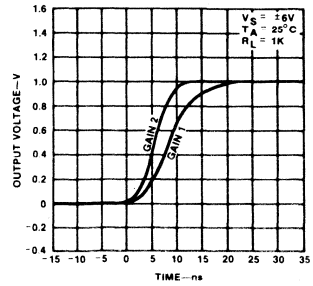
OP04421S

Output Voltage Swing as a Function of Frequency



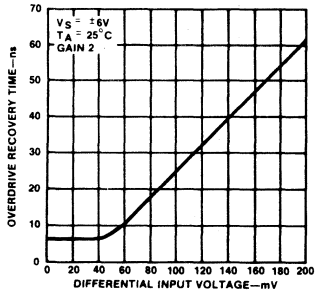
OP04430S

Pulse Response



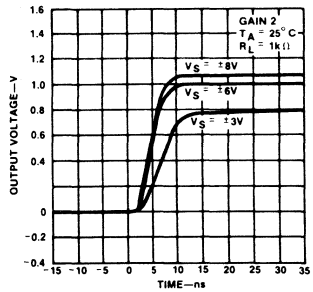
OP04440S

Differential Overdrive Recovery Time



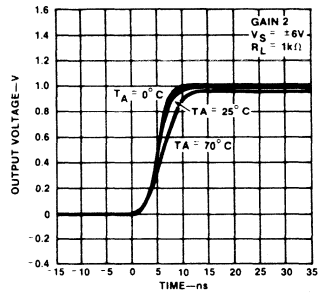
OP04450S

Pulse Response as a Function of Supply Voltage



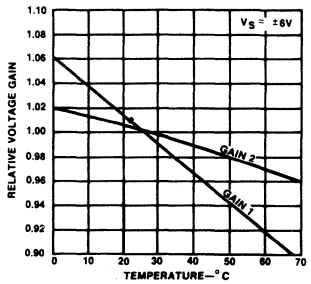
OP04460S

Pulse Response as a Function of Temperature



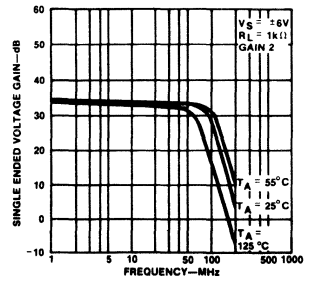
OP04470S

Voltage Gain as a Function of Temperature



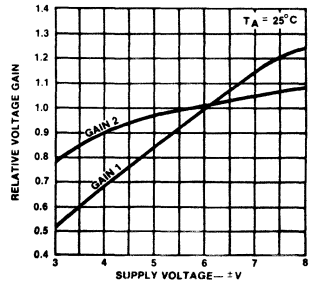
OP04480S

Gain vs Frequency as a Function of Temperature



OP04490S

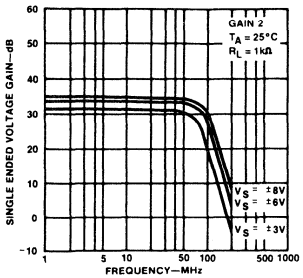
Voltage Gain as a Function of Supply Voltage



OP04500S

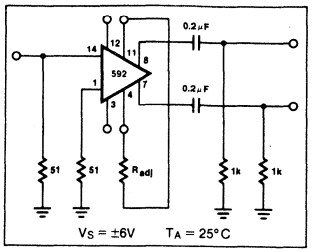
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage



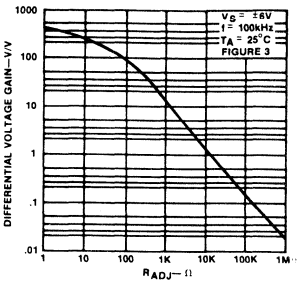
OP04510S

Voltage Gain Adjust Circuit



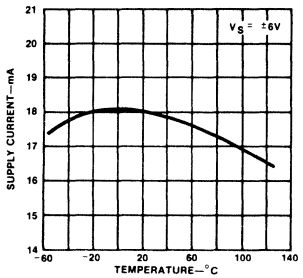
OP04521S

Voltage Gain as a Function of RADJ (Figure 3)



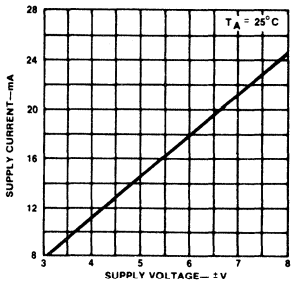
OP04530S

Supply Current as a Function of Temperature



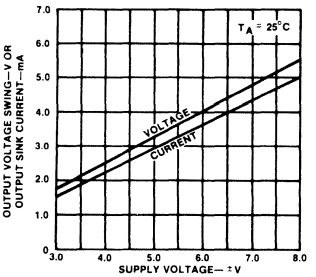
OP04540S

Supply Current as a Function of Supply Voltage



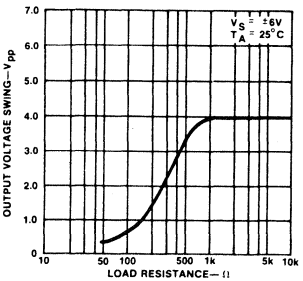
OP04550S

Output Voltage and Current Swing as a Function of Supply Voltage



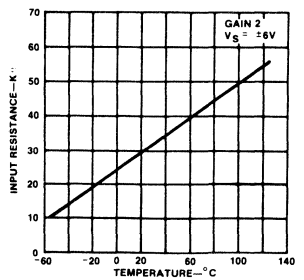
OP04560S

Output Voltage Swing as a Function of Load Resistance



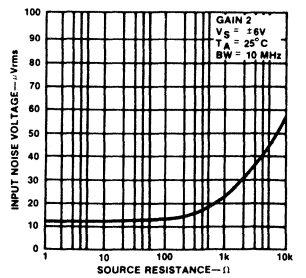
OP04570S

Input Resistance as a Function of Temperature



OP04580S

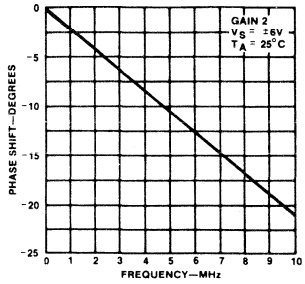
Input Noise Voltage as a Function of Source Resistance



OP04590S

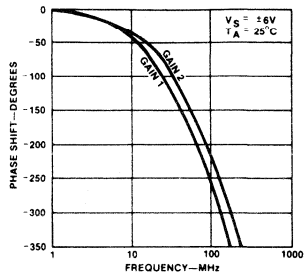
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Phase Shift as a Function of Frequency



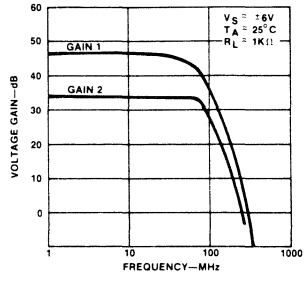
OP04600S

Phase Shift as a Function of Frequency



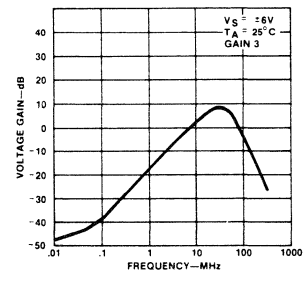
OP04610S

Voltage Gain as a Function of Frequency



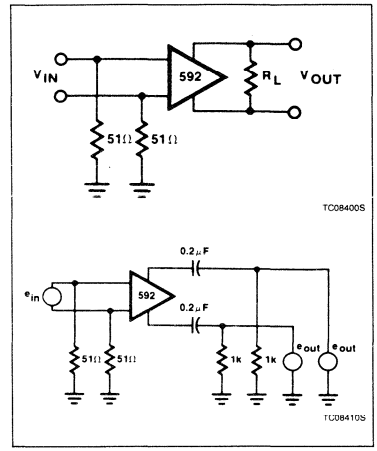
OP04620S

Voltage Gain as a Function of Frequency (All Gain Select Pins Open)

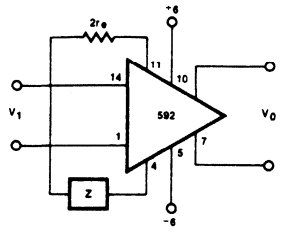


OP04630S

TEST CIRCUITS T_A = 25°C, unless otherwise specified.



TYPICAL APPLICATIONS

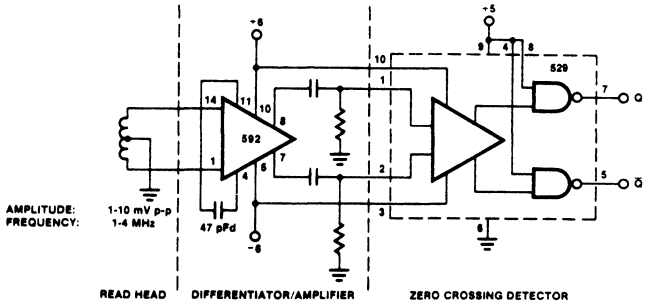


TC08420S

NOTE:

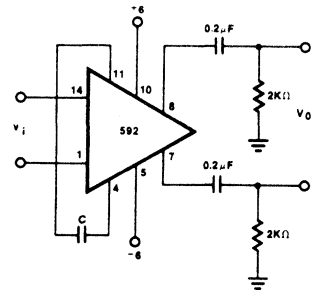
$$\frac{V_0(s)}{V_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e} \cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

Basic Configuration



TC08430S

Disc/Tape Phase-Modulated Readback Systems



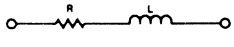
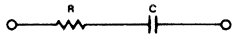
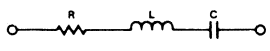
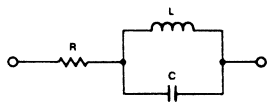
TC08440S

NOTE:
For frequency $F_1 << 1/2\pi(32)C$

$$V_0 \cong 1.4 \times 10^4 C \frac{dVi}{dT}$$

Differentiation with High Common-Mode Noise Rejection

FILTER NETWORKS

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\ s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

TC08422S

NOTES:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.
$S = j\omega$
$\omega = 2\pi f$

μA733/733C
Differential Video Amplifier

Product Specification

DESCRIPTION

The 733 is a monolithic differential input, differential output, wide-band video amplifier. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth, and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter-follower outputs to the inputs of the second stage. The emitter-follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high-performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

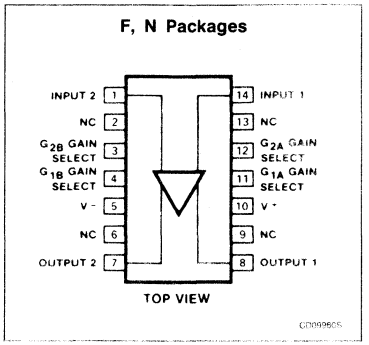
FEATURES

- **120MHz bandwidth**
- **250kΩ input resistance**
- **Selectable gains of 10, 100, and 400**
- **No frequency compensation required**
- **MIL-STD-883A, B, C available**

APPLICATIONS

- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memories**
- **Video recorder systems**

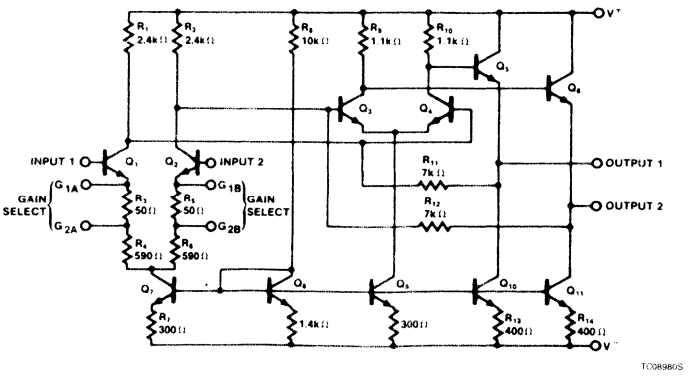
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
14-Pin Ceramic DIP	−55°C to +125°C	μA733F
14-Pin Plastic DIP	−55°C to +125°C	μA733N
14-Pin Plastic DIP	0 to +70°C	μA733CN
14-Pin Ceramic DIP	0 to +70°C	μA733CF

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DIFF}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
V_{CC}	Supply voltage	±8	V
I_{OUT}	Output current	10	mA
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range μA733C μA733	 0 to +70 −55 to +125	 °C °C
$P_{D\ MAX}$	Maximum power dissipation, 25°C ambient temperature (still-air)[1] F package N package	 1190 1420	 mW mW

NOTE:
1. The following derating factors should be applied above 25°C:
   F package at 9.5mW/°C
   N package at 11.4mW/°C.

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_S = ±6V, V_{CM} = 0, unless otherwise specified. Recommended operating supply voltages V_S = ±6.0V.

SYMBOL	PARAMETER	TEST CONDITIONS	μA733C			μA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Differential voltage gain Gain 1[2] Gain 2[2] Gain 3[3]	R_l = 2kΩ, V_{OUT} = $3V_{P-P}$	 250 80 8	 400 100 10	 600 120 12	 300 90 9	 400 100 10	 500 110 11	 V/V V/V V/V
BW	Bandwidth Gain 1[1] Gain 2[2] Gain 3[3]			 40 90 120			 40 90 120		 MHz MHz MHz
t_R	Rise time Gain 1[1] Gain 2[2] Gain 3[3]	V_{OUT} = $1V_{P-P}$		 10.5 4.5 2.5	 12 		 10.5 4.5 2.5	 10 	 ns ns ns
t_{PD}	Propagation delay Gain 1[1] Gain 2[2] Gain 3[3]	V_{OUT} = $1V_{P-P}$		 7.5 6.0 3.6	 10 		 7.5 6.0 3.6	 10 	 ns ns ns
R_{IN}	Input resistance Gain 1[2] Gain 2[2] Gain 3[3]		 10 	 4.0 30 250	 	 20 	 4.0 30 250	 	 kΩ kΩ kΩ
	Input capacitance[2]	Gain 2		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW = 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio Gain 2 Gain 2	 V_{CM} = ±1V, f ≤ 100kHz V_{CM} = ±1V, f = 5MHz	 60 	 86 60	 	 60 	 86 60	 	 dB dB
SVRR	Supply voltage rejection ratio Gain 2	ΔV_S = ±0.5V	50	70		50	70		dB

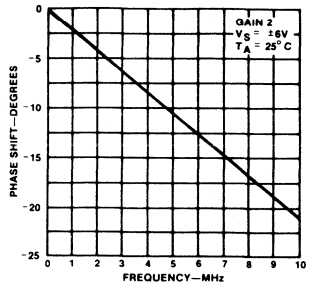
DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = +25°C$, $V_S = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$.

SYMBOL	PARAMETER	TEST CONDITIONS	μA733C			μA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Output offset voltage Gain 1[1] Gain 2 and 3[2, 3]	$R_L = \infty$		 0.6 0.35	 1.5 1.5		 0.6 0.35	 1.5 1.0	 V V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
	Output voltage swing, differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V_{P-P}
I_{SINK}	Output sink current		2.5	3.6		2.5	3.6		mA
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER TEMPERATURE			**0°C ≤ T_A ≤ 70°C**			**-55°C ≤ T_A ≤ 125°C**			
	Differential voltage gain Gain 1[1] Gain 2[2] Gain[3]	$R_l = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	 250 80 8		 600 120 12	 200 80 8		 600 120 12	 V/V V/V V/V
R_{IN}	Input resistance Gain 2[2]		 8			 8			 kΩ
I_{OS}	Input offset current				6			5	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		± 1.0			± 1.0			V
CMRR	Common-mode rejection ratio Gain 2	$V_{CM} = \pm V$, $F \leq 100kHz$	50			50			dB
SVRR	Supply voltage rejection ratio Gain 2	$\Delta V_S = \pm 0\ 5V$	50			50			dB
V_{OS}	Output offset voltage Gain 1[1] Gain 2 and 3[2, 3]	$R_L = \infty$			 1.5 1.5			 1.5 1.2	 V V
V_{DIFF}	Output voltage swing, differential	$R_L = 2k\Omega$	2.8			2.5			V_{P-P}
I_{SINK}	Output sink current		2.5			2.2			mA
I_{CC}	Power supply current	$R_L \pm \infty$			27			27	mA

NOTES:
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

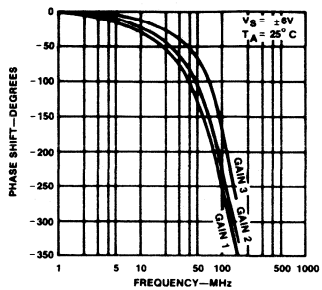
TYPICAL PERFORMANCE CHARACTERISTICS

Phase Shift as a Function of Frequency



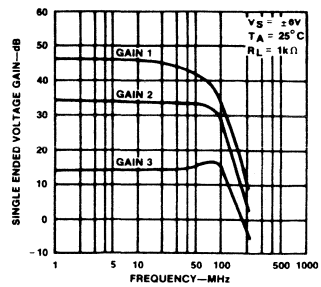
OP05620S

Phase Shift as a Function of Frequency



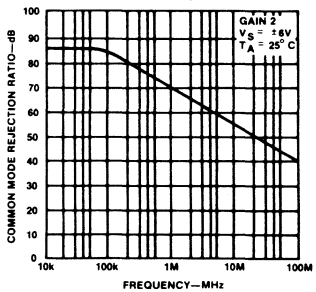
OP05630S

Voltage Gain as a Function of Frequency



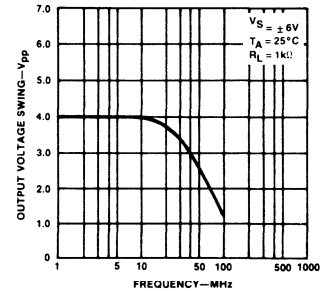
OP05640S

Common Mode Rejection Ratio as a Function of Frequency



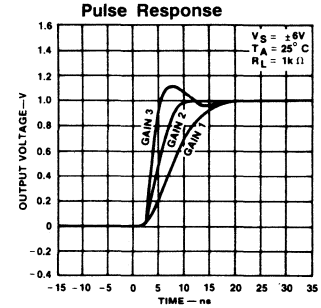
OP05650S

Output Voltage Swing as a Function of Frequency



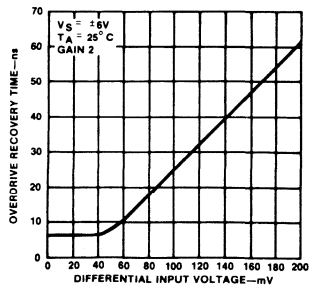
OP05660S

Pulse Response



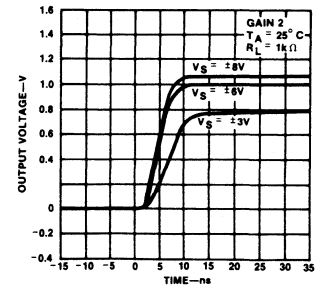
OP05670S

Differential Overdrive Recovery Time



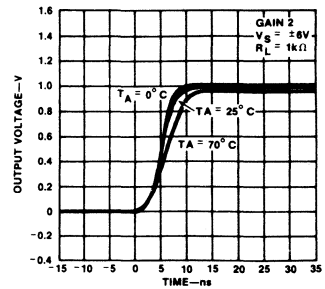
OP05680S

Pulse Response as a Function of Supply Voltage



OP05690S

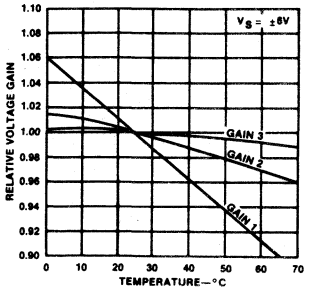
Pulse Response as a Function of Temperature



OP05700S

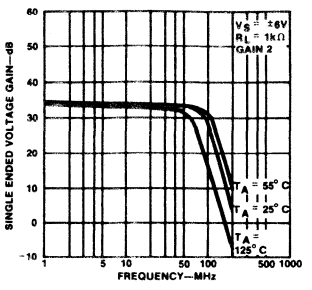
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Voltage Gain as a Function of Temperature



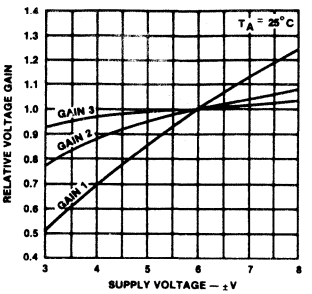
OP05710S

Gain vs Frequency as a Function of Temperature



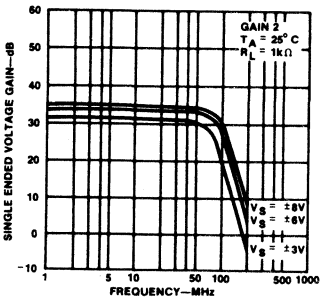
OP05720S

Voltage Gain as a Function of Supply Voltage



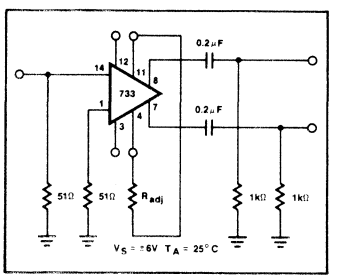
OP05730S

Gain vs Frequency as a Function of Supply Voltage



OP05740S

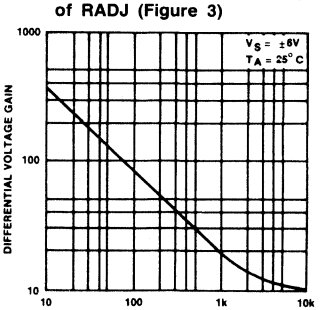
Voltage Gain Adjust Circuit



(Pin numbers apply to K Package)

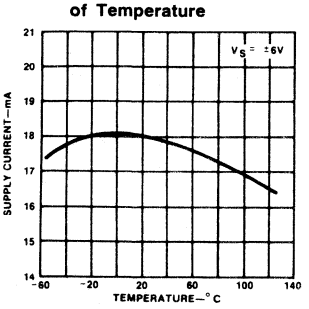
OP05750S

Voltage Gain as a Function of RADJ (Figure 3)



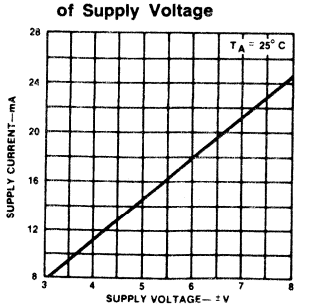
OP05760S

Supply Current as a Function of Temperature



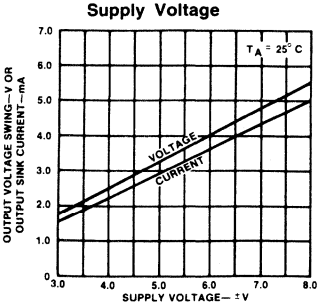
OP05770S

Supply Current as a Function of Supply Voltage



OP05780S

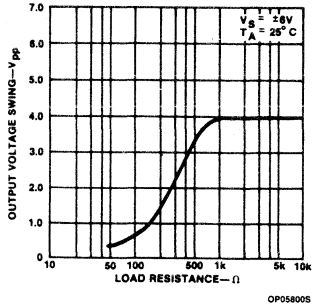
Output Voltage and Current Swing as a Function of Supply Voltage



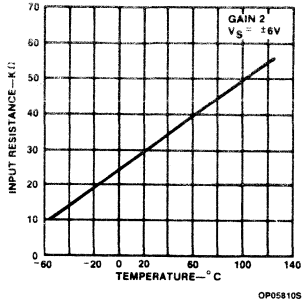
OP05790S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

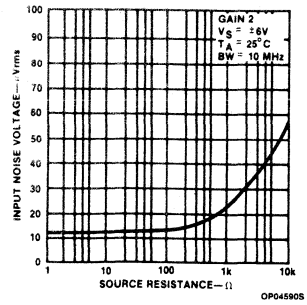
Output Voltage Swing as a Function of Load Resistance



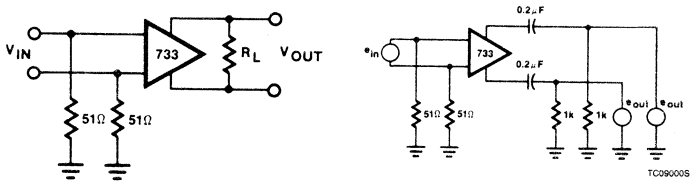
Input Resistance as a Function of Temperature



Input Noise Voltage as a Function of Source Resistance



TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.



AN140
Compensation Techniques for Use with the NE/SE5539

Application Note

NE5539 DESCRIPTION

The Signetics NE/SE5539 ultra-high frequency operational amplifier is one of the fastest monolithic amplifiers made today. With a unity gain bandwidth of 350MHz and a slew rate of 600V/μs, it is second to none. Therefore, it is understandable that to attain this speed, standard internal compensation would have to be left out of its design. As a consequence, the op amp is not unconditionally stable for all closed-loop gains and must be externally compensated for gains below 17dB. Properly done, compensation need not limit slew rate. The following will explain how to use the methods available with the NE/SE5539.

LEAD AND LAG-LEAD COMPENSATION

A useful method for compensating the device for closed-loop gains below seven is to use lag-lead and lead networks as shown in Figure 1. The lead network is primarily concerned with compensating for loss of phase margin caused by distributed board capacitance and input capacitance, while lag-lead is mainly for optimizing transient response. Lead compensation modifies the feedback network and adds a zero to the overall transfer function. This increases the phase, but does not greatly change the gain magnitude. This zero improves the phase margin.

To determine components, it can be shown that the optimal conditions for amplifier stability occur when:

$$(R1)(C_{DIST}) = (R_F)(C_{LEAD}) \qquad (1)$$

However, when the stability criteria is obtained, it should be noted that the actual bandwidth of the closed-loop amplifier will be reduced. Based on using a double-sided copper-clad printed circuit board with a distributed capacitance of 3.5pF and a unity gain configuration, C_{LEAD} would be 3.5pF. Another way of stating the relationship between the distributed capacitance closed-loop gain and the lead compensation capacitor is:

$$C_{LEAD} = C_{DIST}\frac{R1}{R_F} \qquad (2)$$

When bandwidth is of primary concern, the lead compensation will usually be adequate. For closed-loop gains less than seven, lag-lead compensation is necessary for stability.

If transient response is also a factor in design, a lag-lead compensation network may be necessary (Reference Figure 1). For practical applications, the following equations can be used to determine proper lag-lead components:

$$\frac{R_F}{R1/R_{LAG}} \geq 7 \qquad (4)$$

Therefore,

$$R_{LAG} \leq \frac{R_F}{7 - R_F/R1} \qquad (5)$$

Using the above equation will insure a closed-loop gain of seven above the network break frequency. C_{LAG} may now be approximated using:

$$W_{LAG} \cong \frac{2\pi(GBW)}{10}\ \text{Rad/Sec} \qquad (6)$$

$$W_{LAG} = \frac{\pi(GBW)}{5}\ \text{Rad/Sec} \qquad (7)$$

where

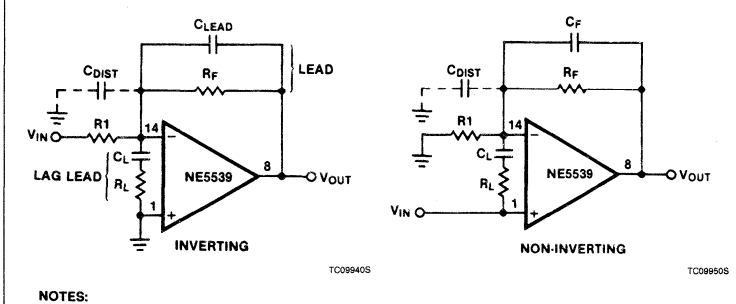
$$W_{LAG} = \frac{1}{(R_{LAG})(C_{LAG})} \qquad (8)$$

therefore,

$$\frac{\pi(GBW)}{5} = \frac{1}{(R_{LAG})(C_{LAG})} \qquad (9)$$

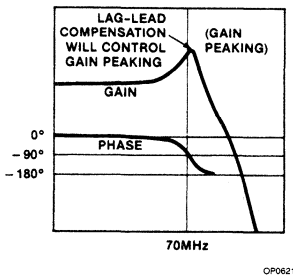
and

$$C_{LAG} = \frac{5}{\pi R_{LAG}(GBW)} \qquad (10)$$

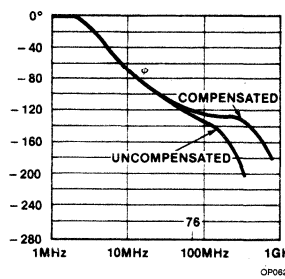


NOTES:
$C_L = C_{LAG}$
$R_L = R_{LAG}$

Figure 1. Standard Lag-Lead Compensation



a. Closed-Loop Inverting Gain of Seven Gain-Phase Response (Uncompensated)



b. Open-Loop Phase

Figure 2

Compensation Techniques for Use with the NE/SE5539 AN140

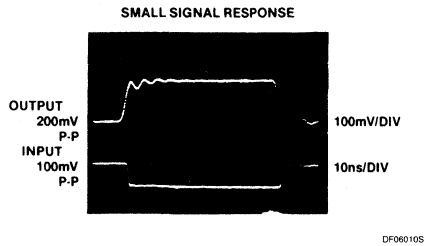


Figure 3. Compensated Pulse Response

This method adds a pole and zero to the transfer function of the device, causing the actual open-loop gain and phase curve to be reshaped, thus creating a progressive improvement above the critical frequency where phase changes rapidly. (Near 70MHz, see Figures 2a and 2b.) But also, the lag-lead network can be adjusted to optimize gain peaking for transient responses. Therefore, rise time, overshoot, and settling time can be changed for various closed-loop gains. The result of using this technique is shown for a pulse amplifier in Figure 3.

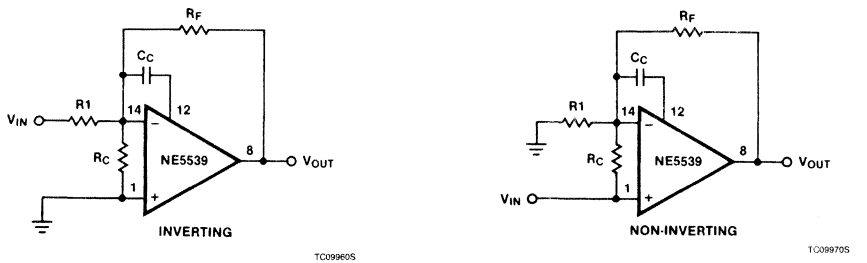


Figure 4. Pin 12 Compensation

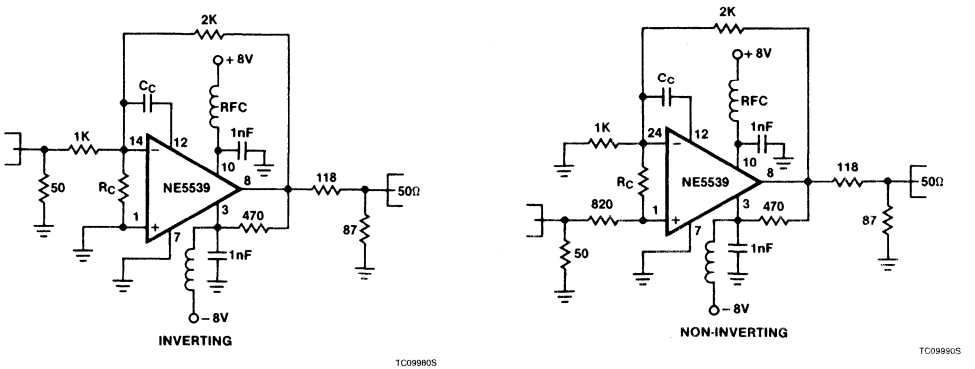


Figure 5. Pulse Response Test Circuits

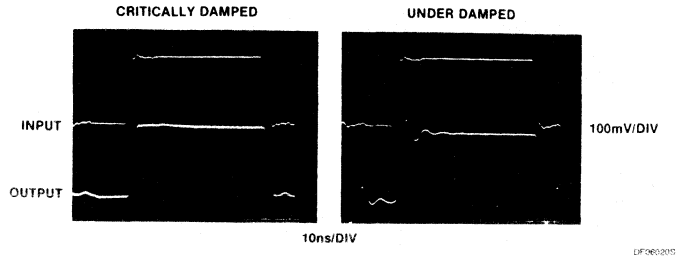


Figure 6. Small Signal Response — Non-Inverting

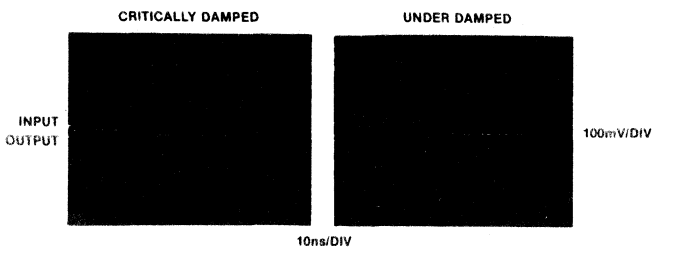


Figure 7. Small Signal Response — Inverting

USING PIN 12 COMPENSATION

An alternate method of external compensation is obtained by use of the NE/SE5539 frequency compensation pin. The circuits in Figure 4 show the correct way to use this pin. As can be seen, this method saves the use of one capacitor as compared to standard lag-lead and lead compensation as shown in Figure 1.

But, most importantly, both methods are equally effective; i.e., a good wide-band amplifier below 17dB, with control over ringing and overshoot. For example, inverting and non-inverting amplifier circuits using Pin 12 are shown in Figure 5. The corresponding pulse response for each circuit is shown in Figures 6 and 7 for the network values recommended. As shown by the response photos, the overshoot and settling time can be controlled by adjusting R_C and C_C. In damping the overshoot, rise time is slightly decreased. Also, the non-inverting configuration (Figure 6) gives a very fast response time compared to the inverting mode.

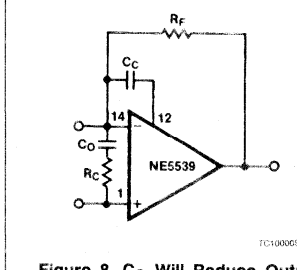


Figure 8. C_O Will Reduce Output Offset and Noise

If it is important to reduce output offset voltage and noise, an additional capacitor, C_O, can be added in series with the resistor (R_C) across the inputs. This should be a large value to block DC but not affect the benefits of the compensation components at high frequencies. A value of 0.01μF as shown in Figure 8 is sufficient.

INTERNAL CHARACTERISTICS OF THE NE/SE5539

In order to better understand the compensation procedure, a detailed discussion of the amplifier follows.

The complete amplifier schematic is shown in Figure 9. To clarify the effect of the compensation pin, the schematic is split into five main parts as shown in Figure 10.

Each segment in Figure 10 is defined as follows: starting from the non-inverting input, Section A_1 is the amplification from the input to the base of transistor Q_4. A_2 is from the base of Q_4 to the summation point at the collector of Q_3. Furthermore, A_3 represents the gain from the non-inverting input to the summation point via the common emitter side of Q_2 and Q_3. Finally, B_F is the feedback factor of the positive feedback loop from the collector of Q_3 to the base of Q_4.

From Figure 10, it can be seen that the total gain (A_T) is:

$$A_T = \frac{A_1 A_2}{1 - (B_F A_2)} + A_3 (1 + B_F A_2)$$

Each term in this equation plays a role at different frequencies to determine the total transfer function of the device. Of particular importance is the pole in A_3 (near 340MHz) which causes a roll-off of 12dB/octave and loss of phase margin just before unity gain. This can be seen in the Bode plot in Figure 11a. To overcome this pole, a capacitor and resistor are connected as shown in Figures 12a and 12b. The compensation pin is connected to the emitter of Q_5, which is in an emitter-follower configuration. Therefore, a reactance connected to Pin 12 acts essentially as if it were connected at the base of Q_5. Since the capacitor is connected here, it is now a component of B_F and a zero is added to the transfer function. The resistor across the input pins controls overall gain and causes A_T to cross 0dB at a lower frequency; the capacitor in the feedback loop controls phase shift and gain peaking.

To further explain, Bode plots of open-loop response using varying capacitor values and corresponding pulse responses are shown in Figures 13a through 13f. The changes in gain and phase can readily be seen, as is the effect on bandwidth.

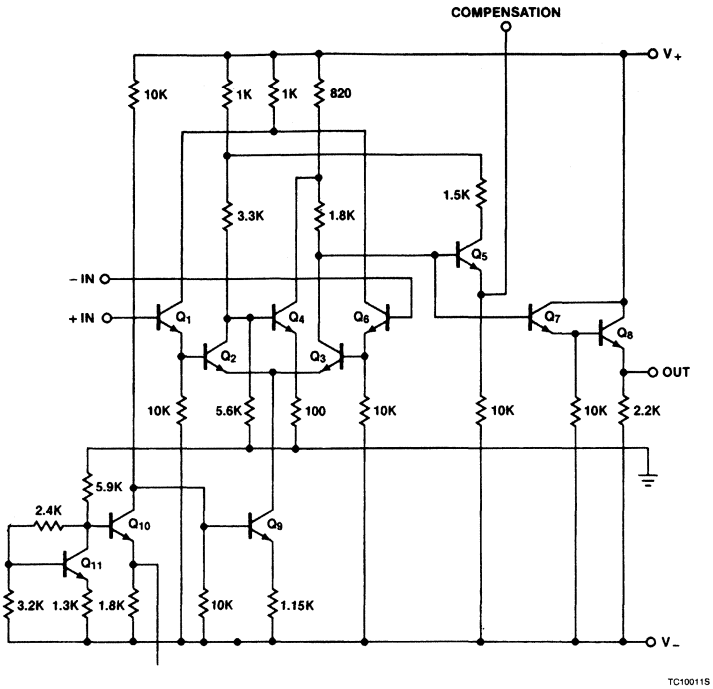


Figure 9. Complete Schematic of NE/SE5539

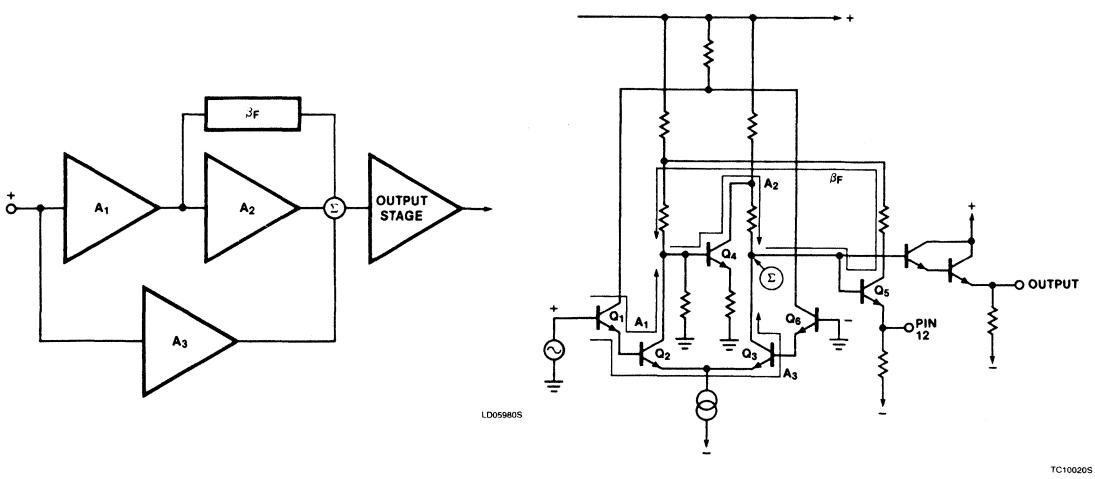
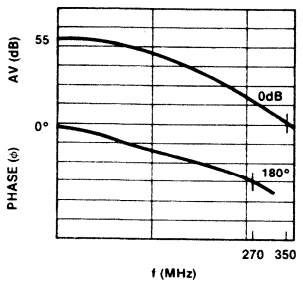


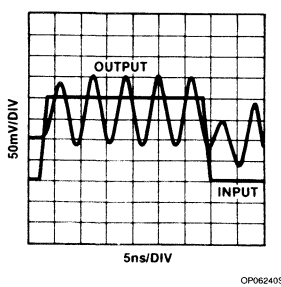
Figure 10. Internal Sections

COMPUTER ANALYSIS

The open-loop and pulse response plots were generated using an IBM 370 computer and SPICE, a general-purpose circuit simulation program. Each transistor in the part is mathematically modeled after actual device parameters, which were measured in the laboratory. These models are then combined with the resistors and voltage sources through node numbers so that the computer knows where each is connected.



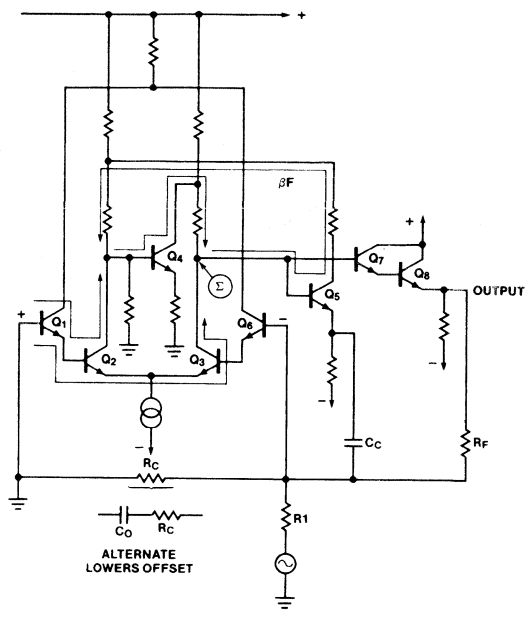
a. Open-Loop Gain — No Compensation (Computer Simulation)



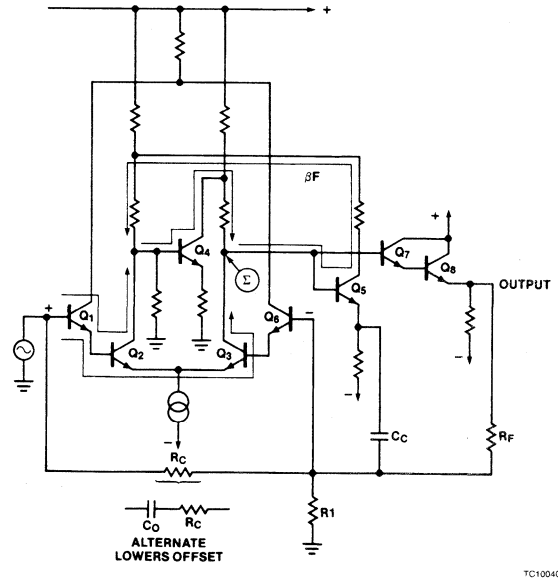
b. Closed-Loop Non-Inverting Response — No Compensation (Computer Simulation — Oscillation is Evident)

Figure 11

To indicate the accuracy of this system, the actual open-loop gain is compared to the computer plots in Figures 14 and 15. The real payoff for this system is that once a credible simulation is achieved, any outside circuit can be modeled around the op amp. This would be used to check for feasibility before breadboarding in the lab. The internal circuit can be treated like a black box and the outside circuit program altered to whatever application the user would like to examine.

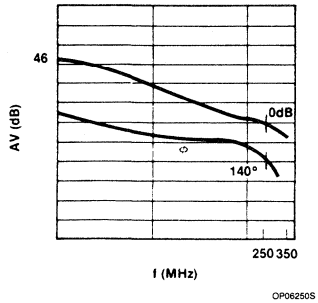


a. Pin 12 Compensation Showing Internal Connections — Inverting

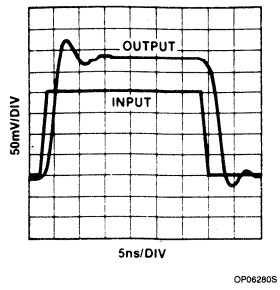


b. Pin 12 Compensation Showing Internal Connections — Non-Inverting

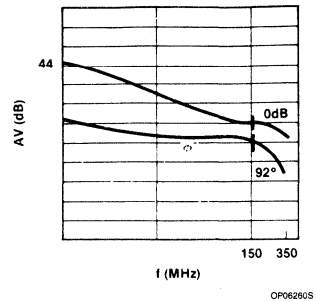
Figure 12



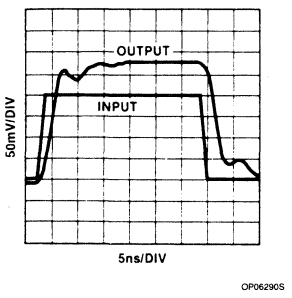
a. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 1pF$, (Computer Simulation)



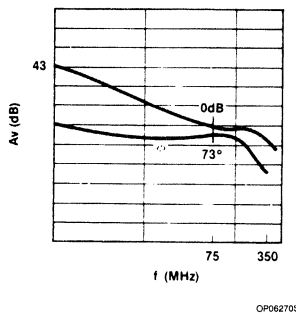
b. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 1pF$, $A_V = 3$ (Computer Simulation — Underdamped)



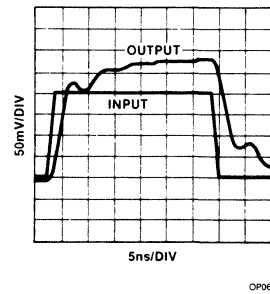
c. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 2pF$ (Computer Simulation)



d. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 2pF$, $A_V = 3$ (Computer Simulation — Critically-Damped)



e. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 3pF$, (Computer Simulation)



f. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 3pF$, $A_V = 3$ (Computer Simulation — Overdamped)

Figure 13

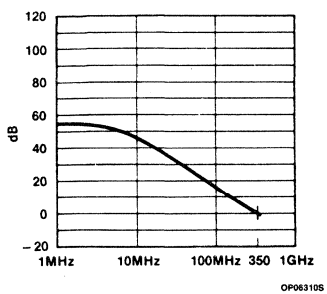


Figure 14. Actual Open-Loop Gain Measured in Lab

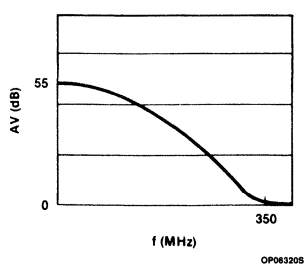


Figure 15. Computer-Generated Open-Loop Gain

1. J. Millman and C. C. Halkias: *Integrated Electronics: Analog and Digital Circuits and Systems,* McGraw-Hill Book Company, New York, 1972.

2. A. Vladimirescu, Kaihe Zhang, A. R. Newton, D. O. Peterson, A. Sanquiovanni-Vincentelli: "Spice Version 2G," University of California, Berkeley, California, August 10, 1981.

3. Signetics: *Analog Data Manual 1983,* Signetics Corporation, Sunnyvale, California 1983.

AN141
Using the NE/SA/SE592 Video Amplifier

Application Note

VIDEO AMPLIFIER PRODUCTS

NE/SA/SE592 Video Amplifier

The 592 is a two-stage differential output, wide-band video amplifier with voltage gains as high as 400 and bandwidths up to 120MHz.

Three basic gain options are provided. Fixed gains of 400 and 100 result from shorting together gain select pins $G_{1A} - G_{1B}$ and $G_{2A} - G_{2B}$, respectively. As shown by Figure 1, the emitter circuits of the differential pair return through independent current sources. This topology allows no gain in the input stage if all gain select pins are left open. Thus, the third gain option of tying an external resistance across the gain select pins allows the user to select any desired gain from 0 to 400V/V. The advantages of this configuration will be covered in greater detail under the filter application section.

Three factors should be pointed out at this time:

1. The gains specified are differential. Single-ended gains are one-half the stated value.
2. The circuit 3dB bandwidths are a function of and are inversely proportional to the gain settings.
3. The differential input impedance is an inverse function of the gain setting.

In applications where the signal source is a transformer or magnetic transducer, the input bias current required by the 592 may be passed directly through the source to ground. Where capacitive coupling is to be used, the base inputs must be returned to ground through a resistor to provide a DC path for the bias current.

Due to offset currents, the selection of the input bias resistors is a compromise. To reduce the loading on the source, the resistors should be large, but to minimize the output DC offset, they should be small — ideally 0Ω. Their maximum value is set by the maximum allowable output offset and may be determined as follows:

1. Define the allowable output offset (assume 1.5V).
2. Subtract the maximum 592 output offset (from the data sheet). This gives the output offset allowed as a function of input offset currents (1.5V – 1.0V = 0.5V).
3. Divide by the circuit gain (assume 100). This refers the output offset to the input.
4. The maximum input resistor size is:

$$R_{MAX} = \frac{\text{Input Offset Voltage}}{\text{Max Input Offset Current}} \quad (1)$$

$$= \frac{0.005V}{5\mu A}$$

$$= 1.00k\Omega$$

Of paramount importance during the design of the NE592 device was bandwidth. In a monolithic device, this precludes the use of PNP transistors and standard level-shifting techniques used in lower frequency devices. Thus, without the aid of level shifting, the output common-mode voltage present on the NE592 is typically 2.9V. Most applications, therefore, require capacitive coupling to the load.

Filters

As mentioned earlier, the emitter circuit of the NE592 includes two current sources.

Since the stage gain is calculated by dividing the collector load impedance by the emitter impedance, the high impedance contributed by the current sources causes the stage gain to be zero with all gain select pins open. As shown by the gain vs. frequency graph of Figure 2, the overall gain at low frequencies is a negative 48dB.

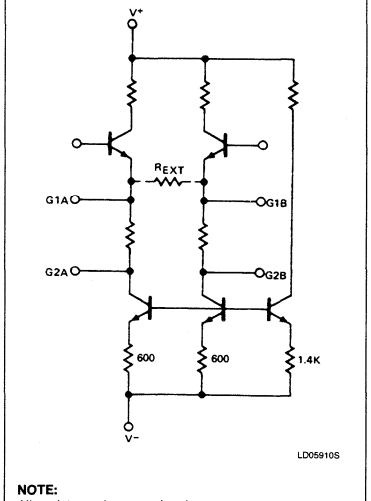
Higher frequencies cause higher gain due to distributed parasitic capacitive reactance. This reactance in the first stage emitter circuit causes increasing stage gain until at 10MHz the gain is 0dB, or unity.

Referring to Figure 3, the impedance seen looking across the emitter structure includes small r_e of each transistor.

Any calculations of impedance networks across the emitters then must include this quantity. The collector current level is approximately 2mA, causing the quantity of 2 r_e to be approximately 32Ω. Overall device gain is thus given by

$$\frac{V_O(s)}{V_{IN}(s)} = \frac{1.4 \times 10^4}{Z_{(S)} + 32} \quad (2)$$

where $Z_{(S)}$ can be resistance or a reactive impedance. Table 2 summarizes the possible configurations to produce low, high, and bandpass filters. The emitter impedance is made to vary as a function of frequency by using capacitors or inductors to alter the frequency response. Included also in Table 2 is the gain calculation to determine the voltage gain as a function of frequency.



NOTE:
All resistor values are in ohms.

Figure 1. 592 Input Structure

Table 1. Video Amplifier Comparison File

PARAMETER	NE/SA/SE592	733
Bandwidth (MHz)	120	120
Gain	0,100,400	10,100,400
R_{IN} (k)	4 – 30	4 – 250
V_{P-P} (Vs)	4.0	4.0

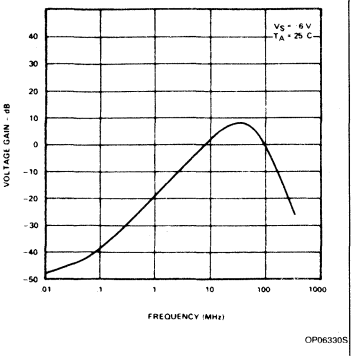
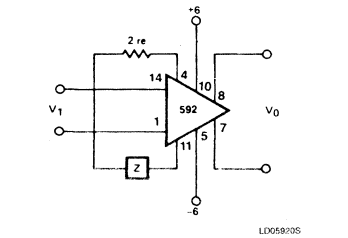


Figure 2. Voltage Gain as a Function of Frequency (All Gain Select Pins Open)



NOTE:

$$\frac{V_0(s)}{V_1(s)} = \frac{1.4 \times 10^4}{Z(s) + 2re} = \frac{1.4 \times 10^4}{Z(s) + 32}$$

Figure 3. Basic Gain Configuration for NE592, N14

Differentiation

With the addition of a capacitor across the gain select terminals, the NE592 becomes a differentiator. The primary advantage of using the emitter circuit to accomplish differentiation is the retention of the high common mode noise rejection. Disc file playback systems rely heavily upon this common-mode rejection for proper operation. Figure 4 shows a differential amplifier configuration with transfer function.

Disc File Decoding

In recovering data from disc or drum files, several steps must be taken to precondition the linear data. The NE592 video amplifier, coupled with the 8T20 bidirectional one-shot, provides all the signal conditioning necessary for phase-encoded data.

When data is recorded on a disc, drum or tape system, the readback will be a Gaussian shaped pulse with the peak of the pulse corresponding to the actual recorded transition point. This readback signal is usually 500μV_{P-P} to 3mV_{P-P} for oxide coated disc files and 1 to 20mV_{P-P} for nickel-cobalt disc files. In order to accurately reproduce the data stream originally written on the disc memory, the time of peak point of the Gaussian readback signal must be determined.

The classical approach to peak time determination is to differentiate the input signal. Differentiation results in a voltage proportional to the slope of the input signal. The zero-crossing point of the differentiator, therefore, will occur when the input signal is at a peak. Using a zero-crossing detector and one-shot, therefore, results in pulses occurring at the input peak points.

A circuit which provides the preconditioning described above is shown in Figure 5. Readback data is applied directly to the input of the first NE592. This amplifier functions as a wide-band AC-coupled amplifier with a gain of 100. The NE592 is excellent for this use because of its high phase linearity, high gain and ability to directly couple the unit with the readback head. By direct coupling of readback head to amplifier, no matched terminating resistors are required and the excellent common-mode rejection ratio of the amplifier is preserved. DC components are also rejected because the NE592 has no gain at DC due to the capacitance across the gain select terminals.

The output of the first stage amplifier is routed to a linear phase shift low-pass filter. The filter is a single-stage constant K filter, with a characteristic impedance of 200Ω. Calculations for the filter are as follows:

$$L = 2R/\omega_C$$

where

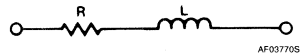
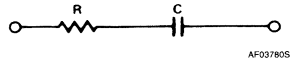
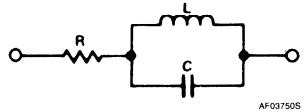
R = characteristic impedance (Ω)

$$C = 1/\omega_C$$

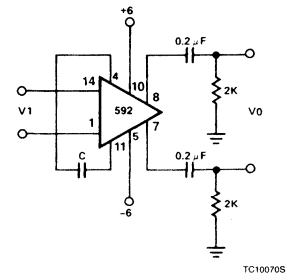
where

ω_C = cut-off frequency (radians/sec)

Table 2. Filter Networks

Z NETWORK	FILTER TYPE	$V_0(s)$ TRANSFER $V_1(s)$ FUNCTION
 AF03770S	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
 AF03780S	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
 AF03790S	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/Ls + 1/LC}\right]$
 AF03750S	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTES:
In the networks above, the R value used is assumed to include 2 r_e, or approximately 32Ω.
S = jΩ
Ω = 2πf



NOTES:
For frequency $F_1 < < 1/2\pi(32)C$

$$V_0 \cong 1.4 \times 10^4 C \frac{dv_i}{dT}$$

All resistor values are in ohms.

Figure 4. Differential with High Common-Mode Noise Rejection

Using the NE/SA/SE592 Video Amplifier

AN141

The second NE592 is utilized as a low noise differentiator/amplifier stage. The NE592 is excellent in this application because it allows differentiation with excellent common-mode noise rejection.

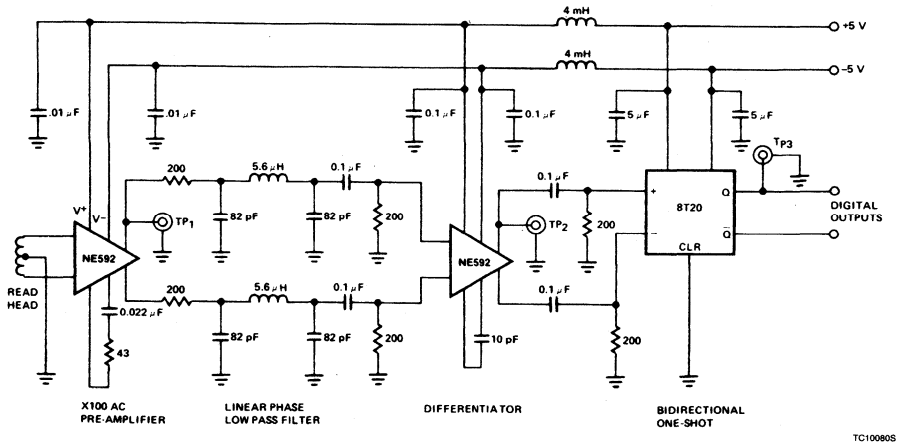
The output of the differentiator/amplifier is connected to the 8T20 bidirectional monostable unit to provide the proper pulses at the zero-crossing points of the differentiator.

The circuit in Figure 5 was tested with an input signal approximating that of a readback signal. The results are shown in Figure 7.

Automatic Gain Control

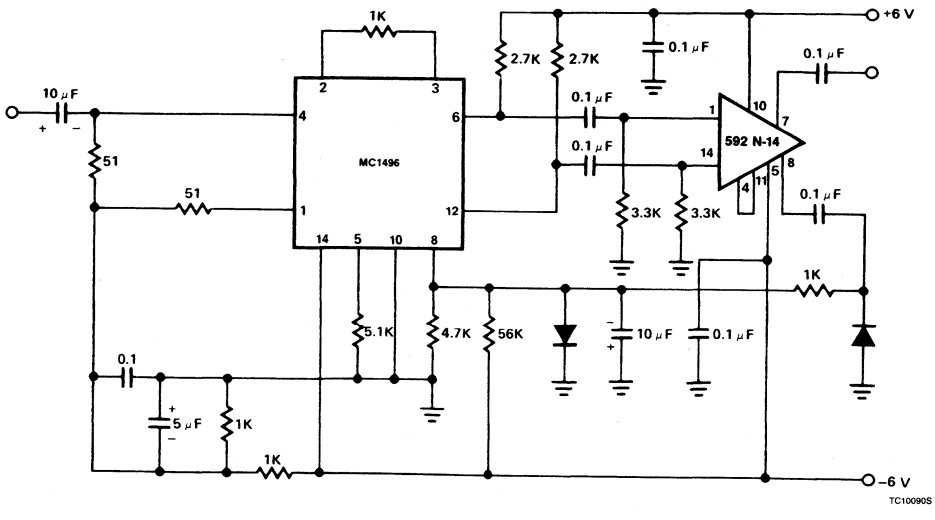
The NE592 can also be connected in conjunction with a MC1496 balanced modulator to form an excellent automatic gain control system.

The signal is fed to the signal input of the MC1496 and RC-coupled to the NE592. Unbalancing the carrier input of the MC1496 causes the signal to pass through unattenuated. Rectifying and filtering one of the NE592 outputs produces a DC signal which is proportional to the AC signal amplitude. After filtering; this control signal is applied to the MC1496 causing its gain to change.



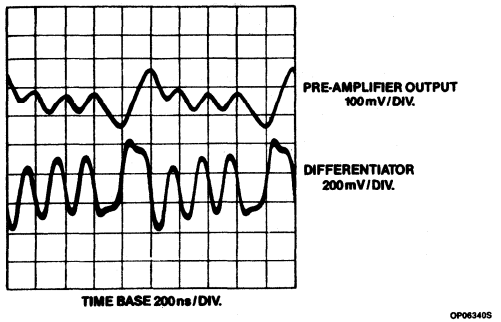
NOTE:
All resistor values are in ohms

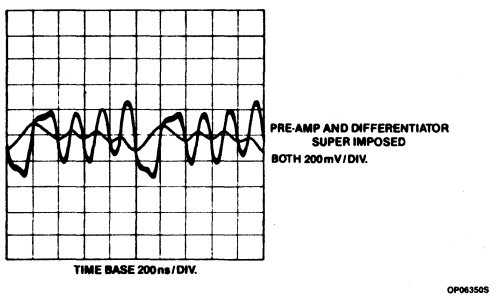
Figure 5. 5MHz Phase-Encoded Data Read Circuitry



NOTE:
All resistor values are in ohms

Figure 6. Wide-band AGC Amplifier





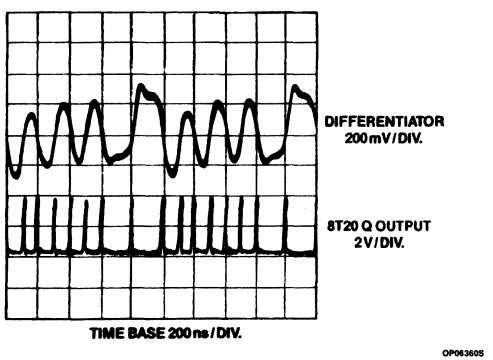


Figure 7. Test Results of Disc File Decoder Circuit

Transconductance amplifiers

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NE5517	dual operational transconductance amplifier	295
NE5517A	dual operational transconductance amplifier	295
AN145	NE5517/A transconductance amplifier applications	309

NE5517/5517A
Dual Operational Transconductance Amplifier

Product Specification

DESCRIPTION

The NE5517 contains two current-controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10dB signal-to-noise improvement referenced to 0.5% THD. The NE5517 is suited for a wide variety of industrial and consumer applications and is recommended as the preferred circuit in the Dolby* HX (Headroom Extension) system.

Constant impedance buffers on the chip allow general use of the NE5517. These buffers are made of Darlington transistor and a biasing network which changes bias current in dependence of I_{ABC}.

Therefore, changes of output offset voltages are almost eliminated. This is an advantage of the NE5517 compared to LM13600. With the LM13600, a burst in the bias current I_{ABC} guides to an audible offset voltage change at the output. With the constant impedance buffers of the NE5517 this effect can be avoided and makes this circuit preferable for high quality audio applications.

FEATURES

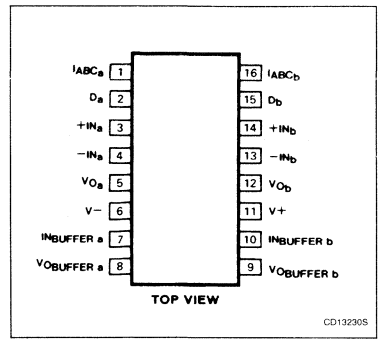
- **Constant impedance buffers**
- **ΔV_{BE} of buffer is constant with amplifier I_{BIAS} change**
- **Pin compatible with LM13600**
- **Excellent matching between amplifiers**
- **Linearizing diodes**
- **High output signal-to-noise ratio**

APPLICATIONS

- **Multiplexers**
- **Timers**
- **Electronic music synthesizers**
- **Dolby™ HX Systems**
- **Current-controlled amplifiers, filters**
- **Current-controlled oscillators, impedances**

Dolby is a registered trademark of Dolby Laboratories Inc., San Francisco, Calif.

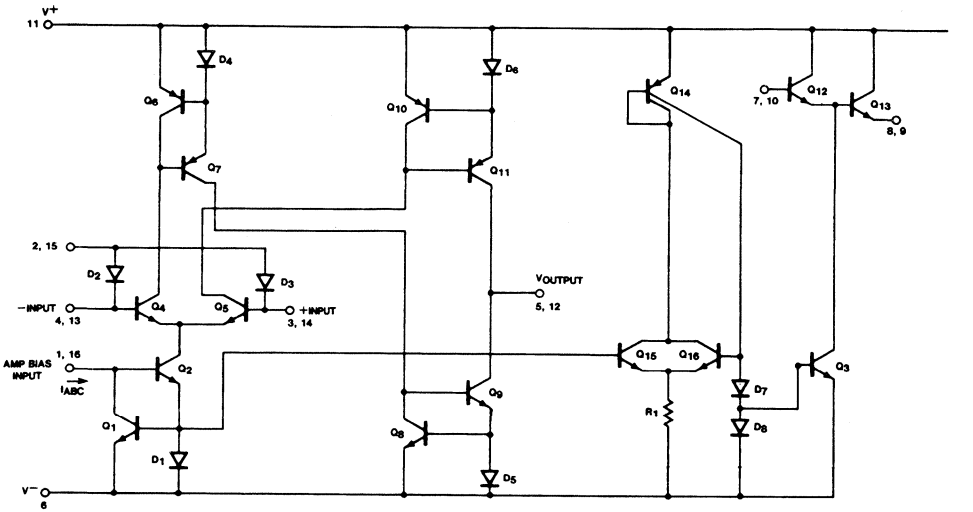
PIN CONFIGURATION



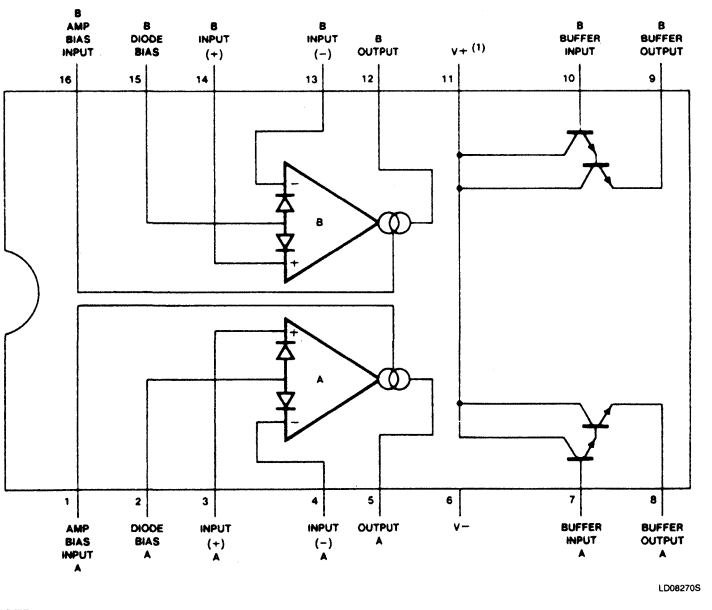
PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	I_{ABC}	Amplifier bias input A
2	D	Diode bias A
3	+ IN	Non-inverting input A
4	− IN	Inverting input A
5	V_O	Output A
6	V−	Negative supply
7	IN_{BUFFER}	Buffer input A
8	VO_{BUFFER}	Buffer output A
9	VO_{BUFFER}	Buffer output B
10	IN_{BUFFER}	Buffer input B
11	V+	Positive supply
12	V_O	Output B
13	− IN	Inverting input B
14	+ IN	Non-inverting input B
15	D	Diode bias B
16	I_{ABC}	Amplifier bias input B

CIRCUIT SCHEMATIC



CONNECTION DIAGRAM



NOTE:
1. V_+ of output buffers and amplifiers are internally connected.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE5517N
16-Pin Plastic DIP	0 to +70°C	NE5517AN
16-Pin SO DIP	0 to +70°C	NE5517D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage[1] NE5517 NE5517A	 36 V_{DC} or ±18 44 V_{DC} or ±22	 V V
P_D	Power dissipation, T_A = 25°C (still air)[2] NE5517N, NE5517AN NE5517D	 1500 1125	 mW mW
V_{IN}	Differential input voltage	±5	V
I_D	Diode bias current	2	mA
I_{ABC}	Amplifier bias current	2	mA
I_{SC}	Output short-circuit duration	Indefinite	
I_{OUT}	Buffer output current[3]	20	mA
T_A	Operating temperature range NE5517N, NE5517AN	 0°C to +70	 °C
V_{DC}	DC input voltage	$+V_S$ to $-V_S$	
T_{STG}	Storage temperature range	−65°C to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. For selections to a supply voltage above ±22V, contact factory.
2. The following derating factors should be applied above 25°C:
   N package at 12.0mW/°C
   D package at 9.0mW/°C
3. Buffer output current should be limited so as to not exceed package dissipation.

DC ELECTRICAL CHARACTERISTICS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	 Over temperature range I_{ABC} 5μA		0.4 0.3	5 5		0.4 0.3	2 5 2	mV mV mV
	$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage		7			7		μV/°C
	V_{OS} including diodes	Diode bias current (I_D) = 500μA		0.5	5		0.5	2	mV
V_{OS}	Input offset change	5μA ≤ I_{ABC} ≤ 500μA		0.1			0.1	3	mV
I_{OS}	Input offset current			0.1	0.6		0.1	0.6	μA
	$\Delta I_{OS}/\Delta T$	Avg. TC of input offset current		0.001			0.001		μA/°C
I_{BIAS}	Input bias current	 Over temperature range		0.4 1	5 8		0.4 1	5 7	μA μA
	$\Delta I_B/\Delta T$	Avg. TC of input current		0.01			0.01		μA/°C

DC ELECTRICAL CHARACTERISTICS[1] (Continued)

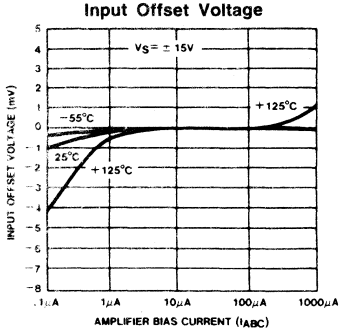
SYMBOL	PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
			Min	Typ	Max	Min	Typ	Max	
g_M	Forward transconductance	Over temperature range	6700 5400	9600	13000	7700 4000	9600	12000	μmho μmho
	g_M tracking			0.3			0.3		dB
I_{OUT}	Peak output current	$R_L = 0$, $I_{ABC} = 5\mu A$ $R_L = 0$, $I_{ABC} = 500\mu A$ $R_L = 0$,	 350 300	5 500	 650	3 350 300	5 500	7 650	μA μA μA
V_{OUT}	Peak output voltage Positive Negative	 $R_L = \infty$, $5\mu A \leq I_{ABC} \leq 500\mu A$ $R_L = \infty$, $5\mu A \leq I_{ABC} \leq 500\mu A$	 +12 −12	 +14.2 −14.4		 +12 −12	 +14.2 −14.4		 V V
I_{CC}	Supply current	$I_{ABC} = 500\mu A$, both channels		2.6	4		2.6	4	mA
	V_{OS} sensitivity Positive Negative	 $\Delta V_{OS}/\Delta V+$ $\Delta V_{OS}/\Delta V-$		 20 20	 150 150		 20 20	 150 150	 μV/V μV/V
CMRR	Common-mode rejection ration		80	110		80	110		dB
	Common-mode range		±12	±13.5		±12	±13.5		V
	Crosstalk	Referred to input[2] 20Hz < f < 20kHz		100			100		dB
I_{IN}	Differential input current	$I_{ABC} = 0$, input = ±4V		0.02	100		0.02	10	nA
	Leakage current	$I_{ABC} = 0$ (Refer to test circuit)		0.2	100		0.2	5	nA
R_{IN}	Input resistance		10	26		10	26		kΩ
B_W	Open-loop bandwidth			2			2		MHz
SR	Slew rate	Unity gain compensated		50			50		V/μs
IN_{BUFFER}	Buff. input current	5		0.4	5		0.4	5	μA
VO_{BUFFER}	Peak buffer output voltage	5	10			10			V
	ΔV_{BE} of buffer	Refer to Buffer V_{BE} test[3] circuit		0.5	5		0.5	5	mV

NOTES:

1. These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, amplifier bias current (I_{ABC}) = 500μA, Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
2. These specifications apply for $V_S = \pm 15V$, $I_{ABC} = 500\mu A$, $R_{OUT} = 5k\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.
3. $V_S = \pm 15$, $R_{OUT} = 5k\Omega$ connected from Buffer output to $-V_S$ and $5\mu A \leq I_{ABC} \leq 500\mu A$.

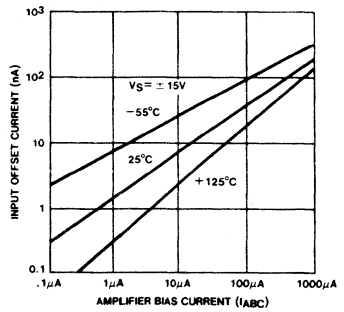
TYPICAL PERFORMANCE CHARACTERISTICS

Input Offset Voltage



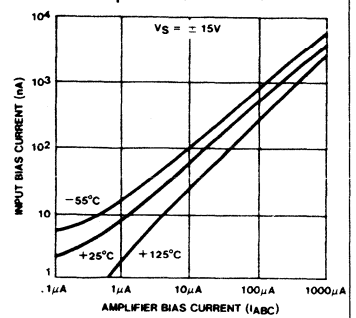
OP19330S

Input Offset Current



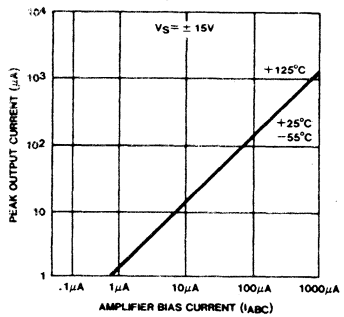
OP19340S

Input Bias Current



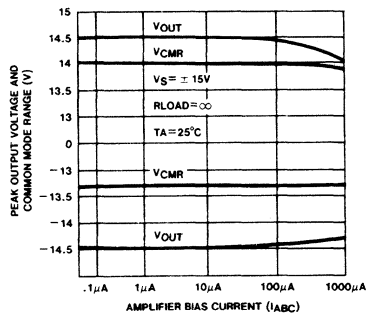
OP19350S

Peak Output Current



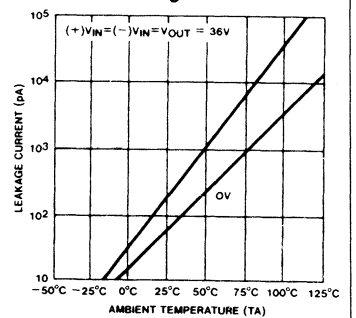
OP19360S

Peak Output Voltage and Common-Mode Range



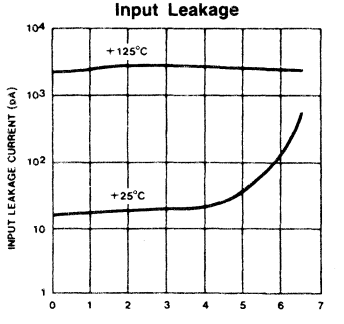
OP19370S

Leakage Current



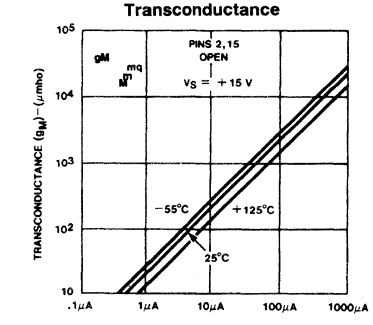
OP19380S

Input Leakage



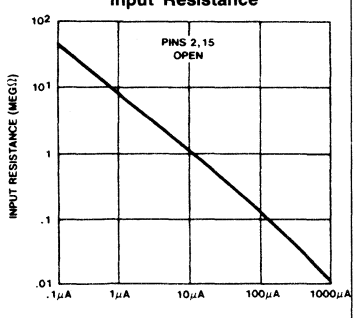
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Transconductance



OP19401S

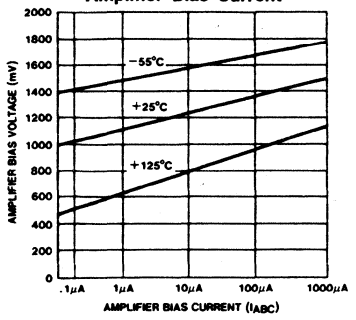
Input Resistance



OP19410S

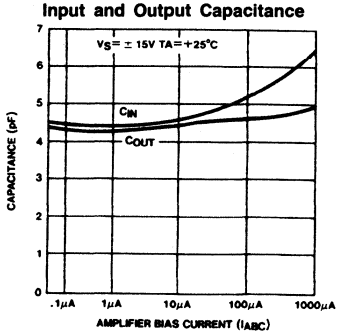
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Amplifier Bias Voltage vs Amplifier Bias Current



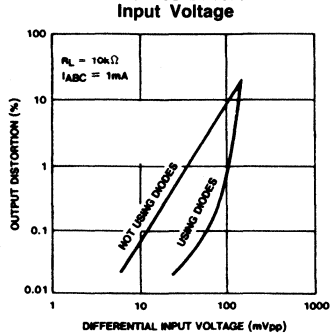
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Input and Output Capacitance



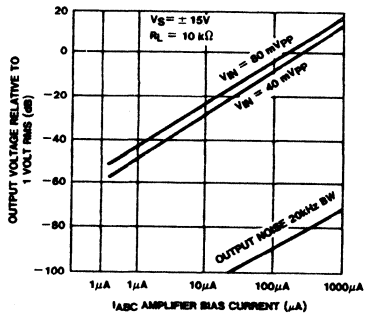
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Distortion vs Differential Input Voltage



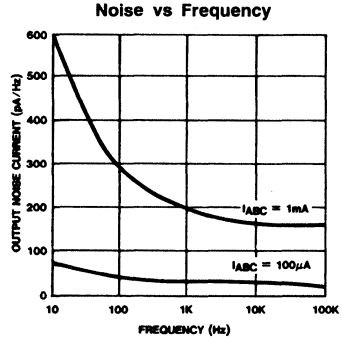
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Voltage vs Amplifier Bias Current



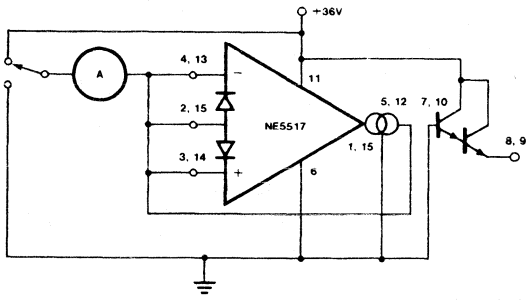
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Noise vs Frequency

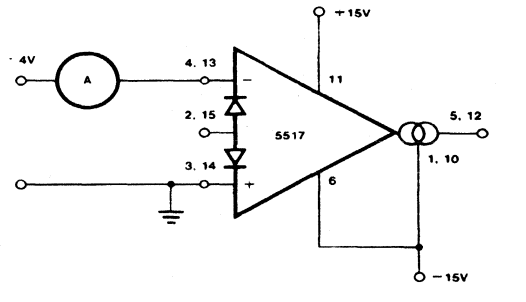


O19450S

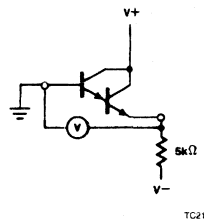
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Leakage Current Test Circuit

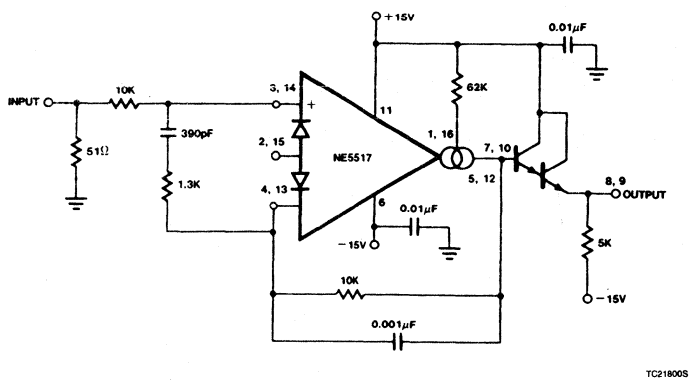


Differential Input Current Test Circuit



Buffer V_{BE} Test Circuit

APPLICATIONS



Unity Gain Follower

CIRCUIT DESCRIPTION

The circuit schematic diagram of one-half of the NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 1.

1. Transconductance Amplifier

The transistor pair, Q_4 and Q_5, forms a transconductance stage. The ratio of their collector currents (I_4 and I_5, respectively) is defined by the differential input voltage, V_{IN}, which is shown in equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

Where V_{IN} is the difference of the two input voltages

$KT \cong 26mV$ at room temperature (300°K).

Transistors Q_1, Q_2 and diode D_1 form a current mirror which focuses the sum of current I_4 and I_5 to be equal to amplifier bias current I_B:

$$I_4 + I_5 = I_B \quad (2)$$

If V_{IN} is small, the ratio of I_5 and I_4 will approach unity and the Taylor series of ln function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

and $I_4 \approx I_5 \approx \frac{1}{2}I_B$

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{\frac{1}{2}I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN}$$

$$I_5 - I_4 = V_{IN} \frac{(I_B q)}{2KT} \quad (4)$$

The remaining transistors (Q_6 to Q_{11}) and diodes (D_4 to D_6) form three current mirrors that produce an output current equal to I_5 minus I_4. Thus:

$$V_{IN} \left\{ I_B \frac{q}{2KT} \right\} = I_O \quad (5)$$

The term $\frac{(I_B q)}{2KT}$ is then the transconductance of the amplifier and is proportional to I_B.

2. Linearizing Diodes

For V_{IN} greater than a few millivolts, equation 3 becomes invalid and the transconductance increases nonlinearly. Figure 2 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume D_2 and D_3 are biased with current sources and the input signal current is I_S. Since

$I_4 + I_5 = I_B$ and $I_5 - I_4 = I_O$, that is:

$I_4 = \frac{1}{2}(I_B - I_O)$, $I_5 = \frac{1}{2}(I_B + I_O)$

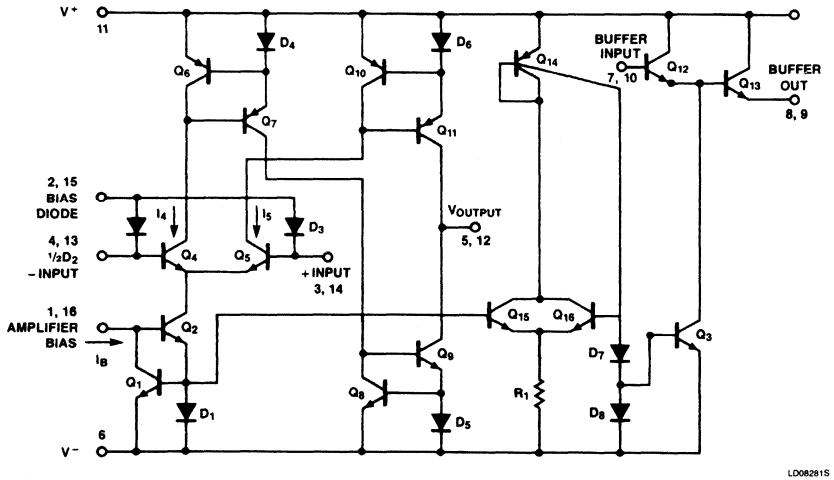


Figure 1. Circuit Diagram of NE5517

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

$$\frac{T}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \ln \frac{\frac{1}{2}(I_B + I_O)}{\frac{1}{2}(I_B - I_O)}$$

$$I_O = I_S \frac{(2^1B)}{I_D} \quad \text{for } |I_S| < \frac{I_D}{2} \qquad (6)$$

The only limitation is that the signal current should not exceed $\frac{1}{2} I_D$.

3. Impedance Buffer

The upper limit of transconductance is defined by the maximum value of I_B (2mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At low values of I_B, a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source (Q_{14}, Q_{15}, Q_{16}, D_7, D_8, and R_1) suits the need.

APPLICATIONS

Voltage-Controlled Amplifier

In Figure 3, the voltage divider R_2, R_3 divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \times \frac{R_3}{R_2 + R_3} \times g_M;$$

$$V_{OUT} = I_{OUT} \times R_L;$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} g_M R_L;$$

$$\boxed{A = \frac{R_3}{R_2 + R_3} \times g_M \times R_L}$$

(3) $g_M = 19.2\ I_{ABC}$

(g_M in μmhos for I_{ABC} in mA)

Since g_M is directly proportional to I_{ABC}, the amplification is controlled by the voltage V_C in a simple way.

When V_C is taken relative to $-V_{CC}$ the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2V is the voltage across two base-emitter baths in the current mirrors. This

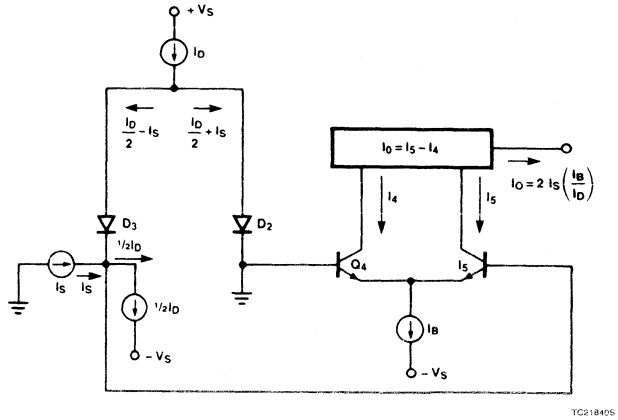


Figure 2. Linearizing Diode

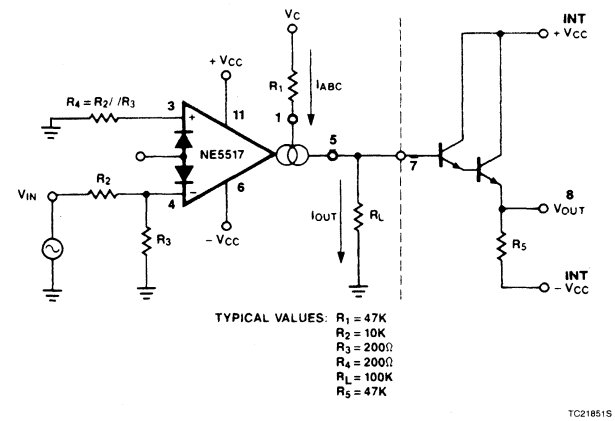


Figure 3

circuit is the base for many applications of the NE5517.

Stereo Amplifier With Gain Control

Figure 4 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3dB is easy to achieve. With the potentiometer, R_P, the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510Ω resistors.

Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to I_{ABC}, the amplification of a signal can be controlled easily. The output current is the product from transconductance × input voltage. The circuit is effective up to approximately 200kHz. Modulation of 99% is easy to achieve.

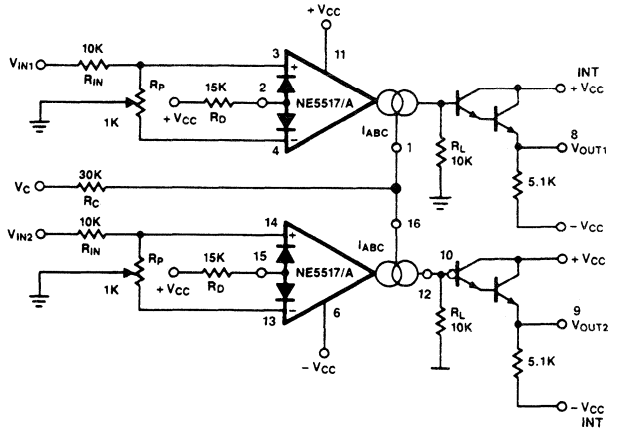


Figure 4. Gain-Controlled Stereo Amplifier

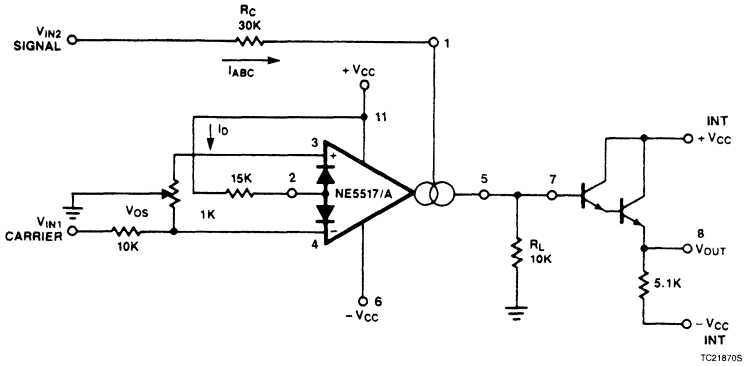


Figure 5. Amplitude Modulator

Voltage-Controlled Resistor (VCR)

Because an OTA is capable of producing an output current proportional to the input voltage, a voltage variable resistor can be made. Figure 6 shows how this is done. A voltage presented at the R_X terminals forces a voltage at the input. This voltage is multiplied by g_M and thereby forces a current through the R_X terminals:

$$R_X = \frac{R + R_A}{g_M \times R_A}$$

where g_M is approximately 19.21 μMHOs at room temperature. Figure 7 shows a Voltage Controlled Resistor using linearizing diodes. This improves the noise performance of the resistor.

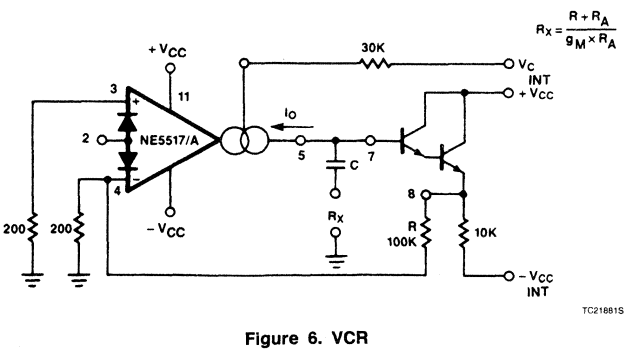


Figure 6. VCR

Voltage-Controlled Filters

Figure 8 shows a Voltage Controlled Low-Pass Filter. The circuit is a unity gain buffer until X_C/g_M is equal to R/R_A. Then, the frequency response rolls off at a 6dB per octave with the −3dB point being defined by the given equations. Operating in the same manner, a Voltage Controlled High-Pass Filter is shown in Figure 9. Higher order filters can be made using additional amplifiers as shown in Figures 10 and 11.

Voltage-Controlled Oscillators

Figure 12 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2Hz to 200kHz is possible by varying I_{ABC} from 1mA to 10μA.

The output amplitude is determined by $I_{OUT} \times R_{OUT}$.

Please notice the differential input voltage is not allowed to be above 5V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 13.

APPLICATION HINTS

To hold the transconductance g_M within the linear range, I_{ABC} should be chosen not greater than 1mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the transistors. The output current range of the DAC normally reaches from 0 to −2mA. In this application, however, the current range is set through R_{REF} (10kΩ) to 0 to −1mA.

$$I_{DAC\ MAX} = 2 \times \frac{V_{REF}}{R_{REF}} = 2 \times \frac{5V}{10k} = 1mA$$

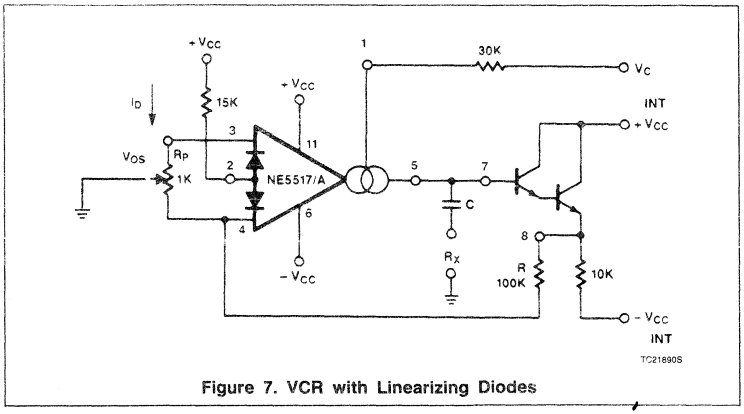
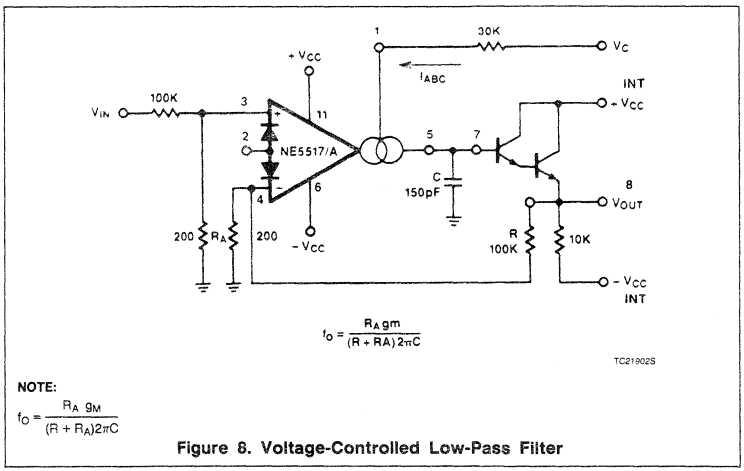


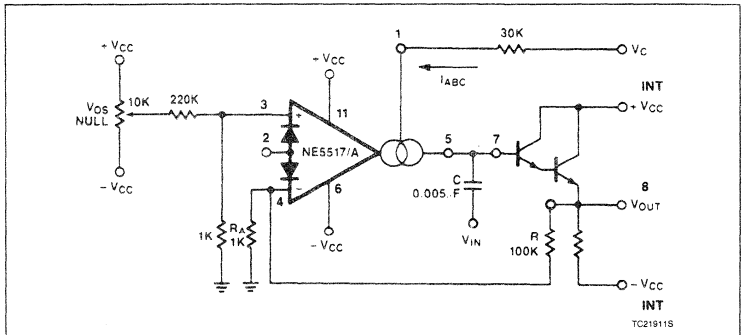
Figure 7. VCR with Linearizing Diodes



NOTE:

$f_O = \frac{R_A\ g_M}{(R + R_A)2\pi C}$

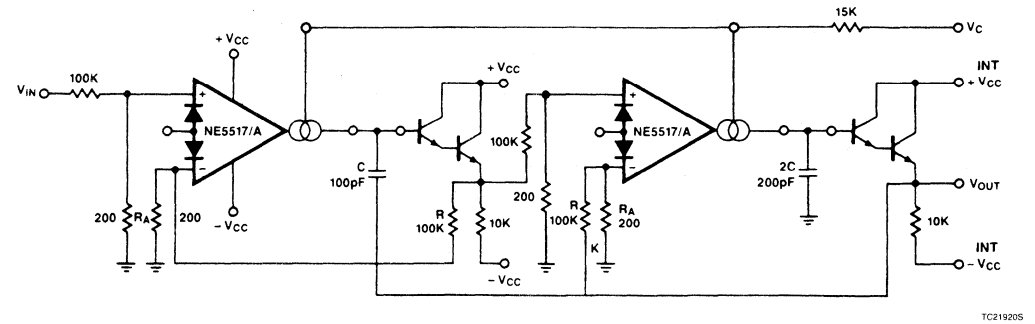
Figure 8. Voltage-Controlled Low-Pass Filter



NOTE:

$f_O = \frac{R_A\ g_M}{(R + R_A)2\pi C}$

Figure 9. Voltage-Controlled High-Pass Filter



NOTE:

$$f_O = \frac{R_A\, g_M}{(R + R_A)2\pi C}$$

Figure 10. Butterworth Filter — 2nd Order

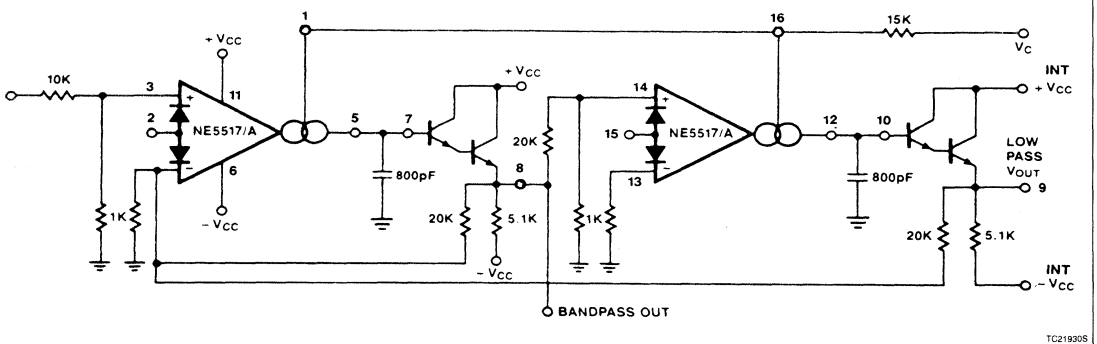


Figure 11. State Variable Filter

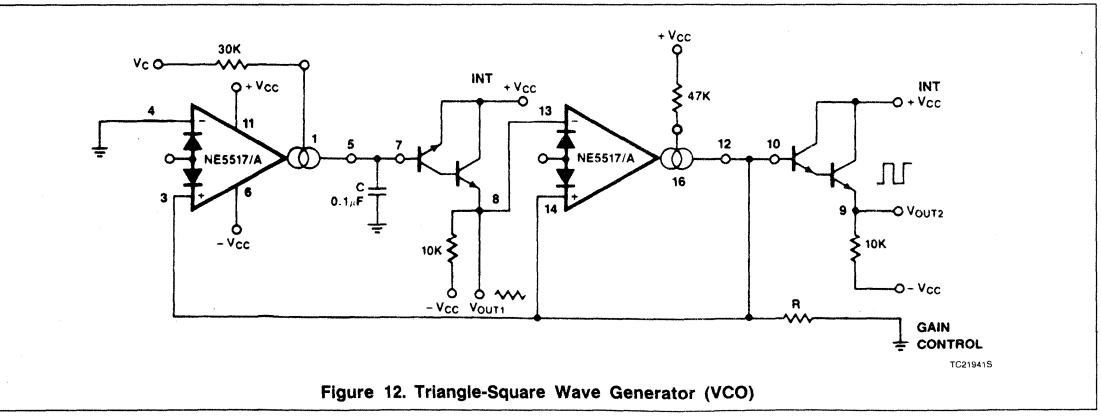
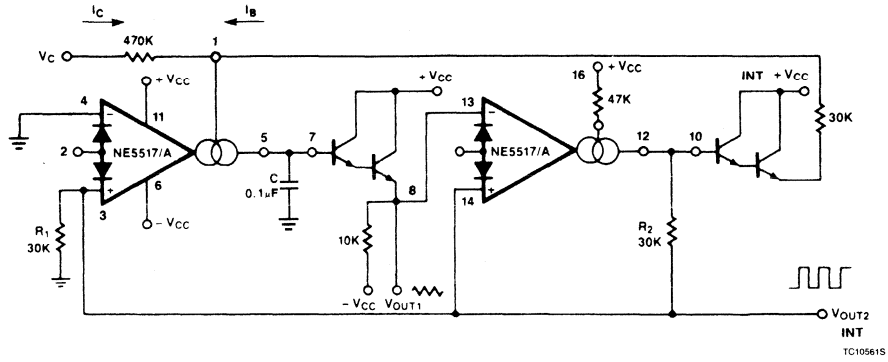


Figure 12. Triangle-Square Wave Generator (VCO)



NOTE:

$$V_{PK} = \frac{(V_C - 0.8)\,R_1}{R_1 + R_2} \quad T_H = \frac{2V_{PK} \times C}{I_B} \quad T_L = \frac{2V_{PK} \times C}{I_C} \quad f_{OSC} \frac{I_C}{2V_{PK} \times C} \quad I_C << I_B$$

Figure 13. Sawtooth Pulse VCO

AN145
NE5517/A Transconductance Amplifier Applications

Application Note

DESCRIPTION

The Signetics NE5517 is a truly versatile dual operational transconductance amplifier. In plain language, it is a voltage-to-current converter governed by the transconductance g_m, which is equivalent to I_{OUT}/V_{IN}. The g_m is increased or decreased linearly by varying the amplifier bias current (I_{ABC}) through an external pin (see Figure 1). From the proper use of the I_{ABC} pin, many control circuits can be realized.

For more insight into the way the part operates, the transconductance can be thought of as gain and is governed by the following equation:

$$g_M = \frac{I_{OUT}}{V_{IN}} = \frac{I_{ABCq}}{2KT} \quad (1)$$

where the transconductance is dependent on the constant KT/q (which is 26mV at 25°C), and I_{ABC} (which is controlled by the user).

To make the device more universal and adaptable for many functions, two impedance buffers for voltage output applications are also included with the amps so that the part can be used as a programmable operational amplifier.

Linearizing diodes provide another useful option. These should be applied when large input voltages or wide temperature variations are encountered. To show the significance of the diodes, compare the difference between Equation 1 without diodes and Equation 2 with diodes:

$$\frac{I_{OUT}}{V_{IN}} = \frac{2\,I_{ABC}}{R_{IN}\,I_D} \quad (2)$$

for I_{IN} greater than $\frac{I_D}{2}$

Here, it can be seen that the transconductance is not temperature dependent. R_{IN} is the signal input resistance and I_{IN} is the signal current. I_{IN} must not exceed half the diode current (I_D, nominally 1mA). The diode current is set by a resistor tied to $+V_{CC}$. A graph showing the output distortion improvement versus differential input voltage when using the diodes is shown in Figure 2.

An advantage that the NE5517 has over similar devices is a special biasing network between the amplifier and output impedance buffers. This network eliminates output offset current changes with a sudden change in the

PIN NO	SYMBOL	NAME AND FUNCTION
1	I_{ABCa}	Amplifier bias input A
2	D_a	Diode bias A
3	$+IN_a$	Non-inverting input A
4	$-IN_a$	Inverting input A
5	I_{OS}	Output A
6	V–	Negative supply
7	IN_{BUFFER}	Buffer input A
8	VO_{BUFFER}	Buffer output A
9	VO_{BUFFER}	Buffer output B
10	IN_{BUFFER}	Buffer input B
11	V+	Positive supply
12	V_O	Output B
13	–IN	Inverting input B
14	+IN	Non-inverting input B
15	D	Diode bias B
16	I_{ABC}	Amplifier bias input B

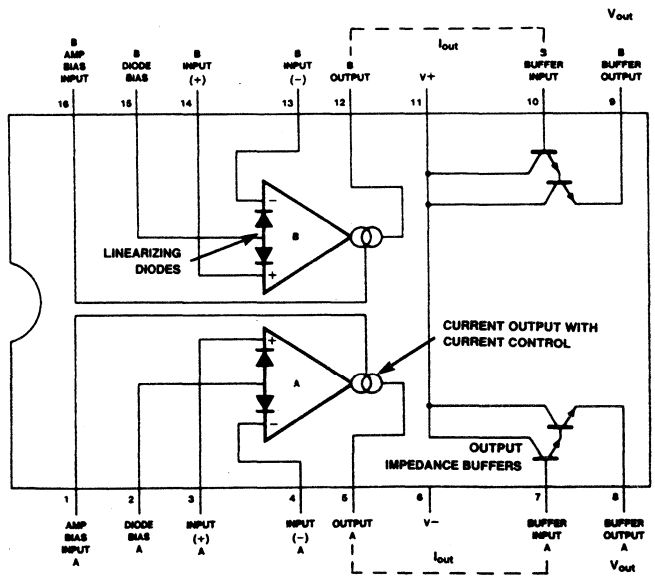


Figure 1. Pin Designation and Functional Diagram

bias current (I_{ABC}). This is particularly important in audio applications where an audible offset would be produced.

APPLICATIONS

An application employing both amplifiers and buffers internal to the NE5517 is the adjustable triangle-square wave generator shown in Figure 3.

The center oscillating frequency is set by the capacitor C at the output of amplifier A. The output amplitude is set by the resistor R connected between the non-inverting inputs, amplifier B output, buffer B input and ground.

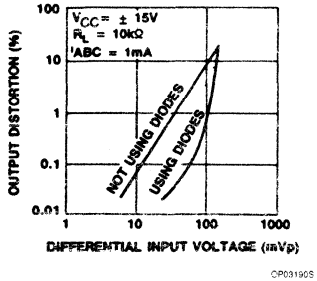


Figure 2. Output Distortion vs Input Voltage Showing Benefit of Diodes

The oscillating frequency is varied by changing V_C, which in turn controls the amplifier bias current (I_{ABC1}). If a positive voltage is applied to V_C, the center frequency will increase linearly with increasing voltage. If a negative is applied, the center frequency will decrease linearly with increasing negative voltage. This makes a very good programmable oscillator with variable amplitude.

By using a large value capacitor and negative control voltage, oscillations in the fractions of Hertz can be realized; a small capacitor and positive control voltage will give frequencies up to 500kHz. Graphs showing the linearity of control voltage versus frequency for different capacitor values are shown in Figure 4.

Pertinent calculations are:

$$f_C = \frac{I_{ABC1}}{4(C)(I_{ABC2})(R)}$$

Where: f_C = center frequency
I_{ABC1} = oscillator control current
I_{ABC2} = amplitude control current
R = amplitude control resistor
C = oscillator control capacitor

Also: Amplitude = (I_{ABC2}) (R)

Another very useful application is to use the NE5517 as a digitally-programmable amplifier. The entire circuit is shown in Figure 5.

The circuit consists of a Signetics microprocessor-compatible DAC, a transistor array, and the NE5517 configured as a voltage-controlled amplifier. This arrangement can also be used with the VCO explained earlier to program its oscillating frequency.

The pertinent equations governing this application are as follows:

$$Av = \frac{V_{OUT}}{V_{IN}} = \frac{BW(10)}{256} \times \frac{I_{DAC\ MAX} \times q \times R_L}{2 \times KT}$$

Where: BW(10) = binary word decimal
$I_{DAC\ MAX}$ = maximum DAC output current (1mA)
R_L = load resistance (30k)
q/KT = 38.5 at 25°C

Also:

$$I_{DAC\ MAX} = 2 \times \frac{V_{REF}}{R_{REF}}$$

$$= 2 \times \frac{5k}{10k} = 1mA$$

Where: V_{REF} = supplied by DAC (5V)
R_{REF} = referenced resistor (10kΩ)

The $I_{DAC\ MAX}$ of 1mA is used to keep the transconductance within the linear range.

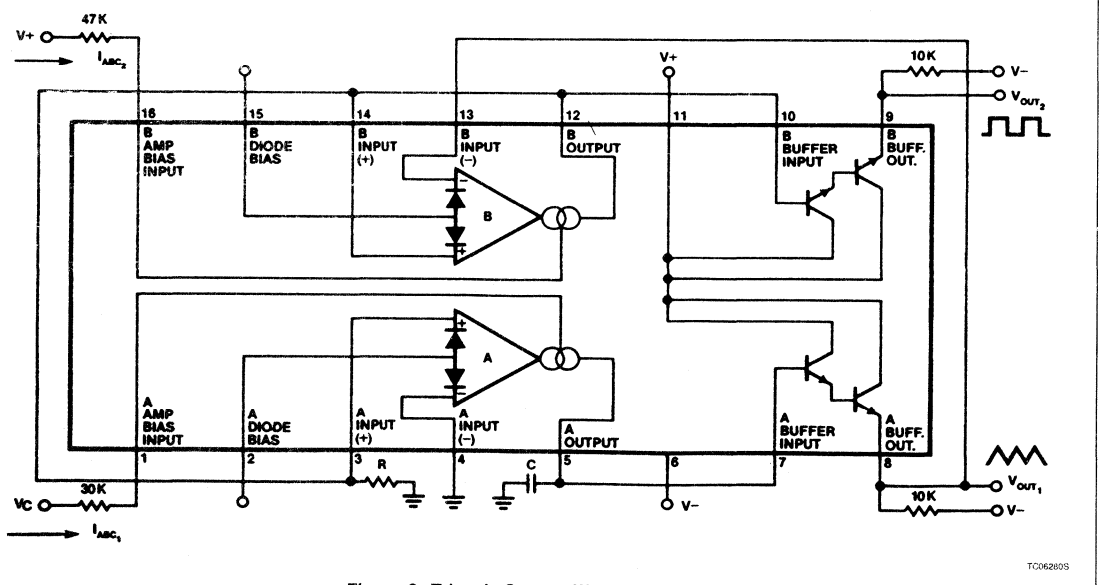
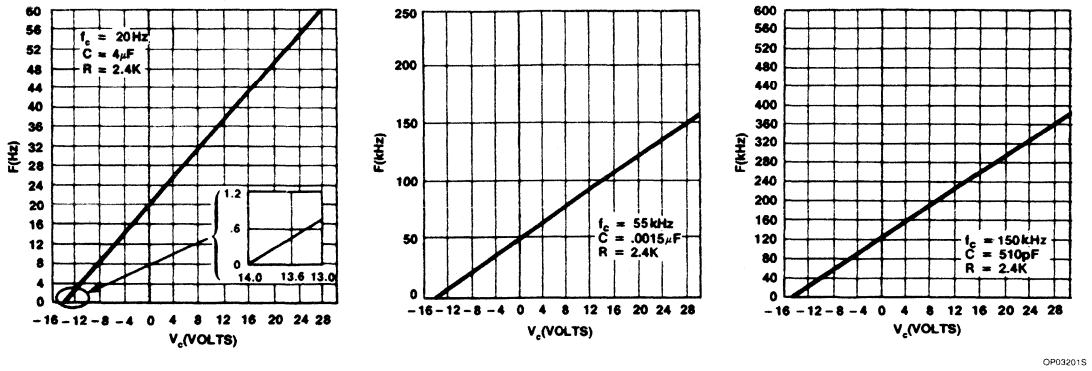


Figure 3. Triangle-Square Wave Generator



a. b. c.

NOTE:
V_C Below −13.6V or above +30V will cause distortion.
Changing the C value will vary the frequency range.

Figure 4. Control Voltage (V_C) vs Frequency Data

The current mirror matches the current flow into the DAC and supplies the same amount to the 5517 control pin. Using a current output DAC is much faster than using a voltage output device to control the part. (If speed is not important, this can be done and the current mirror can be replaced with a resistor.) Also, the gain equation pertains to the signal after the input divider.

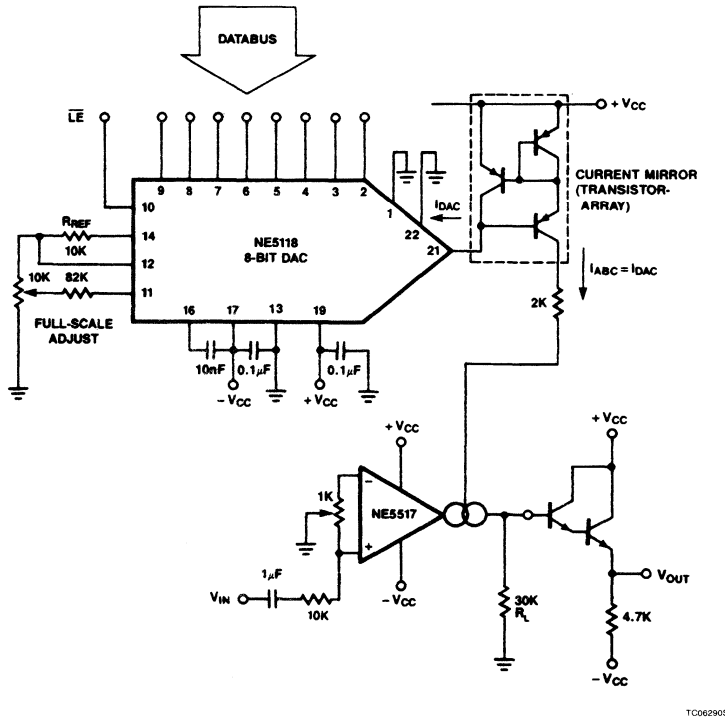


Figure 5. Digitally-Programmable Amplifier

Preamplifiers

		page
NE542	dual low-noise preamplifier	315
AN190	applications of low noise stereo amplifiers: NE542	319

NE542
Dual Low-Noise Preamplifier

Product Specification

DESCRIPTION

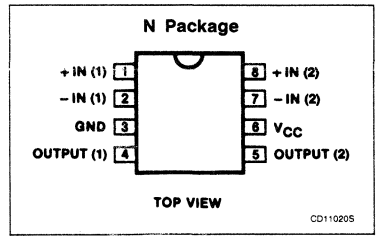
The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110dB supply rejection and 70dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing ($V_{CC}-2V_{P-P}$), and internal compensation to 10dB. The NE542 operates from a single supply across a range of 9 to 24V.

The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplification of small signals.

FEATURES

- **Low noise — 0.7μV total input noise**
- **High gain — 104dB open-loop**
- **Single supply operation**
- **Wide supply range 9 to 24V**
- **Power supply rejection 110dB**
- **Large output voltage swing ($V_{CC}-2V_{P-P}$)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 100kHz ($15V_{P-P}$)**
- **Internally-compensated (stable at 10dB)**
- **Short-circuit protected**
- **High slew rate 5V/μs**

PIN CONFIGURATION



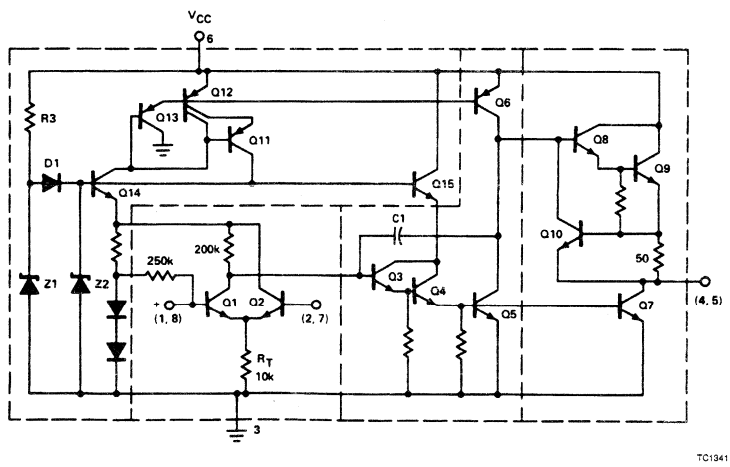
APPLICATIONS

- **Tape preamplifier**
- **Phono preamplifier**
- **Microphone preamplifier**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE542N

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+24	V
P_D	Power dissipation	500	mW
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	= dc

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 14V$, unless otherwise specified.

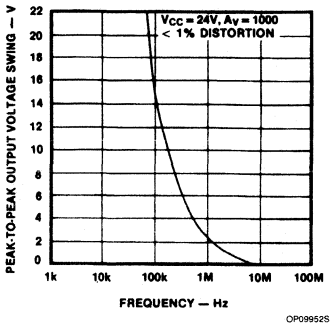
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		9		24	V
I_{CC}	Supply current	$V_{CC} = 9$ to 18V, $R_L = \infty$		9	15	mA
R_{IN}	Input resistance Positive input Negative input			 100 200		 kΩ kΩ
R_{OUT}	Output resistance	Open-loop		150		Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 14V$, unless otherwise specified.

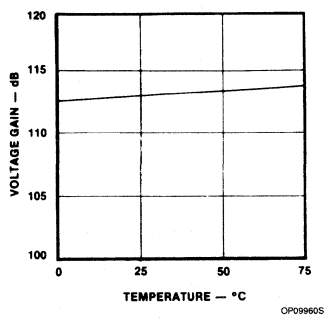
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
A_V	Voltage gain	Open-loop		160,000		V/V
I_{IN}	Negative Input current				0.5	
I_{OUT}	Output current	Source Sink (linear operation)	8 2	14 3		mA mA
V_{OUT}	Output voltage swing		V_{CC} −2.5	V_{CC} −2		V
SR	Small signal bandwidth Slew rate			15 5		MHz V/μs
P_{BW}	Power bandwidth	$15V_{P-P}$		100		kHz
V_{IN}	Maximum input voltage	Linear operation, < 2.5% distortion			300	mV_{RMS}
PSRR	Power supply rejection ratio	f = 60, 120Hz f = 1kHz		100 110		dB dB
	Channel separation	f = 1kHz	40	70		dB
THD	Total harmonic distortion	40dB gain, f = 1kHz		0.1	0.3	%
	Total equivalent input noise	$R_S = 600\Omega$, 100 – 10,000Hz		0.7	1.2	μV_{RMS}
	Noise figure	$R_S = 50k\Omega$, 10 – 10,000Hz $R_S = 20k\Omega$, 10 – 10,000Hz $R_S = 10k\Omega$, 10 – 10,000Hz $R_S = 5k\Omega$, 10 – 10,000Hz		1.2 1.2 1.5 2.4		dB dB dB dB

TYPICAL PERFORMANCE CHARACTERISTICS

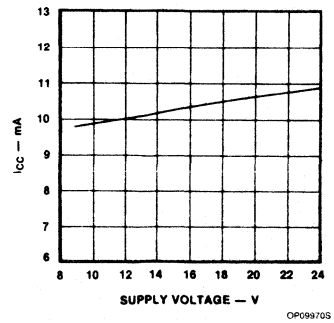
Large-Signal Frequency Response



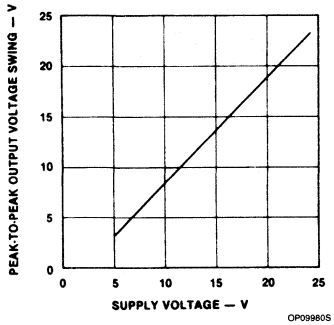
Gain vs Temperature



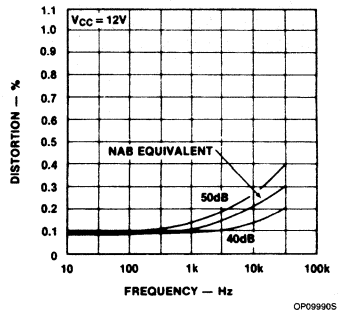
V_{CC} vs I_{CC}



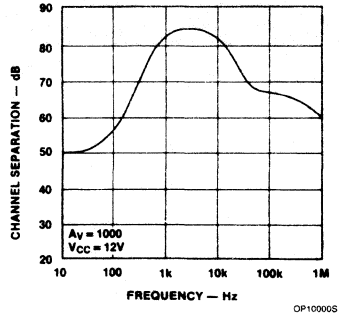
Peak-to-Peak Output Voltage Swing vs V_{CC}



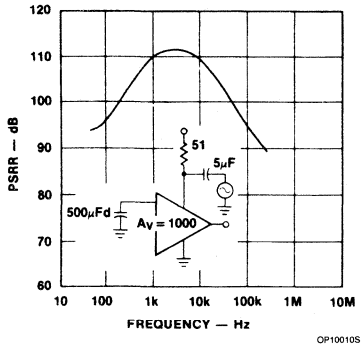
% Distortion



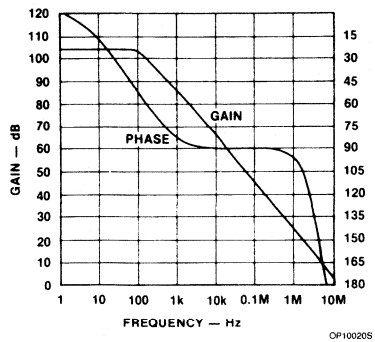
Channel Separation



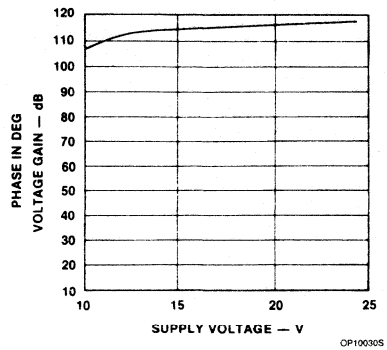
PSRR vs Frequency



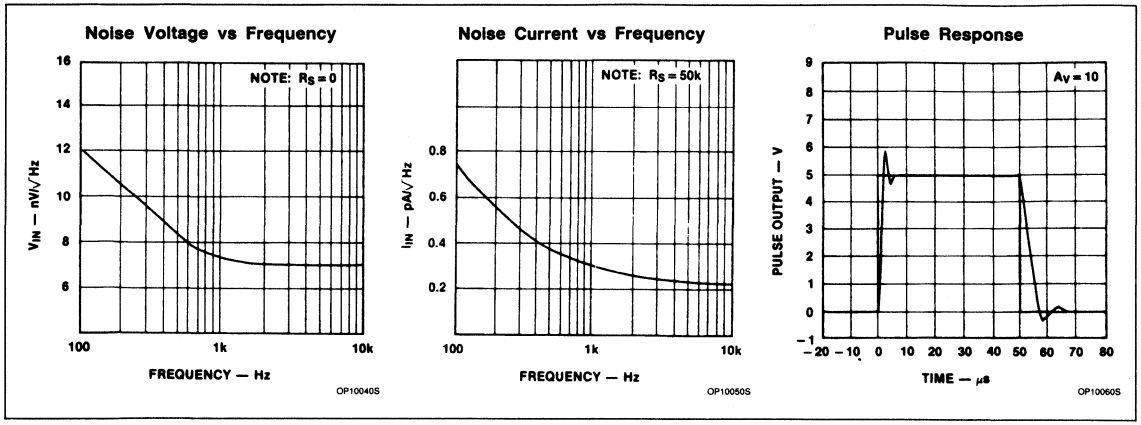
Gain and Phase Response



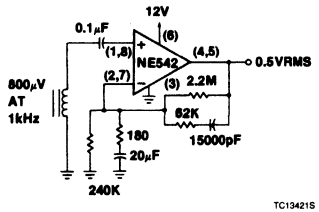
Voltage Gain vs Supply Voltage



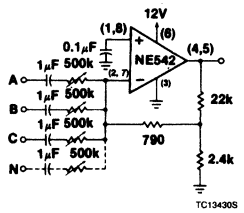
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



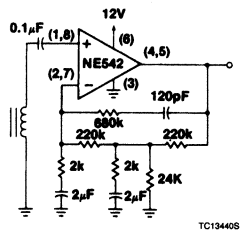
TYPICAL APPLICATIONS



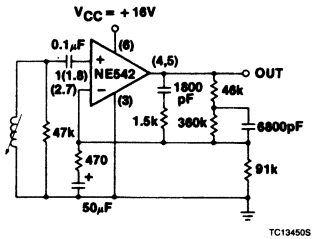
Typical Tape Playback Amplifier



Audio Mixer



Two-Pole Fast Turn-On NAB Tape Preamp



RIAA Magnetic Phono Preamp

NOTE:
All resistor values are typical and in ohms.

AN190
Applications of Low Noise Stereo Amplifiers: NE542

Application Note

Introduction

Stereo preamplifiers have come into greater and greater demand with the increased usage of tape recorders. With stereophonic recording systems, the need increased to have multiple devices in the same package to insure greater thermal tracking and packing density, without sacrificing performance.

The NE542 qualifies as a low noise dual preamplifier. The NE542 is an 8-pin dual in-line device.

This device has greater than 100dB open-loop gain and (15 – 20) MHz gain bandwidth product. In selecting the proper "low noise" preamplifier, several factors must be considered.

1. Frequency shaping characteristic required.
2. Closed-loop response with respect to a system reference level.
3. Response of the record/playback head.
4. System distortion requirements.
5. Response of the tape used.

The following will deal with Items 1, 2, and 4.

When approaching the design criteria of Item 2, the designer should be concerned with the open-loop device characteristics. These characteristics will aid in determining the maximum boost available, knowing that a specific loop gain (open-loop gain minus closed-loop gain) will be necessary to keep the system distortion low and maintain the output impedance of the "low noise" preamplifier constant over the required operating frequency range.

RIAA standards call for a maximum recording velocity of 21cm/sec for stereo discs. This worst-case velocity describes a limit for the preamplifier gain because the input signal at this velocity is maximum.

NAB TAPE EQUALIZATION

Recording and playback characteristics of magnetic tape and record/playback heads are not flat but exhibit a loss at high frequencies and a boost at lower frequencies. To obtain an overall flat frequency response and improved signal-to-noise ratio, the audio signals are equalized by boosting the higher frequencies in amplitude before recording. Playback amplifiers must exhibit bass boost to remove the effects of pre-emphasis for an overall flat response.

Known as the NAB equalization curve, the standard deemphasis employs attenuation from the turnover frequency of 50Hz to the turnover frequency of 3180Hz for 7.5Ips recording. The slower recording speed of 3.75Ips employs turnover frequencies of 50Hz and 1326Hz. These curves are shown in Figure 1. A reference level of 800μV head sensitivity at 1kHz is also used by the NAB.

STEREO PREAMPLIFICATION

The voltage level appearing at the output of tape playback heads and some phono cartridges are too small to be useful without a large amount of low noise preamplification. In addition to providing low noise amplification, the preamplifier should possess enough open-loop gain so that the RIAA and NAB equalization curves can be produced in the feedback networks of the amplifier. The following paragraphs describe the characteristics and applications of the 542. This device provides a matched pair of amplifiers which have been specifically designed to minimize amplifier noise and maximize signal-to-noise ratio.

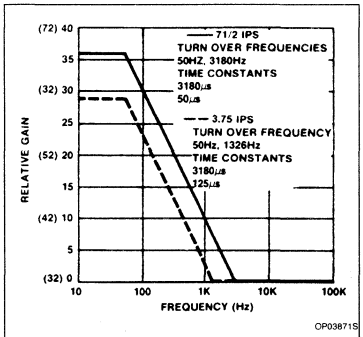


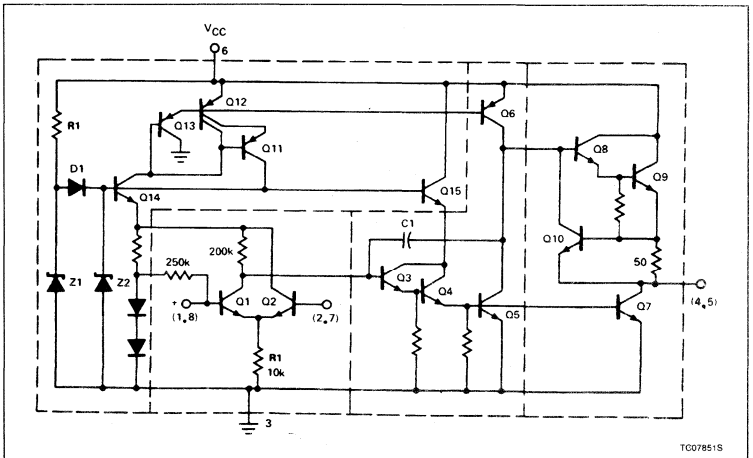
Figure 1. Tape Equalization Curves

NE542 DEVICE DESCRIPTION

The NE542 is a dual low noise amplifier with 104dB open-loop gain produced by two stages of voltage gain followed by one stage of current gain.

In the design of low noise devices, special attention must be focused on the input stage. If differential topography is used, the stage should be designed so that one of the differential transistors is turned off. This reduces the noise contribution by a factor of 1.4 since only one transistor is producing noise. Current sources and mirrors cannot be used for biasing loads because active elements will contribute more noise.

Implementing these observations, the first gain stage of the NE542 is pictured with the complete schematic in Figure 2.



NOTE:
All resistor values are in Ω.

Figure 2. Equivalent Schematic NE542

Applications of Low Noise Stereo Amplifiers: NE542 AN190

Although the differential input configuration degrades the noise performance slightly, using differential inputs has the advantage of higher input impedance, allowing smaller capacitors and larger resistors to be used to achieve the RIAA and NAB curves.

The second stage is a common-emitter amplifier (Q_5) with a current source load (Q_6). The Darlington emitter-follower $Q_3 - Q_4$ provides level shifting and current gain to the common-emitter stage (Q_5) and the output current sink (Q_7). The voltage gain of the second stage is approximately 2000, making the total gain of the amplifier typically 160,000 in the differential input configuration.

The preamplifier is internally-compensated with the pole-spiitting capacitor, C1. This compensates to unity gain at 15MHz. The compensation is adequate to preserve stability to a closed-loop gain of 10.

BIASING

The non-inverting input has been internally-biased from a 1.4V internal voltage source. Following the zero differential rule of amplifiers, the output voltage will be set by the resistor feedback network (R4 and R5) of Figure 3.

The base of Q2 requires 0.5μA bias current. Hence R5 should pass 5μA minimum for stability, for an output DC voltage of $\frac{V_{CC}}{2}$ the values of R4 and R5 are:

$$R5 = \frac{2V_{BE}}{10\ I_B} = 240k\Omega \text{ Max.} \quad (1)$$

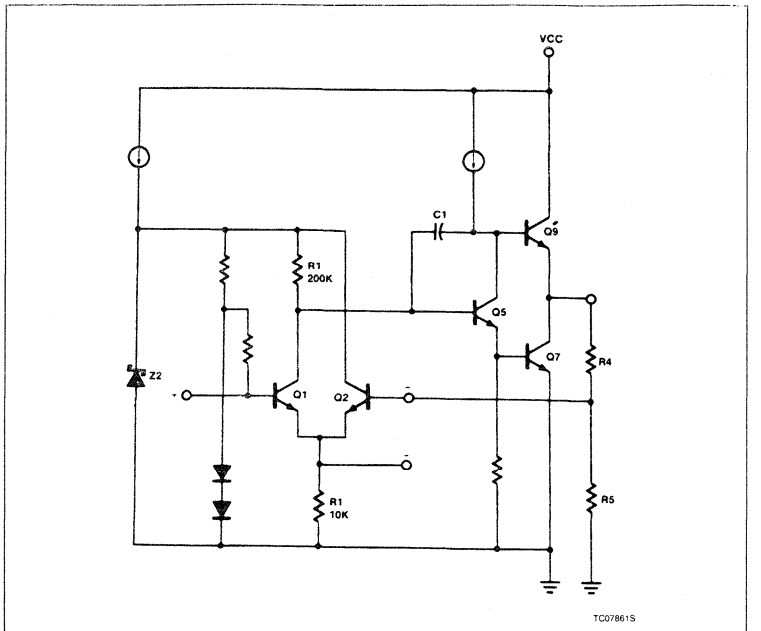
$$R4 = \left(\frac{V_{CC}}{2.8 - 1} \right) \times R5 \quad (2)$$

DC amplifier gain is defined by the ratio of R4 and R5. Open-loop AC gain can be regained by adding a shunt capacitor across R5. The low frequency 3dB corner is then defined by the capacitor-resistor break point.

NAB Tape Preamplifier

Design of a preamplifier begins by determining the gain and output signal amplitudes in reference to the standard 800μV input signal level. For the following design example, we will use the 542 to achieve a 100mV output level at 1kHz following the 7.5Ips NAB equalization curve. The graph of Figure 1 has been calibrated both in absolute gain for this example and relative gain for general use.

From the given parameters, the closed-loop gain becomes 32dB at the highest frequency of interest. The NAB response is achieved by adding frequency-selective AC feedback as depicted by Figure 4. Resistors R4 and R5 select the DC gain as defined by Equations 1 and 2. Placing a value of 200k upon R5, Equation 2 yields a value of 680kΩ.



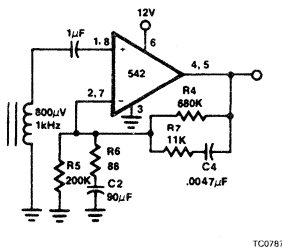
NOTE:
All resistor values are in Ω.

Figure 3. Differential Input Biasing NE542

The lower corner frequency is determined next by the reactance of C4 and R4 such that:

$$f_1 = \frac{0.159}{C4\ R4} \quad (3)$$

Solving for C4 yields a value of 0.0047μF.



NOTE:
All resistor values are in Ω.

Figure 4. NAB Response Amplifier

The upper corner frequency, f_2, is similarly fixed by the reactance of C4 and R7.

$$f_2 = \frac{0.159}{C4\ R7} \quad (4)$$

Then solving Equation 4 for R7 defines a value of 11kΩ.

Midband gain is now fixed by the relationship.

$$A = \frac{R6 + R7}{R6} \quad (5)$$

Solving for the 1kHz gain of 42dB using 11k for R7 yields a value of 88Ω for R6. The final calculation of the low frequency cut-off of the preamp determines the size of C2.

$$C2 = \frac{0.159}{f_{CUTOFF}\,R6} \quad (6)$$

Typical Applications

In addition to the previous detailed design examples, the following general amplifier configurations (see Figures 5 through 8) are presented. The choice of design and the device used is a function of the desired complexity and overall performance.

Applications of Low Noise Stereo Amplifiers: NE542

AN190

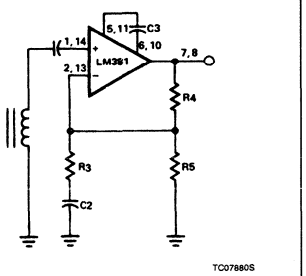


Figure 5. Flat Response Tape Amplifier

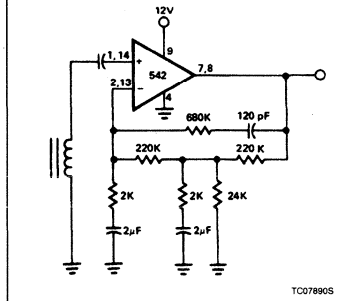
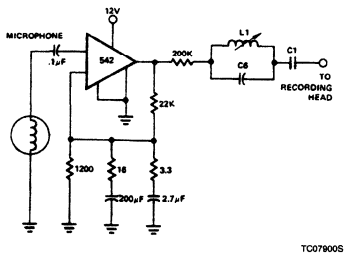


Figure 6. Two-Pole Fast Turn-On NAB Type Preamp



NOTE:
All resistor values are in Ω.

Figure 7. Typical NAB Record Preamplifier

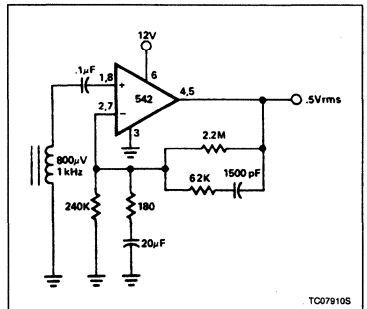


Figure 8. Typical Tape Playback Amplifier

Fibre optic amplifiers

		page
NE5210	transimpedance amplifier (280 MHz)	325
NE5211	transimpedance amplifier (180 MHz)	339
NE5212	transimpedance amplifier (140 MHz)	353
NE5214	post amplifier with link status indicator	367
NE5217	post amplifier with link status indicator	374
SA5211	transimpedance amplifier (180 MHz)	339
SA5212	transimpedance amplifier (140 MHz)	253
SA5214	post amplifier with link status indicator	367
SA5217	post amplifier with link status indicator	374
SE5212	transimpedance amplifier (140 MHz)	353

NE5210
Transimpedance Amplifier (280MHz)

Preliminary Specification

DESCRIPTION

The NE5210 is a 7kΩ transimpedance wide band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber-optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

FEATURES

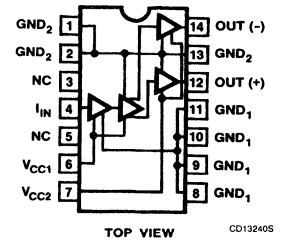
- **Low noise: 3.5pA/√Hz**
- **Single 5V supply**
- **Large bandwidth: 280MHz**
- **Differential outputs**
- **Low input/output impedances**
- **High power supply rejection ratio**
- **High overload threshold current**
- **Wide dynamic range**
- **7kΩ differential transresistance**

APPLICATIONS

- **Fiber-optic receivers, analog and digital**
- **Current-to-voltage converters**
- **Wideband gain block**
- **Medical and scientific instrumentation**
- **Sensor preamplifiers**
- **Single-ended to differential conversion**
- **Low noise RF amplifiers**
- **RF signal processing**

PIN CONFIGURATION

D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE5210D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	6	V
T_A	Operating ambient temperature range	0 to +70	°C
T_J	Operating junction temperature range	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{DMAX}	Power dissipation T_A = 25°C (still air)[1]	1.0	W
I_{INMAX}	Maximum input current[2]	5	mA

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance: θ_{JA} = 125°C/W.
2. The use of a pull-up resistor to V_{CC} for the PIN diode, is recommended.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature range	0 to +90	°C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature range at V_{CC} = 5V, unless otherwise specified. Typical data applies at V_{CC} = 5V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	V
$V_{O\pm}$	Output bias voltage		2.8	3.3	3.7	V
V_{OS}	Output offset voltage			0	80	mV
I_{CC}	Supply current		21	26	32	mA
I_{OMAX}	Output sink/source current[1]		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 8, Procedure 2	±120	±160		μA
I_{INMAX}	Maximum input current overload threshold	Test Circuit 8, Procedure 4	±160	±240		μA

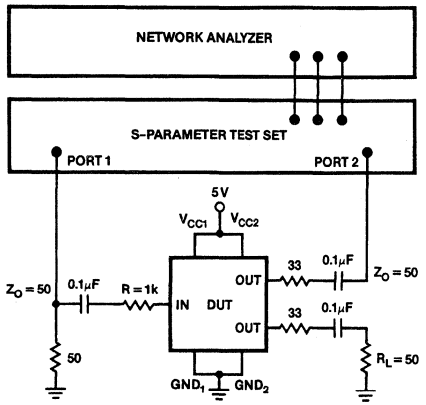
NOTE:
1. Test condition: output quiescent voltage variation is less than 100mV for 3mA load current.

AC ELECTRICAL CHARACTERISTICS Typical data and Min/Max limits apply at V_{CC} = 5V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$ Test Circuit 8, Procedure 1	4.9	7	10	kΩ
R_O	Output resistance (differential output)	DC tested	16	30	42	Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$	2.45	3.5	5	kΩ
R_O	Output resistance (single-ended output)	DC tested	8	15	21	Ω
f_{3dB}	Bandwidth (-3dB)	Test Circuit 1, T_A = 25°C	200	280		MHz
R_{IN}	Input resistance			60		Ω
C_{IN}	Input capacitance			7.5		pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	V_{CC} = 5± 0.5V		9.6	20	%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\,MAX} - T_{A\,MIN}$		0.05	0.1	%/°C
I_N	RMS noise current spectral density (referred to input)	f = 10MHz, T_A = 25°C, Test Circuit 2		3.5	6	pA/$\sqrt{Hz}$
I_T	Integrated RMS noise current over the bandwidth (referred to input) $C_S = 0$[1]	T_A = 25°C Test Circuit 2				
		Δf = 100MHz		37		nA
		Δf = 200MHz		56		nA
		Δf = 300MHz		71		nA
	C_S = 1	Δf = 100MHz		40		nA
		Δf = 200MHz		66		nA
		Δf = 300MHz		89		nA
PSRR	Power supply rejection ratio[2] ($V_{CC1} = V_{CC2}$)	Dc tested, ΔV_{CC} = 0.1V Equivalent AC test circuit 3	20	36		dB
PSRR	Power supply rejection ratio[2] (V_{CC1})	DC tested, ΔV_{CC} = 0.1V Equivalent AC test circuit 4	20	36		dB
PSRR	Power supply rejection ratio[2] (V_{CC2})	DC tested, ΔV_{CC} = 0.1V Equivalent AC test circuit 5		65		dB
PSRR	Power supply rejection ratio[2] (ECL configuration)	f = 0.1MHz, Test Circuit 6		23		dB
V_{OMAX}	Maximum output voltage swing differential	$R_L = \infty$ Test Circuit 8, Procedure 3	2.4	3.2		V_{P-P}
V_{INMAX}	Maximum input amplitude for output duty cycle of 50± 5%[3]	Test Circuit 7	650			mV_{P-P}
t_R	Rise time for 50 mV_{P-P} output signal[4]	Test Circuit 7		0.8	1.2	ns

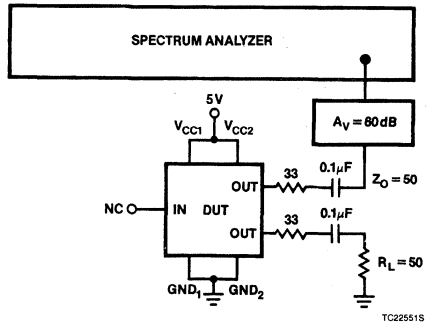
NOTES:
1. Package parasitic capacitance amounts to about 0.2pF.
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} line.
3. Guaranteed by linearity and overload tests.
4. t_R defined as 20 – 80% rise time. It is guaranteed by a -3dB bandwidth test.

TEST CIRCUITS



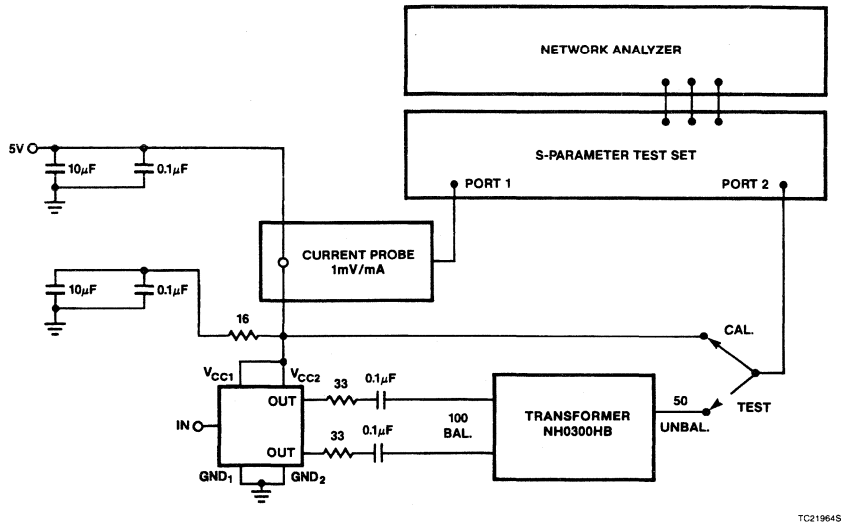
SINGLE-ENDED	DIFFERENTIAL
$R_T \cong \frac{V_{OUT}}{V_{IN}} R = 2 \times S21 \times R$	$R_T = \frac{V_{OUT}}{V_{IN}} R = 4 \times S21 \times R$
$R_O \cong Z_O \left\lvert \frac{1+S22}{1-S22} \right\rvert - 33$	$R_O = 2Z_O \left\lvert \frac{1+S22}{1-S22} \right\rvert - 66$

Test Circuit 1

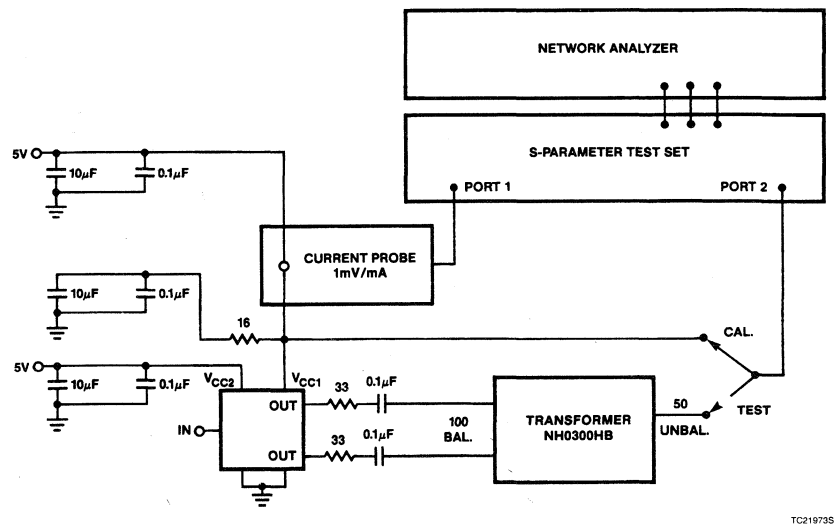


Test Circuit 2

TEST CIRCUITS (Continued)

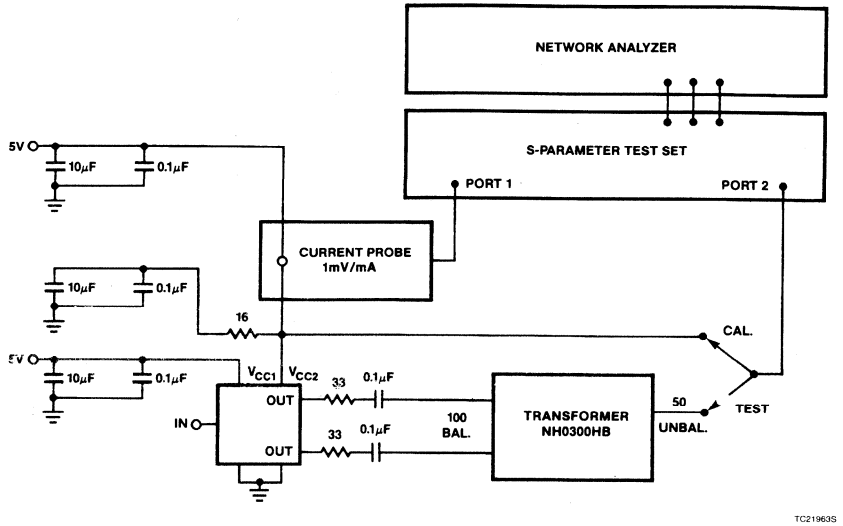


Test Circuit 3

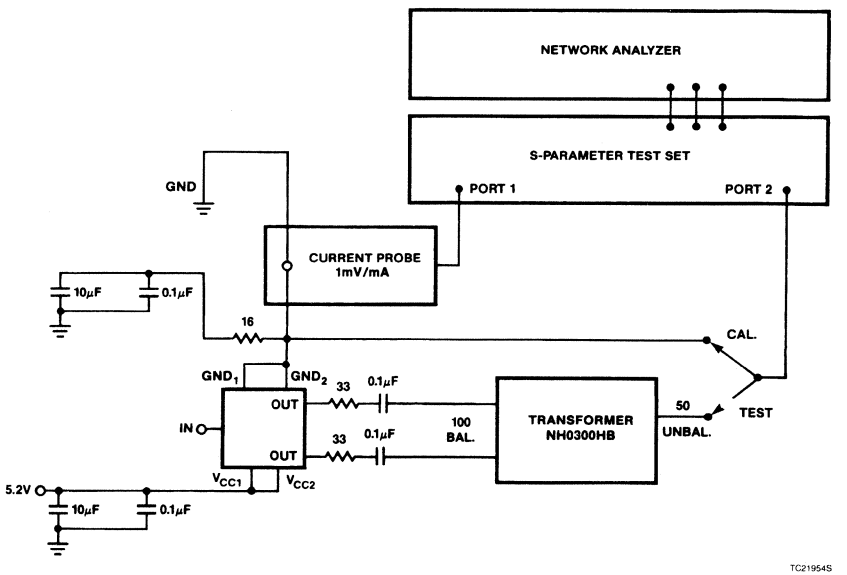


Test Circuit 4

TEST CIRCUITS (Continued)

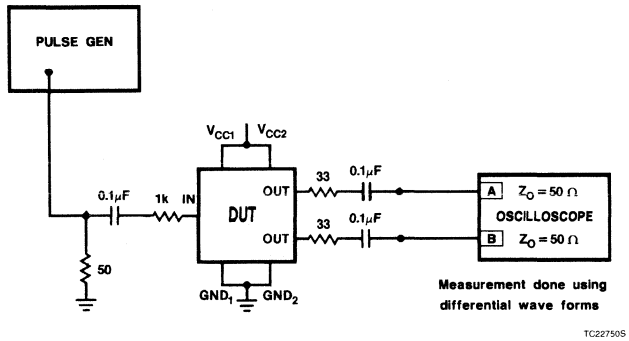


Test Circuit 5



Test Circuit 6

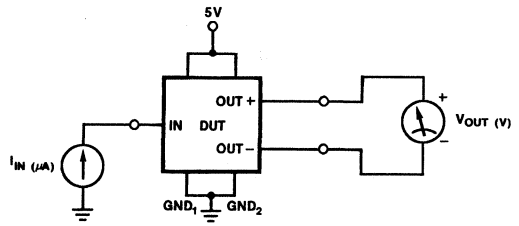
TEST CIRCUITS (Continued)



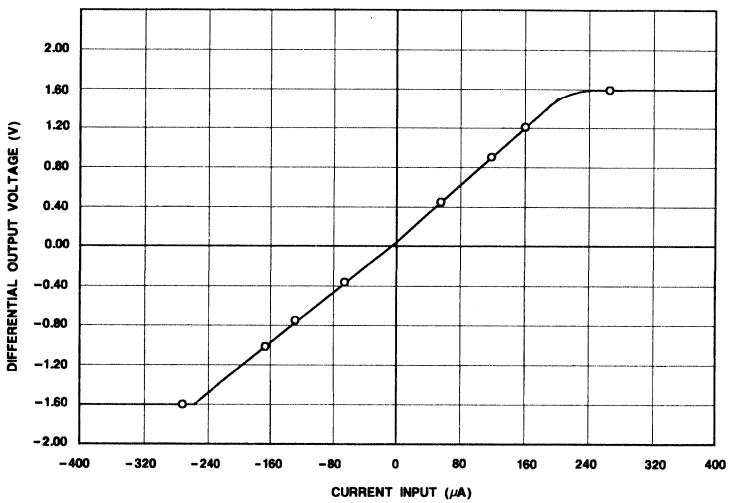
Test Circuit 7

TEST CIRCUITS (Continued)

Typical Differential Output Voltage vs Current Input



TC23460S



OP20990S

NE5210 TEST CONDITIONS

Procedure 1

R_T measured at 60μA
$R_T = (V_{O1} - V_{O2})/(+60\mu A - (-60\mu A))$
Where: V_{O1} Measured at $I_{IN} = +60\mu A$
V_{O2} Measured at $I_{IN} = -60\mu A$

Procedure 2

Linearity = 1 – ABS$((V_{OA} - V_{OB})/(V_{O3} - V_{O4}))$
Where: V_{O3} Measured at $I_{IN} = +120\mu A$
V_{O4} Measured at $I_{IN} = -120\mu A$
$V_{OA} = R_T * (+120\mu A) + V_{O8}$
$V_{OB} = R_T * (-120\mu A) + V_{O8}$

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$
Where: V_{O7} Measured at $I_{IN} = +260\mu A$
V_{O8} Measured at $I_{IN} = -260\mu A$

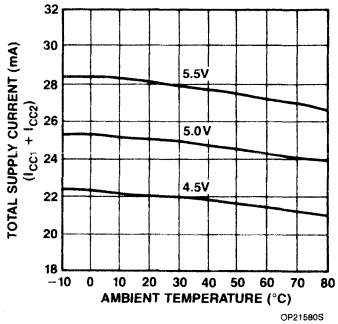
Procedure 4

$I_{IN\ MAX}$ Test Pass Conditions:
$V_{O7} - V_{O5} > 20mV$ and $V_{O6} - V_{O5} > 20mV$
Where: V_{O5} Measured at $I_{IN} = +160\mu A$
V_{O6} Measured at $I_{IN} = -160\mu A$
V_{O7} Measured at $I_{IN} = +260\mu A$
V_{O8} Measured at $I_{IN} = -260\mu A$

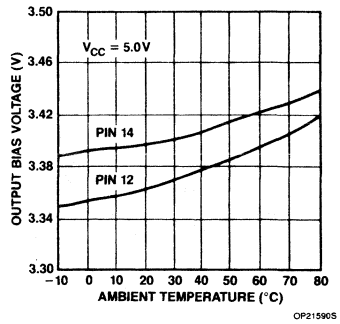
Test Circuit 8

TYPICAL PERFORMANCE CHARACTERISTICS

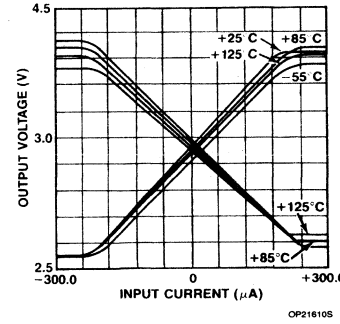
NE5210 Supply Current vs Temperature



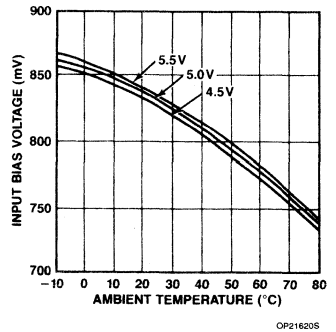
NE5210 Output Bias Voltage vs Temperature



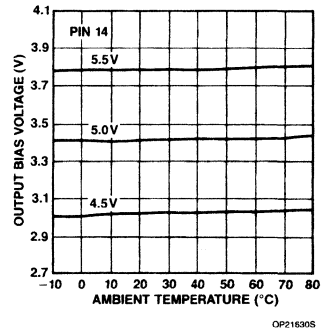
Output Voltage vs Input Current



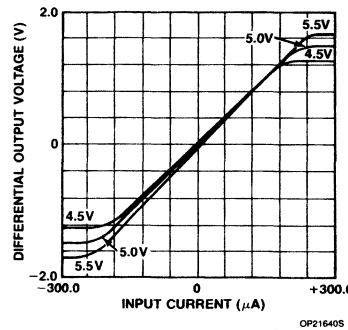
NE5210 Input Bias Voltage vs Temperature



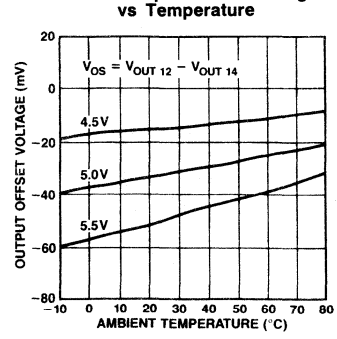
NE5210 Output Bias Voltage vs Temperature



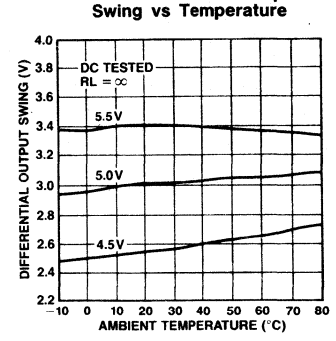
Differential Output Voltage vs Input Current



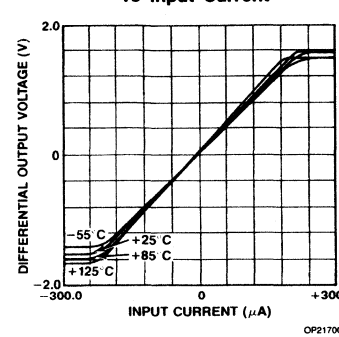
NE5210 Output Offset Voltage vs Temperature



NE5210 Differential Output Swing vs Temperature

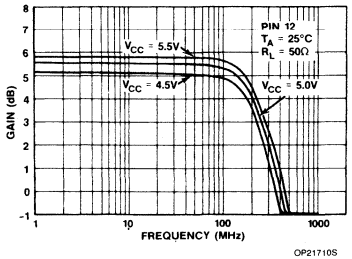


Differential Output Voltage vs Input Current

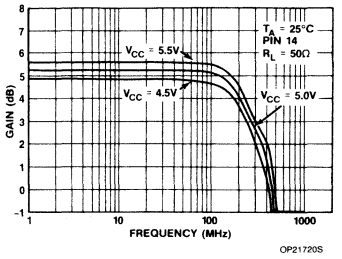


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

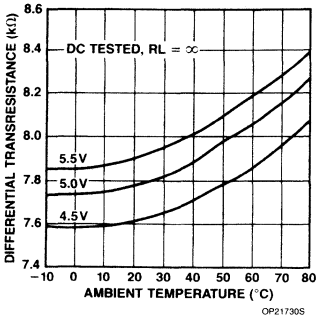
Gain vs Frequency



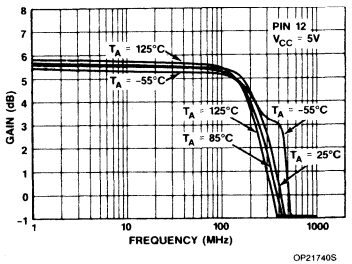
Gain vs Frequency



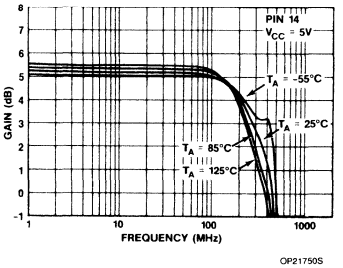
NE5210 Differential Transresistance vs Temperature



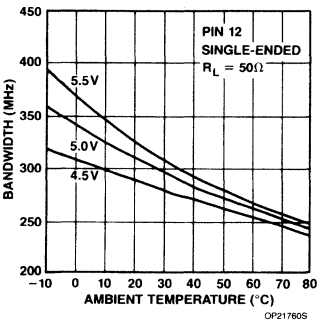
Gain vs Frequency



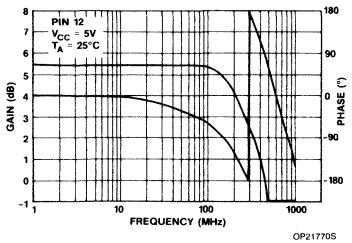
Gain vs Frequency



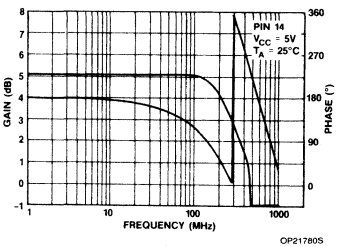
NE5210 Bandwidth vs Temperature



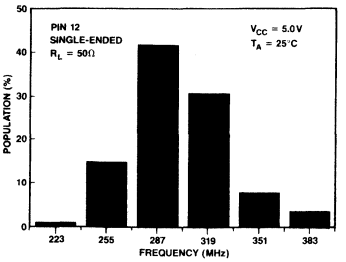
Gain and Phase Shift vs Frequency



Gain and Phase Shift vs Frequency

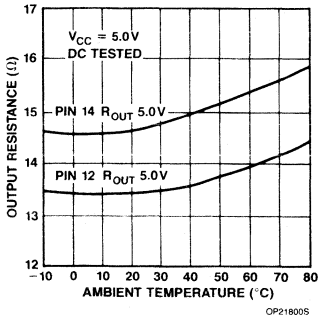


NE5210 Typical Bandwidth Distribution (70 Parts from 4 Wafer Lots)

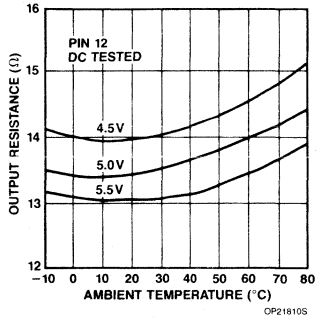


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

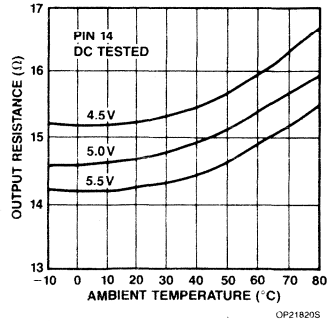
NE5210 Output Resistance vs Temperature



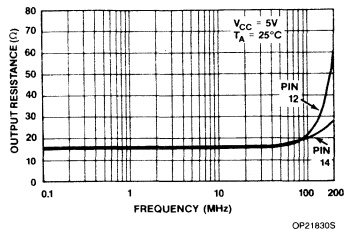
NE5210 Output Resistance vs Temperature



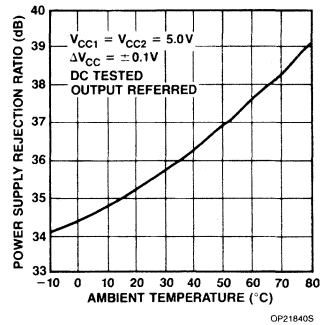
NE5210 Output Resistance vs Temperature



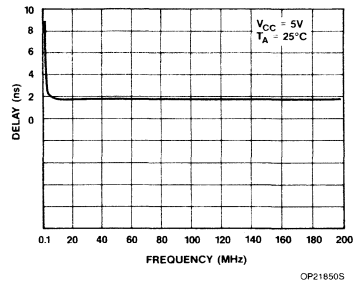
Output Resistance vs Frequency



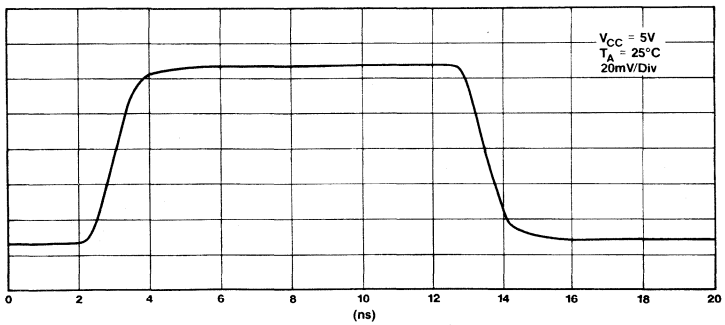
NE5210 Power Supply Rejection Ratio vs Temperature



Group Delay



Output Step Response



Transimpedance Amplifier (280MHz) NE5210

THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5210 is a wide bandwidth (typically 280MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 240μA. The NE5210 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, $R_F = 3.6k\Omega$. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT(diff)}}{I_{IN}} = 2R_F = 2(3.6K) = 7.2k\Omega.$$

The single-ended transresistance of the amplifier is typically 3.6kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, $A_{VOL} \approx 70$. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15}–Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers Q_{11}–Q_{12} which are biased by constant current sources. The collectors of Q_{11}–Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended.

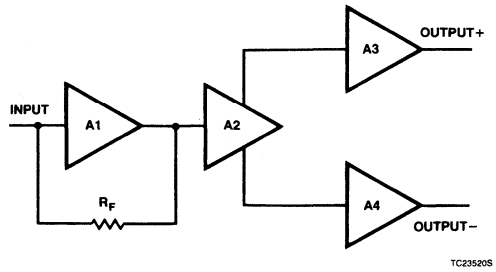


Figure 1. NE5210 – Block Diagram

For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 7.5pF, assuming that $C_S = 0$ where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{3.6k}{71} = 51\Omega.$$

More exact calculations would yield a higher value of 60Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi\ R_{IN}\ C_{IN}}.$$

Assuming typical values for $R_F = 3.6k\Omega$, $R_{IN} = 60\Omega$, $C_{IN} = 7.5pF$

$$f_{-3dB} = \frac{1}{2\pi\ 7.5pF\ 60} = 354MHz.$$

The operating point of Q1, Figure 2, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, $R_{IN} = 60\Omega$ then the total input capacitance, $C_{IN} = (1 + 7.5)$ pF which will lead to only a 12% bandwidth reduction.

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 3.5pA/$\sqrt{Hz}$. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 66nA in a 200MHz bandwidth.

DYNAMIC RANGE CALCULATIONS

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming $I_{INMAX} = 240\mu A$ and a wideband noise of $I_{EQ} = 66nA_{RMS}$ for an external source capacitance of $C_S = 1pF$.

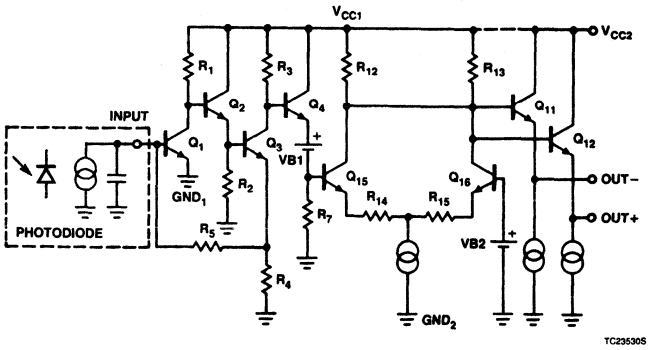


Figure 2. Trans-Impedance Amplifier

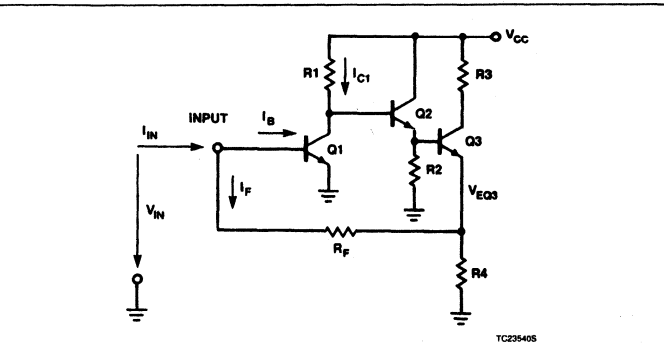


Figure 3. Shunt-Series Input Stage

$$D_E = \frac{\text{(Max. input current)}}{\text{(Peak noise current)}}$$

$$= 20 \log \frac{(240 \times 10^{-6})}{(\sqrt{2}\ 66 \times 10^{-9})}$$

$$= 20 \log \frac{(240\mu A)}{(93nA)} = 68dB.$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

$$\text{Energy of one Photon} = \frac{hc}{\lambda} \text{ watt sec (Joule)}$$

Where h = Planck's Constant = 6.6×10^{-34} Joule sec.
c = speed of light = 3×10^8 mt/sec
c/λ = optical frequency

$$\text{No. of incident photons/sec} = \frac{\frac{P}{hc}}{\lambda} \text{ where P = optical incident power}$$

$$\text{No. of generated electrons/sec} = \eta \cdot \frac{\frac{P}{hc}}{\lambda}$$

where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole pairs}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \cdot \frac{\frac{P}{hc}}{\lambda} \cdot e \text{ Amps (Coulombs/sec.)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

$$\text{Responsivity } R = \frac{\frac{\eta \cdot e}{hc}}{\lambda} \text{ Amp/watt}$$

I = P·R

Assuming a data rate of 400 Mbaud (Bandwidth, B = 200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{66 \times 10^{-9}}{(1.6 \times 10^{-19})(200 \times 10^6)} = 2063$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12 \frac{hc}{\lambda} B\ Z = 12\ 2.3 \times 10^{-19}$$

$$200 \times 10^6\ 2063$$
$$= 1139nW = -29.4dBm,$$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the NE5210, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}$$

$$= \frac{1139 \times 10^{-9} \times 1.6 \times 10^{-19}}{2.3 \times 10^{-19}}$$

$$= 792nA.$$

Choosing the maximum peak overload current of $I_{avMAX} = 240\mu A$, the maximum mean optical power is:

$$P_{avMAX} = \frac{hc\ I_{avMAX}}{\lambda\ q} = \frac{2.3 \times 10^{-19}}{1.6 \times 10^{-19}} 240 \times 10^{-6}$$

$$= 345mW \text{ or } -4.6dBm.$$

Thus the optical dynamic range, D_o is:

$D_o = P_{avMAX} - P_{avMIN} = -4.6 - (-29.4) = 24.8dB.$

This represents the maximum limit attainable with the NE5210 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 850nm wavelength.

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5210 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near

800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1μF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1μF capacitors with 10μF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 4 depicts a 50Mb/s TTL fiber-optic receiver using the BPF31, 850nm LED, the NE5210 and the NE5214 post amplifier.

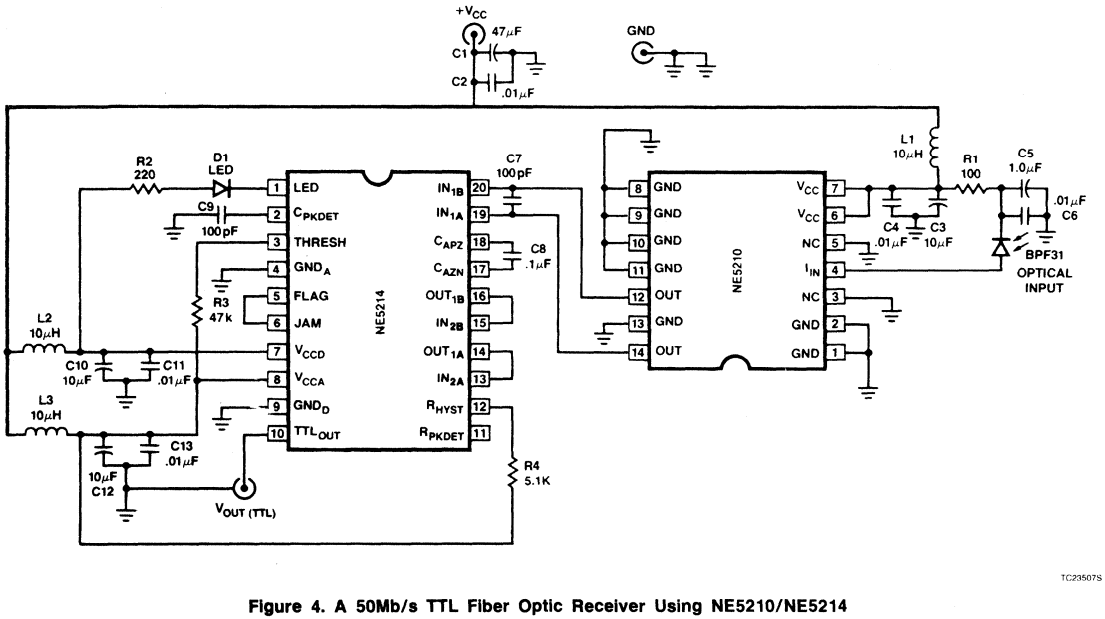


Figure 4. A 50Mb/s TTL Fiber Optic Receiver Using NE5210/NE5214

NE/SA5211
Transimpedance Amplifier (180MHz)

Preliminary Specification

DESCRIPTION

The NE/SA5211 is a 28kΩ transimpedance, wide-band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

FEATURES

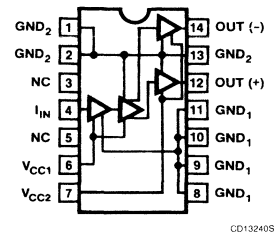
- **Extremely low noise: 1.8pA/$\sqrt{Hz}$**
- **Single 5V supply**
- **Large bandwidth: 180MHz**
- **Differential outputs**
- **Low input/output impedances**
- **High power supply rejection ratio**
- **28kΩ differential transresistance**

APPLICATIONS

- **Fiber optic receivers, analog and digital**
- **Current-to-voltage converters**
- **Wide-band gain block**
- **Medical and scientific Instrumentation**
- **Sensor preamplifiers**
- **Single-ended to differential conversion**
- **Low noise RF amplifiers**
- **RF signal processing**

PIN CONFIGURATION

D Package



TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE5211D
14-Pin Plastic SO	−40 to +85°C	SA5211D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5211	SA5211	
V_{CC}	Power supply	6	6	V
T_A	Operating ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	−55 to +150	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	−65 to +150	°C
$P_{D\ MAX}$	Power dissipation, T_A = 25°C (still-air)[1]	1.0	1.0	W
$I_{IN\ MAX}$	Maximum input current[2]	5	5	mA

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance: θ_{JA} = 125°C/W
2. The use of a pull-up resistor to V_{CC}, for the PIN diode, is recommended.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range		
	NE Grade	0 to +70	°C
	SA Grade	−40 to +85	°C
T_J	Junction temperature range		
	NE Grade	0 to +90	°C
	SA Grade	−40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature at V_{CC} = 5V, unless otherwise specified. Typical data apply at V_{CC} = 5V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5211			SA5211			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	0.55	0.8	1.00	V
$V_{O\pm}$	Output bias voltage		2.8	3.4	3.7	2.7	3.4	3.7	V
V_{OS}	Output offset voltage			0	120		0	130	mV
I_{CC}	Supply current		21	24	30	20	26	31	mA
I_{OMAX}	Output sink/source current[1]		3	4		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 8, Procedure 2	±30	±40		±20	±40		μA
$I_{IN\ MAX}$	Maximum input current overload threshold	Test Circuit 8, Procedure 4	±40	±60		±30	±60		μA

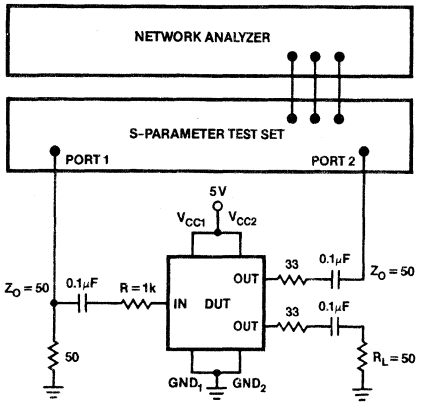
NOTE:
1. Test condition: output quiescent voltage variation is less than 100mV for 3mA load current.

AC ELECTRICAL CHARACTERISTICS Typical data and Min and Max limits apply at V_{CC} = 5V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5211			SA5211			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested $R_L = \infty$ Test Circuit 8, Procedure 1	22	28	35	21	28	36	kΩ
R_O	Output resistance (differentialoutput)	DC tested		30			30		Ω
R_T	Transresistance (single-ended output)	DC tested $R_L = \infty$	11	14	17.5	10.5	14	18.0	kΩ
R_O	Output resistance (single-ended output)	DC tested		15			15		Ω
f_{3dB}	Bandwidth (–3dB)	T_A = 25°C Test circuit 1		180			180		MHz
R_{IN}	Input resistance			200			200		Ω
C_{IN}	Input capacitance			4			4		pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	V_{CC} = 5± 0.5V		3.7			3.7		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\ MAX} - T_{A\ MIN}$		0.025			0.025		%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 f = 10MHz T_A = 25°C		1.8			1.8		pA/$\sqrt{Hz}$
I_T	Integrated RMS noise current over the bandwidth (referred to input)	T_A = 25°C Test Circuit 2							
	$C_S = 0$[1]	Δf = 50MHz Δf = 100MHz Δf = 200MHz		13 20 35			13 20 35		nA nA nA
PSRR	C_S = 1pF Power supply rejection ratio[2] ($V_{CC1} = V_{CC2}$)	Δf = 50MHz Δf = 100MHz Δf = 200MHz DC tested, ΔV_{CC} = .01V Equivalent AC Test Circuit 3	26	13 21 41 32		23	13 21 41 32		nA nA nA dB
PSRR	Power supply rejection ratio[2] (V_{CC1})	DC tested, ΔV_{CC} = .01V Equivalent AC Test Circuit 4	26	32		23	32		dB
PSRR	Power supply rejection ratio[2] (V_{CC2})	DC tested, ΔV_{CC} = .01V Equivalent AC Test Circuit 5	45	65		45	65		dB
PSRR	Power supply rejection ratio (ECL configuration)[2]	f = 0.1MHz Test Circuit 6		23			23		dB
V_{OMAX}	Maximum differential output voltage swing	$R_L = \infty$ Test Circuit 8, Procedure 3	2.4	3.2		1.7	3.2		V_{P-P}
$V_{IN\ MAX}$	Maximum input amplitude for output duty cycle of 50± 5%[3]	Test Circuit 7	160			160			mV_{P-P}
t_R	Rise time for 50mV output signal[4]	Test Circuit 7		0.8	1.2		0.8	1.8	ns

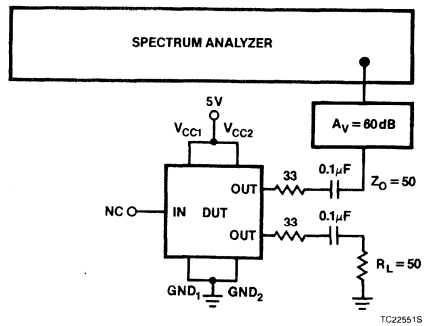
NOTES:
1. Package parasitic capacitance amounts to about 0.2pF.
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} lines.
3. Guaranteed by linearity and overload tests.
4. t_R defined as 20 – 80% rise time. It is guaranteed by – 3dB bandwidth test.

TEST CIRCUITS



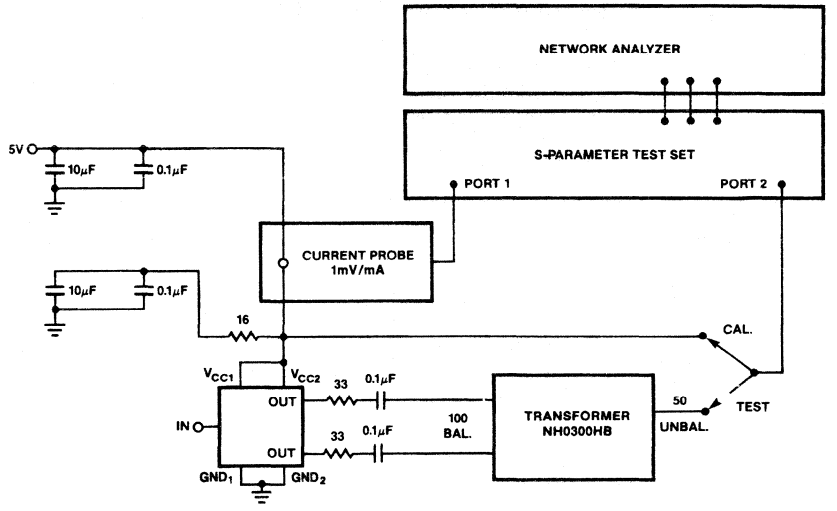
SINGLE-ENDED	DIFFERENTIAL
$R_T \cong \frac{V_{OUT}}{V_{IN}} R = 2 \times S21 \times R$	$R_T = \frac{V_{OUT}}{V_{IN}} R = 4 \times S21 \times R$
$R_O \cong Z_O \left\lvert \frac{1+S22}{1-S22} \right\rvert - 33$	$R_O = 2Z_O \left\lvert \frac{1+S22}{1-S22} \right\rvert - 66$

Test Circuit 1

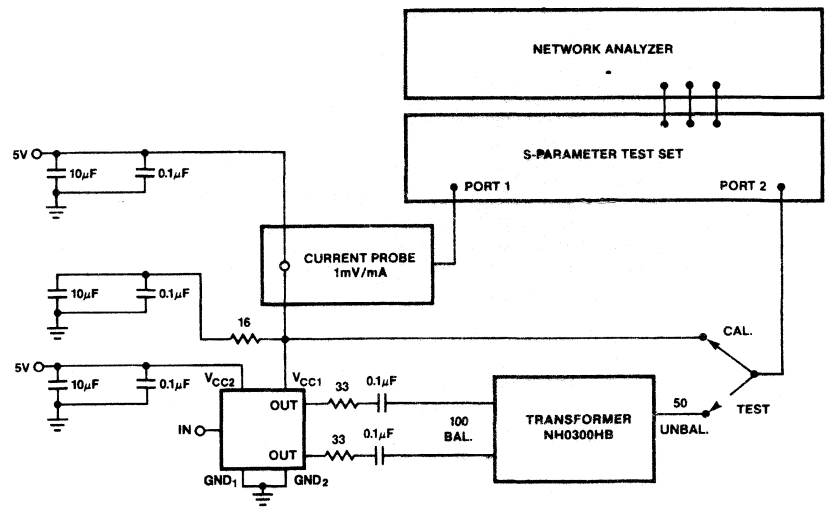


Test Circuit 2

TEST CIRCUITS (Continued)

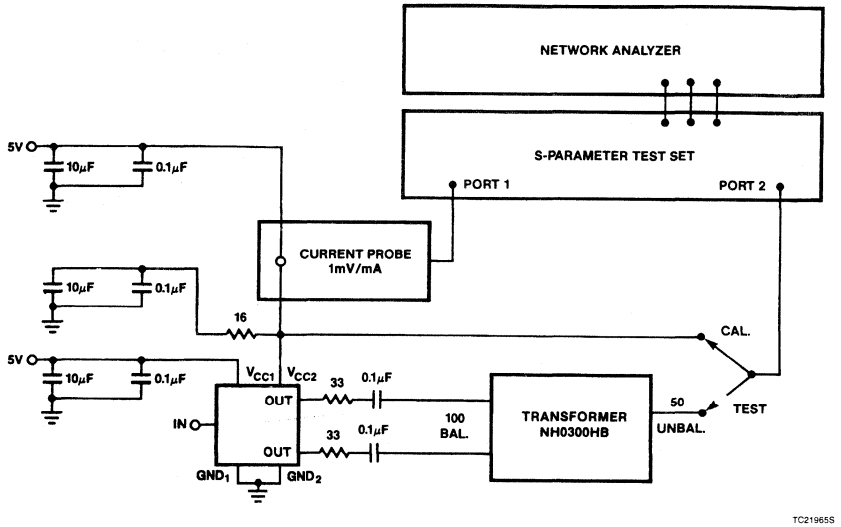


Test Circuit 3

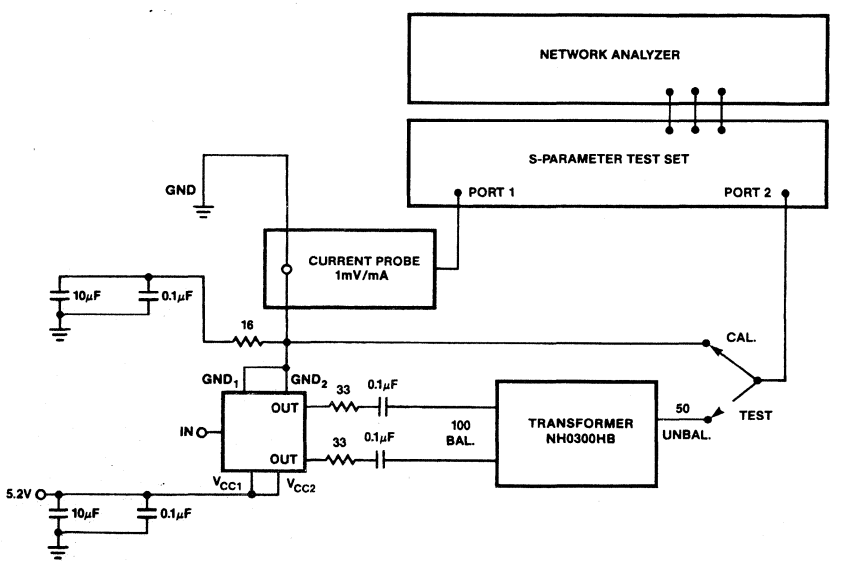


Test Circuit 4

TEST CIRCUITS (Continued)

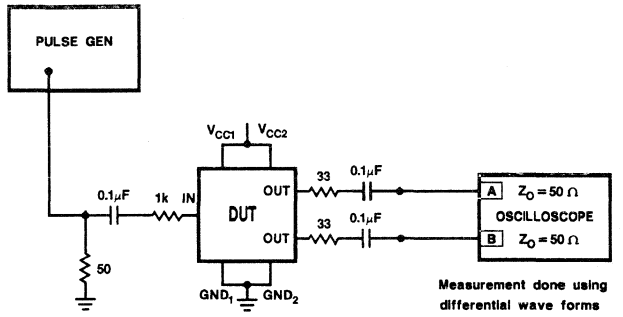


Test Circuit 5



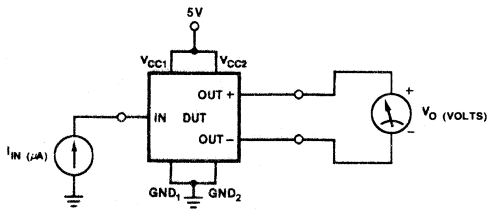
Test Circuit 6

TEST CIRCUITS (Continued)



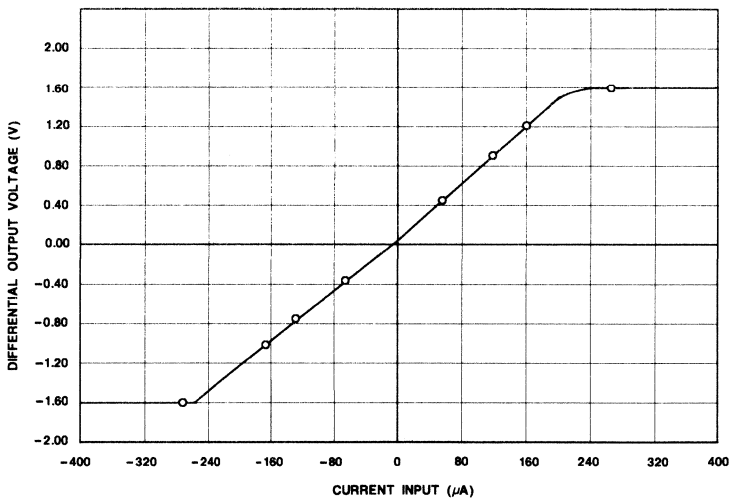
Test Circuit 7

TEST CIRCUITS (Continued)



TC23461S

Typical V_O (Differential) vs I_{IN}



OP20990S

NE5211 TEST CONDITIONS

Procedure 1

R_T measured at 15μA
$R_T = (V_{O1} - V_{O2})/(+15\mu A - (-15\mu A))$
Where: V_{O1} Measured at $I_{IN} = +15\mu A$
V_{O2} Measured at $I_{IN} = -15\mu A$

Procedure 2

Linearity = $1 - ABS((V_{OA} - V_{OB})/(V_{O3} - V_{O4}))$
Where: V_{O3} Measured at $I_{IN} = +30\mu A$
V_{O4} Measured at $I_{IN} = -30\mu A$
$V_{OA} = R_T * (+30\mu A) + V_{O8}$
$V_{OB} = R_T * (-30\mu A) + V_{O8}$

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$
Where: V_{O7} Measured at $I_{IN} = +65\mu A$
V_{O8} Measured at $I_{IN} = -65\mu A$

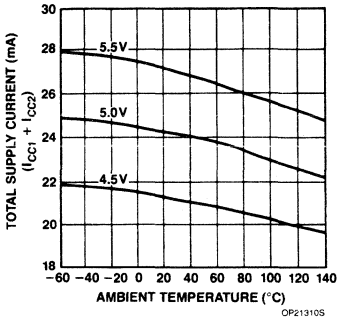
Procedure 4

$I_{IN\ MAX}$ Test Pass Conditions:
$V_{O7} - V_{O5} > 50mV$ and $V_{O6} - V_{O5} > 50mV$
Where: V_{O5} Measured at $I_{IN} = +40\mu A$
V_{O6} Measured at $I_{IN} = -40\mu A$
V_{O7} Measured at $I_{IN} = +65\mu A$
V_{O8} Measured at $I_{IN} = -65\mu A$

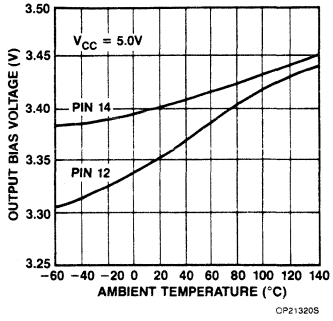
Test Circuit 8

TYPICAL PERFORMANCE CHARACTERISTICS

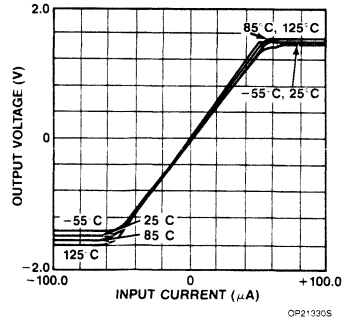
NE5211 Supply Current vs Temperature



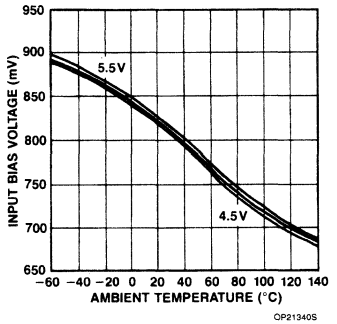
NE5211 Output Bias Voltage vs Temperature



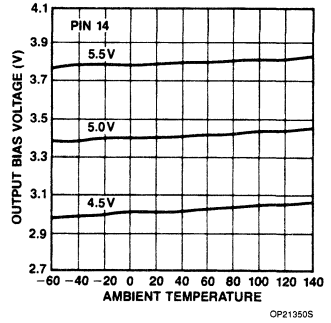
Output Voltage vs Input Current



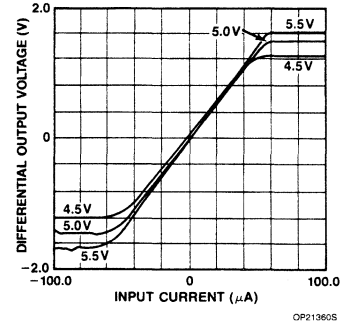
NE5211 Input Bias Voltage vs Temperature



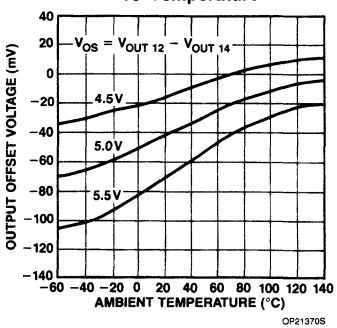
NE5211 Output Bias Voltage vs Temperature



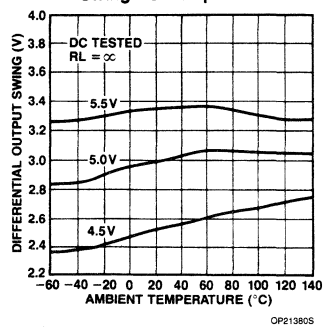
Differential Output Voltage vs Input Current



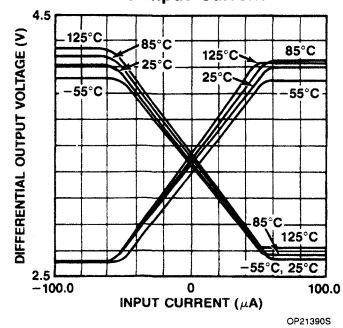
NE5211 Output Offset Voltage vs Temperature



NE5211 Differential Output Swing vs Temperature

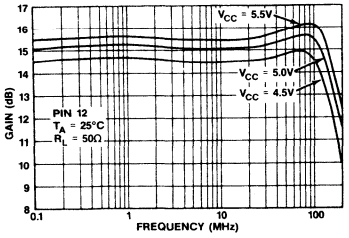


Differential Output Voltage vs Input Current

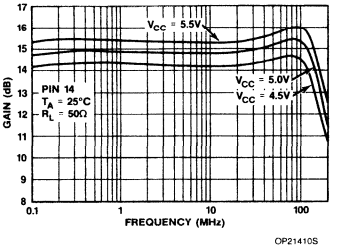


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

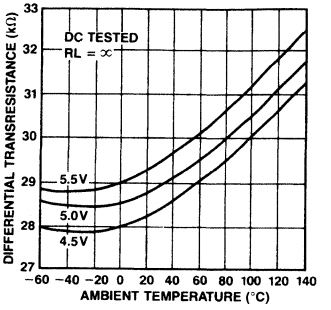
Gain vs Frequency



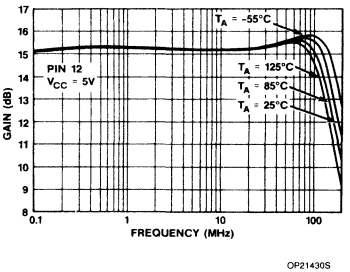
Gain vs Frequency



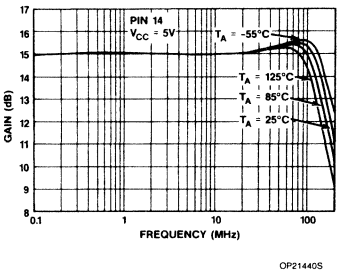
NE5211 Differential Transresistance vs Temperature



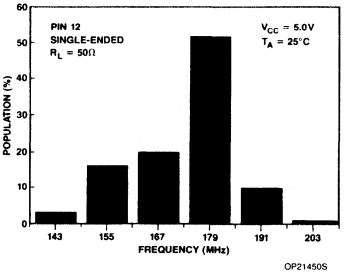
Gain vs Frequency



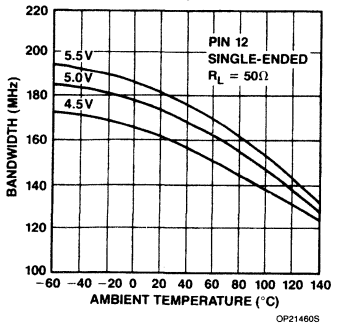
Gain vs Frequency



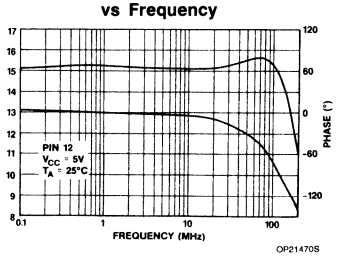
NE5211 Typical Bandwidth Distribution (70 Parts from 3 Wafer Lots)



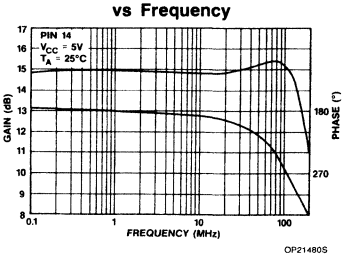
NE5211 Bandwidth vs Temperature



Gain and Phase Shift vs Frequency

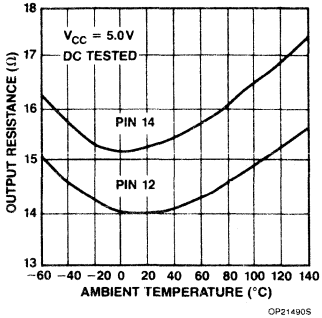


Gain and Phase Shift vs Frequency

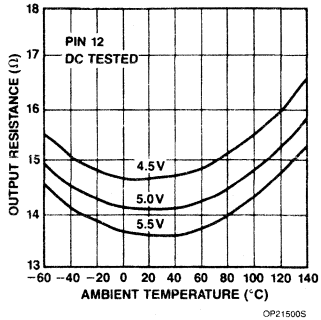


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

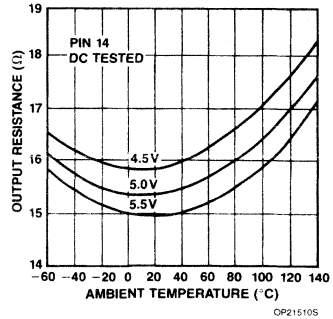
NE5211 Output Resistance vs Temperature



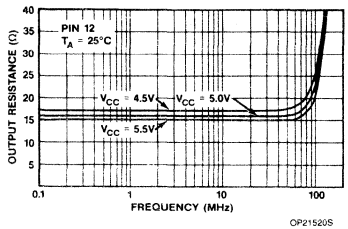
NE5211 Output Resistance vs Temperature



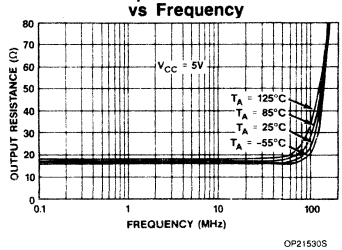
NE5211 Output Resistance vs Temperature



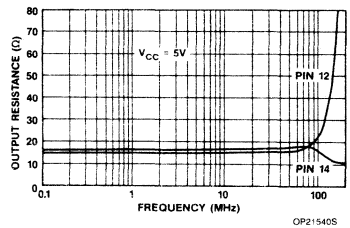
Output Resistance vs Frequency



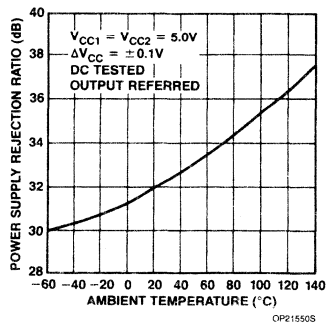
Output Resistance vs Frequency



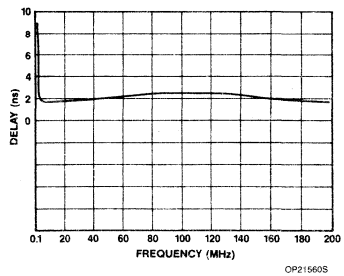
Output Resistance vs Frequency



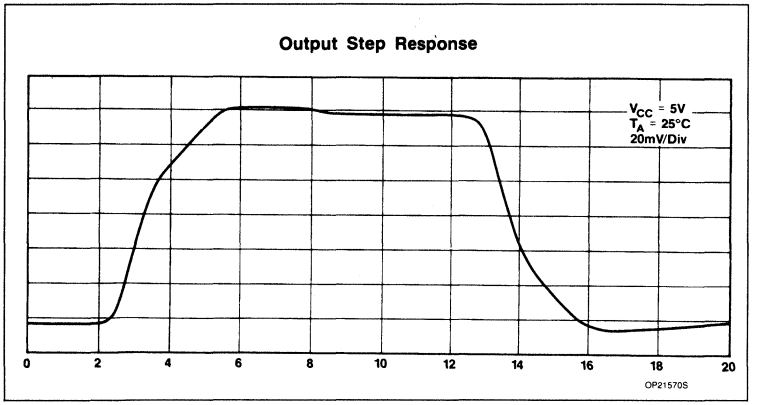
NE5211 Power Supply Rejection Ratio vs Temperature



Group Delay vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5211 is a wide bandwidth (typically 180MHz) transimpedance amplifier designed primarily for high sensitivity. The maximum input current before output stage clipping occurs at typically 50μA. The NE5211 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F = 14.4kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT\ (diff)}}{I_{IN}} = 2R_F = 2(14.4k) = 28.8k\Omega.$$

The single-ended transresistance of the amplifier is typically 14.4kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, $A_{VOL} \approx 70$. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15}–Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers Q_{11}–Q_{12} which are biased by constant current sources. The collectors of Q_{11}–Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 4pF, assuming that $C_S = 0$ where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{14.4k}{71} = 203\Omega.$$

More exact calculations would yield a value of 200Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi\ R_{IN}\ C_{IN}}.$$

Assuming typical values for R_F = 14.4kΩ, R_{IN} = 200Ω, C_{IN} = 4pF:

$$f_{-3dB} = \frac{1}{2\pi\ 4pF\ 200} = 200MHz.$$

The operating point of Q1 has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, R_{IN} = 200Ω then the total input capacitance, C_{IN} = (1 + 4)pF which will lead to only a 20% bandwidth reduction.

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 1.8pA/$\sqrt{Hz}$. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 41nA in a 200MHz bandwidth for C_S = 1pF

DYNAMIC RANGE

The electrical dynamic range can be defined as the radio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 60μA and a wideband noise of I_{EQ} = 41nA_{RMS} for an external source capacitance of C_S = 1pF.

$$D_E = \frac{\text{(Max. input current)}}{\text{(Peak noise current)}}$$

$$= 20 \log \frac{(60 \times 10^{-6})}{(\sqrt{2}\ 41 \times 10^{-9})}$$

$$= 20 \log \frac{(60\mu A)}{(58nA)} = 60dB.$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

$$\text{Energy of one photon} = \frac{hc}{\lambda} \text{ watt sec (Joule)}$$

Where h = Planck's Constant = 6.6×10^{-34} Joule sec.

c = speed of light = 3×10^8 mt/sec

c/λ = optical frequency

$$\text{No. of incident photons/sec} = \frac{P}{\frac{hc}{\lambda}} \text{ where P = optical incident power}$$

$$\text{No. of generated electrons/sec} = \eta \cdot \frac{P}{\frac{hc}{\lambda}}$$

Where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole pairs}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \cdot \frac{P}{\frac{hc}{\lambda}} \cdot e \text{ Amps (Coulombs/sec.)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

$$\text{Responsivity } R = \frac{\eta \cdot e}{\frac{hc}{\lambda}} \text{ Amp/watt}$$

$$I = P \cdot R$$

Assuming a data rate of 400 Mbaud (Bandwidth, B = 200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{i_{eq}}{qB} = \frac{41 \times 10^{-9}}{(1.6 \times 10^{-19})\ (200 \times 10^6)} = 1281$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12 \frac{hc}{\lambda} B\ Z = 12\ 2.3 \times 10^{-19}$$

$200 \times 10^6\ 1281 = 707nW = -31.5dBm,$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the NE5210, at this input power is:

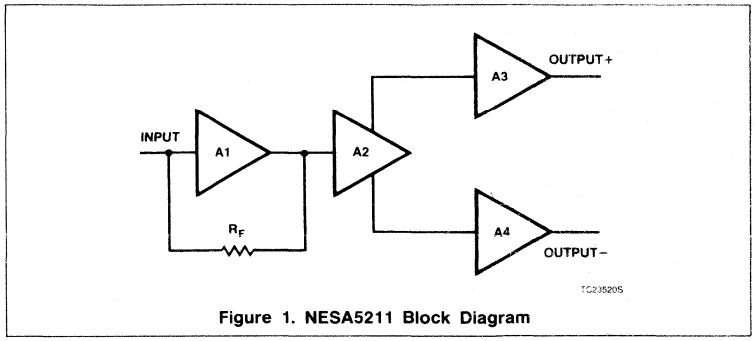


Figure 1. NESA5211 Block Diagram

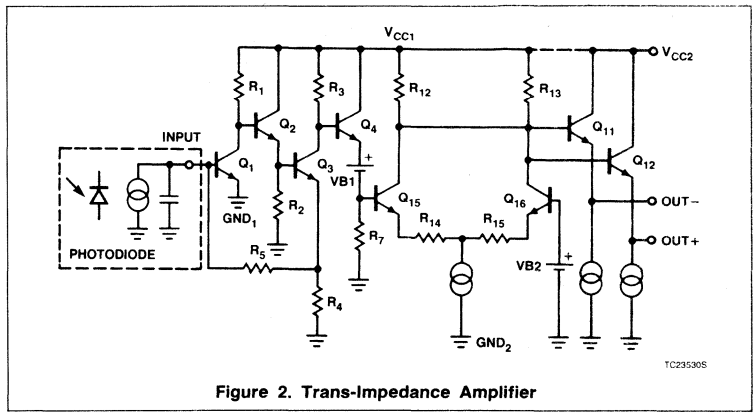


Figure 2. Trans-Impedance Amplifier

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}$$

$$= \frac{707 \times 10^{-9} \times 1.6 \times 10^{-19}}{2.3 \times 10^{-19}}$$

$$= 492nA.$$

Choosing the maximum peak overload current of $I_{avMAX} = 60\mu A$, the maximum mean optical power is:

$$P_{avMAX} = \frac{hc\ I_{avMAX}}{\lambda\ q} = \frac{2.3 \times 10^{-19}}{1.6 \times 10^{-19}} 60 \times 10^{-6}$$

$$= 86mW \text{ or } -10.6dBm.$$

Thus the optical dynamic range, D_o is:

$$D_o = P_{avMAX} - P_{avMIN} = -31.5 - (-10.6)$$
$$= 20.8dB.$$

This represents the maximum limit attainable with the NE5211 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 820nm wavelength.

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5211 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout such that Ground 1 and Ground 2 have very low impedance paths have produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure

1. S. D. Personick, *Optical Fiber Transmission Systems*, Plenum Press, NY, 1981, Chapter 3.

the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1μF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1μF capacitors with 10μF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 4 depicts a 50Mb/s TTL fiber-optic receiver using the BPF31, 850nm LED, the NE5211 and the NE5214 post amplifier. For more information on this circuit, please refer to Application Brief AB1432.

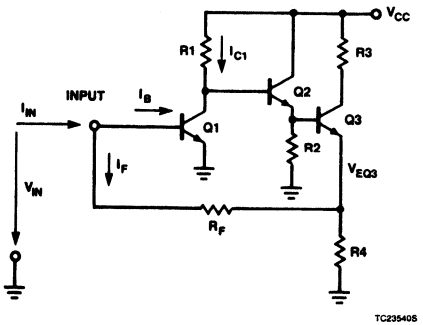


Figure 3. Shunt-Series Input Stage

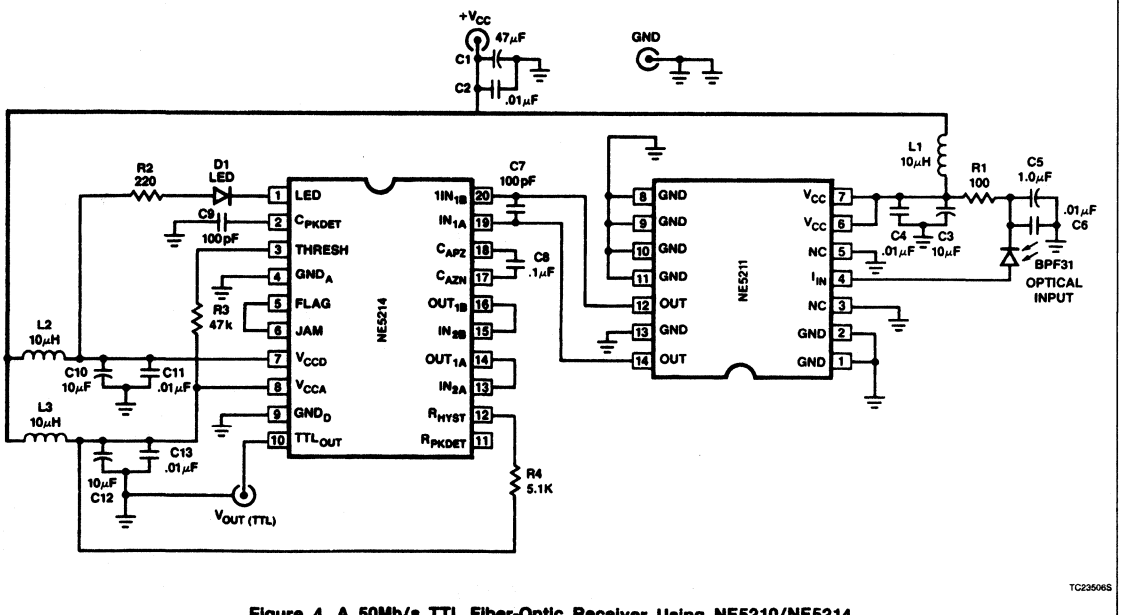


Figure 4. A 50Mb/s TTL Fiber-Optic Receiver Using NE5210/NE5214

NE/SA/SE5212
Transimpedance Amplifier (140MHz)

Product Specification

DESCRIPTION

The NE/SA/SE5212 is a 14kΩ transimpedance, wideband, low noise differential output amplifier, particularly suitable for signal recovery in fiber optic receivers and in any other applications where very low signal levels obtained from high-impedance sources need to be amplified.

FEATURES

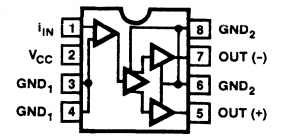
- **Extremely low noise: 2.5pA/$\sqrt{Hz}$**
- **Single 5V supply**
- **Large bandwidth: 140MHz**
- **Differential outputs**
- **Low input/output impedances**
- **High-power supply rejection ratio**
- **14kΩ differential transresistance**

APPLICATIONS

- **Fiber-optic receivers, analog and digital**
- **Current-to-voltage converters**
- **Wideband gain block**
- **Medical and scientific instrumentation**
- **Sensor preamplifiers**
- **Single-ended to differential conversion**
- **Low noise RF amplifiers**
- **RF signal processing**

PIN CONFIGURATION

N, FE, D Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5212N
8-Pin Plastic SO	0 to +70°C	NE5212D
8-Pin Ceramic DIP	0 to +70°C	NE5212FE
8-Pin Plastic SO	−40°C to +85°C	SA5212D
8-Pin Plastic DIP	−40°C to +85°C	SA5212N
8-Pin Ceramic DIP	−40°C to +85°C	SA5212FE
8-Pin Plastic DIP	−55°C to +125°C	SE5212N
8-Pin Ceramic DIP	−55°C to +125°C	SE5212FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING			UNIT
		NE5212	SA5212	SE5212	
V_{CC}	Power Supply	6	6	6	V
$P_{D\ MAX}$	Power dissipation, $T_A = 25°C$ (still air)[1]				
	8-Pin Plastic DIP	1100	1100	1100	mW
	8-Pin Plastic SO	750	750	750	mW
	8-Pin Cerdip	750	750	750	mw
$I_{IN\ MAX}$	Maximum input current[2]	5	5	5	mA
T_A	Operating ambient temperature range	0 to 70	−40 to 85	−55 to 125	°C
T_J	Operating junction	−55 to 150	−55 to 150	−55 to 150	°C
T_{STG}	Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance:
   8-Pin Plastic DIP: 110°C/W
   8-Pin Plastic SO: 160°C/W
   8-Pin Cerdip: 165°C/W
2. The use of a pull-up resistor to V_{CC}, for the PIN diode, is recommended

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	4.5 to 5.5	V
T_A	Ambient temperature ranges		
	NE Grade	0 to +70	°C
	SA Grade	−40 to +85	°C
	SE Grade	−55 to +125	°C
T_J	Junction temperature ranges		
	NE Grade	0 to +90	°C
	SA Grade	−40 to +105	°C
	SE Grade	−55 to +145	°C

DC ELECTRICAL CHARACTERISTICS

Minimum and Maximum limits apply over operating temperature range at $V_{CC} = 5V$, unless otherwise specified. Typical data applies at $V_{CC} = 5V$ and $T_A = 25°C$.

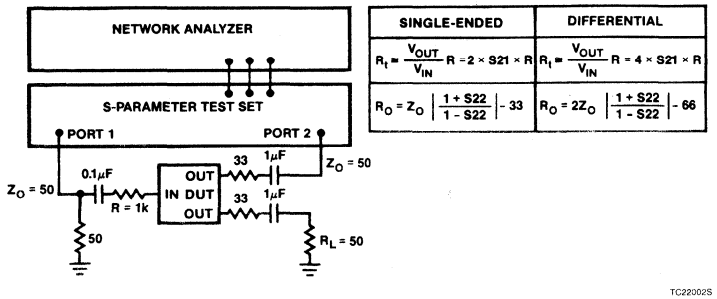
SYMBOL	PARAMETER	TEST CONDITIONS	NE5212			SA/SE5212			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	0.55	0.8	1.05	V
$V_{O\pm}$	Output bias voltage		2.8	3.3	3.7	2.5	3.3	3.8	V
V_{OS}	Output offset voltage				80			120	mV
I_{CC}	Supply current		21	26	32	20	26	33	mA
I_{OMAX}	Output sink/source current		3	4		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 6, Procedure 2	±60	±80		±40	±80		μA
$I_{N\ MAX}$	Maximum input current overload threshold	Test Circuit 6, Procedure 4	±80	±120		±60	±120		μA

AC ELECTRICAL CHARACTERISTICS Minimum and Maximum limits apply over operating temperature range at V_{CC} = 5V, unless otherwise specified. Typical data applies at V_{CC} = 5V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5212			SA/SE5212			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$ Test Circuit 6, Procedure 1	9.8	14	18.2	9.0	14	19	kΩ
R_O	Output resistance (differential output)	DC tested	14	30	42	14	30	46	Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$	4.9	7	9.1	4.5	7	9.5	kΩ
R_O	Output resistance (single-ended output)	DC tested	7	15	21	7	15	23	Ω
f_{3dB}	Bandwidth (-3dB)	Test Circuit 1 D package, T_A = 25°C N, FE packages, T_A = 25°C	100 100	140 120		100 100	140 120		MHz MHz
R_{IN}	Input resistance		75	110	143	70	110	150	Ω
C_{IN}	Input capacitance			10	15		10	18	pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	V_{CC} = 5 ±0.5V		9.6			9.6		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	D package $\Delta T_A = T_{A\ MAX} - T_{A\ MIN}$		0.05			0.05		%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 f = 10MHz T_A = 25°C		2.5			2.5		pA/√Hz
I_T	Integrated RMS noise current over the bandwidth (referred to input) C_S = 0[1]	T_A = 25°C Test Circuit 2 Δf = 50MHz Δf = 100MHz Δf = 200MHz		20 27 40			20 27 40		nA nA nA
	C_S = 1pF	Δf = 50MHz Δf = 100MHz Δf = 200MHz		22 32 52			22 32 52		nA nA nA
PSRR	Power supply rejection ratio[2]	Any package DC tested ΔV_{CC} = 0.1V Equivalent AC Test Circuit 3	26	33		20	33		dB
PSRR	Power supply rejection ratio[2] (ECL configuration)	Any package f = 0.1MHz[1] Test Circuit 4		23			23		dB
$V_{O\ MAX}$	Maximum differential output voltage swing	$R_L = \infty$ Test Circuit 6, Procedure 3	2.4	3.2		1.7	3.2		V_{P-P}
$V_{IN\ MAX}$	Maximum input amplitude for output duty cycle of 50 ±5%[3]	Test Circuit 5		325			325		mV_{P-P}
t_R	Rise time for 50mV output signal[4]	Test Circuit 5		2.0			2.0		ns

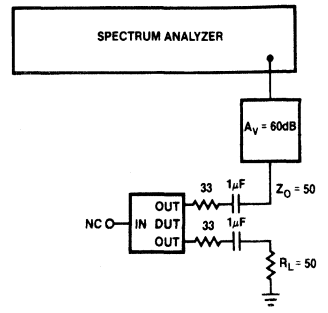
NOTES:
1. Package parasitic capacitance amounts to about 0.2pF.
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} line.
3. Guaranteed by linearity and over load tests.
4. t_R defined as 20 - 80% rise time. It is guaranteed by -3dB bandwidth test.

TEST CIRCUITS

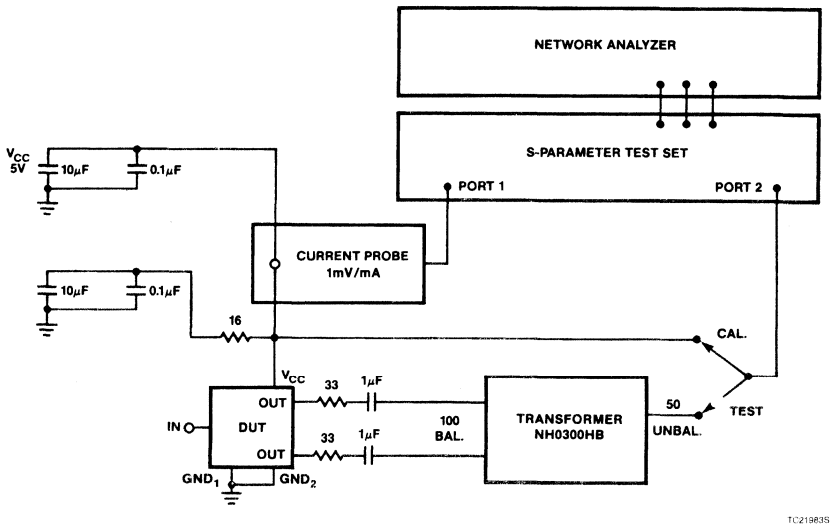


SINGLE-ENDED	DIFFERENTIAL
$R_t = \frac{V_{OUT}}{V_{IN}} R = 2 \times S21 \times R$	$R_t = \frac{V_{OUT}}{V_{IN}} R = 4 \times S21 \times R$
$R_O = Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 33$	$R_O = 2Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 66$

Test Circuit 1

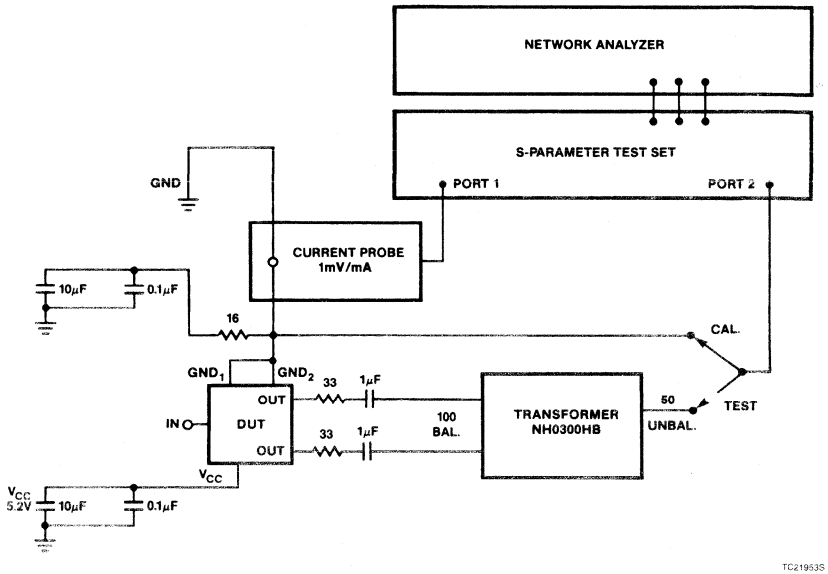


Test Circuit 2

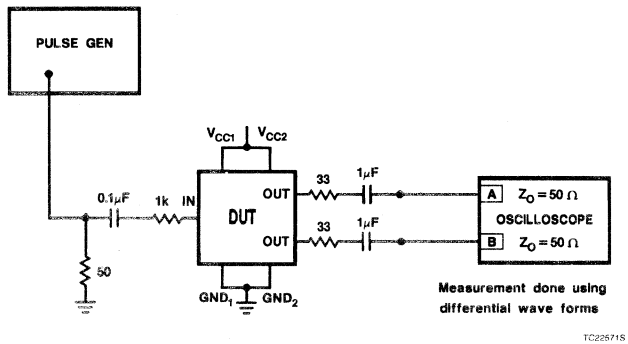


Test Circuit 3

TEST CIRCUITS (Continued)

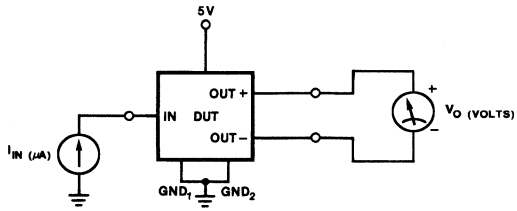


Test Circuit 4



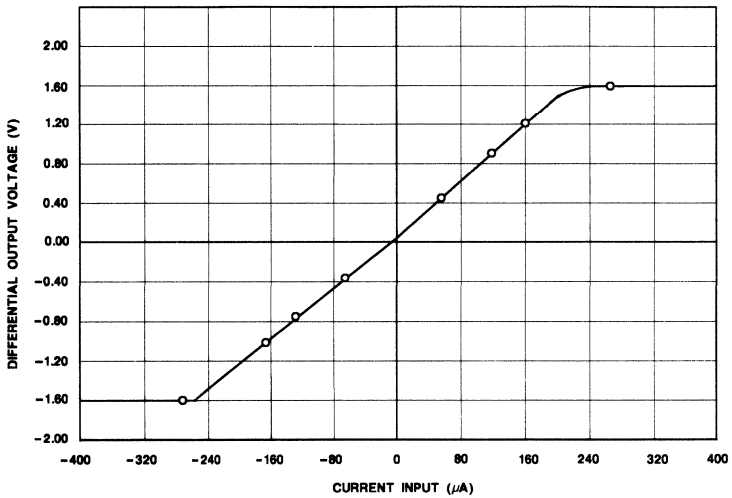
Test Circuit 5

TEST CIRCUITS (Continued)



TC23462S

Typical V_O (Differential) vs I_{IN}



OP20990S

NE5212 TEST CONDITIONS

Procedure 1

R_T measured at 30μA
$R_T = (V_{O1} - V_{O2})/(+30\mu A - (-30\mu A))$
Where: V_{O1} Measured at $I_{IN} = +30\mu A$
V_{O2} Measured at $I_{IN} = -30\mu A$

Procedure 2

Linearity = $1 - ABS((V_{OA} - V_{OB}/(V_{O3} - V_{O4}))$
Where: V_{O3} Measured at $I_{IN} = +60\mu A$
V_{O4} Measured at $I_{IN} = -60\mu A$
$V_{OA} = R_T * (+60\mu A) + V_{O8}$
$V_{OB} = R_T * (-60\mu A) + V_{O8}$

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$
Where: V_{O7} Measured at $I_{IN} = +130\mu A$
V_{O8} Measured at $I_{IN} = -130\mu A$

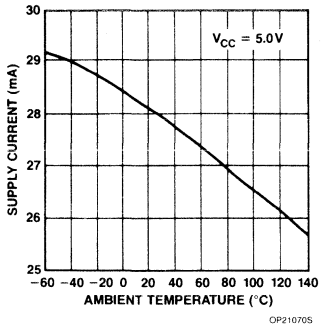
Procedure 4

$I_{IN\ MAX}$ Test Pass Conditions:
$V_{O7} - V_{O5} > 50mV$ and $V_{O6} - V_{O5} > 50mV$
Where: V_{O5} Measured at $I_{IN} = +80\mu A$
V_{O6} Measured at $I_{IN} = -80\mu A$
V_{O7} Measured at $I_{IN} = +130\mu A$
V_{O8} Measured at $I_{IN} = -130\mu A$

Test Circuit 6

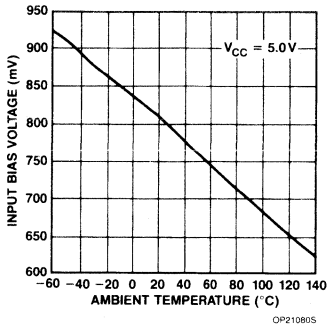
TYPICAL PERFORMANCE CHARACTERISTICS

NE5212 Supply Current vs Temperature



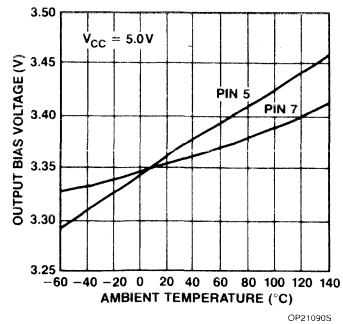
OP21070S

NE5212 Output Bias Voltage vs Temperature



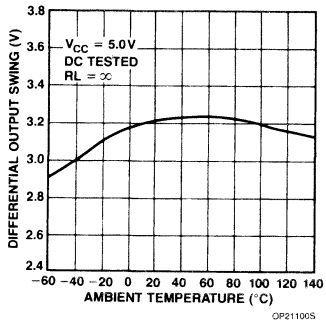
OP21080S

NE5212 Output Bias Voltage vs Temperature



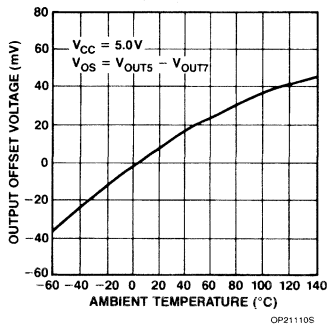
OP21090S

NE5212 Differential Output Swing vs Temperature



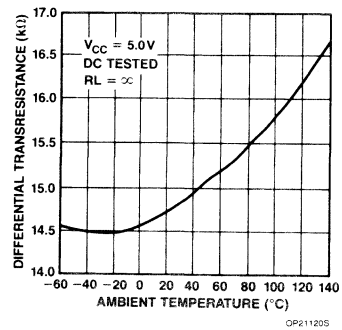
OP21100S

NE5212 Output Offset Voltage vs Temperature



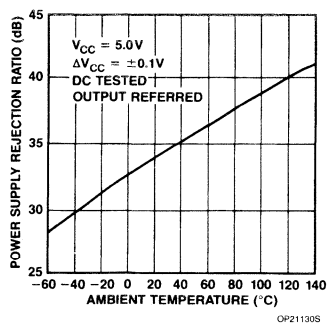
OP21110S

NE5212 Differential Transresistance vs Temperature



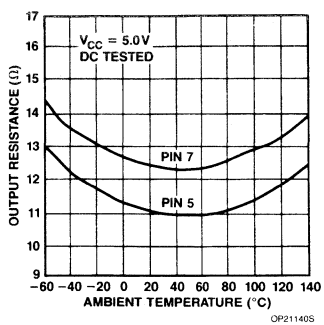
OP21120S

NE5212 Power Supply Rejection Ratio vs Temperature



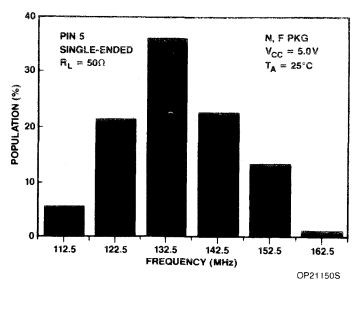
OP21130S

NE5212 Output Resistance vs Temperature



OP21140S

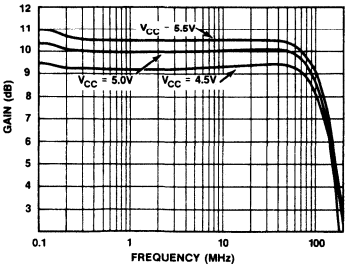
NE5212 Typical Bandwidth Distribution (75 Parts from 3 Wafer Lots)



OP21150S

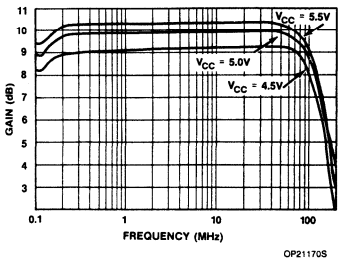
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency



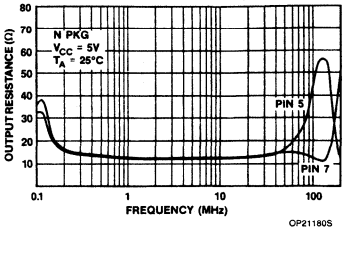
OP21160S

Gain vs Frequency



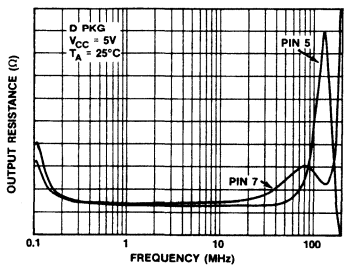
OP21170S

Output Resistance vs Frequency



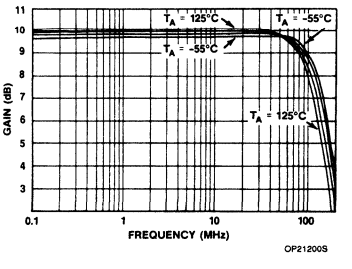
OP21180S

Output Resistance vs Frequency



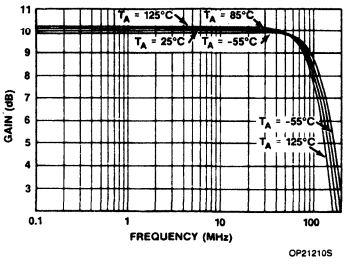
OP21190S

Gain vs Frequency OP21230S



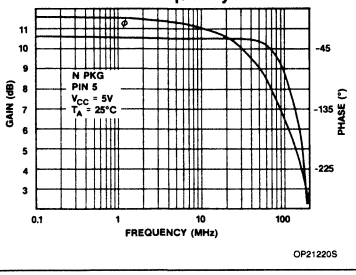
OP21200S

Gain vs Frequency OP21240S



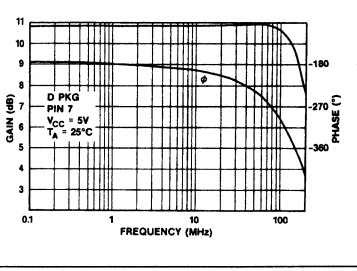
OP21210S

Gain and Phase Shift vs Frequency

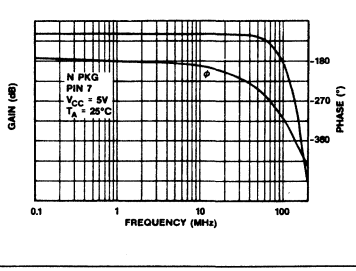


OP21220S

Gain and Phase Shift vs Frequency

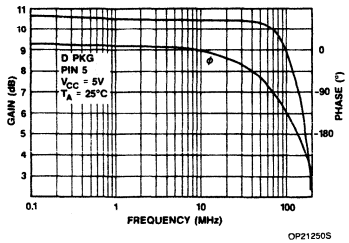


Gain and Phase Shift vs Frequency

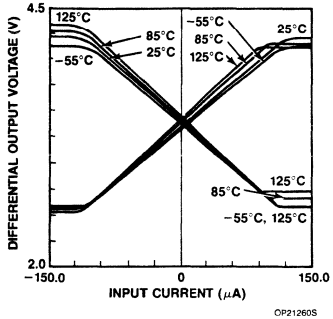


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

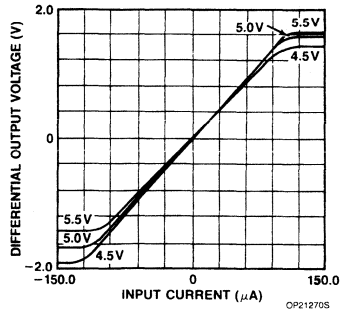
Gain and Phase Shift vs Frequency



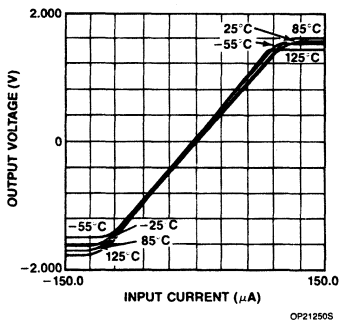
Differential Output Voltage vs Input Current



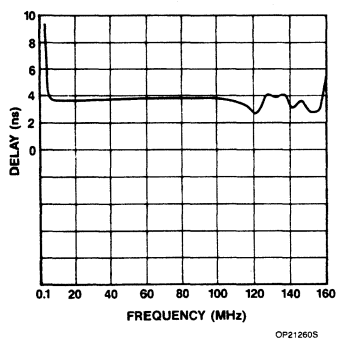
Differential Output Voltage vs Input Current



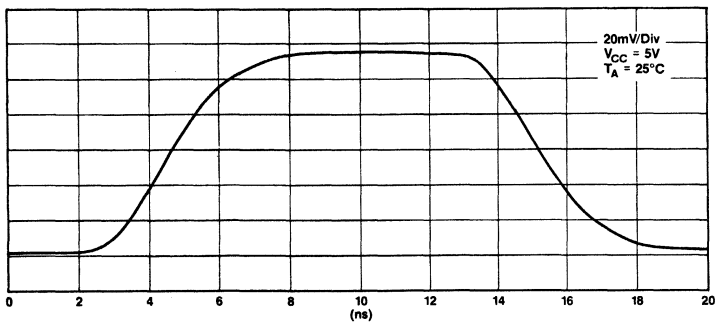
Output Voltage vs Input Current



Group Delay vs Frequency



Output Step Response



THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber optic receivers. The NE5212 is a wide bandwidth (typically 130MHz) transimpedance amplifier designed primarily for high sensitivity. The maximum input current before output stage clipping occurs at typically 120μA. The NE5212 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, $R_F = 7.2k\Omega$. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT(diff)}}{I_{IN}} = 2R_F = 2(7.2k) = 14.4k\Omega.$$

The single-ended transresistance of the amplifier is typically 7.2kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, $A_{VOL} \approx 70$. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15}–Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers Q_{11}–Q_{12} which are biased by constant current sources. The collectors of Q_{11}–Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

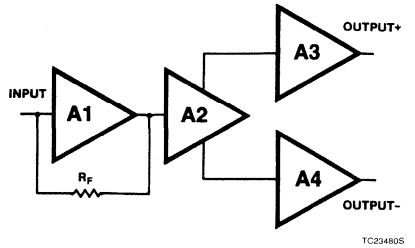


Figure 1. NE5212 – Block Diagram

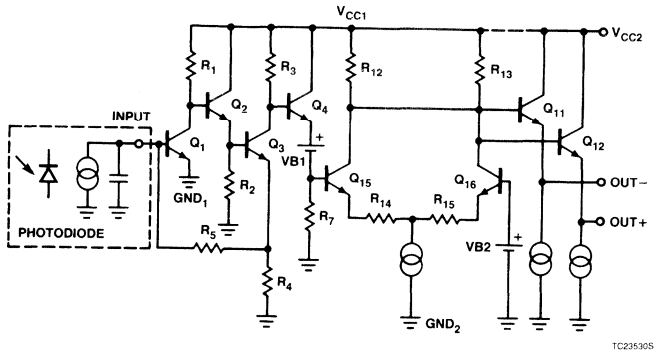


Figure 2. Trans-Impedance Amplifier

BANDWIDTH CALCULATIONS:

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 10pF, assuming that $C_S = 0$ where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{7.2k}{70} = 103\Omega.$$

More exact calculations would yield a value of 110Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi\ R_{IN}\ C_{IN}}.$$

Assuming typical values for $R_F = 7.2k\Omega$, $R_{IN} = 110\Omega$, $C_{IN} = 10pF$:

$$f_{-3dB} = \frac{1}{2\pi\ 110\ 10 \times 10^{-12}} = 145MHz.$$

The operating point of Q1 has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, $R_{IN} = 110\Omega$ then the total input capacitance, $C_{IN} = (1 + 10)$ pF which will lead to only a 9% bandwidth reduction.

NOISE

Most of the currently installed fiber optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very im-

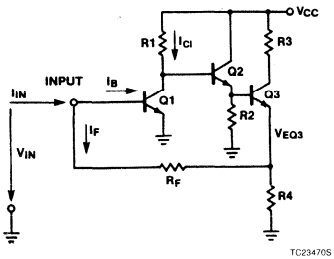


Figure 3. Shunt-Series Input Stage

portant. The input stage achieves a low input referred noise current (spectral density) of 2.5pA/$\sqrt{Hz}$. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input RMS noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 52nA in a 200MHz bandwidth for C_S = 1pF.

DYNAMIC RANGE:

The electrical dynamic range can be defined as the radio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 120μA and a wideband noise of I_{EQ} = 52nA$_{RMS}$ for an external source capacitance of C_S = 1pF.

$$D_E = \frac{\text{(Max. input current)}}{\text{(Peak noise current)}}$$

$$= 20 \log \frac{(120 \times 10^{-6})}{(\sqrt{2}\ 52 \times 10^{-9})}$$

$$= 20 \log \frac{(120\mu A)}{(73nA)} = 64dB.$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

$$\text{Energy of one photon} = \frac{hc}{\lambda} \text{ watt sec (Joule)}$$

Where h = Planck's Constant = 6.6×10^{-34} Joule sec.

c = speed of light = 3×10^8 mt/sec

c/λ = optical frequency

$$\text{No. of incident photons/sec} = \frac{\frac{P}{hc}}{\lambda} \text{ where}$$

P = optical incident power

$$\text{No. of generated electrons/sec} = \eta \cdot \frac{\frac{P}{hc}}{\lambda}$$

Where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole pairs}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \cdot \frac{\frac{P}{hc}}{\lambda} \cdot e \text{ Amps (Coulombs/sec.)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

$$\text{Responsivity } R = \frac{\frac{\eta \cdot e}{hc}}{\lambda} \text{ Amp/watt}$$

$I = P \cdot R$

Assuming a data rate of 400 Mbaud (Bandwidth, B = 200MHz), the noise parameter Z may be calculated as:

$$Z = \frac{i_{eq}}{qB} = \frac{52 \times 10^{-9}}{(1.6 \times 10^{-19})\ (200 \times 10^6)} = 1625$$

where Z is the ratio of RMS noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12 \frac{hc}{\lambda} B\ Z = 12\ 2.3 \times 10^{-19}$$

200×10^6 1625 = 897nW = −30.5dBm,

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum

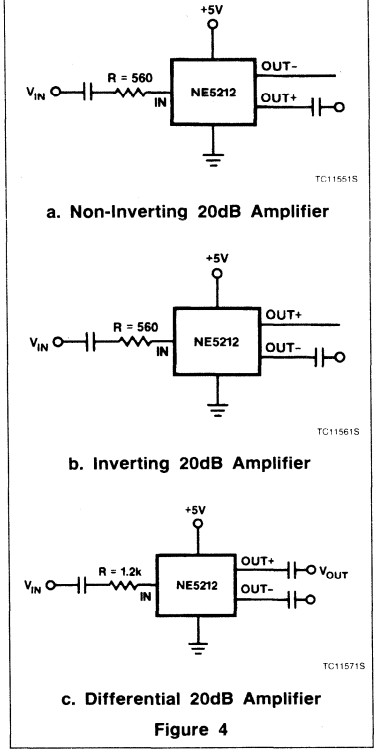


Figure 4

input current to the NE5212, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}$$

$$= \frac{897 \times 10^{-9} \times 1.6 \times 10^{-19}}{2.3 \times 10^{-19}}$$

= 624nA.

Choosing the maximum peak overload current of I_{avMAX} = 120μA, the maximum mean optical power is:

$$P_{avMAX} = \frac{hc\ I_{avMAX}}{\lambda\ q} = \frac{2.3 \times 10^{-19}}{1.6 \times 10^{-19}} = 120 \times 10^{-6}$$

= 86mW or −7.6 dBm.

Thus the optical dynamic range, D_o is:

$D_o = P_{avMAX} - P_{avMIN} = -30.5 - (-7.6) = 22.8dB.$

This represents the maximum limit attainable with the NE5212 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 820nm wavelength.

1. S. D. Personick, *Optical Fiber Transmission Systems*, Plenum Press, NY, 1981, Chapter 3.

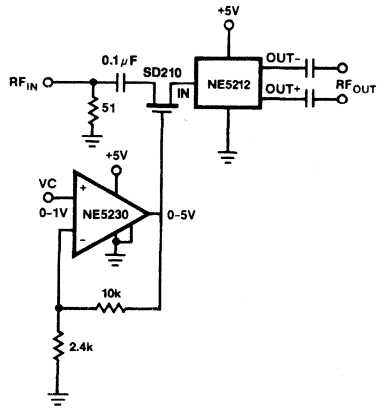


Figure 5. Variable Gain Circuit

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5212 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout such that Ground 1 and Ground 2 have very low impedance paths have produced the best results. This was acomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1μF high-frequency capacitor be inserted between V_{cc1} and V_{cc2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1μF capacitors with 10μF tantalum capacitors from each supply, V_{cc1} and V_{cc2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

BASIC CONFIGURATION

A trans resistance amplifier is a current-to-voltage converter. The forward transfer function then is defined as voltage out divided by current in, and is stated in ohms. The lower the source resistance, the higher the gain. The NE5212 has a differential transresistance of 14kΩ typically and a single-ended transresistance of 7kΩ typically. The device has two outputs: inverting and non-inverting. The output voltage in the differential output mode is twice that of the output voltage in the single-ended mode. Although the device can be used without coupling capacitors, more care is required to avoid upsetting the internal bias nodes of the device. Figure 4 shows some basic configurations.

VARIABLE GAIN

Figure 5 shows a variable gain circuit using the NE5212 and the NE5230 low voltage op amp. This op amp is configured in a non-inverting gain of five. The output drives the gate of the SD210 DMOS FET. The series resistance of the FET changes with this output voltage which in turn changes the gain of the NE5212. This circuit has a distortion of less than 1% and a 25dB range, from −42.2dBm to −15.9dBm at 50MHz, and a 45dB range, from −60dBm to −14.9dBm at 10MHz with 0 to 1V of control voltage at V_C.

16MHz CRYSTAL OSCILLATOR

Figure 6 shows a 16MHz crystal oscillator operating in the series resonant mode using the NE5212. The non-inverting input is fed back to the input of the NE5212 in series with a 2pF capacitor. The output is taken from the inverting output.

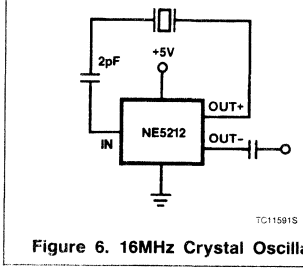


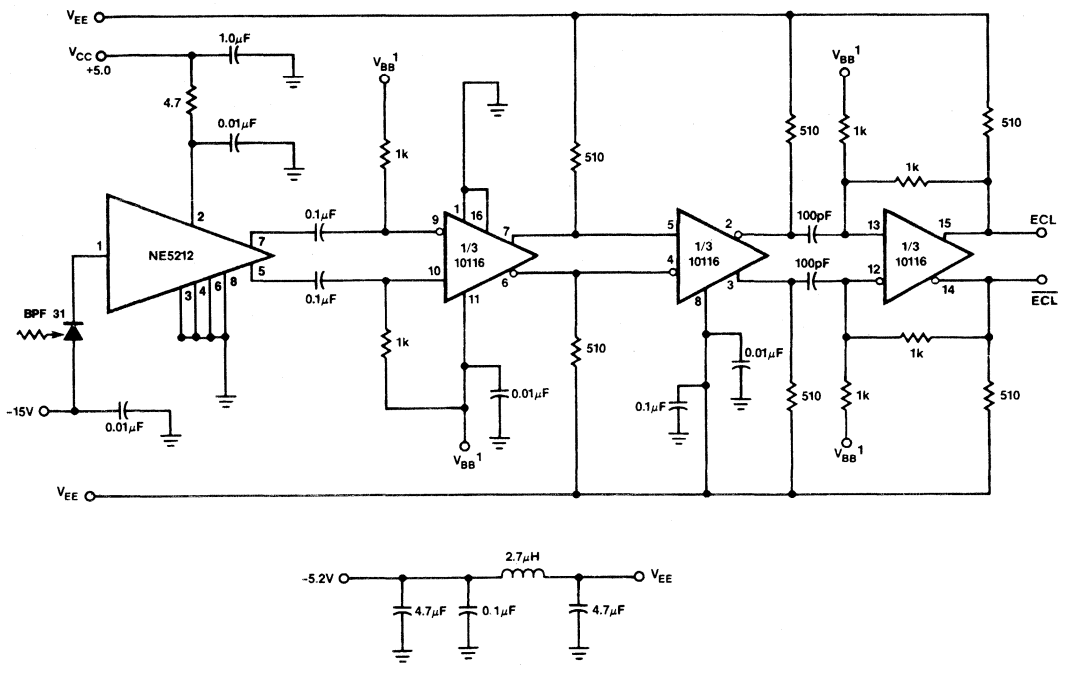
Figure 6. 16MHz Crystal Oscillator

DIGITAL FIBER OPTIC RECEIVER

Figures 7 and 8 show a fiber optic receiver using off-the-shelf components.

The receiver shown in Figure 7 uses the NE5212, the Signetics 10116 ECL line receiver, and Philips/Amperex BPF31 PIN diode. The circuit is a capacitor-coupled receiver and utilizes positive feedback in the last stage to provide the hysteresis. The amount of hysteresis can be tailored to the individual application by changing the values of the feedback resistors to maintain the desired balance between noise immunity and sensitivity. At room temperature, the circuit operates at 50Mbaud with a BER of 10E-10 and over the automotive temperature range at 40Mbaud with a BER of 10E-9. Higher speed experimental diodes have been used to operate this circuit at 220Mbaud with a BER of 10E-10.

Figure 8 depicts a TTL receiver using the NE5212 and the NE5214 fast amplifier system along with the Philips/Amperex PIN diode. The system shown is optimized for 50 Mb/s Non Return to Zero (NRZ) data. A link status indication is provided along with a jamming function when the input level is below a user-programmable threshold level.



NOTE:
1. Tie all V_{BB} points together.

Figure 7. ECL Fiber Optic Receiver

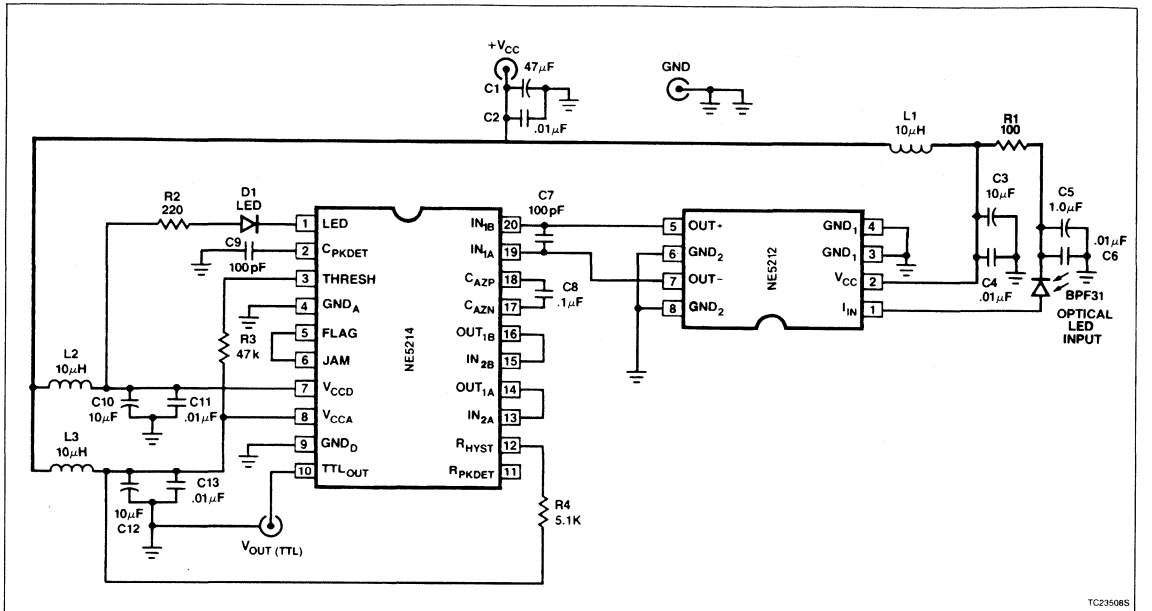


Figure 8. A 50Mb/S TTL Digital Fiber Optic Receiver

NE/SA5214
Postamplifier with Link Status Indicator

Preliminary Specification

DESCRIPTION

THE NE/SA5214 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The NE5214 can be DC coupled with the previous transimpedance stage using NE5210, NE5211 or NE5212 transimpedance amplifiers. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide noise filtering, adjustable input thresholds and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, insuring a low Bit Error Rate (BER). An Auto-Zero loop can be used to minimize the number of external coupling capacitors to one. A signal absent flag indicates when signals are below threshold. Additionally, the low signal condition forces the overall TTL output to a logical Low level. User interaction with this "jamming" system is available. The NE/SA5214 is packaged in a standard 20-pin surface-mount package and typically consumes 42mA from a standard 5V supply. The NE/SA5214 is designed as a companion to the NE/SA5211/5212 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the postamplifier inputs. The NE/SA5212/5214 or NE/SA5211/5214 combinations convert nanoamps of photodetector current into standard digital TTL levels.

FEATURES

- **Postamp for the NE/SA5211/5212 preamplifier family**
- **Wideband operation: typical 75MHz (100MBaud NRZ)**
- **Interstage filtering/equalization possible**
- **Single 5V supply**
- **Low signal flag**
- **Low signal output disable**
- **Link status threshold and hysteresis programmable**
- **LED driver (normally ON with above threshold signal)**
- **Fully differential for excellent PSRR**
- **Auto-zero loop for DC offset cancellation**
- **2kV ElectroStatic Discharge (ESD) protection**

APPLICATIONS

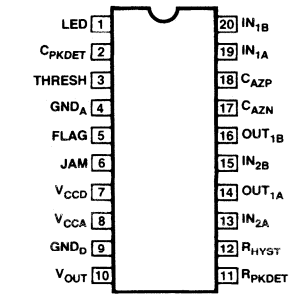
- **Fiber optics**
- **Communication links in Industrial and/or Telecom environment with high EMI/RFI**
- **Local Area Networks (LAN)**
- **Metropolitan Area Networks (MAN)**
- **Synchronous Optical Networks (SONET)**
- **RF limiter**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL	0 to +70°C	NE5214D
20-Pin Plastic SOL	−40°C to +85°C	SA5214D

PIN CONFIGURATION

D[1] Package



TOP VIEW

CD1532OS

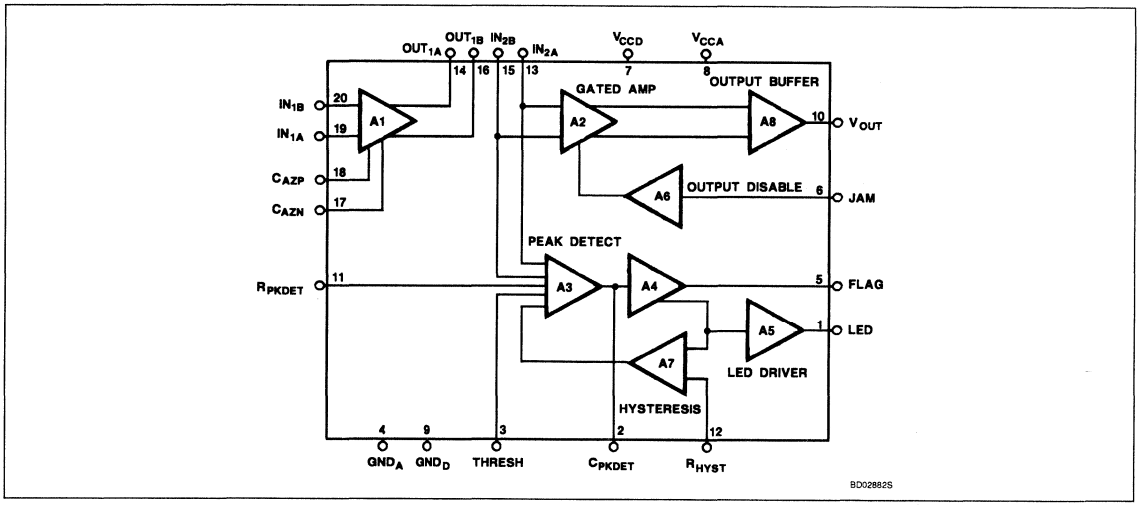
NOTE:
1. SOL — Released in large SO package only.

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON.
2	C_{PKDET}	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a TTL fanout of two.
6	JAM	Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, LOW. This pin is normally connected to the FLAG pin and is TTL-compatible.
7	V_{CCD}	Power supply pin for the digital portion of the chip.
8	V_{CCA}	Power supply pin for the analog portion of the chip.
9	GND_D	Device digital ground pin.
10	V_{OUT}	TTL output pin with a fanout of five.
11	R_{PKDET}	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}.

PIN CONFIGURATION (cont.)

PIN NO.	SYMBOL	DESCRIPTION
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{2A}	Non-inverting input to amplifier A2.
14	OUT_{1A}	Non-inverting output of amplifier A1.
15	IN_{2B}	Inverting input to amplifier A2.
16	OUT_{1B}	Inverting output of amplifier A1.
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Power supply	+6	+6	V
V_{CCD}	Power supply	+6	+6	V
T_A	Operating ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	−55 to +150	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	−65 to +150	°C
P_D	Power dissipation	300	300	mW
V_{IJ}	Jam input voltage	−0.5 to 5.5	−0.5 to 5.5	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Supply voltage	4.75 to 5.25	4.75 to 5.25	V
V_{CCD}	Power supply	4.75 to 5.25	4.75 to 5.25	V
T_A	Ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	0 to +95	−40 to +110	°C
P_D	Power dissipation	250	250	mW

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
I_{CCA}	Analog supply current			30	36		30	37.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.3		10	13.5	mA
V_{I1}	A1 input bias voltage (+/− inputs)		3.16	3.4	3.63	3.13	3.4	3.65	V
V_{O1}	A1 output bias voltage (+/− outputs)		3.17	3.8	4.45	3.10	3.8	4.50	V
A_{V1}	A1 DC gain (without Auto-Zero)			30			30		dB
$A1_{PSRR}$	A1 PSRR (V_{CCA}, V_{CCD})	$V_{CCA} = V_{CCD} = 4.75$ to 5.25V		60			60		dB
$A1_{CMRR}$	A1 CMRR	$\Delta V_{CM} = 200mV$		60			60		dB
V_{I2}	A2 input bias voltage (+/− inputs)		3.59	3.7	3.85	3.56	3.7	3.86	V
V_{OH}	High-level TTL output voltage	$I_{OH} = -200\mu A$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level TTL output voltage	$I_{OL} = 8mA$		0.3	0.4		0.3	0.4	V
I_{OH}	High-level TTL output current	$V_{OUT} = 2.4V$		−40	−26		−40	−24.4	mA
I_{OL}	Low-level TTL output current	$V_{OUT} = 0.4V$	8.0	30		7.0	30		mA

DC ELECTRICAL CHARACTERISTICS (Continued) Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
I_{OS}	Short-circuit TTL output current	$V_{OUT} = 0.0V$		-95			-95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75			0.75		V
V_{RPKDET}	RPKDET	Pin 11 Open		0.72			0.72		V
V_{RHYST}	RHYST bias voltage	Pin 12 Open		0.72			0.72		V
V_{IHJ}	High-level jam input voltage		2.0			2.0			V
V_{ILJ}	Low-level jam input voltage				0.8			0.8	V
I_{IHJ}	High-level jam input current	$V_{IJ} = 2.7V$			20			30	μA
I_{ILJ}	Low-level jam input current	$V_{IJ} = 0.4V$	-450	-240		-485	-240		μA
V_{OHF}	High-level flag output voltage	$I_{OH} = -80\mu A$	2.4	3.8		2.4	3.8		V
V_{OLF}	Low-level flag output voltage	$I_{OL} = 3.2mA$		0.33	0.4		0.33	0.4	V
I_{OHF}	High-level flag output current	$V_{OUT} = 2.4V$		-18	-5.3		-18	-5	mA
I_{OLF}	Low-level flag output current	$V_{OUT} = 0.4V$	3.6	10		3.25	10		mA
I_{SCF}	Short-circuit flag output current	$V_{OUT} = 0.0V$	-60	-40	-25	-61	-40	-26	mA
I_{LEDH}	LED ON maximum sink current	$V_{LED} = 3.0V$	13	22	80	8	22	80	mA

AC ELECTRICAL CHARACTERISTICS Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test circuit	60	75		60	75		MHz
BW_{A1}	Small signal bandwidth (differential OUT_1/IN_1)	Test circuit		75			75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test Circuit		1.6			1.6		V_{P-P}
V_{INL}	Minimum Functional A1 input signal (single ended)	Test CIrcuit[1]		12			12		mV_{P-P}
R_{IN1}	Input resistance (differential at IN_1)			1200			1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2			2		pF
R_{IN2}	Input resistance (differential at IN_2)			1200			1200		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2			2		pF

AC ELECTRICAL CHARACTERISTICS (Continued) Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
R_{OUT1}	Output resistance (differential at OUT_1)			25			25		Ω
C_{OUT1}	Output capacitance (differential at OUT_1)			2			2		pF
V_{HYS}	Hysteresis voltage	Test circuit		3			3		mV_{P-P}
V_{THR}	Threshold voltage range (FLAG ON)	Test circuit, @ 50MHz R_{RHYST}=5k R_{THRESH} = 47k		12			12		mV_{P-P}
t_{TLH}	TTL Output Rise Time 20% to 80%	Test Circuit		1.3			1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test Circuit		1.2			1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1			0.1		ns
t_{PWD}	Pulse width distortion of output	$50mV_{P-P}$, 1010. . .input Distortion = $\frac{T_H - T_L}{T_H + T_L} 10^2$	2.5				2.5		%

NOTE:
1. The NE/SA5214 is capable of detecting a much lower input level. Operation under $12mV_{P-P}$ cannot be guaranteed by present day automatic testers.

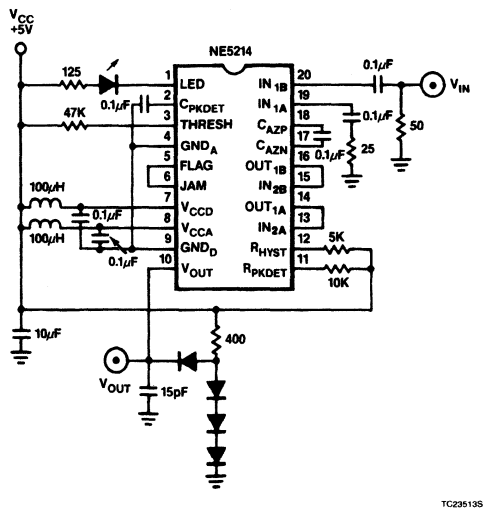
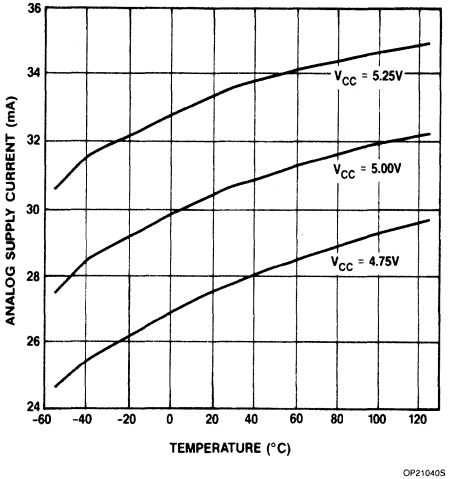


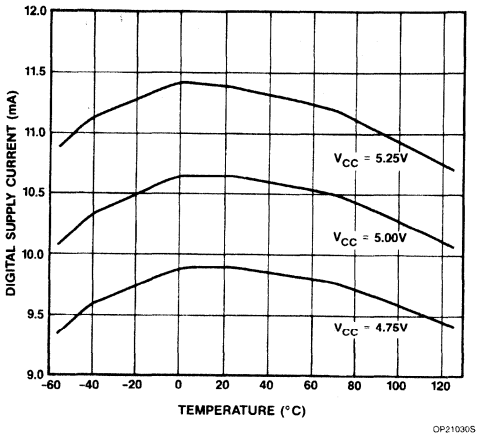
Figure 1. AC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

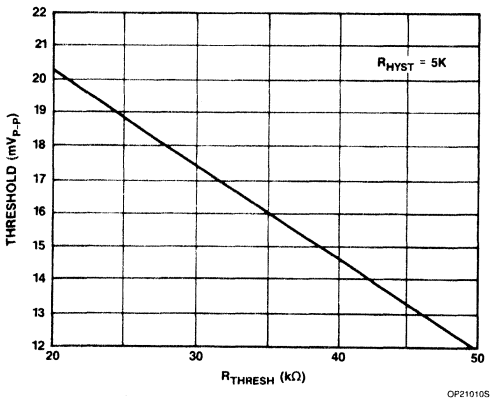
Analog Supply Current vs Temperature



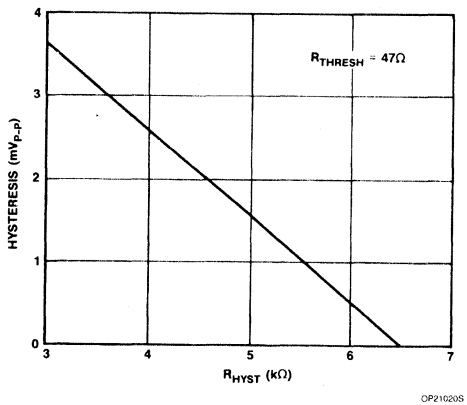
Digital Supply Current vs Temperature



Threshold Voltage vs R_{THRESH}



Hysteresis Voltage vs R_{HYST}



THEORY OF OPERATION AND APPLICATION INFORMATION

The NE 5214 postamplifier system is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

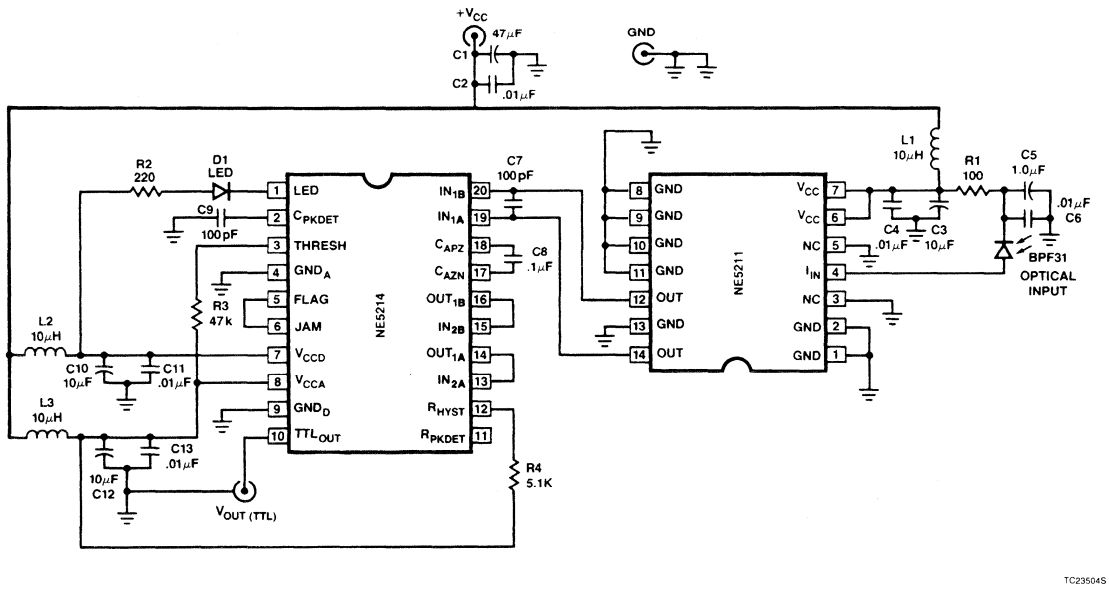
The NE5214 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL HIGH on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the ON state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back to the "JAM" input; this forces the TTL data OUT into a LOW state when no signal is present at the input.

An auto zero loop allows the NE5214 to be directly connected to a transimpedance amplifier such as the NE5210, NE5211, or NE5212 without coupling capacitors. This auto-zero loop cancels the transimpedance amplifier's DC offset, the NE5214 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination. For more information on the NE5214 Theory of Operation, please refer to paper titled "A Low Cost 100 MBaud Fiber-Optic Receiver" by W. Mack et al.

A typical application of the NE5214 postamplifier is depicted in Figure 2. The system uses the NE5211 transimpedance amplifier which has a 28k differential transimpedance gain and a −3dB bandwidth of 140MHz. This typical application is optimized for a 50 Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.

For more information on this application, please refer to AB 1432.



NOTE:
The NE5211/NE5214 combination can operate at data rates in excess of 100Mb/s NRZ.

Figure 2. A 50Mb/s Fiber Optic Receiver

NE/SA5217
Fiber Optic Postamplifier with Link Status Indicator

Objective Specification

DESCRIPTION

THE NE/SA5217 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The NE5217 can be DC coupled with the previous transimpedance stage using NE5210, NE5211 or NE5212 transimpedance amplifiers. The main difference between the NE5217 and the NE5214 is that the NE5217 does not make the output of A1 and input of A2 accessible, instead, it brings out the output of A2 and the input of A8 thus activating the on-chip Schmidt trigger function by connecting two external capacitors. The result is that a much longer string of 1's and 0's, in the bit stream, can be tolerated. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide adjustable input thresholds and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, insuring a low Bit Error Rate (BER). An Auto-Zero loop can be used to minimize the number of external coupling capacitors to one. A signal absent flag indicates when signals are below threshold. Additionally, the low signal condition forces the overall TTL output to a logical Low level. User interaction with this "jamming" system is available. The NE/SA5217 is packaged in a standard 20-pin surface-mount package and typically consumes 42mA from a standard 5V supply. The NE/SA5217 is designed as a companion to the NE/SA5211/5212 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the post-amplifier inputs. The NE/SA5212/5217 or NE/SA5211/5217 combinations convert nanoamps of photodetector current into standard digital TTL levels.

FEATURES

- **Postamp for the NE/SA5211/5212 preamplifier family**
- **Wideband operation: typical 75MHz (100MBaud NRZ)**
- **Interstage filtering/equalization possible**
- **Single 5V supply**
- **Low signal flag**
- **Low signal output disable**
- **Link status threshold and hysteresis programmable**
- **LED driver (normally ON with above threshold signal)**
- **Fully differential for excellent PSRR**
- **Auto-zero loop for DC offset cancellation**
- **2kV ElectroStatic Discharge (ESD) protection**

APPLICATIONS

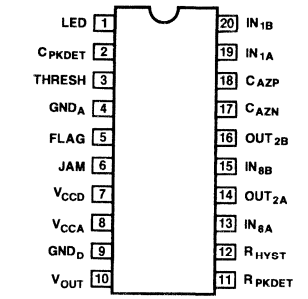
- **Fiber optics**
- **Communication links in Industrial and/or Telecom environment with high EMI/RFI**
- **Local Area Networks (LAN)**
- **Metropolitan Area Networks (MAN)**
- **Synchronous Optical Networks (SONET)**
- **RF limiter**
- **Good for 2^{23}-1 pseudo random number sequence**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL	0 to +70°C	NE5217D
20-Pin Plastic SOL	−40°C to +85°C	SA5217D

PIN CONFIGURATION

D[1] Package



CD15321S

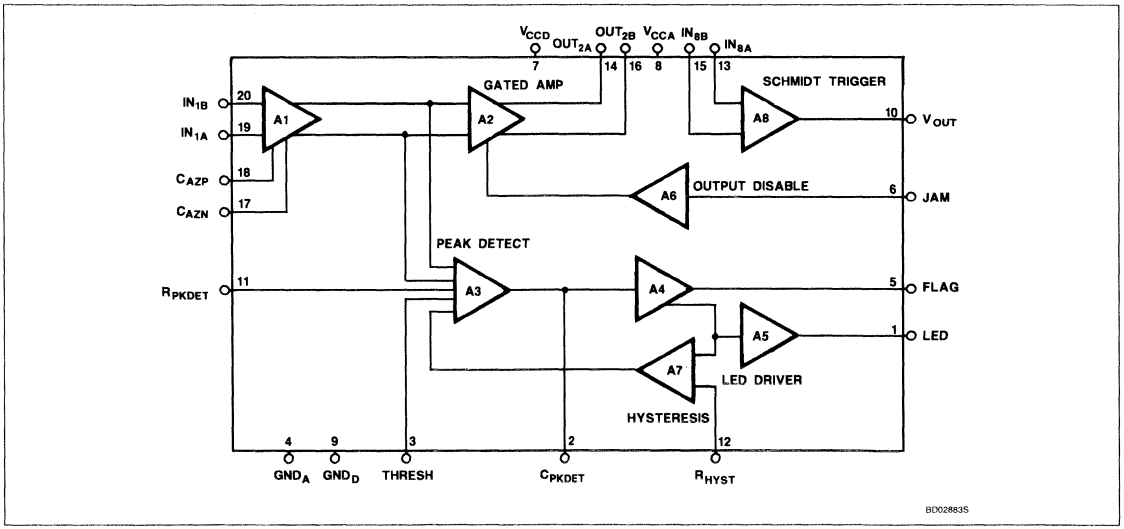
NOTE:
1. SOL — Released in large SO package only.

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON.
2	C_{PKDET}	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a fanout of two.
6	JAM	Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, Low. This pin is normally connected to the FLAG pin and is TTL-compatible.
7	V_{CCD}	Power supply pin for the digital portion of the chip.
8	V_{CCA}	Power supply pin for the analog portion of the chip.
9	GND_D	Device digital ground pin.
10	V_{OUT}	TTL output pin with a fanout of five.
11	R_{PKDET}	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}.

PIN CONFIGURATION (cont.)

PIN NO.	SYMBOL	DESCRIPTION
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{8A}	Non-inverting input to amplifier A8.
14	OUT_{2A}	Non-inverting output of amplifier A2.
15	IN_{8B}	Inverting input to amplifier A8.
16	OUT_{2B}	Inverting output of amplifier A2.
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM



Fiber Optic Postamplifier with Link Status Indicator

NE/SA5217

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Power supply	+6	+6	V
V_{CCD}	Power supply	+6	+6	V
T_A	Operating ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	-55 to +150	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C
P_D	Power dissipation	300	300	mW
V_{IJ}	Jam input voltage	-0.5 to 5.5	-0.5 to 5.5	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Supply voltage	4.75 to 5.25	4.75 to 5.25	V
V_{CCD}	Power supply	4.75 to 5.25	4.75 to 5.25	V
T_A	Ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	0 to +95	-40 to +110	°C
P_D	Power dissipation	250	250	mW

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5214			SA5214			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{CCA}	Analog supply current			30	36		30	37.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.3		10	13.5	mA
V_{I1}	A1 input bias voltage (+/- inputs)	3.16	3.4	3.63	3.13	3.4	3.65	V	
V_{O1}	A1 output bias voltage (+/- outputs)	3.17	3.8	4.45	3.10	3.8	4.50	V	
A_{V1}	A1 DC gain (without Auto-Zero)			30			30		dB
$A1_{PSRR}$	A1 PSRR (V_{CCA}, V_{CCD})	$V_{CCA} = V_{CCD} = 4.75$ to 5.25V		60			60		dB
$A1_{CMRR}$	A1 CMRR	$\Delta V_{CM} = 200mV$		60			60		dB
V_{I8}	A8 input bias voltage (+/- inputs)	3.59	3.7	3.85	3.7	3.86	V		
V_{OH}	High-level TTL output voltage	$I_{OH} = -200\mu A$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level TTL output voltage	$I_{OL} = 8mA$		0.3	0.4		0.3	0.4	V
I_{OH}	High-level TTL output current	$V_{OUT} = 2.4V$		-40	-26		-40	-24.4	μA
I_{OL}	Low-level TTL output current	$V_{OUT} = 0.4V$	8.0	30		7.0	30		mA
I_{OS}	Short-circuit TTL output current	$V_{OUT} = 0.0V$		-95			-95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75			0.75		V
V_{RPKDET}	RPKDET	Pin 11 Open		0.72			0.72		V
V_{RHYST}	RHYST bias voltage	Pin 12 Open		0.72			0.72		V
V_{IHJ}	High-level jam input voltage		2.0			2.0			V
V_{ILJ}	Low-level jam input voltage				0.8			0.8	V
I_{IHJ}	High-level jam input current	$V_{IJ} = 2.7V$			20			30	μA

Fiber Optic Postamplifier with Link Status Indicator

NE/SA5217

DC ELECTRICAL CHARACTERISTICS (Continued)

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5214			SA5214			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{ILJ}	Low-level jam input current	$V_{IJ} = 0.4V$	-450	-240		-485	-240		μA
V_{OHF}	High-level flag output voltage	$I_{OH} = -80\mu A$	2.4	3.8		2.4	3.8		V
V_{OLF}	Low-level flag output voltage	$I_{OL} = 3.2mA$		0.33	0.4		0.33	0.4	V
I_{OHF}	High-level flag output current	$V_{OUT} = 2.4V$		-18	-5.3		-18	-5	mA
I_{OLF}	Low-level flag output current	$V_{OUT} = 0.4V$	3.6	10		3.25	10		mA
I_{SCF}	Short-circuit flag output current	$V_{OUT} = 0.0V$	-60	-40	-25	-61	-40	-26	mA
I_{LEDH}	LED ON maximum sink current	$V_{LED} = 3.0V$	13	22	80	8	22	80	mA

AC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5214			SA5214			UNIT
			Min	Typ	Max	Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test Circuit	60	75		60	75		MHz
BW_{A1}	Small signal bandwidth (differential OUT_1/IN_1)	Test Circuit		75			75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test Circuit		1.6			1.6		V_{P-P}
V_{INL}	Maximum Functional A1 input signal (single ended)	Test Circuit[1]		12			12		mV_{P-P}
R_{IN1}	Input resistance (differential at IN_1)			1200			1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2			2		pF
R_{IN2}	Input resistance (differential at IN_2)			1200			1200		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2			2		pF
R_{OUT1}	Output resistance (differential at OUT_1)			25			25		Ω
C_{OUT1}	Output capacitance (differential at OUT_1)			2			2		pF
V_{HYS}	Hysteresis voltage range	Test circuit, $T_A = 25°C$		3			3		mV_{P-P}
V_{THR}	Threshold voltage range (FLAG ON)	Test circuit, @ 50MHz R_{RHYST}=5k R_{THRESH} = 47k		12			12	mV_{P-P}	
t_{TLH}	TTL Output Rise Time 20% to 80%	Test circuit		1.3			1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test circuit		1.2			1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1			0.1		ns
t_{PWD}	Pulse width distortion of output	$50mV_{P-P}$, 1010. . .input Distortion = $\frac{T_H - T_L}{T_H + T_L} 10^2$	2.5				2.5		%

NOTE:

1. The NE/SA5217 is capable of detecting a much lower input level. Operation under $12mV_{P-P}$ cannot be guaranteed by present day automatic testers.

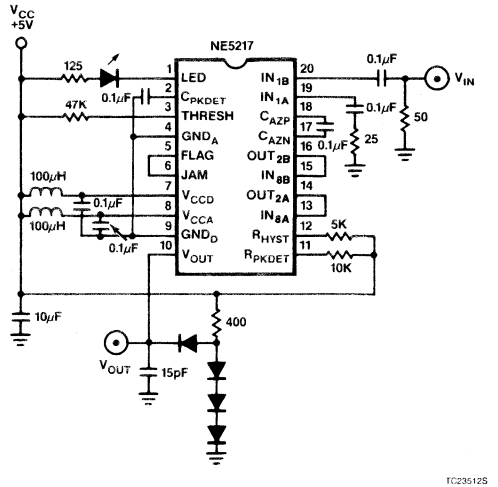
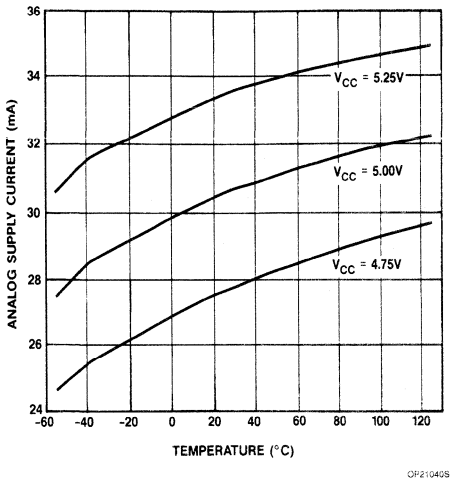


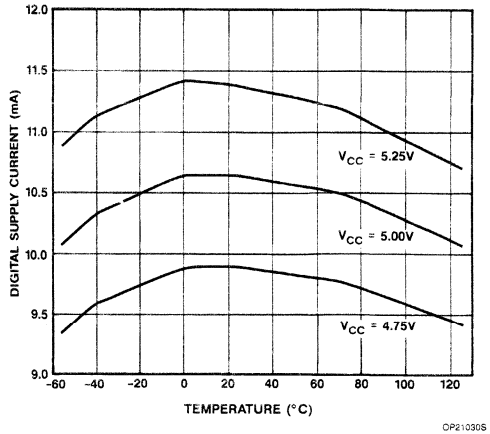
Figure 1. AC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

Analog Supply Current vs Temperature



Digital Supply Current vs Temperature



Fiber Optic Postamplifier with Link Status Indicator

THEORY OF OPERATION AND APPLICATION INFORMATION

The NE 5217 post amplifier system is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

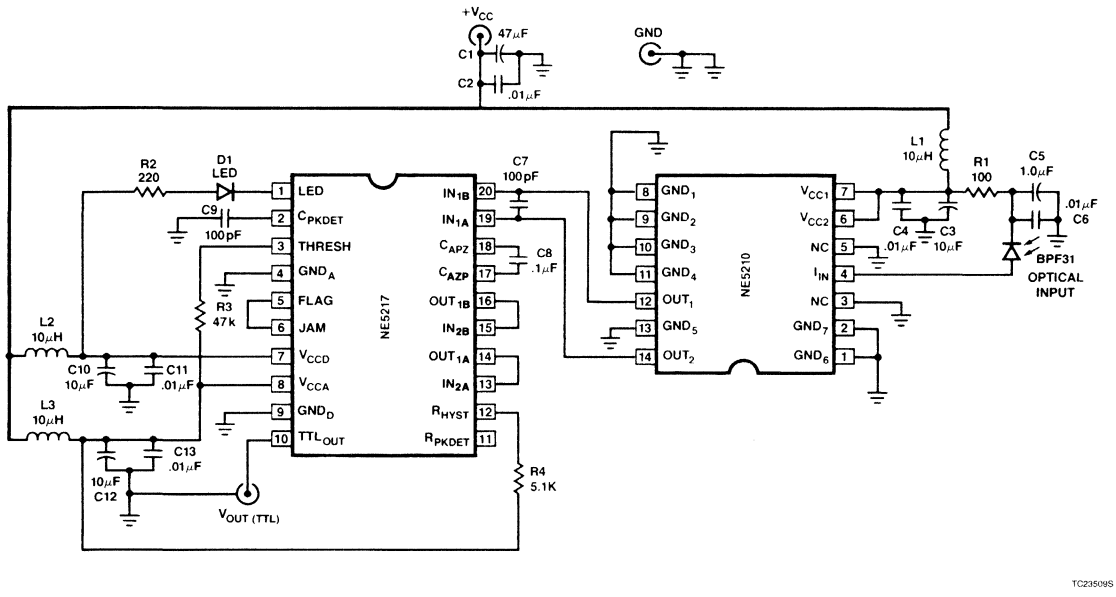
The NE5217 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL HIGH on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the ON state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back to the "JAM" input; this forces the TTL data OUT into a LOW state when no signal is present at the input.

An auto zero loop allows the NE5217 to be directly connected to a transimpedance amplifier such as the NE5210, NE5211, or NE5212 without coupling capacitors. This auto-zero loop cancels the transimpedance amplifiers's DC offset, the NE5217 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination. For more information on the NE5217 Theory of Operation, please refer to paper titled "A Low Cost 100 MBaud Fiber-Optic Receiver" by W. Mack et a1.

A typical application of the NE5217 post amplifier is depicted in Figure 2. The system uses the NE5211 transimpedance amplifier which has a 28k differential transimpedance gain and a -3dB bandwidth of 140MHz. This typical application is optimized for a 50 Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.

For more information on this application, please refer to Application Brief AB 1432.



NOTE:
The NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ.

Figure 2. A 50Mb/s Fiber Optic Receiver

DATA CONVERSION

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AN100
An Overview of Data Converters

Application Note

INTRODUCTION

Large systems are comprised of many different subsystems, all of which must interface to complete the system. All types of circuits, including linear, digital and discrete, are often used in the subsystems.

Interface circuits provide the necessary function of tying the parts of a system together. These circuits are usually not purely linear or digital but contain both types of circuit functions. For instance, sense amplifiers are designed for interface between low level memory outputs and bipolar levels, while differential comparators are designed for interface between analog systems and logic systems.

CONVERTERS

Digital communications, digital instruments and displays have created a demand for low cost reliable converters. Key factors in this demand are:

- The need to communicate with digital computers and equipment for processing and storage of analog signals.
- Severe limitations encountered in reliable analog data transmission over any considerable distance.
- The need for more easily readable displays.

General application areas for converters include: Data processing, data transmission, graphics and displays, audio systems, control systems and arithmetic operations.

SPECIFIC APPLICATIONS

Test Systems

- Transistor tester (Force I_B and I_C)
- Resistor matching
- Programmable power supplies
- Programmable pulse generators
- Programmable current source
- Function generators (ROM drive)

Arithmetic Operations

- Analog division by a digital word
- Analog quotient of 2 digital words
- Analog product of 2 digital words — squaring
- Addition and subtraction with analog output
- Magnitude comparison of 2 digital words
- Digital quotient of 2 analog variables
- Arithmetic operations with words from different logic families

Graphics and Displays

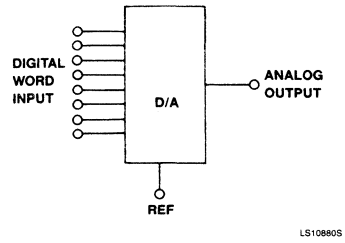
- Polar-to-rectangular conversion
- CRT character generation
- Chart recorder driver
- CRT displays

Data Transmission

- Modem transmitter
- Differential line driver
- Party line multiplexing of analog signals
- Multilevel 2-wire data transmission
- Secure communications (constant power dissipation)

Control Systems

- Reference level generator for setpoint controllers
- Positive peak detector
- Negative peak detector
- Disc drive head positioner
- Microfilm head positioner



NOTES:
Output = Ref. × digital word

$$\text{Output} = \text{Ref.} \times \left(\frac{B_1}{2} + \frac{B_2}{4} + \ldots + \frac{B_N}{2^N}\right)$$

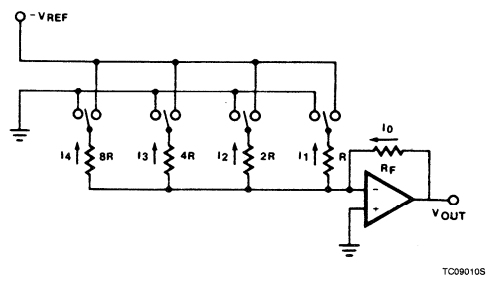
Figure 1. Conversion of a Digitally Coded Signal Input Into an Analog Signal Output

Audio Systems

- Digital AVC and reverberation
- Music distribution
- Organ tone generator
- Audio tracking A/D
- Speech compression and expansion
- Audio digitizing and decoding

DAC Building Blocks

The actual implementation of a D/A system contains four separate parts: A reference quantity; a set of binary switches to simulate binary coefficients $B_1 \ldots B_N$; a weighting network; and an output summing means.



NOTE:

$$V_{OUT} = \frac{R_F}{R} V_{REF} \times \left(b1 + \frac{b_2}{2} + \frac{b_4}{4} + \frac{b_8}{8}\right)$$

Figure 2. Binary-Weighted Ladder Employing Voltage Switching

DAC PRODUCTS SUMMARY

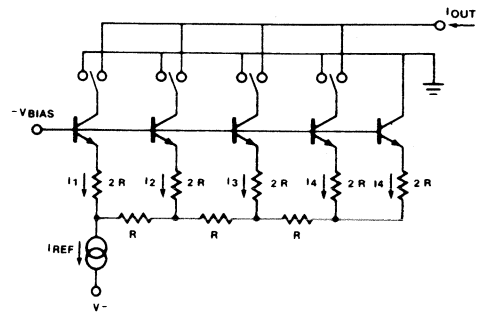
DEVICE	BITS	ACC. %	CONV. SPEED (μs)	OUTPUT		INT REF	INT. LATCH	PACKAGE			TEMPERATURE RANGE		COMMENTS
				V	I			N	D	F	Com'l	Mil	
NE5150	4	0.39	0.01	X		X	X			X	X		3 × 4 Bits with RAM
NE5151	4	0.39	0.01	X		X	X			X	X		3 × 4 Bits w/o RAM
NE5152	4	0.39	0.01	X		X	X			X	X		3 × 4 Bits with RAM
TDA8442	6	0.78		X			X	X			X		4 × 6 Bits I^2C
TDA8444	6	0.78		X			X	X			X		8 × 6 Bits I^2C
MC1408-7	8	0.39	0.07		X			X		X	X		
MC1408-8	8	0.19	0.07		X			X	X	X	X		
MC1508-8	8	0.19	0.07		X					X		X	
DAC08	8	0.19	0.07		X					X		X	
DAC08A	8	0.10	0.07		X					X		X	
DAC08C	8	0.39	0.07		X			X		X	X		
DAC08E	8	0.19	0.07		X			X	X	X	X		
DAC08H	8	0.10	0.07		X			X		X	X		
NE5018	8	0.19	2.3	X		X	X	X	X	X	X		
SE5018	8	0.19	2.3	X		X	X			X		X	
NE5019	8	0.10	2.3	X		X	X	X	X	X	X		
SE5019	8	0.10	2.3	X		X	X			X		X	
NE5118	8	0.19	0.2		X	X	X	X	X	X	X		
SE5118	8	0.19	0.2		X	X	X			X		X	
NE5119	8	0.10	0.2		X	X	X	X	X	X	X		
SE5119	8	0.10	0.2		X	X	X			X	X		
PNA7518	8	0.19	0.013	X			X	X			X		30MHz sampling rate
TDA5702	8	0.39	0.04	X		X	X	X			X		25MSPs
MC3410C	10	0.10	0.25		X			X		X	X		
NE5020	10	0.10	5.0	X		X	X	X		X	X		
NE5410	10	0.05	0.25		X					X	X		± ¼ LSB DNL
SE5410	10	0.05	0.25		X					X		X	± ¼ LSB DNL
MC3410	10	0.05	0.25		X			X		X	X		± ½ LSB DNL
MC3510	10	0.05	0.25		X					X		X	± ½ LSB DNL
AM6012	12	0.05	0.25		X					X	X		± 1 LSB DNL
DAC800V	12	0.012	5.0	X		X		X		X	X		
DAC800I	12	0.012	1.0		X	X		X		X	X		
TDA1540D	14	0.012	0.5		X	X	X			X	X		serial input ± ½ LSB DNL
TDA1540	14	0.003	0.5		X	X	X	X		X	X		serial input
TDA1541	16	0.0008	1.0		X	X	X	X			X		serial input

Binary-Weighted Ladder Employing Voltage Switching

The disadvantages of a binary-weighted ladder employing voltage switching include: a wide range of resistor values which are used in weighting the network, and nodal capacitances which are charged/discharged during conversion (See Figure 2).

R-2R Ladder Network Employing Current Switching

The advantages of this type of network include: no need for a wide range of resistor values, and current switching eliminates transients in nodal parasite capacitances (See Figure 3).



NOTE:
$I_{OUT} = I_{REF} \times (\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{8})$

Figure 3. R-2R Ladder Network Employing Current Switching

KEY SPECIFICATIONS

Speed

The conversion process should represent the input signal with the highest fidelity and minimal lag in time (real-time applications).

Settling Time

Settling time is a measure of a converter's speed and is defined as the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ± ½ LSB (See Figure 4).

Errors

Offset Error — The output current or voltage of a DAC with zero code input. (See Figure 5). Offset can and usually is trimmed to zero with an offset zero adjust circuit.

Gain Error — Deviation in output voltage from correct level when the input calls for a full-scale output. This error may be trimmed to zero (See Figure 6).

Relative Accuracy — The maximum deviation of the DAC output relative to an ideal straight line drawn from zero scale to full-scale (See Figure 7).

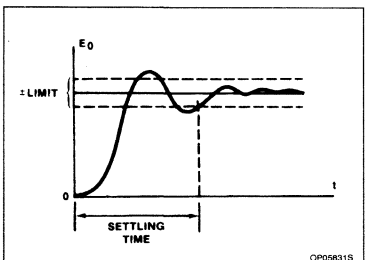


Figure 4. Settling Time

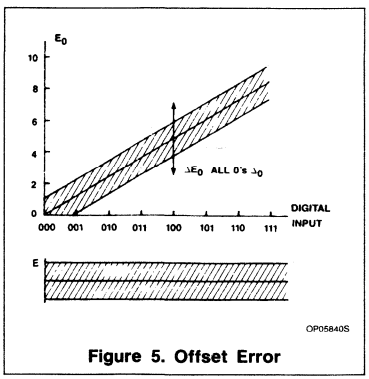


Figure 5. Offset Error

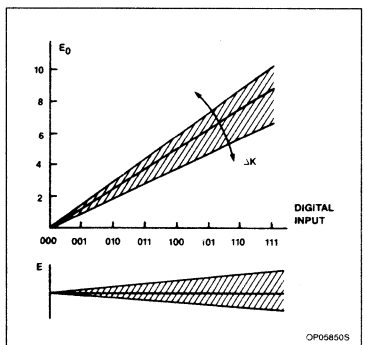


Figure 6. Gain Error

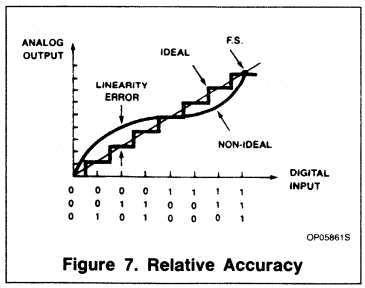


Figure 7. Relative Accuracy

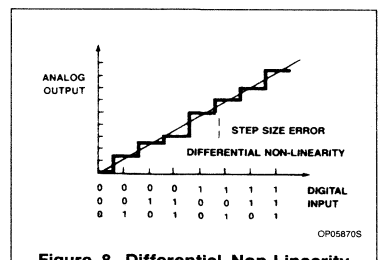


Figure 8. Differential Non-Linearity

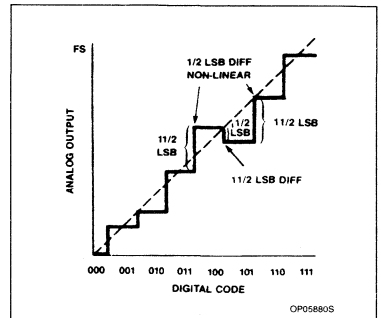


Figure 9. Non-Monotonic (Must be > ± ½ LSB Non-Linear)

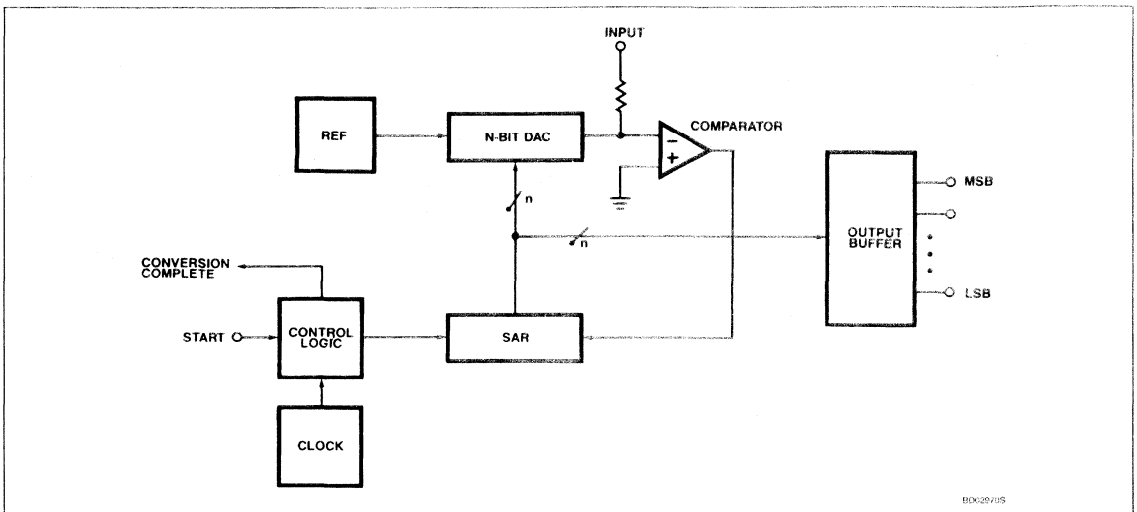


Figure 10. Block Diagram of a Successive Approximation A/D Converter

Differential Non-Linearity — Incremental error from any ideal LSB analog output change when the digital input is changed 1 LSB (See Figure 8).

Monotonicity — As the input code is incremented from one code to the next in sequence, the analog output will either increase or remain constant (See Figure 9).

Stability

Stability is a measure of the independence of converter parameters with respect to variations in external conditions such as temperature and supply voltage.

Temperature Coefficient — The effects of temperature changes of the output. Specified as % full-scale change per degree C.

Supply Rejection — Ability to resist changes in the output with supply changes, specified as % full-scale change per volt of supply change.

Long Term Stability — Measure of how stable the output is over a long period of time.

A/D CONVERTER CIRCUITS

Analog-to-Digital conversion schemes generally fall into one of three categories:

1. Feedback
- Counting
- Tracking (up-down)
- Successive approximation

2. Integrating
- Single slope
- Dual slope
- Triple slope

3. Parallel (Flash)

The type of converter chosen for a given application depends upon many things; the accuracy required, the conversion speed necessary, the necessary immunity to noise, and cost are some of these considerations.

The successive approximation technique is the one most widely used, mainly because of its excellent tradeoffs in resolution, speed, accuracy, and cost.

Figure 10 shows a simplified block diagram of a successive approximation A/D converter. Upon receiving the start signal, the successive approximation register (SAR) is cleared and the most significant bit (MSB) of that register is set. The SAR output is connected to the input of the DAC, the output of which is compared with the unknown input. If the input is less than the DAC output, the MSB is cleared and the next bit is set; if the input is greater than the DAC output, the MSB is left high and the next bit is set. The input is again compared with the DAC output and the second bit cleared or left high, based on the same criteria as for the MSB. This process continues until all bits have been determined. The analog input should not change appreciably during the conversion time. If it did change during this time, the converted output would not be a true indication of the analog input. For this reason, it is common practice to use a sample-and-hold circuit at the converter analog input to hold the input value constant during the conversion process. A sample-and-hold circuit is not necessary if the signal at the input of the converter varies slowly enough and has a noise level low enough so that the input will not change a significant amount during the conversion. The allowable input change during this conversion is generally accepted as the value of ½ LSB (for n-bit accuracy).

Accuracy and speed are determined primarily by the properties of the DAC and the comparator. Linearity is determined primarily by the linearity of the DAC. If the DAC is non-monotonic, one or more codes will be missing from the A/D converter's output range.

Figure 11 is the transfer function of a 3-bit binary coded A/D converter with a 0 to + 10V input range. A 3-bit ADC is shown for simplicity, but the principle applies to ADCs of any resolution. Note that there is a ½ LSB offset at the input such that the first count occurs when the input is equal to ½ LSB. The center of the range for the first step occurs, therefore, when the input is equal to the value of one LSB, and the error at the switch point is limited to ½ LSB. This error is known as the quantization error as it is derived from the smallest input quantity that can be resolved. If an ADC has a specified error of ½ LSB maximum, this means that any transition point can be as far as ½ LSB from where it should be.

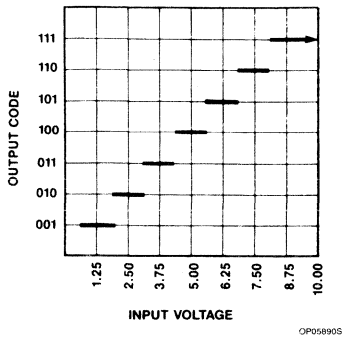


Figure 11. Transfer Function of an Ideal 3-bit ADC With a 0 to 10V Input Range

CONSIDERATIONS FOR A/D CONVERTERS

- Analog input signal range and resolution required
- Linearity requirement and stability
- Conversion speed required
- Monotonicity requirement: Can missing codes be tolerated?
- Character of input signal: Is it noisy, sampled, filtered, slowly varying?
- Transfer characteristics (type of coding)

A/D CONVERTER TERMS

Resolution

Resolution is the input change required to increment the output between the two adjacent codes. This term also refers to the number of bits in the output word and, hence, the number of discrete output codes the input analog signal can be broken into. Expressed in "bits" resolution.

Transfer Characteristic

The Transfer Characteristic is the relationship of the output digital word (code) to the input analog signal, i.e., Binary, BCD.

Conversion Speed

The Conversion Speed is the speed at which an ADC can make repetitive data conversions.

Quantizing Error

Quantizing Error is an inherent error in the conversion process due to finite resolution (discrete output). See Figure 12.

Offset Error

An Offset Error is shown in Figure 13.

Gain Error

A Gain Error is shown in Figure 14.

Relative Accuracy

Relative Accuracy is the deviation of an actual bit transition from the ideal transition value at any level over the range of the ADC (% FS). See Figure 15.

Hysteresis Error

A Hysteresis Error is the code transition voltage dependence relative to the direction from which the transition is approached.

Monotonicity

Monotonicity is when the output code either increases or remains the same for increasing analog input signals. The opposite is true in the reverse direction.

Missing Codes

A Missing Code is a code combination that is skipped. See Figure 16.

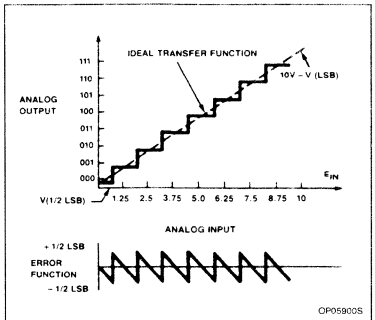


Figure 12. Quantizing Errors

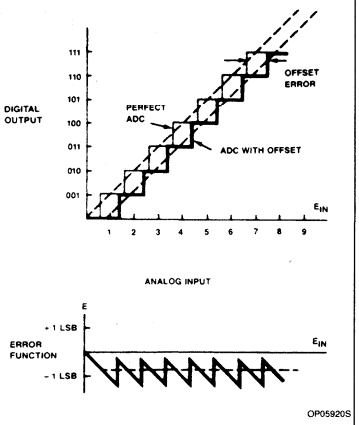


Figure 13. Offset Error

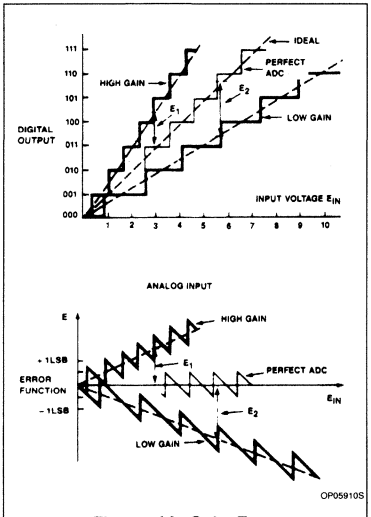


Figure 14. Gain Error

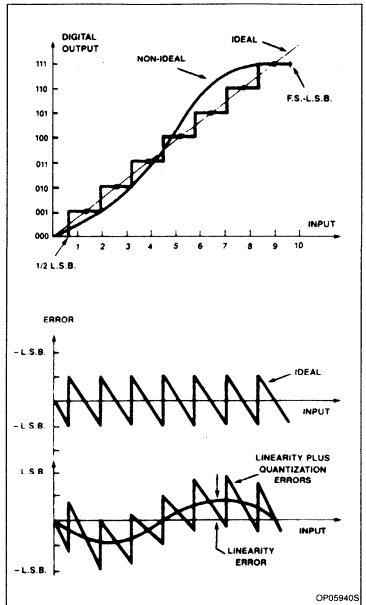


Figure 15. Relative Accuracy

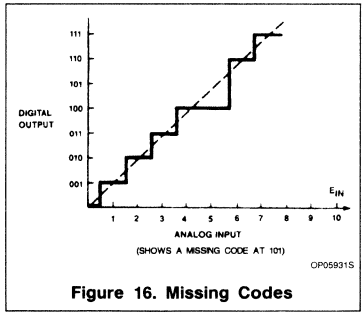


Figure 16. Missing Codes

Sample-and-hold amplifiers

		page
LF198	sample-and-hold amplifier	393
LF298	sample-and-hold amplifier	393
LF398	sample-and-hold amplifier	393
NE5060	precision high-speed sample-and-hold amplifier	398
NE5537	low leakage sample-and-hold amplifier	403
SE5060	precision high-speed sample-and-hold amplifier	398
SE5537	low leakage sample-and-hold amplifier	403

LF198/LF298/LF398
Sample-and-Hold Amplifiers

Product Specification

DESCRIPTION

The LF198/LF298/LF398 are monolithic sample-and-hold circuits which utilize high-voltage ion-implant JFET technology to obtain ultra-high DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FETs are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1μF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feedthrough from input to output in the hold mode even for input signals equal to the supply voltages.

Logic inputs are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS; differential threshold is 1.4V. The LF198/LF298/LF398 will operate from ±5V to ±18V supplies. They are available in an 8-lead TO-5 package, or an 8-pin plastic DIP.

FEATURES

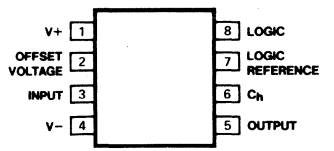
- **Operates from ±5V to ±18V supplies**
- **Less than 10μs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at $C_H = 0.01\mu F$**
- **Low input offset**
- **0.002% gain accuracy**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**

APPLICATION

- **The LF198/LF298/LF398 are ideally suited for a wide variety of sample-and-hold applications, including data acquisition, analog-to-digital conversion, synchronous demodulation, and automatic test setup**

PIN CONFIGURATIONS

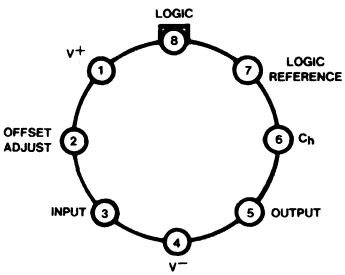
FE, N Packages



TOP VIEW

CD10920S

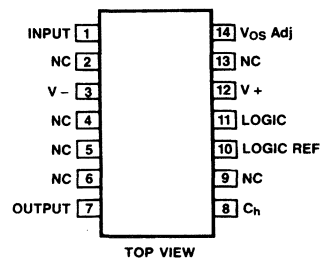
H Package



TOP VIEW

CD10931S

D Package[1]



TOP VIEW

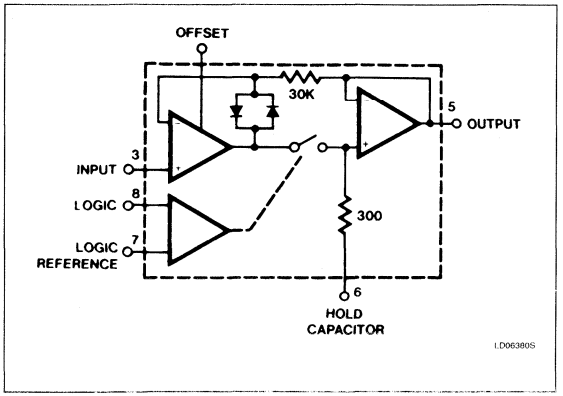
CD10940S

NOTE:
1. SO and non-standard pinouts.

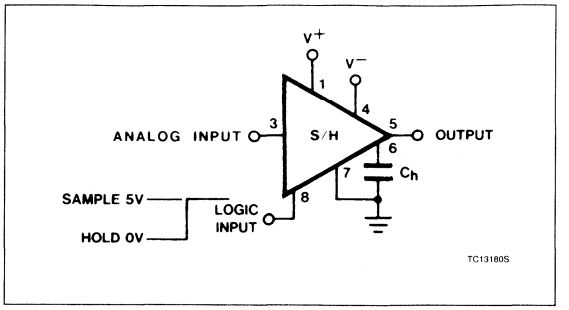
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
8-Pin Cerdip	−55°C to +125°C	LF198FE
8-Pin Metal Can	−55°C to +125°C	LF198H
14-Pin Plastic SO Package	0 to +70°C	LF398D
8-Pin Cerdip	0 to +70°C	LF398FE
8-Pin Metal Can	0 to +70°C	LF398H
8-Pin Plastic DIP	0 to +70°C	LF398N
8-Pin Cerdip	−25°C to +85°C	LF298FE
8-Pin Metal Can	−25°C to +85°C	LF298H

FUNCTIONAL DIAGRAM



TYPICAL APPLICATIONS



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±18	V
	Maximum power dissipation T_A = 25°C (still-air)[3] F package N package D package	 780 1160 1040	 mW mW mW
T_A	Operating ambient temperature range LF198 LF298 LF398	 −55 to +125 −25 to +85 0 to +70	 °C °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
V_{IN}	Input voltage	Equal to supply voltage	
	Logic-to-logic reference differential voltage[2]	+7, −30	V
	Output short-circuit duration	Indefinite	
	Hold capacitor short-circuit duration	10	sec
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. The maximum junction temperature of the LF398 is 150°C. When operating at elevated ambient temperature, the packages must be derated based on the thermal resistance specified.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 8.3mW/°C

DC ELECTRICAL CHARACTERISTICS Unless otherwise specified, the following conditions apply: unit is in "sample" mode; $V_S = \pm 15V$; $T_J = 25°C$; $-11.5V \leq V_{IN} \leq +11.5V$; $C_H = 0.01\mu F$; and $R_L = 10k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

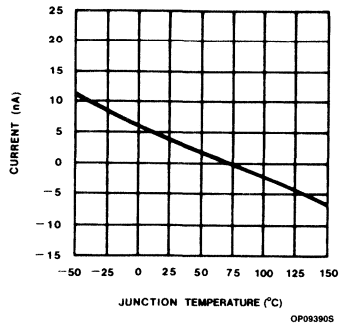
SYMBOL	PARAMETER	TEST CONDITIONS	LF198/LF298			LF398			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[4]	$T_J = 25°C$		1	3 5		2	7 10	mV mV
I_{BIAS}	Input bias current[4]	$T_J = 25°C$ Full temperature range		5	25 75		10	50 100	nA nA
	Input impedance	$T_J = 25°C$		10^{10}			10^{10}		Ω
	Gain error	$T_J = 25°C$, $R_L = 10k$ Full temperature range		0.002	0.005 0.02		0.004	0.01 0.02	% %
	Feedthrough attenuation ratio at 1kHz	$T_J = 25°C$, $C_h = 0.01\mu F$	86	96		80	90		dB
	Output impedance	$T_J = 25°C$, "HOLD" mode Full temperature range		0.5	2 4		0.5	4 6	Ω Ω
	"HOLD" step[2]	$T_J = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
I_{CC}	Supply current[4]	$T_J \leq 25°C$		4.5	5.5		4.5	6.5	mA
	Logic and logic reference input current	$T_J = 25°C$		2	10		2	10	μA
	Leakage current into hold capacitor[4]	$T_J = 25°C$[3], "HOLD" mode		30	100		30	200	pA
t_{AC}	Acquisition time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$ $C_h = 0.01\mu F$		4 20			4 20		μs μs
	Hold capacitor charging current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
	Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		80	110		dB
	Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES:

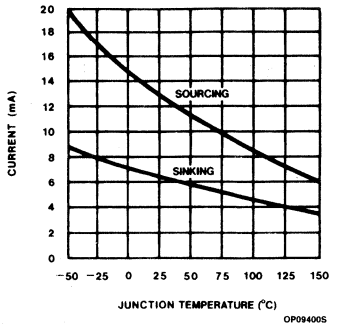
1. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_J = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.
2. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a $0.01\mu F$ hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
3. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
4. The parameters are guaranteed over a supply voltage of ±5 to ±18V.

TYPICAL DC PERFORMANCE CHARACTERISTICS

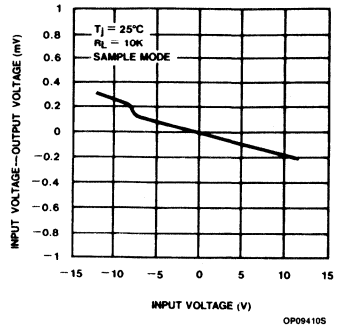
Input Bias Current



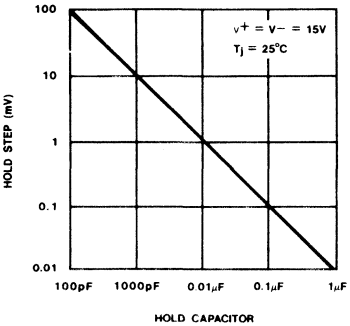
Output Short Circuit Current



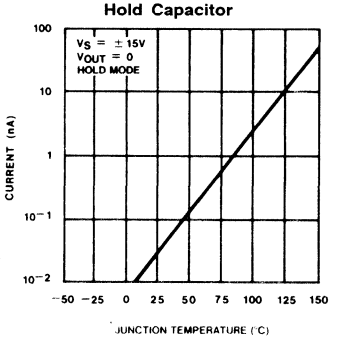
Gain Error



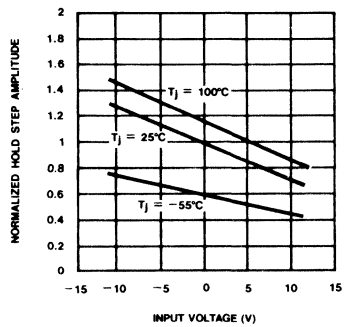
Hold Step



Leakage Current Into Hold Capacitor

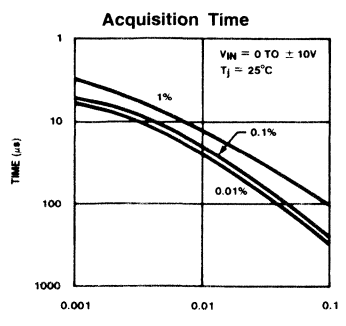


Hold Step Input Voltage

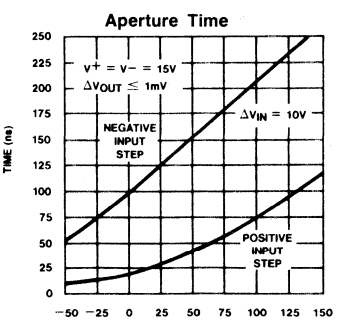


TYPICAL AC PERFORMANCE CHARACTERISTICS

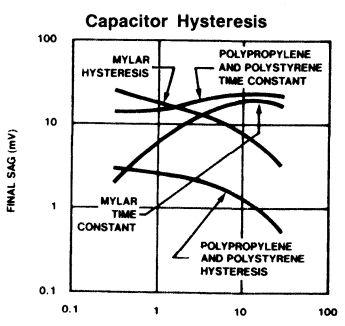
Acquisition Time



Aperture Time

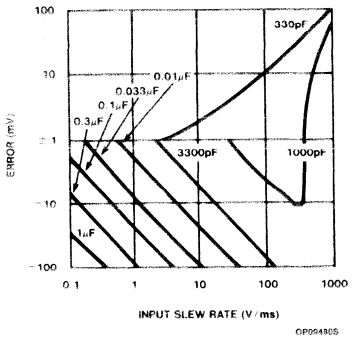


Capacitor Hysteresis



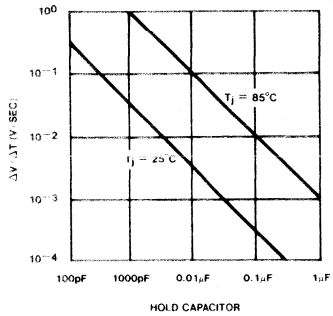
TYPICAL AC PERFORMANCE CHARACTERISTICS (Continued)

Dynamic Sampling Error



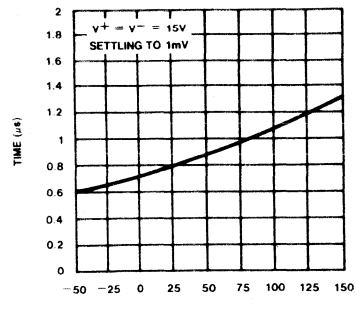
OP09480S

Output Droop Rate



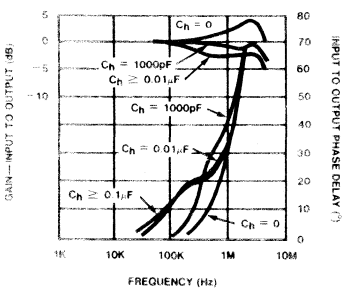
OP09490S

'Hold' Settling Time



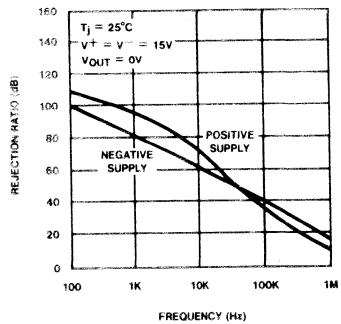
OP09500S

Phase And Gain (Input to Output, Small-Signal)



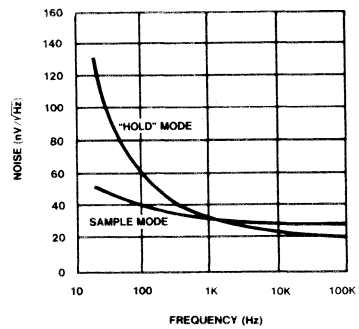
OP09510S

Power Supply Rejection



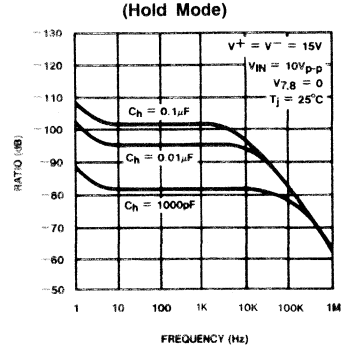
OP09520S

Output Noise



OP09530S

Feedthrough Rejection Ratio (Hold Mode)



OP09541S

NE/SE5060
Precision High-Speed Sample-and-Hold Amplifier

Preliminary Specification

DESCRIPTION

The NE/SE5060 is a high-performance, monolithic sample-and-hold amplifier that features high accuracy, low droop rate, and fast acquisition times required in high-speed data acquisition systems.

The circuit consists of two high impedance buffer amplifiers connected by an analog switch. In the sample mode, the device is in a non-inverting unity-gain configuration. The switch (S2) (see Block Diagram) is implemented as a unique switchable output stage of the input buffer which has been optimized for fast charging of the hold capacitor and a low sample-to-hold step size. In the hold mode, the input signal is effectively disconnected from the circuit by switch S1 to give a low feedthrough, and GM2 maintains 0V across the switch S2, ensuring a low droop rate. The device includes a 100pF hold capacitor. If lower droop rates and smaller sample-to-hold step error is desired at the expense of acquisition time, additional hold capacitance may be added externally. The voltage at the hold capacitor is buffered by the output buffer amplifier to drive the external load.

The device utilizes high voltage ion-implanted JFETs to obtain the low droop rates. The circuit has been designed to minimize the initial zero offset error, which is trimmed at the wafer level to be less than 0.5mV. The NE5060 operates from ±9V to ±17V power supplies with little or no change in the specification as long as the peak input voltage is not within 4V of the supplies.

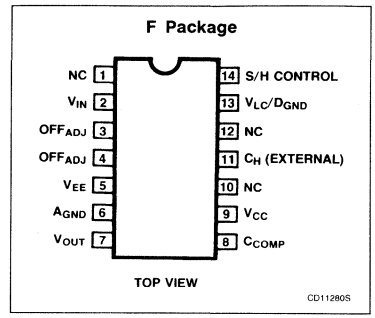
FEATURES

- **Voltage gain** **0.99970**
- **Low signal non-linearity** **0.0035%**
- **Low offset error** **0.5mV**
- **Fast acquisition time** **850ns**
- **Low sample-to-hold step** **1mV**
- **Low droop rate** **0.2μV/μs**
  +25°C (SE/NE5060) **0.2μV/μs**
  +70°C (NE5060) **2.0μV/μs**
  +125°C (SE5060) **150.0μV/μs**
- **Internal 100pF hold capacitor**
- **TTL CMOS Logic compatible**
- **Functional equivalent replacement for HA2420, HA2425, HA5320, AD583 and SMP11**

APPLICATIONS

- **Precision data acquisition systems**
- **D/A converter deglitching**
- **Auto-zero circuits**
- **Peak detectors**

PIN CONFIGURATION



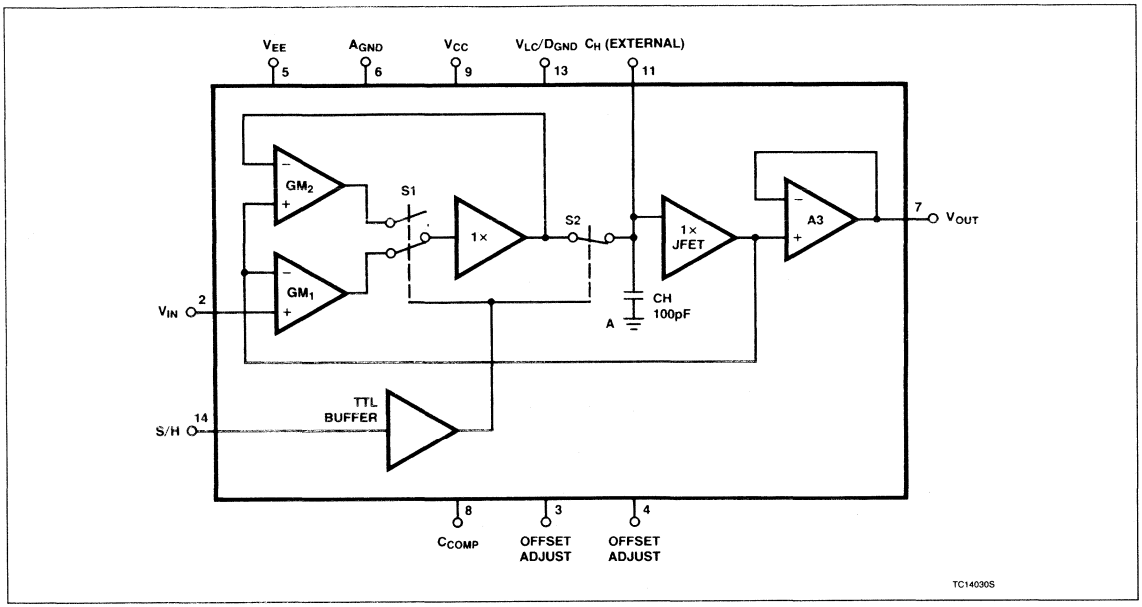
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Hermetic Cerdip	0 to +70°C	NE5060F
14-Pin Hermetic Cerdip	−55°C to +125°C	SE5060F

Precision High-Speed Sample-and-Hold Amplifier

NE/SE5060

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Voltage between V_{CC} and V_{EE}	36	V
V_{IN}	Analog input voltage	±15	V
$V_{S/H}$	Logic input voltage	±15	V
V_{LC}	Logic reference voltage	±15	V
I_{SC}	Output short-circuit duration	Indefinite	
	Hold capacitor short-circuit duration	60	s
P_D	Maximum power dissipation T_A = 25°C (still-air)[1]	1190	mW
T_A	Operating temperature range NE5060 SE5060S[2]	0 to +70 −55 to +125	°C °C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTES:

1. Derate above 25°C at 9.5mW/°C.
2. Operation above 110°C ambient requires that a heat sink be provided so as not to exceed the recommended maximum junction temperature of 150°C.
   θ_{JA} = 110°C/W
   θ_{JC} = 30°C/W
   $T_J = V_{CC} \times I_{CC} \times 0.8 \times \theta_{JA}$
   = 15 (15 + 14) × 0.8 × 110°C/W
   = 38.2°C

DC ELECTRICAL CHARACTERISTICS Test conditions, unless otherwise noted:
V_{CC} = 15V; V_{EE} = −15V; −10V ≤ V_{IN} ≤ 10V; V_{LC} = 0V; $V_{S/H}$ < 0.8V (for sample mode); $V_{S/H}$ > 2.0V (for hold mode); C_H = Internal; device in sample mode; 0°C ≤ T_A ≤ +70°C for NE5060; −55°C ≤ T_A ≤ +125°C for SE5060.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5060			SE5060			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{ZS}	Zero-scale error	V_{IN} = 0V; T_A = 25°C T_{MIN} to T_{MAX}		0.5 1.0	 2.0		0.5 3.0	 4.0	mV mV
I_{BIAS}	Input bias current	V_{IN} = 0V		70	150		70	250	nA
R_{IN}	Input resistance		150	250		100	250		MΩ
A_V	Voltage gain	V_{IN} = ±10V T_A = 25°C T_{MIN} to T_{MAX}	 0.99960 0.99950	 0.99975 0.99965		 0.99960 0.99930	 0.99975 0.99955		V/V V/V
E_L	Linearity error	V_{IN} = ±10V, R_L = 5kΩ		0.0035	0.007		0.0035	0.008	%
V_{INR}	Input voltage range		±10.5	±11		±10.5	±11		V
R_{OUT}	Output resistance			0.15	0.5		0.15	0.5	Ω
I_{LOAD}	Output load current (@ R_O < 0.5Ω)	V_{IN} = ±10V; T_A = 25°C T_{MIN} to T_{MAX}	±10 ±8	±15 ±11		±10 ±7	±15 ±11		mA mA
V_{IH}	Logic "1" voltage		2.0			2.0			V
V_{IL}	Logic "0" voltage				0.8			0.8	V
I_{IH}	Logic input current high	$V_{S/H}$ = 5V			0.1			0.1	μA
I_{IL}	Logic input current low	$V_{S/H}$ = 0V			−15			−15	μA
$E_{N\ RMS}$	Output noise	DC to 260kHz		250			250		μV
V_{CC}	Positive supply voltage[1]		13.5	15	16.5	13.5	15	16.5	V
V_{EE}	Negative supply[1]		−13.5	−15	−16.5	−13.5	−15	−16.5	V
I_{CC}	Positive supply current			11.5	15		11.5	15	mA
I_{EE}	Negative supply current			−11.5	−14		−11.5	−14	mA
PSRR+	Positive supply rejection ratio	V_{CC} = 15V ±5% V_{IN} = 0V V_{IN} = ±10V	 85 80	 100 90		 85 80	 100 90		dB dB dB
PSRR−	Negative supply rejection ratio	V_{EE} = −15V ±5% V_{IN} = 0V V_{IN} = ±10V	 65 57	 72 63		 65 57	 72 63		 dB dB

NOTE:
1. Recommend operating supply voltage range for V_{IN} = ±10V; DC specification production tested only at ±15V.

AC ELECTRICAL CHARACTERISTICS Test conditions, unless otherwise specified:
V_{CC} = 15V; V_{EE} = −15V; V_{IN} = 0V; V_{LC} = 0V; R_L = 2kΩ; C_L = 50pF; C_H = Internal;
$V_{S/H}$ = 0.4V (for sample mode); $V_{S/H}$ = 3.5V (for hold mode); T_A = +25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
SR	Slew rate[1]		16	20		V/μs
	Overshoot[1]			6		%
BW	Full power bandwidth	V_{IN} = 20V_{P-P}		260		kHz
t_{AQ}	Acquisition time,[1, 2]			850	1250	ns
t_{APD}	Aperture delay			30		ns
t_{AP}	Aperture time			25		ns
t_{APU}	Aperture uncertainty			1		ns
V_{HT}	Sample – Hold transient (peak to peak)[3]			2	15	mV
t_{HM}	Hold mode settling[2, 3]			35	125	ns
Q_t	Charge transfer[3]			0.1	0.25	pC
	Hold step[3, 4]			1.0	2.5	mV
dV_H/dt	Drop rate	T_A = +25°C 0°C to +70°C −55°C to +125°C		0.2 2 150	 5 200	μV/μs μV/μs μV/μs
I_D	Drop current	T_A = +25°C 0°C to +70°C −55°C to +125°C		2 100 10	 500 20	pA pA nA
	Hold mode feedthrough	V_{IN} = 10V_{P-P}; 100kHz		2		mV

NOTES:
1. V_{IN} = ±10V step.
2. To within 1.0mV of its final value (0.01%).
3. $V_{S/H\ (HIGH)}$ = 3.5V; t_R = 50ns (V_{IL} to V_{IH}).
4. Can be adjusted to zero.

Precision High-Speed Sample-and-Hold Amplifier

APPLYING THE NE/SE5060

The NE/SE5060 is a high-performance sample-and-hold amplifier. In the track mode the device behaves as a non-inverting unity gain amplifier. In the hold mode the device holds the value of the output voltage that was present at the instant the sample-to-hold signal goes high.

Hold Capacitor

The NE/SE5060 includes an on-chip hold capacitor and achieves fast acquisition, low hold step, and droop rate which are adequate for most high-speed applications. However, if a smaller hold step and lower droop rate are desired, then an external hold capacitor (C_H) may be added from Pin 11 to ground (Pin 6). The external hold capacitor should have high insulation resistance and low dielectric absorption to minimize droop errors.

If an external hold capacitor is used, then additional compensation capacitance of value $0.03C_H$ should be connected between Pin 8 and ground. Exact value and type are not critical. The additional hold capacitor will reduce the slew rate and increase acquisition time.

Offset Adjustment

The NE/SE5060 hold step error can be adjusted to zero using the offset adjustment pins as shown in the 'Typical Connections'. The error should be adjusted with the device in the hold mode, so that both the initial offset error and the hold-step error are nulled to zero. If desired, the center-tap of the offset adjustment potentiometer may be connected to V_{CC} through a 1MΩ resistor in series with the center-tap of the potentiometer.

Layout and Other Considerations

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01μF to 0.1μF ceramic) should be provided for each power supply terminal to Pin 6 as close to the device as possible.

The ideal ground connections are as follows:

- a wide trace between Pin 6 and Pin 13
- Pin 6 to each power supply ground
- a separate trace from Pin 6 to the signal ground
- Pin 13 to digital ground.

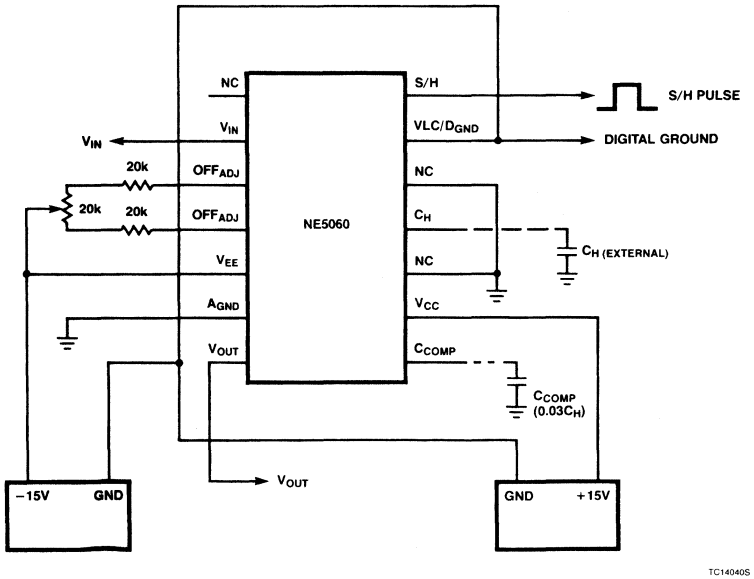
The hold capacitor (Pin 11) is sensitive to stray coupling. Any connection made to this pin should be kept short and guarded by a ground plane since nearby signal lines or power supply voltages will introduce errors in the hold mode.

In unity gain applications requiring no external hold capacitor, the NE/SE5060 can directly replace the HA2420, HA2425, and HA5320. In applications requiring an additional hold capacitor, it should be remembered that the capacitor should be connected from Pin 11 to ground.

Sample/Hold Input

Optimum performance is achieved with a clean (no ringing) sample-to-hold pulse with a rise time between 20ns and 50ns.

NE/SE5060 is compatible with all logic families. For TTL and DTL interface, simply ground Pin 13. The internal threshold voltage is set to 1.4V above the voltage at Pin 13. For CMOS and HTL interface, the appropriate voltage may be applied to Pin 13. For proper operation the voltage applied at Pin 13 must be at least 4V below the positive supply and 3V above the negative supply.



NOTE:
C_H and C_{COMP} required only if external hold capacitance is desired.

Figure 1. NE5060 Typical Connections

NE/SE5537
Sample-and-Hold Amplifier

Product Specification

DESCRIPTION

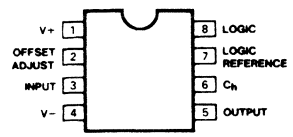
The NE5537 monolithic sample-and-hold amplifier combines the best features of ion-implanted JFETs with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin-compatible with the LF198, and features superior performance in droop rate and output drive capability. The circuit shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the sample mode. The first amplifier has bipolar input transistors which give the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2kΩ load. The logic input is compatible with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the sample mode occurring when the logic input is high. It is available in 8-lead TO-5, 8-pin plastic DIP packages, and 14-pin SO packages.

FEATURES

- **Operates from ±5V to ±18V supplies**
- **Hold leakage current 6pA @ $T_J = 25°C$**
- **Less than 4μs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at $C_H = 0.01\mu F$**
- **Low input offset: 1MV (typical)**
- **0.002% gain accuracy with $R_L = 2k\Omega$**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**

PIN CONFIGURATIONS

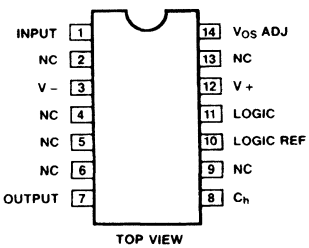
FE and N Packages



TOP VIEW

CD11611S

D[1] Package

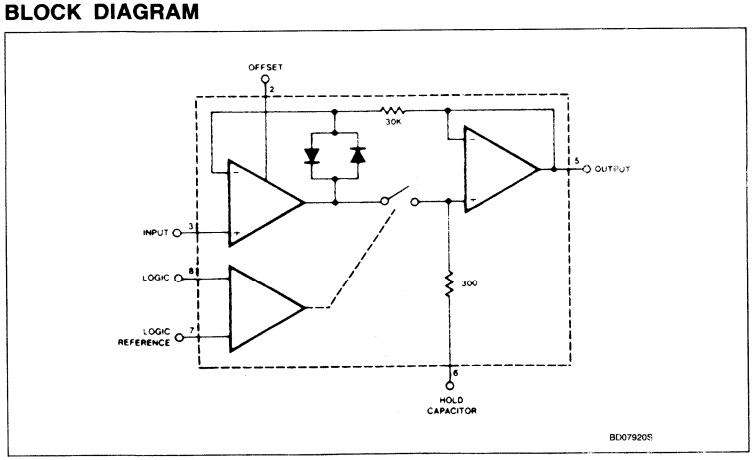


TOP VIEW

CD11631S

NOTE:
1. SO and non-standard pinouts.

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5537N
14-Pin Plastic SO	0 to +70°C	NE5537D
8-Pin Plastic DIP	−55°C to +125°C	SE5537FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Voltage supply	±18	V
P_D	Maximum power dissipation T_A = 25°C (still-air)[1] N package D package FE package	 1160 1090 780	 mW mW mW
T_A	Operating ambient temperature range SE5537 NE5537	 −55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
V_{IN}	Input voltage	Equal to supply voltage	
	Logic to logic reference differential voltage[2]	+7, −30	V
	Output short circuit duration	Indefinite	
	Hold capacitor short circuit duration	10	s
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 8.3mW/°C
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

DC ELECTRICAL CHARACTERISTICS[1]

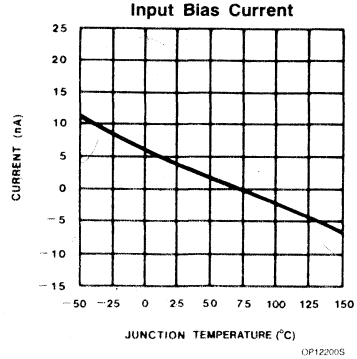
SYMBOL	PARAMETER	TEST CONDITIONS	SE5537			NE5537			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[4]	$T_J = 25°C$ Full temperature range		1	3 5		2	7 10	mV mV
I_{BIAS}	Input bias current[4]	$T_J = 25°C$ Full temperature range		5	25 75		10	50 100	nA nA
	Input impedance	$T_J = 25°C$		10^{10}			10^{10}		Ω
	Gain error	$T_J = 25°C$, $-10V \leq V_{IN} \leq 10V$, $R_L = 2k\Omega$ $-11.5V \leq V_{IN} \leq 11.5V$, $R_L = 10k\Omega$ Full temperature range		0.002	0.007 0.02		0.004	0.01 0.02	% %
	Feedthrough attenuation ratio at 1kHz	$T_J = 25°C$, $C_H = 0.01\mu F$	86	96		80	90		dB
	Output impedance	$T_J = 25°C$, "HOLD" mode Full temperature range		0.5	2 4		0.5	4 6	Ω
	"HOLD" Step[2]	$T_J = 25°C$, $C_H = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
I_{CC}	Supply current[4]	$T_J = 25°C$		4.5	6.5		4.5	7.5	mA
	Logic and logic reference input current	$T_J = 25°C$		2	10		2	10	μA
	Leakage current into hold capacitor[4]	$T_J = 25°C$ "hold" mode[3]		6	50		6	100	pA
	Acquisition time to 0.1%	$V_{OUT} = 10V$, $C_H = 1000pF$ $C_H = 0.01\mu F$		4 20			4 20		μs μs
	Hold capacitor charging current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
SVRR	Supply voltage rejection ratio	$V_{OUT} = 0V$	80	110		80	110		dB
	Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES:

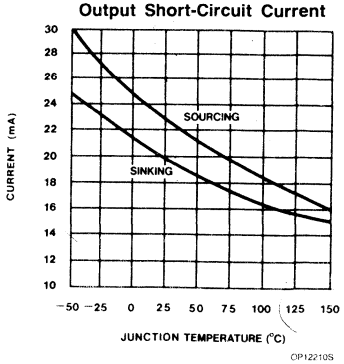
1. Unless otherwise specified, the following conditions apply: Unit is in "sample" mode. $V_S = \pm 15V$, $T_J = 25°C$, $-11.5V \leq V_{IN} \leq 11.5V$, $C_H = 0.01\mu F$, and $R_L = 2k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.
2. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01F hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
3. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
4. These parameters guaranteed over a supply voltage range of ±5 to ±18V.

TYPICAL PERFORMANCE CHARACTERISTICS

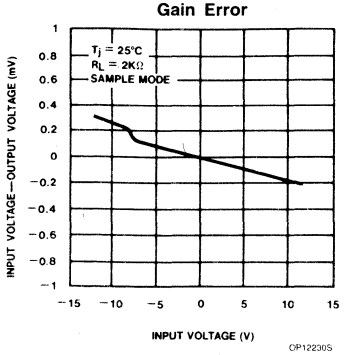
Input Bias Current



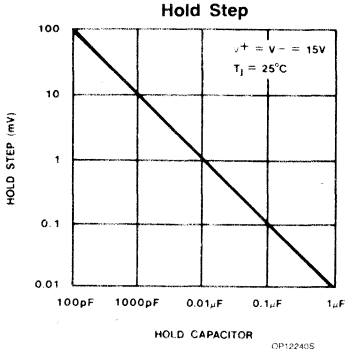
Output Short-Circuit Current



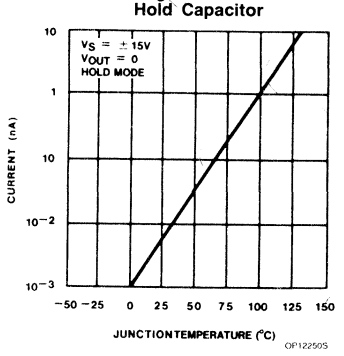
Gain Error



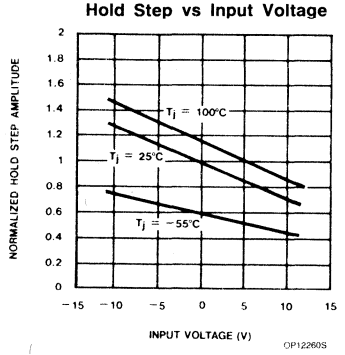
Hold Step



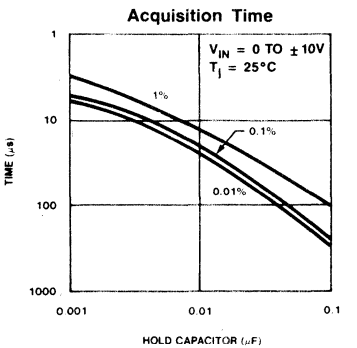
Leakage Current Into Hold Capacitor



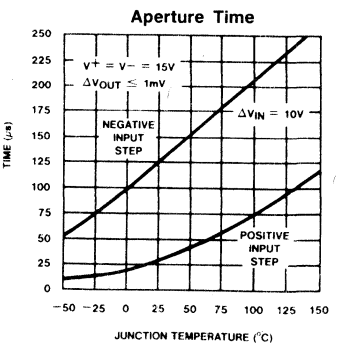
Hold Step vs Input Voltage



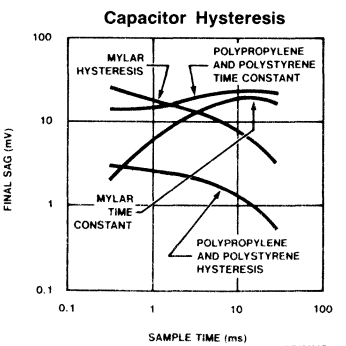
Acquisition Time



Aperture Time

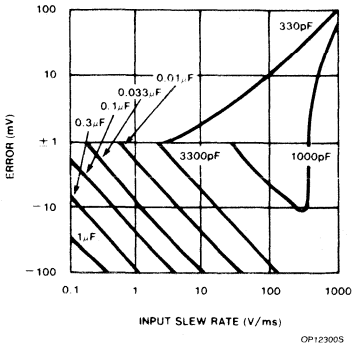


Capacitor Hysteresis



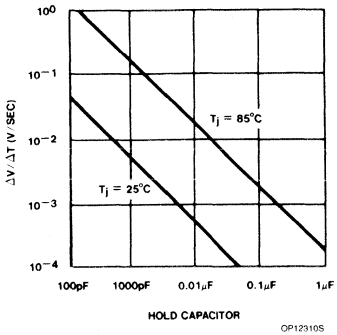
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Dynamic Sampling Error



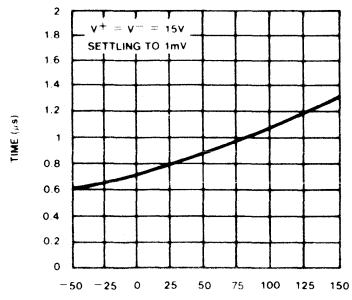
OP12300S

Output Droop Rate



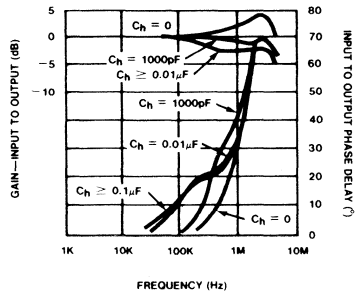
OP12310S

Hold Settling Time



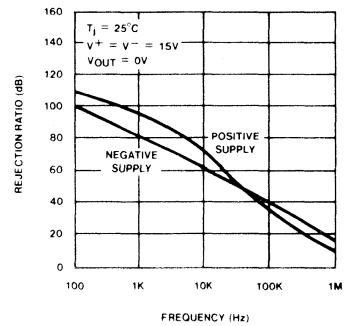
OP12320S

Phase and Gain (Input-to-Output, Small-Signal)



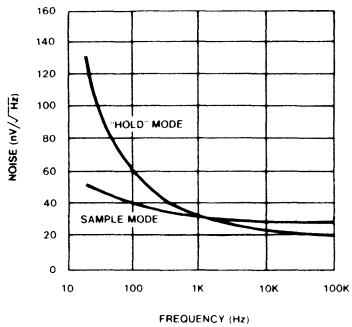
OP12330S

Power Supply Rejection



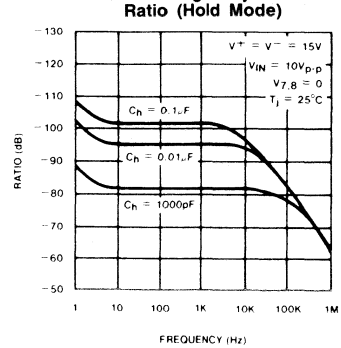
OP12340S

Output Noise



OP12350S

Feedthrough Rejection Ratio (Hold Mode)



OP12360S

SAMPLE-AND-HOLD

For many years designers have used the sample-and-hold (or track-and-hold) to operate on analog information in a time frame which is expedient.

By sampling a segment of the information and holding it until the proper timing for converting to some form of control signal or readout, the designer maintains certain freedom in performing predetermined manipulative functions. Therefore, the sample-and-hold can be defined as a "selective analog memory cell".

The memory is volatile and will also decay with time.

When using the sample-and-hold method for evaluating signal information, the designer is given the added feature of eliminating outside noise elements. With the analog-to-digital converter products available today, the "DC memory" of the sample-and-hold can be easily converted to digital format and further incorporated into microprocessor-based systems.

Parametric evaluation of the sample-and-hold will be discussed in the following paragraphs.

DEFINITION OF TERMS

Acquisition Time —
The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Delay Time —
The time elapsed from the hold command to the opening of the switch.

Aperture Jitter —
Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

Aperture Time —
The delay required between "HOLD" command and an input analog transition, so that the transition does not affect the held output.

Bandwidth —
The frequency at which the gain is down 3dB from its DC value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

Dynamic Sampling Error —
The error introduced into the hold output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Effective Aperture Delay —
The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure of Merit —
The ratio of the available charging current during sample mode to the leakage current during hold mode.

Gain Error —
The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Mode Droop —
The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

Hold Mode Feedthrough —
The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

Hold Settling Time —
The time required for the output to settle within 1mV of final value after the "HOLD" logic command.

Hold Step —
The voltage step at the output of the sample-and-hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is 5V.

Sample-to-Hold Offset Error —
The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

Slew Rate —
The fastest rate at which the sample-and-hold output can change (specified in V/μs).

Threshold Level —
That level which causes the switch control to change state.

BASIC BLOCK DIAGRAM

The basic circuit concept of the sample-and-hold circuit incorporates the use of two (2) operational amplifiers and a switch control mechanism (which determines sample, hold or track conditions).

The block diagram of the NE5537 is a closed loop, non-inverting unity gain sample-and-hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop so that the output voltage is identical to the input voltage (with consideration for input offset voltage, offset current, and temperature variations which are common to all sample-and-hold circuits, be they monolithic, hybrid or modular).

When the sampling switch is open (in the hold mode), the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels via a timing sequence remote from the sample-and-hold device (See Figure 1). The switch control has a floating reference (Pin 7), referred to as the logic reference which makes the sample-and-hold device compatible to several types of external logic signals (TTL, PMOS, and CMOS). The switching device operates at a threshold level of 1.4V.

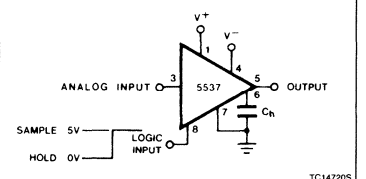


Figure 1. Typical Connection

The switch mechanism is on (sampling an information stream) when the logic level is high (Pin 8 is 1.4V higher than Pin 7) and presents a load of 5μA to the input logic signal. The analog sampled signal is amplified, stored (in the external holding capacitor), and buffered. At the end of the sampling period, the internal switch mechanism turns off (switch opens) and the "stored analog memory" information on the external capacitor (Pin 6) is loaded down by an operational amplifier connected in the unity gain non-inverting configuration. This input impedance of this amplifier is effectively:

$$R = R_{IN}(A_{OL})/(1 + 1/A)$$

where
- R = Effective input impedance
- R_{IN} = Open-loop input impedance
- A_{OL} = Open-loop gain
- A = AC loop gain

Therefore, the higher the open-loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the "leakage" current and the better the droop characteristics.

In actuality, the amplifiers are designed with special leakage current cancellation circuits along with FET input devices. The leakage current cancellation circuits give better high temperature operation. (Remember that the FET amplifiers double in required bias current

for every 10 degree increase in junction temperature.)

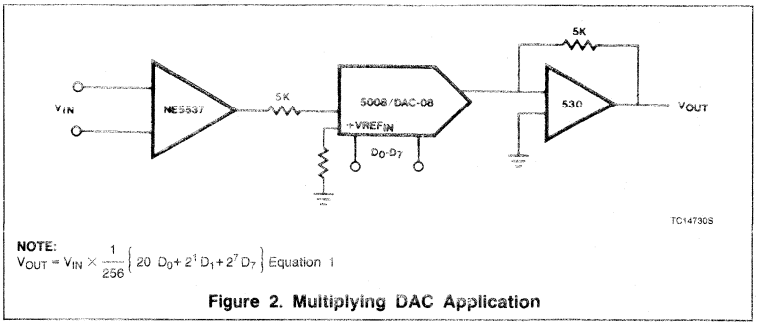
Sampling time for the NE5537 is less than 10μs (measured to 0.1% of input signal). Leakage current is 6pA at a rate output load of 2kΩ.

BASIC APPLICATIONS

Multiplying DAC

As depicted in the block diagram of Figure 2, the sample-and-hold circuit is used to supply a "variable" reference to the digital-to-analog converter. As the input reference varies, the output will change in accordance with Equation 1, shown in Figure 2.

Varying the input signal reference level can aid the system in performing both compression and expansion operations. The multiplying DACs used are the Signetics NE/SE5008; however, if the rate of change of the reference variation is kept slow enough, a microprocessor-compatible DAC can be incorporated, such as the NE5018 or the NE5020.



NOTE:
$V_{OUT} = V_{IN} \times \frac{1}{256} \{ 20\ D_0 + 2^1 D_1 + 2^7 D_7 \}$ Equation 1

Figure 2. Multiplying DAC Application

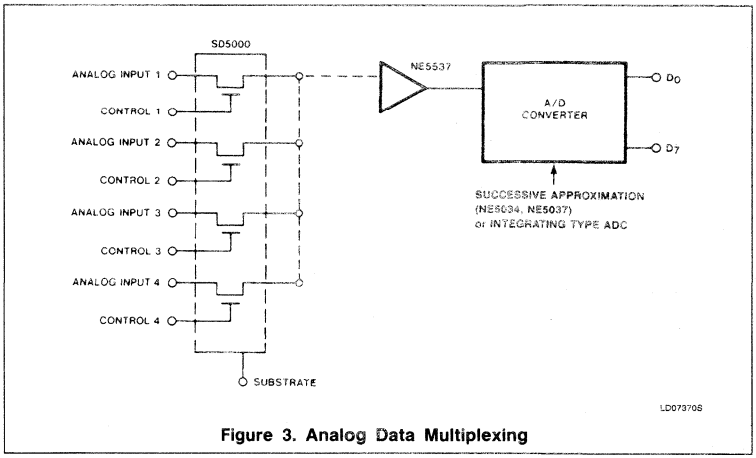


Figure 3. Analog Data Multiplexing

DATA ACQUISITION SYSTEMS

As mentioned earlier, the designer may wish to operate on several different segments of an "analog" signal; however, he is limited by the fact that only one analog-to-digital converter channel is available to him. Figure 3 shows the means by which a multiplexing system may be accomplished.

APPLICATION HINTS

Hold Capacitor

A significant source of error in an accurate sample-and-hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back in the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with > 1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. The hysteresis relaxation time constant in polystyrene, for instance, is 10 – 50ms. If A-to-D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

DC ZEROING

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1kΩ potentiometer which has one end tied to V+ and the other end tied through a resistor to ground. The resistor should be selected to give ≃0.6mA through the 1kΩ potentiometer.

Sampling Dynamic Signals

Sampling errors due to moving (changing) input signals are of significant concern to designers employing sample-and-hold circuits. There exist finite phase delays through the sample-and-hold circuit causing an input-output phase of differential for moving signals. In addition, the series protection resistor (300Ω to Pin 6 of the NE5537) will add an RC time constant, over and above the slew rate limitation of the input buffer/current drive amplifier. This means that at the moment the "HOLD" command arrives, the hold capacitor voltage may be somewhat different from the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 V_{P-P} at 10kHz. Maximum dV/dt is 0.6V/μs. With no analog phase delay and 100ns logic delay, one could expect up to (0.1μs) (0.6V/μs) = 60mV error if the "HOLD" signal arrived near maximum dV/dt of the input. A positive-going input would give a ±60mV error. Now assume a 1MHz (3dB) bandwidth for the overall analog loop. This generates a phase delay of 160ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs) (0.6V/μs) = –96mV (analog) for a total of –36mV. To add to the confusion, analog delay is proportional to hold capacitor value, while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled "Aperture Time" has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "HOLD" command. This curve is based on a 1mV error fed into the output.

A second curve, "Hold Settling Time," indicates the time required for the output to settle to 1mV after the "HOLD" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Logic signals also couple to the hold capacitor. This hold capacitor should be guarded by a PC card trace connected to the sample-and-hold output. This will also minimize board leakage.

SPECIAL NOTES

1. Not all definitions herein defined are measured parametrically for the NE5537, but are legitimate terms used in sample-and-hold systems.
2. Reference should be made to *Design Engineering*, Volumes 23 (Nov. 8, 1978), 25 (Dec. 6, 1978) and 26 (Dec. 20, 1978) for articles written by Eugene Zuch of Datel Systems, Inc., for a further discussion of sample-and-hold circuits.
3. Reference also made to National Semiconductor Corporation's Special Functions Data Book (1976).

ADCs

		page
ADC0803-1	8-bit ADC (CMOS)	413
ADC0804-1	8-bit ADC (CMOS)	413
ADC0805-1	8-bit ADC (CMOS)	413
ADC0820	8-bit CMOS ADC with track/hold	426
NE5034	8-bit high-speed ADC	439
NE5036	6-bit ADC (serial output)	446
NE5037	6-bit ADC (parallel outputs)	453
AN1311	low cost A/D conversion using the NE5044	*

* See Motor control section.

ADC0803/4/5-1
CMOS 8-Bit A/D Converters

Product Specification

DESCRIPTION

The ADC0803 family is a series of three CMOS 8-bit successive approximation A/D converters using a resistive ladder and capacitive array together with an auto-zero comparator. These converters are designed to operate with microprocessor-controlled buses using a minimum of external circuitry. The 3-State output data lines can be connected directly to the data bus.

The differential analog voltage input allows for increased common-mode rejection and provides a means to adjust the zero-scale offset. Additionally, the voltage reference input provides a means of encoding small analog voltages to the full 8 bits of resolution.

FEATURES

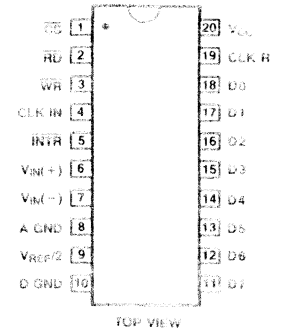
- **Compatible with most microprocessors**
- **Differential inputs**
- **3-State outputs**
- **Logic levels TTL and MOS compatible**
- **Can be used with internal or external clock**
- **Analog input range 0V to V_{CC}**
- **Single 5V supply**
- **Guaranteed specification with 1MHz clock**

APPLICATIONS

- **Transducer-to-microprocessor interface**
- **Digital thermometer**
- **Digitally-controlled thermostat**
- **Microprocessor-based monitoring and control systems**

PIN CONFIGURATION

D[1], N Packages

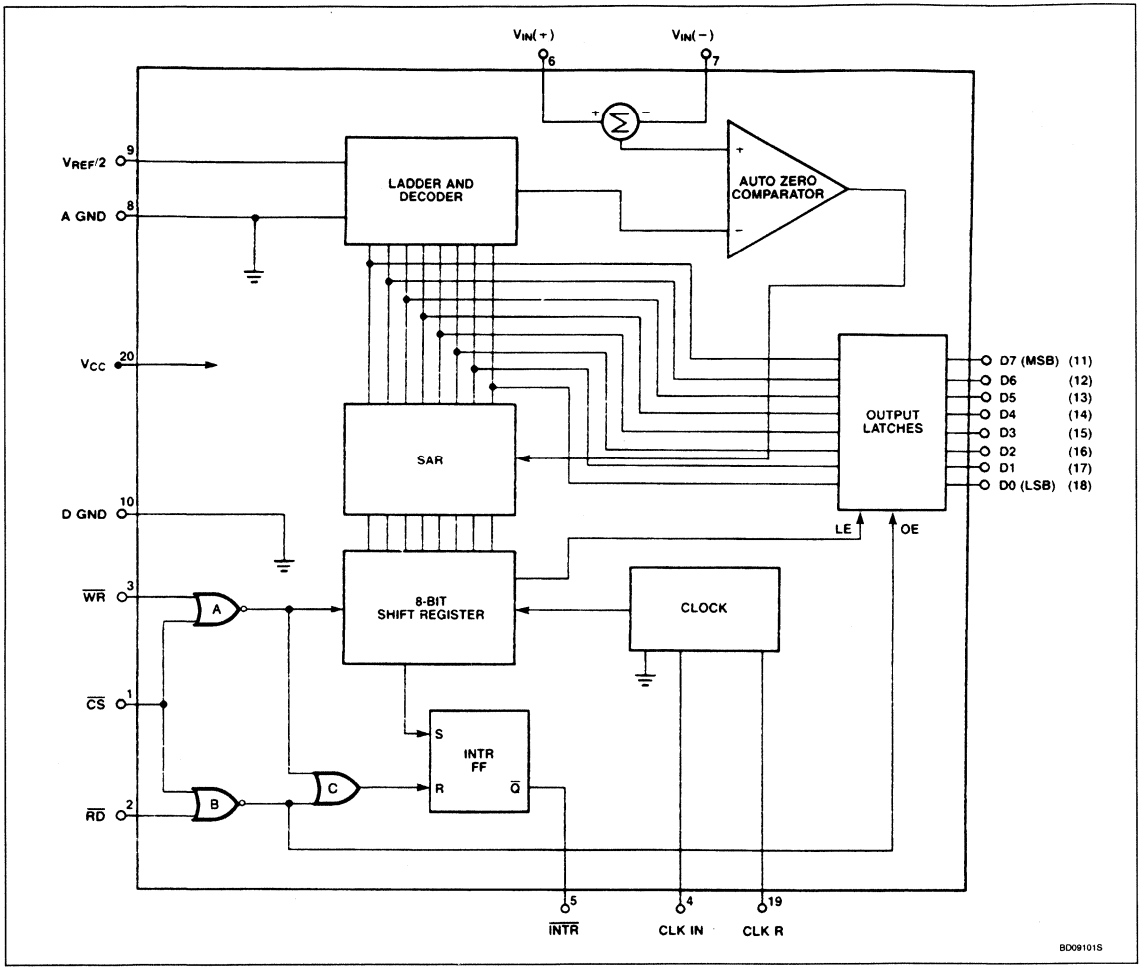


NOTE:
SOL — Released in large SO package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	−40°C to +85°C	ADC0803/04/05-1 LCN
20-Pin Plastic DIP	0 to 70°C	ADC0804-1 CN
20-Pin Plastic SO	0 to 70°C	ADC0803/04-1 CD
20-Pin Plastic SO	−40°C to 85°C	ADC0803/04-1 LCD

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	6.5	V
	Logic control input voltages	−0.3 to +16	V
	All other input voltages	−0.3 to (V_{CC} +0.3)	V
T_A	Operating temperature range ADC0803/04-1 LCD	−40 to +85	°C
	ADC0803/04/05-1 LCN	−40 to +85	°C
	ADC0803/04-1 CD	0 to +70	°C
	ADC0804-1 CN	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Maximum power dissipation T_A = 25°C (still air)[1] N package D package	 1690 1390	 mW mW

NOTE:
1. Derate above 25°C, at the following rates:
   N package at 13.5mW/°C
   D package at 11.1mW/°C

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V, f_{CLK} = 1MHz, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	ADC0803/4/5			UNIT
			Min	Typ	Max	
	ADC0803 Relative accuracy error (adjusted)	Full-Scale adjusted			0.50	LSB
	ADC0804 Relative accuracy error (unadjusted)	$\frac{V_{REF}}{2}$ = 2.500V_{DC}			1	LSB
	ADC0805 Relative accuracy error (unadjusted)	$\frac{V_{REF}}{2}$ = has no connection			1	LSB
R_{IN}	$\frac{V_{REF}}{2}$ Input resistance	V_{CC} = 0V[2]	400	680		Ω
	Analog input voltage range		−0.05		V_{CC} +0.05	V
	DC common-mode error	Over analog input voltage range		1/16	1/8	LSB
	Power supply sensitivity	V_{CC} = 5V ± 10%[1]		1/16		LSB
Control inputs						
V_{IH}	Logical "1" input voltage	V_{CC} = 5.25V_{DC}	2.0		15	V_{DC}
V_{IL}	Logical "0" input voltage	V_{CC} = 4.75V_{DC}			0.8	V_{DC}
I_{IH}	Logical "1" input current	V_{IN} = 5V_{DC}		0.005	1	μA_{DC}
I_{IL}	Logical "0" input current	V_{IN} = 0V_{DC}	−1	−0.005		μA_{DC}

DC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 5.0V, f_{CLK} = 1MHz, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	ADC0803/4/5			UNIT
			Min	Typ	Max	
Clock in and clock R						
V_{T+}	Clock in positive-going threshold voltage		2.7	3.1	3.5	V_{DC}
V_{T-}	Clock in negative-going threshold voltage		1.15	1.8	2.1	V_{DC}
V_H	Clock in hysteresis $(V_{T+}) - (V_{T-})$		0.6	1.3	2.0	V_{DC}
V_{OL}	Logical "0" clock R output voltage	I_{OL} = 360μA, V_{CC} = 4.75V_{DC}			0.4	V_{DC}
V_{OH}	Logical "1" clock R output voltage	I_{OH} = −360μA, V_{CC} = 4.75V_{DC}	2.4			V_{DC}
Data output and $\overline{INTR}$						
V_{OL}	Logical "0" output voltage					
	Data outputs	I_{OL} = 1.6mA, V_{CC} = 4.75V_{DC}			0.4	V_{DC}
	$\overline{INTR}$ outputs	I_{OL} = 1.0mA, V_{CC} = 4.75V_{DC}			0.4	V_{DC}
V_{OH}	Logical "1" output voltage	I_{OH} = −360μA, V_{CC} = 4.75V_{DC}	2.4			V_{DC}
		I_{OH} = −10μA, V_{CC} = 4.75V_{DC}	4.5			V_{DC}
I_{OZL}	3-State output leakage	V_{OUT} = 0V_{DC}, $\overline{CS}$ = Logical "1"	−3			μA_{DC}
I_{OZH}	3-State output leakage	V_{OUT} = 5V_{DC}, $\overline{CS}$ = Logical "1"			3	μA_{DC}
I_{SC}	+ Output short-circuit current	V_{OUT} = 0V, T_A = 25°C	4.5	12		mA_{DC}
I_{SC}	− Output short-circuit current	V_{OUT} = V_{CC}, T_A = 25°C	9.0	30		mA_{DC}
I_{CC}	Power supply current	f_{CLK} = 1MHz, $V_{REF/2}$ = Open, $\overline{CS}$ = Logical "1", T_A = 25°C		3.0	3.5	mA

NOTES:
1. Analog inputs must remain within the range: $-0.05 \leq V_{IN} \leq V_{CC} + 0.05V$.
2. See typical performace characteristics for input resistance at V_{CC} = 5V.

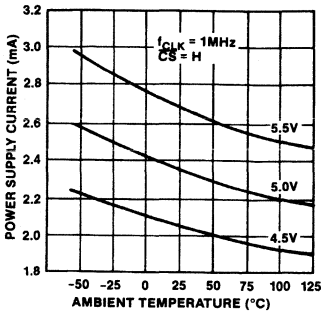
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	ADC0803/4/5			UNIT
					Min	Typ	Max	
	Conversion time			f_{CLK} = 1MHz[1]	66		73	μs
f_{CLK}	Clock frequency[1]				0.1	1.0	3.0	MHz
	Clock duty cycle[1]				40		60	%
CR	Free-running conversion rate			$\overline{CS}$ = 0, f_{CLK} = 1MHz $\overline{INTR}$ tied to $\overline{WR}$			13690	conv/s
$t_{W(\overline{WR})L}$	Start pulse width			$\overline{CS}$ = 0	30			ns
t_{ACC}	Access time	Output	$\overline{RD}$	$\overline{CS}$ = 0, C_L = 100pF		75	100	ns
t_{1H}, t_{0H}	3-State control	Output	$\overline{RD}$	CL = 10pF, R_L = 10kΩ See 3-State test circuit		70	100	ns
t_{W1}, t_{R1}	$\overline{INTR}$ delay	$\overline{INTR}$	$\overline{WD}$ or $\overline{RD}$			100	150	ns
C_{IN}	Logic input = capacitance					5	7.5	pF
C_{OUT}	3-State output capacitance					5	7.5	pF

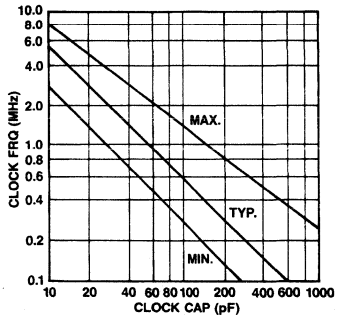
NOTE:
1. Accuracy is guaranteed at f_{CLK} = 1MHz. Accuracy may degrade at higher clock frequencies.

TYPICAL PERFORMANCE CHARACTERISTICS

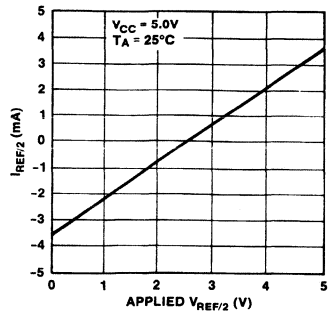
Power Supply Current vs Temperature



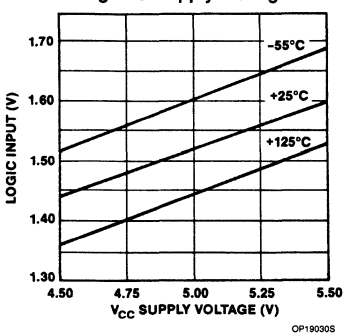
Clock Frequency vs Clock Capacitor



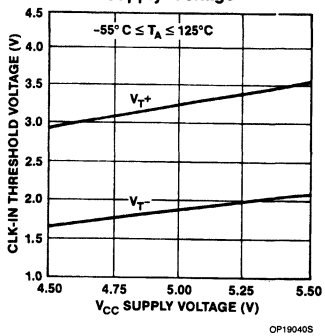
Input Current vs Applied Voltage at $V_{REF/2}$ Pin



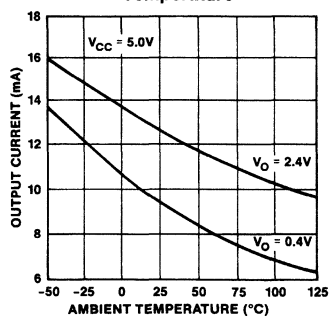
Logic Input Threshold Voltage vs Supply Voltage



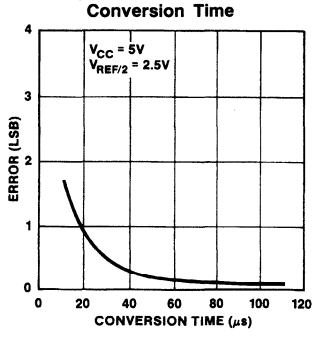
CLK-IN Threshold Voltage vs Supply Voltage



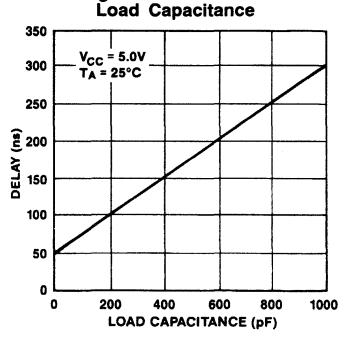
Output Current vs Temperature



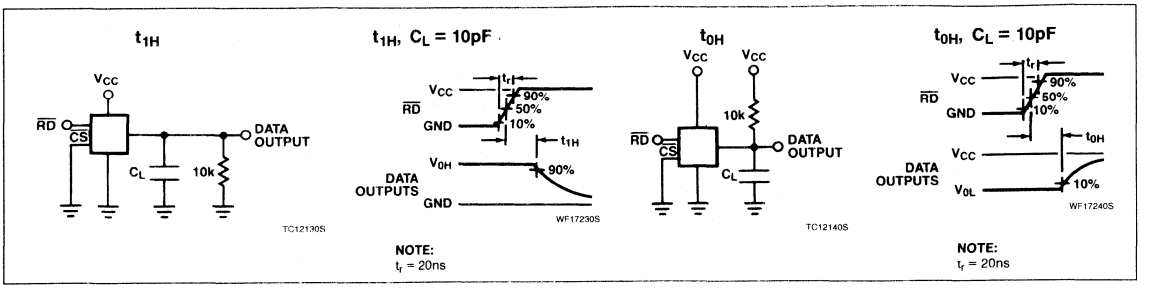
Full Scale Error vs Conversion Time



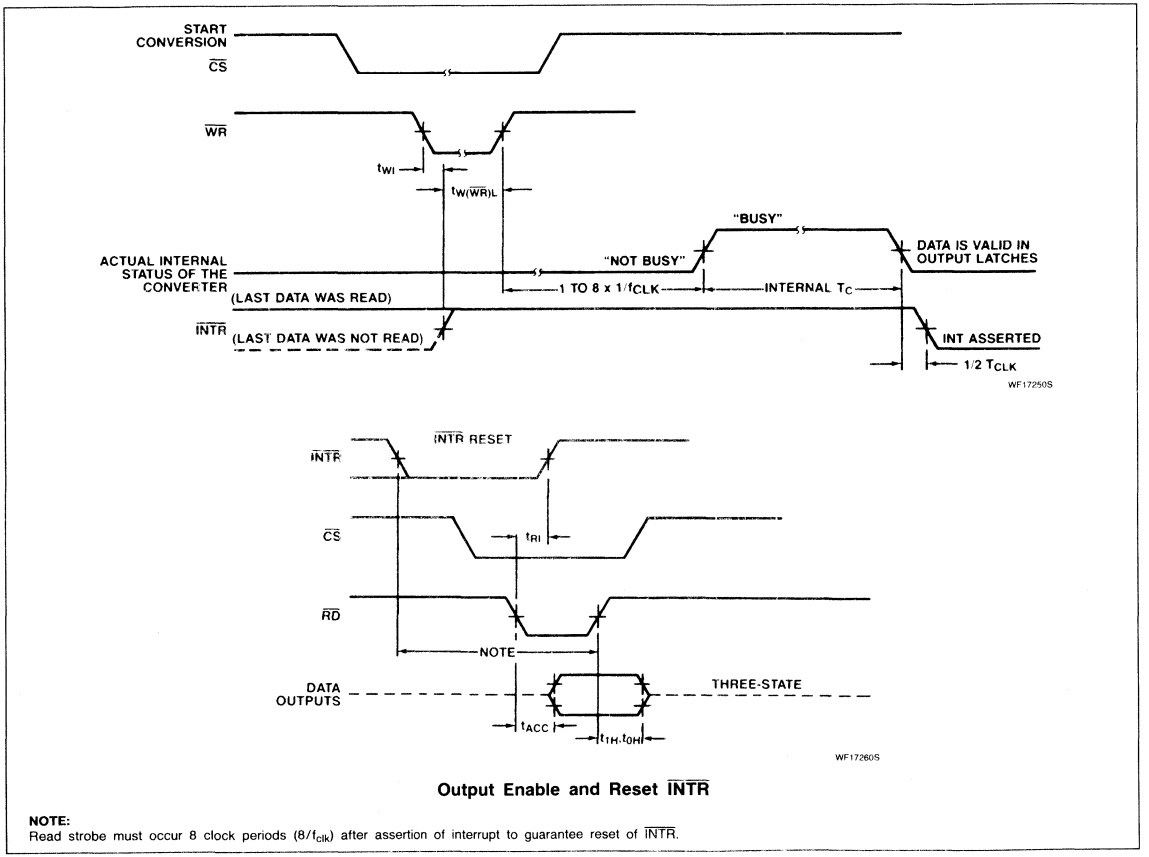
Delay From $\overline{RD}$ Falling Edge to Data Valid vs Load Capacitance



3-STATE TEST CIRCUITS AND WAVEFORMS (ADC0801-1)



TIMING DIAGRAMS (All timing is measured from the 50% voltage points)



Output Enable and Reset INTR

NOTE:
Read strobe must occur 8 clock periods ($8/f_{clk}$) after assertion of interrupt to guarantee reset of INTR.

FUNCTIONAL DESCRIPTION

These devices operate on the Successive Approximation principle. Analog switches are closed sequentially by successive approximation logic until the input to the auto-zero comparator [$V_{IN(+)} - V_{IN(-)}$] matches the voltage from the decoder. After all bits are tested and determined, the 8-bit binary code corresponding to the input voltage is transferred to an output latch. Conversion begins with the arrival of a pulse at the $\overline{WR}$ input if the CS input is low. On the High-to-Low transition of the signal at the WR or the CS input, the SAR is initialized, the shift register is reset, and the $\overline{INTR}$ output is set high. The A/D will remain in the reset state as long as the $\overline{CS}$ and $\overline{WR}$ inputs remain low. Conversion will start from one to eight clock periods after one or both of these inputs makes a Low-to-High transition. After the conversion is complete, the $\overline{INTR}$ pin will make a High-to-Low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion result. A read ($\overline{RD}$) operation (with $\overline{CS}$ low) will clear the $\overline{INTR}$ line and enable the output latches. The device may be run in the free-running mode as described later. A conversion in progress can be interrupted by issuing another start command.

Digital Control Inputs

The digital control inputs (CS, WR, $\overline{RD}$) are compatible with standard TTL logic voltage levels. The required signals at these inputs correspond to Chip Select, START Conversion, and Output Enable control signals, respectively. They are active-Low for easy interface to microprocessor and microcontroller control buses. For applications not using microprocessors, the $\overline{CS}$ input (Pin 1) can be grounded and the A/D START function is achieved by a negative-going pulse to the $\overline{WR}$ input (Pin 3). The Output Enable function is achieved by a logic low signal at the $\overline{RD}$ input (Pin 2), which may be grounded to constantly have the latest conversion present at the output.

ANALOG OPERATION

Analog Input Current

The analog comparisons are performed by a capacitive charge summing circuit. The input capacitor is switched between $V_{IN(+)}$4 and $V_{IN(-)}$, while reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the most recent total value set by the successive approximation register.

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These transient currents occur at the leading edge of the internal clock pulses. They decay rapidly so do not inherently cause errors as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors and Source Resistance

Bypass capacitors at the input will average the charges mentioned above, causing a DC and an AC current to flow through the output resistance of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input at full scale. This current can be a few microamps, so bypass capacitors should NOT be used at the analog inputs of the $V_{REF}/2$ input for high resistance sources (> 1kΩ). If input bypass capacitors are desired for noise filtering and a high source resistance is desired to minimize capacitor size, detrimental effects of the voltage drop across the input resistance can be eliminated by adjusting the full scale with both the input resistance and the input bypass capacitor in place. This is possible because the magnitude of the input current is a precise linear function of the differential voltage.

Large values of source resistance where an input bypass capacitor is not used will not cause errors as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (< 1kΩ) for a passive RC section or add an op amp active filter (low pass). For applications with source resistances at or below 1kΩ, a 0.1μF bypass capacitor at the inputs will prevent pickup due to series lead inductance or a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the resistor and capacitor should be placed out of the feedback loop) from the output of the op amp, if used.

Analog Differential Voltage Inputs and Common-Mode Rejection

These A/D converters have additional flexibility due to the analog differential voltage input. The $V_{IN(-)}$ input (Pin 7) can be used to subtract a fixed voltage from the input reading (tare correction). This is also useful in a 4/20mA current loop conversion. Common-mode noise can also be reduced by the use of the differential input.

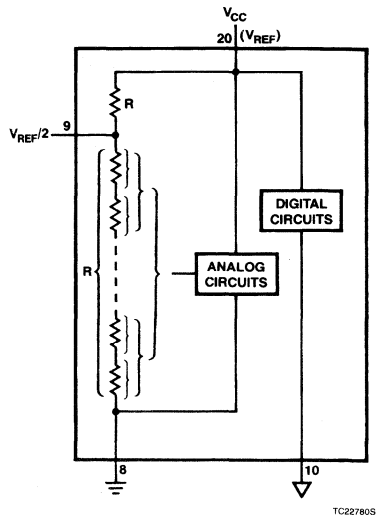
The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is 4.5 clock periods. The maximum error due to this time difference is given by:

$$V(max) = (V_P)(2f_{CM})(4.5/f_{CLK}),$$

where:

V = error voltage due to sampling delay
V_P = peak value of common-mode voltage
f_{CM} = common mode frequency

For example, with a 60Hz common-mode frequency, f_{cm}, and a 1MHz A/D clock, F_{CLK}, keeping this error to 1/4 LSB (about 5mV)



NOTE:
The $V_{REF}/2$ voltage is either ½ the V_{CC} voltage or is that which is forced at Pin 9.

Figure 1. Internal Reference Design

would allow a common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\,V(max)\,(f_{CLK})\,]}{(2f_{CM})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})\,(10^4)}{(6.28)\,(60)\,(4.5)} = 2.95V$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode voltage levels than this, however.

An analog input span less than the full 5V capability of the device, together with a relatively large zero offset, can be easily handled by use of the differential input. (See Reference Voltage Span Adjust).

Noise and Stray Pickup

The leads of the analog inputs (Pins 6 and 7) should be kept as short as possible to minimize input noise coupling and stray signal pick-up. Both EMI and undesired digital signal coupling to these inputs can cause system errors. The source resistance for these inputs should generally be below 5kΩ to help avoid undesired noise pickup. Input bypass capacitors at the analog inputs can create errors as described previously. Full scale adjustment with any input bypass capacitors in place will eliminate these errors.

Reference Voltage

For application flexibility, these A/D converters have been designed to accommodate fixed reference voltages of 5V to Pin 20 or 2.5V to Pin 9, or an adjusted reference voltage at Pin 9. The reference can be set by forcing it at $V_{REF}/2$ input, or can be determined by the supply voltage (Pin 20). Figure 1 indicates how this is accomplished.

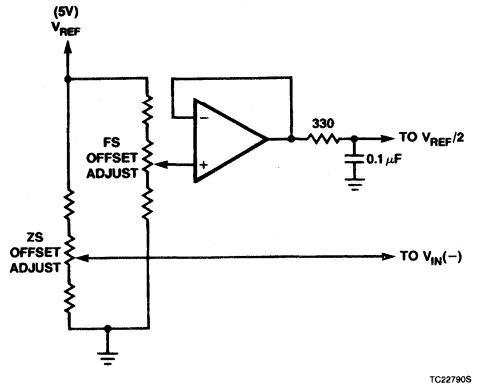


Figure 2. Offsetting the Zero Scale and Adjusting the Input Range (Span)

Reference Voltage Span Adjust

Note that the Pin 9 ($V_{REF}/2$) voltage is either 1/2 the voltage applied to the V_{CC} supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. In addition to allowing for flexible references and full span voltages, this also allows for a ratiometric voltage reference. The internal gain of the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at Pin 9.

For example, a dynamic voltage range of the analog input voltage that extends from 0 to 4V gives a span of 4V (4 – 0), so the $V_{REF}/2$ voltage can be made equal to 2V (half of the 4V span) and full scale output would correspond to 4V at the input.

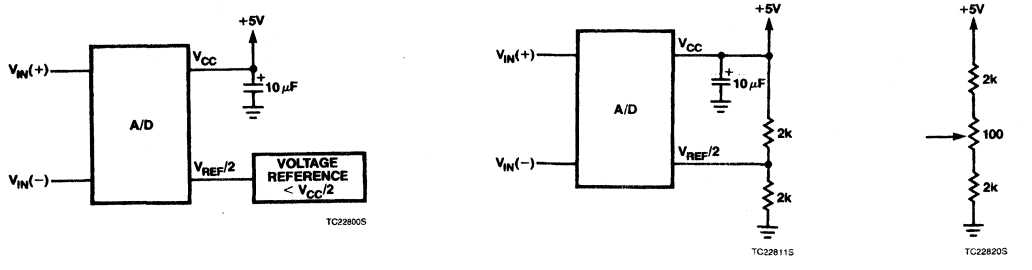
On the other hand, if the dynamic input voltage had a range of 0.5 to 3.5V, the span or dynamic input range is 3V (3.5 – 0.5). To encode this 3V span with 0.5V yielding a code of zero, the minimum expected input (0.5V, in this case) is applied to the $V_{IN}(-)$ pin to account for the offset, and the $V_{REF}/2$ pin is set to 1/2 the 3V span, or 1.5V. The A/D converter will now encode the $V_{IN}(+)$ signal between 0.5 and 3.5V with 0.5V at the input corresponding to a code of zero and 3.5V at the input producing a full scale output code. The full 8 bits of resolution are thus applied over this reduced input voltage range. The required connections are shown in Figure 2.

Operating Mode

These converters can be operated in two modes:

1) absolute mode
2) ratiometric mode

In absolute mode applications, both the initial accuracy and the temperature stability of the reference voltage are important factors in the accuracy of the conversion. For $V_{REF}/2$ voltages of 2.5V, initial errors of ±10mV will cause conversion errors of ± 1 LSB due to the gain of 2 at the $V_{REF}/2$ input. In reduced span applications, the initial value and stability of the $V_{REF}/2$ input voltage become even more important as the same error is a larger



a. Fixed Reference **b. Fixed Reference Derived from V_{CC}** **c. Optional Full Scale Adjustment**

Figure 3. Absolute Mode of Operation

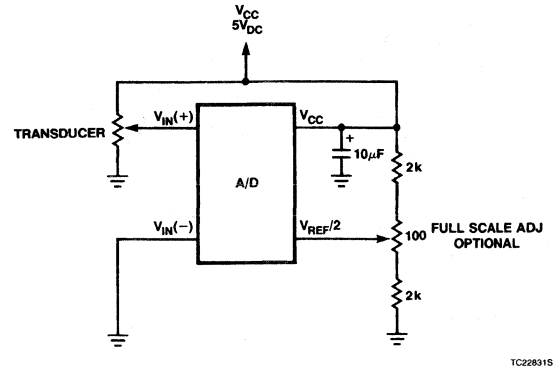


Figure 4. Ratiometric Mode of Operation with Optional Full Scale Adjustment

percentage of the $V_{REF}/2$ nominal value. See Figure 3.

In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter, and, therefore, cancels out in the final digital code. See Figure 4.

Generally, the reference voltage will require an initial adjustment. Errors due to an improper reference voltage value appear as full-scale errors in the A/D transfer function.

ERRORS AND INPUT SPAN ADJUSTMENTS

There are many sources of error in any data converter, some of which can be adjusted out. Inherent errors, such as relative accuracy, cannot be eliminated, but such errors as full-scale and zero scale offset errors can be eliminated quite easily. See Figure 2.

Zero Scale Error

Zero scale error of an A/D is the difference of potential between the ideal 1/2 LSB value (9.8mV for $V_{REF}/2 = 2.500V$) and that input voltage which just causes an output transition from code 0000 0000 to a code of 0000 0001.

If the minimum input value is not ground potential, a zero offset can be made. The converter can be made to output a digital code of 0000 0000 for the minimum expected input voltage by biasing the $V_{IN}(-)$ input to that minimum value expected at the $V_{IN}(-)$ input to that minimum value expected at the $V_{IN}(+)$ input. This uses the differential mode of the converter. Any offset adjustment should be done prior to full scale adjustment.

Full Scale Adjustment

Full scale gain is adjusted by applying any desired offset voltage to $V_{IN}(-)$, then applying the $V_{IN}(+)$ a voltage that is 1 – 1/2 LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of $V_{REF}/2$ input voltage (or the V_{CC} supply if there is no $V_{REF}/2$ input connection) for a digital output code which just changes from 1111 1110 to 1111 1111. The ideal $V_{IN}(+)$ voltage for this full-scale adjustment is given by:

$$V_{IN}(+) = V_{IN}(-) - 1.5 \times \frac{V_{MAX} - V_{MIN}}{255}$$

where:

V_{MAX} = high end of analog input range (ground referenced)

V_{MIN} = low end (zero offset) of analog input (ground referenced)

CLOCKING OPTION

The clock signal for these A/Ds can be derived from external sources, such as a system clock, or self-clocking can be accomplished by adding an external resistor and capacitor, as shown in Figure 5.

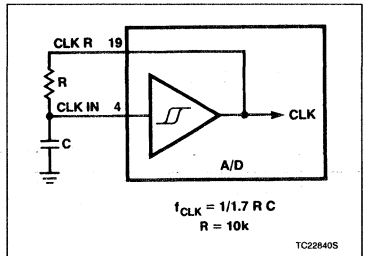


Figure 5. Self-Clocking the Converter

Heavy capacitive or DC loading of the CLK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF are allowed. This permits driving up to seven A/D converter CLK IN pins of this family from a single CLK R pin of one converter. For larger loading of the clock line, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin.

Restart During a Conversion

A conversion in process can be halted and a new conversion began by bringing the $\overline{CS}$ and $\overline{WR}$ inputs low and allowing at least one of them to go high again. The output data latch is not updated if the conversion in progress is not completed; the data from the previously completed conversion will remain in the output data latches until a subsequent conversion is completed.

Continuous Conversion

To provide continuous conversion of input data, the $\overline{CS}$ and $\overline{RD}$ inputs are grounded and $\overline{INTR}$ output is tied to the $\overline{WR}$ input. This $\overline{INTR}/\overline{WR}$ connection should be momentarily forced to a logic low upon power-up to insure circuit operation. See Figure 6 for one way to accomplish this.

DRIVING THE DATA BUS

This CMOS A/D converter, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry tied to the data bus will add to the total capacitive loading, even in the high impedance mode.

There are alternatives in handling this problem. The capacitive loading of the data bus slows down the response time, although DC specifications are still met. For systems with a relatively low CPU clock frequency, more time is available in which to establish proper logic levels on the bus, allowing higher capacitive loads to be driven (see Typical Performance Characteristics).

At higher CPU clock frequencies, time can be extended for I/O reads (and/or writes) by inserting wait states (8880) or using clock-extending circuits (6800, 8035).

Finally, if time is critical and capacitive loading is high, external bus drivers must be used. These can be 3-State buffers (low power Schottky is recommended, such as the N74LS240 series) or special higher current drive products designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended as the PNP input offers low loading of the A/D output, allowing better response time.

POWER SUPPLIES

Noise spikes on the V_{CC} line can cause conversion errors as the internal comparator will respond to them. A low inductance filter capacitor should be used close to the converter V_{CC} pin and values of 1μF or greater are recommended. A separate 5V regulator for the converter (and other 5V linear circuit-

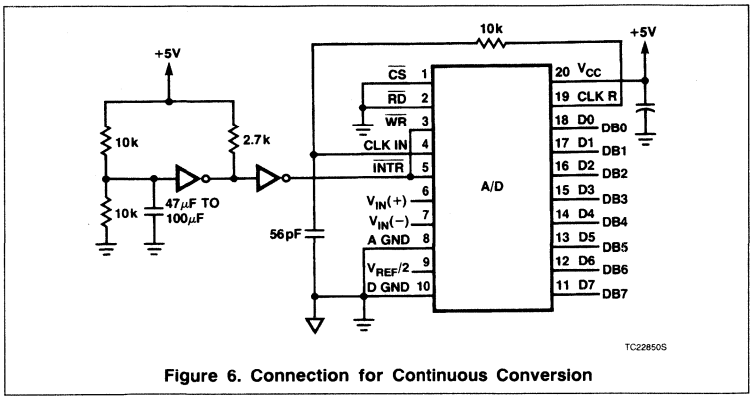


Figure 6. Connection for Continuous Conversion

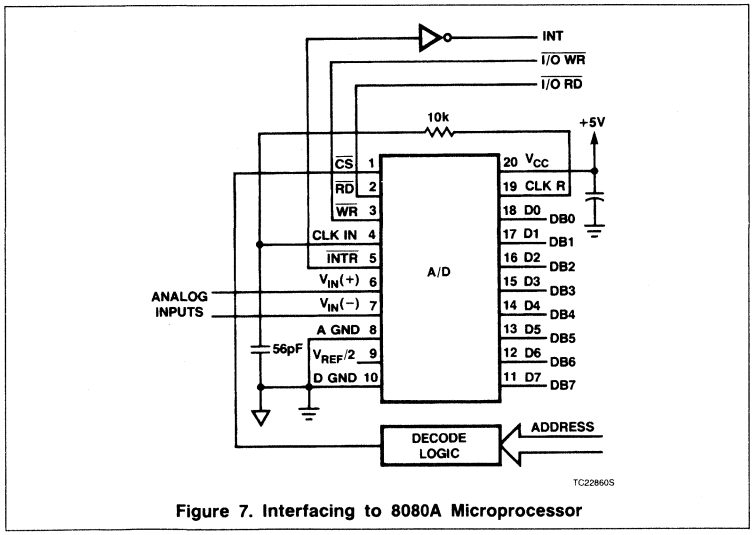


Figure 7. Interfacing to 8080A Microprocessor

ry) will greatly reduce digital noise on the V_{CC} supply and the attendant problems.

WIRING AND LAYOUT PRECAUTIONS

Digital wire-wrap sockets and connections are not satisfactory for breadboarding this (or any) A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped or kept as far as possible from the analog signal leads. Single wire analog input leads may pick up undesired hum and noise, requiring the use of shielded leads to the analog inputs in many applications.

A single-point analog ground separate from the logic or digital ground points should be used. The power supply bypass capacitor and the self-clocking capacitor, if used, should be returned to digital ground. Any $V_{REF}/2$ bypass capacitor, analog input filter capacitors, and any input shielding should be returned to the analog ground point. Proper grounding will minimize zero-scale errors which are present in every code. Zero-scale errors can usually be traced to improper board layout and wiring.

APPLICATIONS

Microprocessor Interfacing

This family of A/D converters was designed for easy microprocessor interfacing. These converters can be memory mapped with appropriate memory address decoding for $\overline{CS}$ (read) input. The active-Low write pulse from the processor is then connected to the $\overline{WR}$ input of the A/D converter, while the processor active-Low read pulse is fed to the converter $\overline{RD}$ input to read the converted data. If the clock signal is derived from the microprocessor system clock, the designer/programmer should be sure that there is no attempt to read the converter until 74 converter clock pulses after the start pulse goes high. Alternatively, the $\overline{INTR}$ pin may be used to interrupt the processor to cause reading of the converted data. Of course, the converter can be connected and addressed as a peripheral (in I/O space), as shown in Figure 7. A bus driver should be used as a buffer to the A/D output in large microprocessor systems where the data leaves the PC board and/or must drive capacitive loads in excess of 100pF. See Figure 9.

Interfacing the SCN8048 microcomputer family is pretty simple, as shown in Figure 8. Since the SCN8048 family has 24 I/O lines, one of these (shown here as bit 0 or port 1) can be used as the chip select signal to the converter, eliminating the need for an address decoder. The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing to a dummy address.

Digitizing a Transducer Interface Output

Circuit Description

Figure 10 shows an example of digitizing transducer interface output voltage. In this case, the transducer interface is the NE5521, an LVDT (Linear Variable Differential Transformer) Signal Conditioner. The diode at the A/D input is used to insure that the input to the A/D does not go excessively beyond the supply voltage of the A/D. See the NE5521 data sheet for a complete description of the operation of that part.

Circuit Adjustment

To adjust the full scale and zero scale of the A/D, determine the range of voltages that the transducer interface output will take on. Set the LVDT core for null and set the Zero Scale Scale Adjust Potentiometer for a digital output from the A/D of 1000 000. Set the LVDT core for maximum voltage from the interface and set the Full Scale Adjust potentiometer so the A/D output is just barely 1111 1111.

A Digital Thermostat

Circuit Description

The schematic of a Digital Thermostat is shown in Figure 11. The A/D digitizes the output of the LM35, a temperature transducer IC with an output of 10mV per °C. With $V_{REF}/2$ set for 2.56V, this 10mV corresponds to 1/2 LSB and the circuit resolution is 2°C. Reducing $V_{REF}/2$ to 1.28 yields a resolution of 1°C. Of course, the lower $V_{REF}/2$ is, the more sensitive the A/D will be to noise.

The desired temperature is set by holding either of the set buttons closed. The SCC80C451 programming could cause the desired (set) temperature to be displayed

while either button is depressed and for a short time after it is released. At other times the ambient temperature could be displayed.

The set temperature is stored in an SCN8051 internal register. The A/D conversion is started by writing anything at all to the A/D with port pin P10 set high. The desired temperature is compared with the digitized actual temperature, and the heater is turned on or off by clearing setting port pin P12. If desired, another port pin could be used to turn on or off an air conditioner.

The display drivers are NE587s if common anode LED displays are used, and NE589s if common cathode LED displays are used. Of course, it is possible to interface to LCD displays as well.

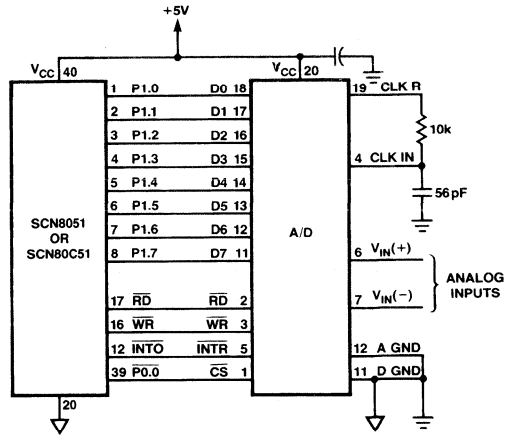


Figure 8. SCN8051 Interfacing

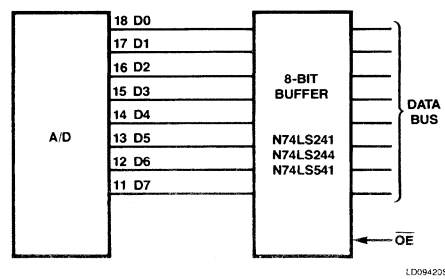


Figure 9. Buffering the A/D Output to Drive High Capacitance Loads and for Driving Off-Board Loads

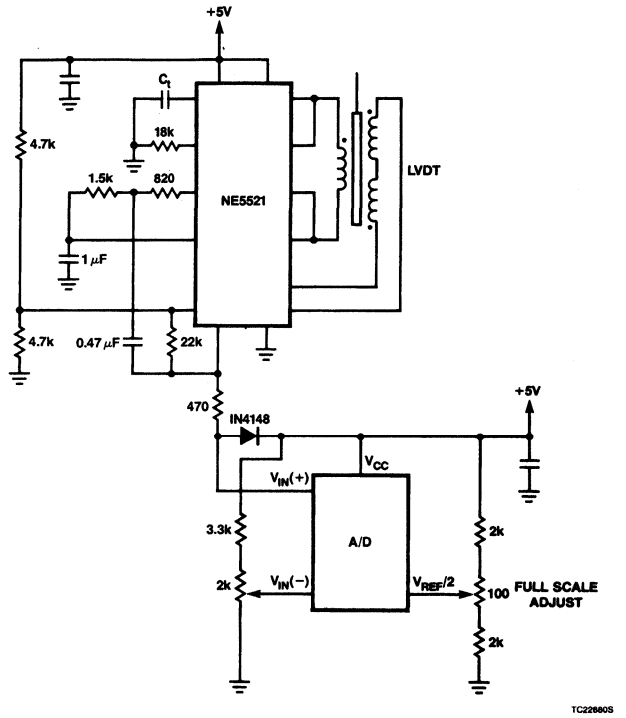


Figure 10. Digitizing a Transducer Interface Output

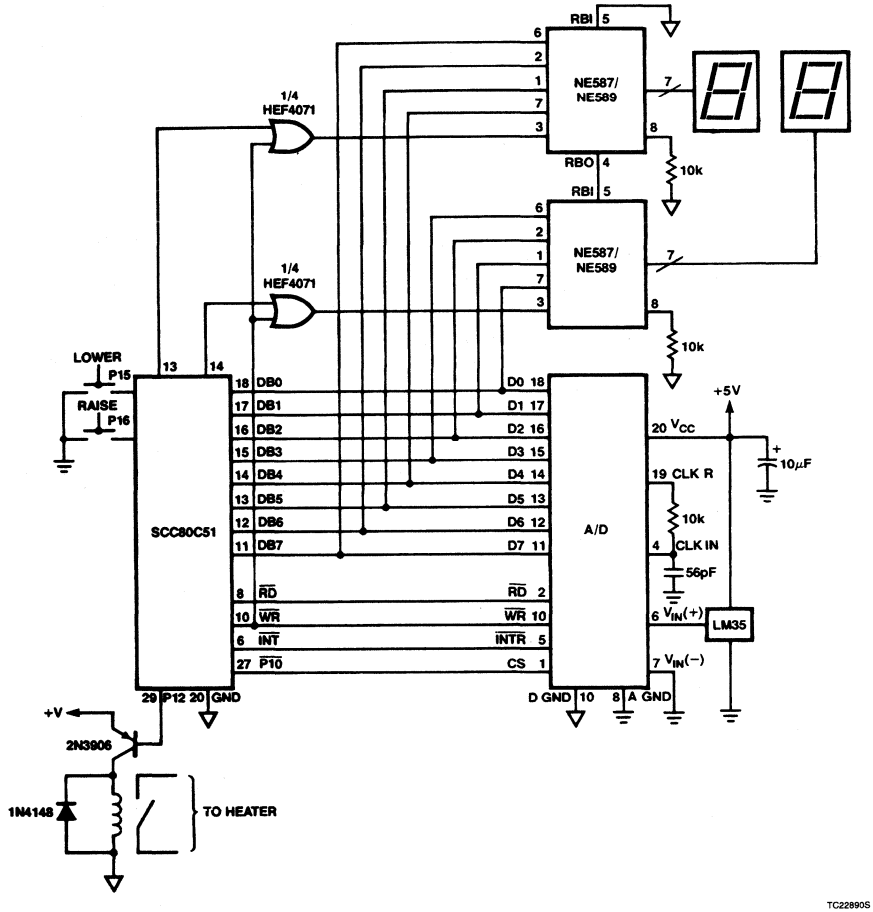


Figure 11. Digital Thermostat

ADC0820

8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function

Preliminary Specification

DESCRIPTION

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5μs conversion time while dissipating a maximum 75mW of power. The half-flash technique consists of 31 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold for signals slewing at less than 100mV/μs.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

FEATURES

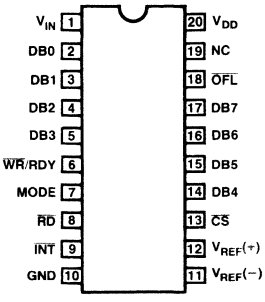
- **Built-in track-and-hold function**
- **No missing codes**
- **No external clocking**
- **Single supply — $5V_{DC}$**
- **Easy interface to all microprocessors, or operates stand-alone**
- **Latched 3-State outputs**
- **Logic inputs and outputs meet both MOS and TTL voltage level specifications**
- **Operates ratiometrically or with any reference value equal to or less than V_{DD}**
- **0V to 5V analog input voltage range with single 5V supply**
- **No zero- or full-scale adjust required**
- **Overflow output available for cascading**
- **0.3″ standard width 20-pin DIP**

APPLICATIONS

- **Microprocessor-based monitoring and control systems**
- **Transducer/μP interface**
- **Process control**
- **Logic analyzers**
- **Test and measurement**

PIN CONFIGURATION

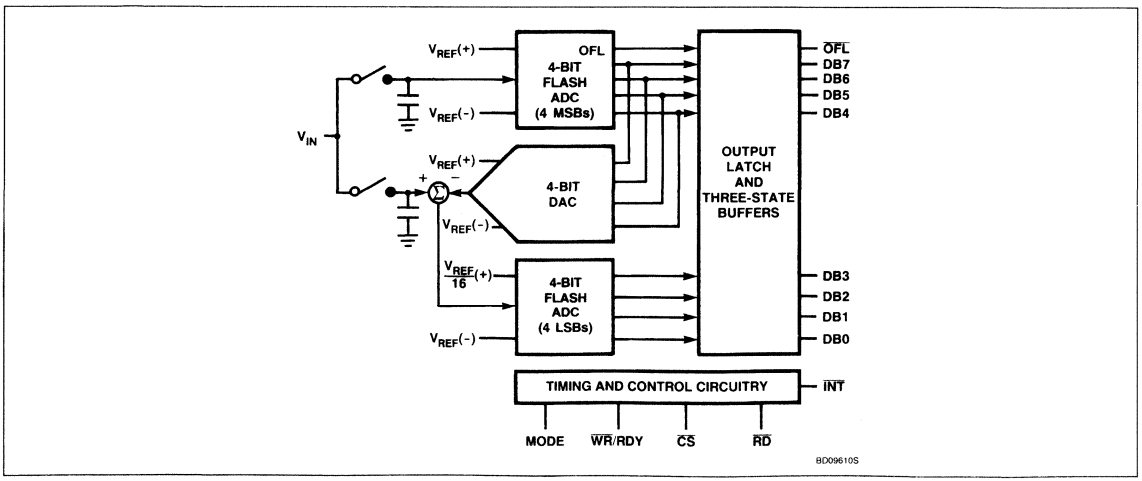
D, F, N Packages



TOP VIEW

CD12921S

BLOCK DIAGRAM



BD09610S

8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function

ADC0820

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	ADC0820BNEN
20-Pin Plastic SO package	0 to +70°C	ADC0820BNED
20-Pin Plastic DIP	0 to +70°C	ADC0820CNEN
20-Pin Plastic SO package	0 to +70°C	ADC0820CNED
20-Pin Plastic DIP	−40°C to +85°C	ADC0820BSAN
20-Pin Plastic SO package	−40°C to +85°C	ADC0820BSAD
20-Pin Plastic DIP	−40°C to +85°C	ADC0820CSAN
20-Pin Plastic SO package	−40°C to +85°C	ADC0820CSAD
20-Pin Ceramic DIP	−55°C to +125°C	ADC0820BSEF
20-Pin Ceramic DIP	−55°C to +125°C	ADC0820CSEF

PIN DESCRIPTION

PIN NO	SYMBOL	DESCRIPTION
1	V_{IN}	Analog input; range = GND ≤ V_{IN} ≤ V_{DD}
2	DB0	3-state data output — Bit 0 (LSB)
3	DB1	3-state data output — Bit 1
4	DB2	3-state data output — Bit 2
5	DB3	3-state data output — Bit 3
6	$\overline{WR}$/RDY	**WR-RD Mode** $\overline{WR}$: With $\overline{CS}$ Low, the conversion is started on the falling edge of $\overline{WR}$. Approximately 800ns (the preset internal time out, t_i) after the $\overline{WR}$ rising edge, the result of the conversion will be strobed into the output latch, provided that $\overline{RD}$ does not occur prior to this time out (see Figures 3a and 3b). **RD Mode** RDY: This is an open-drain output (no internal pull-up device). RDY will go Low after the falling edge of $\overline{CS}$; RDY will go 3-State when the result of the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system (see Figure 1).
7	Mode	Mode: Mode selection input — it is internally tied to GND through a 30μA current source. RD Mode: When mode is Low. WR-RD Mode: When mode is High.
8	$\overline{RD}$	**WR-RD Mode** With $\overline{CS}$ Low, the 3-State data outputs (DB0 – DB7) will be activated when $\overline{RD}$ goes Low. $\overline{RD}$ can also be used to increase the speed of the converter by reading data prior to the preset internal time out (T_i ~ 800ns). If this is done, the data result transferred to output latch is latched after the falling edge of the $\overline{RD}$ (see Figures 3a and 3b). **RD Mode** With $\overline{CS}$ Low, the conversion will start with $\overline{RD}$ going Low; also, $\overline{RD}$ will enable the 3-State data outputs at the completion of the conversion. RDY going 3-State and $\overline{INT}$ going Low indicate the completion of the conversion (see Figure 1).

8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function

PIN DESCRIPTION (Continued)

PIN NO	SYMBOL	DESCRIPTION
9	$\overline{INT}$	**WR-RD Mode** $\overline{INT}$ going Low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ will go Low ~ 800ns (the preset internal time out, t_I) after the rising edge of $\overline{WR}$ (see Figure 3a); or $\overline{INT}$ will go Low after the falling edge of $\overline{RD}$, if $\overline{RD}$ goes Low prior to the 800ns time out (see Figure 3b). $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see Figures 3a and 3b). **RD Mode** $\overline{INT}$ going Low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see Figure 1).
10	GND	Ground
11	$V_{REF}(-)$	The bottom of resistor ladder, voltage range: $GND \leq V_{REF}(-) \leq V_{REF}(+)$
12	$V_{REF}(+)$	The top of resistor ladder, voltage range: $V_{REF}(-) \leq V_{REF}(+) \leq V_{DD}$.
13	$\overline{CS}$	$\overline{CS}$ must be Low in order for the $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	3-State data output — Bit 4
15	DB5	3-State data output — Bit 5
16	DB6	3-State data output — Bit 6
17	DB7	3-State data output — Bit 7 (MSB)
18	$\overline{OFL}$	Overflow output — if the analog input is higher than the $V_{REF}(+)-\frac{1}{2}$ LSB, $\overline{OFL}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit).
19	NC	No connection
20	V_{DD}	Power supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage	7	V
	Logic control inputs	-0.2 to $V_{DD}+0.2$	V
	Voltage at other inputs and output	-0.2 to $V_{DD}+0.2$	V
T_{STG}	Storage temperature range	-65 to $+150$	°C
P_D	Maximum power dissipation[3] $T_A = 25°C$ (still-air) F package N package D package	 1560 1690 1390	 mW mW mW
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C
T_A	Operating ambient temperature range ADC0820BSEF/CSEF ADC0820BSAN/CSAN/BSAD/CSAD ADC0820BNEN/CNEN/BNED/CNED	$T_{MIN} \leq T_A \leq T_{MAX}$ -55 to $+125$ -40 to $+85$ 0 to $+70$	 °C °C °C

NOTES:
1. Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.
2. All voltages are measured with respect to GND, unless otherwise specified.
3. Derate above 25°C, at the following rates:
   F package at 12.5mW/°C.
   N package at 13.5mW/°C.
   D package at 11.1mW/°C.

8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function

ADC0820

DC ELECTRICAL CHARACTERISTICS RD mode (Pin 7 = 0), V_{DD} = 5V, $V_{REF}(+)$ = 5V, and $V_{REF}(-)$ = GND, unless otherwise specified. Limits apply from T_{MIN} to T_{MAX}.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ[3]	Max	
	Resolution			8	8	8	bits
	Unadjusted error[1]	ADC0820B ADC0820C				± ½ ± 1	LSB LSB
R_{REF}	Reference resistance			1	1.6	4	kΩ
$V_{REF}(+)$	Input voltage			$V_{REF}(-)$		V_{DD}	V
$V_{REF}(-)$	Input voltage			GND		$V_{REF}(+)$	V
V_{IN}	Input voltage			GND − 0.1		V_{DD} + 0.1	V
	Maximum analog input leakage current	$\overline{CS} = V_{DD}$ $V_{IN} = V_{DD}$ V_{IN} = GND		−3		3	μA
	Power supply sensitivity	V_{DD} = 5V ± 5%			± 1/16	± ¼	LSB
$V_{IN(1)}$	Logical "1" input voltage	V_{DD} = 5.25V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	2.0		V_{DD}	V
			Mode	3.5		V_{DD}	V
$V_{IN(0)}$	Logical "0" input voltage	V_{DD} = 4.75V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	GND		0.8	V
			Mode	GND		1.5	V
$I_{IN(1)}$	Logical "1" input current	$V_{IN(1)}$ = 5V; $\overline{CS}$, $\overline{RD}$ $V_{IN(1)}$ = 5V; $\overline{WR}$ $V_{IN(1)}$ = 5V; Mode			 30	1 3 200	μA μA μA
$I_{IN(0)}$	Logical "0" input current	$V_{IN(0)}$ = 0V; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		−1			μA
$V_{OUT(1)}$	Logical "1" output voltage	V_{DD} = 4.75V, I_{OUT} = −360μA; DB0 − DB7, $\overline{OFL}$, $\overline{INT}$		2.4	4.6		V
		V_{DD} = 4.75V, I_{OUT} = −10μA DB0 − DB7, $\overline{OFL}$, $\overline{INT}$		4.5	4.74		V
$V_{OUT(0)}$	Logical "0" output voltage	V_{DD} = 4.75V, I_{OUT} = 1.6mA; DB0 − DB7, $\overline{OFL}$, $\overline{INT}$, RDY			0.2	0.4	V
I_{OZ}	3-state output current	V_{OUT} = 5V; DB0 − DB7, RDY V_{OUT} = 0V; DB0 − DB7, RDY		 −3		3	μA μA
I_{SOURCE}	Output source current	V_{OUT} = 0V, DB0 − DB7, $\overline{OFL}$ $\overline{INT}$		6 4.5	12 8		mA mA
I_{SINK}	Output sink current	V_{OUT} = 5V; DB0 − DB7, $\overline{OFL}$, $\overline{INT}$, RDY		7	20		mA
I_{DD}	Supply current	$\overline{CS} = \overline{WR} = \overline{RD}$ = 0			6	15	mA
V_{DD}	Range			4.5		5.5	V

8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function

ADC0820

AC ELECTRICAL CHARACTERISTICS

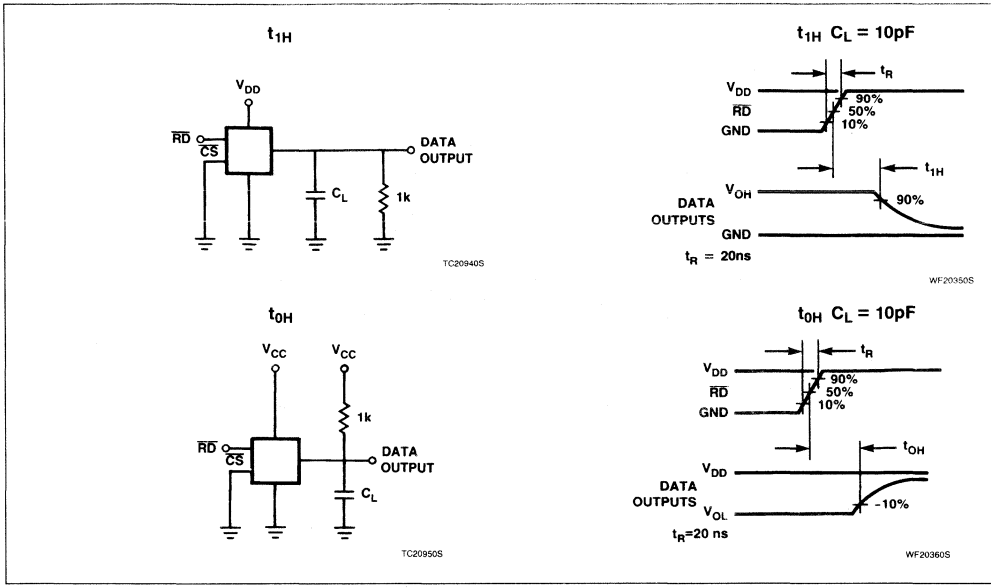
V_{DD} = 5V, $t_R = t_F$ = 20ns, $V_{REF(+)}$ = 5V, $V_{REF(-)}$ = 0V, and T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS[4]			UNIT
				Min	Typ[3]	Max	
t_{CRD}	Conversion time for RD mode		Mode = 0, Figure 1		1.6	2.5	μs
t_{ACCO}	Access time (delay from falling edge of $\overline{RD}$ to output valid)		Mode = 0, Figure 1		t_{CRD} + 20	t_{CRD} + 50	ns
t_{CWR-RD}	Conversion time for WR-RD mode		Mode = V_{DD}, t_{WR} = 600ns, t_{RD} = 600ns; Figures 3a and 3b			1.52	μs
t_{WR}	Write time	Min	Mode = V_{DD}, Figures 3a and 3b[2]	600			ns
		Max				50	μs
t_{RD}	Read time	Min	Mode = V_{DD}, Figures 3a and 3b[2]	600			ns
t_{ACC1}	Access time (delay from falling edge of $\overline{RD}$ to output valid)		Mode = V_{DD}, $t_{RD} < t_I$; Figure 3b, C_L = 15pF		190	280	ns
			C_L = 100pF		210	320	ns
t_{ACC2}	Access time (delay from falling edge of $\overline{RD}$ to output valid)		Mode = V_{DD}, $t_{RD} > t_I$; Figure 3a, C_L = 15pF		70	120	ns
			C_L = 100pF		90	150	ns
t_I	Internal comparison time		Mode = V_{DD}; Figures 2 and 3a, C_L = 50pF		800	1300	ns
t_{1H}, t_{0H}	Three-state control (delay from rising edge of $\overline{RD}$ to Hi-Z state)		R_L = 1kΩ, C_L = 10pF		100	200	ns
$t_{\overline{INT}L}$	Delay from rising edge of $\overline{WR}$ to falling edge of $\overline{INT}$		Mode = V_{DD}, C_L = 50pF $t_{RD} > t_I$; Figure 3a $t_{RD} < t_I$; Figure 3b		 t_{RD} + 200	 t_I t_{RD} + 290	 ns ns
$t_{\overline{INT}H}$	Delay from rising edge of $\overline{RD}$ to rising edge of $\overline{INT}$		Figures 1, 3a, and 3b, C_L = 50pF		125	225	ns
$t_{\overline{INT}HWR}$	Delay from rising edge of $\overline{WR}$ to rising edge of $\overline{INT}$		Figure 2, C_L = 50pF		175	270	ns
t_{RDY}	Delay from $\overline{CS}$ to RDY		Figure 1, C_L = 50pF, Mode = 0		50	100	ns
t_{ID}	Delay from $\overline{INT}$ to output valid		Figure 2		20	50	ns
t_{RI}	Delay from $\overline{RD}$ to $\overline{INT}$		Mode = V_{DD}, $t_{RD} < t_I$; Figure 3b		200	290	ns
t_P	Delay from end of conversion to next conversion		Figures 1, 2, 3a, and 3b[2]	500			ns
SR	Slew rate, tracking				0.1		V/μs
C_{VIN}	Analog input capacitance				45		pF
C_{OUT}	Logic output capacitance				5		pF
C_{IN}	Logic input capacitance				5		pF

NOTES:
1. Unadjusted error includes offset, full-scale, and linearity errors.
2. Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified.
3. Typicals are at 25°C and represent most likely parametric norm.
4. Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function

3-STATE TEST CIRCUITS AND WAVEFORMS



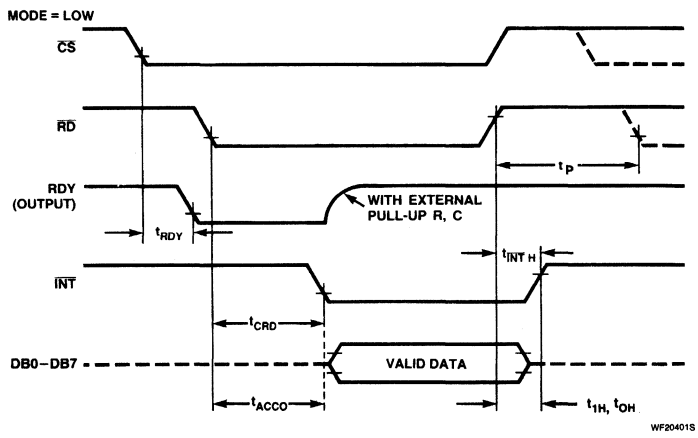


Figure 1. RD Mode

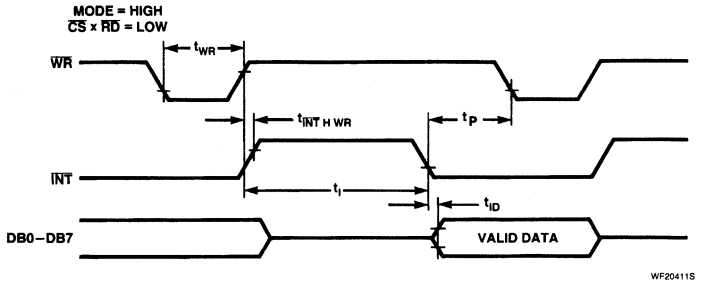
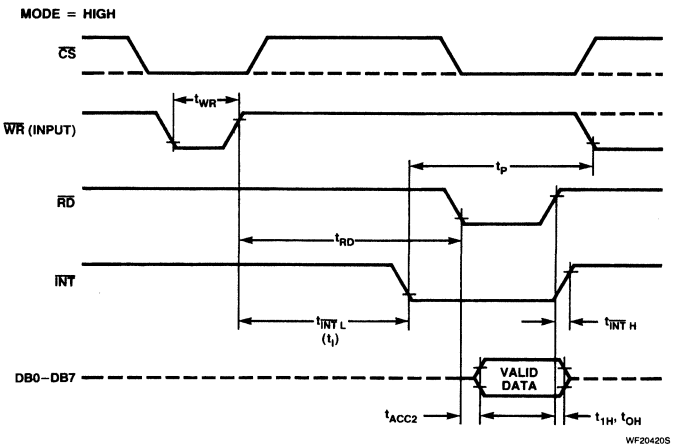
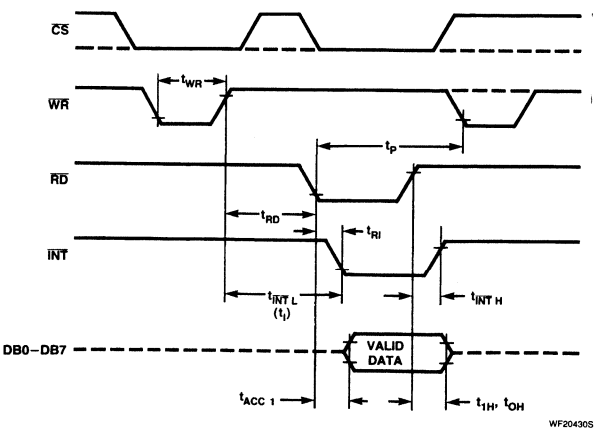


Figure 2. Stand-Alone Mode



a. WR – RD Mode ($t_{RD} > t_I$)



b. WR – RD Mode ($t_{RD} < t_I$)

Figure 3

8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function

ADC0820

FUNCTIONAL DESCRIPTION

General Operation

The ADC0820 uses two 4-bit flash A/D converters to make an 8-bit measurement (Block Diagram). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word.

The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder which most closely approximates the analog input. In addition, the "sampled data" comparators used in the ADC0820 provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

The Sampled-Data Comparator

Each comparator in the ADC0820 consists of a CMOS inverter with a capacitively-coupled input (Figure 4). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter's feedback switch (Figure 4a) are closed. In this interval, C is charged to the connected input (V1) less the inverter's bias voltage (V_S, approximately 1.6V). In the second cycle (Figure 4b), these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter's input (V_S') becomes

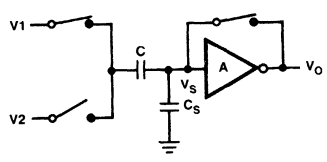
$$V_S' = V_S + (V2-V1)\frac{C}{C + C_S}$$

and the output will go High or Low depending on the sign of $V_S'-V_S$.

The actual circuitry used in the ADC0820 is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (Figure 5), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor (S switches) and opening all of the other switches. The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.

Architecture

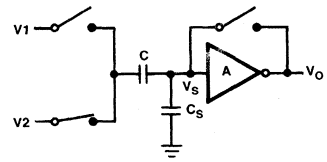
In the ADC0820, 15 comparators are used in the MS and LS 4-bit flash A/D converters. The MS (most significant) flash ADC also has one additional comparator to detect input overrange. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.



- $V_O = V_S$
- V ON C = V1 − V_B
- C_S = STRAY INPUT NODE CAPACITOR
- V_S = INVERTER INPUT BIAS VOLTAGE

TC20962S

a. Zeroing Phase

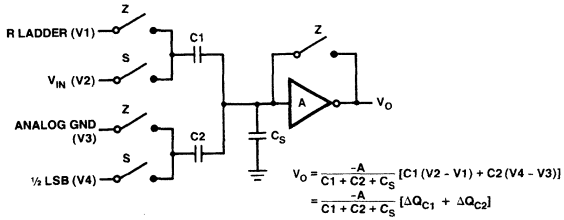


- $V_S' - V_S = (V2 - V1)\frac{C}{C + C_S}$
- $V_O' = \frac{-A}{C + C_S}[CV2 - CV1]$
- V_O' IS DEPENDENT ON V2−V1

TC20971S

b. Compare Phase

Figure 4. Sampled Data Comparator



TC20980S

Figure 5. ADC0820 Comparator (From MS Flash ADC)

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To start a conversion in the WR-RD mode, the $\overline{WR}$ line is brought Low. At this instant the MS comparators go from zeroing to comparison mode (Figure 8). When $\overline{WR}$ is returned High after at least 600ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600ns later, the $\overline{RD}$ line may be pulled Low to latch the lower four data bits and finish the 8-bit conversion. When $\overline{RD}$ goes Low, the flash A/Ds change state once again in preparation for the next conversion.

Figure 8 also outlines how the converter's interface timing relates to its analog input (V_{IN}). In WR-RD mode, V_{IN} is measured while $\overline{WR}$ is Low. In RD mode, sampling occurs during the first 800ns of $\overline{RD}$. Because of the input connections to the ADC0820's LS and MS comparators, the converter has the ability to sample V_{IN} at one instant, despite the fact that two separate 4-bit conversions are being done. More specifically, when $\overline{WR}$ is Low the MS flash is in compare mode (connected to V_{IN}, and the LS flash is in zero mode (also connected to V_{IN}). Therefore both flash ADCs sample V_{IN} at the same time.

Digital Interface

The ADC0820 has two basic interface modes which are selected by strapping the Mode pin High or Low.

RD Mode (Figure 6a)

With the Mode pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling $\overline{RD}$ Low until output data appears. An $\overline{INT}$ line is provided which goes Low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.

When in RD mode, the comparator phases are internally triggered. At the falling edge of $\overline{RD}$, the MS flash converter goes from zero to compare mode and the LS ADC's comparators enter their zero cycle. After 800ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800ns, the lower four bits are recovered.

WR Then RD Mode (Figures 6b and c)

With the Mode pin tied High, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the $\overline{WR}$ input; however, there are two options for reading the output data which relate to interface timing. If an interrupt-driven scheme is desired, the user can wait for $\overline{INT}$ to go Low before reading the conversion result. $\overline{INT}$ will typically go Low 800ns after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exer-

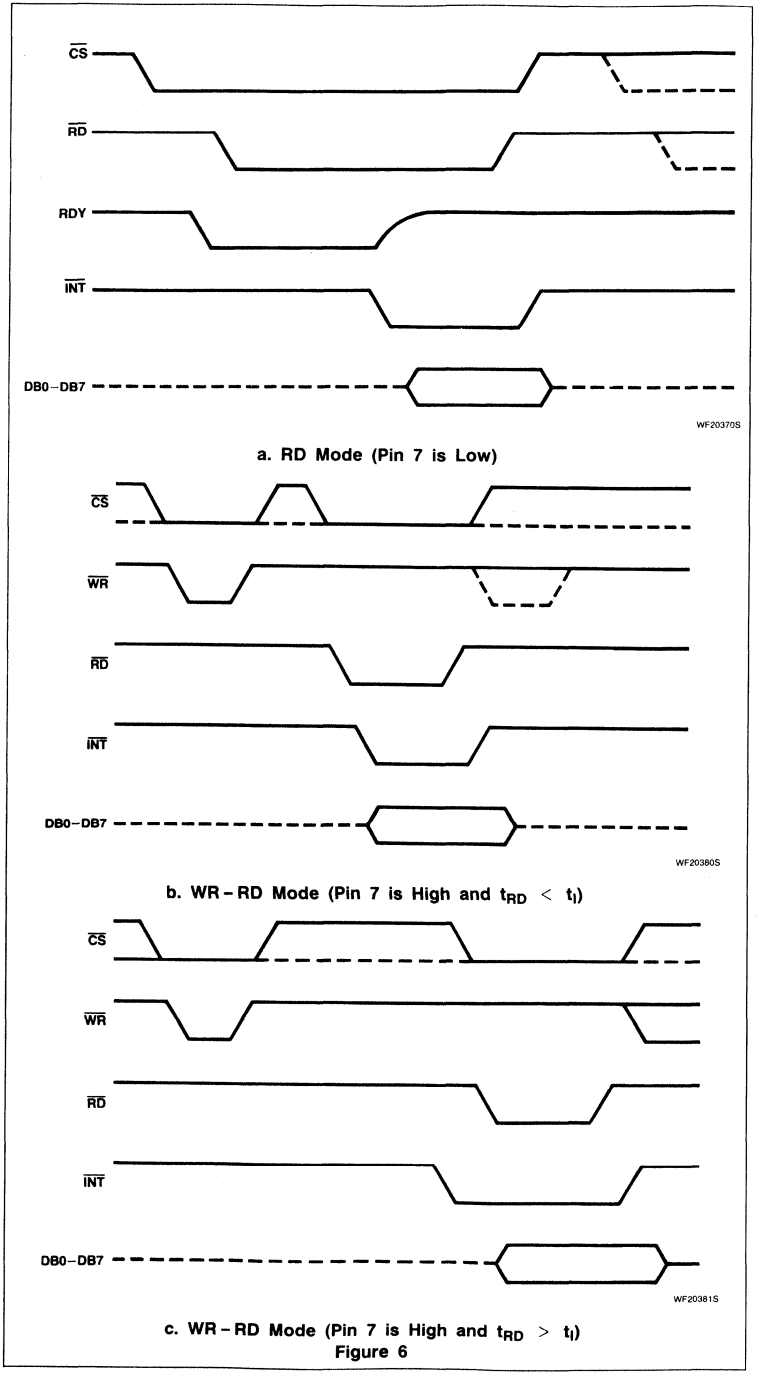


Figure 6

8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function

ADC0820

cise a Read after only 600ns. If this is done, $\overline{INT}$ will immediately go Low and data will appear at the outputs.

Stand-Alone (Figure 7)

For stand-alone operation in WR-RD mode, $\overline{CS}$ and $\overline{RD}$ can be tied Low and a conversion can be started with $\overline{WR}$. Data will be valid approximately 800ns following $\overline{WR}$'s rising edge.

Other Interface Considerations

In order to maintain conversion accuracy, $\overline{WR}$ has a maximum width spec of 50μs. When the MS flash ADC's sampled data comparators are in comparison mode ($\overline{WR}$ is Low), the input capacitors (C, Figure 5) must hold their charge. Switch leakage can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion, a new conversion cannot be started until this phase is complete. The minimum spec for this time is 500ns (t_P in Figure 1, 2, 3a, and 3b).

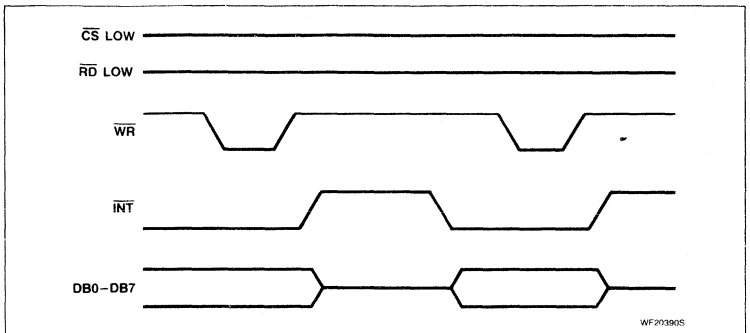


Figure 7. WR – RD Mode (Pin 7 is High) Stand-Alone Operation

ANALOG CONSIDERATIONS

Reference and Input

The two V_{REF} inputs of the ADC0820 are fully differential and define the zero- to full-scale input range of the A/D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing $V_{REF}(V_{REF} = V_{REF}(+) - V_{REF}(-))$ to less than 5V, the sensitivity of the converter can be increased (i.e., if V_{REF} = 2V, then 1 LSB = 7.8mV). The input/reference arrangement also facilitates ratiometric operation and, in many cases, the chip power supply can be used for transducer power as well as the V_{REF} source.

This reference flexibility lets the input span not only be varied, but also offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. Figure 9 shows some of the configurations that are possible.

Input Current

Due to the unique conversion techniques employed by the ADC0820, the analog input behaves somewhat differently than in conventional devices. The A/D's sampled data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the ADC0820 is shown in Figure 10a. When a conversion starts ($\overline{WR}$ Low, WR-RD mode), all input switches close, connecting V_{IN} to 31 1pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, V_{IN} still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase. In other words, the LS ADC uses V_{IN} as its zero-phase input.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 5kΩ to 10kΩ). In addition, about 12pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in Figure 10b. As R_S increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that $\overline{WR}$ is Low. Since other factors force this time to be at least 600ns, input time constants of 100ns can be accommodated without special consideration. Typical total input capacitance values of 45pF allow R_S to be 1.5kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

Input Filtering

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_{IN}, will not degrade the A/D's performance in most cases. In effect, the ADC0820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is Low, so at least 600ns will be provided to charge the ADC's input capacitance. It is therefore not

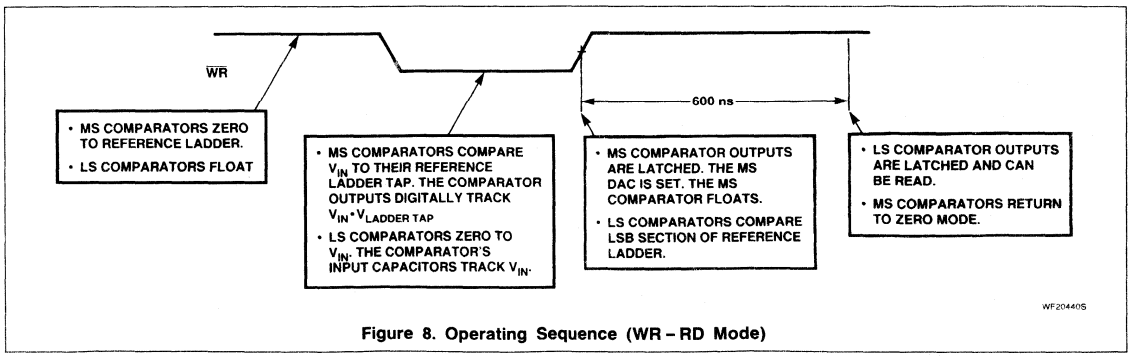
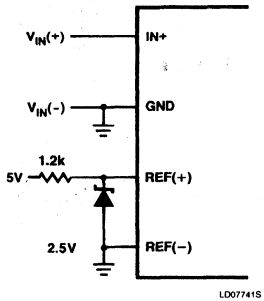
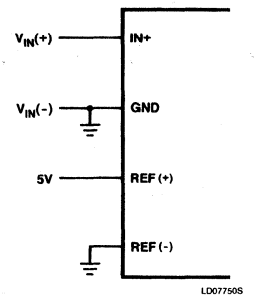


Figure 8. Operating Sequence (WR – RD Mode)

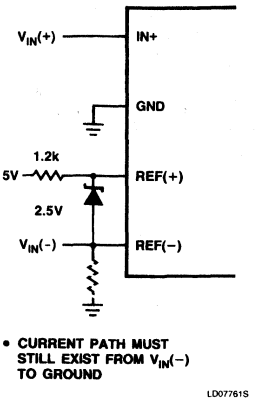
8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function



a. External Reference 2.5V Full-Scale

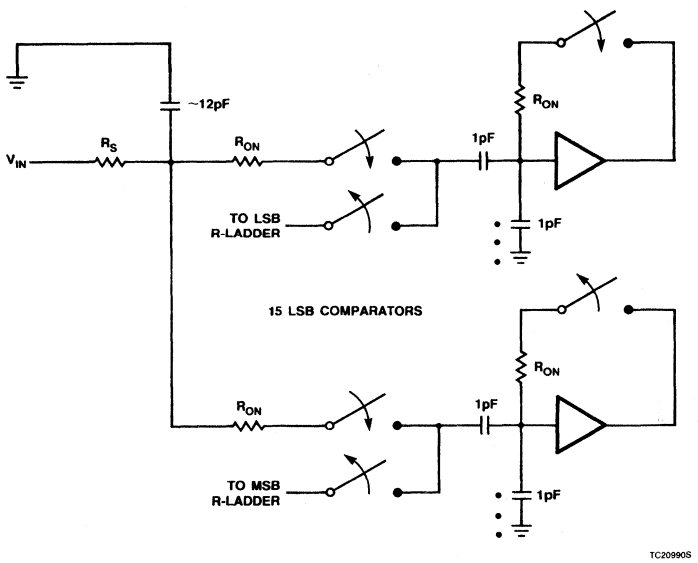


b. Power Supply as Reference

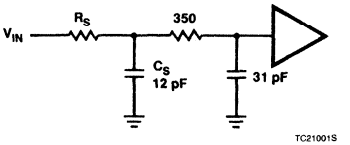


c. Input not Referred to GND

Figure 9. Analog Input Options



a.



b.

Figure 10

8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function

necessary to filter out these transients by putting an external cap on the V_{IN} terminal, if an input amplifier that can settle within 600ns is used to drive the input. The NE530 is a suitable op amp for driving the input of the ADC0820.

Inherent Sample-Hold

Another benefit of the ADC0820's input mechanism is its ability to measure a variety of high-speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least ½ LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high-speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled data comparators, by nature of their input switching, already accomplish this function to a large degree (Section 1.2). Although the conversion time for the ADC0820 is 1.5μs, the time through which V_{IN} must be ½ LSB stable is much smaller. Since the MS flash ADC uses V_{IN} as its "compare" input and the LS ADC uses V_{IN} as its "zero" input, the ADC0820 only "samples" V_{IN} when $\overline{WR}$ is Low. Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_{IN} approximately 100ns after the rising edge of $\overline{WR}$ (100ns due to internal logic propagation delay) will be the measured value.

Input signals with slew rates typically below 100mV/μs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1μs would still not be able to measure a 5V, 1kHz sine wave without the aid of an external sample-and-hold. The ADC0820, with no such help, can typically measure 5V, 7kHz waveforms.

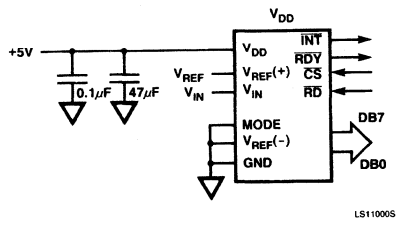


Figure 11. 8-Bit Resolution Configuration

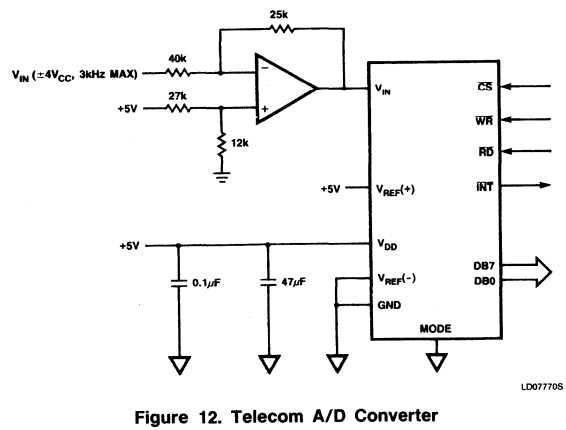


Figure 12. Telecom A/D Converter

8-Bit, High-Speed, μP-Compatible A/D Converter With Track/Hold Function

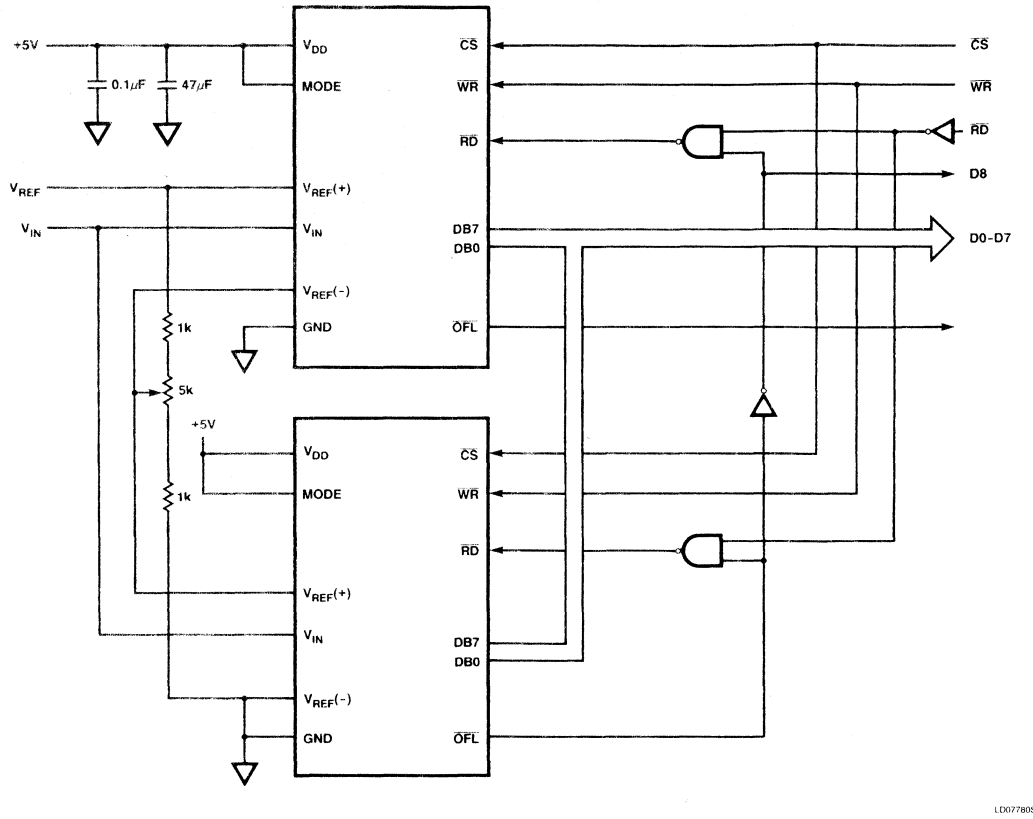


Figure 13. 9-Bit Resolution Configuration

NE5034
8-Bit High-Speed A/D Converter

Product Specification

DESCRIPTION

The NE5034 is a high-speed microprocessor-compatible 8-bit analog-to-digital converter. It uses the successive approximation conversion technique, and includes the comparator, reference DAC, SAR, an internal clock and 3-State buffers all on the same chip.

The converter can accommodate a wide analog input voltage range, bipolar or unipolar, selectable through external input resistors. An external capacitor controls the internal clock frequency, providing conversion times down to 17μs. Faster conversion times are possible using an external clock.

Microprocessor interfacing requirements are simple, allowing analog-to-digital conversion with a minimum of external components.

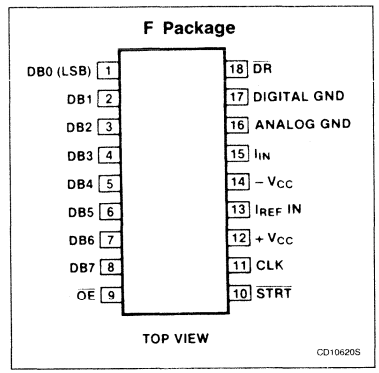
FEATURES

- **8-bit resolution and accuracy**
- **Accepts unipolar or bipolar inputs**
- **3-State output buffers for easy microprocessor interface**
- **Choice of internal or external clocking**
- **Short conversion time, 17μs typical using internal clock**

APPLICATIONS

- **All microprocessor-based monitoring and control systems requiring analog signal inputs**
- **Typical applications include: Automated process control, machine tools, robots, test and measurement instruments, environmental controls**
- **Other applications include: Ratiometric A/D conversion, very high resolution A/D conversion systems requiring high-speed 8-bit building blocks**

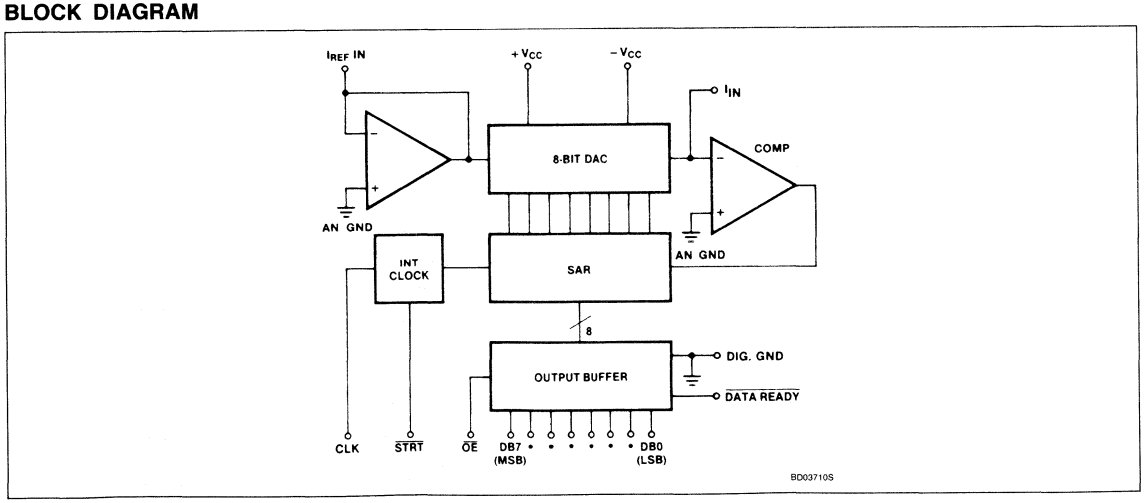
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Cerdip	0 to +70°C	NE5034F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	0 to +6	V
$V_{CC}-$	Negative supply voltage	0 to −15	V
I_{REF}	Reference current	1.5	mA
I_{IN}	Analog input current	5.0	mA
V_O	Data output voltage	6.0	V
V_L	Analog GND to Digital GND Logic input voltage	1.0 −1 to $V_{CC}+$	V V
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package	 1500	 mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTE:
1. Derate above 25°C at the following rates:
   F package at 12.0mW/°C.

DC ELECTRICAL CHARACTERISTICS

$+V_{CC} = 5.0V$, $-V_{CC} = -12V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		8	8	8	Bits
	Relative accuracy error[1, 2]				± ½	LSB
$V_{CC}+$	Positive supply range		4.75	5.0	5.25	V
$V_{CC}-$	Negative supply range		−11.4	−12	−12.6	V
ϵ_{FS}	Full-scale gain error	$I_{REF} = 1.0mA$, $T_A = 25°C$		±2	±5	LSB
ϵ_{ZS}	Zero-scale offset error	$I_{REF} = 1.0mA$, $T_A = 25°C$		±0.5	±1	LSB
PSR	Power supply rejection[3]	$I_{REF} = 1.0mA$, $V_{CC} = +4.75$ to $+5.25V$, $V_{CC} = -11.4$ to $-12.6V$			± ½	LSB
V_{IH}	Logic 1 input voltage ($\overline{STRT}$ and $\overline{OE}$)		2.0			V
V_{IH}	Logic 1 input voltage ext. clock		2.4			V
V_{IL}	Logic 0 input voltage ($\overline{STRT}$ and $\overline{OE}$)				0.8	V
V_{IL}	Logic 0 input voltage ext clock				0.7	V
I_{IH}	Logic 1 input current ($\overline{STRT}$ and $\overline{OE}$)	$V_{IN} = 2.4V$			20	μA
I_{IH}	Logic 1 input current ext clock	$V_{IN} = 2.4V$		100		μA
I_{IL}	Logic 0 input current ($\overline{STRT}$ and $\overline{OE}$)	$V_{IN} = 0.4V$		−20	−100	μA
I_{IL}	Logic 0 input current ext. clock	$V_{IN} = 0.7V$		−100		μA
V_{OL}	Logic 0 output voltage	$I_{OL} = 1.6mA$, $\overline{OE} = 0.8V$			0.4	V
V_{OH}	Logic 1 output voltage	$I_{OH} = 400\mu A$, $\overline{OE} = 0.8V$	2.4			V
I_{OZ}	Three-state leakage	$\overline{OE} = 2.0V$, $V_{OL} = 0V$ or $5V$		±10		μA
$I_{CC}+$	Positive supply current	$V_{CC} = +5V$, $V_{CC} = -12V$		18	36	mA
I_{CC}	Negative supply current	$V_{CC} = +5V$, $V_{CC} = -12V$		−11	−22	mA

NOTES:
1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero-scale to full-scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the 8-bit level which is 0.39% of the full-scale voltage.
3. Maximum change in full-scale.

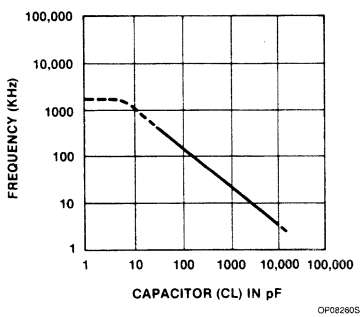
AC ELECTRICAL CHARACTERISTICS $V+ = +5V$, $V- = -12V$, $T_A = 25°C$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
	Internal clock frequency			C_L = 60pF (See Figure 1)		500		kHz
	External clock frequency						700	kHz
t_W	$\overline{STRT}$ pulse width			Clock freq. = 500kHz	400			ns
	External clock pulse width positive/negative				600			ns
t_S	Setup time[1]			See Figure 3	300			ns
t_{PD}	(Out data) propagation delay	data out	$\overline{OE}$	See Figure 2		50	200	ns
t_{PD}	(Out $\overline{DR}$) propagation delay	data ready out	8th clock	See Figure 3		700		ns
t_{PD}	(3-State) propagation delay	high impedance o/p	$\overline{OE}$	See Figure 2		60	200	ns
t_{PD}	(DB0) propagation delay	DB0	$\overline{DR}$	See Figure 3			500	ns
t_{PD}	(SDR) $\overline{STRT}$ low to $\overline{DR}$ high	data ready high	$\overline{STRT}$ low	See Figure 3		700		ns

NOTE:
1. See description of "Setup time".

TYPICAL PERFORMANCE CHARACTERISTICS

Internal Clock Frequency vs External Capacitor (C_L)



Conversion Time vs Clock Frequency

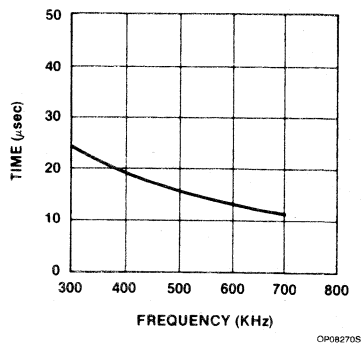
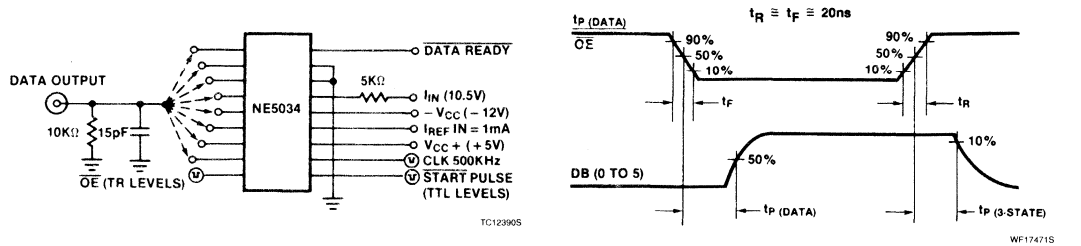
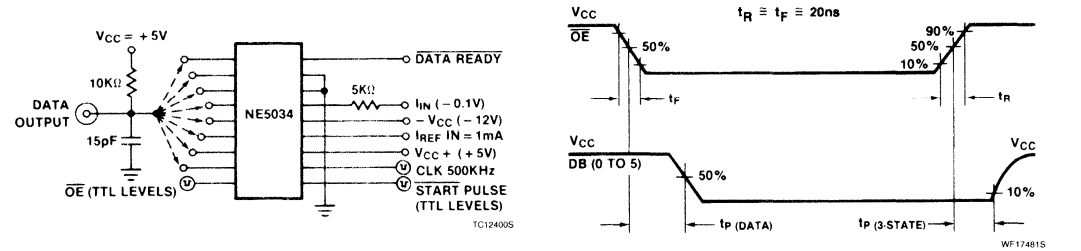


Figure 1

TEST LOAD CIRCUITS



a. Data Output High



b. Data Output Low

Figure 2

FUNCTIONAL PIN DEFINITIONS

DATA READY (DR)

This is an output pin used to indicate that a conversion is in progress. DR goes to a logic "1" when STRT is at a logic "0". At the completion of a conversion DR returns to a logic "0". There is a delay (MAX 0.5μs) from the time DR goes to "0" to the time DB0 data is valid.

DB0 – DB7

Eight 3-State data outputs each with a drive capability of one TTL load. DB0 is the LSB and DB7 is the MSB.

OE

Output enable input. When OE is at a logic "1" the data outputs assume a high impedance state. With OE at a logic "0", data is placed on the outputs. Data appearing on the outputs is only valid if both OE and DR are at logic "0" (see note on DR timing).

STRT

This pin is used to reset the converter and start a new conversion. A logic "0" applied to this pin for a minimum of 400ns will reset the converter to a condition with DB7 at a logic "1" and all other Data outputs at logic "0". It will also cause DR to go to a logic "1" (see timing diagrams for delay times). Conversion will start with the 1st clock pulse after STRT returns to a logic "1" (see notes on setup time required). A STRT pulse while a conversion is taking place will cause the conversion to be aborted and the converter will reset. (See notes on short-cycle operation).

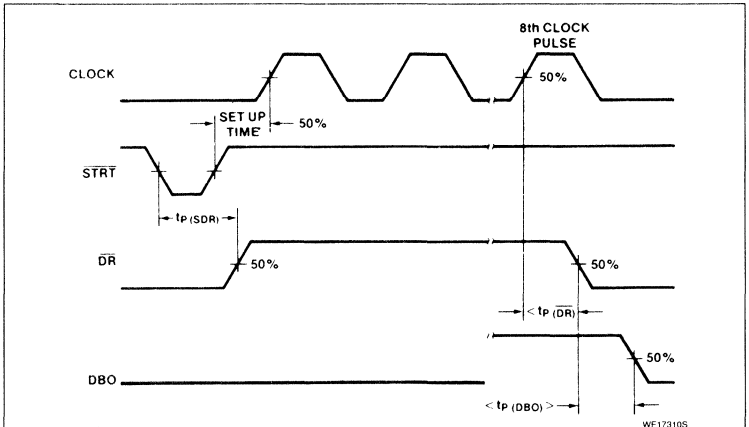


Figure 3

CLK IN

An external capacitor between this pin and ground generates the internal clock pulses. (See diagram for clock frequency vs capacitor value). In order to synchronize the internal clock, to the start pulse a diode (small signal type, e.g., 1N914) should be connected between STRT and CLK IN (see Figures 4 and 5). Without this diode the start pulse could occur at a time which could cause one of the conditions described in the Note on "setup" time. Applying an external TTL- or MOS-compatible clock to this pin slaves the NE5034 to external clock frequency. In this case, the diode is not required but the "set-up" time requirements should be noted.

8-Bit High-Speed A/D Converter NE5034

BASIC CIRCUIT DESCRIPTION

The NE5034 is an 8-bit A/D converter which incorporates the successive-approximation conversion method. Upon receipt of the $\overline{STRT}$ pulse, successive bits, beginning with the MSB (DB7), are applied to the input of the internal 8-bit current output DAC by the I^2L successive-approximation register (SAR) (see Block Diagram).

The comparator determines whether the output current of the DAC is greater or less than the input current converted from the unknown analog input voltage through an external input resistor. If the DAC output current is greater, the data latch for the trial bit is reset to a '0'; if it is less, the trial data bit stays at '1'. After all the bits from DB7 to DB0 have been tried, the SAR contains a valid 8-bit binary output code which accurately represents the unknown analog input to within ± ½LSB (± 0.2%). This binary output will now remain in the SAR until another $\overline{STRT}$ pulse is applied.

During the successive-approximation sequence, the $\overline{DATA\ READY}$ signal remains at '1'. Upon completion of the conversion, the signal goes to a '0', indicating that data is valid and ready. If the $\overline{OE}$ input is left at a '0' during the conversion, the DATA OUTPUT shows the conversion sequence (see short cycle section). When the $\overline{OE}$ line is made a logic '1', the output buffers will go to a high impedance state and will remain so until the $\overline{OE}$ is returned to a '0' state.

TIMING DESCRIPTION

The timing diagram shown in Figure 7 shows the successive trial and decisions for each data bit.

With $\overline{STRT}$ at a logic "0" the converter is reset to a condition with DB7 at a logic "1", DR at a logic "1" and DB0 – DB6 at logic "0".

Conversion starts after $\overline{STRT}$ returns to a logic "1". Starting with DB7 each bit is tried in turn, with the decision point being at the time of the positive-going edge of the clock. Starting with the first positive edge after $\overline{STRT}$ returns to logic "1" (see note on "setup" time). The eighth positive-going edge makes the decision on DB0 (LSB) and also causes $\overline{DR}$ to return to a logic "0" to indicate the conversion is complete. (See note on $\overline{DR}$ timing.)

SHORT-CYCLE OPERATION

In applications where less than 8 bits of resolution are required, the NE5034 can be operated to achieve shorter conversion times. No hard wire changes are required to perform "short-cycling".

Conversion to X number of bits is completed at the end of X + 0.5 clock cycles (after a start pulse) $\overline{DR}$ will still be at a logic "1" state.

$\overline{OE}$ can be used to 3-State the outputs even during short-cycle operation.

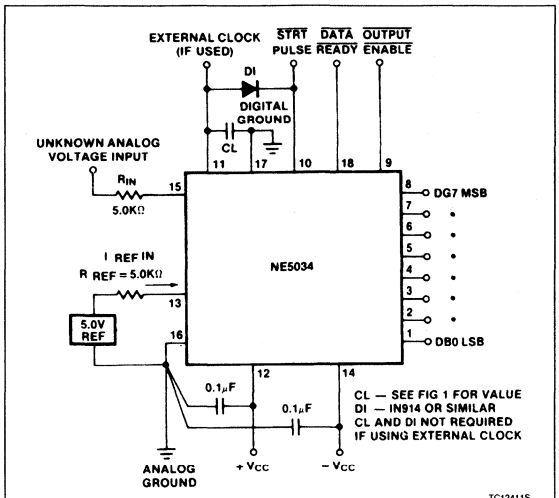


Figure 4. Basic Setup Diagram Unipolar Input Values (0 – 10V)

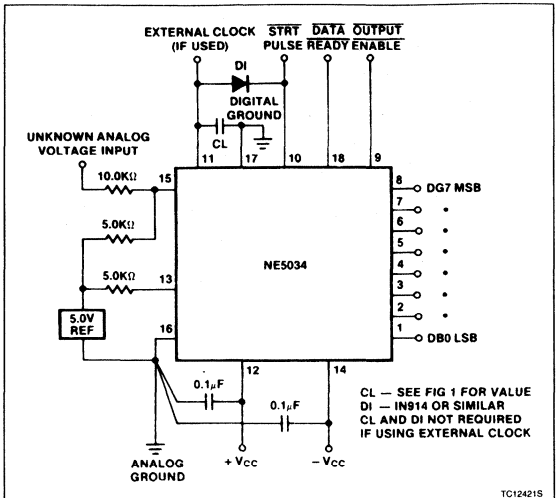


Figure 5. Basic Setup Diagram Bipolar Input Values (± 10V Range)

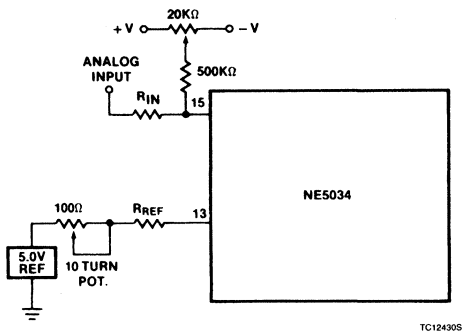


Figure 6. Suggested Zero-/Full-Scale Adjust Circuit

SETUP TIME

When using an external clock, the positive-going edge of the start pulse must be synchronized to the clock pulse. There is a "setup" time of 300ns required between the time of the start pulse returning to a logic "1" and the next positive-going edge of the clock.

If the positive edge of the start pulse occurs less than 300ns prior to the positive clock edge, one of the following conditions will occur:

a) The converter recognizes the clock pulse and converts as normal.

b) The conversion starts one clock pulse later.

c) The conversion never starts. This will be indicated by the fact that $\overline{DR}$ does not return to logic "0". In this case a new start pulse will be required.

DATA READY ($\overline{DR}$) TIMING

After $\overline{DR}$ returns to a logic "0", indicating a conversion is complete, there is a time delay of 500ns before the data at DB0 output (the Least Significant Bit) is valid.

ZERO OFFSET (NEGATIVE FULL-SCALE) CALIBRATION PROCEDURES

1. Apply continuous start pulses to the $\overline{STRT}$ input.
2. Apply ½ LSB in the case of unipolar operation, or ½ LSB above — FS in the case of bipolar operation to the analog input.
3. Observe all data outputs after each conversion is completed.
4. Adjust the potentiometer connected to I_{IN} (see Figure 6) until the LSB flickers between '0' and '1', and all other data outputs remain '0' following each conversion.

FULL-SCALE (POSITIVE FULL-SCALE) CALIBRATION:

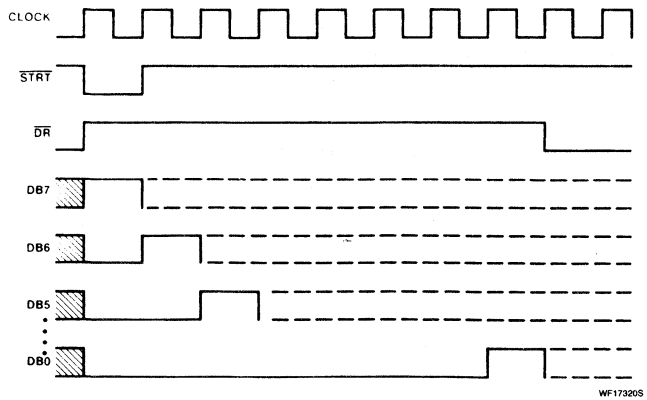
1. Apply continuous start pulses to the $\overline{STRT}$ input.
2. Apply full-scale minus 1½ LSB to the analog input.
3. Observe all data outputs after each conversion is completed.
4. Adjust the voltage applied to V_{REF} in (Figure 4) until the LSB varies between '0' and '1', and all other data outputs stay '1' after each conversion.

NOTES:

1. Where an input of ½ LSB is called for, the voltage is equal to: $\frac{FS}{256}$.
2. The sequence of calibration should be:
   a. Zero offset
   b. Full-scale adjust
   c. Zero offset
   d. Full-scale adjust

OPERATING PRECAUTIONS

Analog and digital grounds should have separate returns. Noise and jitter on digital ground will degrade accuracy unless the input is referenced to a 'clean' analog ground.



NOTES:
1. $\overline{OE}$ = Logic '0'
2. See 'Short-Cycle' section

Figure 7. NE5034 Timing Diagram

UNIPOLAR BINARY OPERATION

A standard connection for a 0 to 10V unipolar binary operation, with $V_{REF\ IN}$ equal to +5V, is shown in Figure 4. The NE5034 can quantize full-scale ranges of 1V to 10V. It should be noted, however, that for smaller full-scale ranges, the accuracy and speed will degrade.

The input voltage versus output code relationship for unipolar operation is shown in Table 1. The full-scale range is 2 times $I_{REF\ IN}$.

Table 1. Unipolar — Binary

ANALOG INPUT 1, 2, 3	DIGITAL OUTPUT CODE MSB LSB
FS – 1 LSB	1 1 1 1 1 1 1 1
FS – 2 LSB	1 1 1 1 1 1 1 0
¾ FS	1 1 0 0 0 0 0 0
½ FS + 1 LSB	1 0 0 0 0 0 0 1
½ FS	1 0 0 0 0 0 0 0
½ FS – 1 LSB	0 1 1 1 1 1 1 1
¼ FS	0 1 0 0 0 0 0 0
1 LSB	0 0 0 0 0 0 0 1
0	0 0 0 0 0 0 0 0

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full-scale; i.e., $2 1_{REF\ IN}$ (Unipolar mode).
3. 1 LSB equals $(2^{-8})(FS)$.
4. "FS" is full-scale; i.e., $I_{REF\ IN}$ (Bipolar mode).

Table 2. Bipolar — Offset Binary

ANALOG INPUT 1, 3, 4	DIGITAL OUTPUT CODE MSB LSB
+(FS – 1 LSB)	1 1 1 1 1 1 1 1
+(FS – 2 LSB)	1 1 1 1 1 1 1 0
+(½ FS)	1 1 0 0 0 0 0 0
+(1 LSB)	1 0 0 0 0 0 0 1
0	1 0 0 0 0 0 0 0
–(1 LSB)	0 1 1 1 1 1 1 1
–(½ FS)	0 1 0 0 0 0 0 0
–(FS – 1 LSB)	0 0 0 0 0 0 0 1
–FS	0 0 0 0 0 0 0 0

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full-scale; i.e., $2 1_{REF\ IN}$ (Unipolar mode).
3. 1 LSB equals $(2^{-8})(FS)$.
4. "FS" is full-scale; i.e., $I_{REF\ IN}$ (Bipolar mode).

BIPOLAR (OFFSET BINARY) OPERATION

A standard connection for a –5 to +5V or –10 to +10V bipolar operation is shown in Figure 5.

NE5036
6-Bit A/D Converter (Serial Output)

Product Specification

DESCRIPTION

The NE5036 is an easy-to-use, low cost, successive-approximation Analog-to-Digital converter, fabricated in Bipolar/I^2L technology, and packaged in a convenient 8-pin miniDIP package.

With an external reference voltage, the NE5036 will accept input voltages between 0V and V_{REF}. Holding the $\overline{START}$ pin low for at least 8 clock pulses in duration will provide the 6-bit result of the conversion in a serial format.

FEATURES

- **Three-state output buffer for easy microprocessor interfacing**
- **Fast successive-approximation converter, 23μs**
- **TTL compatible inputs and outputs**
- **Easy interface to CMOS microprocessors**
- **Guaranteed no missing codes over full operating range**
- **Single supply operation, +5V**
- **High impedance analog inputs**
- **Positive true binary serial output**

APPLICATIONS

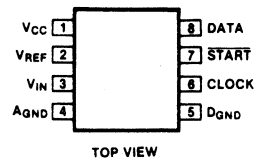
- **Temperature control**
- **μP-based appliances**
- **Light level monitor**
- **Electronic toys**
- **Joystick interface**
- **μP/transducer interface**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Cerdip	0 to +70°C	NE5036FE
8-Pin Plastic DIP	0 to +70°C	NE5036N
14-Pin SO Package	0 to +70°C	NE5036D

PIN CONFIGURATIONS

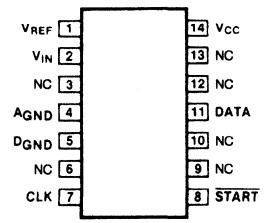
FE, N Packages



TOP VIEW

CD10631S

D^1 Package

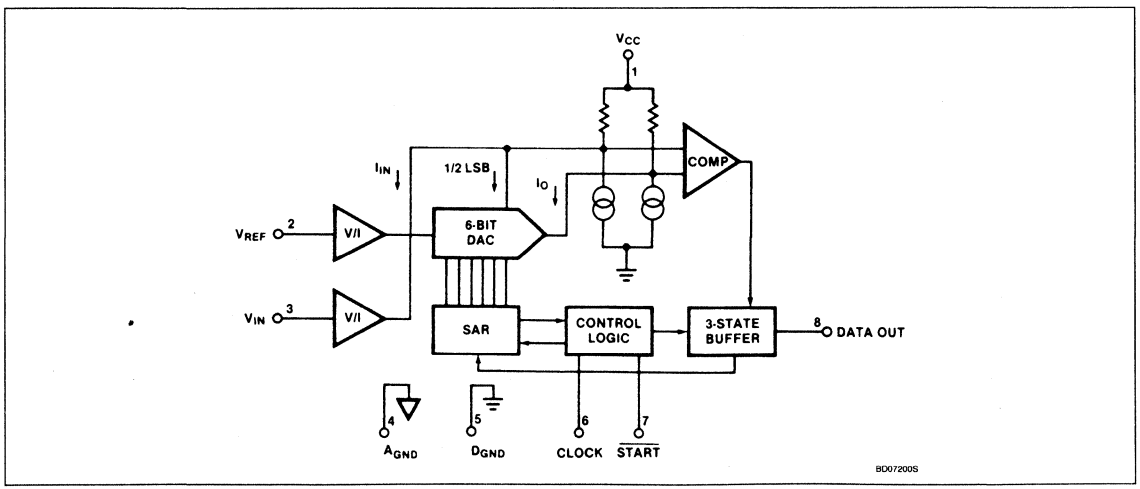


TOP VIEW

CD10641S

NOTE:
1. SO and non-standard pinouts.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN\ (Analog)}$	Analog input voltage	7	V
$V_{IN\ (Digital)}$	Digital input voltage ($\overline{START}$ & CLOCK)	7	V
D_{OUT}	Data output pin 3-State mode Enabled mode	 7 20	 V mA
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	−65 to 150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1] FE package N package D package	 780 1160 1090	 mW mW mW

NOTE:
1. Derate above 25°C at the following rates:
   FE package at 6.0mW/°C.
   N package at 9.3mW/°C.
   D package at 8.3mW/°C.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V; V_{REF} = 2.0V; Clock = 350kHz; 0°C ≤ T_A ≤ 70°C, unless otherwise specified. Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		6	6	6	Bits
	Relative accuracy[1, 2]			¼	½	LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ϵ_{FS}	Full-scale gain error[2, 3, 4]	V_{REF} = 2.0V, T_A = 25°C		±1	±2	LSB
ϵ_{ZS}	Zero-scale offset error[2]	V_{REF} = 2.0V, T_A = 25°C		±½	−½, +2	LSB
PSR	Power supply rejection Max change in full-scale[2]	V_{REF} = 2.0V 4.75V ≤ V_{CC} ≤ 5.5V		±½	±1	LSB
I_{IN}	Analog input bias current	0 ≤ V_{IN} ≤ 2.5V		1	10	μA
I_{REF}	Reference bias current	0 ≤ V_{REF} ≤ 2.5V		1	10	μA
R_{IN}	Analog input resistance		3	30		MΩ
V_{IH}	Logic '1' input voltage		2.0			V
V_{IL}	Logic '0' input voltage				0.8	V
I_{IH}	Logic '1' input current				10	μA
I_{IL}	Logic '0' input current			1	10	μA
I_{OH}	Logic '1' output current	2.4V ≤ V_{OH}	300			μA
I_{OL}	Logic '0' output current	V_{OL} ≤ 0.4V	1.6			mA
I_{OZ}	Three-state leakage current			±0.1	±40	μA
I_{CC}	Positive supply current			14	24	mA
P_D	Power dissipation				132	mW

NOTES:
1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on the straight line drawn from zero-scale to full-scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the bit level which is 1.56% of the full-scale voltage.
3. Full-scale gain error is the deviation of the code transition point (111110 to 111111) from its ideal value (accounting for offset error at 000000).
4. The analog input voltage (V_{IN}) range is from 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance V_{REF} can be any value from 1.5V to 2.5V.)

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V; V_{REF} = 2.0V; Clock = 350kHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C. (Refer to test figures.)

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
f_{MAX}	Max clock frequency			50% duty cycle	350			kHz
t_{CONV}	Conversion time						8	Clock cycles
t_W	Clock pulse width[3]				1.3			μs
t_S	Setup time, $\overline{START}$ to clock[2]	Clock	$\overline{START}$		500			ns
$t_{P\ (OUT)}$	Propagation delay[1]	Data out	Clock	T_A = 25°C, $t_R = t_F$ < 20ns			600	ns
$t_{P\ (3\text{-STATE})}$	Propagation delay[1]	Data (3-State)	$\overline{START}$	T_A = 25°C, $t_R = t_F$ < 20ns			600	ns

NOTES:
1. The time between the specified reference points on the clock and the output waveforms with the output changing (Low-to-High or High-to-Low).
2. The High-to-Low transition of the $\overline{START}$ pulse should occur at least 500ns prior to the negative edge of the clock pulse to insure its recognition. The $\overline{START}$ pulse should stay high for at least 500ns between conversions to guarantee proper recognition.
3. Negative or positive.

CIRCUIT DESCRIPTION

NE5036 is a complete 6-bit, serial output, A/D converter which incorporates the successive approximation method. The chip includes the internal control logic, the successive approximation register (SAR), 6-bit DAC, comparator and the output buffer. An externally-generated clock source (maximum frequency = 350kHz) must be provided to Pin 6. An external reference voltage supplied to Pin 2 sets the full-scale range of the A/D converter as shown in the Block Diagram.

Upon the $\overline{START}$ pin going low, successive approximation conversion commences after the first low-going edge of the clock pulse. Successive bits, beginning with the MSB (D5), are applied to the input of the internal 6-bit current output DAC by the I^2L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to 0 and simultaneously the output buffer goes to 0. If it is less, that bit stays at 1 and the output buffer goes to 1. After the second High-to-Low transition of the clock pulse, the MSB (D5) data is valid. On successive clock pulses, successive bits are tried and the output buffer represents that bit. $\overline{START}$ has to stay low for at least 8 clock pulses for the conversion to be completed and to access the 6-bit result of the conversion. A conversion in process can be interrupted by issuing another $\overline{START}$ pulse.

When $\overline{START}$ is in a high state, the output buffer is in a high impedance state.

The timing diagram for the device is shown in Figure 1.

TRANSFER CHARACTERISTICS

The NE5036 is designed to have a nominal ½ LSB offset, so that the code transition points are located ½ LSB on either side of the exact analog input for a given code. Thus, the first transition (000000 to 000001) will occur at an input of ½ LSB (15.63mV with a V_{REF} of 2.0V), plus any offset. Subsequent transition (to full-scale — 111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

The ideal transfer characteristic of NE5036 is shown in Figure 2.

LAYOUT PRECAUTIONS

Analog ground (Pin 4) and Digital ground (Pin 5) are not connected internally and should be connected together as close to the device as possible for optimum performance. The leads to the analog inputs should be kept as short as possible to minimize input noise pick-up. Input bypass capacitors from the analog inputs to ground will eliminate noise pick-up. Power supplies should be decoupled with at least 1μF and should be located close to the device to minimize the effects of noise spikes on V_{CC}.

The reference input and the analog voltage input must both remain stable during conversion to insure accuracy and proper operation. This can be done by adequately bypassing these inputs and/or keeping the impedance at these inputs at or below 2kΩ.

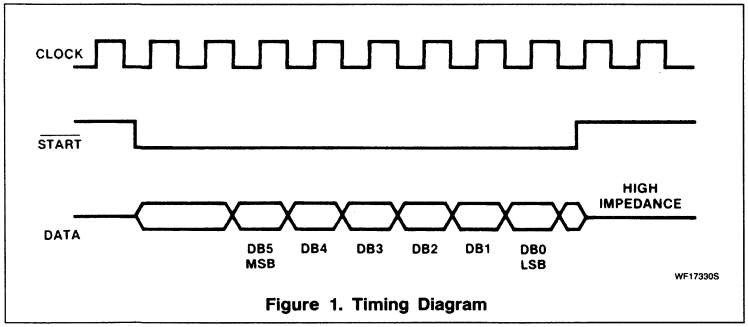


Figure 1. Timing Diagram

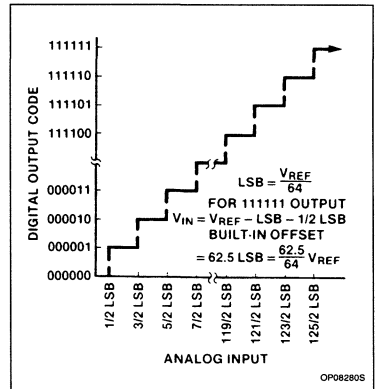
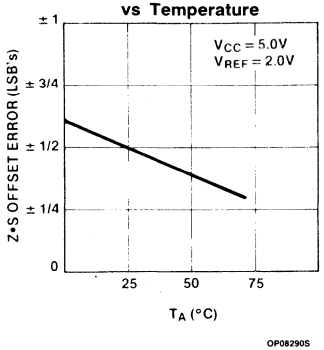


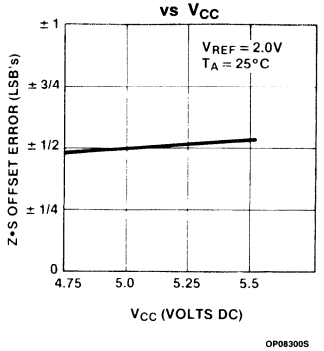
Figure 2. Ideal Transfer Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS

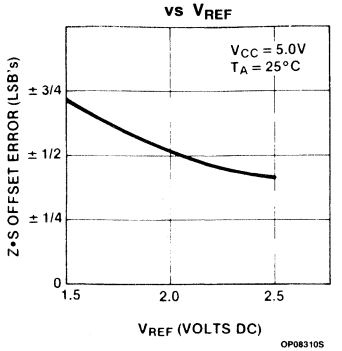
Zero-Scale Offset Error vs Temperature



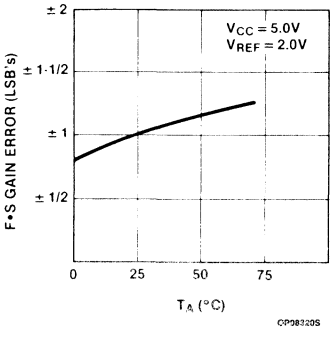
Zero-Scale Offset Error vs V_{CC}



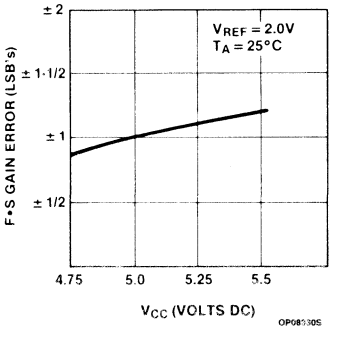
Zero-Scale Offset Error vs V_{REF}



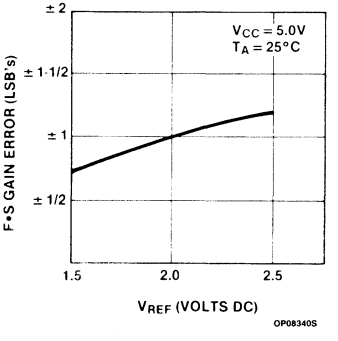
Full-Scale Gain Error vs Temperature



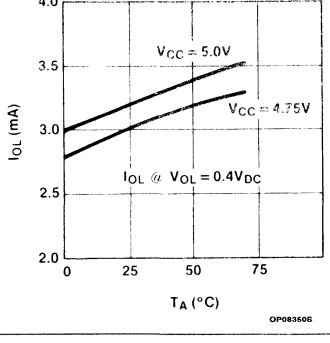
Full-Scale Gain Error vs V_{CC}



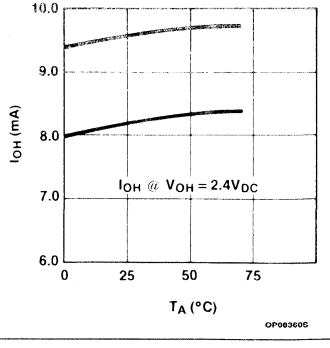
Full-Scale Gain Error vs R_{REF}



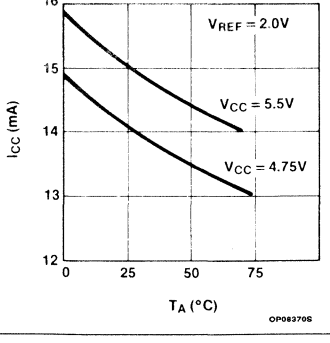
I_{OL} vs Temperature (Data Output)



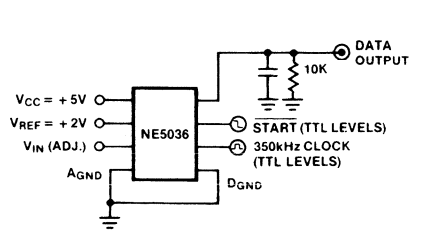
I_{OH} vs Temperature (Data Output)



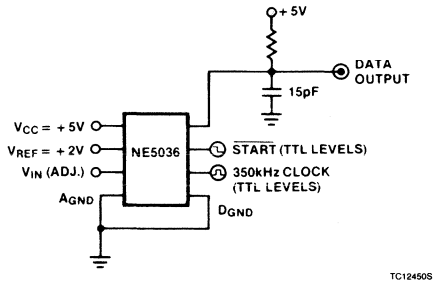
I_{CC} vs Temperature



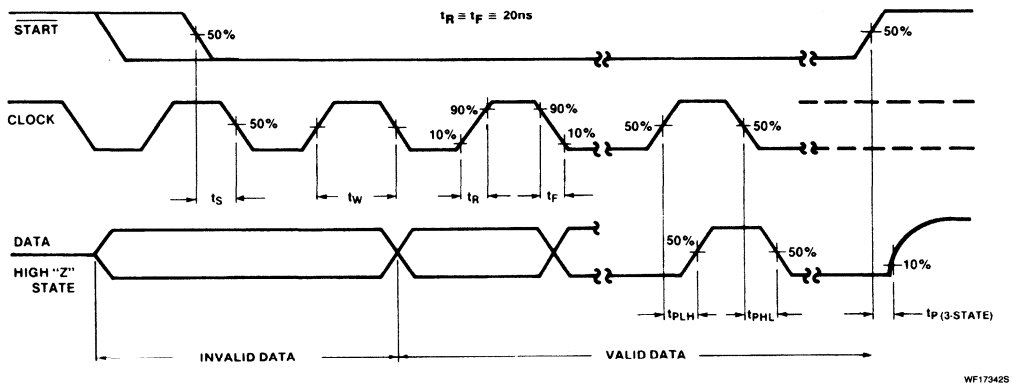
AC TEST CIRCUITS AND WAVEFORMS



Data Output (Low-to-High)

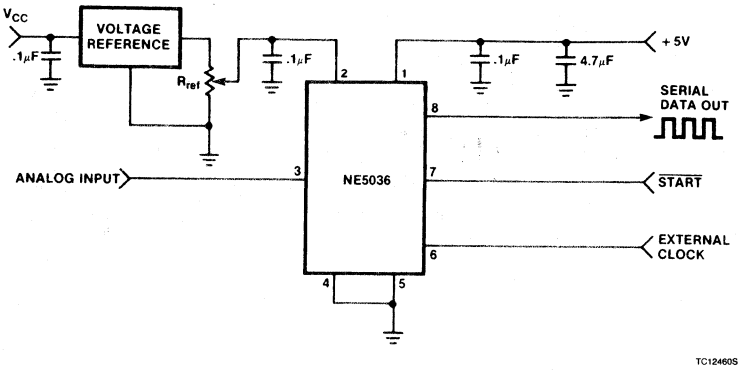


Data Output (High-to-Low)

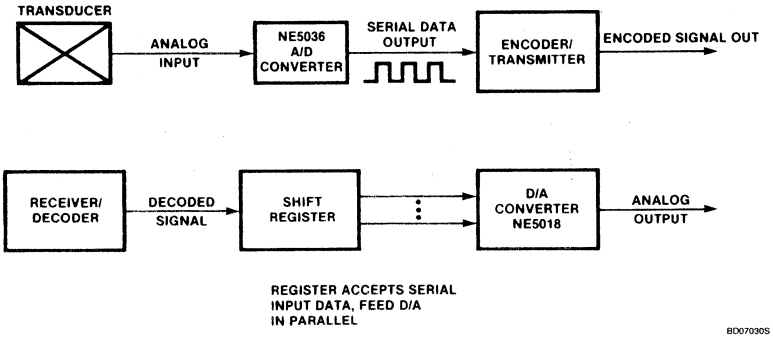


Propagation Delay Time t_P (Data)

TYPICAL APPLICATIONS



1. Basic NE5036 Configuration



2. Digital Communications Using NE5036

NE5037
6-Bit A/D Converter (Parallel Outputs)

Product Specification

DESCRIPTION

The NE5037 is a low cost, complete successive-approximation analog-to-digital (A/D) converter, fabricated using Bipolar/I^2L technology. With an external reference voltage, the NE5037 will accept input voltages between 0V and V_{REF}. An external $\overline{START}$ pulse of at least 300ns in duration will provide the 6-bit result of the conversion in parallel format. Full conversion with no missing codes occurs in 9μs.

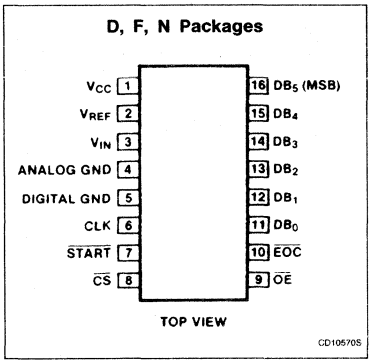
FEATURES

- **TTL-compatible inputs and outputs**
- **3-State output buffer**
- **Easy interface to CMOS microprocessors**
- **Fast conversion — 9μs**
- **Guaranteed no missing codes over full temp range**
- **Single-supply operation, +5V**
- **Positive true binary outputs**
- **High-impedance analog inputs**

APPLICATIONS

- **Temperature control**
- **μP-based appliances**
- **Light level monitors**
- **Head position sensing**
- **Electronic toys**
- **Joystick interface**

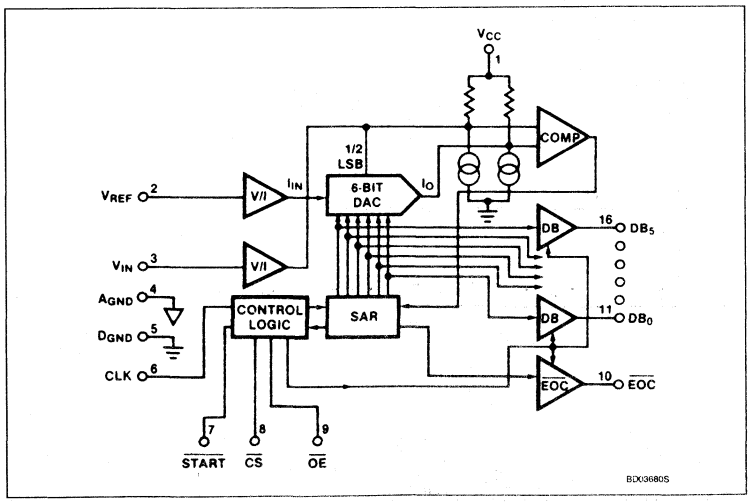
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE5037F
16-Pin Plastic DIP	0 to +70°C	NE5037N
16-Pin Plastic SO package	0 to +70°C	NE5037D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN(Analog)}$	Analog input voltage	7	V
$V_{IN(Digital)}$	Digital input voltage ($\overline{CS}$, $\overline{OE}$, $\overline{START}$, CLK)	7	V
D_{OUT}	Data outputs (DB0 to DB5) 3-state mode Enabled mode (each output)	 7 5	 V mA
$\overline{EOC}$	End of conversion	V_{CC}	
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	−65 to 150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1] F package N package D package	 1190 1450 1090	 mW mW mW

NOTE:

1. Derate above 25°C at the following rates:
   F package = 9.5mW/°C.
   N package = 11.6mW/°C.
   D package = 8.7mW/°C.

6-Bit A/D Converter (Parallel Outputs) NE5037

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V; V_{REF} = 2.0V; Clock = 1MHz; 0°C ≤ T_A ≤ 70°C, unless otherwise specified. Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		6	6	6	Bits
	Relative accuracy[1,2]			¼	½	LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ϵ_{FS}	Full-scale gain error[2,3,4]	V_{REF} = 2.0V, T_A = 25°C		± 1	± 2	LSB
ϵ_{ZS}	Zero-scale offset error[2]	V_{REF} = 2.0V, T_A = 25°C		± ½	−½, +2	LSB
PSR	Power supply rejection	V_{REF} = 2.0V		± ½	± 1	LSB
	Max change in full-scale[2]	4.75V ≤ V_{CC} ≤ 5.5V				
I_{IN}	Analog input bias current	0 ≤ V_{IN} ≤ 2.5V		1	10	μA
I_{REF}	Reference bias current	0 ≤ V_{REF} ≤ 2.5V		1	10	μA
R_{IN}	Analog input resistance		3	30		MΩ
V_{IH}	Logic '1' input voltage		2.0			V
V_{IL}	Logic '0' input voltage				0.8	V
I_{IH}	Logic '1' input current				10	μA
I_{IL}	Logic '0' input current			1	10	μA
I_{OH}	Logic '1' output current[5]	2.4V ≤ V_{OH}	300			μA
I_{OL}	Logic '0' output current[5]	V_{OL} ≤ 0.4V	1.6			mA
I_{OZ}	3-State leakage current			± 0.1	± 40	μA
I_{CC}	Positive supply current			18	24	mA
P_D	Power dissipation				132	mW

NOTES:

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero-scale to full-scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the 6-bit level which is 1.56% of the full-scale voltage.
3. Full-scale gain error is the deviation of the full-scale code transition point (111110 to 111111) from its ideal value.
4. The analog input voltage (V_{IN}) range is 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance, V_{REF} can be any value from 1.5V to 2.5V.)
5. The data outputs have active pull-ups. The $\overline{EOC}$ line is open-collector with a nominal 5kΩ internal pull-up resistor.

AC ELECTRICAL CHARACTERISTICS

V_{CC}=5.0V; V_{REF}=2.0V; Clock=1MHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C. (Refer to AC test figures.)

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
f_{MAX}	Maximum clock frequency				1			MHz
t_W	Start pulse width				300			ns
	Minimum positive/negative clock pulse width				300			ns
t_{CONV}	Conversion time						9	Clock cycles
$t_{P\ (OUT\ DATA)}$	Propagation delay[1]	Data out	$\overline{OE}$	T_A = 25°C, t_R = t_F ≤ 20ns			500	ns
$t_{P\ (OUT\ EOC)}$	Propagation delay[2]	$\overline{EOC}$	Clock	T_A = 25°C, t_R = t_F ≤ 20ns			800	ns
$t_{P\ (3\text{-}STATE)}$	Propagation delay, 3-State	3-State Data	$\overline{OE}$	T_A = 25°C, t_R = t_F ≤ 20ns			500	ns

NOTES:

1. Propagation delay of data outputs is defined as the delay in the data outputs reading their final value after the low going edge of $\overline{OE}$.
2. Propagation delay of $\overline{EOC}$ is defined as the delay in $\overline{EOC}$ going low, following the low going edge of the 9th clock pulse after the start pulse.

CIRCUIT DESCRIPTION

NE5037 is a complete 6-bit, parallel output, microprocessor compatible, A/D converter which incorporates the successive-approximation method. The chip includes the internal control logic, the successive-approximation register (SAR), 6-bit DAC, comparator and output buffers. An externally-generated clock source (max frequency = 1MHz) must be provided to Pin 6. An external reference voltage supplied to Pin 2 sets the full-scale range of the A/D converter.

The $\overline{CS}$ pin must be at a low level prior to the start of the conversion process. Upon receipt of a $\overline{START}$ pulse, the internal control logic resets the SAR. On the first low-going edge of the clock pulse, successive approximation conversion commences. Successive bits beginning with the MSB (D5) are supplied to the input of the internal 6-bit current output DAC by the I^2L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, which is converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to '0' and the corresponding output buffer goes to '0' simultaneously. If it is less, it stays at '1' and the output buffer also stays at '1'. On successive clock pulses, successive bits of the DAC are tried and the corresponding output buffer represents the bits of the DAC. On the eighth low-going edge of the clock pulse (after the receipt of the start pulse), the $\overline{EOC}$ pin goes low, thereby indicating that the conversion is complete. The output data is now valid. In order to access the result of the conversion, the $\overline{OE}$ pin must be set to a low level. $\overline{EOC}$ is reset to a high state when $\overline{OE}$ is low. When $\overline{OE}$ is in a '1' state, the output buffers are in a high impedance state.

Refer to Figure 1 for the timing diagram.

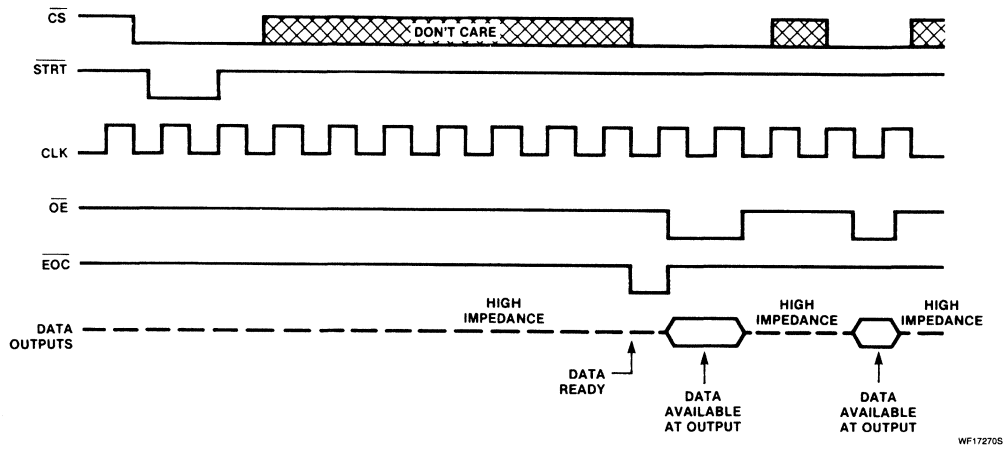


Figure 1. Timing Diagram

TRANSFER CHARACTERISTICS

The ideal transfer characteristic of the NE5037 is shown in Figure 2.

The NE5037 is designed to have a nominal ½ LSB offset so that the code transition points are located ½ LSB on either side of the exact analog inputs for a given code.

Thus the first transition (000000 to 000001) will occur at an input of ½ LSB (15.63mV with a V_{REF} of 2.0V). Subsequent transitions will occur at nominal increments of 1 LSB. The last transition (to full-scale — 111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

LAYOUT PRECAUTIONS

Analog ground (Pin 4) and digital ground (Pin 5) are not connected internally and should be connected together as close to the device as possible for optimum performance. The circuit will operate with as much as ±200mV between the two grounds but some degradation will occur. The leads to the analog inputs should be kept as short as possible to minimize noise pick-up. Input bypass capacitors from the analog inputs to ground will eliminate noise pick-up. Power supplies should be decoupled with at least 1μF located close to the device to minimize the effects of noise spikes.

The reference input and the analog voltage input must both remain stable during conversion to insure accuracy and proper operation. This can be done by adequately bypassing these inputs and/or keeping the impedance of these inputs at or below 2kΩ.

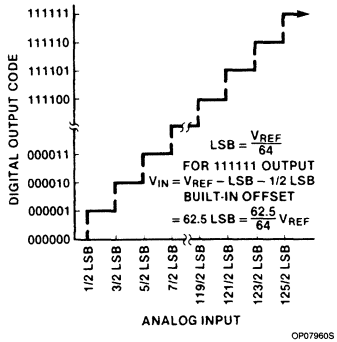
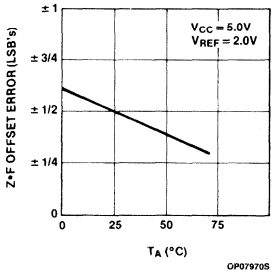


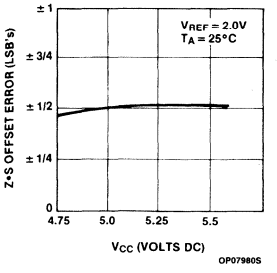
Figure 2. Ideal Transfer Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS

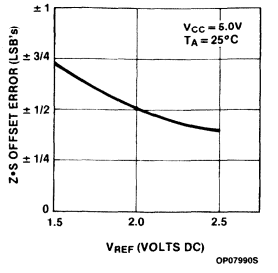
Zero-Scale Offset Error vs Temp



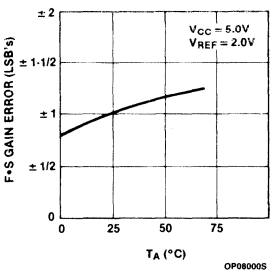
Zero-Scale Offset Error vs V_{CC}



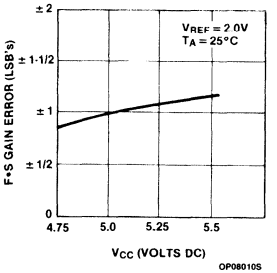
Zero-Scale Offset Error vs V_{REF}



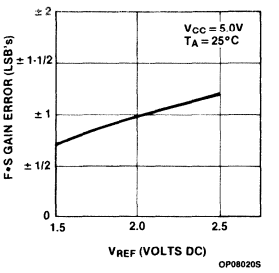
Full-Scale Gain Error vs Temp



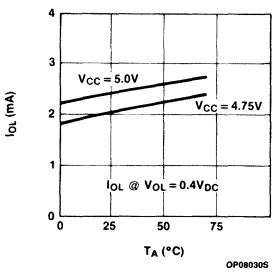
Full-Scale Gain Error vs V_{CC}



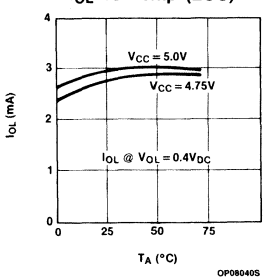
Full-Scale Gain Error vs V_{REF}



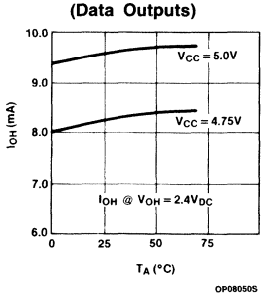
I_{OL} vs Temp (Data Outputs)



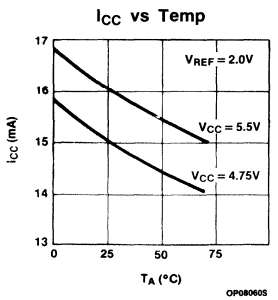
I_{OL} vs Temp ($\overline{EOC}$)



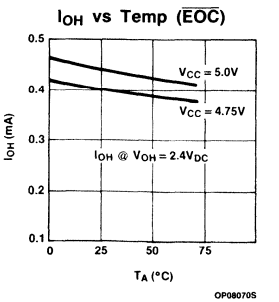
I_{OH} vs Temp (Data Outputs)



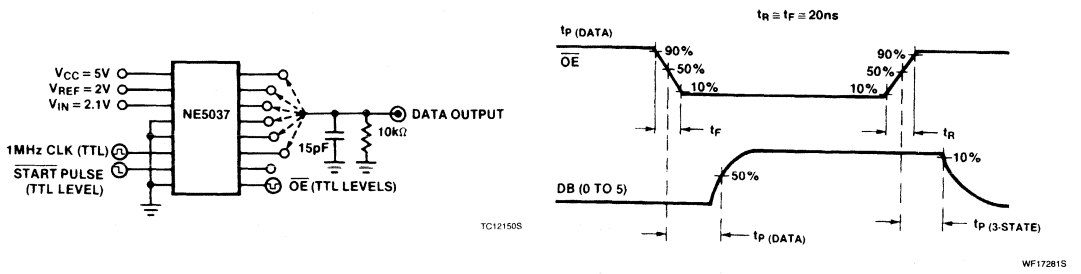
I_{CC} vs Temp



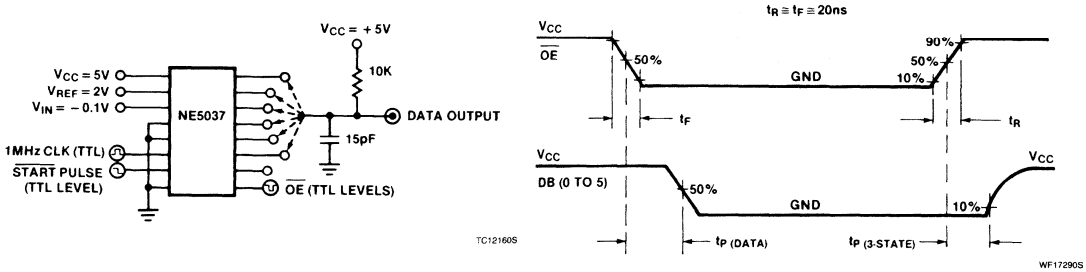
I_{OH} vs Temp ($\overline{EOC}$)



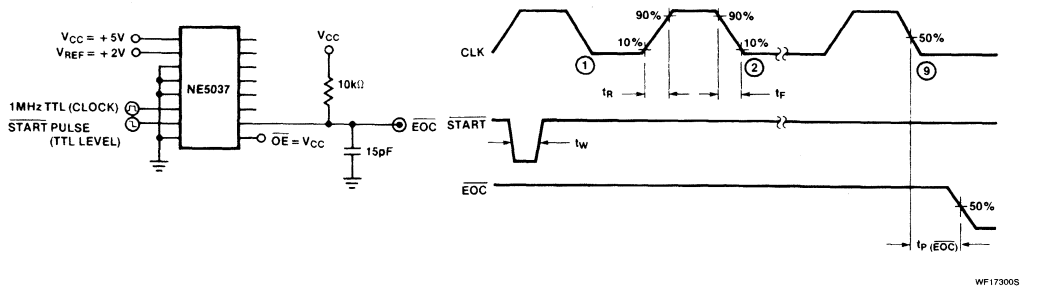
AC TEST CIRCUITS AND WAVEFORMS



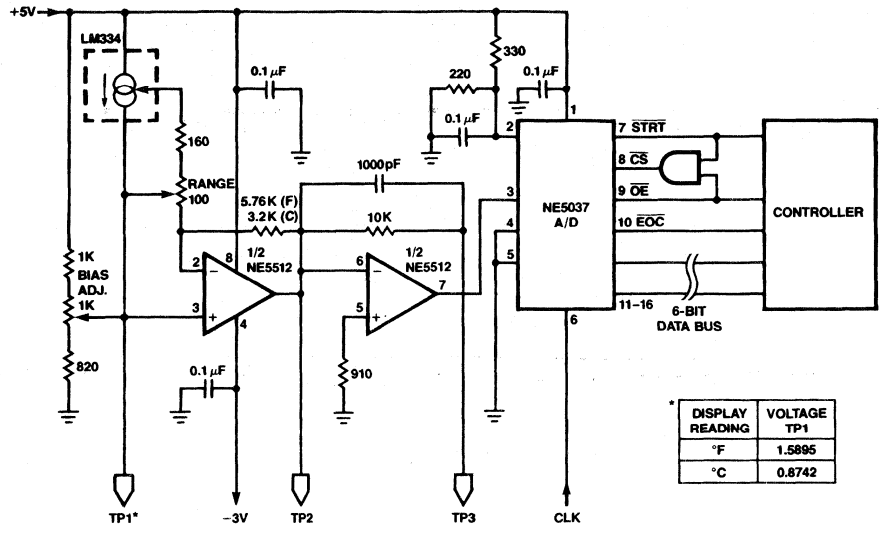
Propagation Delay Time $t_{P(Data)}$ and $t_{P(3\text{-State})}$



Data Output High



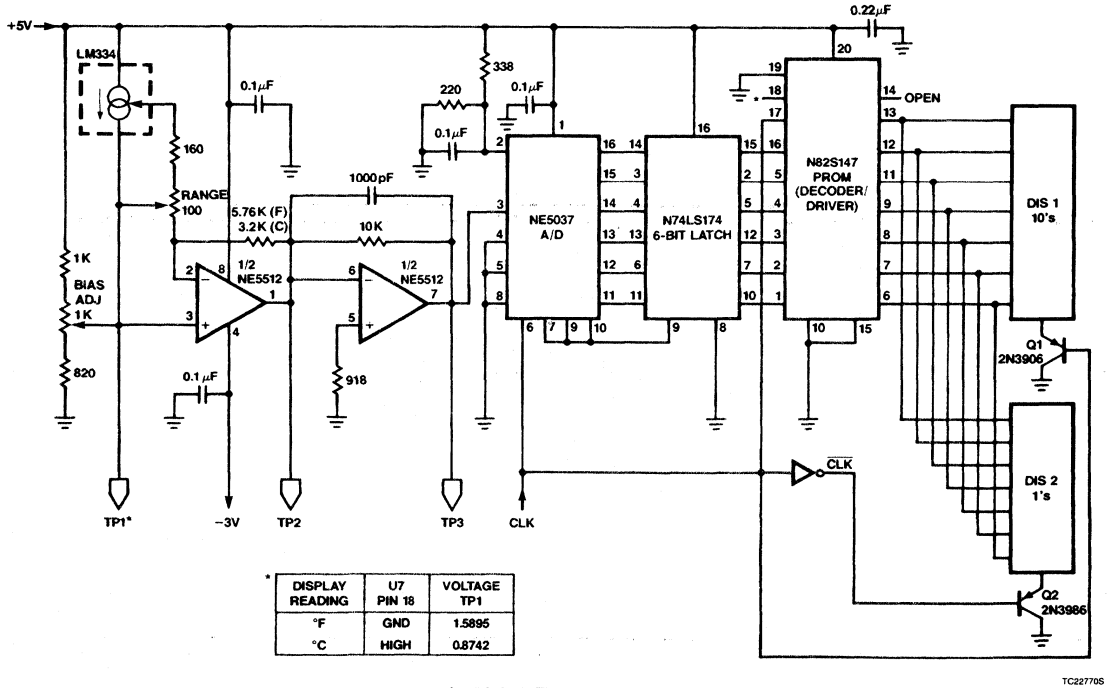
Propagation Delay Time EOC $t_{P(EOC)}$



* DISPLAY READING	VOLTAGE TP1
°F	1.5895
°C	0.8742

TC22760S

a. Temperature Sensor



* DISPLAY READING	U7 PIN 18	VOLTAGE TP1
°F	GND	1.5895
°C	HIGH	0.8742

TC22770S

b. Digital Thermometer

Figure 3

6-Bit A/D Converter (Parallel Outputs)

NE5037

APPLICATION

- **0 to 63°C Temperature Sensor**

CIRCUIT DESCRIPTION

The temperature sensor of Figure 3 provides an input to Pin 3 of the NE5037 of 32mV/°C. This 32mV is the value of one LSB for the NE5037. The LM334 is a three-terminal temperature sensor and provides a current of 1μA for each °Kelvin. The first section of the dual opmp is connected as a trans-impedance afplifier to convert the current from the LM334 to a voltage, which is amplified and inverted by the section amplifier. Note that the first amplifier requires different values of feedback resistance for °C and °F. The NE5512 was chosen for its low temperature coefficient of input bias current as excessive I_{OS} tempco would degrade temperature tracking.

To read temperature, conversion is started by sending a momentary low signal to Pin 7 of the NE5037. When Pin 10 of the NE5037 goes low, conversion is complete and a low is applied to Pin 9 of the NE5037 to read data on Pins 11 through 16. Note that this temperature data is in straight binary format.

The controller can be a microprocessor in a temperature control application, or discrete circuitry in a simple temperature reporting application. A temperature reporting (digital thermometer) circuit is shown in Figure 3b. The NE5037 A/D converter is connected in a continuous conversion mode by connecting together Pins 7, 9, and 10. Should this pin be momentarily shorted to any relatively low impedance point, conversion will stop. Conversion will resume upon interruption and restoration of the power. These pins are also connected to the latch enable of a 6-bit latch because the data at the converter output is available for only a short time when the converter is in the continuous conversion mode. The (P)ROM) must have the correct code for converting the data from the NE5037 (used as address for the (P)ROMs) to the appropriate segment drive codes. Note that the circuit of Figure 3b shows a circuit which can be used to display either Fahrenheit or Centigrade temperatures.

The displayed output could easily be converted to degrees Fahrenheit (°F) by the controller of Figure 3a or through the (P)ROMs of Figure 3b. When doing this, a third (hundreds) digit (P)ROM and display will be needed for displaying temperatures above 99°F.

An inexpensive clock can be made from NAND gates or inverters, as shown in Figure 3c.

CIRCUIT ADJUSTMENT

The circuit should be at a known ambient temperature for a few minutes before making adjustments.

1. Adjust bias adjust potentiometer for the voltage indicated in the chart in Figure 3b.
2. With the circuit (or sensor U3, if it is remotely located) at a known temperature for 2 to 3 minutes, adjust range control for a correct reading on the displays.

This should provide an accuracy of ± 3 counts (3° F or C). Higher accuracy may require NE5037 reference voltage regulation.

DACs

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MC3410C	10-bit high-speed multiplying DAC	504
MC3510	10-bit high-speed multiplying DAC	504
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NE5019	8-bit microprocessor-compatible DAC	518
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AN101
Applying the DAC08

Application Note

Reference Amplifier Setup

The DAC08 Series are multiplying D-to-A converters in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full-scale output current is a linear function of the reference current and is given by this equalization where $I_{REF} = I_{14}$.

$$I_{FS} = \frac{255}{256} \times I_{REF}$$

In positive reference applications shown in Figure 1, an external positive reference voltage forces current through R14 into the V_{REF} (+) terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to V_{REF} (−) at Pin 15, shown in Figure 2. Reference current flows from ground through R14 into $V_{REF}(+)$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. R15 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15 as shown in Figure 3. The negative common-mode range of the reference amplifier is given by the following equation:

$$V_{CM^-} = V- + (I_{REF} \cdot 1k\Omega) + 2.5V$$

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into 2 resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a +10.0V reference is recommended for optimum full-scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications, the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full-scale trimming which eliminates potentiometer TC effects is shown in Figure 4.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from Pin 16 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications".

Multiplying Operation

The DAC08 Series provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA.

Reference Amplifier Compensation for Multiplying Applications

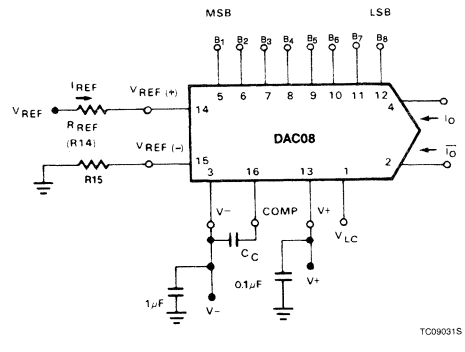
AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 16 to V−. The value of this capacitor depends on the impedance presented to Pin 14. For R14 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37 and 75pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

For fastest multiplying response, low values of R14 enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the preceding values will suffice and the amplifier must be heavily compensated, which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and CC = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to I_{REF} = 2mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme shown in Figure 5. This technique provides lowest full-scale transition times. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at Pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16mA/μs, which is relatively independent of R_{IN} and V_{IN} values.

Logic Inputs

The DAC08 design incorporates a logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −11V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC08 is pow-



NOTES:

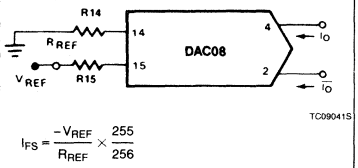
$I_{FS} \approx + \frac{V_{REF}}{R_{REF}} \times \frac{255}{256}$ $I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation typical values are:
V_{REF} = +10.000V, R_{REF} = 5,000Ω, R15≈R_{REF},
C_C = 0.01μF, V_{LC} = 0V(ground)

Figure 1. Basic Positive Reference Operation

ered from a +5V supply. Minimum input logic swing is given by the following equation:

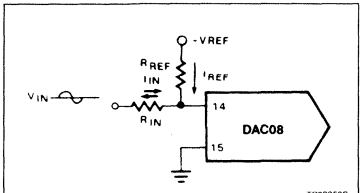
$$V- + (I_{REF} \cdot 1k\Omega) + 2.5V$$



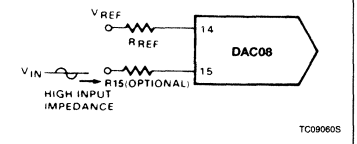
$$I_{FS} = \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

R_{REF} sets I_{FS}, R15 is for bias current cancellation.

Figure 2. Basic Negative Reference Operation



$I_{REF} \geq$ Peak Negative Swing of I_{IN}



$+V_{REF}$ must be above Peak Positive Swing of V_{IN}

Figure 3. Accomodating Bipolar References

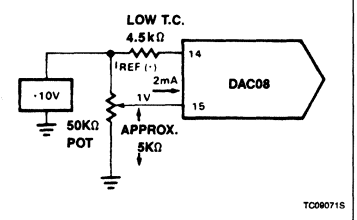


Figure 4. Recommended Full-Scale Adjustment Circuit

The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control in (Pin 1, V_{LC}). Figure 6 shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground Pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see Figure 7. For general setup of the logic control circuit, it should be noted that Pin 1 may source up to 200μA. External circuitry should be designed to accommodate this current.

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

Analog Output Currents

Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FS}$. Current appears at the true output when a 1 is applied to each logic input. As the binary count increases, the sink current at Pin 4 increases proportionally, in the fashion of a positive logic D-to-A converter. When a 0 is applied to any input bit, that current is turned off at Pin 4 and turned on at Pin 2. A decreasing logic count increases I_O as in a negative or inverted logic D-to-A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}. Do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V- and is independent of the positive supply. Negative compliance is given by the equation:

$$V- + (I_{REF} \cdot 1k\Omega) + 3.0V$$

Note that lower values of I_{REF} will allow a greater output compliance.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as balanced-bridge A/D circuits, as well as driving center-tapped coils and transformers.

Power Supplies

The DAC08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq$ 1mA is recommended.

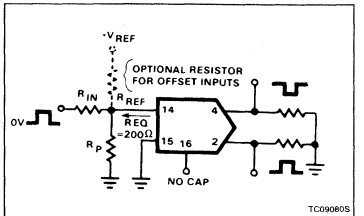


Figure 5. Pulsed Reference Operation

Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range. Consult the various figures for guidance. For example, operation at -4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible; however, at least 8V total must be applied between Pins 2 and 4, and Pin 3 to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.

Power consumption may be calculated by this equation:

$$P_D = (I+)(V+) + (I+)(V-) + (I_{REF})(V-)$$

A useful feature of the DAC08 design is that supply current is constant and independent of input logic states. This is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

Temperature Performance

The linearity and monotonicity specifications of the DAC08 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is low, typically ±10ppm/°C with zero-scale output current and drift essentially negligible compared to ½ LSB.

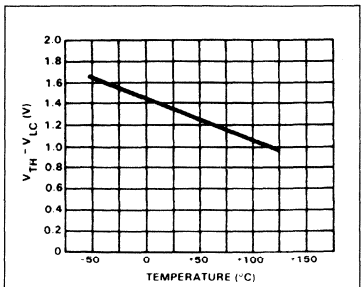


Figure 6. $V_{TH} - V_{LC}$ vs Temperature

Full-scale output drift performance will be best with +10.0V references, as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift.

Settling times of the DAC08 decrease approximately 10% at −55°C, and an increase of about 15% at +125°C is typical.

Settling Time

The DAC08 is capable of extremely fast settling times (typically 70ns at I_{REF} = 2.0mA).

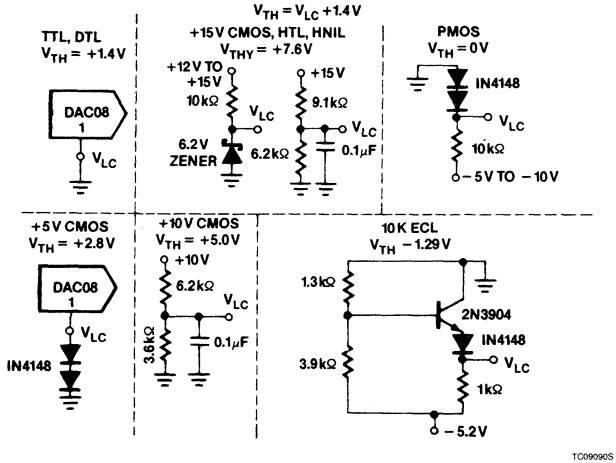
Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 8 bits. Settling time to within ½ LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 70ns, thus determining the overall settling time of 70ns. Settling to 6-bit accuracy requires about 55 to 60ns. The output capacitance, including the package, is approximately 15pF. Therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4μA. Therefore, a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Figure 8 uses a cascode design to permit driving a 1kΩ load with less than 5pF of parasite capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value; thus, settling time may be observed at lower values of I_{REF}.

The DAC08 switching transients or glitches are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is dependent of input logic states. 0.1μF capacitors at the supply pins provide full transient performance.



NOTE:
Do not exceed negative logic input range of DAC

Figure 7. Interfacing With Various Logic Families

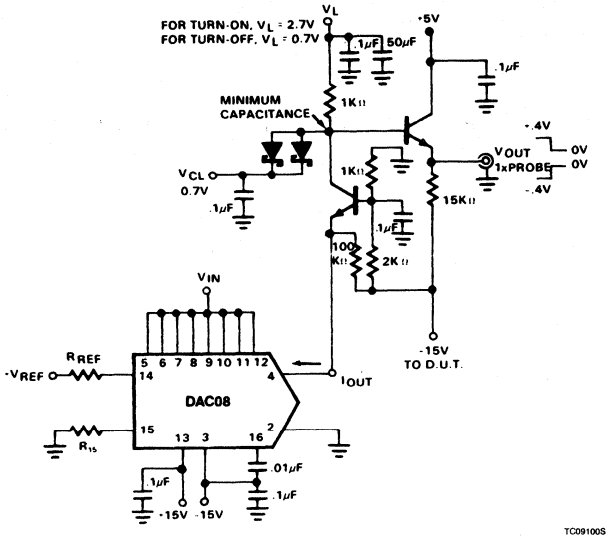
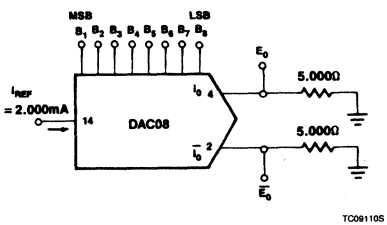


Figure 8. Settling Time Measurement

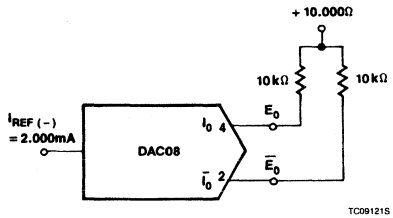
TYPICAL APPLICATIONS



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	I_O (mA)	$\overline{I_O}$ (mA)	E_O	$\overline{E_O}$
Full-scale	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	0.000
Full-scale – LSB	1	1	1	1	1	1	1	0	1.984	0.008	-9.920	-0.040
Half-scale + LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
Half-scale	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
Half-scale – LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
Zero-scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
Zero-scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

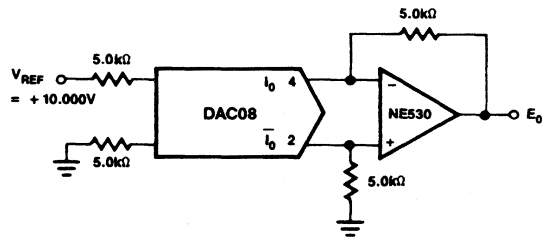
Figure 9. Basic Unipolar Negative Operation

TYPICAL APPLICATIONS (Continued)



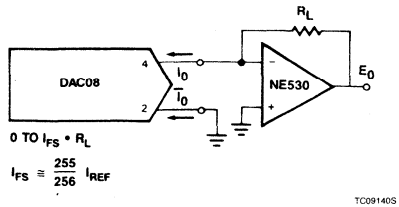
	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O	$\overline{E_O}$
Pos full-scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos full-scale − LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero-scale + LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero-scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero-scale − LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg full-scale + LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg full-scale	0	0	0	0	0	0	0	0	+10.000	−9.920

Figure 10. Basic Bipolar Output Operation



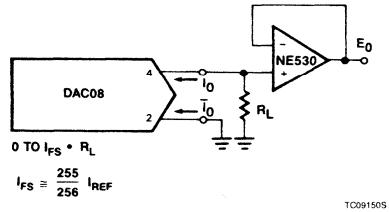
	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O
Pos full-scale	1	1	1	1	1	1	1	1	+9.920
Pos full-scale − LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero-scale	1	0	0	0	0	0	0	0	+0.040
(−) Zero-scale	0	1	1	1	1	1	1	1	−0.040
Neg full-scale + LSB	0	0	0	0	0	0	0	1	−9.840
Neg full-scale	0	0	0	0	0	0	0	0	−9.920

Figure 11. Symmetrical Offset Binary Operation



NOTE:
For complementary output (operation as negative logic DAC), connect inverting input of op amp to I_O (Pin 2); connect $\overline{I_O}$ (Pin 4) to ground.

Figure 12. Positive Low Impedance Output Operation



NOTE:
For complementary output (operation as a negative logic DAC), connect non-inverting input of op amp to I_O (Pin 2); connect $\overline{I_O}$ (Pin 4) to ground.

Figure 13. Negative Low Impedance Output Operation

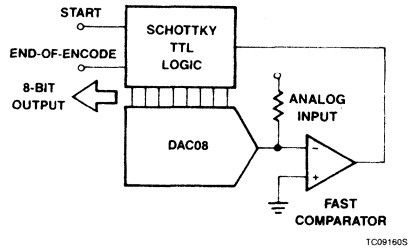
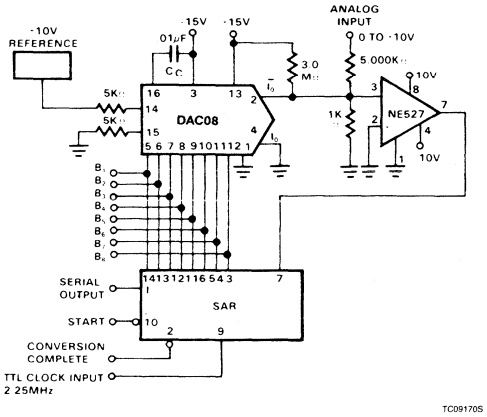
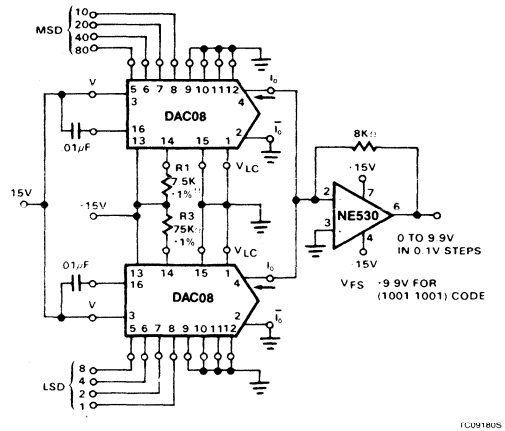


Figure 14. Low Cost 8-Bit 1μs A-to-D Converter



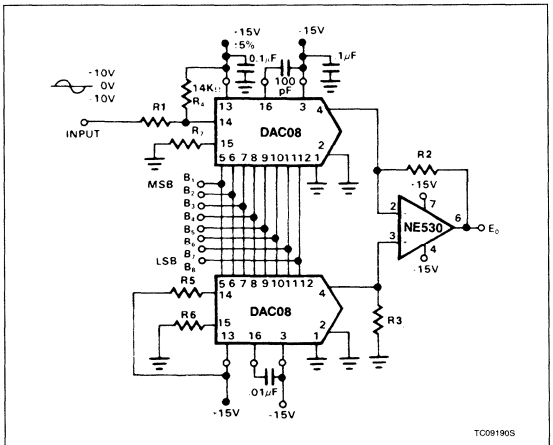
NOTE:
Connect "start" to "conversion complete" for continuous conversions.

Figure 15. 3 IC Low Cost A-to-D Converter



NOTE:
Output is directly proportional to positive power supply.

Figure 16. Low Cost 2-Digit BCD DAC



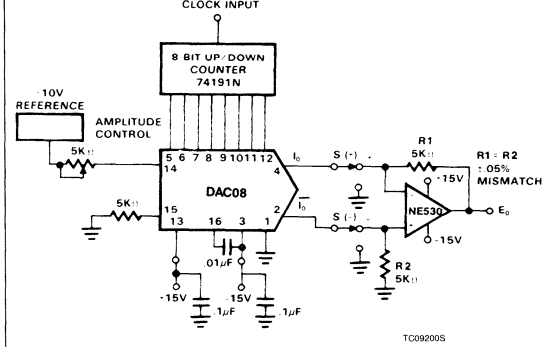
Bipolar input offset binary output

Performs 2 quadrant multiplications — AC input controls output polarity.

NOTES:
1. R1 = R2 = R3
2. R4 = R5
3. E_O DC to 20kHz = ± 5V
4. E_O DC to 10kHz = ± 10V

Figure 17. DC-Coupled Digital Attenuator/ Programmable Gain Amplifier

OUTPUT TYPE (E_0)	SWITCH S(+)	CONDITIONS S(-)
Unipolar positive	+	GND
Unipolar negative	GND	-
Bipolar	+	-



NOTES:
1. Bipolar output is symmetrical around zero, adjustable peak-to-peak amplitude.
2. For triangle wave, count up to full, reverse and count down.
3. For positive-going sawtooth, count up to full, clear, repeat.
4. For negative-going sawtooth, count down, clear, repeat.
5. For other waveforms, use a ROM programmed with the desired function.

Figure 18. High-Speed Waveform Generator

AN105
Digital Attenuator

Application Note

Figure 1 shows a DC-coupled Digital Attenuator or Programmable Gain Amplifier.

Pin 14 of the DAC is a Virtual Ground. Current must always flow into Pin 14, so the current through R4 must be greater than that through R1 when the input signal is at its most negative usable value. If the input signal value goes low enough to cause the current through R1 to be greater than that through R4, output clipping will occur.

To extend the operating frequency range, the compensation cap, C_C, needs to be minimized, which implies that the resistance at Pin 14 (R1 and R4) must be minimized. If the voltage to which R4 and R5 are returned has any noise on it at all, R4 and R5 should be formed of two series resistors with the junction of them bypassed with 0.1μF to ground. Pin 15 could be grounded with a small sacrifice in accuracy and temperature drift. R6 and R7 compensate for reference amplifier input offset.

R1 and R4 should be chosen such that, when the input is at peak usable signal, the total current into Pin 14 does not exceed 4mA. When the input is most negative, R1 current must be less than R4 current (remember, Pin 14 is always at 0V). Also, when the input is at its absolute positive peak value, current into Pin 14 should not exceed 5mA. Minimum compensation capacitor, (C_C), in pF is 15 times the parallel combination of R1 and R4 in kΩ.

With a single DAC, there is a DC offset at the circuit output that varies with the digital word input. To eliminate this, we use a second DAC to subtract this offset at the sum node of the op amp.

Example 1: Input signal is to be $20V_{P-P}$, centered at 0V. Maximum input frequency is to be 15kHz. Power supplies available are $\pm$ 15V, both regulated. Determine values of all resistors for maximum gain of unity.

Solution 1: At minimum input (−10V), reference current, I_{REF} is

$$I_{REF} = \frac{15V}{R4} + \frac{(-10V)}{R1}$$

If minimum $I_{REF} = 0$, then

$$\frac{15V}{R4} = \frac{10V}{R1}$$

and $R4 = (1.5)(R1)$

Therefore, 60% of I_{REF} comes through R4. If we let I_{REF} go to about 3.9mA (4mA is max. recommended), R4 current is found to be $I_{R4} = (0.6)\ (3.9mA) = 2.34mA$ and R4 = 6.4k.

The balance of the reference current I_{R1} is found to be

$I_{R1} = 3.9mA - I_{R4}$
or
$I_{R1} = 3.9mA - 234mA = 1.56mA$
and
R1 = 6.4k

Using commonly available values, and remembering that R4 current must exceed R1 current, we set

R1 = 6.8k
and R4 = 6.2k.

Maximum reference current is now

$$I_{REF}(max) = \frac{15V}{6.2k} + \frac{10V}{6.8k} = 3.9mA.$$

The parallel combination of R1 and R4 is found to be 3.24k, so minimum compensation capacitor value is

$C_C(min) = (3.24)(15)pF = 48.6pF.$

If we use 50pF, from the graph we find f_{MAX} to be 370kHz. For unity gain,

R2 = R1 = 6.8k
R3 = R2 = 6.8k
R5 = R1 = 6.8k

$$R6 = R7 = \frac{(R1)(R4)}{R1 + R4} = 3.24k$$

(use 3.3k)

Example 2: Usable input signal is $12V_{P-P}$, centered at 0V, with occasional excursion to twice this amplitude, which we do not care about. Maximum input frequency is to be

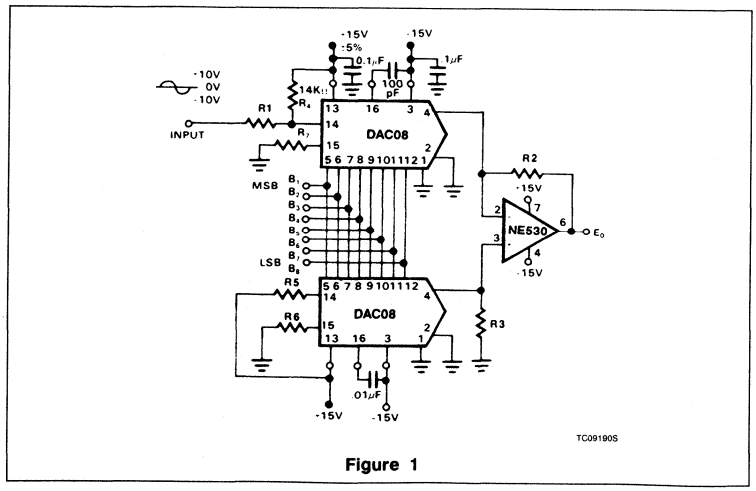


Figure 1

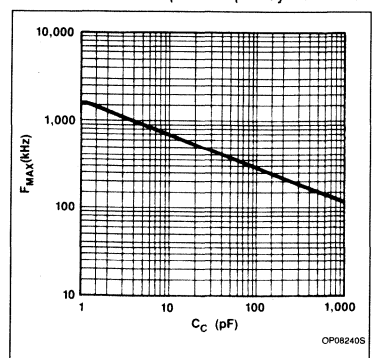


Figure 2

500kHz. Available power supplies are +5V logic supply, +15V, −15V, all regulated. Determine values of all resistors and C_C for maximum gain of 2.

Solution 2: To extend the frequency response, we want minimum compensation capacitor value; therefore, we need minimum R1 and R4 values, so we want to return R4 to as low a regulated supply as is possible; we will use the 5V logic supply.

At minimum usable input,

$$I_{REF} = \frac{5V}{R4} - \frac{6V}{R1}$$

or, for

$$I_{REF} = 0, \quad \frac{5V}{R4} = \frac{6V}{R1}$$

therefore, 55% of I_{REF} comes through R4, and

R4 = (5/6)R1.

Because peak input goes to +12V, this condition should not cause I_{REF} to exceed 5mA, and

$$\frac{12V}{R1} + \frac{5V}{R4} = 5mA$$

Recall that R4 = (5/6)R1

$$\frac{12V}{R1} + \frac{5}{(5/6)(R1)} = 5mA$$

$$\frac{12V}{R1} + \frac{6V}{R1} = 5mA$$

R1 = 3.6k
and R4 = (5/6)R1 = 3.0k.

Because the reference source will be the 5V logic supply, which will be noisy, we will split R4 into two resistors and bypass their junction with 0.1μF to ground. Furthermore, to be sure that R4 current exceeds R1 current, we will increase R1 to 4.3k. The absolute maximum reference current is now

$$I_{REF}(max) = \frac{12V}{4.3k} + \frac{5V}{3k} = 4.46mA.$$

The parallel combination of R1 and R4 is 1.77k, so minimum compensation capacitor is

$C_C(min) = (15)(1.77) = 26.5pF.$

If we use 27pF, the graph tells us the maximum frequency is about 470kHz, which is 6% lower than desired. If we wanted to further extend this frequency range, we find that we can reduce R4 to two resistors of 1.1k and 1.2k, bringing the absolute maximum reference current to

$$I_{REF}(max) = \frac{12V}{4.3k} + \frac{5V}{2.3k} = 4.96mA$$

and the maximum usable reference current becomes

$$I_{REF} = \frac{6V}{4.3k} + \frac{5V}{2.3k} = 3.57mA,$$

below the 5mA and 4mA respective desired maximum values. Now the resistance at Pin 14 is the parallel combination of R1 and R4, or 1.5k, and the minimum compensation capacitor becomes

$C_C(min) = (15)(1.5)pF = 22pF.$

The graph tells us we can just go to 500kHz.

AM6012
12-Bit Multiplying D/A Converter

Product Specification

DESCRIPTION

The AM6012 12-bit multiplying Digital-to-Analog converter provides high-speed and 0.025% differential nonlinearity over its full commercial temperature range.

The D/A converter uses a 3-bit segment generator for the MSBs in conjunction with a 9-bit R-2R diffused resistor ladder to provide 12-bit resolution without costly trimming processes. This technique guarantees a very uniform step size (up to ± ½ LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs.

The dual complementary outputs of the AM6012 increase its versatility, and effectively double the peak-to-peak output swing. Digital inputs, in addition, can be configured to accept all popular logic families.

While the device requires a reference input of 1mA for a 4mA full-scale current, operation is nearly independent of power supply voltage shifts. The power supply rejection ratio is ±0.001% FS/% ΔV. The devices will work from +5, −12V to ±18V rails, with as low as 230mW power consumption typical.

FEATURES

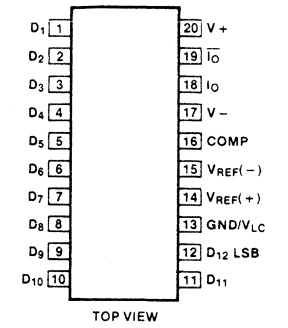
- **12-bit resolution**
- **Accurate to within ±0.05%**
- **Monotonic over temperature**
- **Fast settling time, 250ns typical**
- **Trimless design for low cost**
- **Differential current outputs**
- **High-speed multiplying capability**
- **Full-scale current, 4mA (with 1mA reference)**
- **High output compliance voltage, −5 to +10V**
- **Low power consumption, 230mW**

APPLICATIONS

- **CRT displays, computer graphics**
- **Robotics and machine tools**
- **Automatic test equipment**
- **Programmable power supplies**
- **CAD/CAM systems**
- **Data acquisition and control systems**
- **Analog-to-digital converter systems**

PIN CONFIGURATION

D[1] and F Packages



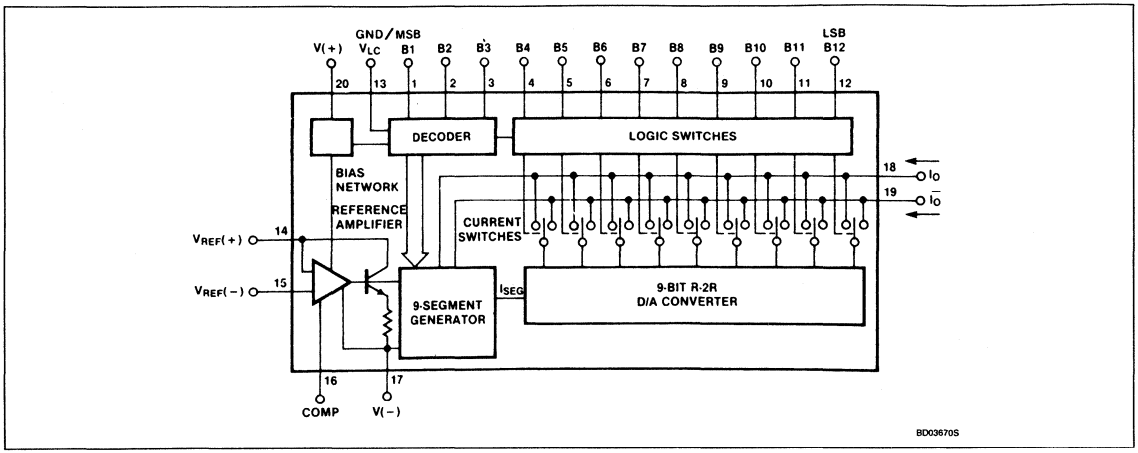
NOTE:
1. Available in large SO (SOL) package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Cerdip	0 to +70°C	AM6012F
20-Pin Plastic SOL	0 to +70°C	AM6012D

12-Bit Multiplying D/A Converter — AM6012

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature AM6012F	 0 to +70	 °C
T_{STG}	Storage temperature range	−65°C to +150	°C
T_{SOLD}	Lead soldering temperature 10sec max	300	°C
V_S	Power supply voltage	±18	V
	Logic inputs	−5V to +18	V
	Voltage across current outputs	−8V to +12	V
V_{REF}	Reference inputs V_{14}, V_{15}	V− to V+	
V_{REF}	Reference input differential voltage (V_{14} to V_{15})	±18	V
I_{REF}	Reference input current (I_{14})	1.25	mA
P_D	Maximum power dissipation, T_A = 25°C, (still-air)[1] F package D package	 1560 1390	 mW mW

NOTE:
1. Derate above 25°C, at the following rate:
   F package at 12.5mW/°C.
   D package at 11.1mW/°C.

DC ELECTRICAL CHARACTERISTICS $V+ = +15V$, $V- = -15V$, $I_{REF} = 1.0mA$, $0°C \leq T_A \leq 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		12			Bits
	Monotonicity		12			Bits
DNL	Differential nonlinearity	Deviation from ideal step size			±0.025	%FS
			12			Bits
NL	Nonlinearity	Deviation from ideal straight line			±.05	%FS
I_{FS}	Full-scale current	$V_{REF} = 10.000V$ $R_{14} - R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.935	3.999	4.063	mA
TCI_{FS}	Full-scale tempco			±10	±40	ppm/°C
				±0.001	±0.004	%FS/°C
V_{OC}	Output voltage compliance	DNL Specification guaranteed over compliance range $R_{OUT} > 10M\Omega$ typ.	−5		+10	V
I_{FSS}	Symmetry	$I_{FS} - I_{\overline{FS}}$		±0.4	±2.0	μA
I_{ZS}	Zero-scale current				0.10	μA
V_{IL} V_{IH}	Logic input levels — Logic "0"				0.8	V
	Logic input levels — Logic "1"		2.0			
I_{IN}	Logic input current	$V_{IN} = -5$ to $+18V$			40	μA
V_{IS}	Logic input swing	$V- = -15V$	−5		+18	V
I_{REF}	Reference current range		0.2	1.0	1.1	mA
I_{15}	Reference bias current		0	−0.5	−2.0	μA
dI/dt	Reference input slew rate	$R_{14(eq)} = 800\Omega$ $C_C = 0pF$	4.0	8.0		mA/μs
$PSSI_{FS+}$	Power supply sensitivity	$V+ = +13.5V$ to $+16.5V$, $V- = -15V$		±0.0005	±0.001	%FS/%
$PSSI_{FS-}$		$V- = -13.5V$ to $-16.5V$, $V+ = +15V$		±0.00025	±0.001	
V+	Power supply range	$V_{OUT} = 0V$	4.5		18	V
V−			−18		−10.8	
I+	Power supply current	$V+ = +5V$, $V- = -15V$		5.7	8.5	mA
I−				−13.7	−18.0	
I+		$V+ = +15V$, $V- = -15V$		5.7	8.5	
I−				−13.7	−18.0	
P_D	Power dissipation	$V+ = +5V$, $V- = -15V$		234	312	mW
		$V+ = +15V$, $V- = -15V$		291	397	

AC ELECTRICAL CHARACTERISTICS $V+ = +15V$, $V- = -15V$, $I_{REF} = 1.0mA$, $0°C \leq T_A \leq 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_S	Settling time	To ±½ LSB, all bits ON or OFF, $T_A = 25°C$		250	500	ns
t_{PLH} t_{PHL}	Propagation delay — all bits	50% to 50%		25	50	ns
C_{OUT}	Output capacitance			20		pF

CIRCUIT DESCRIPTION

The AM6012 is a 12-bit DAC which uses diffused resistors and requires no trimming to guarantee monotonicity over the temperature range. A segmented DAC design guarantees a more uniform step size over the temperature range than is normally available with trimmed 12-bit converters. The converter features differential high compliance current outputs, wide supply range, and a multiplying reference input.

In many converter applications, uniform step size is more important than conformance to an ideal straight line. Many 12-bit converters are used for high resolution rather than high linearity, since few transducers are more linear than ±0.1%. All classic binarily weighted converters require ± ½ LSB (±0.012%) linearity in order to guarantee monotonicity, which requires very tight resistor matching and tracking. The AM6012 uses conventional bipolar processing to achieve high differential linearity and monotonicity without requiring correspondingly high linearity, or conformance to an ideal straight line.

One design approach which provides monotonicity without requiring high linearity is the MOS switch-resistor string. This circuit is actually a full complement to a current-switched R-2R DAC since it is slower, has a voltage output, and, if implemented at the 12-bit level, would use 4096 low tolerance resistors rather than a minimum number of high tolerance resistors as in the R-2R network. Its lack of speed and density for 12 bits are its drawbacks.

With the segmented DAC approach, the 4096 required output levels are composed of 8 groups of 512 steps each. Each step group is generated by a 9-bit DAC, and each of the segment slopes is determined by one of 8 equal current sources. The resistors which determine monotonicity are in the 9-bit DAC. The major carry of the 9-bit DAC is repeated in each of the 8 segments, and requires eight times lower initial resistor accuracy and tracking to maintain a given differential nonlinearity over temperature.

The operation of the segmented DAC may be visualized by assuming an input code of all zeroes. The first segment current I_O is divided into 512 levels by the 9-bit multiplying DAC and fed to the output, I_{OUT}. As the input code increases, a new segment current is selected for each 512 counts. The previous segment is fed to output I_{OUT} where the new step group is added to it, thus ensuring monotonicity independent of segment resistor values. All higher order segments feed $\overline{I_{OUT}}$.

With the segmented DAC approach, the precision of the 8 main resistors determines linearity only. The influence of each of these resistors on linearity is four times lower than that of the MSB resistor in an R-2R DAC. Hence, assuming the same resistor tolerances for both, the linearity of the segmented approach would actually be higher than that of an R-2R design.

The step generator or 9-bit DAC is composed of a master and a slave ladder. The slave ladder generates the four least significant bits from the remainder of the master ladder by active current splitting utilizing scaled emitters. This saves ladder resistors and greatly reduces the range of emitter scaling required in the 9-bit DAC. All current switches in the step generator are high-speed fully-differential switches which are capable of switching low currents at high speed. This allows the use of a binary scaled network all the way to the least significant bit which saves power and simplifies the circuitry.

Diffused resistors have advantages over thin film resistors beyond simple economy and bipolar process compatibility. The resistors are fabricated in single crystal rather than amorphous material which gives them better long term stability and tracking and much higher moisture resistance. They are diffused at 1000°C and so are resistant to changes in value due to thermal and chemical causes. Also, no burn-in is required for stability. The contact resistance between aluminum and silicon is more predictable than between aluminum and an amorphous thin film, and no sandwich metals are required to enhance or protect the contact or limit alloying. The initial match between two diffused resistors is similar to that of thin film since both are defined by photomasks and chemical etching. Since the resistors are not trimmed or altered after fabrication, their tracking and long-term characteristics are not degraded.

DIFFERENTIAL VS INTEGRAL NONLINEARITY

Integral nonlinearity, for the purposes of the discussion, refers to the "straightness" of the line drawn through the individual response points of a data converter. Differential nonlinearity, on the other hand, refers to the deviation of the spacing of the adjacent points from a 1 LSB ideal spacing. Both may be expressed as either a percentage of full-scale output or as fractional LSBs or both. The graphs in Figure 1 define the manner in which these parameters are specified. The left graph shows a portion of the transfer curve of a DAC with ½ LSB INL and the (implied) DNL spec of 1 LSB. Below this is a graphic representation of the way this would appear on a CRT screen where the AM6012 is used as a display driver. On the right is a portion of the transfer curve of a DAC specified for 2 LSB INL with ½ LSB DNL specified and the graphic display below it.

One of the characteristics of an R-2R DAC in standard form is that any transition which causes a zero LSB change (i.e., the same output for two different codes) will exhibit the same output each time that transition occurs. The same holds true for transitions causing a 2 LSB change. These two problem transitions are allowable for the standard definition of monotonicity and also allow the device to be specified very tightly for INL. The major problem arising from this error type is in A/D converter implementations. Inputs producing the same output are now represented by ambiguous output codes for an identical input. Also, two LSB gaps can cause large errors at those input levels (assuming ½ LSB quantizing levels). It can be seen from the two figures that the DNL-specified D/A converter will yield much finer grained data than the INL-specified part, thus improving the ability of the A/D to resolve changes in the analog input.

ANALOG OUTPUT CURRENTS

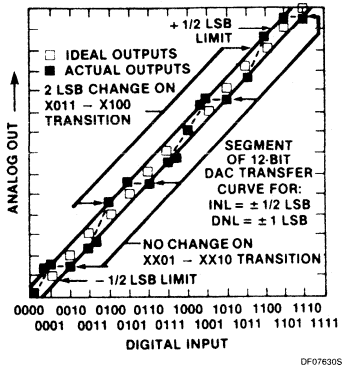
Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at Pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at Pin 18 and turned on at Pin 19. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required, it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V– and is independent of the positive supply. Negative compliance is +10V above V–.

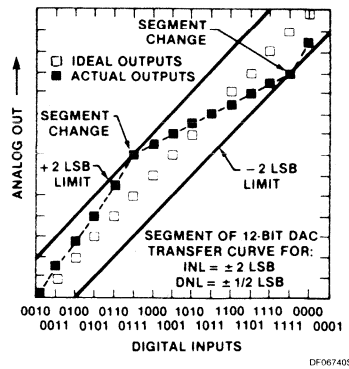
The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

DIFFERENTIAL LINEARITY COMPARISON

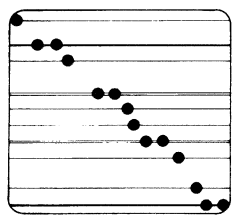
D/A Converter With
± ½ LSB INL, ± 1 LSB DNL



D/A Converter With
± 2 LSB INL, ± ½ LSB DNL



Video Deflection by DACs



Video Deflection by DACs

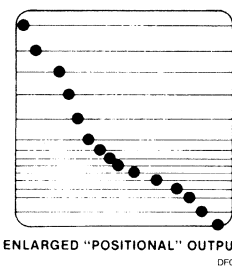


Figure 1

POWER SUPPLIES

The AM6012 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V– supplies of –10V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at –9V with $I_{REF} = 1mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the AM6012 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc., remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the AM6012 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ± 10ppm/°C, with zero-scale output current and drift essentially negligible compared to ½ LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full-scale drift.

SETTLING TIME

The AM6012 is capable of extremely fast settling times, typically 250ns at $I_{REF} = 1.0mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within ½ LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ns. The output capacitance of the AM6012 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ± 2μA, therefore a 2.5kΩ load is needed to provide adequate drive for most oscilloscopes. At I_{REF} values of less than 0.5mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111111 to 100000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ± 0.1% of the final value, and thus settling times may be observed at lower values of I_{REF}.

AM6012 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

APPLICATIONS INFORMATION

Reference Amplifier Setup

The AM6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF},$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at Pin 15. Reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors (Figure 2a).

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15. The negative common-mode range of the reference amplifier is given by: V_{CM-} = V– plus ($I_{REF} \times 3k\Omega$) plus 1.8V. The positive common-mode range is V+ less 1.23V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}.

MULTIPLYING OPERATION

The AM6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V–. The value of this capacitor depends on the impedance presented to Pin 14. For R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 5, 12 and 25pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin (see Figure 2b).

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1kΩ and C_C = 5pF, the reference amplifier slews at 4mA/ms enabling a transition from I_{REF} = 0 to I_{REF} = 1mA in 250ns.

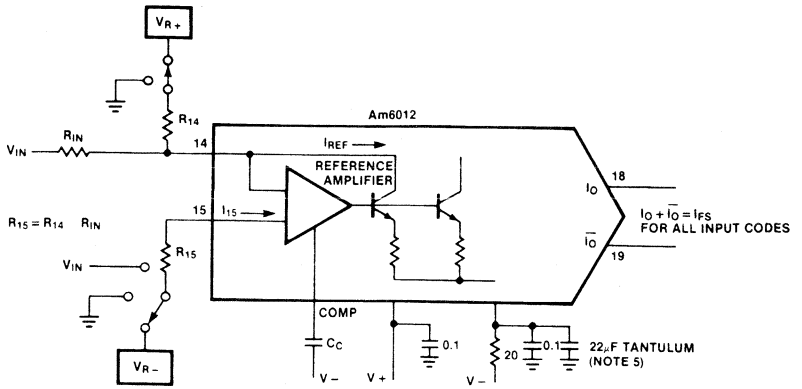
Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at Pin 14 is 800Ω and C_C = 0. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The AM6012 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic threshold voltage. For V– = –15V, the logic inputs may swing between –5 and +10V. This enables direct interface with +15V CMOS logic, even when the AM6012 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by:

V– plus ($I_{REF} \times 3k\Omega$) plus 1.8V.

The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (Pin 13, V_{LC}). For TTL interface, simply ground Pin 13. When interfacing ECL, an $I_{REF} \leqslant 1mA$ is recommended. For general setup of the logic control circuit, it should be noted that Pin 13 will sink 1.1mA typical. External circuitry should be designed to accommodate this current (Figure 3).



REFERENCE CONFIGURATION	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive reference	V_{R+}	0V	N/C	0.01μF	V_{R+}/R_{14}
Negative reference	0V	V_{R-}	N/C	0.01μF	$-V_{R-}/R_{14}$
Lo impedance bipolar reference	V_{R+}	0V	V_{IN}[1]		$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$[2]
Hi impedance bipolar Reference	V_{R+}	V_{IN}	N/C[1]		$(V_{R+} - V_{IN})/R_{14}$[3]
Pulsed reference[4]	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

NOTES:
1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least $5pF \times R_{14(eq)}$ in kΩ. For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at Pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V− with 20Ω and bypass with 22μF tantulum capacitor.
6. Reference current and reference resistor — there is a 1-to-4 scale factor between the reference current (I_{REF}) and the full-scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 4mA$, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10V}{4mA} = 10k\Omega \qquad R_{14} = R_{15}$$

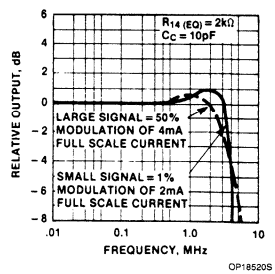
a. Reference Amplifier Biasing

Minimum Size Compensation Capacitor (I_{FS} = 4mA, I_{REF}=1.0mA)

$R_{14(EQ)}$ (kΩ)	C_C (pF)
10	50
5	25
2	10
1	5
.5	0

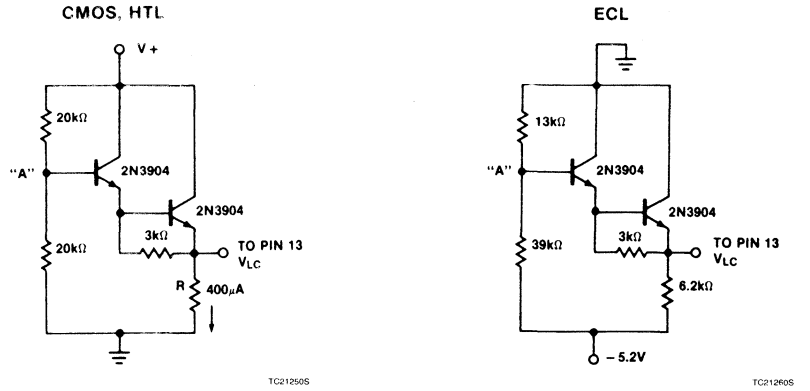
NOTE:
A 0.01μF capacitor is recommended for fixed reference operation.

Reference Amplifier Frequency Response



b.

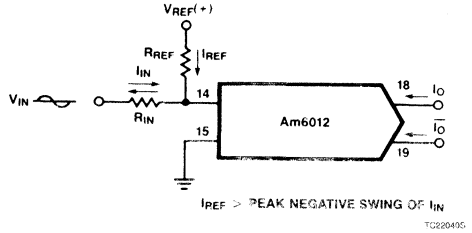
Figure 2



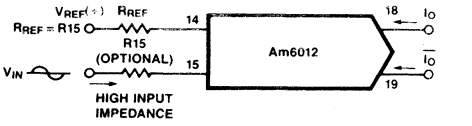
NOTE:
1. Set the voltage 'A' to the desired logic input switching threshold.
2. Allowable range of logic threshold is typically −5V to + 13.5V when operating the DAC on ± 15V supplies.

Figure 3. Interfacing Circuits for ECL, CMOS, HTL Logic Inputs

ACCOMMODATING BIPOLAR REFERENCE

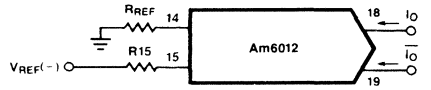


NOTE:
$I_{REF} > $ Peak negative swing of I_{IN}.



NOTE:
$V_{REF}(+)$ Must be above peak positive swing of V_{IN}.

BASIC NEGATIVE REFERENCE OPERATION



$$I_{FS} \approx \frac{V_{REF}(-)}{R_{REF}} \times 4$$

NOTE:
R_{REF} SETS I_{FS}; R15 IS FOR A BIAS CURRENT CANCELLATION.

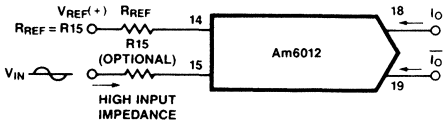
TC22050S

NOTE:

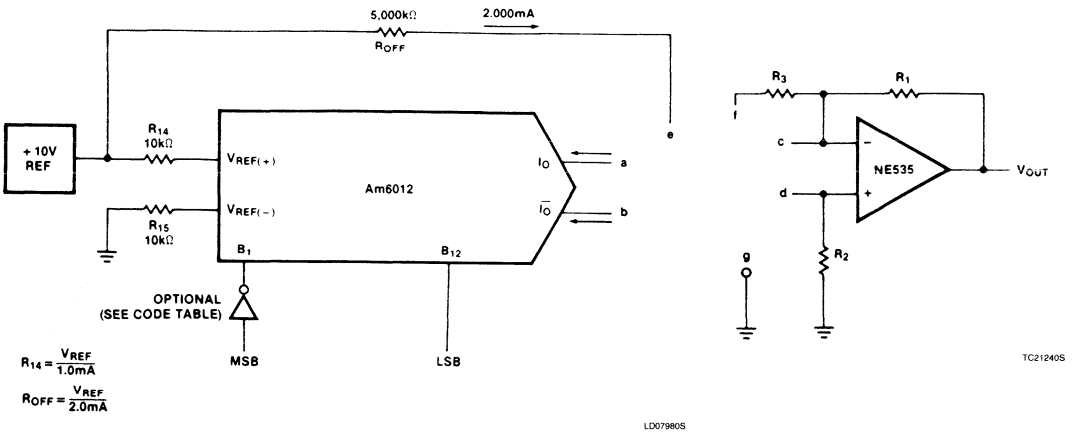
$$I_{FS} \approx \frac{V_{REF}(-)}{R_{REF}} \times 4$$

R_{REF} sets I_{FS}; R15 is for a bias current cancellation.

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT



APPLICATION CIRCUITS



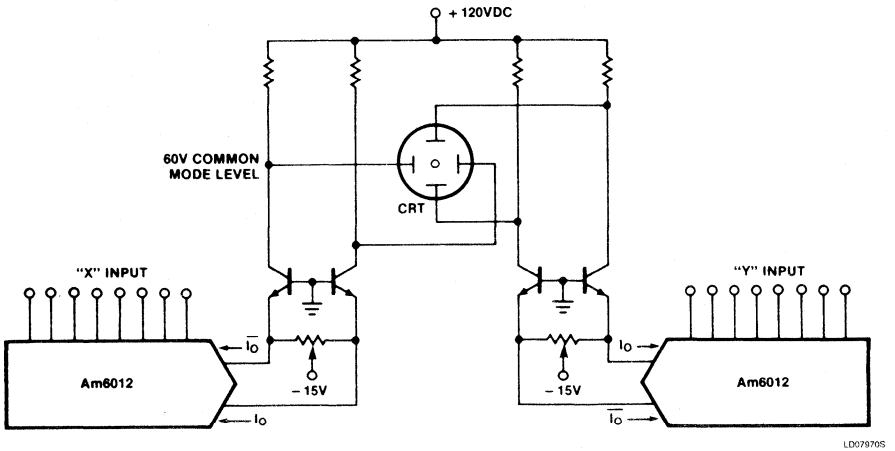
CODE FORMAT		CONNECTIONS	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_0 (mA)	$\bar{I}_0$ (mA)	V_{OUT}
Unipolar	Straight binary; one polarity with true input code, true zero output.	a – c b – g R1 = R2 = 2.5k	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
			Positive full-scale –LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
			Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
	Complementary binary; one polarity with complementary input code, true zero output.	a – g b – c R1 = R2 = 2.5k	Positive full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
			Positive full-scale –LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
			Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000
Symmetrical Offset	Straight offset binary; offset half-scale, symmetrical about zero, no true zero output.	a – c b – d f – g R1 = R3 = 2.5k R2 = 1.25k	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
			Positive full-scale –LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
			(+) Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
			(–) Zero-scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0024
			Negative full-scale –LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9927
			Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–9.9976
	1's complement; offset half-scale, symmetrical about zero, no true zero output, MSB complemented (need inverter at B1).	a – c b – d f – g R1 = R3 = 2.5k R2 = 1.25k	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
			Positive full-scale –LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
			(+) Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
			(–) Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0024
			Negative full-scale –LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9927
			Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–9.9976
Offset with True Zero	Offset binary; offset half-scale, true zero output.	e – a – c b – g R1 = R2 = 5k	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
			Positive full-scale –LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
			+LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
			Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
			–LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0049
			Negative full-scale +LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9951
			Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–10.000
	2's complement; offset half-scale, true zero output, MSB complemented (need inverter at B1).	e – a – c b – g R1 = R2 = 5k	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1			
			Positive full-scale –LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
			+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
			Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
			–1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.049
			Negative full-scale +LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9951
			Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–10.000

Figure 4. AM6012 Logic Inputs

ADDITIONAL CODE MODIFICATIONS

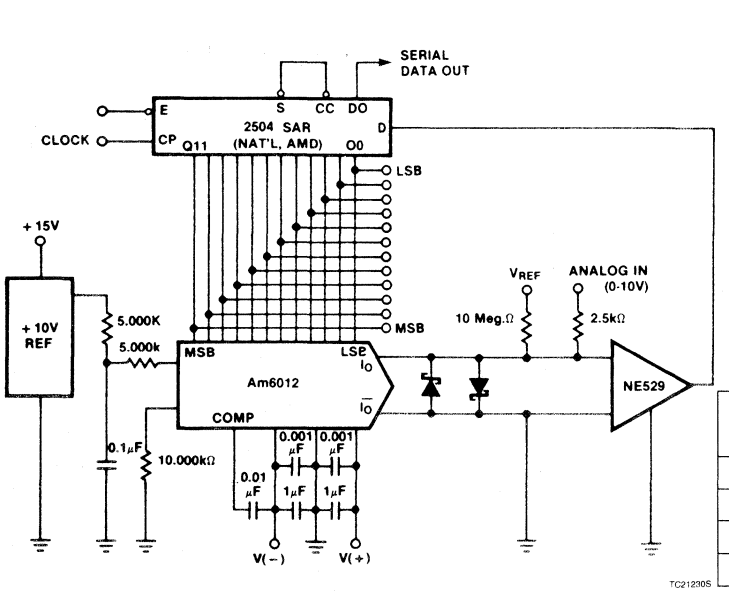
1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

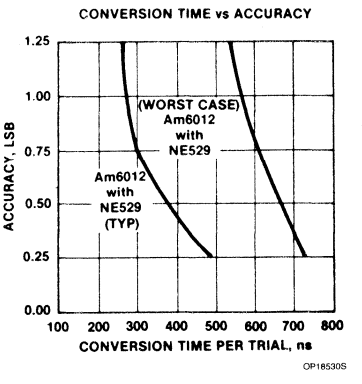
APPLICATION CIRCUITS



NOTES:
1. Full differential drive lowers power supply voltage.
2. Eliminates inverting amplifiers and transformers.
3. Independent beam centering controls.

Figure 5. CRT Display Driver

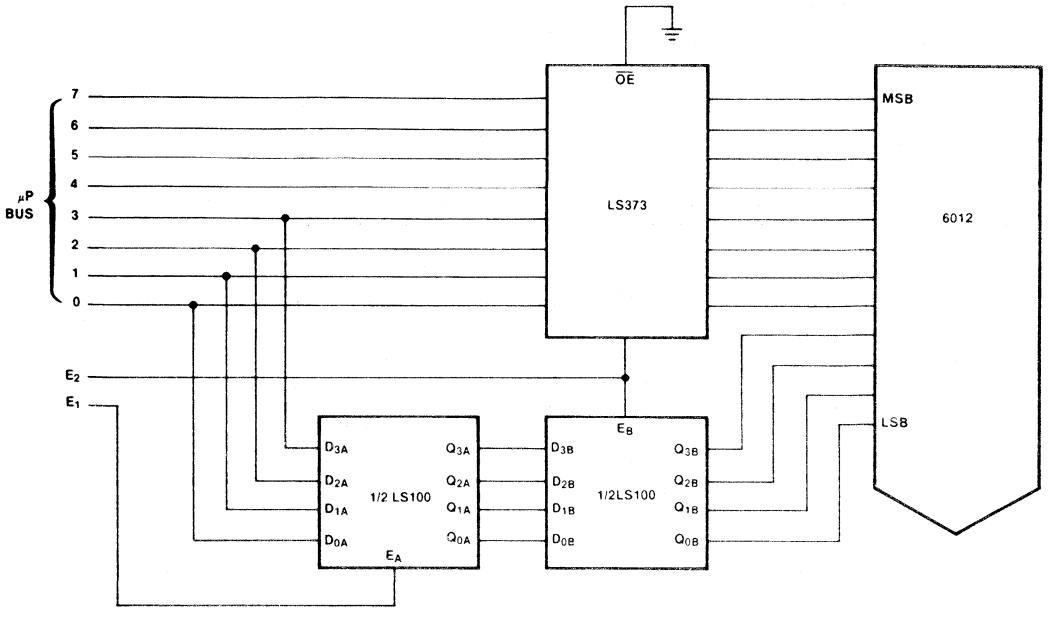




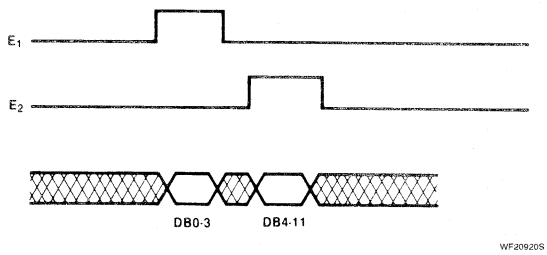
CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
NE529	100	150
TOTAL	383ns	705ns
× 13	5.0μs	9.1μs

Figure 6. 12-Bit High-Speed A/D Converter

APPLICATION CIRCUITS



a. Interface With 8-Bit Microprocessor Bus



b. Timing Sequence

NOTE:
Data remains on inputs of DAC until updated by E2 pulse. Timing will depend on processor used.

Figure 7

DAC08 Series
8-Bit High-Speed Multiplying D/A Converter

Product Specification

DESCRIPTION

The DAC08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 70ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20-to-1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All DAC08 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range. Device performance is essentially unchanged over the ± 4.5V to ± 18V power supply range, with 37mW power consumption attainable at ± 5V supplies.

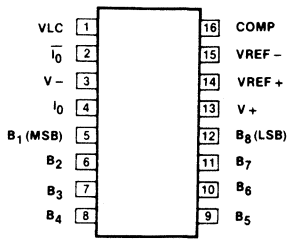
The compact size and low power consumption make the DAC08 attractive for portable and military aerospace applications.

FEATURES

- **Fast settling output current — 70ns**
- **Full-scale current prematched to ± 1 LSB**
- **Direct interface to TTL, CMOS, ECL, HTL, PMOS**
- **Relative accuracy to 0.1% maximum over temperature range**
- **High output compliance −10V to +18V**
- **True and complemented outputs**
- **Wide range multiplying capability**
- **Low FS current drift — ± 10ppm/°C**
- **Wide power supply range — ± 4.5V to ± 18V**
- **Low power consumption — 37mW at ± 5V**

PIN CONFIGURATIONS

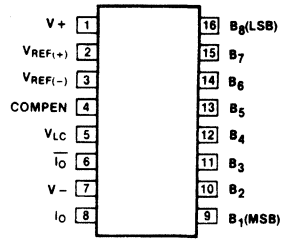
F, N Packages



TOP VIEW

CD10580S

D Package[1]



TOP VIEW

CD10590S

NOTE:
1. SO and non-standard pinouts.

APPLICATIONS

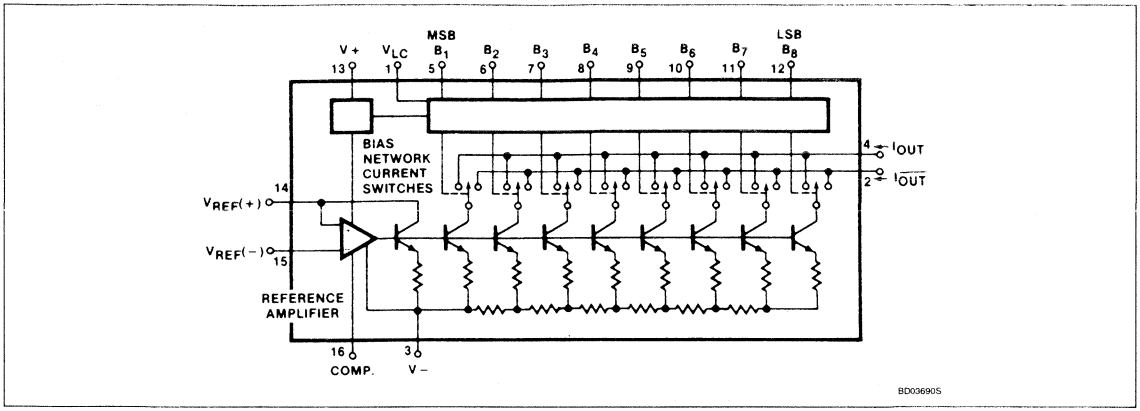
- **8-bit, 1μs A-to-D converters**
- **Servo-motor and pen drivers**
- **Waveform generators**
- **Audio encoders and attenuators**
- **Analog meter drivers**
- **Programmable power supplies**
- **CRT display drivers**
- **High-speed modems**
- **Other applications where low cost, high speed and complete input/output versatility are required**
- **Programmable gain and attentuation**
- **Analog-Digital multiplication**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Hermetic Cerdip	−55°C to +125°C	DAC08F
16-Pin Hermetic Cerdip	−55°C to +125°C	DAC08AF
16-Pin Plastic DIP	0 to +70°C	DAC08CN
16-Pin Hermetic Cerdip	0 to +70°C	DAC08CF
16-Pin Plastic DIP	0 to +70°C	DAC08EN
16-Pin Hermetic Cerdip	0 to +70°C	DAC08EF
16-Pin Plastic SO	0 to +70°C	DAC08ED
16-Pin Hermetic Cerdip	0 to +70°C	DAC08HF
16-Pin Plastic DIP	0 to +70°C	DAC08HN

8-Bit High-Speed Multiplying D/A Converter — DAC08 Series

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+ to V−	Power supply voltage	36	V
$V_5 - V_{12}$	Digital input voltage	V− to V− plus 36V	
V_{LC}	Logic threshold control	V− to V+	
V_0	Applied output voltage	V− to +18	V
I_{14}	Reference current	5.0	mA
V_{14}, V_{15}	Reference amplifier inputs	V_{EE} to V_{CC}	
P_D	Maximum power dissipation $T_A = 25°C$ (still-air)[1]		
	F package	1190	mW
	N package	1450	mW
	D package	1090	mW
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
T_A	Operating temperature range		
	DAC08, DAC08A	−55 to +125	°C
	DAC08C, E, H	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:
1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C.
   N package at 11.6mW/°C.
   D package at 8.7mW/°C.

DC ELECTRICAL CHARACTERISTICS

Pin 3 must be at least 3V more negative than the potential to which R_{15} is returned.

$V_{CC} = \pm 15V$, $I_{REF} = 2.0mA$, Output characteristics refer to both I_{OUT} and $I_{\overline{OUT}}$ unless otherwise noted. DAC08C, E, H: $T_A = 0°C$ to $70°C$. DAC08/08A: $T_A = -55°C$ to $125°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	DAC08C			DAC08E DAC08			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution Monotonicity		8 8	8 8	8 8	8 8	8 8	8 8	Bits Bits
	Relative accuracy Differential non-linearity	Over temperature range			±0.39 ±0.78			±0.19 ±0.39	%FS %FS
TCI_{FS}	Full-scale tempco			±10			±10		ppm/°C
V_{OC}	Output voltage compliance	Full-scale current change < ½ LSB	−10		+18	−10		+18	V
I_{FS4}	Full-scale current	$V_{REF} = 10.000V$, R_{14}, $R_{15} = 5.000k\Omega$	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full-scale symmetry	$I_{FS4} - I_{FS2}$		±2.0	±16		±1.0	±8.0	μA
I_{ZS}	Zero-scale current			0.2	4.0		0.2	2.0	μA
I_{FSR}	Full-scale output current range	R_{14}, $R_{15} = 5.000k\Omega$ $V_{REF} = +15.0V$, $V- = -10V$ $V_{REF} = +25.0V$, $V- = -12V$	2.1 4.2			2.1 4.2			mA
V_{IL} V_{IH}	Logic input levels Low High	$V_{LC} = 0V$	 2.0		0.8	 2.0		0.8	V
I_{IL} I_{IH}	Logic input current Low High	$V_{LC} = 0V$ $V_{IN} = -10V$ to $+0.8V$ $V_{IN} = 2.0V$ to $18V$		−2.0 0.002	−10 10		−2.0 0.002	−10 10	μA
V_{IS}	Logic input swing	$V- = -15V$	−10		+18	−10		+18	V
V_{THR}	Logic threshold range	$V_S = \pm 15V$	−10		+13.5	−10		+13.5	V
I_{15}	Reference bias current			−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference input slew rate		4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS+}$ PSI_{FS-}	Power supply sensitivity Positive Negative	$I_{REF} = 1mA$ $V+ = 4.5$ to $5.5V$, $V- = -15V$; $V+ = 13.5$ to $16.5V$, $V- = -15V$ $V- = -4.5$ to $-5.5V$, $V+ = +15V$; $V- = -13.5$ to -16.5, $V+ = +15V$		0.0003 0.002	0.01 0.01		0.0003 0.002	0.01 0.01	%FS/%VS
I+ I−	Power supply current Positive Negative	$V_S = \pm 5V$, $I_{REF} = 1.0mA$		3.1 −4.3	3.8 −5.8		3.1 −4.3	3.8 −5.8	mA
I+ I−	Positive Negative	$V_S = +5V$, $-15V$, $I_{REF} = 2.0mA$		3.1 −7.1	3.8 −7.8		3.1 −7.1	3.8 −7.8	
I+ I−	Positive Negative	$V_S = \pm 15V$, $I_{REF} = 2.0mA$		3.2 −7.2	3.8 −7.8		3.2 −7.2	3.8 −7.8	
P_D	Power dissipation	±5V, $I_{REF} = 1.0mA$ +5V, −15V, $I_{REF} = 2.0mA$ ±15V, $I_{REF} = 2.0mA$		37 122 156	48 136 174		37 122 156	48 136 174	mW

DC ELECTRICAL CHARACTERISTICS (Continued) Pin 3 must be at least 3V more negative than the potential to which R_{15} is returned.
$V_{CC} = \pm 15V$, $I_{REF} = 2.0mA$, Output characteristics refer to both I_{OUT} and $I_{\overline{OUT}}$, unless otherwise noted. DAC08C, E, H: $T_A = 0°C$ to $70°C$. DAC08/08A: $T_A = -55°C$ to $125°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	DAC08H DAC08A			UNIT
			Min	Typ	Max	
	Resolution Monotonicity		8 8	8 8	8 8	Bits Bits
	Relative accuracy Differential non-linearity	Over temperature range			±0.1 ±0.19	%FS %FS
TCI_{FS}	Full-scale tempco			±10	±50	ppm/°C
V_{OC}	Output voltage compliance	Full-scale current change ½ LSB	−10		+18	V
I_{FS4}	Full-scale current	$V_{REF} = 10.000V$, R_{14}, $R_{15} = 5.000k\Omega$	1.984	1.992	2.000	mA
I_{FSS}	Full-scale symmetry	$I_{FS4} - I_{FS2}$		±1.0	±4.0	μA
I_{ZS}	Zero-scale current			0.2	1.0	μA
I_{FSR}	Full-scale output current range	R_{14}, $R_{15} = 5.000k\Omega$ $V_{REF} = +15.0V$, $V- = -10V$ $V_{REF} = +25.0V$, $V- = -12V$	 2.1 4.2			mA
V_{IL} V_{IH}	Logic input levels Low High	$V_{LC} = 0V$	 2.0		0.8	V
I_{IL} I_{IH}	Logic input current Low High	$V_{LC} = 0V$ $V_{IN} = -10V$ to $+0.8V$ $V_{IN} = 2.0V$ to $18V$		 −2.0 0.002	 −10 10	μA
V_{IS}	Logic input swing	$V- = -15V$	−10		+18	V
V_{THR}	Logic threshold range	$V_S = \pm 15V$	−10		+13.5	V
I_{15}	Reference bias current			−1.0	−3.0	μA
dI/dt	Reference input slew rate		4.0	8.0		mA/μs
$PSSI_{FS+}$ PSI_{FS-}	Power supply sensitivity Positive Negative	$I_{REF} = 1mA$ $V+ = 4.5$ to $5.5V$, $V- = -15V$; $V+ = 13.5$ to $16.5V$, $V- = -15V$ $V- = -4.5$ to $-5.5V$, $V+ = +15V$; $V- = -13.5$ to -16.5, $V+ = +15V$		 0.0003 0.002	 0.01 0.01	%FS/%VS
I+ I−	Power supply current Positive Negative	$V_S = \pm 5V$, $I_{REF} = 1.0mA$		3.1 −4.3	3.8 −5.8	mA
I+ I−	Positive Negative	$V_S = +5V$, $-15V$, $I_{REF} = 2.0mA$		3.1 −7.1	3.8 −7.8	
I+ I−	Positive Negative	$V_S = \pm 15V$, $I_{REF} = 2.0mA$		3.2 −7.2	3.8 −7.8	
P_D	Power dissipation	$\pm 5V$, $I_{REF} = 1.0mA$ $+5V$, $-15V$, $I_{REF} = 2.0mA$ $\pm 15V$, $I_{REF} = 2.0mA$		37 122 156	48 136 174	mW

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	DAC08C			DAC08E DAC08			DAC08H DAC08A			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_S	Settling time	To ± ½ LSB, all bits switched on or off, T_A = 25°C		70	135		70	135		70	135	ns
t_{PLH} t_{PHL}	Propagation delay Low-to-High High-to-Low	T_A = 25°C, each bit. All bits switched		35	60		35	60		35	60	ns

TEST CIRCUITS

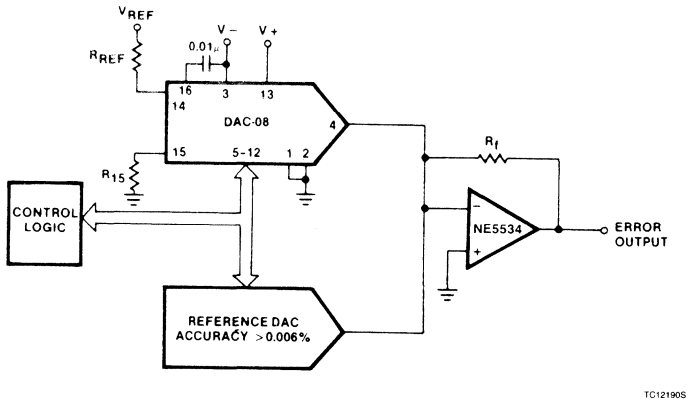
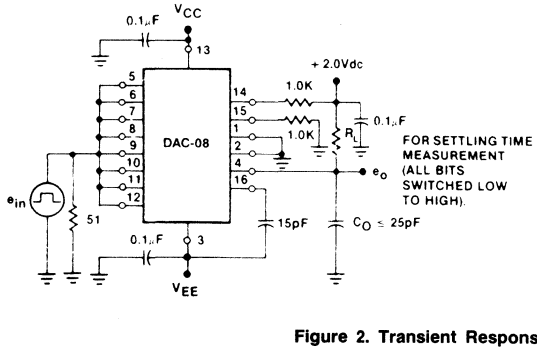


Figure 1. Relative Accuracy Test Circuit



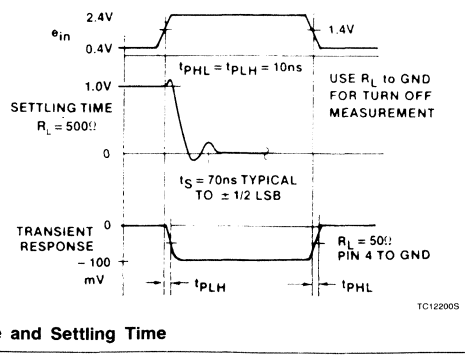


Figure 2. Transient Response and Settling Time

TEST CIRCUITS (Continued)

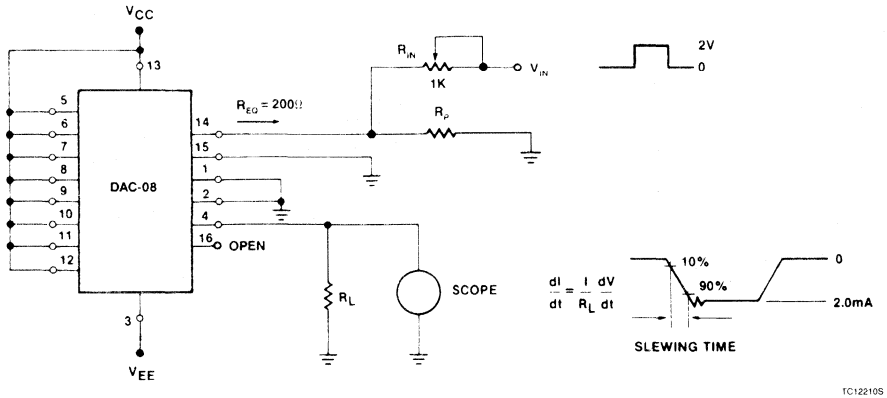
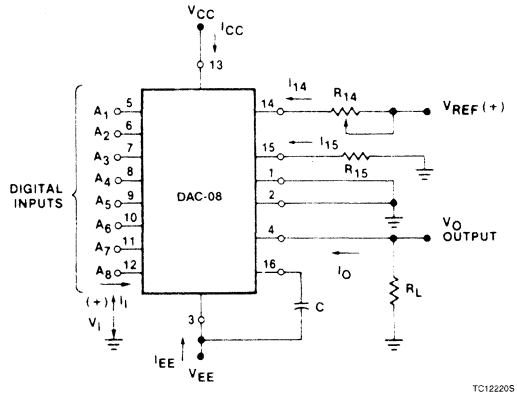


Figure 3. Reference Current Slew Rate Measurement



NOTES:
(See text for values of C.)
Typical values $R_{14} = R_{15} = 1k$
$V_{REF} = +2.0V$
$C = 15pF$
V_I and I_I apply to inputs A_1 through A_8
The resistor tied to Pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256}\right\}$$

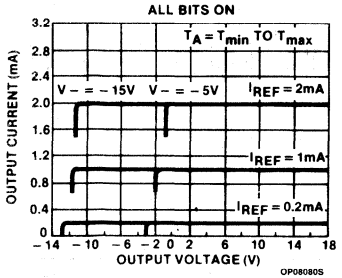
where $K \cong \frac{V_{REF}}{R_{14}}$

and A_N = '1' if A_N is at High Level
A_N = '0' if A_N is at Low Level

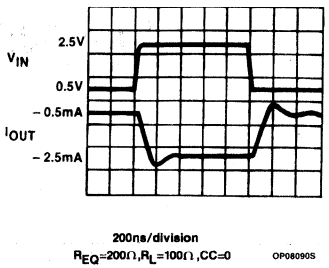
Figure 4. Notation Definitions

TYPICAL PERFORMANCE CHARACTERISTICS

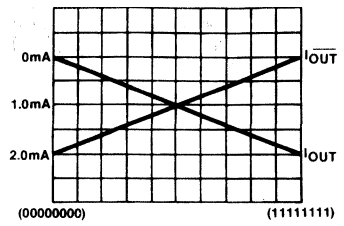
Output Current vs Output Voltage (Output Voltage Compliance)



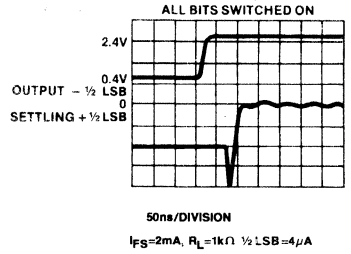
Fast Pulsed Reference Operation



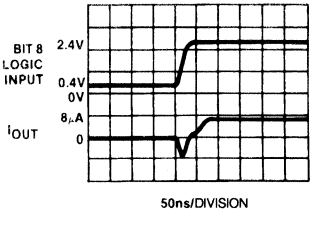
True and Complementary Output Operation



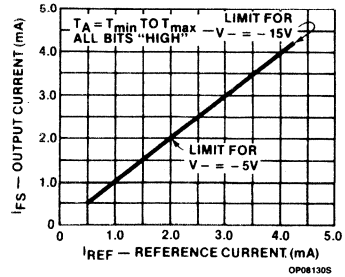
Full-Scale Settling Time



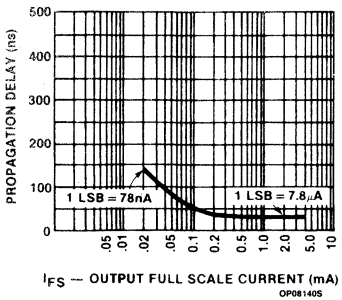
LSB Switching



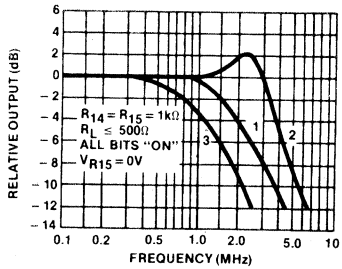
Full-Scale Current vs Reference Current



LSB Propagation Delay vs IFS



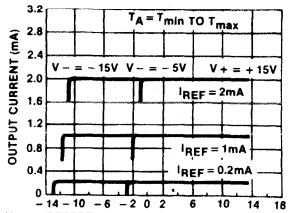
Reference Input Frequency Response



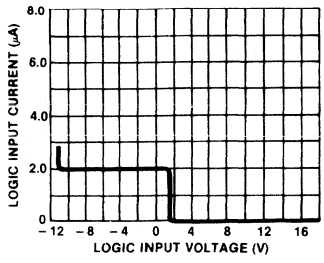
NOTES:
Curve 1: CC = 15pF, V_{IN} = 2.0V P-P centered at +1.0V
Curve 2: CC = 15pF, V_{IN} = 50mV P-P centered at +200mV
Curve 3: CC = 0pF, V_{IN} = 100mV P-P centered at 0V and applied through 50Ω connected to Pin 14. +2.0V applied to R_{14}.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

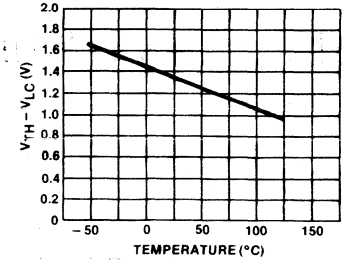
Reference AMP Common-Mode Range All Bits On



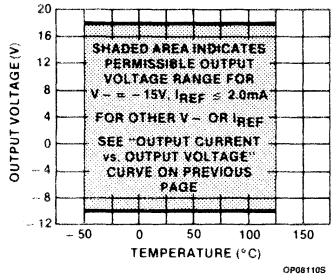
Logic Input Current vs Input Voltage



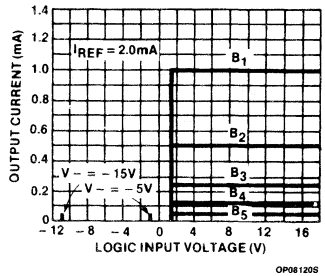
$V_{TH} - V_{LC}$ vs Temperature



Output Voltage Compliance vs Temperature

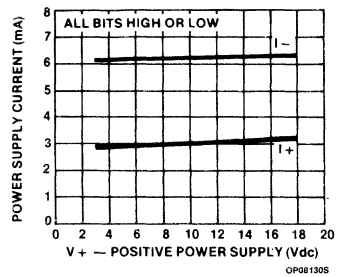


Bit Transfer Characteristics

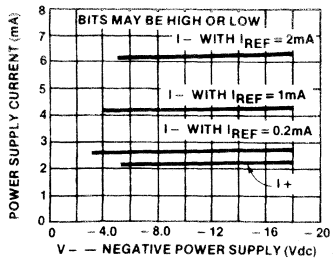


NOTE:
B_1 through B_8 have identical transfer characteristics. Bits are fully switched, with less than ½ LSB error, at less than ±100mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0V over the operating temperature range (V_{LC} = 0.0V).

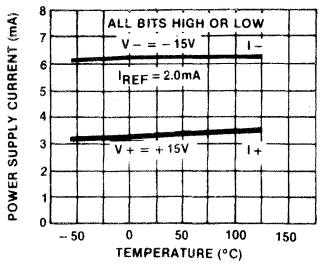
Power Supply Current vs V+



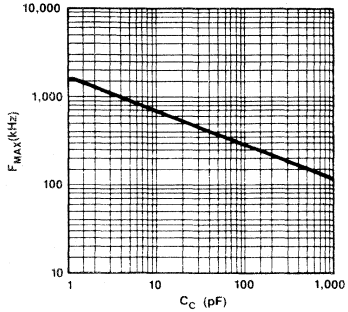
Power Supply Current vs V−



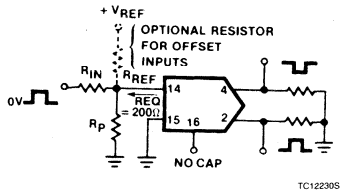
Power Supply Current vs Temperature



Maximum Reference Input Frequency vs Compensation Capacitor Value



TYPICAL APPLICATION



NOTES:
REQ = $R_{IN} \| R_P$
Typical Values
R_{IN} = 5kΩ
+V_{IN} = 10V

Pulsed Referenced Operation

FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into Pin 14 regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. R_{15} may be eliminated with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased as R_{14} value is increased. This is in order to maintain proper phase margin. For R_{14} values of 1.0, 2.5, and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF, respectively. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply.)

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at Pin 15.

When using a DC reference voltage, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage, but if a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be formed of two series resistors with the junction of the two resistors bypassed with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods applies and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage at Pin 4 must always be at least 4.5V more positive than the voltage of the negative supply (Pin 3) when the reference current is 2mA or less, and at least 8V more positive than the negative supply when the reference current is between 2mA and 4mA. This is necessary to avoid saturation of the output transistors, which would cause serious accuracy degradation.

Output Current Range

Any time the full-scale current exceeds 2mA, the negative supply must be at least 8V more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full-scale accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current after zero-scale current has been nulled out. The relative accuracy of the DAC08 series is essentially constant over the operating temperature range due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC08 series has a very low full-scale current drift over the operating temperature range.

The DAC08 series is guaranteed accurate to within ± ½ LSB at +25°C at a full-scale output current of 1.992mA. The relative accuracy test circuit is shown in Figure 1. The 12-bit converter is calibrated to a full-scale output current of 1.99219mA, then the DAC08 full-scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total of ± ½ part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification of the DAC08 series.

Monotonicity

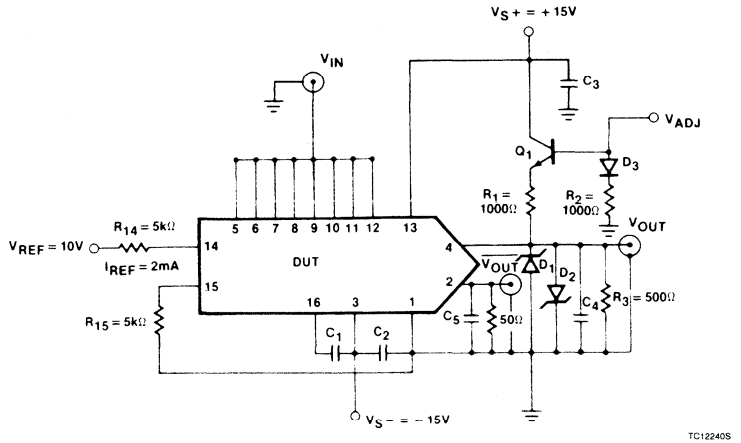
A monotonic converter is one which always provides analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The DAC08 series is monotonic for all values of reference current above 0.5mA. The recommended range for operation is a DC reference current between 0.5mA and 4.0mA.

Settling Time

The worst-case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70ns for settling to within ½ LSB for 8-bit accuracy. This time applies when $R_L < 500\Omega$ and $C_O < 25pF$. The slowest single switch is the least significant bit, which typically turns on and settles in 65ns. In applications where the DAC functions in a positive-going ramp mode, the worst-case condition does not occur and settling times less than 70ns may be realized.

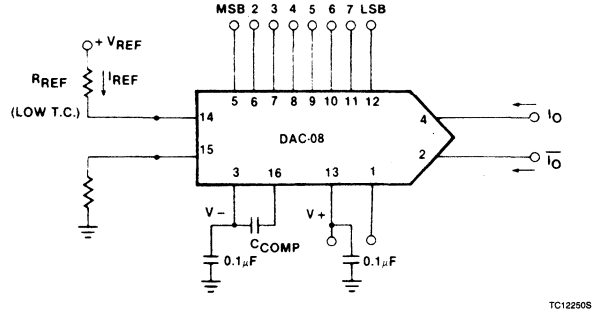
Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, minimum scope lead length, and avoidance of ground loops are all mandatory.

SETTLING TIME AND PROPAGATION DELAY



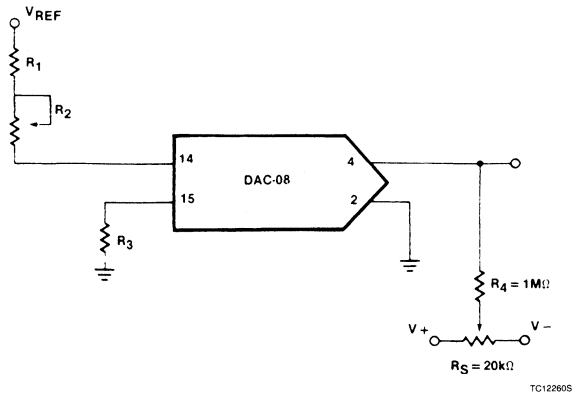
NOTES:
D_1, D_2 = IN6263 or equivalent
D_3 = IN914 or equivalent
C_1 = 0.01μF
C_2, C_3 = 0.1μF
Q_1 = 2N3904
C_4, C_5 = 15pF and includes all probe and fixturing capacitance.

BASIC DAC08 CONFIGURATION



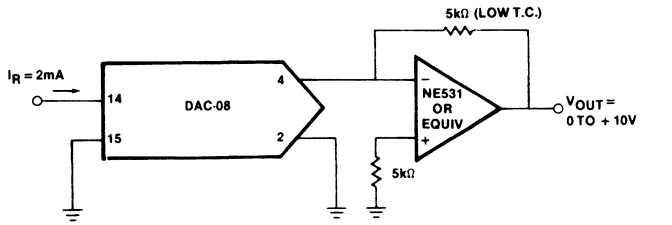
NOTE:
$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$; $I_O + \overline{I_O} = I_{FS}$ for all logic states

RECOMMENDED FULL-SCALE AND ZERO-SCALE ADJUST

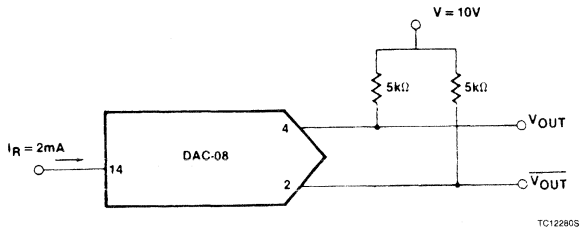


NOTES:
R_1 = low T.C.
$R_3 = R_1 + R_2$
$R_2 \simeq 0.1\ R_1$ to minimize pot. contribution to full-scale drift

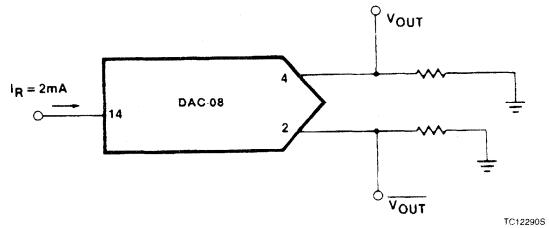
UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT



UNIPOLAR VOLTAGE OUTPUT FOR HIGH IMPEDANCE OUTPUT

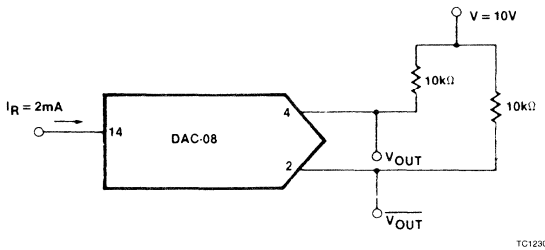


a. Positive Output



b. Negative Output

BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	V_{OUT}	$\overline{V_{OUT}}$
Positive full-scale	1	1	1	1	1	1	1	1	−9.920V	+10.000
Positive FS − 1LSB	1	1	1	1	1	1	1	0	−9.840V	+9.920
+Zero-scale + 1LSB	1	0	0	0	0	0	0	1	−0.080V	+0.160
Zero-scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero-scale − 1LSB	0	1	1	1	1	1	1	1	0.080	0.000
Negative full scale − 1LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Negative full scale	0	0	0	0	0	0	0	0	+10.000	−9.920

MC1508-8/1408-8/1408-7
8-Bit Multiplying D/A Converter

Product Specification

DESCRIPTION

The MC1508/MC1408 series of 8-bit monolithic digital-to-analog converters provide high-speed performance with low cost. They are designed for use where the output current is a linear product of an 8-bit digital word and an analog reference voltage.

FEATURES

- **Fast settling time — 70ns (typ)**
- **Relative accuracy ±0.19% (max error)**
- **Non-inverting digital inputs are TTL and CMOS compatible**
- **High-speed multiplying rate 4.0mA/μs (input slew)**
- **Output voltage swing +0.5V to −5.0V**
- **Standard supply voltages +5.0V and −5.0V to −15V**
- **Military qualifications pending**

APPLICATIONS

- **Tracking A-to-D converters**
- **2½-digit panel meters and DVMs**
- **Waveform synthesis**
- **Sample-and-hold**
- **Peak detector**
- **Programmable gain and attenuation**
- **CRT character generation**
- **Audio digitizing and decoding**
- **Programmable power supplies**
- **Analog – digital multiplication**
- **Digital – digital multiplication**
- **Analog – digital division**
- **Digital addition and subtraction**
- **Speech compression and expansion**
- **Stepping motor drive**
- **Modems**
- **Servo motor and pen drivers**

CIRCUIT DESCRIPTION

The MC1508/MC1408 consists of a reference current amplifier, an R-2R ladder, and 8 high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

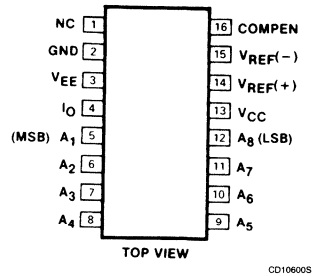
The switches are non-inverting in operation; therefore, a high state on the input turns on the specified output current component.

The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992mA for a 2.0mA reference amplifier current if the NPN current source pair is perfectly matched.

PIN CONFIGURATIONS

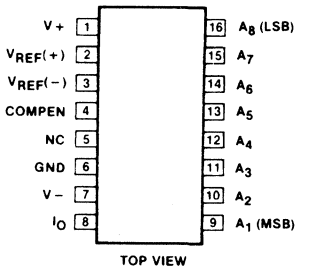
F, N Packages



TOP VIEW

CD10600S

D Package[1]

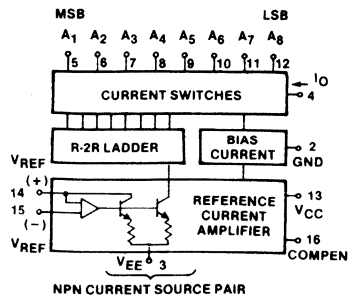


TOP VIEW

CD10610S

NOTE:
1. SO and non-standard pinouts.

BLOCK DIAGRAM



BD03700S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	−55°C to +125°C	MC1508-8F
16-Pin Plastic DIP	0 to +70°C	MC1408-7N
16-Pin Cerdip	0 to +70°C	MC1408-7F
16-Pin SO package	0 to +70°C	MC1408-8D

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Positive power supply voltage	+5.5	V
V_{EE}	Negative power supply voltage	−16.5	V
$V_5 - V_{12}$	Digital input voltage	0 to V_{CC}	V
V_O	Applied output voltage	−5.2 to +18	V
I_{14}	Reference current	5.0	mA
V_{14}, V_{15}	Reference amplifier inputs	V_{EE} to V_{CC}	
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package N package D package	 1190 1450 1080	 mW mW mW
T_{SOLD}	Lead soldering temperature (10sec)	300	°C
T_A	Operating temperature range MC1508 MC1408	 −55 to +125 0 to +75	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.6mW/°C
   D package at 8.6mW/°C

DC AND AC ELECTRICAL CHARACTERISTICS[1]

Pin 3 must be 3V more negative than the potential to which R_{15} is returned.

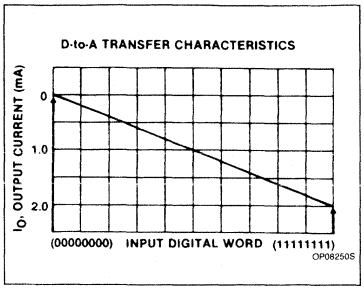
$V_{CC} = +5.0V_{DC}$, $V_{EE} = -15V_{DC}$, $\frac{V_{REF}}{R_{14}} = 2.0mA$ unless otherwise specified.

MC1508: $T_A = -55°C$ to $125°C$. MC1408: $T_A = 0°C$ to $75°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1508-8			MC1408-8			MC1408-7			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
E_r	Relative accuracy	Error relative to full-scale I_O, Figure 3			±0.19			±0.19			±0.39	%
t_S	Settling time[1]	To within ½ LSB, includes t_{PLH}, $T_A = +25°C$, Figure 4		70			70			70		ns
t_{PLH} t_{PHL}	Propagation delay time Low-to-High High-to-Low	$T_A = +25°C$, Figure 4		35	100		35	100		35	100	ns
TCI_O	Output full-scale current drift			−20			−20			−20		ppm/°C
V_{IH} V_{IL}	Digital input logic level (MSB) High Low	Figure 5	2.0		0.8	2.0		0.8	2.0		0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (MSB) High Low	Figure 5 $V_{IH} = 5.0V$ $V_{IL} = 0.8V$		0 −0.4	0.04 −0.8		0 −0.4	0.04 −0.8		0 −0.4	0.04 −0.8	mA
I_{15}	Reference input bias current	Pin 15, Figure 5		−1.0	−5.0		−1.0	−5.0		−1.0	−5.0	μA
I_{OR}	Output current range	Figure 5 $V_{EE} = -5.0V$ $V_{EE} = -7.0V$ to $-15V$	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA
I_O	Output current	Figure 5 $V_{REF} = 2.000V$, $R14 = 1000\Omega$	1.9	1.99	2.1	1.9	1.99	2.1	1.9	1.99	2.1	mA
$I_{O(min)}$	Off-state	All bits low		0	4.0		0	4.0		0	4.0	μA
V_O	Output voltage compliance	$E_r \leq 0.19\%$ at $T_A = +25°C$, Figure 5 $V_{EE} = -5V$ V_{EE} below $-10V$		−0.6, +10 −5.5, +10	−0.55, +0.5 −5.0, +0.5		−0.6, +10 −5.5, +10	−0.55, +0.5 −5.0, +0.5		−0.6, +10 −5.5, +10	−0.55, +0.5 −5.0, +0.5	V_{DC}
SRI_{REF}	Reference current slew rate	Figure 6		8.0			8.0			8.0		mA/μs
PSRR(−)	Output current power supply sensitivity	$I_{REF} = 1mA$		0.5	2.7		0.5	2.7		0.5	2.7	μA/V
I_{CC} I_{EE}	Power supply current Positive Negative	All bits low, Figure 5		+2.5 −6.5	+22 −13		+2.5 −6.5	+22 −13		+2.5 −6.5	+22 −13	mA
V_{CCR} V_{EER}	Power supply voltage range Positive Negative	$T_A = +25°C$, Figure 5	+4.5 −4.5	+5.0 −15	+5.5 −16.5	+4.5 −4.5	+5.0 −15	+5.5 −16.5	+4.5 −4.5	+5.0 −15	+5.5 −16.5	V_{DC}
P_D	Power Dissipation	All bits low, Figure 5 $V_{EE} = -5.0V_{DC}$ $V_{EE} = -15V_{DC}$		34 110	170 305		34 110	170 305		34 110	170 305	mW

NOTE:
1. All bits switched.

TYPICAL PERFORMANCE CHARACTERISTICS



FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into Pin 14 regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. R_{15} may be eliminated and Pin 15 grounded, with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increasing values of R_{14} to maintain proper phase margin. For R_{14} values of 1.0, 2.5, and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply).

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15}, as shown in Figure 2. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at Pin 15.

Capacitive bypass to ground is recommended when a DC reference voltage is used. The 5.0V logic supply is not recommended as a reference voltage, but if a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be formed of two series resistors and the junction of the two resistors bypassed with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage at Pin 4 must always be at least 4.5V more positive than the voltage of the negative supply (Pin 3) when the reference current is 2mA or less, and at least 8V more positive than the negative supply when the reference current is between 2mA and 4mA. This is necessary to avoid saturation of the output transistors, which would cause serious degradation of accuracy.

Signetics' MC1508/MC1408 does not need a range control because the design extends the compliance range down to 4.5V (or 8V — see above) above the negative supply voltage without significant degradation of accuracy. Signetics' MC1508/MC1408 can be used in sockets designed for other manufacturers' MC1508/MC1408 without circuit modification.

Output Current Range

Any time the full-scale current exceeds 2mA, the negative supply must be at least 8V more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full-scale accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current after zero-scale current has been nulled out. The relative accuracy of the MC1508/MC1408 is essentially constant over the operating temperature range because of the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current; however, the MC1508/MC1408 has a very low full-scale current drift over the operating temperature range.

The MC1508/MC1408 series is guaranteed accurate to within ± ½ LSB at +25°C at a full-scale output current of 1.99mA. The relative accuracy test circuit is shown in Figure 3. The 12-bit converter is calibrated to a full-scale output current of 1.99219mA; then the MC1508/MC1408's full-scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total of ± ½ part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification of the MC1508/MC1408.

Monotonicity

A monotonic converter is one which always provides an analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The MC1508/MC1408 is monotonic for all values of reference current above 0.5mA. The recommended range for operation is a DC reference current between 0.5mA and 4.0mA.

Settling Time

The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70ns for settling to within ½ LSB for 8-bit accuracy. This time applies when $R_L < 500\Omega$ and $C_O < 25pF$. The slowest single switch is the least significant bit, which typically turns on and settles in 65ns. In applications where the D-to-A converter functions in a positive going ramp mode, the worst-case condition does not occur and settling times less than 70ns may be realized.

Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, minimum scope lead length, good ground planes, and avoidance of ground loops are all mandatory.

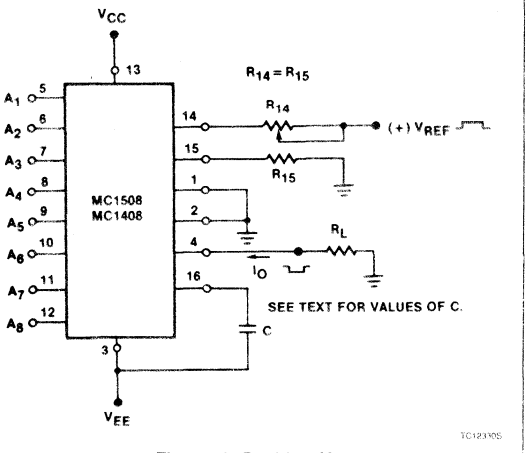


Figure 1. Positive V_{REF}

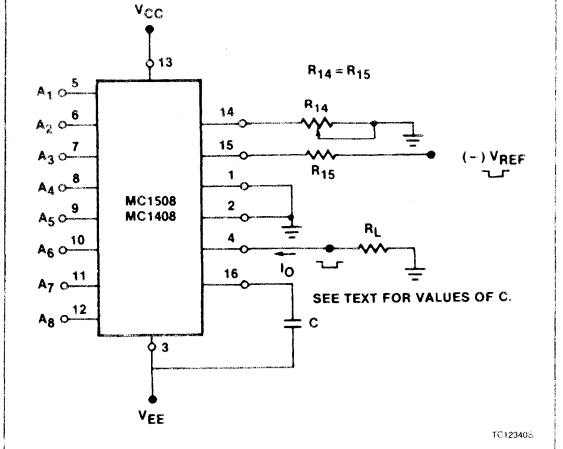


Figure 2. Negative V_{REF}

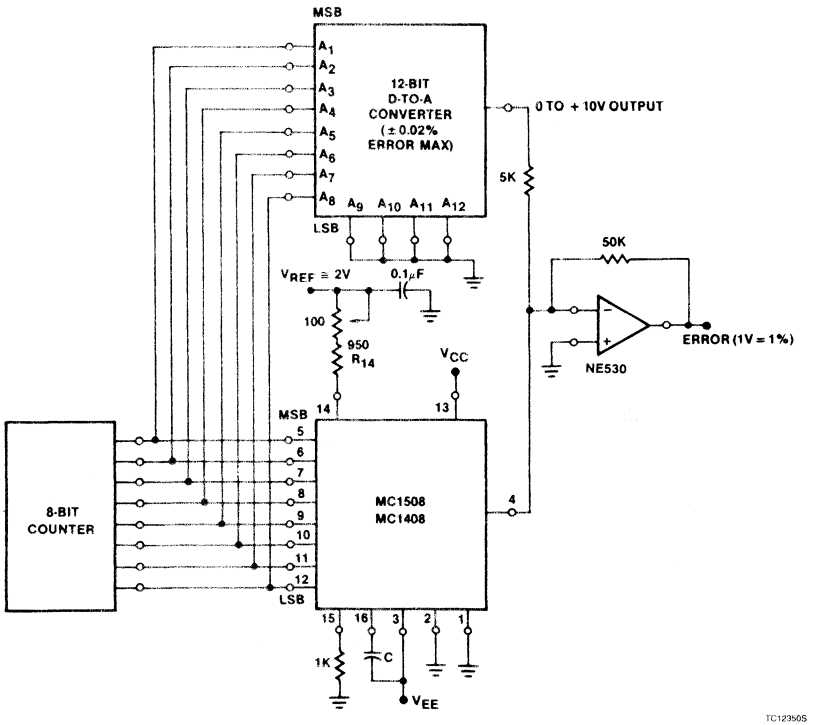


Figure 3. Relative Accuracy

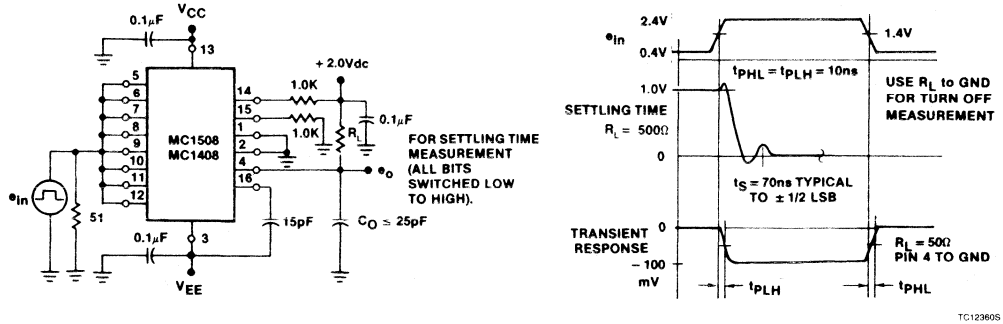


Figure 4. Transient Response and Settling Time

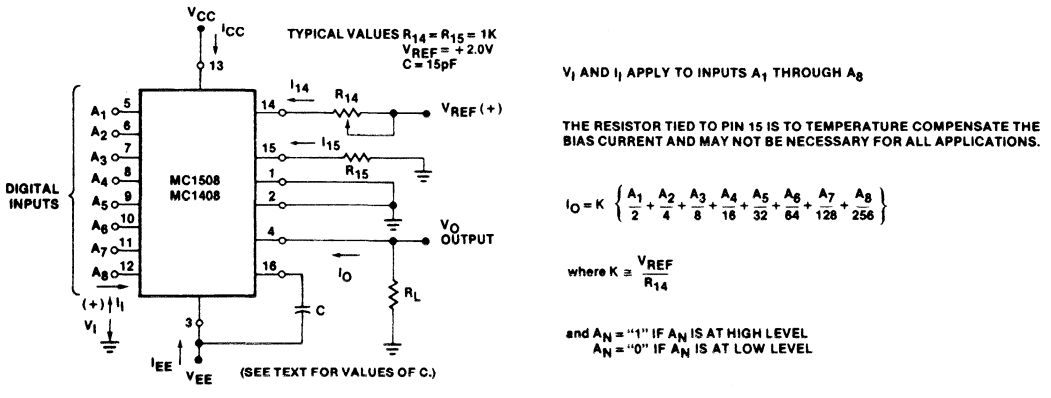


Figure 5. Notation Definitions

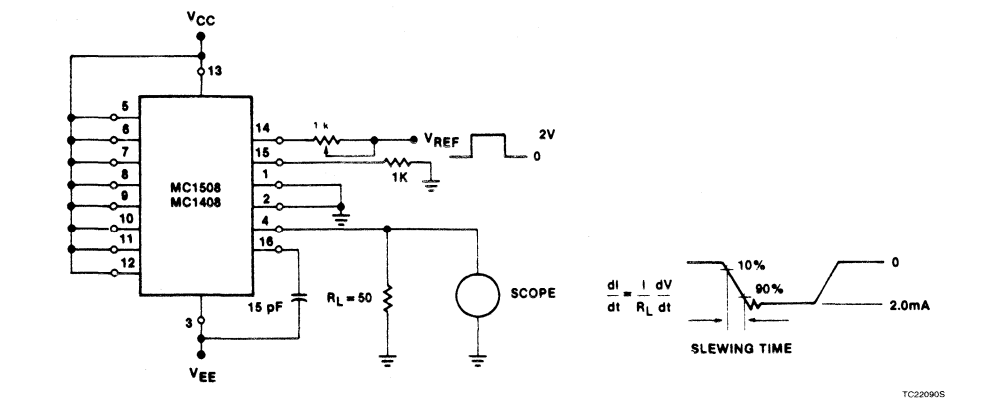


Figure 6. Reference Current Slew Rate Measurement

MC3410, MC3510, MC3410C

10-Bit High-Speed Multiplying D/A Converter

Product Specification

DESCRIPTION

The MC3410 series are 10-bit Multiplying Digital-to-Analog Converters. They are capable of high-speed performance, and are used as general-purpose building blocks in cost-effective D/A systems.

The Signetics' design provides complete 10-bit accuracy without laser trimming, and guaranteed monotonicity over temperature. Segmented current sources, in conjunction with an R-2R DAC provides the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

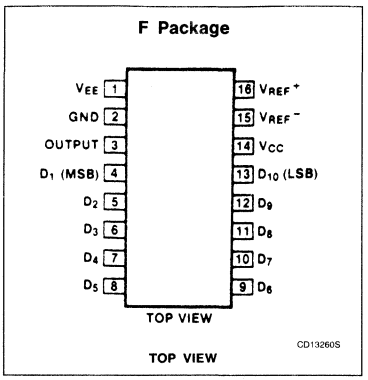
FEATURES

- **10-bit resolution and accuracy (± 0.05%)**
- **Guaranteed monotonicity over temperature**
- **Fast settling time — 250ns typical**
- **Digital inputs are TTL and CMOS compatible**
- **Wide output voltage compliance range**
- **High-speed multiplying input slew rate — 20mA/μs**
- **Reference amplifier internally-compensated**
- **Standard supply voltages +5V and −15V**

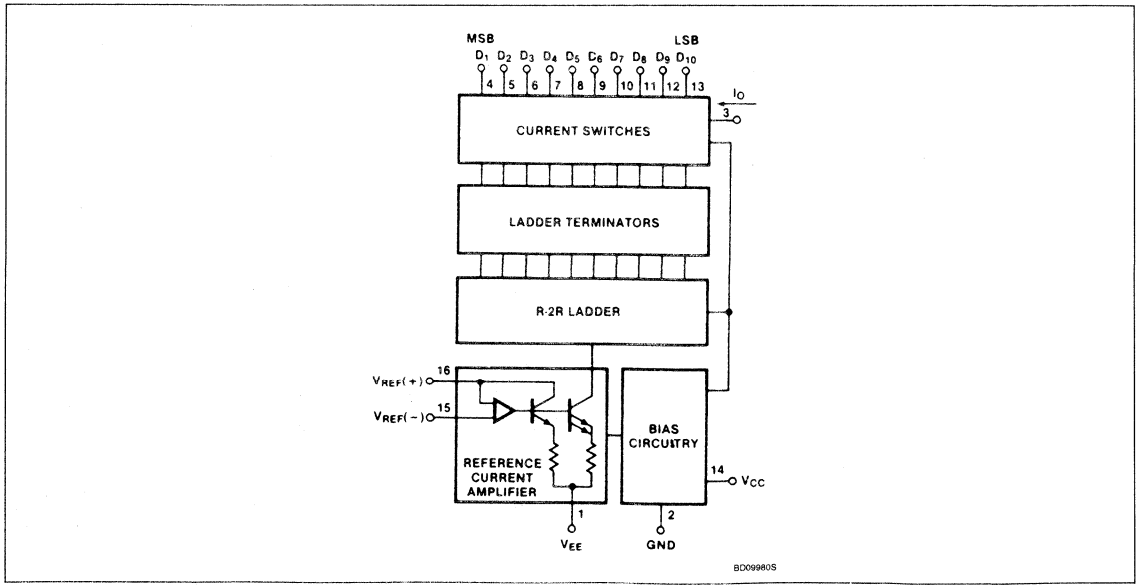
APPLICATIONS

- **Successive approximation A/D converters**
- **High-speed, automatic test equipment**
- **High-speed modems**
- **Waveform generators**
- **CRT displays**
- **Strip CHART and X-Y plotters**
- **Programmable power supplies**
- **Programmable gain and attenuation**

PIN CONFIGURATION



BLOCK DIAGRAM



10-Bit High-Speed Multiplying D/A Converter

MC3410, MC3510, MC3410C

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	MC3410F
16-Pin Cerdip	0 to +70°C	MC3410CF
16-Pin Cerdip	−55°C to +125°C	MC3510F

ABSOLUTE MAXIMUM RATINGS T_A = +25°C unless otherwise noted

SYMBOL	PARAMETER	RATING	UNIT
V_{CC} V_{EE}	Power supply	+7.0 −18	V_{DC} V_{DC}
V_I	Digital input voltage	+15	V_{DC}
V_O	Applied output voltage	0.5, −5.0	V_{DC}
$I_{REF(16)}$	Reference current	2.5	mA
V_{REF}	Reference amplifier inputs	V_{CC}, V_{EE}	V_{DC}
$V_{REF(D)}$	Reference amplifier differential inputs	0.7	V_{DC}
T_A	Operating ambient temperature range MC3510 MC3410, 3410C	 −55 to +125 0 to +70	 °C °C
T_J	Junction temperature, ceramic package	+150	°C
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1] F package	 1190	 mW

NOTE:
1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C

10-Bit High-Speed Multiplying D/A Converter

MC3410, MC3510, MC3410C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5.0V_{DC}, V_{EE} = −15$_{DC}$, $\frac{V_{REF}}{R16}$ = 2.0mA, all digital inputs at high logic level.

MC3510: T_A = −55°C to +125°C, MC3410 Series: T_A = 0°C to +70°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC3410, MC3510			MC3410C			UNIT
			Min	Typ	Max	Min	Typ	Max	
E_r	Relative accuracy (error relative to full-scale I_O)	T_A = 25°C			±0.05			±0.1	%
					1/4			1/2	LSB
TCE_r	Relative accuracy drift (relative to full-scale I_O)			2.5			2.5		ppm/°C
	Monotonicity	Over temperature	10			10			Bits
t_S	Settling time to within ± 1/2 LSB (all bits LOW-to-HIGH)	T_A = 25°C		250			250		ns
t_{PLH} t_{PHL}	Propagation delay time	T_A = 25°C		35 20			35 20		ns
TCI_O	Output full scale current drift				60			70	ppm/°C
V_{IH}	Digital input logic levels (all bits) HIGH-level, Logic "1" LOW-level, Logic "0"		2.0		0.8	2.0		0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (all bits) HIGH-level, V_{IH} = 5.5V LOW-level, V_{IL} = 0.8V			 −0.05	+.04 −0.4		 −0.05	+.04 −0.4	mA
$I_{REF(15)}$	Reference input bias current (Pin 15)			−1.0	−5.0		−1.0	−5.0	μA
I_{OR}	Output current range			4.0	5.0		4.0	5.0	mA
I_{OH}	Output current (all bits high)	V_{REF} = 2.000V, R_{16} = 1000Ω	3.8	3.996	4.2	3.8	3.996	4.2	mA
I_{OL}	Output current (all bits low)	T_A = 25°C		0	2.0		0	4.0	μA
V_O	Output voltage compliance	T_A = 25°C			−2.5 +0.2			−2.5 +0.2	V_{DC}
SR I_{REF}	Reference amplifier slew rate			20			20		mA/μs
ST I_{REF}	Reference amplifier settling time	0 to 4.0mA, ±0.1%		2.0			2.0		μs
PSRR(−)	Output current power supply sensitivity			0.003	0.01		0.003	0.02	%/%
C_O	Output capacitance	V_O = 0		25			25		pF
C_I	Digital input capacitance (all bits high)			4.0			4.0		pF
I_{CC} I_{EE}	Power supply current (all bits low)			 −11.4	+18 −20		 −11.4	+18 −20	mA
V_{CC} V_{EE}	Power supply voltage range	T_A = 25°C	+4.75 −14.25	+5.0 −15	+5.25 −15.75	+4.75 −14.25	+5.0 −15	+5.25 −15.75	V_{DC}
	Power consumption (all bits low) (all bits high)			 220 200	 380		 220 200	 380	mW

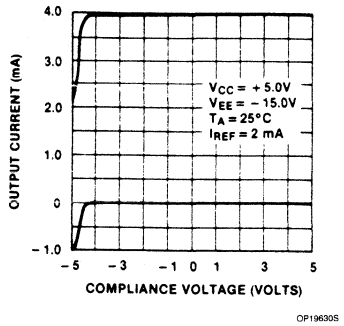


Figure 1. Output Current vs Output Compliance Voltage

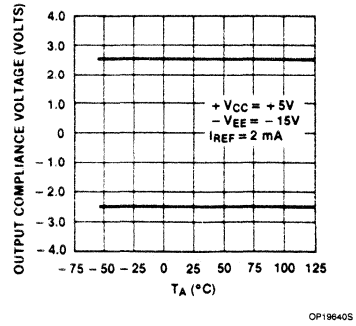


Figure 2. Maximum Output Compliance Voltage vs Temperature

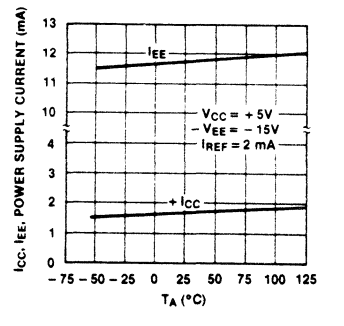


Figure 3. Power Supply Current vs Temperature

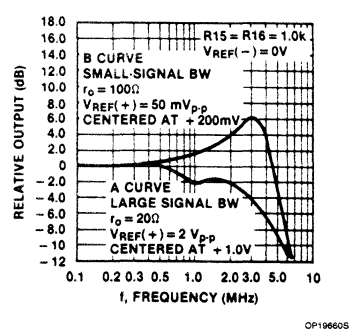


Figure 4. Reference Amplifier Frequency Response

10-Bit High-Speed Multiplying D/A Converter

MC3410, MC3510, MC3410C

CIRCUIT DESCRIPTION

The MC3410 consists of four segment current sources which generate the two most significant bits (MSBs), and an R-2R DAC implemented with ion-implanted resistors for scaling the remaining eight least significant bits (LSBs) (See Figure 5). This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully differential current switches. The switches use current steering for speed.

An on-chip high-slew reference current amplifier drives the R-2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input. Out-board resistor R_{16} (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0V and a 1kΩ resistor tied to Pin 16, the full-scale current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R_{16} should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R_{16} to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R_{16} should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1μF capacitor to ground.

The reference amplifier is internally-compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R_{16} and reference voltages which supply 2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R_{16} increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R_{16} = 1.0kΩ, and settling time is ≈ 10μs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

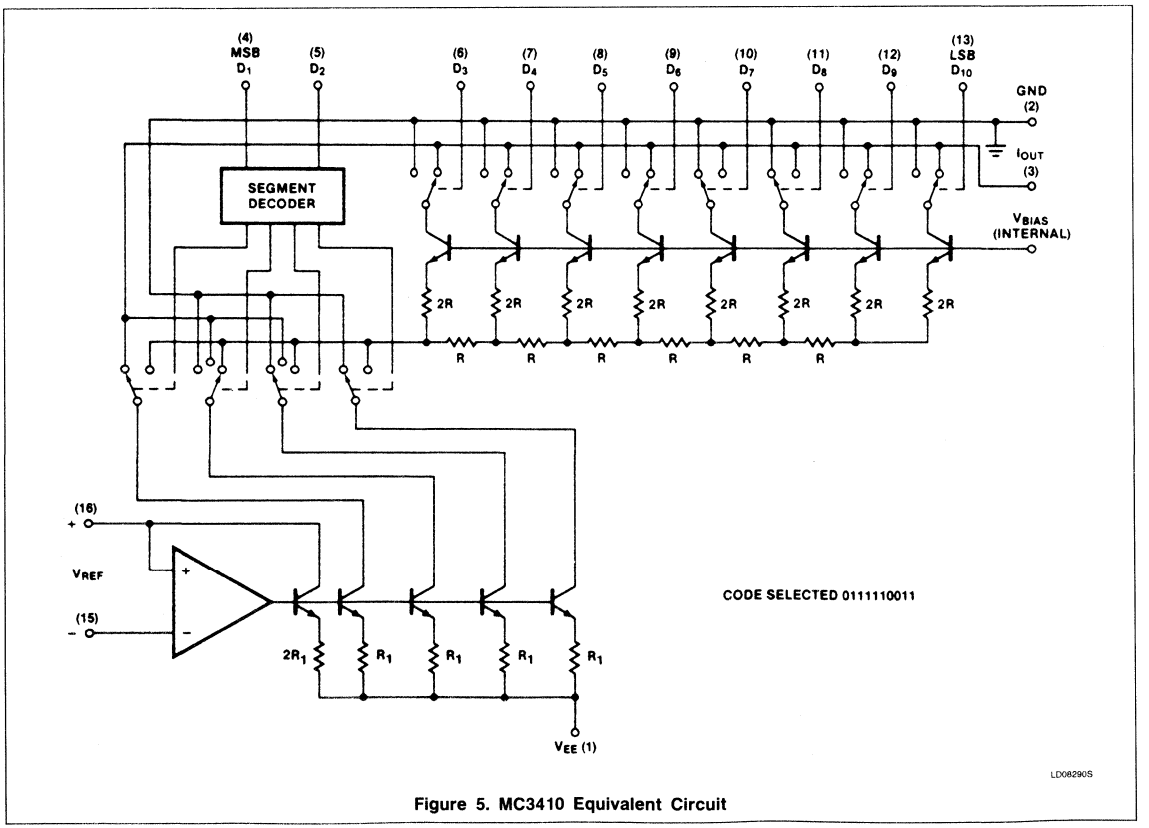
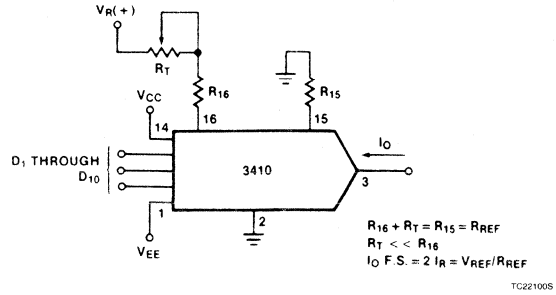


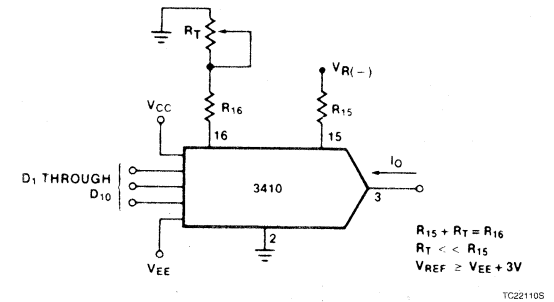
Figure 5. MC3410 Equivalent Circuit

10-Bit High-Speed Multiplying D/A Converter

MC3410, MC3510, MC3410C



a. Positive Reference Voltage



b. Negative Reference Voltage

Figure 6. Basic Connections

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from −2.5 to +0.2V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if $V_{EE} > -15V$.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full-scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full-scale current. The relative accuracy of the MC3410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full-scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the MC3410 has a low full-scale current drift with temperature.

The MC3510 and the MC3410 are accurate to within ±0.05% at 25°C with a reference current of 2.0mA on Pin 16.

MONOTONICITY

The MC3410, MC3510 and MC3410C are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250ns for the output to settle to within ± ½ LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (< 0.7V) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625Ω is connected to ground, allowing the output to swing to −2.5V, the settling time increases to 1.5μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

A typical test setup for measuring settling time is shown in Figure 7. The same setup for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.

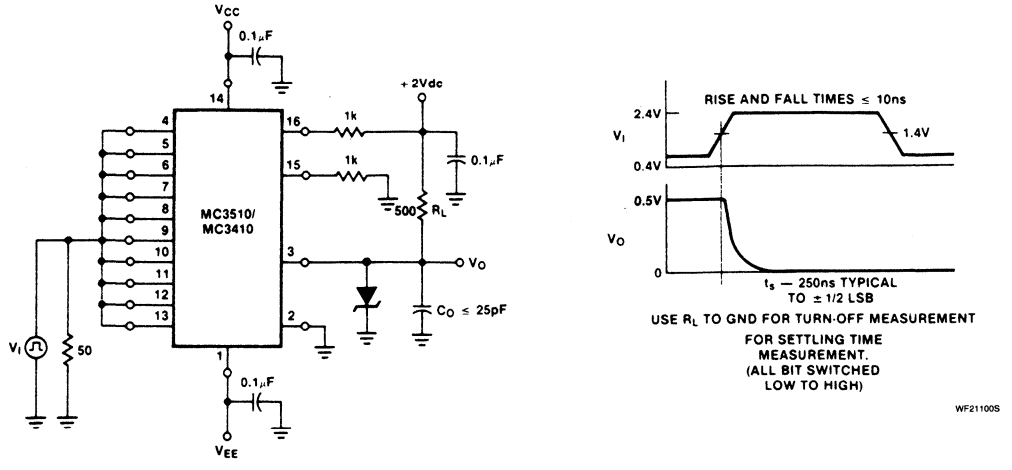


Figure 7. Settling Time

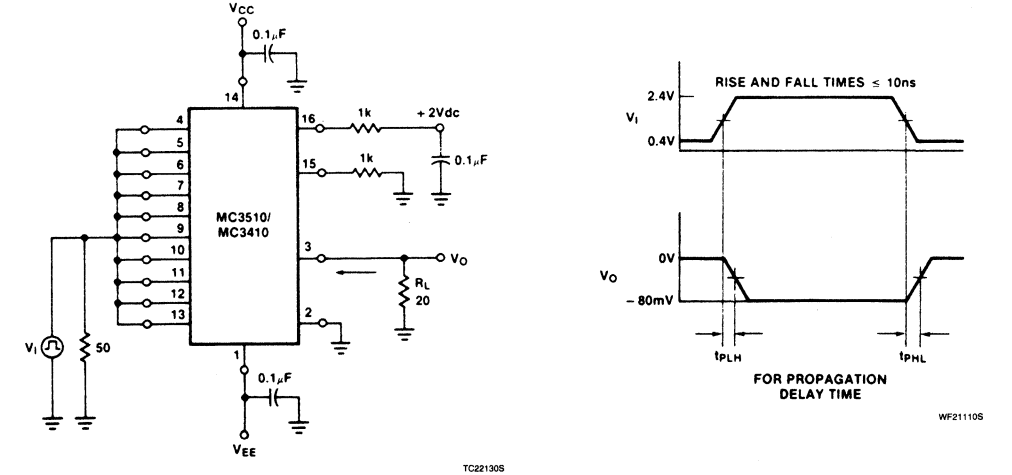


Figure 8. Propagation Delay Time

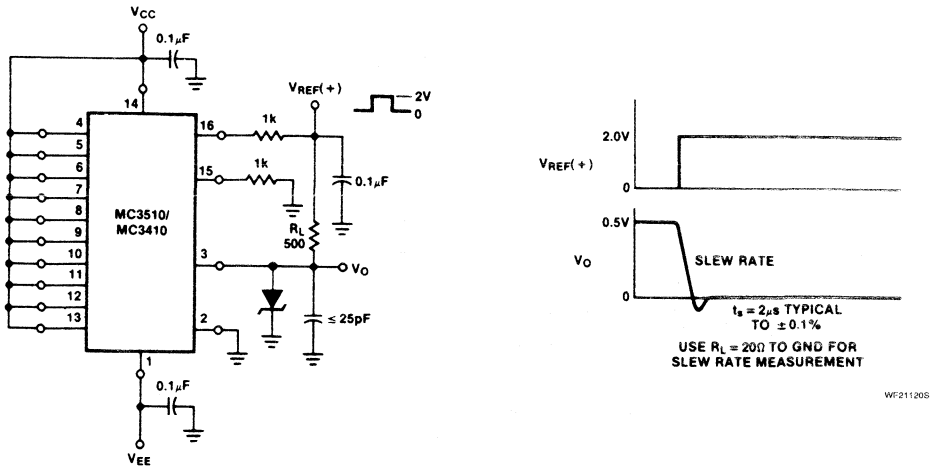
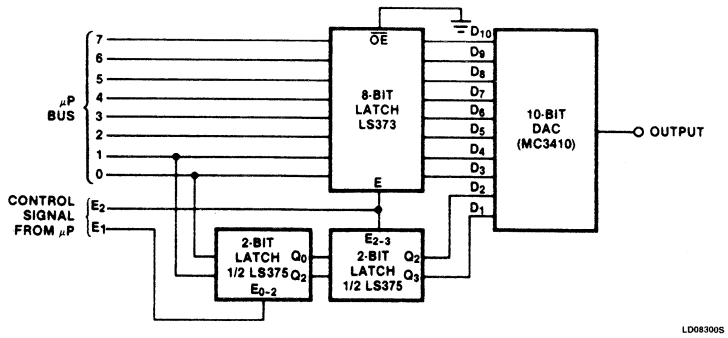
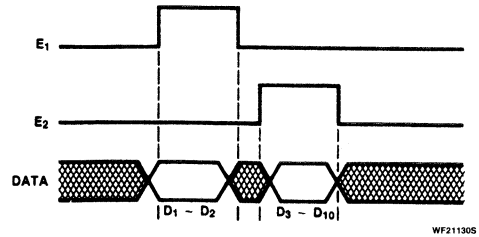


Figure 9. Reference Amplifier Settling Time and Slew Rate

TYPICAL APPLICATIONS





THE VALID DATA WILL BE LATCHED TO THE DAC UNTIL UPDATED WITH E_2 PULSE.
TIMING WILL DEPEND ON THE PROCESSOR USED.

Figure 10. Interfacing 10-Bit DAC With 8-Bit Microprocessor

NE/SE5018
8-Bit μP-Compatible D/A Converter

Product Specification

DESCRIPTION

The NE/SE5018/19 is a complete 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches which are controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale while maintaining a low temperature coefficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

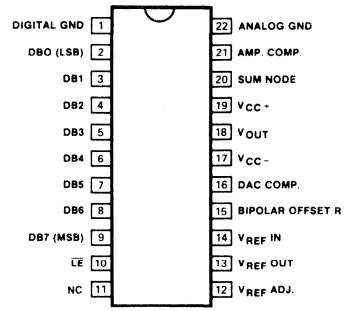
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± ½ LSB (0.19%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other μPs**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog – digital multiplication**

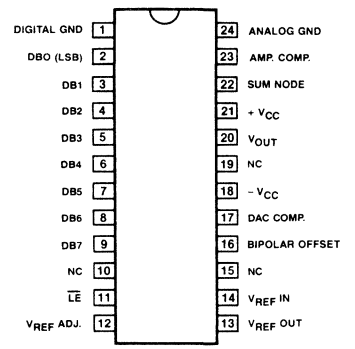
PIN CONFIGURATIONS

F, N Packages



CD09820S

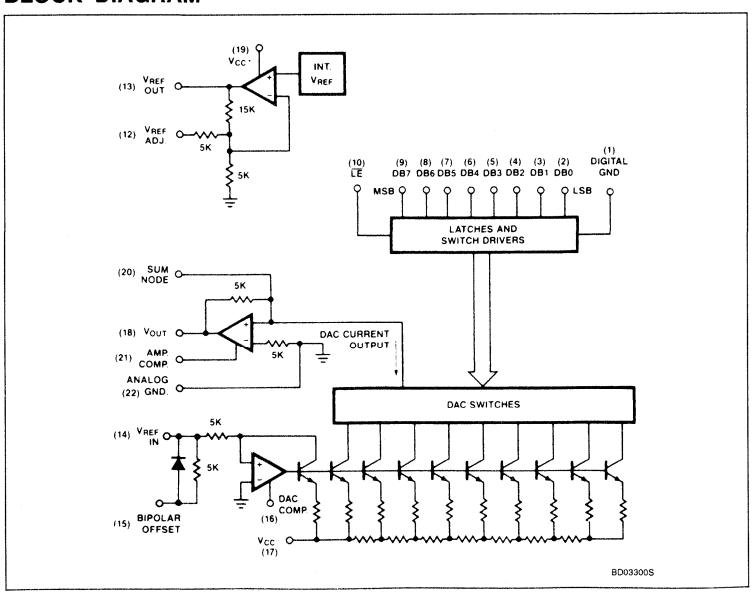
D Package[1]



CD09830S

NOTE:
1. SOL and non-standard pinout.

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
22-Pin Cerdip	0 to +70°C	NE5018F
22-Pin Cerdip	−55°C to +125°C	SE5018F
22-Pin Plastic DIP	0 to +70°C	NE5018N
22-Pin Plastic DIP	−55°C to +125°C	SE5018N
24-Pin SOL Package	0 to +70°C	NE5018D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at V_{REF} input	12	V
V_{REF} ADJ	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
$I_{REF\ SC}$	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1] F package N package D package	 1740 2190 1600	 mW mW mW
T_A	Operating temperature range SE5018 NE5018	 −55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   F package at 13.9mW/°C.
   N package at 17.5mW/°C.
   D package at 12.8mW/°C.

DC ELECTRICAL CHARACTERISTICS $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5018			NE/SE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, 2V < V_{IN} < 18V		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, −5V < V_{IN} < 0.8V		−2.0	−10		−2.0	−10	μA
V_{FS}	Full-scale output	Unipolar mode, V_{REF} = 5.000V, all bits high, T_A = 25°C	9.50		10.5	9.50		10.5	V
$+V_{FS}$	Full-scale output	Bipolar mode, V_{REF} = 5.000V all bits high, T_A = 25°C	4.75		5.25	4.75		5.25	V
$-V_{FS}$	Negative full scale	Bipolar mode, V_{REF} = 5.000V, all bits low, T_A = 25°C	−5.25		−4.75	−5.25		−4.75	V
V_{ZS}	Zero-scale Output	Unipolar mode, V_{REF} = 5.000V all bits low, T_A = 25°C	−30		+30	−30		+30	mV
I_{OS}	Output short circuit current	T_A = 25°C, V_{OUT} = 0V		15	40		15	40	mA
$PSR+_{(OUT)}$	Output power supply rejection (+)	V− = −15V, 13.5V ≤ V+ ≤ 16.5V, external $V_{REF\ IN}$ = 5.000V		0.001	0.01		0.001	0.01	%FS %VS
$PSR-_{(OUT)}$	Output power supply rejection (−)	V+ = −15V, −13.5V ≤ V− ≤ −16.5V, external $V_{REF\ IN}$ = 5.000V		0.001	0.01		0.001	0.01	%FS %VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN}$ = 5.000V		20			20		ppm/°C
TC_{ZS}	Zero-scale temperature coefficient			5			5		ppm/°C
I_{REF}	Reference output current				3			3	mA
I_{REFSC}	Reference short circuit current	T_A = 25°C[8] $V_{REF\ OUT}$ = 0V		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	V− = −15V, 13.5V ≤ V+ ≤ 16.5V, I_{REF} = 1.0mA		0.003	0.01		0.003	0.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	V+ = −15V, −13.5V ≤ V− ≤ 16.5V,		0.003	0.01		0.003	0.01	%VR/%VS
V_{REF}	Reference voltage	I_{REF} = 1.0mA T_A = 25°C	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	I_{REF} = 1.0mA		60			60		ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	I_{REF} = 1.0mA, T_A = 25°C	4.15	5.0	5.85	4.15	5.0	5.85	kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+$ = 15V		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}-$ = −15V		−10	−15		−10	−15	mA
P_D	Power dissipation	I_{REF} = 1.0mA, V_{CC} = ±15V		255	435		255	435	mW

NOTE:
1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[1] $V_{CC} = \pm 15V$, $T_A = 25°C$.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	NE/SE5018/19			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	± ½ LSB	Input	All bits low-to-high[2]		1.8		μs
t_{SHL}	Settling time	± ½ LSB	Input	All bits high-to-low[3]		2.3		μs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high[2]		300		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low[3]		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change[2, 3]		150		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition[4]		300		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition[5]		150		ns
t_S	Setup time	$\overline{LE}$	Input	1, 6	100			ns
t_H	Hold time	Input	$\overline{LE}$	1, 6	50			ns
t_{PW}	Latch enable pulse width			1, 6	150			ns

NOTES:
1. Refer to Figure 3.
2. See Figure 6.
3. See Figure 7.
4. See Figure 8.
5. See Figure 9.
6. See Figure 10.
7. For reference currents > 3mA, use of an external buffer is required.

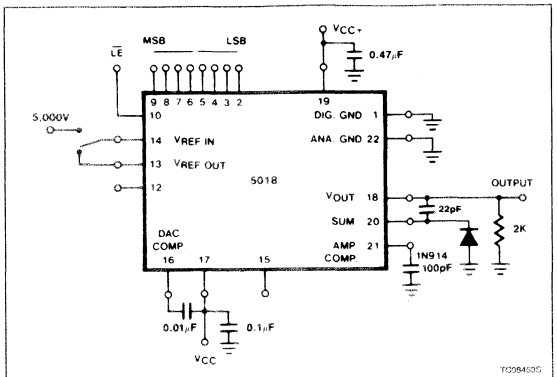


Figure 2. DC Parametric Test Configuration

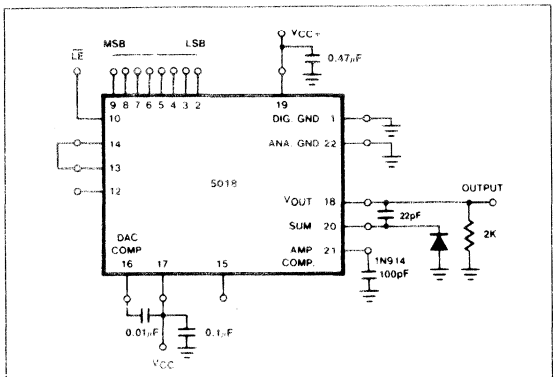


Figure 3. AC Parametric Test Configuration

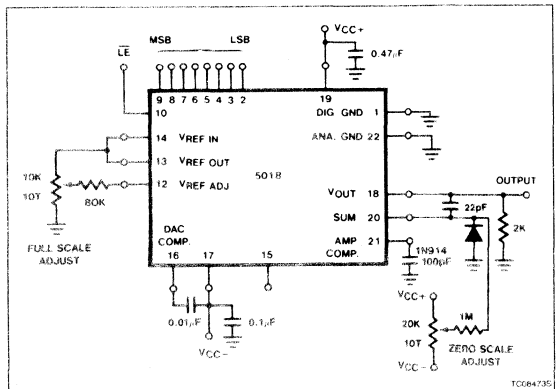


Figure 4. Full-/Zero-Scale Adjust — Unipolar Output (0 – 10V)

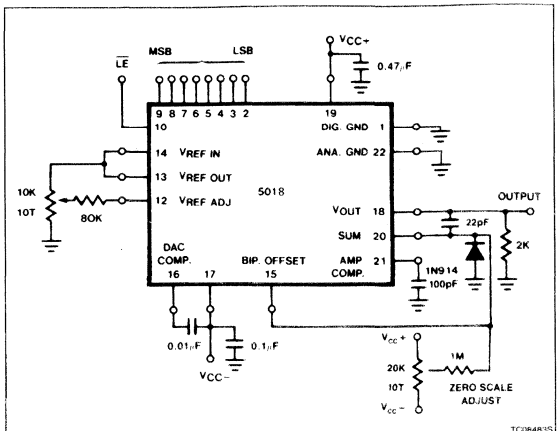


Figure 5. Bipolar Output Operation (– 5 to + 5V)

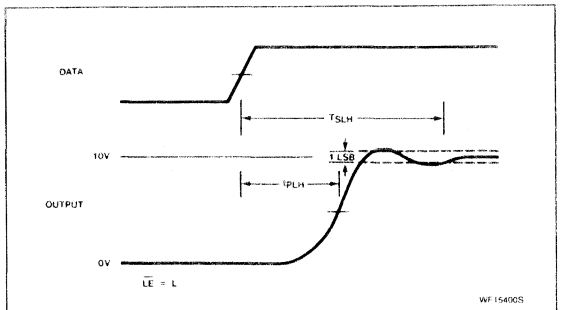


Figure 6. Settling Time and Propagation Delay, Low-to-High Data

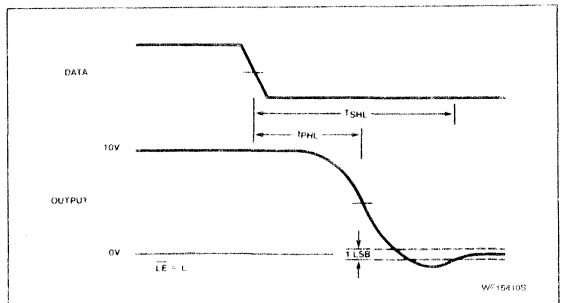


Figure 7. Settling Time and Propagation Delay, High-to-Low Data

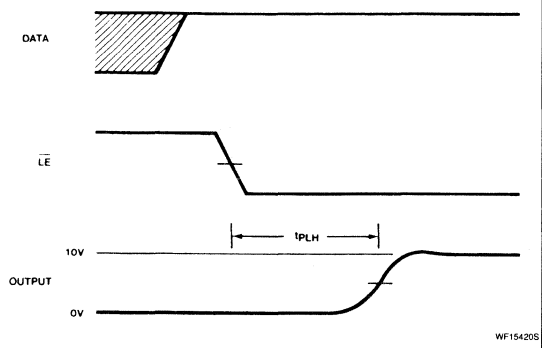


Figure 8. Propagation Delay, Latch Enable to Output

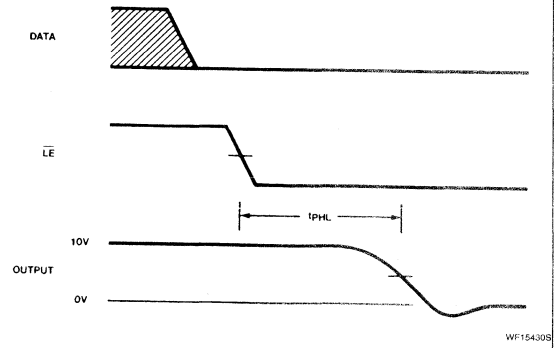


Figure 9. Propagation Delay, Latch Enable to Output

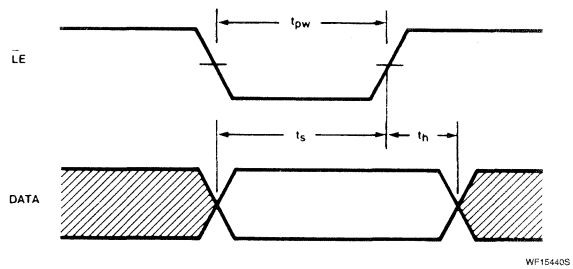


Figure 10. Latch Enable Pulse Width, Setup and Hold Times

NE/SE5019
8-Bit μP-Compatible D/A Converter

Product Specification

DESCRIPTION

The NE5019 is a complete 8-bit digital-to-analog converter sub-system on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale, while maintaining a low temperature coefficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

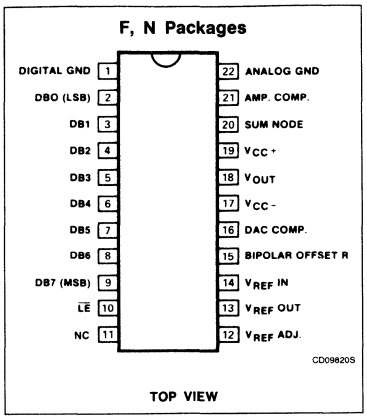
FEATURES

- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± ¼ LSB (0.1%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other μPs**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog – digital multiplication**

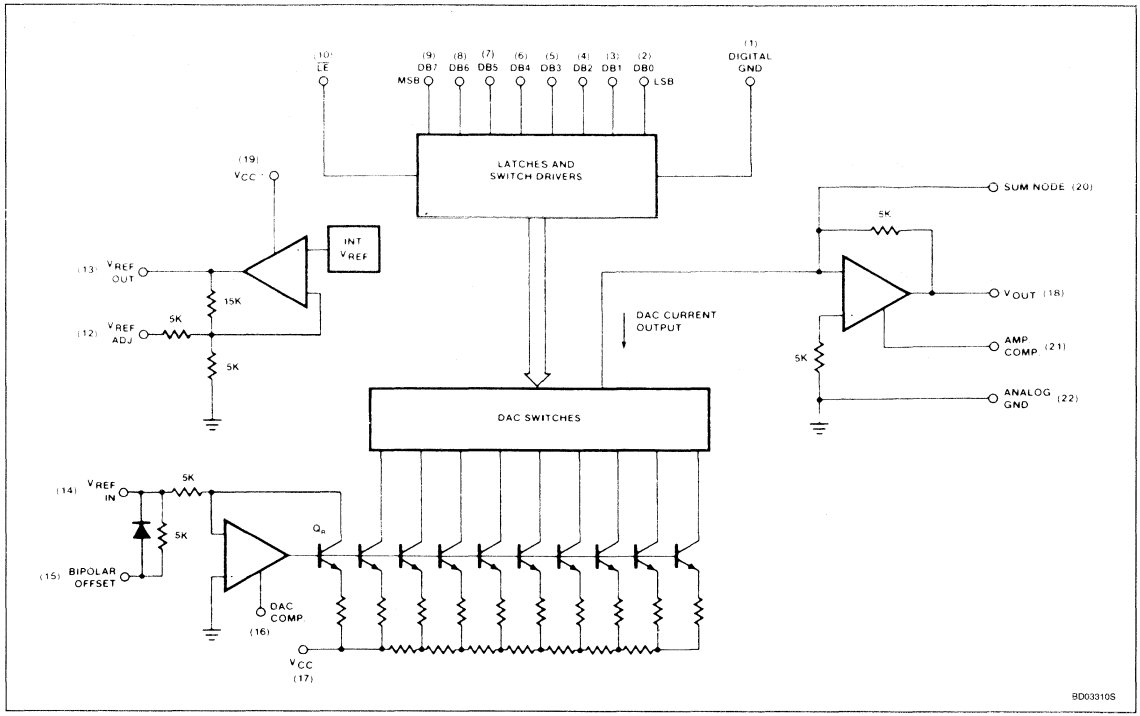
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
22-Pin Cerdip	−55°C to +125°C	SE5019F
22-Pin Cerdip	0 to +70°C	NE5019F
22-Pin Plastic DIP	0 to +70°C	NE5019N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_I	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at V_{REF} input	12	V
$V_{REF\ ADJ}$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
$I_{REF\ SC}$	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	mA
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	mA
P_D	Maximum power dissipation, $T_A = 25°C$, (still-air)[1] F package N package	 1740 2190	 mW mW
T_A	Operating temperature range SE5019 NE5019	 −55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTE:
1. Derate above 25°C at the following rates:
   F package at 13.9mW/°C.
   N package at 17.5mW/°C.

DC ELECTRICAL CHARACTERISTICS $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leq T_A \leq 125°C$, NE5019. $0°C \leq T_A \leq 70°C$, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full-scale output	Unipolar mode, $V_{REF} = 5.000V$, all bits high, $T_A = 25°C$	9.5		10.5	9.5		10.5	V
$+V_{FS}$	Full-scale output	Bipolar mode, $V_{REF} = 5.000V$, all bits high, $T_A = 25°C$	4.75		5.25	4.75		5.25	V
$-V_{FS}$	Negative full-scale	Bipolar mode, $V_{REF} = 5.000V$, all bits low, $T_A = 25°C$	−5.25		−4.75	−5.25		−4.75	V
V_{ZS}	Zero-scale output	Unipolar mode, $V_{REF} = 5.000V$, all bits low, $T_A = 25°C$	−30		+30	−30		+30	mV
I_{OS}	Output short circuit current	$T_A = 25°C$, $V_{OUT} = 0V$		15	40		15	40	mA
$PSR+_{(out)}$	Output power supply rejection (+)	V− = −15V, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		0.001	0.01		0.001	0.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	V+ = 15V, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		0.001	0.01		0.001	0.01	%FS/%VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero-scale temperature coefficient			5			5		ppm/°C

NOTE:
Refer to Figure 1.

DC ELECTRICAL CHARACTERISTICS (Continued)

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leq T_A \leq 125°C$, NE5019. $0°C \leq T_A \leq 70°C$, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 8			3			3	mA
$I_{REF\ SC}$	Reference short circuit current	$T_A = 25°C$, $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	V- = -15V, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		0.003	0.01		0.003	0.01	%VR/%VS
$PSR-_{REF}$	Reference power supply rejection (-)	V+ = 15V, $-13.5V \leq V- \leq 16.5V$		0.003	0.01		0.003	0.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.15	5.0	5.85	4.15	5.0	5.85	kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		-10	-15		-10	-15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE:
Refer to Figure 1.

AC ELECTRICAL CHARACTERISTICS[1]

$V_{CC} = \pm 15V$, $T_A = 25°C$[2].

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	NE/SE5019			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	± ½ LSB	Input	All bits low-to-high[2]		1.8		μs
t_{SHL}	Settling time	± ½ LSB	Input	All bits high-to-low[3]		2.3		μs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high[2]		300		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low[3]		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change[2, 3]		150		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition[4]		300		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition[5]		150		ns
t_S	Setup time	$\overline{LE}$	Input	[1, 6]	100			ns
t_H	Hold time	Input	$\overline{LE}$	[1, 6]	50			ns
t_{PW}	Latch enable pulse width			[1, 6]	150			ns

NOTES:
1. Refer to Figure 2.
2. See Figure 5.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. For reference current > 3mA, use of an external buffer is required.

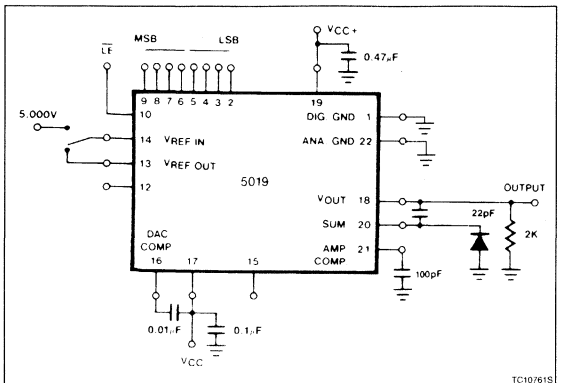


Figure 1. DC Parametric Test Configuration

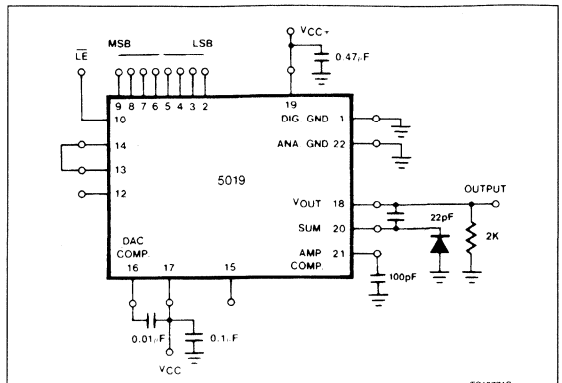


Figure 2. AC Parametric Test Configuration

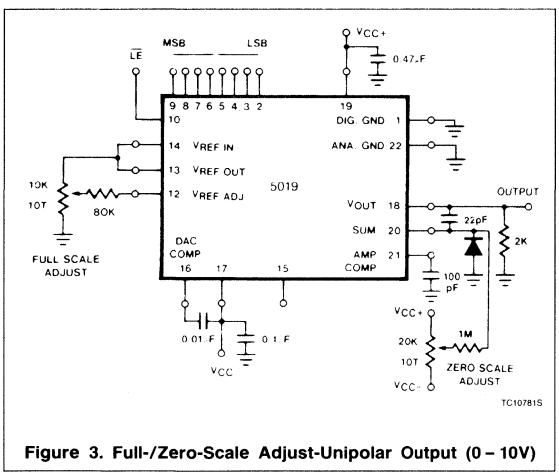


Figure 3. Full-/Zero-Scale Adjust-Unipolar Output (0 – 10V)

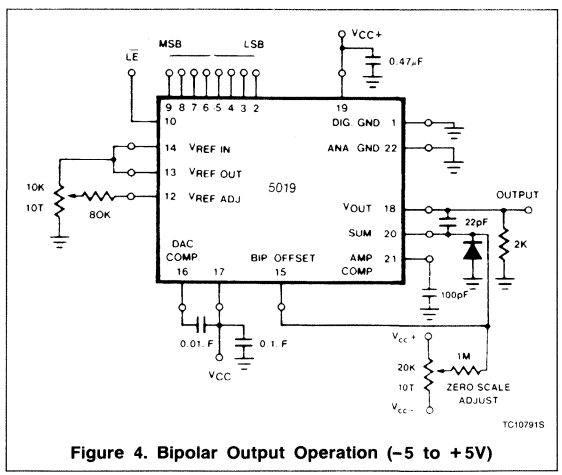


Figure 4. Bipolar Output Operation (–5 to +5V)

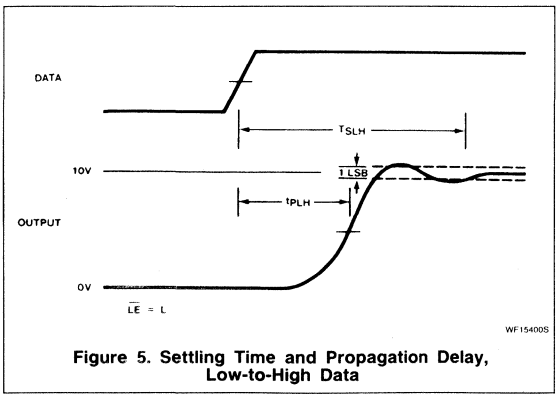


Figure 5. Settling Time and Propagation Delay, Low-to-High Data

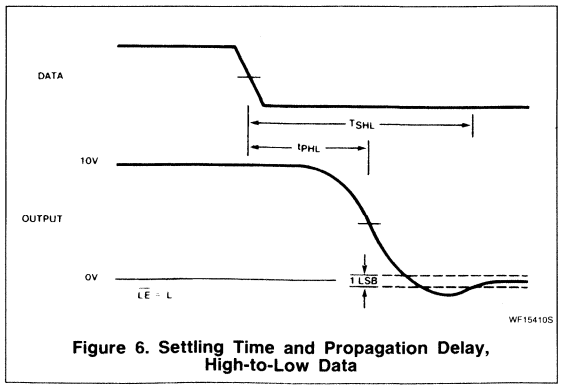


Figure 6. Settling Time and Propagation Delay, High-to-Low Data

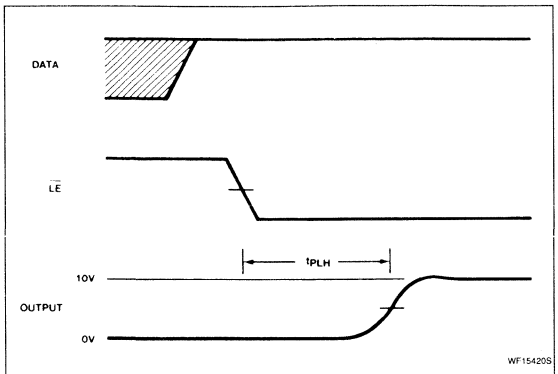


Figure 7. Propagation Delay, Latch Enable to Output

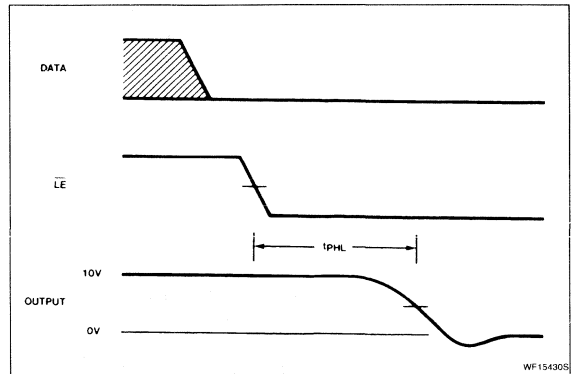


Figure 8. Propagation Delay, Latch Enable to Output

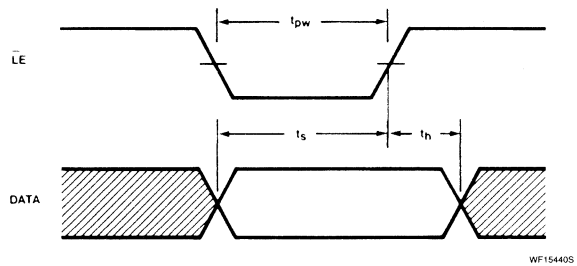


Figure 9. Latch Enable Pulse Width, Setup and Hold Times

NOT FOR NEW DESIGN

NE5020
10-Bit μP-Compatible D/A Converter

Product Specification

DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital-to-analog converter subsystem. This device offers 10-bit resolution and ±0.1% accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds, and addressing capability allow the NE5020 to directly interface with most microprocessor- and logic-controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

FEATURES

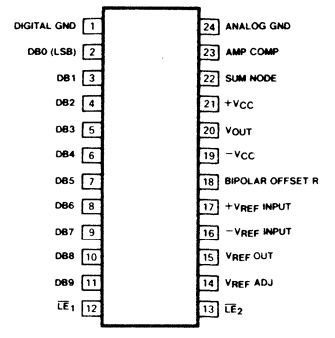
- **10-bit resolution**
- **Guaranteed monotonicity over operating range**
- **±0.1% relative accuracy**
- **Unipolar (0V to +10V) and bipolar (±5V) output range**
- **Logic bus compatible**
- **5μs settling time**

APPLICATIONS

- **Precision 10-bit D/A converters**
- **10-bit analog-to-digital converters**
- **Programmable power supplies**
- **Test equipment**
- **Measurement instruments**

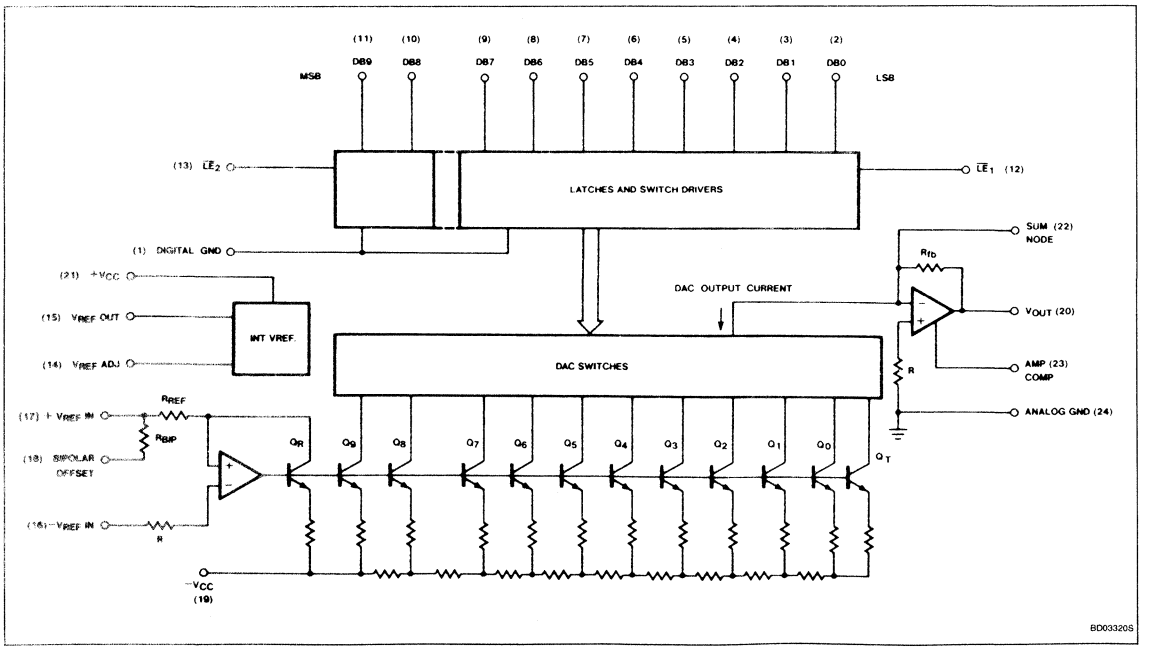
PIN CONFIGURATION

F, N Packages



TOP VIEW CD10050S

BLOCK DIAGRAM



10-Bit μP-Compatible D/A Converter — NE5020

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Cerdip	0 to 70°C	NE5020F
24-Pin Plastic DIP	0 to 70°C	NE5020N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}^+	Positive supply voltage	18	V
V_{CC}^-	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at $+V_{REF}$ input	12	V
$V_{REF\ ADJ}$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Maximum power dissipation T_A = 25°C, (still-air)[1] F package N package	 2150 2150	 mW mW
T_A	Operating temperature range NE5020	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   F package at 17.2mW/°C.
   N package at 17.2mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0 \leq T_A \leq 70°C$, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution Monotonicity Relative accuracy				10 10 ±0.1	Bits Bits %FS
V_{CC}^+ V_{CC}^-	Positive supply voltage Negative supply voltage		11.4 −11.4	15 −15	16.5 −16.5	V V
$V_{IN(1)}$ $V_{IN(0)}$	Logic "1" input voltage Logic "0" input voltage	Pin 1 = 0V Pin 1 = 0V	2.0		 0.8	V V
$I_{IN(1)}$ $I_{IN(0)}$	Logic "1" input current Logic "0" input current	Pin 1 = 0V, $2 < V_{IN} < 18V$ Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		0.1 −2.0	10 −10	μA μA
V_{FS}	Full-scale output	Unipolar mode, V_{REF} = 5.000V, all bits high, T_A = 25°C	9.5		10.5	V
$+V_{FS}$	Full-scale output	Bipolar mode, V_{REF} = 5.000V, all bits high, T_A = 25°C	4.75		5.25	V
$-V_{FS}$	Negative full-scale	Bipolar mode, V_{REF} = 5.000V, all bits low, T_A = 25°C	−5.25		−4.75	V

NOTE:
1. Refer to Figure 1.

DC ELECTRICAL CHARACTERISTICS (Continued)

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0 \leq T_A \leq 70°C$, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{ZS}	Zero-scale output	Unipolar mode, $V_{REF} = 5.000V$, all bits low, $T_A = 25°C$	-30		+30	mV
I_{OS}	Output short-circuit current	$T_A = 25°C$, $V_{OUT} = 0V$		±15	±40	mA
$PSR+_{(OUT)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		0.001	0.01	%FS/%VS
$PSR-_{(OUT)}$	Output power supply rejection (-)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		0.001	0.01	%FS/%VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20		ppmFS/°C
TC_{ZS}	Zero-scale temperature coefficient			5		ppmFS/°C
I_{REF}[2]	Reference output current				3	mA
$I_{REF\ SC}$	Reference short circuit current	$T_A = 25°C$, $V_{REF\ OUT} = 0V$		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01	%VR/%VS
$PSR-_{REF}$	Reference power supply rejection (-)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60		ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	$I_{REF} = 1.0mA$		5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		-10	-15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435	mW

NOTE:
1. Refer to Figure 1.
2. For $I_{REF\ OUT}$ greater than 3mA, an external buffer is required.

AC ELECTRICAL CHARACTERISTICS[1]

$V_{CC} = \pm 15V$, $T_A = 25°C$.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	± ½ LSB	Input	All bits low-to-high[2]		5		μs
t_{SHL}	Settling time	± ½ LSB	Input	All bits high-to-low[3]		5		μs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high[2]		30		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low[3]		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change[2,3]		150		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition[4]		300		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition[5]		150		ns
t_S	Set-up time	$\overline{LE}$	Input	[1,6]	100			ns
t_H	Hold time	Input	$\overline{LE}$	[1,6]	50			ns
t_{PW}	Latch enable pulse width			[1,6]	150			ns

NOTES:
1. Refer to Figure 2.
2. See Figure 5.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.

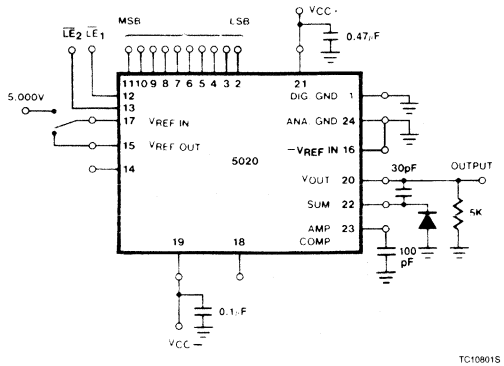


Figure 1. DC Parametric Test Configuration

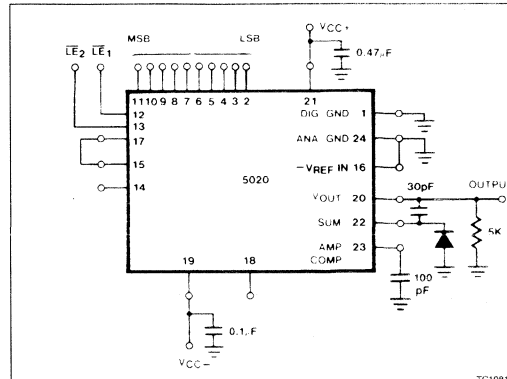


Figure 2. AC Parametric Test Configuration

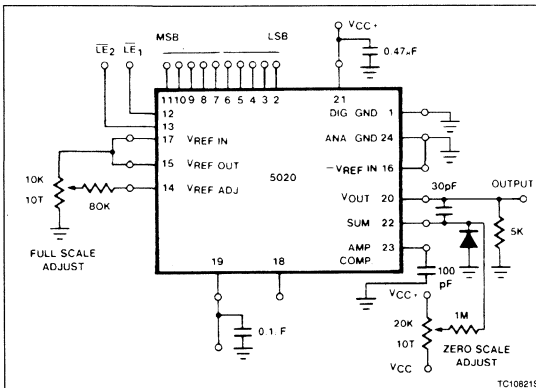


Figure 3. Full-/Zero-Scale Adjust — Unipolar Output (0 – 10V)

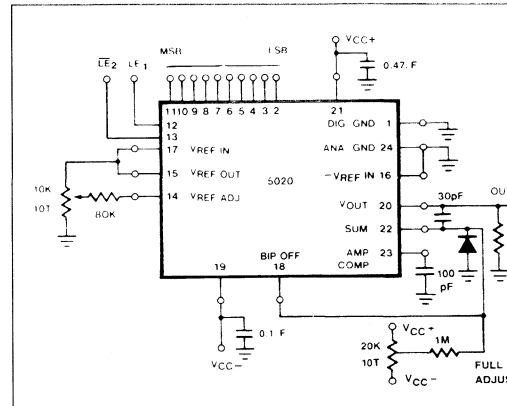


Figure 4. Bipolar Output Operation (−5 to +5V)

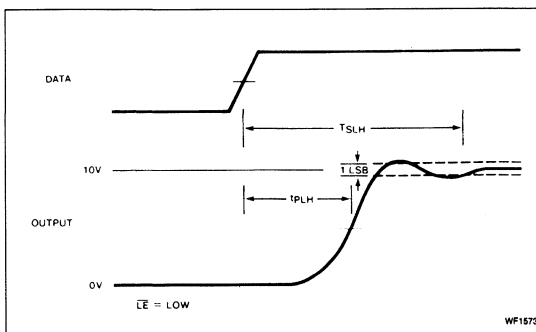


Figure 5. Settling Time and Propagation Delay, Low-to-High Data

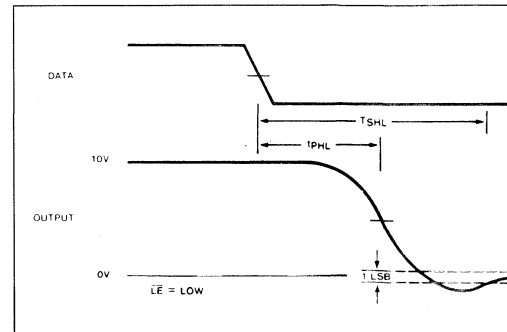


Figure 6. Settling Time and Propagation Delay, High-to-Low Data

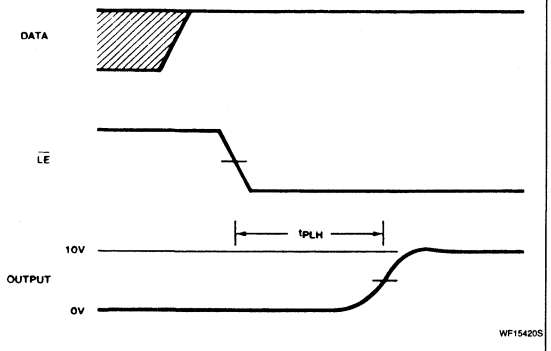


Figure 7. Propagation Delay, Latch Enable to Output

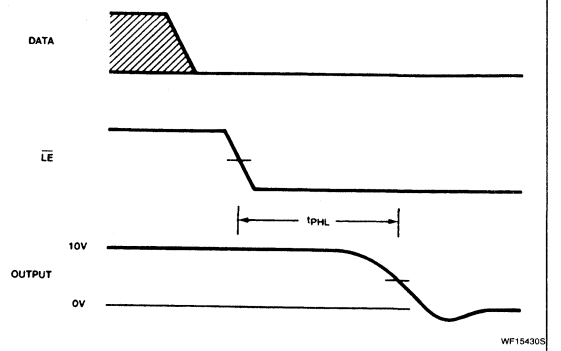


Figure 8. Propagation Delay, Latch Enable to Output

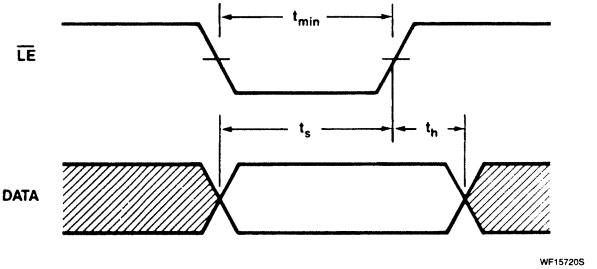


Figure 9. Latch Enable Pulse Width, Setup and Hold Times

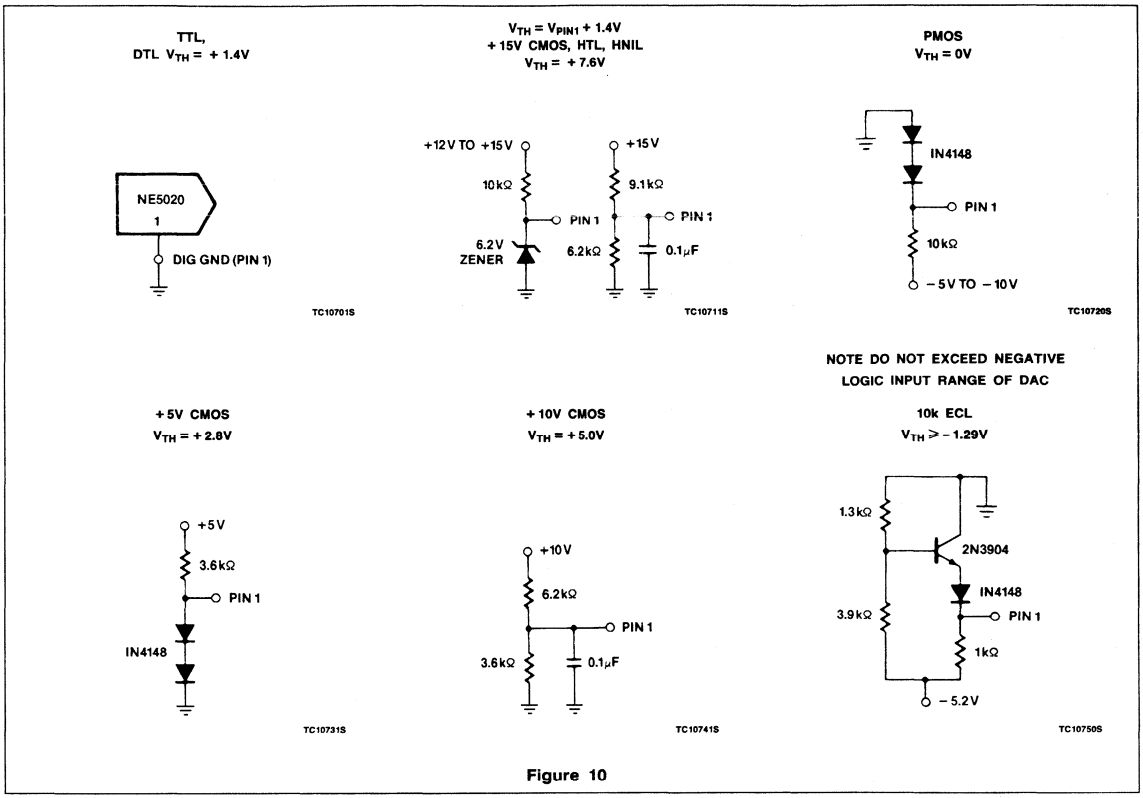


Figure 10

CIRCUIT DESCRIPTION

The NE5020 provides ten data latches, an internal voltage reference, application resistors, and a scaled output voltage in addition to the basic DAC components (see Block Diagram).

Latch Circuit

Digital interface with the NE5020 is readily accomplished through the use of two latch enable ports ($\overline{LE}_1$ and $\overline{LE}_2$) and ten data input latches. $\overline{LE}_2$ controls the two most significant bits of data (DB_9 and DB_8) while $\overline{LE}_1$ controls the eight lesser significant bits (DB_7 through DB_0). Both the latch enable ports ($\overline{LE}$) and the data inputs are static- and threshold-sensitive. When the latch enable ports ($\overline{LE}$) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the $\overline{LE}$ with a low static (Logic '0'), the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on

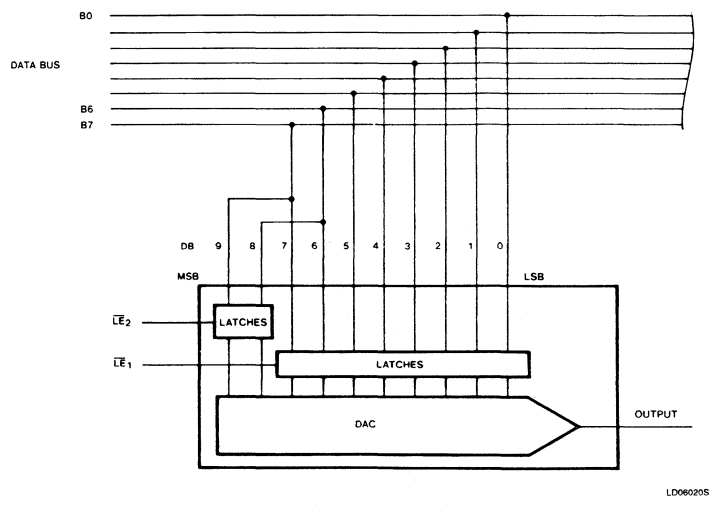


Figure 11. NE5020 μP Interface 8-Bit Data Bus Example

which $\overline{LE}$ goes high) 'memorizes' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

The data inputs are inactive and high impedance (typically requiring −2μA for low (0.8V max) or 0.1μA for high (2.0V min)) when the $\overline{LE}$ is high. Any changes on the data bus with $\overline{LE}$ high will have no effect on the DAC output.

The digital logic inputs ($\overline{LE}$ and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4V with respect to the voltage level on the digital ground pin (Pin 1). Figure 10 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

To be compatible with a bus-oriented system, the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 9 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50ns after $\overline{LE}$ is changed to a high state.

The independent $\overline{LE}$ ($\overline{LE}_1$ and $\overline{LE}_2$) lines allow for direct interface from an 8-bit data bus (see Figure 11). Data for the two MSBs is supplied and stored when $\overline{LE}_2$ is activated low and returned high according to the NE5020 timing requirements. Then $\overline{LE}_1$ is activated low and the remaining eight LSBs of data are transferred into the DAC. With $\overline{LE}_1$ returning high, the loading of 10-bit data word from an 8-bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16-bit bus or any other data bus with 10 or greater data bits.

This can be accomplished from an 8-bit data bus by utilizing an external latch circuit to preload the two MSB data values. Figure 12 shows the circuit configuration.

After preloading (via $\overline{LE}$ preload) the external latch with the two MSB values, $\overline{LE}_2$ is activated low and the eight LSBs and the two MSBs are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.

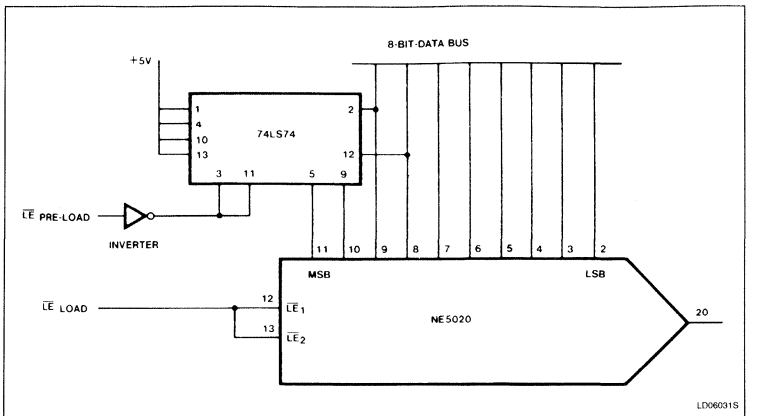


Figure 12. Preloading the 2 MSBs to Provide a Single-Step Output

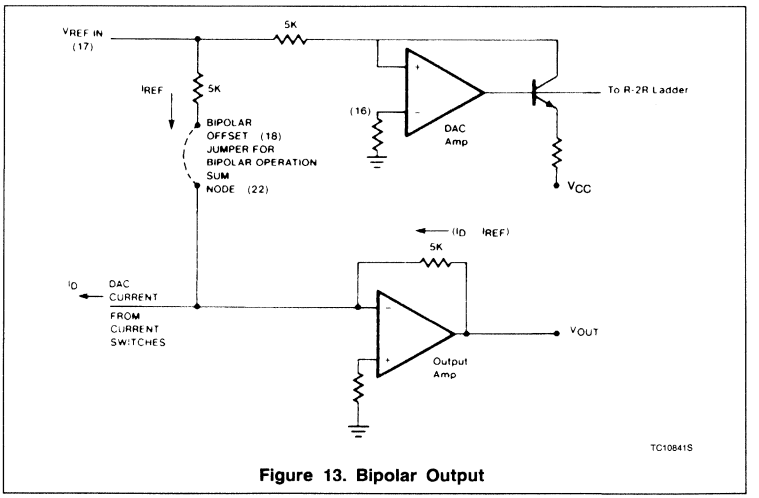


Figure 13. Bipolar Output

Reference Interface

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long-term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5V reference output. Providing a $V_{REF\ ADJ}$ (Pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in Figure 15 performs not only V_{REF} adjustment, but also full-scale output adjust. Notice that the $V_{REF\ ADJ}$ pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the $V_{REF\ ADJ}$ pin and observing good layout practices.

The $V_{REF\ OUT}$ node can drive loads greater than the DAC V_{REF} input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier be used.

Input Amplifier

The DAC reference amplifier is a high gain internally-compensated op amp used to convert the input reference voltage to a precision bias current for the DAC ladder network.

The Block Diagram details the input reference amplifier and current ladder. The voltage-to-current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5V V_{REF}. This current sets the input bias to the ladder network. Data bit 9 (DB_9)(Q_9), when turned on, will mirror this current and will contribute 1mA to the output. DB_8 (Q_8) will contribute ½ of that value or 0.5mA, and so on. These current values act as current

sinks and will add at the sum node to produce a DAC ladder to sum node function of:

$$I_{OUT} = \frac{2V_{REF}}{R_{REF}}\left(\frac{DB9}{2}+\frac{DB8}{4}+\frac{DB7}{8}+\frac{DB6}{16}+\frac{DB5}{32}+\frac{DB4}{64}+\frac{DB3}{128}+\frac{DB2}{256}+\frac{DB1}{512}+\frac{DB0}{1024}\right).$$

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically 0.7V/μs and source impedances at the $V_{REF\ INPUT}$ greater than 5kΩ should be avoided to maintain stability.

The $-V_{REF\ INPUT}$ pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode $+V_{REF\ INPUT}$ is grounded and the negative reference is tied directly to the $-V_{REF\ INPUT}$. The $-V_{REF\ INPUT}$ contains a 5kΩ resistor that matches a like resistor in the $+V_{REF\ INPUT}$ to reduce voltage offset caused by op amp input bias currents.

Output Amplifier and Interface

The NE5020 provides an on-chip output op amp to eliminate the need for additional external active circuits. Its two-stage design with feed-forward compensation allows it to slew at 15V/μs and settle to within ± ½LSB in 5μs. These times are typical when driving the rated loads of $R_L \geqslant 5k$ and $C_L \leqslant 50pF$ with recommended values of $C_{FF} = 1nF$ and $C_{FB} = 30pF$. Typical input offset voltages of 5mV and 50kΩ open-loop gain insure that an accurate current-to-voltage conversion is performed when using the on-chip R_{FB} resistor. R_{FB} is matched to R_{REF} and R_{BIP} to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition I_{OUT} will limit at ± 15mA typical. Recovery from this condition to rated accuracy will be determined by duration of short-circuit and die temperature stabilization.

Bipolar Output Voltage

The NE5020 includes a thermally matched resistor, R_{BIP}, to offset the output voltage by 5V to obtain −5V to +5V output voltage range operation. This is accomplished by shorting Pins 18 and 22 (see Figure 13). This connection produces a current equal to (V_{REFIN} − SUM NODE) ÷ R_{BIP} (1mA nominal), which is injected into the sum node. Since full-scale current out is approximately 2mA (1.9980mA), (2mA − 1mA)5kΩ = 5V will appear at the output. For zero DAC output currents, 1mA is still injected into sum node and $V_{OUT} = -(5k\Omega)(1mA) = -5V$. Zero-scale adjust and full-scale adjust are performed as described below, noting that full-scale voltage is now approximately +5V. Zero-scale adjust may be used to trim $V_{OUT} = 0.00$ with the MSB high or $V_{OUT} = -5.0V$ with all bits off.

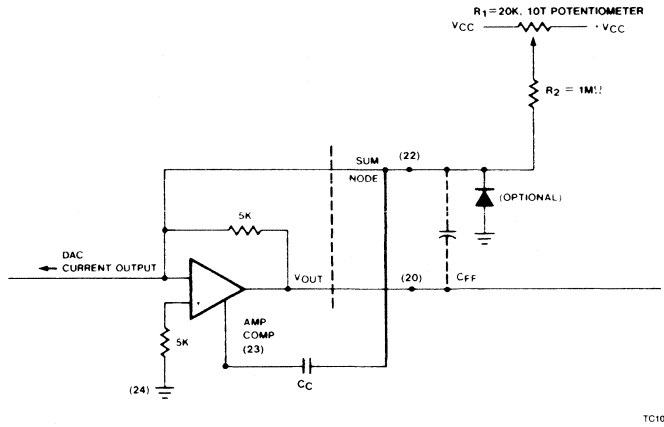


Figure 14. Zero-Scale Adjustment

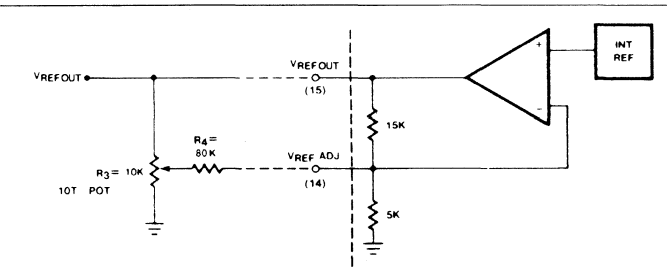


Figure 15. Reference Adjust Circuit

Zero-Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is shown in Figure 14. The trim is the result of injecting a current from resistor R_2 that counteracts the error current. Adjusting potentiometer R_1 until V_{OUT} equals 0.000V in the unipolar mode or −5.000V in the bipolar mode (see bipolar section) accomplishes this trim.

Full-Scale Adjustment

A recommended full-scale adjustment circuit, when using the internal voltage reference, is shown in Figure 15. Potentiometer R_3 is adjusted until V_{OUT} equals 9.99023V. In many applications where the absolute accuracy of full-scale is of low importance when compared to the other system accuracy factors this adjustment circuit is optional.

As resistors R_{REF}, R_{FB}, and R_{BIP} shown in the Block Diagram are integrated in close proximity, they match and track in value closely over wide ambient temperature variations. Typical matching is less than ±0.3% which implies that typical full-scale (or gain) error is less than ±0.3% of ideal full-scale value.

NE/SE5118/5119

8-Bit Microprocessor-Compatible D/A Converter — Current Output

Linear Products

Product Specification

DESCRIPTION

The NE/SE5118/19 is a high-speed 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultralow loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale, while maintaining a low temperature coefficient.

The output has high voltage compliance, increasing versatility.

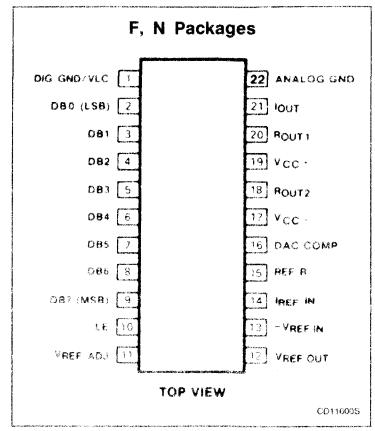
FEATURES

- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Fast settling output current — 200ns**
- **Accurate to ± ¼LSB (0.1%)**
- **Monotonic to 8 bits**
- **Reference short-circuit protected**
- **Compatible with 8086, 6800 and many other microprocessors**

APPLICATIONS

- **Precision 8-BIT D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**
- **CRT display drivers**
- **High-speed modems**

PIN CONFIGURATION



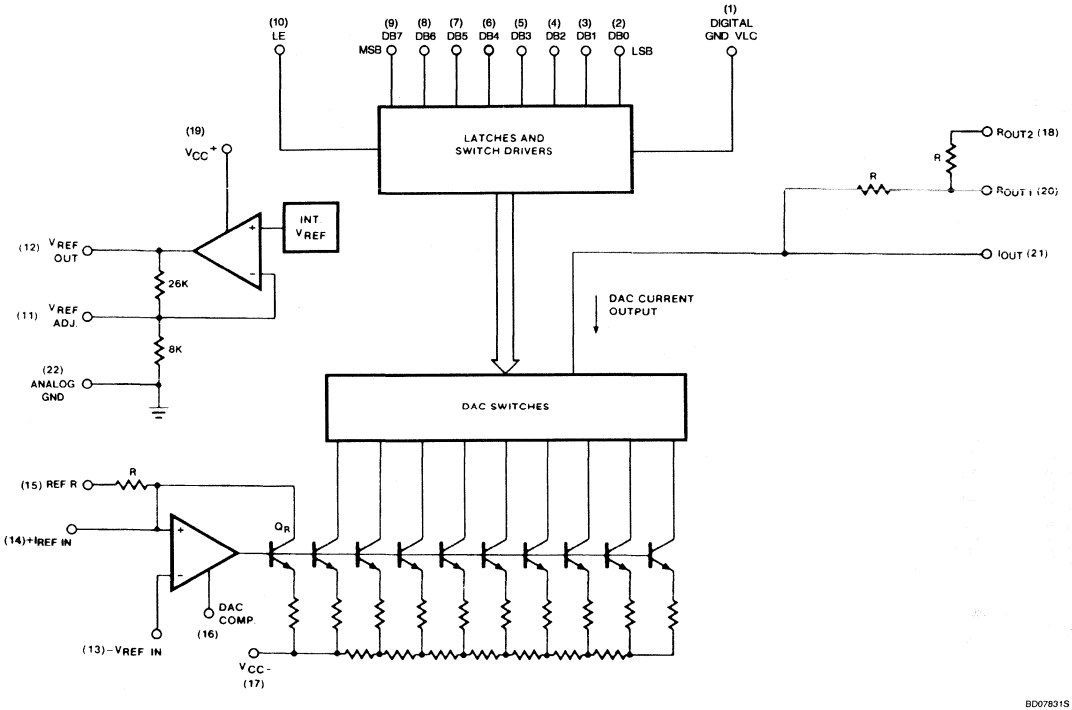
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
22-Pin Plastic DIP	0 to +70°C	NE5119N
22-Pin Ceramic DIP	0 to +70°C	NE5119F
22-Pin Ceramic DIP	−55°C to +125°C	SE5119F

8-Bit Microprocessor-Compatible D/A Converter — Current Output

NE/SE5118/5119

BLOCK DIAGRAM



NOTE:
All R values equal 5kΩ and are thermally matched.

8-Bit Microprocessor-Compatible D/A Converter — Current Output

NE/SE5118/5119

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at V_{REF} input	12	V
$V_{REF\ ADJ}$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
$I_{REF\ IN}$	Reference input current (Pin 14)	3	mA
P_D	Maximum power dissipation $T_A = 25°C$ (still-air)[1] F package N package	 1740 2190	 mW mW
T_A	Operating ambient temperature range SE5119 NE5119	 −55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:
1. Derate above 25°C, at the following rates:
   F package at 13.9mW/°C.
   N package at 17.5mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+$ = +15V, $V_{CC}-$ = −15V, SE5119. −55°C ≤ T_A ≤ 125°C, NE5119. 0°C ≤ T_A ≤ 70°C, unless otherwise specified. Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5118			NE/SE5119			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15	16.5	11.4	15	16.5	V
$V_{CC}-$	Negative supply voltage		−11.4	−15	−16.5	−11.4	−15	−16.5	V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, 2V < V_{IN} < 18V		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, −5V < V_{IN} < 0.8V		−2.0	−10		−2.0	−10	μA
I_{FS}	Full-scale output current	Unipolar operation $V_{REF\ IN}$ = 5.000V, T_A = 25°C	1.90	1.992	2.10	1.90	1.992	2.10	mA
I_{ZS}	Zero-scale current			1			1		μA
V_{REF}	Reference voltage	I_{REF} = 1mA, T_A = 25°C	4.9	5.0	5.25	4.9	5.0	5.25	V
$PSR+_{(OUT)}$	Output power supply rejection (+)	V− = −15V, 13.5V ≤ V+ ≤ 16.5V external $V_{REF\ IN}$ = 5.000V		0.001	0.01		0.001	0.01	%FS/%VS

8-Bit Microprocessor-Compatible D/A Converter — Current Output

NE/SE5118/5119

DC ELECTRICAL CHARACTERISTICS (Continued)

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5119. $-55°C \leq T_A \leq 125°C$, NE5119. $0°C \leq T_A \leq 70°C$, unless otherwise specified. Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5118			NE/SE5119			UNIT
			Min	Typ	Max	Min	Typ	Max	
$RSR-_{(OUT)}$	Output power supply rejection (–)	V+ = 15V, $-13.5V \leq V- \leq -16.5V$ external $V_{REF\ IN} = 5.000V$		0.001	0.01		0.001	0.01	%FS/%VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN} = 5.000V$ (Pin 15)		20			20		ppm/°C
TC_{ZS}	Zero-scale temperature coefficient	$I_{REF\ IN} = 1.00mA$ (Pin 14)		5			5		ppm/°C
I_{REF}	Reference output current	$T_A = 25°C$			3			3	mA
I_{REFSC}	Reference short circuit current[1]	$V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	V– = –15V, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		0.003	0.01		0.003	0.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (–)	V+ = 15V, $-13.5V \leq V- \leq 16.5V$, $I_{REF} = 1.0mA$		0.003	0.01		0.003	0.01	%VR/%VS
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $R_{REF\ IN}$ input impedance			5.0			5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		–10	–15		–10	–15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE:
1. *For reference currents > 3mA, use of an external buffer is required.*

AC ELECTRICAL CHARACTERISTICS

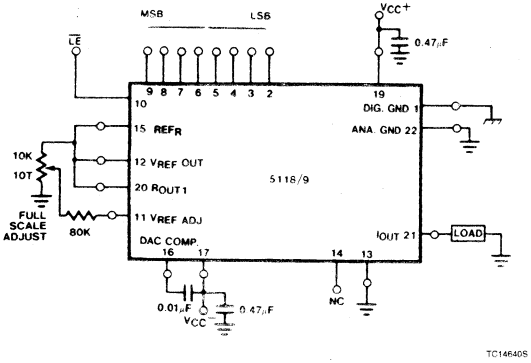
$V_{CC} = \pm 15V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	NE/SE5118/19			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	± ½ LSB	Input	All bits Low-to-High		200		ns
t_{SHL}	Settling time	± ½ LSB	Input	All bits High-to-Low		200		ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-High		60		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-Low		60		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change		60		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-High transition		60		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-Low transition		60		ns
t_S	Setup time	$\overline{LE}$	Input		100			ns
t_H	Hold time	Input	$\overline{LE}$		50			ns
t_{PW}	Latch enable pulse width				150			ns

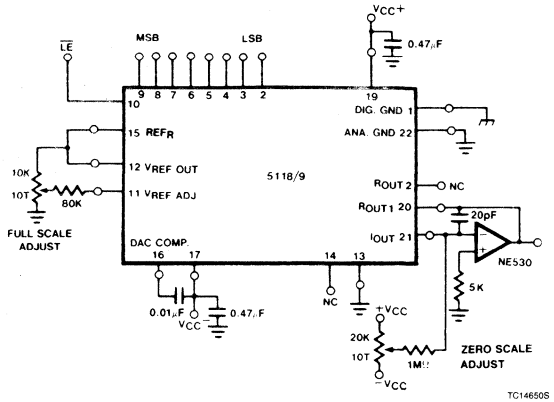
8-Bit Microprocessor-Compatible D/A Converter — Current Output

NE/SE5118/5119

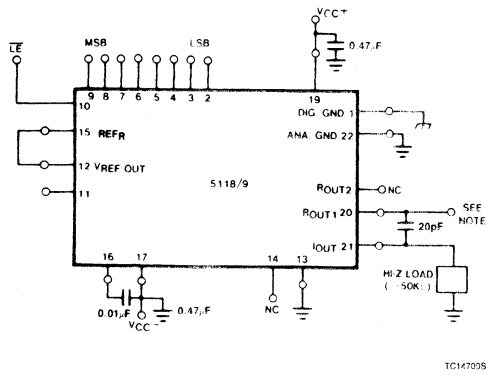
TYPICAL APPLICATIONS

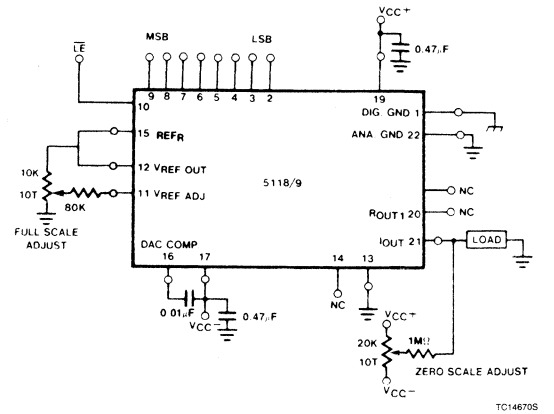


Bipolar Output Operation (−1mA to +1mA)



Unipolar Voltage Output (0 to +10V)





NOTE:

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	−10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

Fast Voltage Output

Basic Unipolar Current Output (0 to −2mA)

NE5150/5151/5152
Triple 4-Bit RGB D/A Converter With and Without Memory

Product Specification

DESCRIPTION

The NE5150/5151/5152 are triple 4-bit DACs intended for use in graphic display systems. They are a high performance — yet cost effective — means of interfacing digital memory and a CRT. The NE5150/5152 are single integrated circuit chips containing special input buffers, an ECL static RAM, high-speed latches, and three 4-bit DACs. The input buffers are user-selectable as either ECL or TTL compatible for the NE5150. The NE5152 is similar to the NE5150, but is TTL compatible only, and operates off of a single +5V supply. The RAM is organized as 16 × 12, so that 16 "color words" can be down-loaded from the pixel memory into the chip memory. Each 12-bit word represents 4 bits of red, 4 bits of green and 4 bits of blue information. This system gives 4096 possible colors. The RAM is fast enough to completely reload during the horizontal retrace time. The latches resynchronize the digital data to the DACs to prevent glitches. The DACs include all the composite video functions to make the output waveforms meet RS-170 and RS-343 standards, and produce $1V_{P-P}$ into 75Ω. The composite functions (reference white, bright, blank, and sync) are latched to prevent screen-edge distortions generally found on "video DACs." External components are kept to an absolute minimum (bypass capacitors only as needed) by including all reference generation circuitry and termination resistors on-chip, by building in high-frequency PSRR (eliminating separate V_{EE}s and costly power supplies and filtering), and by using a single-ended clock. The guaranteed maximum operating frequency for the NE5150/5152 is 110MHz over the commercial termperature range. The devices are housed in a standard 24-pin package and consume less than 1W of power.

The NE5151 is a simplified version of the NE5150, including all functions except the memory. Maximum operating frequency is 150MHz.

FEATURES

- **Single-chip**
- **On-board ECL static RAM**
- **4096 colors**
- **ECL and TTL compatible**
- **110MHz update rate (NE5150, 5152)**
- **150MHz update rate (NE5151)**
- **Low power and cost**
- **Drives 75Ω cable directly**
- **Internal reference**
- **40dB PSRR**
- **No external components necessary**

APPLICATIONS

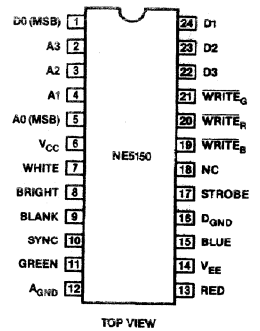
- **Bit-mapped graphics**
- **Super high-speed DAC**
- **Home computers**
- **Raster-scan displays**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Ceramic DIP	0°C to +70°C	NE5150F
24-Pin Ceramic DIP	0°C to +70°C	NE5151F
24-Pin Ceramic DIP	0°C to +70°C	NE5152F
24-Pin Plastic SOL	0°C to +70°C	NE5152D

PIN CONFIGURATIONS

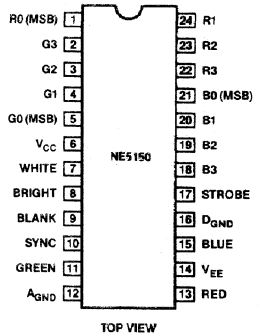
NE5150 F Package



TOP VIEW

CD09550S

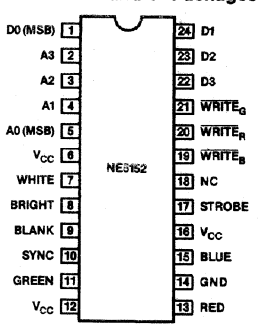
NE5151 F Package



TOP VIEW

CD10432S

NE5152 D[1] and F Packages



TOP VIEW

CD09570S

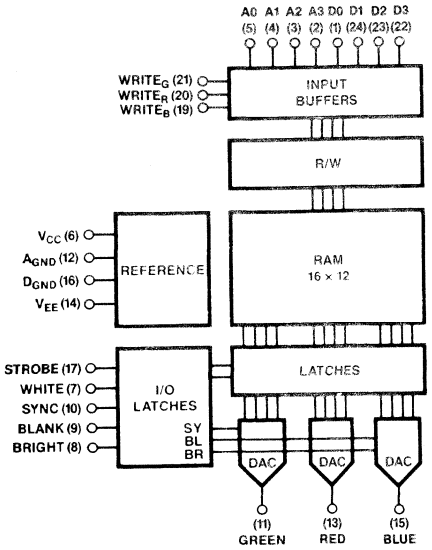
NOTE:
1. Available in large SO pakage only.

Triple 4-Bit RGB D/A Converter With and Without Memory

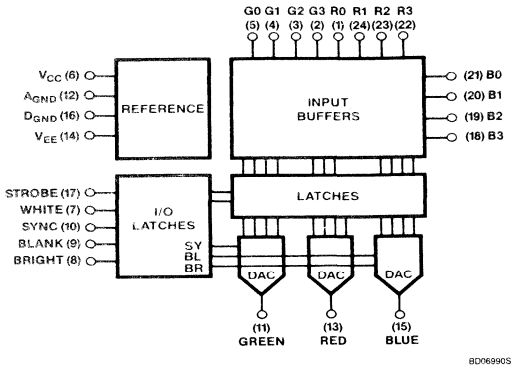
NE5150/5151/5152

BLOCK DIAGRAMS

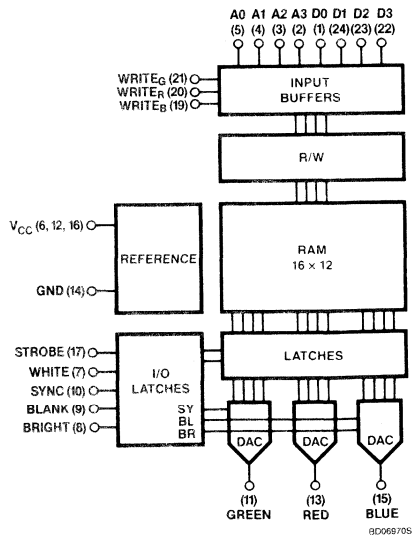
NE5150



NE5151



NE5152



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Temperature range		
T_A	Operating	0 to +70	°C
T_{STG}	Storage	−65 to +150	°C
V_{CC}	Power supply	7.0	V
V_{EE}		−7.0	V
	Logic levels		
	TTL-high	5.5	V
	TTL-low	−0.5	V
	ECL-high	0.0	V
	ECL-low	0 to V_{EE}	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < +70°C, for NE5150/5151; V_{CC} = +5V (TTL), GND = 0V for NE5152, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Resolution	4			bits
	Monotonicity	4			bits
NL	Non-linearity		± 1/16	± 1/2	LSB
DNL	Differential non-linearity		± 1/8	± 1	LSB
	Offset error (25°C) [1111] (BRT = 1)		−1/5	± 1	LSB
	Gain error (25°C) [0000] (BRT = 1)		± 1/2	± 1	LSB
V_{CC}	Positive power supply (TTL mode) (NE5150)	4.5	5.0	5.5	V
	(TTL mode) (NE5151)	4.75	5.0	5.5	V
	(ECL mode)	−0.1	0.0	0.1	V
V_{EE}	Negative power supply (TTL or ECL mode) (NE5150/5151)	−4.75	−5.0	−5.5	V
I_{CC}	Positive supply current (NE5150/5151)		15	25	mA
	(NE5152)		175	210	mA
I_{EE}	Negative supply current (NE5150)		175	210	mA
	(NE5151)		145	175	mA
	Analog voltage range (ZS to FS)		603		mV
	Gain tracking (any two channels)			± 1/4	LSB
LSB	Least significant bit		40.2		mV
EWH	Enhanced white level (25°C)[2]		0		mV
BS	Bright shift (25°C)(0 to 1)		71.4		mV
EBL	Enhanced blanking level (25°C)[2]		−674		mV
ESY	Enhanced sync level (25°C)[2]		−960		mV
R_O	Output resistance (25°C)	67.5	75.0	82.5	Ω
V_{IH}	TTL logic input high	2.0			V
V_{IL}	TTL logic input low			0.8	V
I_{IH}	TTL logic high input current (V_{IN} = 2.4V)			20	μA
I_{IL}	TTL logic low input current (V_{IN} = 0.4V)			−1.6	mA
V_{IH}	ECL logic input high	−1.045			V
V_{IL}	ECL logic input low			−1.48	V
I_{IH}	ECL logic high input current (V_{IN} = −0.8V)			−1.0	mA
I_{IL}	ECL logic low input current (V_{IN} = −1.8V)			−1.0	mA

TEMPERATURE CHARACTERISTICS V_{CC} = +5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < +70°C, for NE5150/5151; V_{CC} = +5V (TTL), GND = 0V for NE5152, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Offset TC[1]		±50	±100	ppm/°C
	Gain TC[1]		±70	±200	ppm/°C
	Gain Tracking TC (any two channels)		±20	±50	ppm/°C
	Enhanced white level TC[1]		±50	±100	ppm/°C
	Bright shift TC		±70	±200	ppm/°C
	Enhanced blanking level TC		±100	±300	ppm/°C
	Enhanced sync level TC		±100	±300	ppm/°C
	Output resistance TC		+1000	+2000	ppm/°C

NOTES:
1. Normalized to full-scale (603mV).
2. With respect to [1111] (BRT = 1).

AC ELECTRICAL CHARACTERISTICS V_{CC} = +5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < +70°C, for NE5150/5151; V_{CC} = +5V (TTL), GND = 0V for NE5152, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
f_{MAX}	Maximum operating frequency (NE5150/5152)	110			MHz
t_{WAS}	Write address setup (NE5150/5152)	0			ns
t_{WAH}	Write address hold (NE5150/5152)	0			ns
t_{WDS}	Write data setup (NE5150/5152)	4			ns
t_{WDH}	Write data hold (NE5150/5152)	2			ns
t_{WEW}	Write enable pulse width (NE5150/5152)	3			ns
t_{RCS}	Read composite[1] setup (NE5150/5152)	3			ns
t_{RCH}	Read composite[1] hold (NE5150/5152)	2			ns
t_{RAS}	Read address setup (NE5150/5152)	3			ns
t_{RAH}	Read address hold (NE5150/5152)	2			ns
t_{RSW}	Read strobe pulse width (NE5150/5152)	3			ns
t_{RDD}	Read DAC delay (NE5150/5152)		8		ns
f_{MAX}	Maximum operating frequency (NE5151)	150			MHz
t_{CS}	Composite[1] setup (NE5151)	3			ns
t_{CH}	Composite[1] hold (NE5151)	2			ns
t_{DS}	Data-bits setup (NE5151)	1			ns
t_{DH}	Data-bits hold (NE5151)	5			ns
t_{SW}	Strobe pulse width (NE5151)	3			ns
t_{DD}	DAC delay (NE5151)		8		ns
t_R	DAC rise time (10 – 90%)		3		ns
t_S	DAC full-scale settling time[2]		10		ns
C_{OUT}	Output capacitance (each DAC)		10		pF
SR	Slew rate		200		V/μs

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
GE	Glitch energy			30	pV-s
PSRR[3]	Power supply rejection ratio (to red, green or blue outputs)				
	V_{EE} at 1kHz		43		dB
	V_{EE} at 10MHz		28		dB
	V_{EE} at 50MHz		14		dB
	V_{CC} at 1kHz		80		dB
	V_{CC} at 10MHz		50		dB
	V_{CC} at 50MHz		36		dB

NOTES:
1. Composite implies any of the WHITE, BRIGHT, BLANK or SYNC signals.
2. Setting to ± ½ LSB, measured from STROBE 50% point (rising edge). This time includes the delay throught the strobe input buffer and latch.
3. Listed PSRR is for the NE5150/51. The NE5152 PSRR specs are identical to the V_{EE} numbers in the table.

NE5150 PIN DESCRIPTION

Write enable inputs use negative-true logic while all other inputs are positive-true. All inputs operate synchronously with the positive edge-triggered strobe input. When V_{CC} is taken high (5V), all inputs are TTL compatible. When V_{CC} is grounded, all inputs are ECL compatible. All DACs are complementary, so that all ones is the highest absolute voltage and all zeroes is the lowest. All ones is called zero-scale (ZS) and all zeroes is called full-scale (FS). The analog output voltage is approximately 0V (ZS) to −1V (SYNC).

Pins 1, 24, 23, 22: **DATA** bits D0 (MSB) through D3, used to input digital information to the memory during the write phase. During this phase, the data bits are presented to the internal latches (noninverted) and the DACs will output the analog equivalent of the stored word, unless overridden by WHITE, BLANK or SYNC.

Pins 5, 4, 3, 2: **ADDRESS** lines A0 (MSB) through A3, used for selecting a memory address to write to or read from.

Pin 7: **WHITE** command. Presets the latches to all ones [1111] and outputs 0V absolute on all DACs. Can be modified to −71mV absolute when BRIGHT is taken low. Will be overridden by either a BLANK or SYNC command.

Pin 8: **BRIGHT** command. A low input here turns on an additional −71mV (10 IRE unit) switch, shifting all other levels downward. Not overridden by any other input.

Pin 9: **BLANK** command. Presets the latches to all zeroes [0000] and turns on an additional −71mV (10 IRE unit) switch. Absolute output is −671mV. Can be modified another −71mV to −742mV absolute when BRIGHT is taken low. Will override WHITE, and will be overridden by SYNC.

Pin 10: **SYNC** command. Presets the latches to all zeroes [0000] and turns on the BLANK switch. Additionally turns on a −286mV (40 IRE unit) switch in the green channel only. Absolute output is −671mV for the red and blue channels, and −957mV for the green channel. All levels can be shifted −71mV by taking BRIGHT low. Overrides WHITE and BLANK.

Pins 11, 13, 15: **GREEN, RED, BLUE.** Analog outputs with 75Ω internal termination resistors. Can directly drive 75Ω cable and should be terminated at the display end of the line with 75Ω. Output voltage range is approximately 0V to −1V, independent of whether the digital inputs are ECL or TTL compatible. All outputs are simultaneously affected by the WHITE, BLANK or BRIGHT commands. Only the GREEN channel carries SYNC information.

NOTE:
There are 100 IRE units from WHITE to BLANK. One IRE unit is approximately 7.1mV. Full-scale is 90 IRE units and 10 IRE units is ⅛ of full-scale (e.g., BRIGHT function).

Pins 19, 20, 21: $\overline{\text{WRITE}}_B$, $\overline{\text{WRITE}}_R$, $\overline{\text{WRITE}}_G$. Write enable commands for each of the three 16 × 4 memories. When all write commands are high, then the READ operation is selected. This is the normal display mode. To write data into memory, the write enable pin is taken low. Data D0 − D3 will be written into address A0 − A3 of each memory when its corresponding write enable pin goes low.

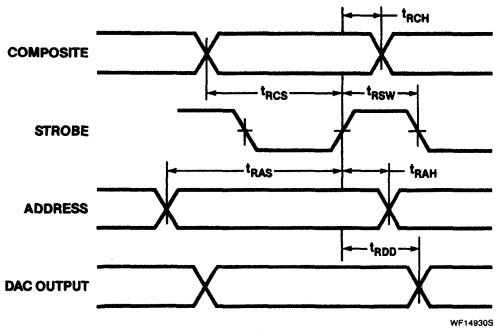
Pin 17: **STROBE.** The strobe signal is the main system clock and is used for resynchronizing digital signals to the DACs. Preventing data skew eliminates glitches which would otherwise become visible color distortions on a CRT display. The strobe command has no special drive requirements and is TTL or ECL compatible.

Pins 12, 16: A_{GND}, D_{GND}. Both Analog and Digital ground carry a maximum of approximately 100mA of DC current. For proper operation, the difference voltage between A_{GND} and D_{GND} should be no greater than 50mV, preferably less.

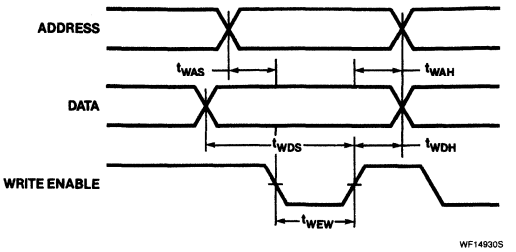
Pin 14: V_{EE}. The negative power supply is the main chip power source. V_{CC} is only used for TTL input buffers. As is usual, good bypassing techniques should be used. The chip itself has a good deal of power supply rejection — well up into the VHF frequency range — so no elaborate power supply filtering is necessary.

Pin 18: **NC.** This unused pin should be tied high or low.

NE5150/5152 TIMING DIAGRAMS



Read Cycle



Write Cycle

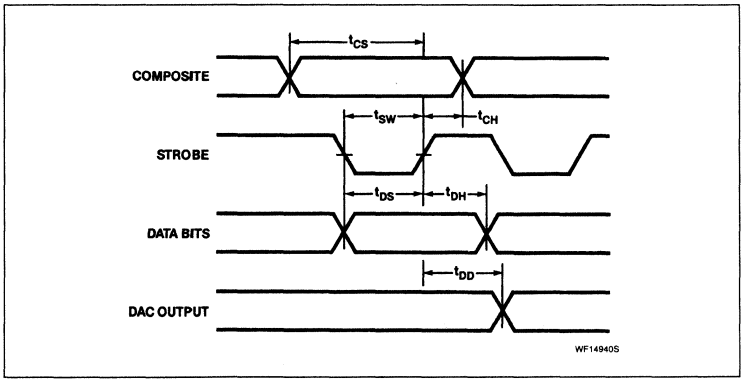
NE5151 PIN DESCRIPTION AND TIMING DIAGRAM

The eleven digital inputs D0 – D3, A0 – A3, $\overline{\text{WRITE}}_{G/R/B}$, and the unused Pin 18 of the NE5150 are replaced in the NE5151 with the three 4-bit DAC digital inputs G0 – G3, R0 – R3, and B0 – B3. All other pin functions (e.g., composite functions, power supplies, strobe, etc.) are identical to the NE5150.

NE5152 PIN DESCRIPTION

The NE5152 is a TTL-compatible-only version of the NE5150, operating off of a single +5V supply. V_{CC} Pins 6, 12 and 16 should be connected to +5V and Pin 14 to 0V. DAC output is referenced to V_{CC}.

NE5151 TIMING DIAGRAM



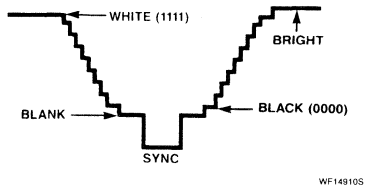
NE5150/NE5151/NE5152 LOGIC TABLE

SYNC	BLANK	WHITE	BRIGHT	DATA	ADDRESS	OUTPUT[3]	CONDITION
1	X	X	0	X	X	−1031mV	SYNC[1]
1	X	X	1	X	X	−960mV	Enhanced SYNC[1]
0	1	X	0	X	X	−746mV	BLANK
0	1	X	1	X	X	−674mV	Enhanced BLANK
0	0	1	0	X	X	−71mV	WHITE
0	0	1	1	X	X	0mV	Enhanced WHITE
0	0	0	0	[0000]	Note 2	−674mV	BLACK (FS)
0	0	0	1	[0000]	Note 2	−603mV	Enhanced BLACK (EFS)
0	0	0	0	[1111]	Note 2	−71mV	WHITE (ZS)
0	0	0	1	[1111]	Note 2	0mV	Enhanced WHITE (EZS)

NOTES:

1. Green channel output only. RED and BLUE will output BLANK or Enhanced BLANK under these conditions.
2. For the NE5150/5152 the DATA column represents the memory data accessed by the specific address. For the NE5151, the DATA is the direct digital inputs.
3. Note output voltages in Logic Table are referenced to V_{CC} for the NE5152 only.

COMPOSITE VIDEO WAVEFORM



NE/SE5410
10-Bit High-Speed Multiplying D/A Converter

Product Specification

DESCRIPTION

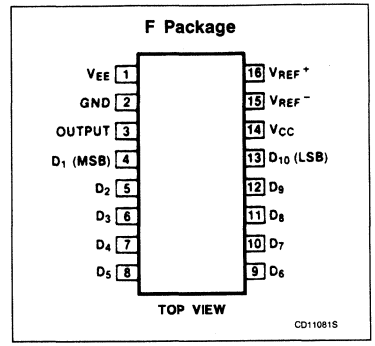
The NE5410/SE5410 are 10-bit Multiplying Digital-to-Analog Converters pin- and function-compatible with the industry-standard MC3410, but with improved performance. These are capable of high-speed performance, and are used as general-purpose building blocks in cost effective D/A systems.

The NE/SE5410 provides complete 10-bit accuracy and differential non-linearity over temperature, and a wide compliance voltage range. Segmented current sources, in conjunction with an R/2R DAC, provide the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

FEATURES

- **Pin- and function-compatible with MC3410**
- **10-bit resolution and accuracy (± 0.05%)**
- **Guaranteed differential non-linearity over temperature**
- **Wide compliance voltage range — −2.5 to +2.5V**
- **Fast settling time — 250ns typical**
- **Digital inputs are TTL- and CMOS-compatible**
- **High-speed multiplying input slew rate — 20mA/μs**
- **Reference amplifier internally-compensated**
- **Standard supply voltages +5V and −15V**

PIN CONFIGURATION



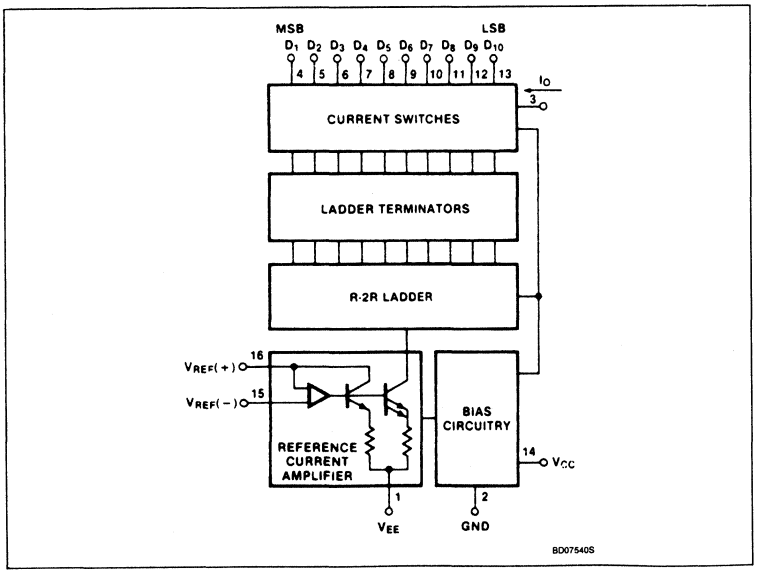
APPLICATIONS

- **Successive approximation A/D converters**
- **High-speed, automatic test equipment**
- **High-speed modems**
- **Waveform generators**
- **CRT displays**
- **Strip CHART and X-Y plotters**
- **Programmable power supplies**
- **Programmable gain and attenuation**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE5410F
16-Pin Cerdip	−55 to +125°C	SE5410F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS T_A = +25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	+7.0	V_{DC}
V_{EE}		−18	V_{DC}
V_I	Digital input voltage	+15	V_{DC}
V_O	Applied output voltage	+4, −5.0	V_{DC}
$I_{REF(16)}$	Reference current	2.5	mA
V_{REF}	Reference amplifier inputs	V_{CC}, V_{EE}	V_{DC}
$V_{REF(D)}$	Reference amplifier differential inputs	0.7	V_{DC}
T_A	Operating temperature range SE5410 NE5410	 −55 to +125 0 to +70	 °C °C
T_J	Junction temperature Ceramic package	 +150	 °C
T_{STG}	Storage temperature	−65 to +150	°C
P_D	Maximum power dissipation T_A = 25°C (still-air)[1]	1190	mW

NOTE:
1. Derate above 25°C at the following rate:
   F package at 9.5mW/°C.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5.0V_{DC}, V_{EE} = −15V_{DC}, I_{REF} = 2.0mA, all digital inputs at high logic level. SE5410: T_A = −55°C to +125°C, NE5410 Series: T_A = 0°C to +70°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
ϵ_R	Relative accuracy (Error relative to full scale I_O)	Over temperature		±0.025	±0.05	%
				± ¼	± ½	LSB
	Differential non-linearity	Over temperature		±0.025	±0.05	%
				± ¼	± ½	LSB
t_S	Settling time to within ± ½ LSB (all bits low to high)	T_A = 25°C		250		ns
t_{PLH} t_{PHL}	Propagation delay time	T_A = 25°C		35 20		ns
TCI_O	Output full-scale current drift			20	40	ppm/°C
V_{IH}	Digital input logic levels (all bits) High level, Logic "1" Low level, Logic "0"		2.0		 0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (all bits) High level, V_{IH} = 5.5V Low level, V_{IL} = 0.8V				20 −20	μA
$I_{REF(15)}$	Reference input bias current (Pin 15)			−1.0	−5.0	μA
I_{OH}	Output current (all bits high)	V_{REF} = 2.000V, R_{16}=1000Ω	3.937	3.996	4.054	mA
I_{OL}	Output current (all bits low)	T_A = 25°C		0	0.4	μA
V_O	Output voltage compliance	T_A = 25°C ϵ_R < 0.050% relative to full-scale			−2.5 +2.5	V_{DC}
SR I_{REF}	Reference amplifier slew rate			20		mA/μs

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = +5.0V_{DC}$, $V_{EE} = -15V_{DC}$, $I_{REF} = 2.0mA$, all digital inputs at high logic level. SE5410: $T_A = -55°C$ to $+125°C$, NE5410 Series: $T_A = 0°C$ to $+70°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
ST I_{REF}	Reference amplifier settling time	0 to 4.0mA, ±0.1%		2.0		μs
PSRR(−)	Output current power supply sensitivity			0.003	0.01	%/%
C_O	Output capacitance	$V_O = 0$		25		pF
C_I	Digital input capacitance (all bits high)			4.0		pF
I_{CC} I_{EE}	Power supply current (all bits low)			+2 −12	+4 −18	mA
V_{CC} V_{EE}	Power supply voltage range	$T_A = 25°C$ $V_O = 0$	+4.75 −14.25	+5.0 −15	+5.25 −15.75	V_{DC}
	Power consumption			190	300	mW

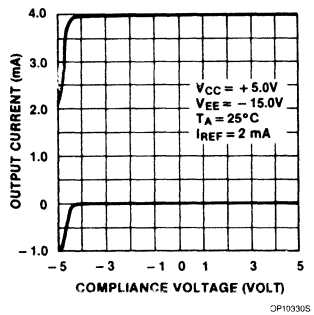


Figure 1. Output Current vs Output Compliance Voltage

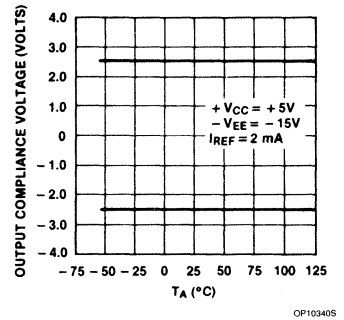


Figure 2. Maximum Output Compliance Voltage vs Temperature

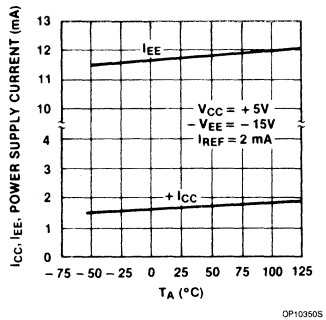


Figure 3. Power Supply Currents vs Temperature

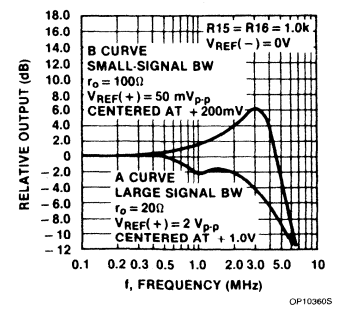


Figure 4. Reference Amplifier Frequency Response

CIRCUIT DESCRIPTION

The NE5410 consists of four segment current sources which generate the 2 Most Significant Bits (MSBs), and an R/2R DAC implemented with ion-implanted resistors for scaling the remaining 8 Least Significant Bits (LSBs) (see Figure 5). This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully-differential current switches. The switches use current steering for speed.

An on-chip high slew reference current amplifier drives the R/2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input: out-board resistor R16 (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0V and a 1kΩ resistor tied to Pin 16, the full-scale current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R16 should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1μF capacitor to ground.

The reference amplifier is internally-compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply 2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16 = 1.0kΩ, and settling time is ≈10μs. The reference amplifier phase margin decreases as the current souce value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

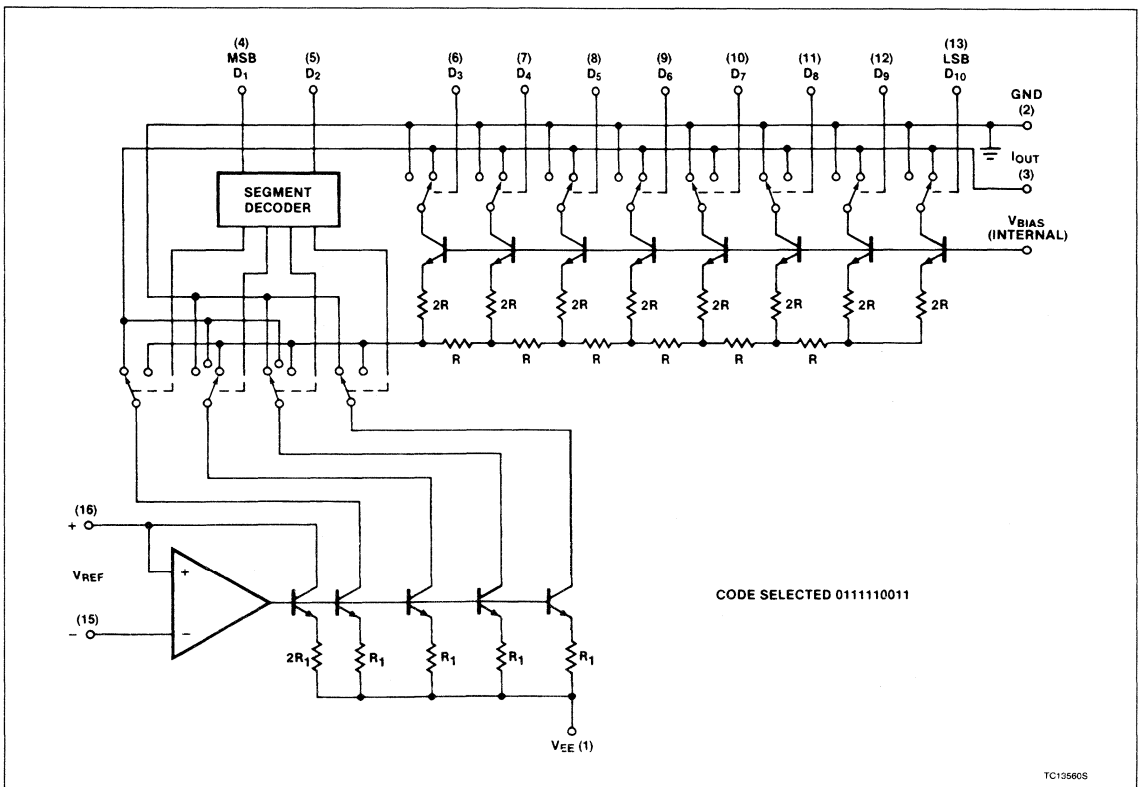
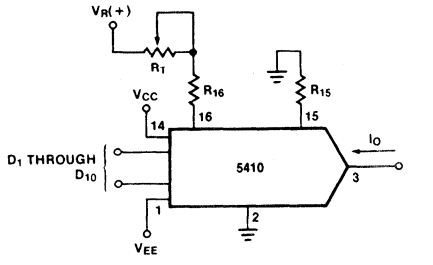
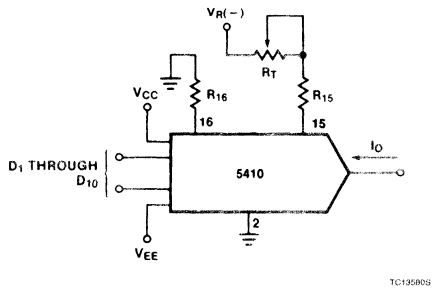


Figure 5. NE5410 Equivalent Circuit



NOTES:
$R_{16} + R_T = R_{15} = R_{REF}$
$R_T < < R_{16}$
I_O F.S. = 2 $I_R = V_{REF}/R_{REF}$

a. Positive Reference Voltabe



NOTES:
$R_{15} + R_T = R_{16}$
$R_T < < R_{15}$
$|V_{REF}| \geq |V_{EE}| + 3V$

b. Negative Reference Voltage

Figure 6. Basic Connections

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from −2.5 to +2.5V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if $V_{EE} > -15V$.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full-scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full-scale current. The relative accuracy of the NE5410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full-scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the NE5410 has a low full-scale current drift with temperature.

The SE5410 and the NE5410 are accurate to within ± ½ LSB at 25°C with a reference current of 2.0mA on Pin 16.

MONOTONICITY

The NE5410 and SE5410 are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched "on," which corresponds to a LOW-to-HIGH transition for all bits. This time is typically 250ns for the output to settle to within ± ½ LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (< 0.7V) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625Ω is connected to ground, allowing the output to swing to −2.5V, the settling time increases to 1.5μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

A typical test setup for measuring settling time is shown in Figure 7. The same setup for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.

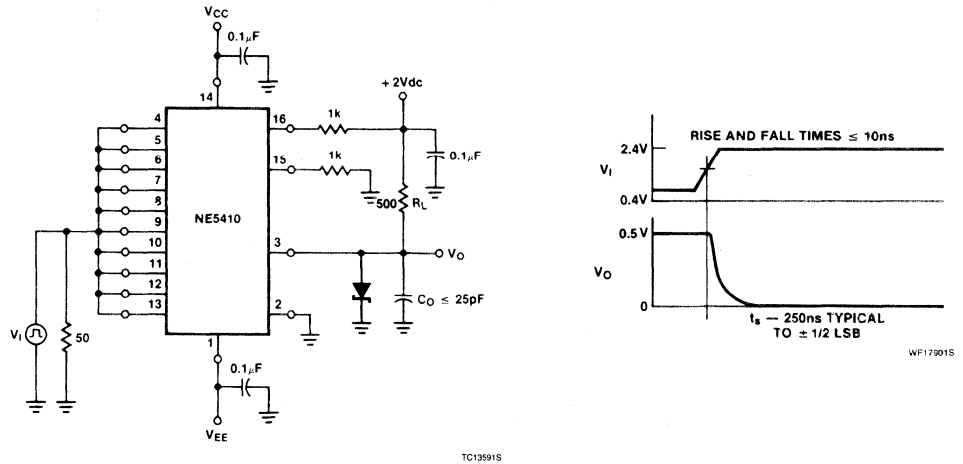


Figure 7. Settling Time

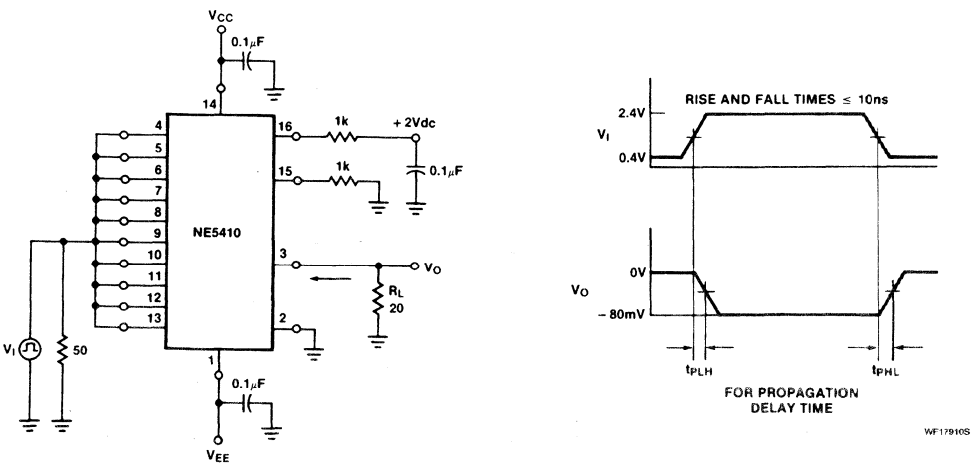
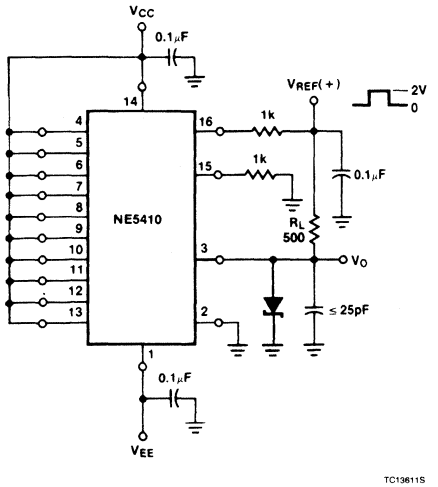
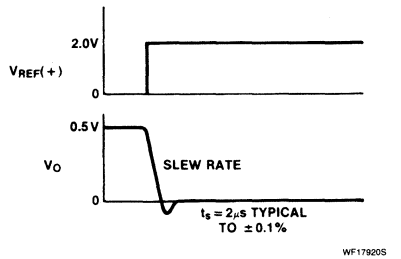


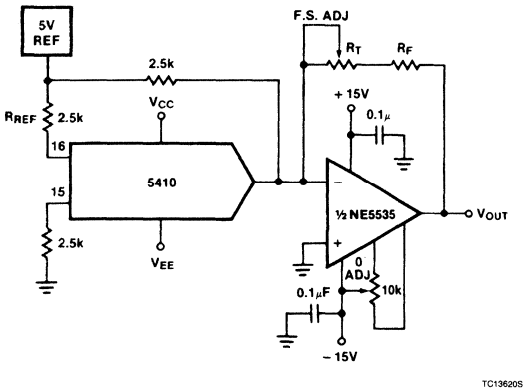
Figure 8. Propagation Delay Time

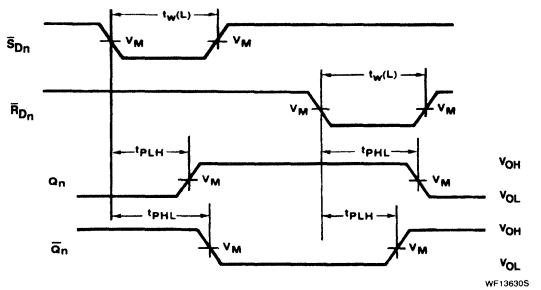




NOTE:
Use $R_L = 20\Omega$ to GND for slew rate measurement.

Figure 9. Reference Amplifier Settling Time and Slew Rate

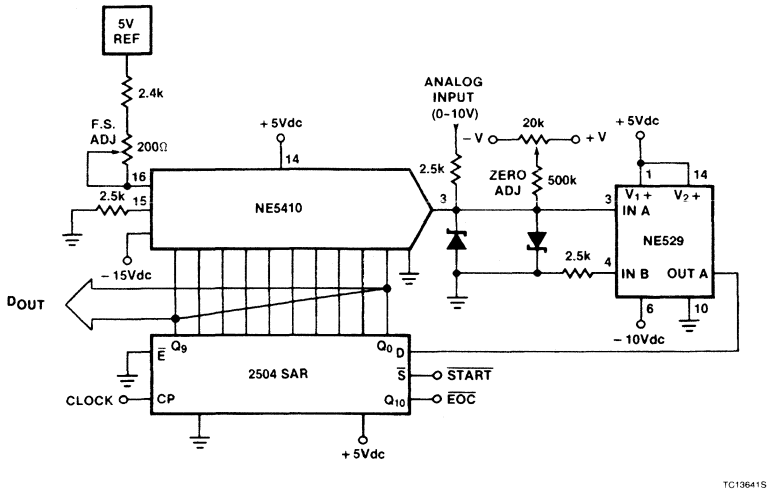




a. Bipolar Output (–10 to +10V)

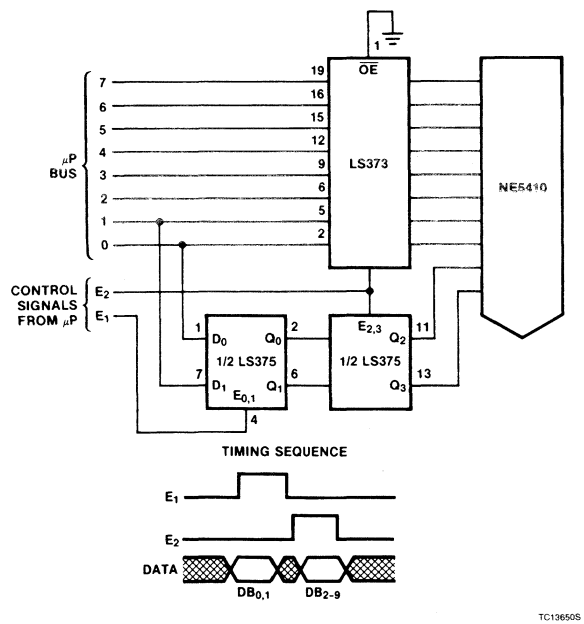
b. Unipolar Positive Output (0 – 10V)

Figure 10. Voltage Output Circuits



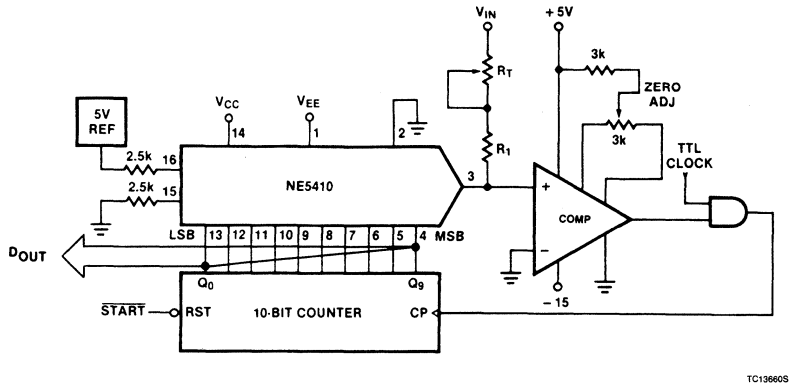
NOTES:
10-bit conversion time = 3.3μs with 3MHz clock.
This converter uses a 2504 12-bit successive approximation register in the short cycle operating mode where the end of conversion signal is taken from the first unused bit of the SAR (Q_{10}).

Figure 11. Successive Approximation A/D Converter



NOTE:
With this double latch technique, valid data will be latched to the DAC until updated with the E_2 pulse. Timing will depend on the processor used.

Figure 12. 8-Bit μP Bus Interface



NOTE:

V_{IN} FULL SCALE = 4mA $(R_1 + R_T)\left(\frac{1023}{1024}\right)$

Figure 13. Staircase A/D

AN106
Using the DAC08 Without Negative Supply

Application Note

USING THE DAC08 WITHOUT A NEGATIVE SUPPLY

The DAC08 can be used without a negative supply if a few precautions are observed:

1. V_{CC} must be in the range of 10V to 30V.
2. $V_{REF(-)}$ must be at least 3V more positive than Pin 3 at all times.
3. Pins 2 and 4 must always be at least 5V above Pin 3 for reference currents up to 2mA, and at least 8V above Pin 3 for reference currents above 2mA.
4. Pin 1 must be at least 5V above Pin 3.

Figure 1 shows the DAC08 in a circuit without a negative supply with two MC1489s used as level shifters. The need for level shifters is implied from requirement 4 above, since the logic threshold is about 1.35V above Pin 1. V_O must be the same potential as the positive logic supply because of the internal circuitry of the MC1489.

If $V_{REF(+)}$ is a very stable source with no ripple or noise, R1 and R2 can be a single resistor. The same is true of R3 and R4 if $V_{REF(-)}$ is a very stable source. Resistor values are determined as follows:

$$R1 + R2 = \frac{V_{REF(+)} - V_{REF(-)}}{I_{REF}}$$

$$R3 + R4 = R1 + R2$$

where I_{REF} is reference current through R1 and R2
(Pin 14 is at $V_{REF(-)}$ potential)

The value of the compensation capacitor, C_C, is determined by the relationship:

$$C_C = 15\ (R1 + R2)$$

where C_C is in pF and R1 and R2 are in kΩ.

V_O (DAC08 Pin 1 and MC1489 Pin 7) must be at least 5V for DAC08 reference currents at or below 2mA, and at least 8V for reference currents above 2mA. V_O must also be equal to the positive potential of the logic supply, as mentioned above. It should be noted that the MC1489 inverts the logic inputs.

EXAMPLE

Power supply voltages of +5V and +15V are available and the input logic is TTL. The need is for a DAC with a full-scale output of 2mA.

- V_O is set to +5V
- V_{CC} for the DAC08 and the MC1489 are set to +15V
- If $V_{REF(+)}$ and $V_{REF(-)}$ are set to +15V and +5V respectively,

$$R1 + R2 = \frac{15 - 5}{I_{REF}} = \frac{10V}{2mA} = 5k\Omega$$

- R3 + R4 should also add up to 5kΩ.
- C_C is 15(5)pF = 75pF.

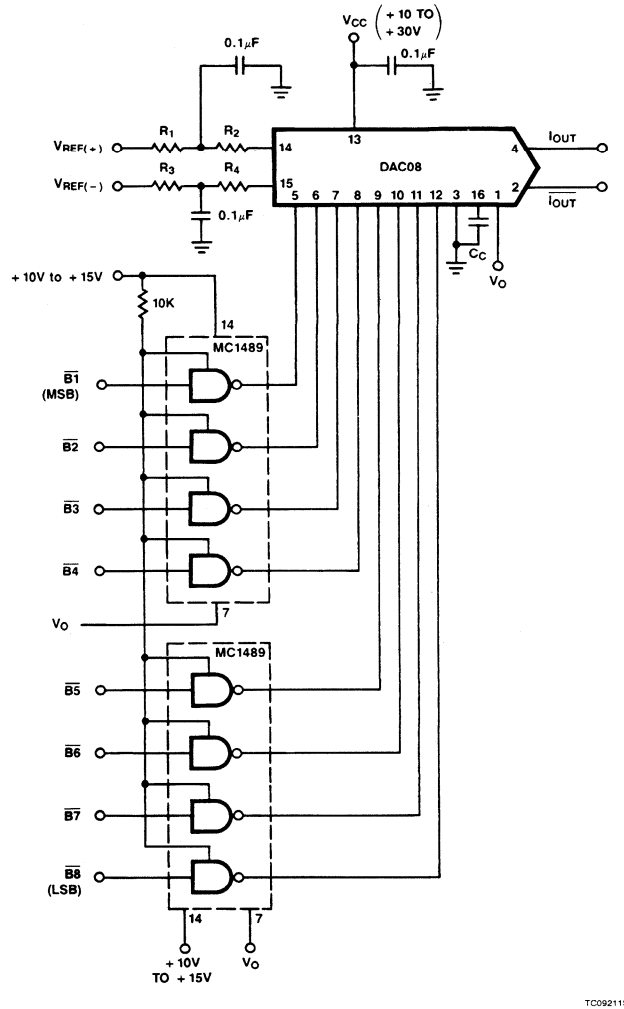


Figure 1. Using the DAC08 Without a Negative Supply

AN109
Microprocessor-Compatible DACs

Application Note

DAC products are designed to convert a digital code to an analog signal. Since a common source of digital signals is the data bus of a microprocessor, DAC circuits that are bus compatible ease the design engineer's interface problems.

WHAT FEATURES MAKE A DEVICE BUS-COMPATIBLE?

The five conditions which determine processor bus compatibility are:

- Inputs must present low bus load
- Addressing must be provided
- Inputs must be latched
- Logic thresholds must be compatible
- Timing requirements should be adequate ($< 1\mu s$)

Signetics' microprocessor-compatible DACs, the NE5018 series, meet these requirements. In addition, they provide an internal reference source. The NE5018 provides a scaled voltage output, eliminating the need for an external op amp. The NE5118 is identical to the NE5018, except it provides the user with a current output. Figure 1 shows a typical microprocessor system with analog output using the NE5018 to provide a programmable voltage and an NE5118 to provide a programmable current.

The following discussions detail the operation of the NE5018 and NE5118 series DACs.

LATCH CIRCUIT

The latch circuits of the NE5018 and NE5118 are identical. Both the data inputs and latch enable ($\overline{LE}$) input feature ultra-low loading for ease of interfacing. The 8-bit data latch, controlled by the latch enable input, is static and level sensitive. When ($\overline{LE}$) is low, all the latches become transparent and the output changes as the bit pattern changes on the data bus. When the latch enable returns to its high state, the last set of inputs are held by the latch and a unique output corresponding to the binary word in the latch is produced. While the latch enable is high, the latch inputs represent a high impedance load on the data bus and changes on the data bus have no effect on the DAC output.

The digital logic input for the NE5018 and NE5118 series DACs utilize a differential input logic system with a threshold level of +1.4V with respect to the voltage level on the digital ground pin (Pin 1). To be compatible with microprocessors, the DAC should respond in as short a period as possible to insure full utilization of the microprocessor and I/O data bus lines. Figure 2 gives the typical timing requirements of the latch circuits in the NE5018 and NE5118.

The voltage levels on the data bus should be stable for approximately 150ns before latch enable returns to high level. The timing diagram shows 100ns is required for setup time and the information on the data lines should remain valid for another 50ns.

REFERENCE INTERFACE

The NE5018 and NE5118 contain an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long-term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5V reference output. Providing a $V_{REF\ ADJ}$ (Pin 12) allows easy trimming of the reference output (Pin 13). Use of a 10k pot and series resistor, as shown in Figure 3, adjusts the gain of the buffer amplifier, therefore varying the output reference voltage level.

This network can then be used as a full-scale output adjust. A variation in the $V_{REF\ OUT}$ of ~0.8V, results in a corresponding 1.6V variation in the full-scale output. This is more than adequate since the untrimmed $V_{REF\ OUT}$ is typically within 200mV of the nominal 5V. The $V_{REF\ OUT}$ will provide a maximum of 5mA drive and can be used as a reference voltage for other system components, if required.

Since a potential need exists to use the NE5018 and NE5118 as multiplying DACs, the V_{REF} is not connected internally, allowing the use of external reference sources. To utilize the internal reference, the $V_{REF\ OUT}$ (Pin 13) must be jumper-connected to the $V_{REF\ IN}$ (Pin 14). This also makes it possible to use a common reference for other D/A or A/D circuits in a system.

INPUT AMPLIFIER OF THE NE5018

The DAC reference amplifier has been designed to eliminate the need for compensa-

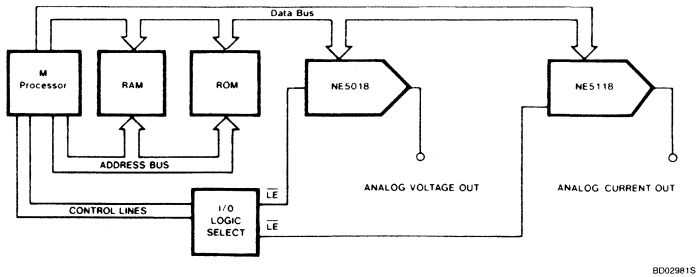


Figure 1. Interfacing to a Microprocessor

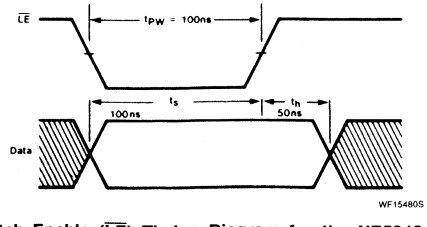


Figure 2. Latch Enable ($\overline{LE}$) Timing Diagram for the NE5018 and NE5118

tion when operating from the internal reference or from an external reference which is buffered by an op amp or low impedance source. Compensation is required, however, when operating from a high impedance source. The addition of an external resistance reduces the phase margin of the amplifier making it less stable. Compensation, when required, is a single capacitor from Pin 16 to ground.

Figure 4 details the input reference amplifier and current ladder. The voltage-to-current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5V V_{REF}. This current sets the input bias to the ladder network. Data bit 7 (DB_7) Q_7, when turned on, will mirror this current and will contribute 1mA to the output. DB_6 (Q_6) will contribute ½ of that value or 0.5mA, and so on. If all bits are on, the output current will be 2mA – 1 LSB. The full-scale V_{OUT} will be ($I_{OUT}R_F$) or 2mA – 1 LSB × 5k) = (10V – 1 LSB) = 9.961V. The overall input/output expression for the NE5018 is:

$$V_{OUT} = 2V_{REF} \times \left(\frac{DB7}{2} + \frac{DB6}{4} + \frac{DB5}{8} + \frac{DB4}{16} + \frac{DB3}{32} + \frac{DB2}{64} + \frac{DB1}{128} + \frac{DB0}{256} \right)$$

The minimum current for the ladder network to be operative in the linear region is 500μA. Therefore, the minimum V_{REF} input is 2.5V. The slew rate of the reference amplifier is typically 0.7V/μs without compensation. The input structure of the NE5118 is slightly different and will be discussed in greater detail later. Q_T provides a termination for the R-2R ladder network and does not contribute to I_{OUT}.

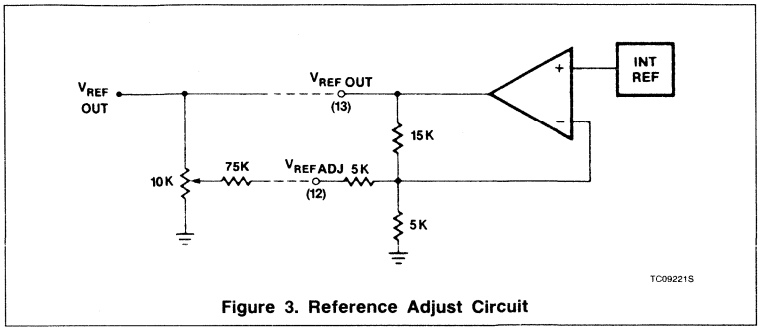


Figure 3. Reference Adjust Circuit

OUTPUT INTERFACE OF THE NE5018

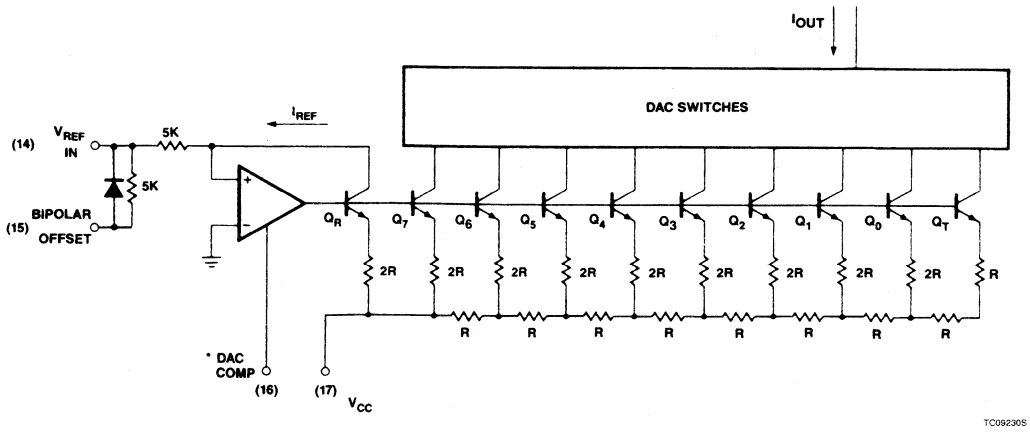
The NE5018 has an internal op amp which provides a voltage output, while the NE5118 is a current output device. The NE5018 output op amp is a two-stage design with feedforward compensation. Having a slew rate of 10V/μs, it provides a voltage output from 0 to 10V (±0.2%) typically within 2μs (the time allowed for the output voltage to settle to within ½ LSB). Compensation must be provided externally as shown in Figure 5.

The addition of the optional diode between the summing node (Pin 20) and ground prevents the DAC current switches from driving the op amp into saturation during large-signal transitions which would increase the settling time.

Zero adjust circuits, such as the one shown in Figure 5, may also be connected to the summing node to provide a means to zero the output when all zeros are present on the input. Not all applications require a zero adjust circuit since the untrimmed zero-scale is typically less than 5mV. Excess stray capacitance at the sum node of the output op amp may necessitate the use of a feedback capacitor from V_{OUT} to the sum node (C_{FF}) to insure stability of the op amp. Typical values of C_{FF} range from 15 to 22pF. The rated load of the op amp is ~ 2kΩ. For stability, the load capacitance should be minimized (50pF max).

MODES OF OPERATION OF THE NE5018

The NE5018 has two basic modes of operation: unipolar and bipolar. When operating in the unipolar mode, the output range is 0 to +10V. To change from unipolar to bipolar operation, the bipolar offset pin is connected



NOTE:
DAC compensation may be required if V_{REF} resistance exceeds 10kΩ.

Figure 4. R-2R Ladder Network Develops a Scaled Reference Current Value Into the DAC Switching Network

to the summing node. This provides the 5V offset required for this mode of operation. The output now will have a range from −5 to +5V. Figure 6 details the connection of the NE5018 in the bipolar mode of operation.

With the bipolar offset, Pin 15, connected to the sum node, Pin 20, it forms a unity gain inverter with an input of $+V_{REF}$. The bipolar offset develops an I_{REF} current through the internal 5k resistor. This current is then fed to the sum node of the output amplifier where it is summed with the current output of the DAC ladder network. Assume for the moment that the current output of the ladder network is 0mA. With a V_{REF} equal to +5V, I_{REF} is 1mA and the output of the op amp is converted to −5V. If the DAC switches are now set to full-scale, the current from the DAC ladder is 2mA. This is summed against the 1mA I_{REF} and causes the output of the op amp to swing from −5V to +5V.

$(I_{DAC} - I_{REF})5k = (2mA - 1mA)5k = +5V$

Since the bipolar offset resistor is monolithic, tracking with the 5k feedback resistor of the output amplifier is excellent.

Note that the bipolar offset pin could not be used when using the DAC in a multiplier application since the V_{OUT} would reflect an inverted input signal.

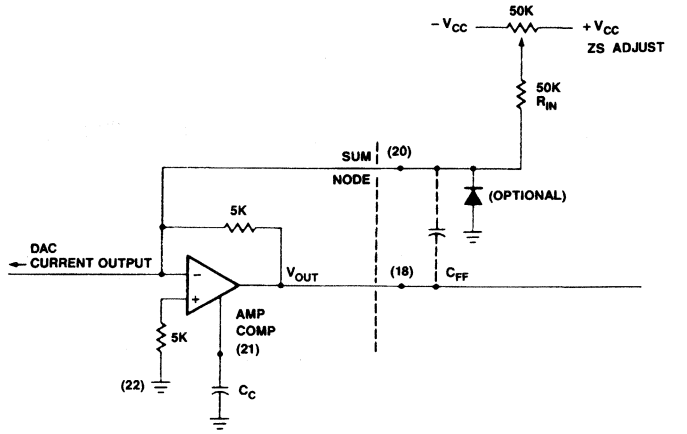


Figure 5. Zero-Scale Adjust

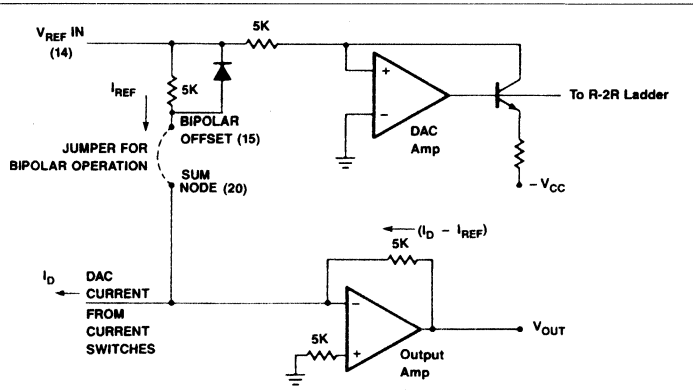


Figure 6. Bipolar Output

NOTES ON THE NE5118 CURRENT OUTPUT DAC

The basic operation of the NE5118 current output DAC is the same as the NE5018. The current output structure allows the user to provide a programmable current sink (I_{OUT} max of 2mA). Several jumper options provide a variety of operational modes. Figure 7 is a block diagram of the NE5118. The input logic and V_{REF} portions are identical to the NE5018.

REFERENCE INPUT AMPLIFIER

The characteristics of the reference input amplifier are identical to the NE5018; however, extended versatility of the input structure allows for both current (via Pin 14) or voltage (via Pin 15) reference inputs.

The maximum DAC output current is 2mA. The DAC has an internal gain of 2, limiting the maximum usable input current to 1mA.

NOTE:

The absolute maximum input current should be limited to 5mA to prevent damage to the input reference amplifier.

Figure 8 shows the basic operating mode of the NE5118 using an external current reference resistor (R_1) and a positive reference voltage.

This voltage can be provided by either an internal or external reference voltage. Figure 9 shows a typical connection using a voltage input directly via Pin 15.

Besides a reduced parts count, use of the internal R_{REF} provides excellent tracking characteristics with the R_{OUT} resistor (Pin 20) when developing a high slew rate voltage output. The negative V_{REF} input must be returned to ground directly or through R_2. R_2 is optional and is used to cancel minor errors developed by the input bias currents of the reference amplifier ($R_2 = R_1$ in Figure 8). A negative voltage can be the reference by using the $-V_{REF}$ input pin as shown in Figure 10.

The positive V_{REF} is returned to ground via R_{IN} (Pin 15). As with the NE5018, a compensation capacitor on Pin 16 is not required if the V_{REF} is supplied by a low impedance source.

OUTPUT STRUCTURE

The output of the NE5118 is a current sink with a capacity of 2mA (full-scale) capable of settling to 0.2% in 200ns. Internal bias and feedback resistors are also made available to ease the designer's task of interfacing.

Figure 11 shows the NE5118 using a current-to-voltage converter at the output to provide a high slew rate voltage output. Using the NE538 as shown can provide 60V/μs slew rate output. The diode at the inverting node of the op amp improves the response time by preventing saturation of the op amp during large signal transitions. The feedback resistor

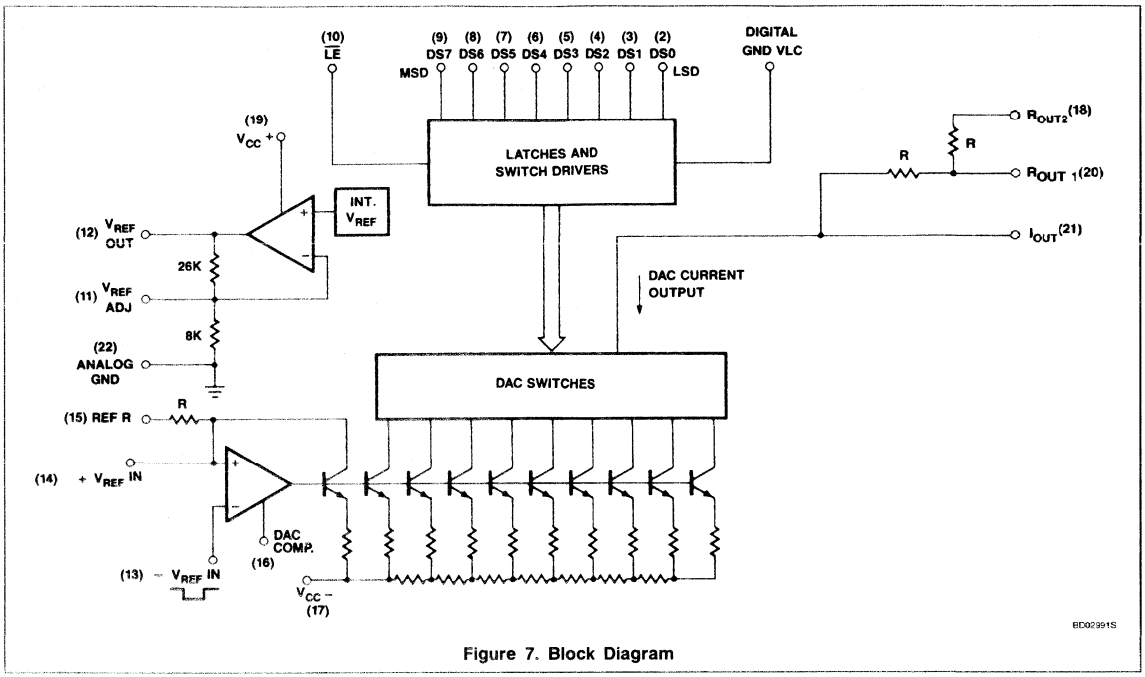


Figure 7. Block Diagram

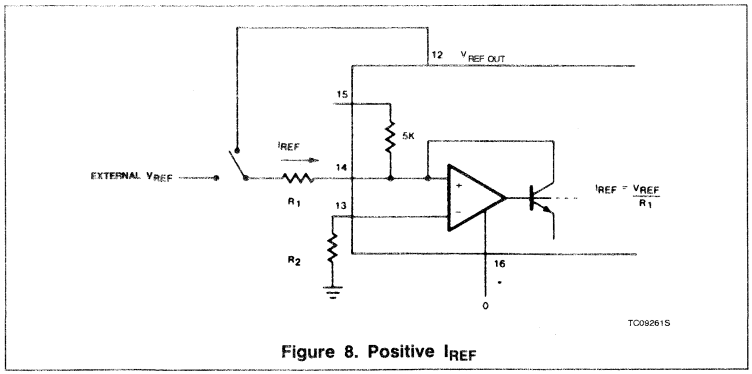


Figure 8. Positive I_{REF}

R_{OUT1} (Pin 20) is provided internally, providing excellent thermal tracking characteristics with the R_{REF} at the input.

Bipolar operation can be accomplished by connecting the V_{REFOUT} (Pin 12) to the R_{OUT} resistor (Pin 20) (Figure 12). The principal is the same as the NE5018 bipolar operation. The internal resistors exhibit excellent thermal tracking characteristics.

An alternate method of bipolar output operation is shown in Figure 12. The R_{REF} and R_{OUT} set up a current-to-voltage converter while two (2) external resistors provide a bipolar offset. R_{EXT_1} and R_{EXT_2} should have similar thermal tracking characteristics.

The NE5118 can provide a voltage output directly when driving a high impedance load as shown in Figure 13. With a full-scale current of 2mA, Pin 20 tied to +10V and a digital input of zero, the high impedance load will see +10V. For a full-scale digital input, the load will see 0V. Since the load and the internal resistor form a voltage divider, their ratio determines full-scale accuracy.

By connecting the R_{OUT} resistor (Pin 20) to ground (Figure 13), the output voltage seen by the load ranges from 0V as zero-scale to −10V as full-scale. Only a few of the many possible output configurations have been shown to demonstrate the NE5118 flexibility.

CIRCUIT EXAMPLES

Now that the basics of the NE5018 and the NE5118 have been discussed, let's examine some specific circuits. Figure 14 is a microprocessor-controlled programmable gain amplifier, using the NE5018. The V_{REF} output is fed to the non-inverting input to a differential amplifier. $R_1 + R_2$ places $2.5V_{DC}$ bias on the V_{REF} input. R_2 can be made adjustable to precisely control the DC reference input. The analog input is fed to the inverting input of the differential amplifier with a gain of unity. An input range of 0 to 2.5V will produce an output of 10V to 5V full-scale. $V_{REF\ IN}$ will vary from 5V to 2.5V. The current ladder is always kept in the linear operating range and the output will not become distorted.

No compensation is required for the DAC reference amplifier since the $V_{REF\ IN}$ is fed from a low impedance source. With a compensation cap of 33pF on the output amplifier, the frequency response of the output is linear to at least 20kHz with less than 0.1% distortion with an input amplitude of $1V_{P-P}$. The NE5018 is seen by the microprocessor as an I/O device.

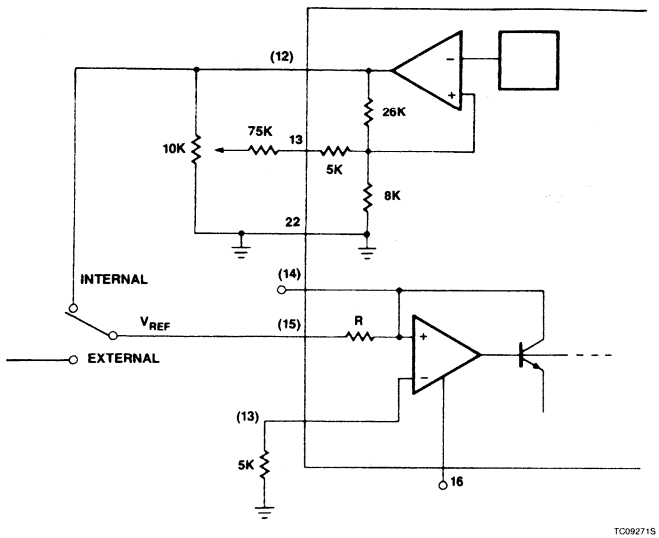


Figure 9. Positive V_{REF}

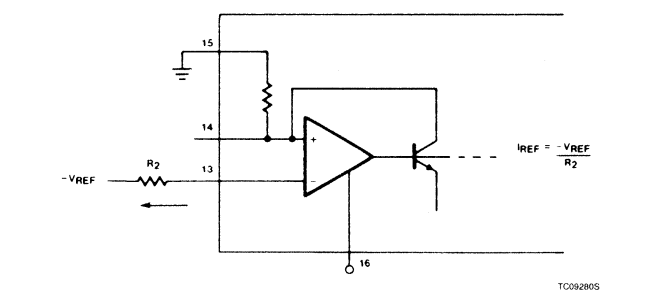


Figure 10. Using a Negative I_{REF}

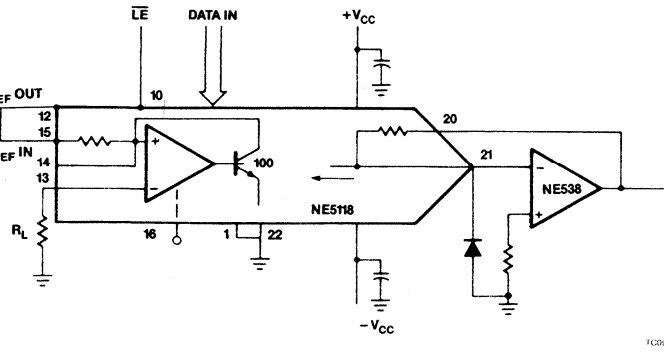


Figure 11. High Slew Rate Voltage Outputs

In Figure 15, the N5018 and NE5118 provide a method of summing two digital words and generating a voltage output. The latch enable feature of both devices direct connection to a data bus, using address decoding. These devices greatly reduced the total component count required to perform this operation.

The reference voltage is common to both DACs, being provided by the NE5018. The bipolar offset resistor of the NE5018 provides the 1mA current reference for the NE5118. Using the internal resistor of the NE5018 to develop the reference current enhances the thermal tracking since the current-to-voltage resistor of the output op amp is also in the NE5018. Both DACs can be addressed by a microprocessor using an address decoder to select DAC A or DAC B.

Figure 16 is a schematic of the NE5118 and a NE527 as a high-speed programmable limit sensor (or A/D converter). A 4.8V zener diode is used on the comparator input to insure the input voltage range of the comparator is not exceeded. The outputs of the NE527 comparator are complementary, easing the logic interface requirement. If the strobe function is not used, the strobe inputs should be tied high, through a 10kΩ resistor.

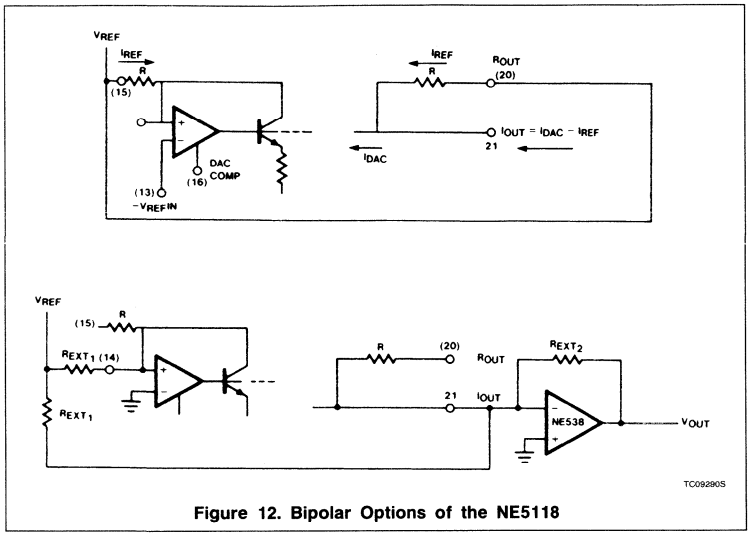
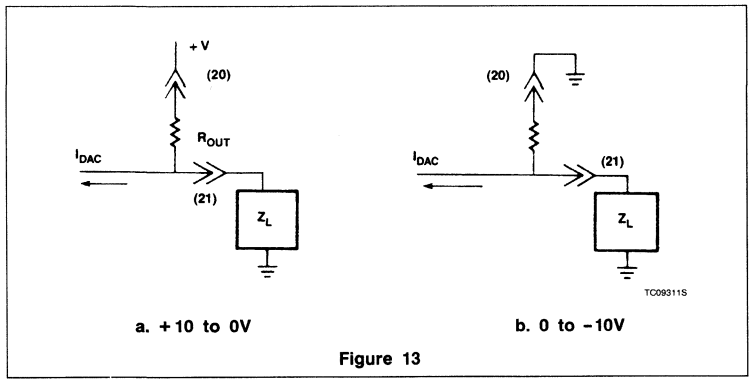


Figure 12. Bipolar Options of the NE5118



a. +10 to 0V

b. 0 to −10V

Figure 13

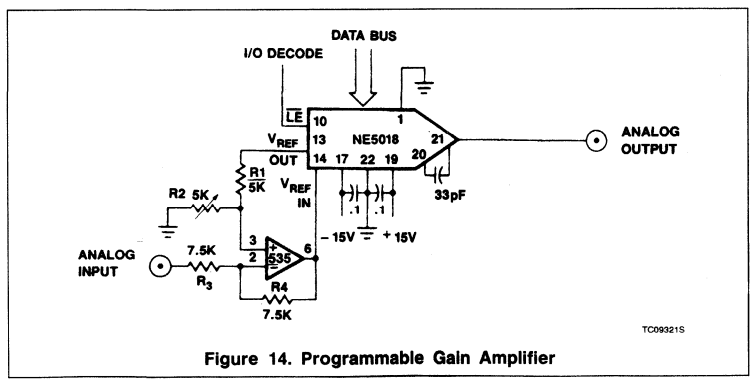


Figure 14. Programmable Gain Amplifier

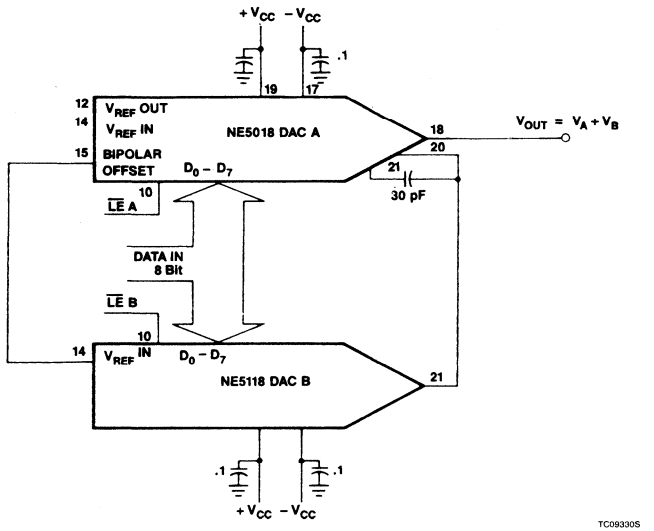


Figure 15. Analog Summation With Digital Inputs

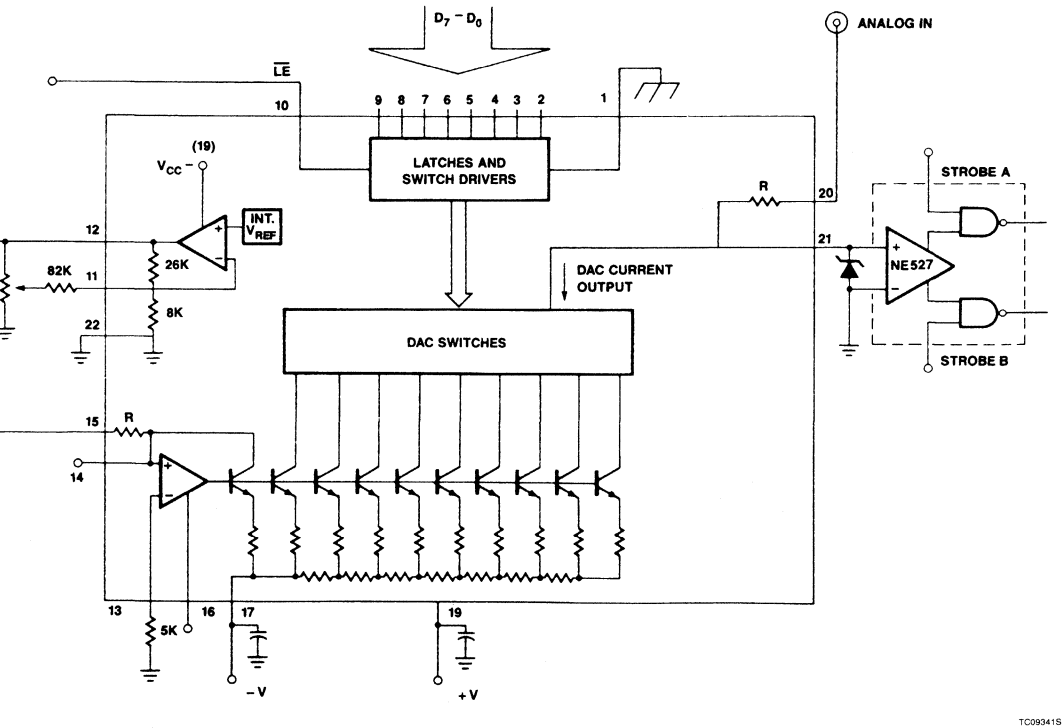


Figure 16. Programmable Limit Comparator

AN1081
NE5150/51/52 Family of Video Digital-to-Analog Converters

Application Note

INTRODUCTION

Raster-scan systems and bit-mapped graphics are here to stay. For a computer to be of use, it needs an interactive means of communicating with the user. So for every computer, whether it is a 10MFLOP (millions of floating-point operations per second) supercomputer or a home computer for playing video games, some type of terminal or graphics display device is needed. Not long ago, inputs to the computer were made using stacks of Hollerith cards pushed into a hopper and then read into the computer. Results would then come from a printer. The hardcopy results were exactly what they looked like: final judgment from the computer. In order to respond, it was back to the punch-card machine. Needless to say, debugging programs became quite laborious. This problem led to the interactive display, allowing the user to enter information and see the results immediately. A new age in computing had arrived.

The areas of word processing, on-screen circuit simulation, and computer graphics developed with great rapidity. As technology improved, so did the ability to make larger displays having more colors and better resolution. As software developed, so did techniques such as windowing, the use of icons, and the ability to use graphic input devices such as mouses, light pens, and joysticks. Three-dimensional images and photographic quality reproduction soon followed.

Of the different technologies, how did raster scanning predominate over other forms? What differentiates bit-mapped graphics systems from character or vector-map systems? In the following sections it will become clear how technology and economics drove the market and, consequently, product development.

Displays: Raster, Vector Refresh, Storage Tube

A *raster* is technically a display of horizontal lines. How the display is created is what makes it unique. An electron beam generated by a CRT (Cathode Ray Tube) and containing video information, starts at the top left of the screen and traces a path to the right part of the screen (see Figure 1). It makes a slight angle as it travels across. The gun is then turned off as the beam rapidly returns to the left. It then repeats this zig-zag path until it reaches the bottom of the screen. The gun is again turned off as the beam travels back to the top of the screen. This entire process is repeated from 30 to 60 times per second so flicker is decreased (motion pictures or film typically display 24 images per second). What the electron beam has done is *scanned* its information onto the screen. This process is called *raster scanning.*

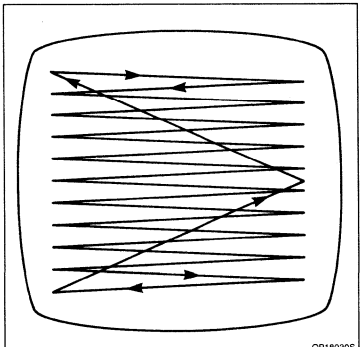


Figure 1. Raster-Scanned Display

All television sets display information in this manner. For television sets in the United States, the screen is redrawn 30 times per second. Additionally, the screen is *interlaced*, meaning that every other line is scanned and then the lines in between are scanned. This gives the illusion that the image is continuous. Since the television sets have 525 lines, 262.5 lines are scanned first (the odd field) and then the other 262.5 (the even field) are scanned. To visualize this, consider a 21-line system (see Figure 2). Scanning occurs at the above-mentioned 30Hz rate which is also known as the *frame rate*. Two fields (odd and even) equal one frame. Scanning 525 lines 30 times a second equals 15,750 horizontal lines scanned in a second. This is called the *horizontal scan frequency*. These are standard in the U.S., coming under the standard known as NTSC (National Television Standards Committee). In Europe, television has 625 lines and has a frame rate of 25Hz, or half the power line frequency, 50Hz.

Vector refresh displays, or stroke-writers, work on the principle that one line is the base unit of information. Each line then corresponds to a vector. Instead of scanning continuously, information is drawn line-by-line, hence the name stroke-writer. These systems off-load the refreshing tasks to special hardware, making the system slightly more cost-effective. Still, during the 1960's making them proved too expensive for everyday applications.

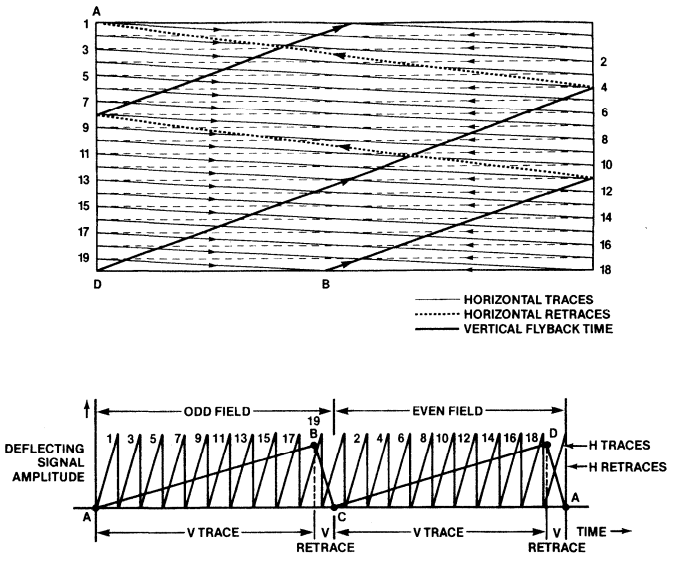
In 1971, Tektronix introduced the Direct View Storage Tube (DVST) for displaying and interfacing graphic data. It was based on oscilloscope techniques, storing information in a special, long-persistence phosphor which coats the inside of the screen. The display resolution is limited only by the phosphor grain size and the quality of the deflection circuitry. Although inexpensive, these devices were fine for oscilloscopes in the lab, but too cumbersome for fully interactive work. When the screen would redraw itself after the entry of new information, the sudden disappearance and reappearance was almost like looking at the light of a camera flashbulb. Another problem with the storage refresh screen was that when new information entered, it would write directly over the existing information. Only upon refreshing the screen would the new information be clear and readable. In many cases, the annoyance did not justify the low cost.

Bit-Mapped Graphics

In a bit-mapped graphics system, the screen is divided into individual elements called pixels, short for picture elements. When they say "bit-mapped", each pixel corresponds to a bit, or, in most cases, an address or memory location. This is what differentiates television from bit-mapped computer displays. Although both systems use raster scanning techniques, the information transmitted on television is continuous — a stream of analog information between horizontal sync pulses (the pulses used to denote the beginning and end of a horizontal line) — whereas in bit-mapped systems, each line is divided into discrete elements (the aforementioned pixels). The approximation of analog images would then be determined by the pixel density or screen resolution. As an example, Figure 3 shows a line approximated by a finite number of pixels.

The lines seem to staircase rather than flow because of the enlargement of the pixels. The effect is known in some computer graphics circles as "jaggies", short for jagged edges.

So, with more pixels, better resolution is possible. This is not without a price, though. Since each pixel corresponds to a memory



NOTES:
A sample scanning pattern for 21 interlaced lines per frame and 10½ lines per field. The corresponding H and V sawtooth deflection waveforms are shown below pattern. Starting at point A, the scanning motion continues through B, C, and D, and back to A again.

Figure 2. Interlaced Raster for 21-Line System

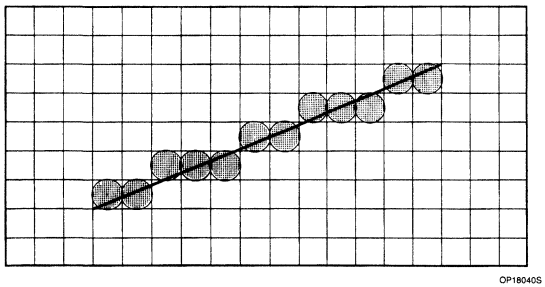


Figure 3. Ideal Line and Its Discrete Pixel Representation

location, memory cost rises dramatically as pixel resolution increases. Drawing speed must also increase since more pixels have to be drawn to maintain the ⩾30Hz frame rate needed to avoid flicker. Clearly then, the increase in bit-mapped graphics systems can be tied to the continuing price reductions in memory, specifically, the Dynamic Random Access Memory (DRAM). Fortunately, as the price has dropped, the memory size has not stood still. The last 14 years have seen size increases from 4k to 16k, 16k to 64k, 64k to 256k, and now, 256k to 1M bits of memory. One might expect to see DRAMs on the order of 4Mb within 2 to 3 years. Additionally, the continuing development of video RAMs cannot be ignored.

A bit-mapped system might be described in one of three ways. First, assume the display is monochrome and that each pixel can be represented by a certain number, for instance, 4 bits of information. This means that there are $2^4 = 16$ possible values of shading. Each bit of information can be represented by a "plane" of information. The plane would correspond to the area that was mapped by the pixels, namely the drawing area or display. Imagine an 8×8 pixel display. This means that there are 4 bit-planes and each pixel would have to pierce all four planes to give the proper information (see Figure 4). This is a fairly quick way to draw the screen since the data goes directly from the bit-map to the DAC (Digital/Analog Converter; DAC is singular here since the display is monochrome).

A direct conversion system for color is the second step. This is just an upgrade of the first case. Instead of 4 bit-planes, there are 12: three sets of the 4 planes for the three primary colors red, green, and blue. The advantage here is that there are now $2^{12} = 4096$ different colors, but the corresponding disadvantage is that the memory requirement has tripled. For more bit resolution per pixel, the associated memory demands increase by 3 times the pixel size times n, where n is the additional bit of resolution per pixel.

The third type of bit-map system uses a color look-up table (CLUT) as the driver for the display. The operation is straightforward. As the controller scans the bit-map each time it comes upon a pixel, it retrieves the bits which are then decoded into an address. This address is a pointer to the look-up table where sixteen 12-bit words (colors) are stored (see Figure 5). Once selected, that word is then sent to the color DACs and, from there, to the screen. The idea is similar to that of having cache memory in a computer, a fast memory used when the information in the memory is frequently accessed. Note that the bit-planes grow as n for 2^n additional colors while memory grows for 3n in the direct conversion case, a definite savings in memory.

The limitation in this case is that only 16 colors can be displayed at a time. In some systems, however, the CLUT is fast enough to be reloaded during the horizontal retrace time (CLUT size is sometimes referred to as the maximum number of colors that can be displayed on one horizontal line). This is especially important if the image is to simulate a smooth motion such as the rotation of a merry-go-round or the movement of an object with mirrored surfaces. In most cases, 16 colors is sufficient for any single display. 64 colors (6 bit-planes) is extremely good. 256 colors (8 bit-planes) is definitely a luxury.

It's clear that the memory speed and memory density, which are direct functions of the color and screen resolution, play a large part in the feasibility of a bit-mapped system. For that reason, the enormous gains and technological advancements in the field of memory design have made bit-mapped raster-scan graphic systems the best choice for both cost and performance.

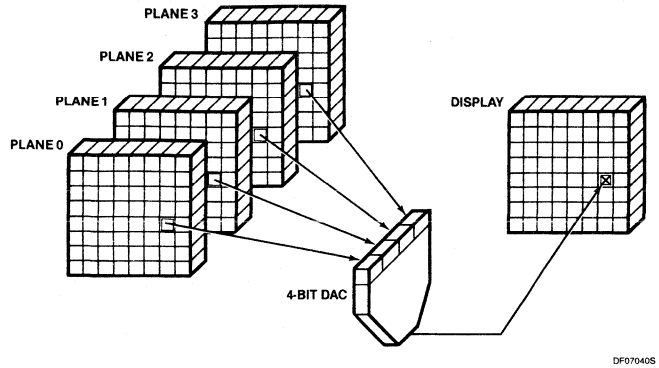


Figure 4. Monochrome Bit-Map With Direct Conversion to Display

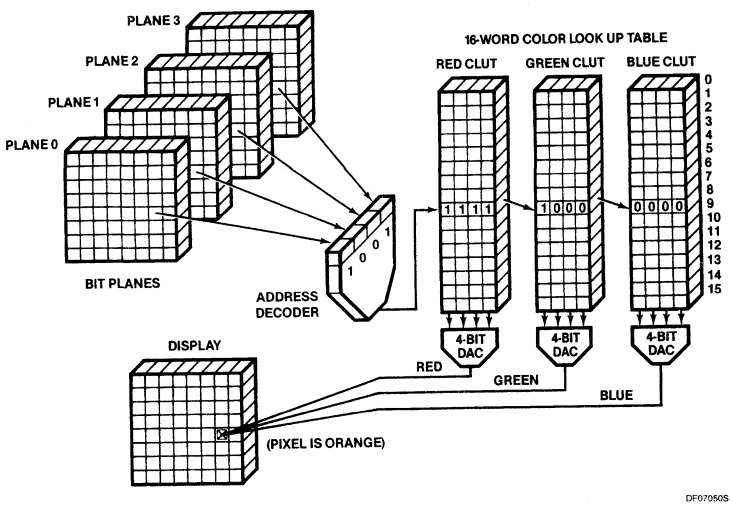


Figure 5. Color Bit-Map With 16-Word Color Look-Up Table

ISSUES FOR GRAPHIC DISPLAY SYSTEMS

Making the DAC Fit the Application

When designing graphic display systems, there are many decisions to be made in specifying the hardware and software needed for a system. What kind of speed is necessary in a given application? What kind of resolution will the users of the system require? Is color needed or will monochrome be adequate? If color, how many colors? Will images be viewed in two or three dimensions? How much memory is needed? How should the microprocessor/CRT controller/video DAC/frame buffer be matched with the rest of the system? What's the best type of software for a particular application? and on and on. . .

These questions could form the subject of an entire book and so will not be discussed in detail. This section will, however, discuss the few issues needed in the selection of the proper video DAC for a system.

Display Resolution vs Bit Resolution

When the quality of a display terminal is being evaluated, one primary consideration is the kind of resolution it has. There are two different types of resolution: display resolution, which is determined by the monitor and cannot be changed by the design; and bit resolution, which is dependent on the design of the video DAC used.

Display resolution determines how many pixels can be projected onto the monitor at any one time. (Actually, only one pixel is displayed on the screen at a time, in rapid succession). Table 1 shows commonly-used screen resolutions corresponding to various applications.

However, since each pixel must correspond to a memory element, the more pixels per screen the faster the DAC and video RAM must be in order to write the information to the screen fast enough to avoid flicker. This imposes speed requirements that have to be satisfied.

The other type of resolution, bit resolution, depends on the type of DAC used. The number of bits converted also determines the size of the color palette which is the number of possible colors that can be displayed. This should not be confused with the number of colors displayed at once (see Section on Color Look-Up Tables). Assuming that the monitor is an RGB-type, the bit resolution, n, must be multiplied by 3 to get the total bit resolution, 3n. Taking this number as 2^{3n} gives the size of our color palette. Table 2 shows common bit sizes for video DACs with their corresponding palettes.

It should be clear that, if imaging is the goal, a higher bit resolution gives access to the assorted tones and mixtures of colors that make color graphics as realistic as possible. The major problems associated with higher-resolution DACs are that they are larger and more complex than lower-resolution DACs and tend to take longer for their signals to settle. This has a direct effect on selection of the proper DAC for a particular system because of the DAC's bandwidth and because of the need to weigh advantages and disadvantages of higher and lower bit resolutions.

For a low-end personal computer graphics screen on which the pixels can actually be seen at arm's length, it makes little sense to have a bit resolution that shows flesh tones because the benefit of the large palette is defeated by a screen that shows jagged edges. On the other hand, having a high screen resolution with a limited amount of colors does not defeat the purpose in the same way — if many colors aren't needed.

Integrated circuit layout, for instance, may not require thousands of colors — only enough to distinguish 12 – 15 masks; but sharply defined edges and zooming ability are needed to examine the circuit. The need for this user could be a bit resolution of 2 (64 colors) and a display resolution of 1024 × 1280.

For all this talk of colors and bit resolution, monochrome should not be totally ignored. After all, people got along fine with black and white TV for years before color came along. For applications such as word processing or

Table 1. Display Resolutions With Applications

DISPLAY RESOLUTION	APPLICATION
250 × 500	Low-end personal computers (home computers)
640 × 480	High-end personal computers
600 × 800	Next-generation personal computers
768 × 576	Next-generation personal computers
1024 × 800	Workstations
1024 × 1024	High-end workstations
1024 × 1280	High-end graphics terminals (CAE/CAD)
1024 × 1500	High-end graphics terminals (3-D Imaging)
1500 × 1500	High-end graphics terminals
2048 × 2048	High-end graphics terminals (photo quality)

Table 2. Bit Resolution With Palette Size

BITS/DAC	RGB	PALETTE SIZE	APPLICATION
1	3	8	Digital RGB, "rainbow colors"
2	6	64	Some home and personal computers
4	12	4096	Color workstations, CAD/CAE
6	18	262,144	High-end CAD/CAE, medical imaging
8	24	16,777,216	Photographic quality reproduction

Table 3. Display Resolution With Minimum DAC Speed

DISPLAY RESOLUTION	# PIXELS	MINIMUM DAC SPEED
250 × 500	125,000	10MHz
640 × 480	308,000	25MHz
600 × 800	480,000	38MHz
768 × 576	443,000	35MHz
1024 × 800	820,000	65MHz
1024 × 1024	1,049,000	85MHz
1024 × 1280	1,311,000	105MHz
1024 × 1500	1,536,000	125MHz
1500 × 1500	2,250,000	180MHz
2048 × 2048	4,195,000	330MHz

circuit design, monochrome is fine. To achieve different shades of black and white, no chrominance operation is necessary. All of the bit resolution can be done with one DAC to operate on the luminance, or brightness signal. In this case, the brightness resolution can be said to be 2^n. Remember, the decision to go with color or monochrome does not rest upon the designers of the graphics board. A monitor is either color or monochrome to begin with. Adding a color video DAC won't change that.

DAC Speed

The DAC's update rate or bandwidth is a crucial consideration in choosing a DAC if the type of monitor has already been specified. For raster-scan systems, a few calculations can be made to determine the minimum speed required for the DAC.

First of all, assume that the screen needs to be refreshed at 60Hz to avoid flicker. To account for the electron beam going back to the top to start the next frame, assume that the retrace time is 30% of the drawing time. Multiply the frame rate by 1.3 to account for the retrace. Thus, the minimum bandwidth for the DAC would be determined by the following formula:

Speed (Hz) = 1.3 (retrace factor)
× # pixels × 60Hz (frame rate)

For the screen resolutions noted earlier, a new table can be generated for the minimum DAC speed required (see Figure 8).

For the 60Hz frame rate, the screen is probably not interlaced. Interlacing the screen at 30Hz would give the same effect because interlacing gives the *illusion* that the screen is being refreshed at a faster rate. The DAC would only have to operate at a quarter of the speed of the 60Hz non-interlaced rate because only half of the lines are being drawn at a speed that's half the 60Hz frame rate. This is how scanning operates under the NTSC television standard. The FCC says that televisions can't refresh the screen faster than 30Hz, so interlacing was developed to get around it. There are no such restrictions in graphics monitors. In fact, there are monitors that have horizontal scan rates as much as 4 times faster (65kHz) than that for television (15.75kHz).

Color Look-Up Tables: Yes or No?

As mentioned in the Bit-Mapped Graphics section, graphic systems may have direct conversion from a bit-map or they can use color look-up tables (CLUTs). It should be pointed out that one is not necessarily faster than the other. Speed depends primarily on the system. A fast CLUT is of no use if the external frame buffer can't load a new set of colors into the CLUT during the retrace time (horizontal or vertical). A video DAC without the CLUT may be faster since it can bypass the memory accesses needed for the CLUT, but, as seen in the Bit-Mapped Graphics section, the extra cost of the bit-planes (1 million additional bits for a 1024 × 1024 display) may be excessive, and accessing the additional planes may produce some design problems.

If a CLUT is needed, the size of the CLUT should also be a major consideration. Each bit-plane added requires 2^n more memory cells. Constraints on die-size and power requirements become apparent. Also, one must ask whether one needs 16, 32, 64, 128, or 256 colors on every line. This depends on the color resolution desired *for the entire screen.* An easy way to determine the system needs is to picture the most common scene that would be displayed. The general rule is that the more complex and three-dimensional the images that are required, the more variations and shading are needed to truly represent them. Conversely, if the image is simple and two-dimensional, fewer colors would be needed. An example of the former would be geological formations. For the latter, consider the colors of flags of the world's nations. Almost all of them can be displayed with a CLUT of 16 colors. Remember, this refers to the number of colors needed at any one time.

No flag has more than 16 colors. The range of colors available for display after CLUT refresh depends on the color resolution or the number of data bits for each pixel.

Gamma Correction

A problem encountered in both television systems and in display monitors in general is the gamma effect. This is due to the nonlinear relationship between light output and the signal voltage applied to a cathode-ray tube. Although it would be desirable to have the luminous output of the phosphors on the display to vary directly with the changes in the signal applied to it, they usually do not. Each monitor has its own characteristic, but the international convention is to assume that the fractional value of the luminous output can be approximated by raising the percentage of display signal input to the 2.2 power. For example, a 60% of full-scale input signal will result in 33% of the full-scale luminous output ($0.6^{2.2} = 0.33$).

In Figure 6, the monitor does not respond linearly for a linear input signal. Adding a gamma correction circuit can take care of this problem.

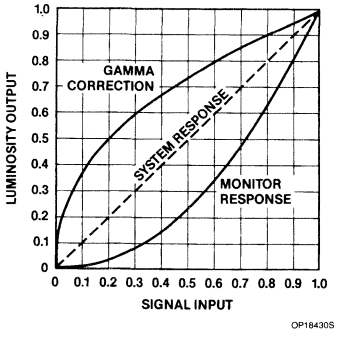


Figure 6. Monitor and System Response With Gamma Correction

In the television industry, correction for this non-linearity takes place at the camera as the image is recorded. The camera takes the 2.2 root of its full-scale fractional value. This cancels the gamma effect and produces a linear system response.

In graphics systems for which the image is generated from digital information, DACs convert the digital information into a voltage that drives the guns of the CRT. Basically, the systems designer has three choices:

1. Correct for gamma in the software. This can be done by using the 2.2 power/root compensation to pixel values before they are stored into the frame buffer. This could be an expensive addition to the software and might slow the overall system because of the added computation time.
2. Apply analog gamma correction in the hardware. The correction factor could be done with additional circuitry to the output of the DAC before it drives the monitor. As mentioned before, this presents an additional hardware overhead. This is not done, however, without some risks. Since every monitor has individual characteristics, the resulting correction would not look the same on every monitor.
3. Ignore the whole subject and accept the non-linearity of the luminous output as a characteristic of the system. Since most graphics applications are for the generation of images for specific problems and not for the lifelike reproduction of scenes (although it would be desirable), a gamma correction mechanism is unnecessary.

This last approach seems to be the most prevalent solution since few, if any, DACs contain gamma correction circuitry. When graphics software designers select their colors, they do so for the best visual performance. This fine-tuning for colors and shading is really software gamma correction because they can select the digital information needed for colors and intensity and see the results from the other side of the monitor.

CIRCUIT FEATURES AND OPERATION

This section covers the basic features and operation of the NE5150/51/52. The first two sections briefly discuss RS-170 and RS-343A, the standards for color and monochrome video systems. The next section covers the composite video signal (CVS) that is specified in the two previous standards.

RS-343A and RS-170

RS-170, the Electrical Performance Standards for Monochrome Television Studio Facilities, and RS-343A, the Electrical Performance Standards for High Resolution Monochrome Closed Circuit Television Cameras, were issued in November 1957 and September 1969, respectively, by the EIA (Electronic Industries Association). The specifications outlined in RS-343A determine the voltage levels required for the part.

Composite Video Signal

Shown in Figure 7 is a section of a composite video signal. With the exception of the BRIGHT function, the levels and tolerances are specified by RS-343A.

Sync, Blank, and Setup

The sync signal is situated 286mV (40 IRE) below the blanking level which lies 714mV (100 IRE) below the reference white level (next section). The sync signal synchronizes the monitor horizontal and vertical scanning. This, and the rest of the composite video signal, is not to be confused with the composite sync signal which is often used for a combined horizontal *and* vertical sync signal.

The blank level lies just below the reference black level, separated by an amount known as the setup. The difference between reference white and the blanking level is defined as 100 IRE. Applying the blanking level voltage to the monitor input will reduce the CRT electron beam current so that there will be no visible trace of the electron gun on the phosphor.

For television, the setup is defined as the *ratio* between the reference white and the reference black level measured from the blanking level. It is usually expressed as a percentage. Basically, it's the difference between the reference black level and the composite blanking level. RS-343A has set the limits of the setup as 7.5 ±5 IRE. Any value between 2.5 to 12.5% of the blanked picture signal can be designated as the setup (2.5 – 12.5 IRE or 17.85 – 89.25mV). Since the full-scale range of the video signal represents 100 IRE, a percentage of the signal is synonymous with its IRE value. For the NE5150, the setup is 71mV or 10 IRE.

Reference Black and White

Reference black and white correspond to the signal levels for a maximum limit of black and white peaks. White corresponds to having all color guns on and black to having all guns off. The gray scale, which refers to the rest of the color values and contains a majority of the signal information, is defined by the amplitude between reference white and reference black. Since the reference white to blanking level is fixed at 100 IRE, the reference black level is determined by the setup. Since the setup can be between 2.5 and 12.5 IRE, the gray scale range must reflect those tolerances and so has a range of 92.5 ±5 IRE (660.5mV ±35.7mV).

To allow for a BRIGHT function, the NE5150/51/52 family of video DACs were designed for a full-scale range (blank to reference white) of 675mV (about 94 IRE) and a gray-scale range of 643mV (about 90 IRE). Using the BRIGHT function adds 71mV (10 IRE) to the reference white value.

For instance, in a 12-bit system like the NE5150/51/52, using 4 bits/DAC would enable us to resolve the gray scale range into 16 parts. For the NE5150, that would be about 40.1mV (5.6 IRE) = 1 LSB. For 6 bits, 64 parts could be resolved, and for 8 bits, 256 parts.

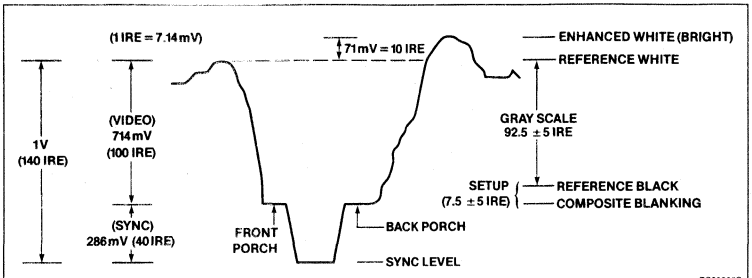


Figure 7. RS-343A Video and Sync Levels

NE5150/NE5151/NE5152 LOGIC TABLE

SYNC	BLANK	WHITE	BRIGHT	DATA	ADDRESS	OUTPUT[3]	CONDITION
1	X	X	0	X	X	−1031mV	SYNC[1]
1	X	X	1	X	X	−960mV	Enhanced SYNC[1]
0	1	X	0	X	X	−746mV	BLANK
0	1	X	1	X	X	−674mV	Enhanced BLANK
0	0	1	0	X	X	−71mV	WHITE
0	0	1	1	X	X	0mV	Enhanced WHITE
0	0	0	0	[0000]	Note 2	−674mV	BLACK (FS)
0	0	0	1	[0000]	Note 2	−603mV	Enhanced BLACK (EFS)
0	0	0	0	[1111]	Note 2	−71mV	WHITE (ZS)
0	0	0	1	[1111]	Note 2	0mV	Enhanced WHITE (EZS)

NOTES:
1. Green channel output only. RED and BLUE will output BLANK or ENHANCED BLANK (BRIGHT ON) under these conditions.
2. For the NE5150/5152, the DATA column represents the memory data accessed by the specific address. For the NE5151, the DATA is the direct digital inputs.
3. Note output voltages in Logic Table are referenced to V_{CC} for the NE5152 only.

Device Description and Operation

Corresponding to the RS-343A requirements outlined in the previous section, the logic table indicates the output voltages given the digital inputs shown. Although the output voltages for the DACs are shown, the user should also know what is happening to the circuit and how the priority given to each function influences the output. [All ones (1111) is called zero-scale (ZS) and all zeroes (0000) is called full-scale (FS).]

The BLANK command presets all the latches to all zeroes (0000) and sends the output to its blanking level of 100 ± 5 IRE below reference white (−71mV) or about −746mV. When BRIGHT is on (a '1'), the output is raised 10 IRE (71mV or 1/9th of full-scale) to −674mV. BLANK overrides WHITE and is overridden by SYNC.

The WHITE command presets the latches to all ones (1111) and outputs −71mV to all DACs. When the BRIGHT command is on, this value is raised to 0V. WHITE will be overridden by both SYNC and BLANK.

The SYNC command presets all of the latches to zeroes and turns on the BLANK switch. In addition, it turns on a 40 IRE switch (drops voltage 286mV) in the GREEN channel only. So the GREEN channel sits at 140 IRE down and the RED and BLUE channels will be 100 IRE below ground.

The BRIGHT command turns off one current switch within the circuit and adds 10 IRE (71mV) to the output levels of all three guns. This comes in handy if using a cursor (optional blinking) to brighten other parts of the screen. This switch cannot be overridden by any other switch.

Referring to the pinouts of both the NE5150/52 and the NE5151 (see Figure 8), there are additional considerations.

The $\overline{WRITE}_G$, $\overline{WRITE}_R$, and $\overline{WRITE}_B$ pins are the write enable pins for each of the 16 × 4 memories in the CLUT. When these pins are pulled High, the memory is then in the READ mode. This is the normal mode of operation. To write to the memory, **one** of the pins must be pulled Low. The data on D0 – D3 will then be written to the memory location A0 – A3 of the corresponding WRITE pin.

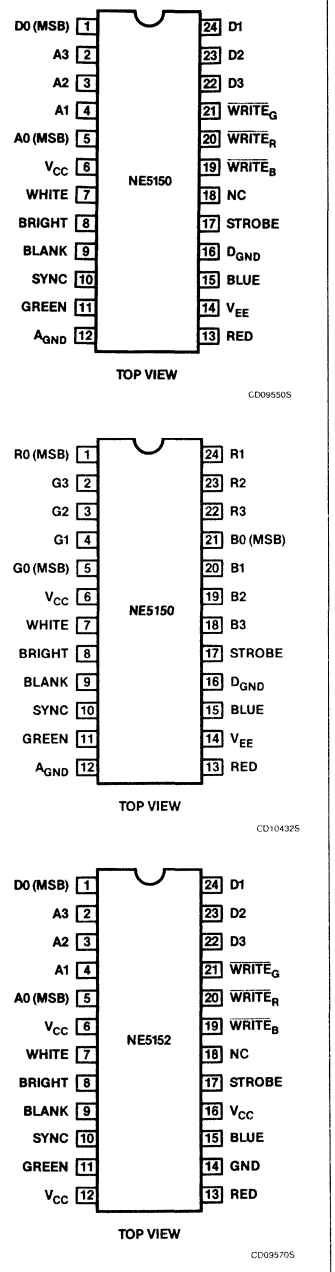


Figure 8. Pinouts of NE5150/52 and NE5151

STROBE is the main system clock and synchronizes all digital operations on the DAC.

The strobe is ECL and TTL compatible and demands no special drive requirements. The positive edge of STROBE clocks the latches.

The GREEN, RED, and BLUE pins are the analog outputs of the DACs. The DACs are voltage output and need no external components (75Ω resistors are on-chip). The output voltage range is approximately 0 to −1V and is independent of the input logic (either TTL or ECL).

The DATA and ADDRESS bits are designated so that D0 and A0 represent the most significant data and address bits (MSB), respectively. Similarly, D3 and A3 correspond to the least significant data and address bits (LSB). Since the NE5151 has no CLUT, there is no need for the address pins (4) or the write enable pins (3). Adding the NC (no connection) pin (1) gives the eight additional input pins for two 4-bit DACs. The original data bus now carries the logic for the RED gun.

Analog and digital ground (A_{GND} and D_{GND}) should always be connected together in any configuration and should not have more than 50mV of potential between them to insure proper operation of the device. The next section will cover connection of V_{CC} and V_{EE}, in addition to A_{GND} and D_{GND}, on different system configurations.

Using Different Logic and Supply Voltages

Different users have different needs. Some have access to dual supplies, other only to single-ended supplies. Signal logic may be TTL or ECL. In any case or configuration, the NE5150/51/52 family can be used. The following configurations cover most cases.

Explanation of the configurations are as follows:

A. Case A shows a basic ECL configuration for the NE5150 and NE5151. The signal voltage is basic ECL with a −1.3V threshold and is powered from ground and −5V (or −5.2V). Since the TTL buffers are no longer needed, V_{CC} is tied to analog and digital ground (A_{GND} and D_{GND}), excluding the buffers from the circuit.

B. In some cases, people use ECL logic but run it off a single supply, +5V and ground. In this case, operation is the same except that the supplies are shifted up 5V. In this new ECL mode, the threshold −1.3V is moved up by 5V to +3.7V. ECL operation is not available for the NE5152.

C. For TTL operation in the NE5150 and NE5151, dual supplies are normally needed. If available, standard TTL-level signals with a +1.4V threshold (between a logic '1' Low of 2.0V and a logic '0' High of 0.8V) can be connected directly.

D. In some situations, a dual supply is not available. Single-supply TTL operation is made possible by making similar connections and by pulling up the inputs of each pin with a 10kΩ resistor connected to V_{CC} = +5V. This is necessary because the threshold is now 3.7V.

E. Case (D) necessitated the construction of the NE5152, which has only one mode using a single 5V supply and accepts TTL inputs. A_{GND} and D_{GND} become V_{CCA} and V_{CCD} and are tied to V_{CC}.

In some cases, a single supply is used and the internal ECL mode has been shifted up to the positive supply; the output voltage will be swinging from 0V to −1V, but, referenced from V_{CC} = +5V, it will swing from 5V to 4V. If the monitor accepts only positive sync pulses or video information, DC-offsetting the outputs or AC-coupling them with 1μF capacitors would make the signal acceptable to the monitor.

Since the outputs have internal 75Ω resistors, the monitor should have a 75Ω resistor to ground in order to doubly-terminate the cable and to prevent reflections.

Unused Inputs

For ECL mode (NE5150), any unused inputs, regardless of desired permanent stage, should be tied to a fixed-level output of an unused gate.

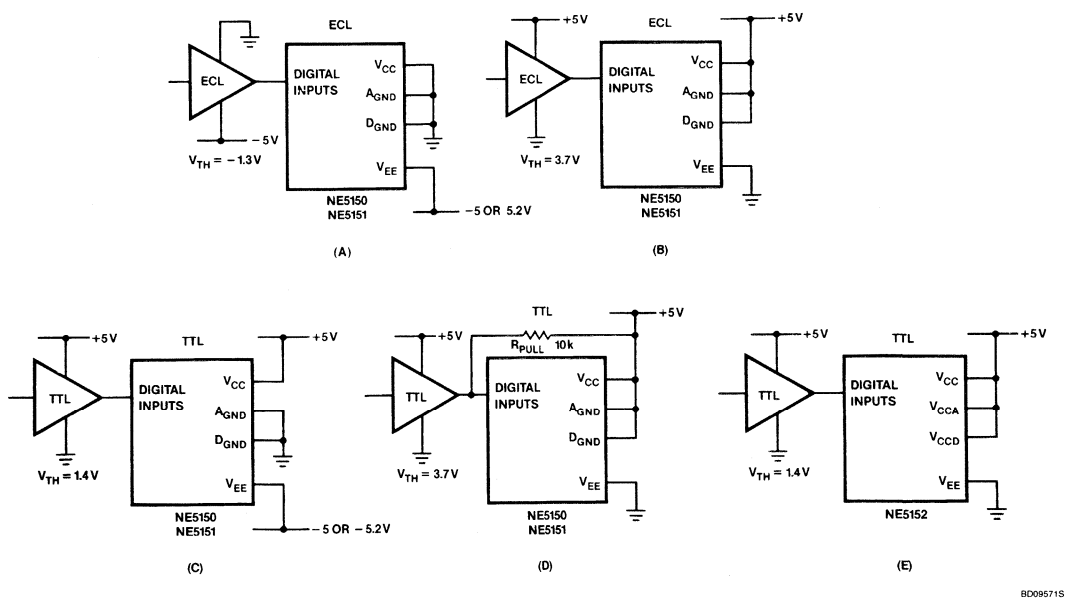


Figure 9. Video DAC Modes of Operation

BLOCK DIAGRAMS

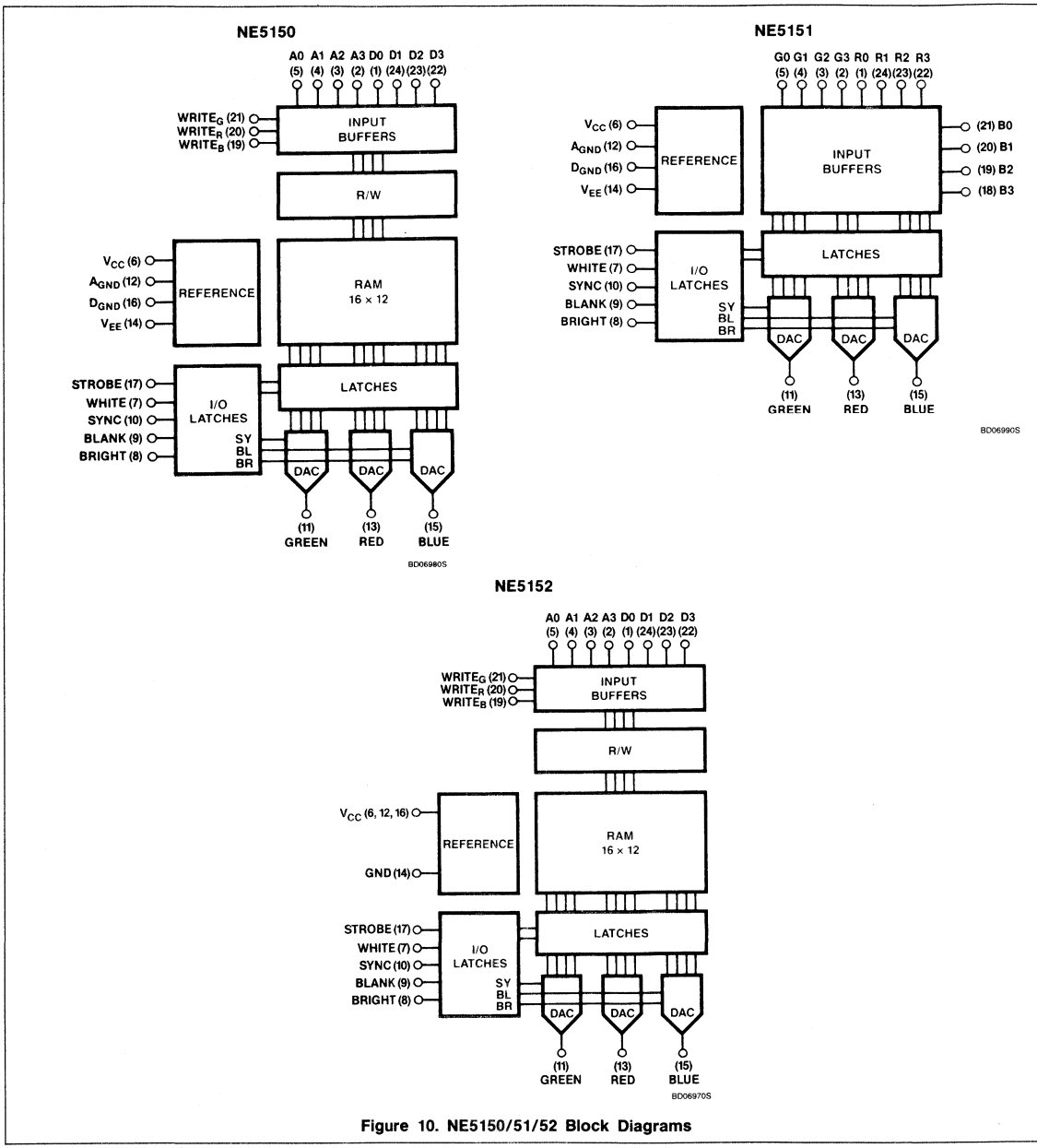


Figure 10. NE5150/51/52 Block Diagrams

Circuit Description

As can be seen from the block diagrams in Figure 13, the only difference between the NE5150/52 and the NE5151 is the lack of a color look-up table on the NE5151. Bypassing the CLUT with its assorted address decoding, sense amplifiers, and read/write logic enables it to not only use 200mW less power, but also to increase its update rate to 150MHz.

The NE5151 is basically the same die as the NE5150/52, with the exception of a metal mask option that permits it to bypass all of the circuitry associated with the CLUT. It is also bonded differently to enable all 12 bits to be loaded into the DAC at any one time instead of being multiplexed 4 bits at a time to the NE5150/52 CLUT.

DAC Reference

The need for separate references for the DACs resulted from the problems associated with glitching and crosstalk between the DACs. When one DAC maintains a constant value through pixel updates, while another undergoes major transitions such as the 1111 to 0000 on/off switching of currents through the DAC, feedthrough can be expected if all 3 DACs derive their reference voltage from the same source. Having separate references solves this problem. It also isolates the DACs from each other and the other parts of the circuit.

The reasons for choosing the DAC shown in Figure 12 are its simplicity, the bandgap's insensitivity to temperature variations, and its excellent supply rejection (PSRR) through high frequencies. It consists of a PTAT current source supplying a bandgap reference. The output of the bandgap is approximately −1.2V.

To provide the bias for the different current sources on each of the DAC stages, the circuit uses a control amplifier that provides negative feedback to maintain its stability. BIT and its complement drive the differential pair that (along with QS2) makes up one part of the DAC. The bandgap drives the current sources through the control amplifier. If the bias line voltage should rise or fall, the negative feedback in the QS1 and QS3 current path would correct for it.

The control amplifier consists of a transconductance stage driving an emitter-follower. The output of the emitter-follower provides a low-output impedance line that drives QS4. The inclusion of QS4 prevents switching transients from degrading settling time. The control amplifier has a 60MHz unity-gain bandwidth, providing power supply rejection up into the VHF range.

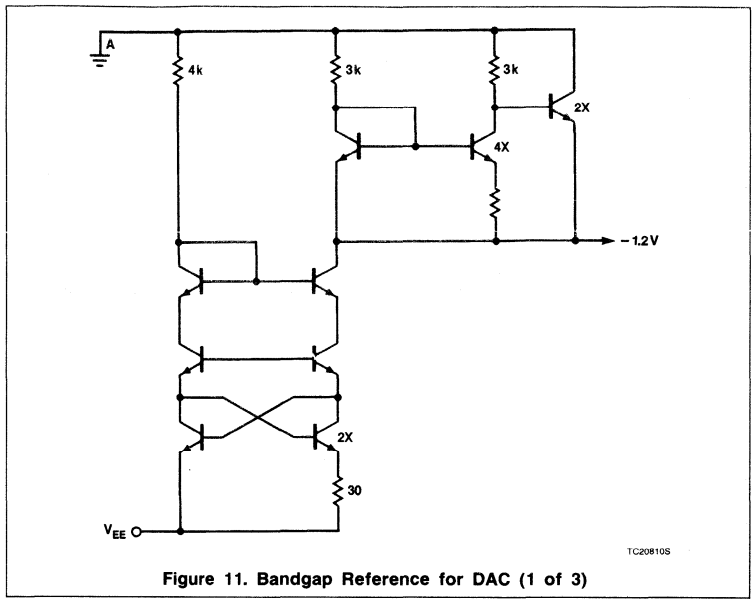


Figure 11. Bandgap Reference for DAC (1 of 3)

Digital-to-Analog Converters

The three DACs consist of differential pairs that are switched on or off depending on the value of the bits. Each of the transistors switches a different amount of current depending on the significance of each bit (see Figure 13). Although only one transistor is shown for each bit, the circuit actually has several transistors in parallel to get the required current. In this case, B3 is the least significant bit since it switches the least amount of current and would produce the smallest voltage drop across the 75Ω load resistor. The reverse is true for B0, the most significant bit, since it draws the most current.

So for all bits low, 0000, all of the current would go through the load resistor, bringing the output voltage to its lowest point. If all three DACs are low, this would correspond to reference BLACK. All bits high, or 1111, shunt current away from the load and leave the output voltage at reference WHITE. Different combinations of bits give 16 values between WHITE and BLACK. One additional 2mA switch is turned on by the input value of BRIGHT, which level-shifts the output by 1/9th the full-scale value, or about 10%. The BLANK and SYNC pins work in a similar manner. Refer to the Logic Table beside Figure 8 for the output voltages for each of these functions.

Some of the problems associated with DACs can be attributed to switching glitches, usually measured in terms of glitch energy. Glitching occurs when digital switching of the transistors causes spikes onto the collectors of the current sources to each of the differential pairs. These current spikes charge the collector-base capacitance, C_{JC}, of the collector transistor, and result in a slower settling time. The asymmetrical turn-on/off behavior of bipolar transistors and mismatched load bit-wiring capacitances also contribute to glitches. This can also be seen as an overshoot of the waveform, a "glitch" on the rising or falling edge of what should look like a square wave. Signals that overshoot the desired analog output level consequently take longer to settle to their final value. The measure of this overshoot is the glitch energy, usually given in pV-sec. The units do not actually work out as units of energy or Joules, which is C-V (Coulomb-Volts), but result from measuring the area of the glitch [Area = Height (V) × Width (psec)].

The NE5150/51/52 resolves this problem by putting the current sources in series with another set of transistors (see Figure 14). The stage below the differential pair is then biased by a low-impedance line which reduces the effect of the current spiking. The biasing for the lower transistor comes from the control amplifier mentioned in the DAC Reference Section.

Video DAC Timing

For the NE5150 and NE5152, the presence of the memory dictates both a READ and a WRITE cycle, whereas the NE5151 needs only one diagram. The explanation of each of the waveforms can be found in the timing glossary. For the guaranteed specifications, the user is referred to the data sheet.

NE5150/52 (With CLUT)
In the NE5150/52 READ cycle, the COMPOSITE signal refers to either the WHITE, BRIGHT, BLANK, or SYNC signals. The read composite hold time, t_{RCH}, is defined from the rising edge of the strobe to the end of the composite pulse. This is the required time the composite signal must remain on the bus for latching. The time between the end of the composite pulse to the next rising edge of the strobe defines the read composite setup time, t_{RCS}. This is the same as the read address setup time, t_{RAS}. The read DAC delay time, t_{RDD}, is the propagation time of the signal through the device clocked from the strobe to the 50% change of the DAC output.

In the WRITE cycle, t_{WAS}, the write address setup time is defined by the start of address to the falling edge of the write enable strobe. At the end of this time, data can be written to the CLUT. Both ADDRESS and DATA must remain latched until they reach the rising edge of the WRITE ENABLE. This defines the WRITE ENABLE pulse width, t_{WEW}. The data should also be latched at the same time as the address. The start of the data (and address) to the end of the write enable pulse is defined as t_{WDS}, or the write data setup time. After the write pulse finishes, an address and data hold time is also specified.

NE5151 (No CLUT)
Since the NE5151 has no memory for the signal to propagate through, it typically has a faster conversion time. As can be seen from the pinouts, the three 4-bit words enter the DAC simultaneously as opposed to the sequential 4-bit loading scheme used in the NE5150/52. With no memory, there's no need for READ or WRITE cycles and so there is only one standard timing diagram. (See Figure 16).

This timing diagram is similar to the READ cycle of the NE5150/52 with the exception that addresses are not clocked to the CLUT; instead, data bits are sent directly to the DACs. In this case, t_{DH} is analogous to the address hold time in the NE5150/52. All other definitions are analogous to the earlier READ case.

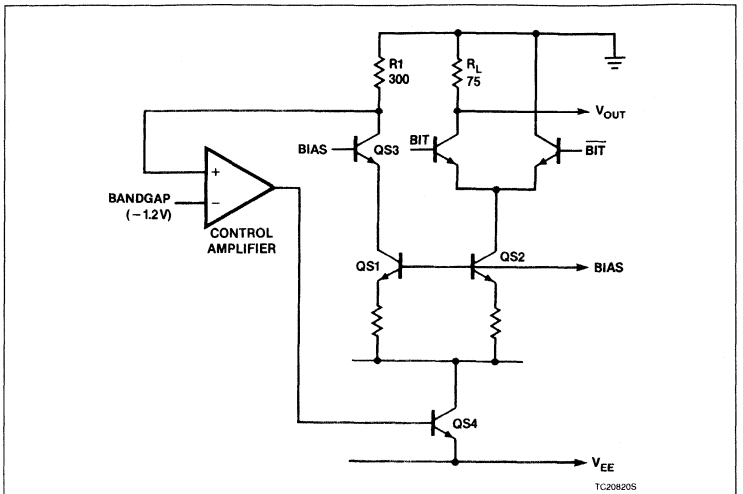


Figure 12. Negative Feedback Referenced to Bandgap

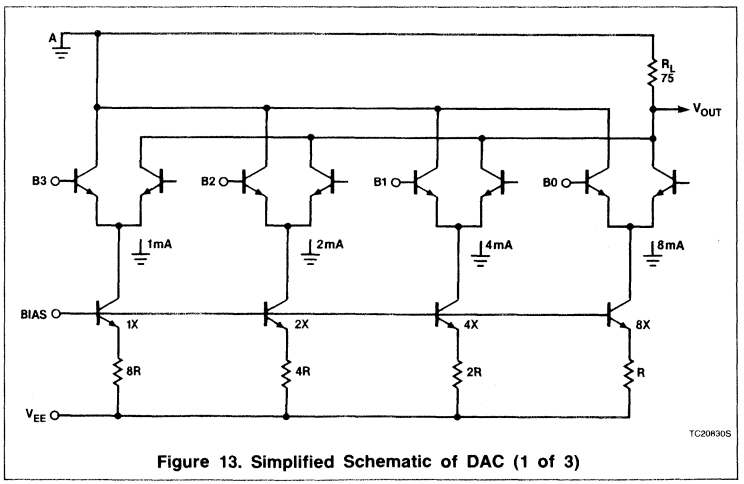


Figure 13. Simplified Schematic of DAC (1 of 3)

WORKSTATION APPLICATION

Introduction

This section describes the design of a color graphics interface for the Modula, Inc. Lilith Workstation. The workstation initially loads 16 colors (it only requires 16) into the NE5150's color look-up table. After the colors are loaded, the workstation then generates addresses to the look-up table. The entire color range (4096) is not required in this application.

The LILITH Workstation
The Lilith Workstation is a 16-bit workstation manufactured by Modula, Inc. It was originally designed by Niklaus Wirth and his students at the Swiss Federal Institute of Technology (ETH). The Lilith is a Modula-2 computing engine. In its original package, the Lilith includes 256kB of memory, a 15MB Winchester disk drive, a floppy disk, a mouse, and an 832 × 640 monochrome graphics tube.

The Signetics Logic Design Group in Orem, Utah, has modified the Lilith by adding 2MB of memory and a high-resolution 1024 × 1024 color monitor. The changes made to the Lilith graphics section comprise the bulk of this application description. Benchmarks of the modified workstation have shown that its performance on applications ranging from matrix multiplications to complete circuit analysis is approximately half as fast as a VAX 11/780 minicomputer. In addition to the circuit simulator used, the Signetics-modified Lilith also supports a layout editor, SLED, that uses about 10,000 lines of Modula-2 source code. More detailed information on the Lilith can be obtained from the manufacturer and from the articles listed in the reference section.

For the purposes of this application, it is sufficient to know that the Lilith contains a 16-bit data bus for interaction with the SCC63484 Advanced CRT Controller and a

14-bit bus that is used to initialize the color look-up table in the NE5150 video DAC. Read/write, I/O lines, CLOCK, data acknowledge, and chip select signals are also sent to the SCC63484 for data and control purposes.

Software Aspects (Pascal and Modula-2) Modula-2 is a superset of Pascal. Anyone with a working knowledge of Pascal should have no trouble programming a Lilith workstation or in understanding the initialization program outlined in this section. Some noteworthy features about Modula-2 and its influence on the architecture of the Lilith (the M-machine) is the fact that the Lilith instruction set (M-code) has only 256 carefully chosen instructions. This limits any instruction to a 1B length and increases the speed of operation. The Modula-2 language constructs map neatly to M-code. There are no excess instructions to add extra baggage. For additional details, the reader is referred to the August 1984 issue of BYTE magazine that contains several good articles on Modula-2.

Considering each '1' as ON and each '0' as OFF, the binary values for each color can be specified for each of the respective guns. Starting from the top, all guns OFF = BLACK. Similarly, all guns ON corresponds to word 7, WHITE. In the software definition module used to load the values, two constants were declared: black = 0 and white = 15. These correspond to the addresses shown in the table and were predefined because of their frequent use. Single guns completely ON give 1, 2, and 4 — the primary colors RED, GREEN, and BLUE, respectively.

System Hardware

The basic system configuration for the color graphics interface is shown below. The Lilith workstation sends data to the SCC63484 and the NE5150. The information sent to the NE5150 is the data for the CLUT initialization. Control signals are sent to the ACRTC. The ACRTC in turn controls the video DAC. The frame buffer sends and receives data (via an address/data buffer stage) to and from the ACRTC for video DAC addressing. The ACRTC also provides horizontal and vertical sync to the CRT while the video DAC supplies the video information. One stage not shown is the address and data buffering for the frame buffer and the pixel stage. This stage, in addition to assorted logic and timing chips, merely facilitates functionality between the major blocks shown in Figure 21.

The host microprocessor, system memory, and DMA control are local to the workstation and will not be described. The horizontal and vertical deflection sections are local to the CRT and will also be omitted. The rest of this section supplies an overall parts list and then describes each of the graphics blocks in somewhat greater detail. Although the actual pin numbers have been omitted, the functionality of each pin is shown for understanding. For actual pinouts and more detailed information, refer to the appropriate data sheet.

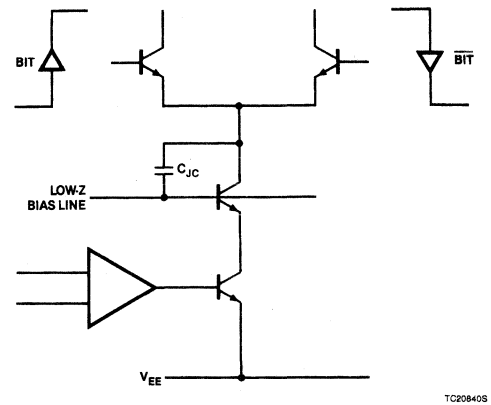


Figure 14. Low-Z Bias Line to Improve Settling Time of DAC

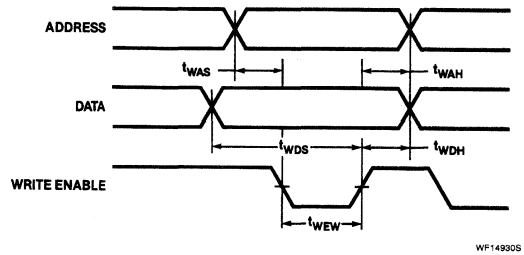


Figure 15. NE5150/52 READ and WRITE Cycle Timing Diagrams

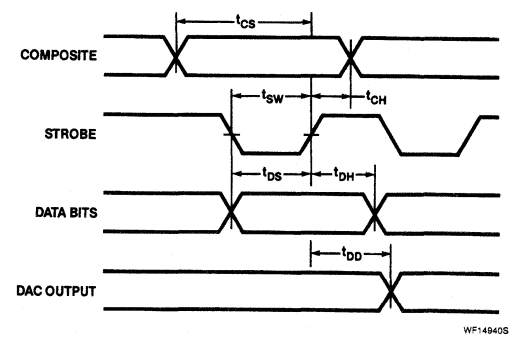


Figure 16. NE5151 Timing Diagram

Parts List

The following parts were used in the design of the color graphics interface (the actual quantity of each part is not listed). The "F" designation stands for Signetics FAST-type logic.

- NE5150 Video DAC
- SCC63484 Advanced CRT Controller
- MB85103-10 64k × 8 Dynamic RAM modules (Fujitsu)
- 7404 Hex Inverter
- 7432 2-Input NAND Gate

- 7474 Dual D-Type Flip-Flop
- 74123 Dual Retriggerable Monostable Multivibrator
- 74138 1-of-8 Decoder/Demultiplexer
- 74F139 Dual 1-of-4 Decoder/Multiplexer
- 74F157 Quad 2-Input Data Selector/ Multiplexer (Non-Inverted)
- 74F161 4-Bit Binary Counter
- 74F164 8-Bit Serial-In/Parallel-Out Shift Register
- 74F166 8-Bit Serial/Parallel-In, Serial-Out Shift Register
- 74F245 Octal Transceiver (3-State)
- 74F373 Octal Transparent Latch
- 7905 5V Voltage Regulator
- M1001 40MHz Crystal (MF Electronics)

PC Board Layout Considerations

Whenever dealing with high-frequency systems, analog or digital, care must be taken with PC board layout in order to insure good, reliable operation. Video DACs are hybrid devices in the sense that they are both analog and digital. They are also run at frequencies well into the RF range. This makes them especially susceptible to RF interference and different types of radiation. Signal traces should be kept as short as possible and 90° turns should be avoided. Power supplies should have adequate decoupling.

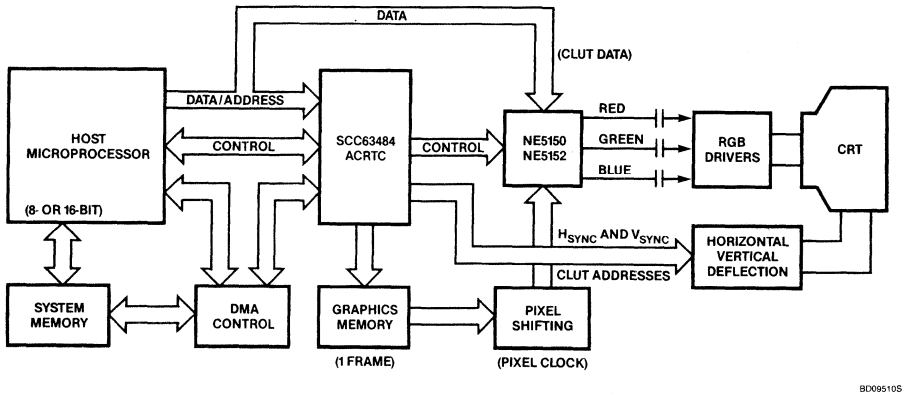


Figure 17. Block Diagram of Color Graphics Interface

More details are provided in the reference section under Reference Number 4, "Getting the Best Performance From Your Video Digital-to-Analog Converter".

Functional Description

The interface is designed to drive a Mitsubishi C-6919 or 6920 19-inch monitor. The monitor has 1024 × 1024 display resolution. Of these, 1024 × 768 pixels are actually drawn, giving us about 790,000 pixels, and, according to our earlier formulas, requiring a DAC with a conversion frequency of about 62MHz. That, however, assumes a non-interlaced display with a frame rate of 60Hz. This application uses a 30Hz interlaced display and so it needs only one-fourth that speed since it is drawing half as many lines at half of the frame rate. The pixel clock is derived from a 40MHz crystal. Other timing signals are also derived from the same crystal.

Table 4. Colors with Corresponding Bit Values

WORD #	COLOR	BLUE	GREEN	RED
0	BLACK	0000	0000	0000
1	RED	0000	0000	1111
2	GREEN	0000	1111	0000
3	YELLOW	0000	1111	1111
4	BLUE	1111	0000	0000
5	VIOLET	1111	0000	1111
6	TURQUOISE	1111	1111	0000
7	WHITE	1111	1111	1111
8	GREY	1010	1010	1010
9	ORANGE	0000	1000	1111
10	AVOCADO	0000	1010	1000
11	LIME	0101	1111	1111
12	NAVY	1111	1000	1000
13	ROUGE	1000	0000	1111
14	LAVENDER	1111	1111	1000
15	PEA	1000	1111	1000

NOTE:
The colors listed are for an application example only. The colors were randomly ordered and their gun and bit values in no way represent the de facto standard values or colors.

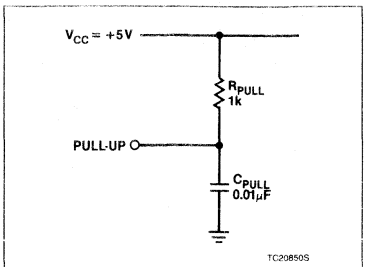


Figure 18. Circuit for Pull-Up to V_{CC}

The interface uses a 512kByte frame buffer that is organized as 64k by 64-bit words. Within each 16-bit block of memory (1 of 4 per word), there are 4 pixels of 4 bits each. Each bit supplies an address to the Color Look-Up Table in the Video DAC. The interface shifts out 64-bits or 16 pixels of information during each display cycle.

In each of the following schematics certain pins have been pulled up to V_{CC}, indicated by an arrow. For each arrow pointing to PULL-UP, the connection goes into the pull-up circuit shown below.

C_{PULL} is used for decoupling any power line ripple. Each point has a similar circuit.

ADVANCED CRT CONTROLLER

The Signetics SCC63484 is a state-of-the-art device ideal for controlling raster-scan-type CRTs. It is a CMOS VLSI system that can control both text and graphics. One of the advantages of this part is its ability to do on-board graphic processing in its Drawing and Display Processor, relieving some of the computational overhead from the Lilith.

Another attractive feature of the part is its flexibility. It has three different operating modes: character only, graphic only, and multiplexed character/graphic mode. In addition, it offers three scanning modes: non-interlace, interlace sync (this application), and interlace sync and video modes. With 2MB of graphic memory and a maximum drawing speed of 2 million pixels/second, it can supply the information to almost any type of high-resolution display (4096 × 4096 pixels maximum).

For additional information on the command set and a full listing of features, please refer to the data sheet and user's manual. This application note will concentrate on only the interconnections relevant to this application.

In this configuration (Figure 19), the SCC63484 Graphics Controller provides the horizontal and vertical sync pulses to the CRT and important timing pulses to the address and data buffers. It supplies timing to the frame buffer, the pixel-shifting stage, and to the frame buffer through direct and logical modifications made to the following system outputs:

1. MRD — Memory Read or the Bus Direction Control Line. This determines the bus direction for the Frame Buffer Data Bus.
2. $\overline{DRAW}$ — the Drawing/Refresh Cycle pin. This differentiates between drawing cycles and CRT display refresh cycles.
3. $\overline{AS}$ — Address Strobe. This provides the address strobe for demultiplexing the frame buffer/data bus (MAD0/MAD15).
4. MCYC — Memory Clock. Provides the frame buffer memory access timing. Equal to one-half the frequency of 2CLK signal.
5. $\overline{DISP1}$ — Display Enable Timing. This is a programmable display enable timing signal used to selectively enable, disable, and blank logical screens.
6. MAD0 – MAD15 — Address and Data Bus. Multiplexed frame buffer address/data bus.
7. MA16, MA17 — Address Bits/Raster Address Outputs. Gives the higher-order address bits for graphic screens and the raster address outputs for character screens. (lower 2 bits of MA16 – MA19).

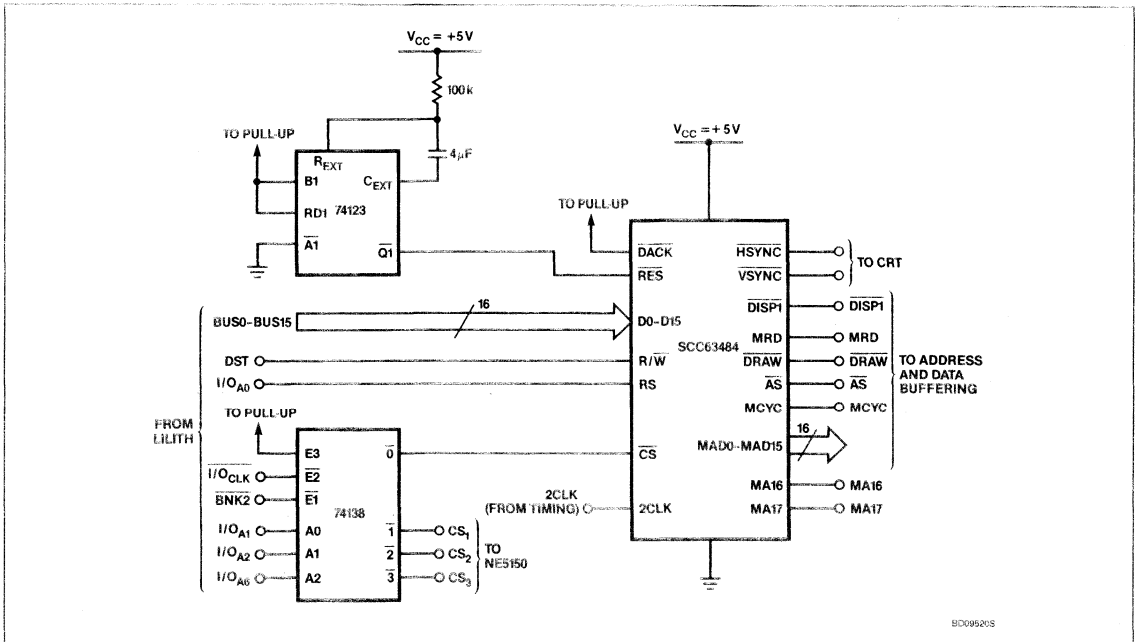


Figure 19. SCC63484 Advanced CRT Controller

The 2CLK signal provides the main clock input to the SCC63484 and is derived from the pixel clock (see System Timing).

The ACRTC also provides horizontal and vertical sync pulses directly to the CRT via the $\overline{HSYNC}$ and $\overline{VSYNC}$ outputs.

In Figure 19, the 16-bit bus of the Lilith is connected directly to the data inputs. The Lilith also provides a write signal (DST) to the R/$\overline{W}$ input. The first I/O line (I/OA0) is connected to the RS (Register Select) input. In addition, there is a high-order I/O bank select, three lower-order address lines, and a negative true I/O clock that, used with the 74138 Decoder, selects one of 4 devices: the ACRTC or 3 areas in the NE5150's color look-up table.

On the ACRTC, a 74123 one-shot produces a reset pulse ($\overline{RES}$) on power-up. The Data Acknowledge pin is not used and is pulled up to V_{CC}.

ADDRESS AND DATA BUFFERING

The address and data buffer stage provides an interface between the SCC63484 and the rest of the circuit. This stage takes the address/data lines MAD0 – MAD15 and separates them into two blocks. The 74F373 latches the upper bank for the addresses; this is the first bank. The second bank consists of 74F245 transceivers in the lower bank for the data.

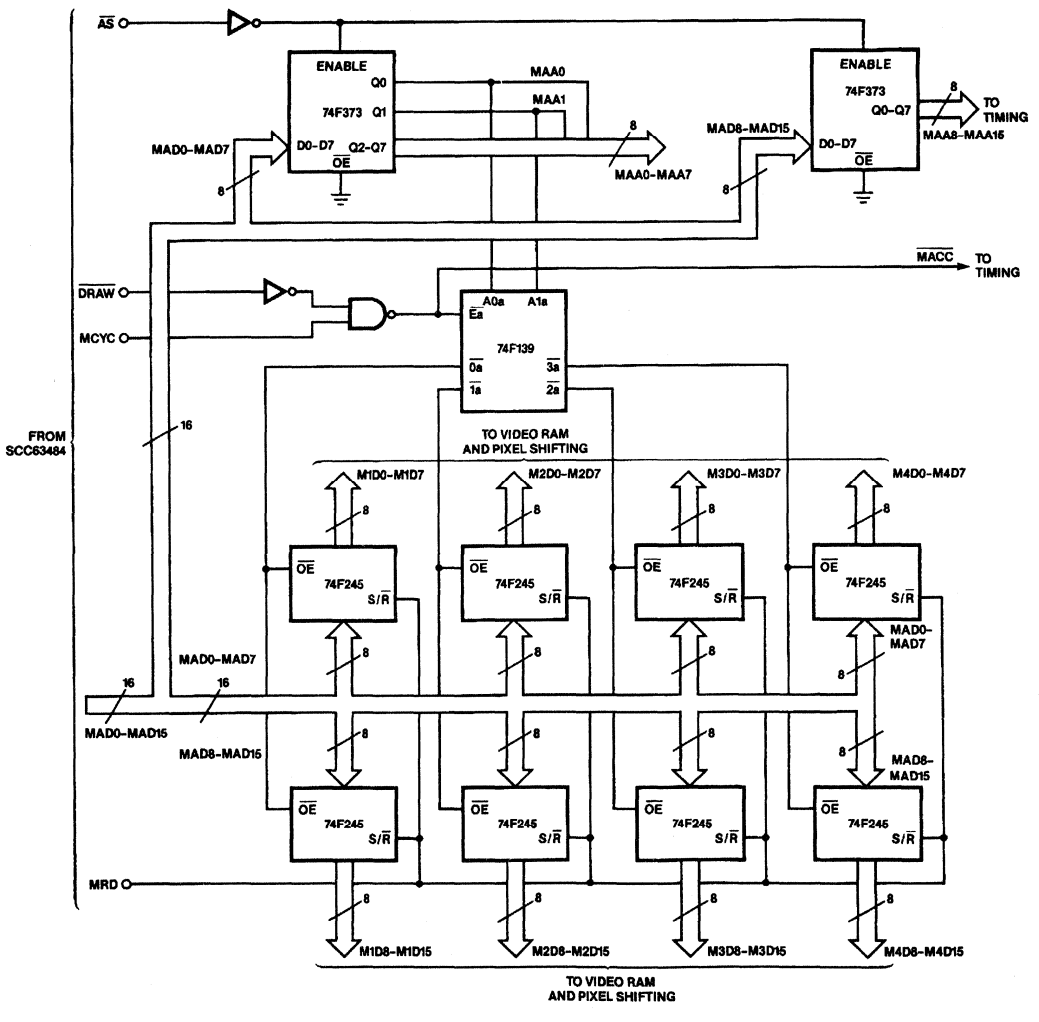


Figure 20. Address and Data Buffering

The 74F373s are used to latch the addresses at the beginning of every memory cycle. The latches are enabled by the $\overline{AS}$ signal coming from the ACRTC. Since the ACRTC is configured to increment its display addresses by four between display cycles, 4 words or 64 bits are shifted out every cycle. For modifying memory cycles, the two lower address lines are used to enable one of four sets of 74F245 transceivers (2 per set). Enabling is performed by the 74F139 Decoder. The signal that clocks the decoder is a combination of MCYC (Memory Cycle) and $\overline{DRAW}$, that results in a new signal, $\overline{MACC}$. This signal is also used in the timing block.

The transceiver outputs are now written into the frame buffer. From there, they will be sent to the pixel-shifting stage and then to the DAC. Each set of four 4-bit pixels in a serial string of displayed pixels is contained in a different block of memory. This is the reason the two lower-order address signals are used to select one of the four banks in the Video RAM (frame buffer).

SYSTEM TIMING

In a system as complicated as a graphics display board, the timing of the various elements grows exceedingly complicated as the number of components grows. It becomes even more apparent when the components are individual systems with their own set of timing considerations. In our case, this means the Lilith, the ACRTC, and the frame buffer.

Figure 21 shows the many elements it takes to generate the timing signals for the system. In the middle of the diagram, there are two 74F164 8-bit serial-in/parallel-out shift registers that count the timing states for the rest of the interface. The Address Strobe ($\overline{AS}$) signal, coming from the ACRTC, starts and ends this timing train. Because of the pulse width of $\overline{AS}$, many states at the end of the train are unusable. The video RAM $\overline{RAS}$ signal (Row Address Strobe) starts at the beginning of State 1, and terminates as $\overline{AS}$ goes Low, activating the register's MR (Master Reset). The precharge requirement of $\overline{RAS}$ is met by the $\overline{AS}$ pulse width.

The 74F157 Multiplexers are connected in such a way that the lower-order addresses are used for the video RAM row addresses (the 157 on top). At the beginning of State 3, the higher-order addresses are presented at the Video RAM address inputs as the column address. At State 5 the $\overline{CAS}$ signal becomes valid. Because of changes in the data hold (WRITE cycle) and data setup (READ cycle) of the ACRTC, the timing edge of $\overline{CAS}$ might have to be changed to insure proper operation.

MRD (Memory Read) along with a combination of MCYC and $\overline{DRAW}$ from the Address and Data Buffer called $\overline{MACC}$, are used with the two lowest-order address lines from the 74F373s (MAA0 and MAA1) to write-select one of the four memory planes (this memory plane runs orthogonal to the bit-planes discussed earlier). Because this signal comes well before the $\overline{CAS}$ signal, this qualifies as an early WRITE cycle, allowing the use of DRAMs with Data-In and Data Out signals connected together.

Using two flip-flops, the output of the lower shift register generates the PE (Parallel Enable) signal for the pixel-shifting stage. Because it is clocked from the fifth point in the shifter, this pulse occurs between States 10 and 11.

The upper left-hand corner of Figure 21 shows the creation of the 2CLK signal derived from the 40MHz pixel clock by using a 74F161 Counter that performs a divide-by-eight operation.

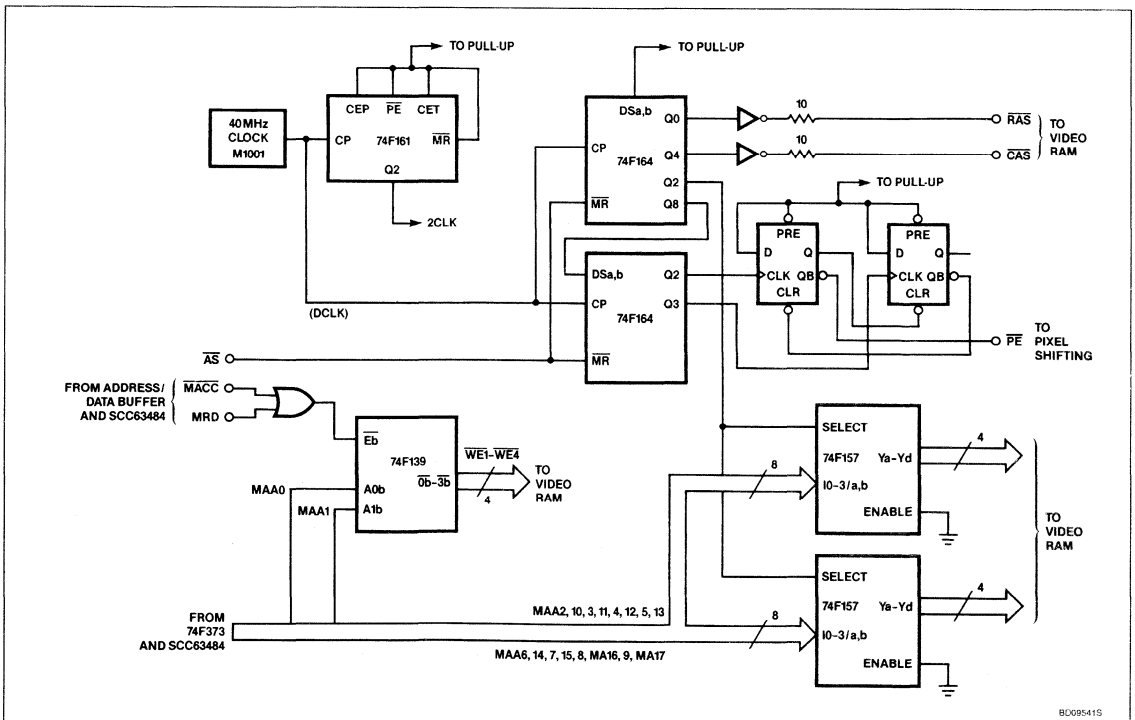


Figure 21. Components for System Timing

PIXEL SHIFTING

The pixel-shifting stage consists of 8 very fast 74F166 Shift Registers divided into 4 banks, one for each address bit. These shift registers have maximum operating frequencies of 120MHz.

The data comes from the address and data buffering and the video RAM. The $\overline{PE}$ (Parallel Enable Input) signal from the system timing block activates the register, while the pixel clock, DCLK, strobes each of the registers. All chips are permanently enabled by grounding their chip enable ($\overline{CE}$) pins. The master reset ($\overline{MR}$) is permanently disabled by tying it to a pull-up.

The connection between the registers and the memory is such that all the bits of each pixel are shifted out simultaneously before going to the 74F157 multiplexer. From there, they address the colors of the CLUT on the Video DAC.

VIDEO RAM

The phrase "Video RAM" refers to a set of dynamic RAMs used as the memory section in this application. It is not meant to be confused with the Video RAM which is a dedicated device for video applications.

The Video RAM or frame buffer section consists of 8 Fujitsu MB85103-10 modules. The 10 suffix signals a 100ns row access time. The cycle time is about 200ns, or about 5MHz. This is fine because only the pixel clock has to travel at the high screen draw speeds. These modules are SIPs (single in-line packages) and were used because of space considerations. Each module consists of eight 64k × 1-bit DRAMs, giving eight modules of 64k × 8 or a 64k × 64 buffer. This buffer is divided into four sections (64k × 16) that represent the four bits of address that are shifted out to the NE5150's CLUT.

One can see how the frame buffer is set up to shift out data to the pixel shifter. The memory is divided into 4 banks that are write-selected by the $\overline{WE1}$ – $\overline{WE4}$ pulses. Two modules (64k × 16 bits) make up one bank. This makes up the four 16-bit words that are shifted out. But where is the information for each pixel? Taking the 1st bank as an example, it can be divided into 4 quadrants:

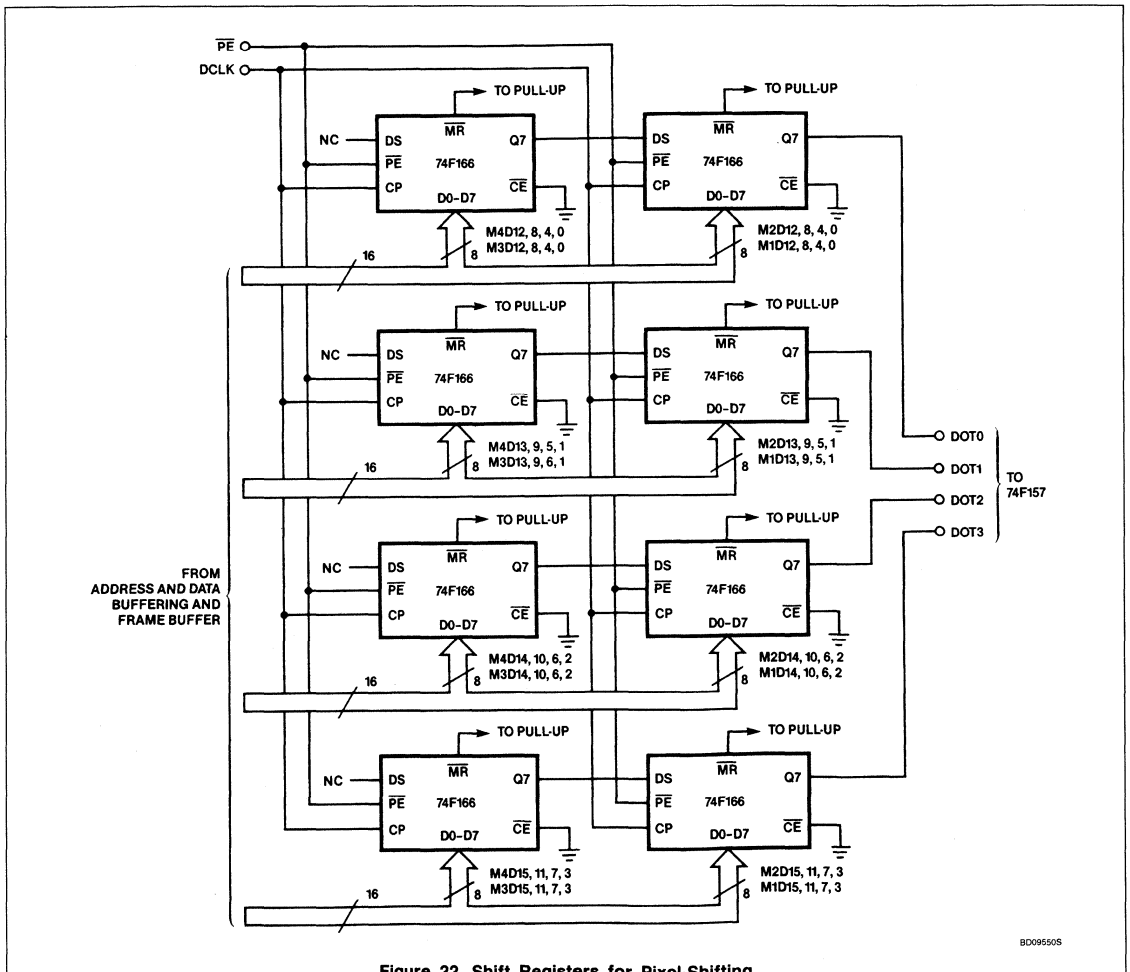


Figure 22. Shift Registers for Pixel-Shifting

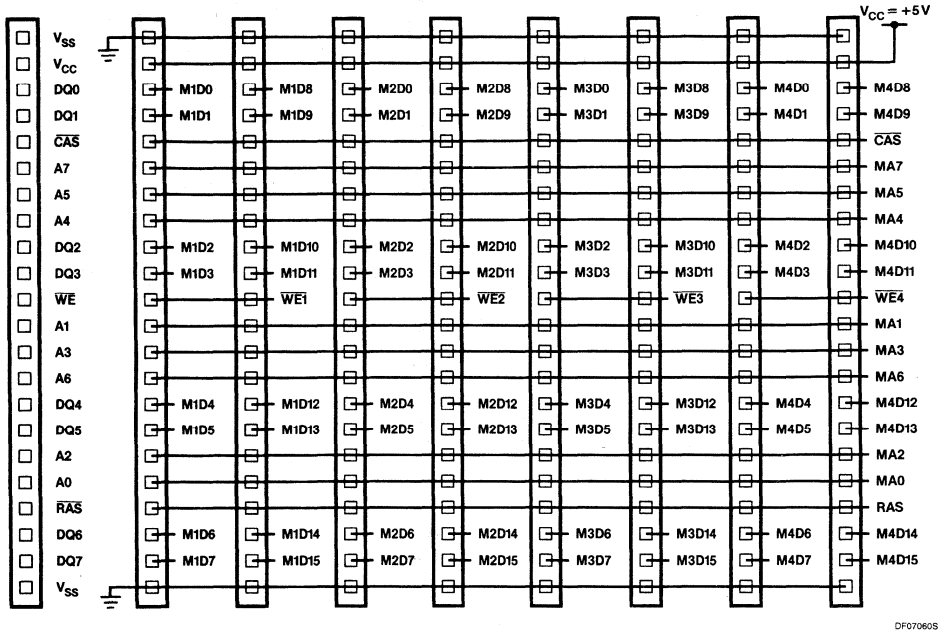


Figure 23. Memory Configuration to Store Pixels

M1D0 – M1D3, M1D4 – M1D7, M1D8 – M1D11, and M1D12 – M1D15. Each of these quadrants represents a dot. By tracking each dot in parallel back to the shift register in the pixel-shifting stage, they turn out to be each of the four quadrants in parallel. Comparing diagrams reveals the same to be true for each of the quadrants in each of the four banks of memory. Each quadrant, then, corresponds to one pixel, and all of the pixels for one bank are written out to the shift register during a write cycle.

VIDEO DAC INTERFACE

The interface to the NE5150 is shown in Figure 24. The 8-bit data bus comes from the lower 8 bits of the Lilith. The low 4 bits are connected directly to the Video DAC data inputs. Bits 4 – 7 are tied to the 74F157 Multiplexer. This provides the address to the CLUT when it is initialized.

The other set of inputs to the multiplexer comes from the pixel-shifting stage. After the first CLUT initialization, all of the addresses come from the pixel-shifter. The inverters, NAND gates, and OR gates are used to delay the write pulses $\overline{WRR}$, $\overline{WRG}$, and $\overline{WRB}$ so that they fit into the address setup window. The chip select pulses come from the 74F138 which are selected by the Lilith. $\overline{I/OCLK}$ clocks the 74138 and the OR gates for the chip select.

DCLK drives the STROBE of the DAC and clocks the two D-type flip-flops which provide the BLANKing signal. Both of these signals come from the ACRTC and the system timing section. The WHITE, BRIGHT, and SYNC inputs are not utilized and are connected to ground. V_{EE} is run off a 7905 voltage regulator powered by a –12V power supply.

The capacitors to the monitor and voltage regulator are polarized with the positive end to the monitor for the RGB outputs and to ground for the regulator. The regulator uses Tantalum capacitors.

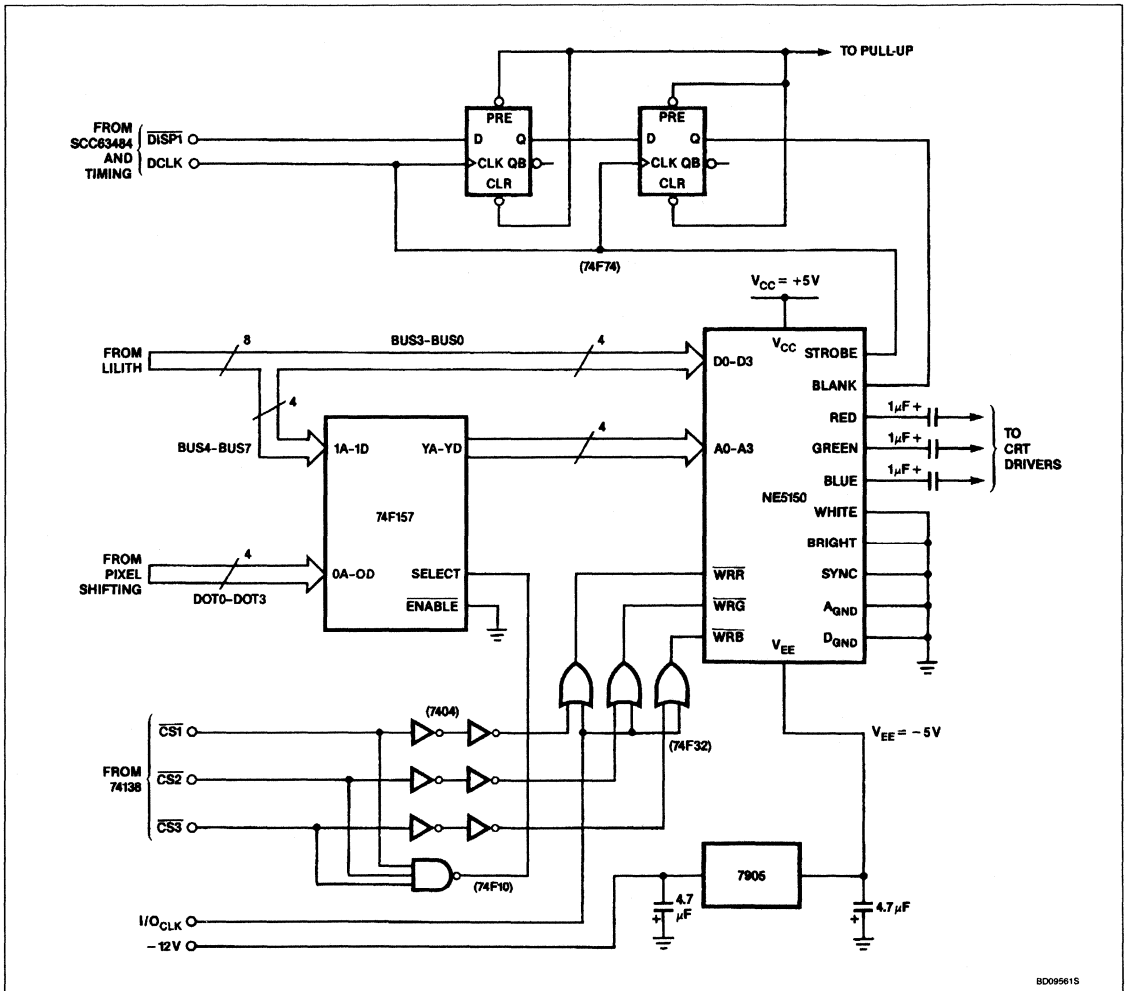


Figure 24. NE5150 Video DAC Interface

NE5150/51/52 Family of Video Digital-to-Analog Converters AN1081

GLOSSARY

This glossary consists of three parts: a section for graphics terminology, one for the timing of the NE5150 used in the Lilith workstation application, and a list of references. For the glossary section, many analogies are made with television to clarify some terminology.

GRAPHICS TERMINOLOGY

ACRTC — Short for Advanced CRT Controller. A device that helps to interface a microprocessor or microcomputer with a monitor. Advanced refers to the Signetics ACRTC, the SCC63484, called advanced because of its ability to do most of its graphics computations on-board, thus relieving some of the workload from the microprocessor and increasing its overall efficiency.

Bit-Map, Bit-Plane — A memory representation in which one or more bits correspond to a pixel. For each bit used in the representation of a pixel, there is a plane on which it can be mapped. To represent each pixel by 4 bits, 4 bit planes are needed. This is the case whether the bits store the actual data for the pixel or hold the address of the memory location containing the data.

Blanking — The process of turning off an electron gun so that it leaves no trace on the screen as it returns to the left or top of the screen in a raster-scan system. Applies to both television sets and monitors. The period for the blanking is defined as the horizontal blanking and the vertical blanking interval for their respective cases.

CRT — Short for Cathode Ray Tube, a type of electron tube that produces an electron beam that strikes the phosphor-coated screen, causing that screen to emit light.

Chrominance — The color information supplied in a signal. While this information has to be extracted by color decoders in television (via phase differencing with a fixed-frequency subcarrier), in computer monitors and bit-mapped systems it is supplied digitally and then converted to analog to directly drive color guns.

Color Look-up Table — Sometimes referred to as the CLUT, it is associated with a Video DAC and speeds system access of often-used colors. The time savings results because a color can be generated by sending a CLUT address to the DAC instead of loading a word from external memory. Current CLUTs range in size from 16 to 256 words. Word length depends on the bit resolution of the DAC.

DAC — Short for Digital-to-Analog Converter. Most DACs have a single output. Some have as many as eight. RGB Video DACs have three — one for each of the primary colors. Video DACs typically operate at very high speeds since they have to supply a new piece of information for each pixel on the screen at rates of 30 to 80 times per second.

ECL — Short for Emitter-Coupled-Logic. A fast, non-saturating form of bipolar logic that usually operates from 0 to −5.2V. It has a threshold of −1.3V.

Frame Buffer — Sometimes used interchangeably with video RAM. A frame buffer is a large, fast-access store of memory that contains the digital information necessary to display part or all of a display. It is used in conjunction with bit-mapped graphic systems. It actually "stores" the bit-plane.

Glitch Energy — The area displaced by an analog signal as it overshoots or undershoots its ideal value. This is a problem usually found in DACs. Units are usually given in pV-s. When glitch energy is high, settling times tend to be longer and may result in visual color aberrations on the screen.

Hue — The actual color(s) on a monitor. The hue depends on the frequency of the light striking the human eye. For television transmission, it is determined by the video signal's phase difference with a color subcarrier reference frequency. For computer graphics systems, it is determined by the combination of binary values applied to the DAC. The resolution of hue/colors is determined by the bit length of each word of information.

Lilith — The brand name of the workstation manufactured by Modulo, Inc. of Provo, UT.

Luminance — The brightness information in a video signal. A black and white (monochrome) monitor displays only variations in brightness. Only a luminance signal is being manipulated. The same holds true for television. Although chrominance information is also present in a television signal, B/W TV sets do not have the necessary decoders.

Modula-2 — A language that is the superset of Pascal. This was also invented by Niklaus Wirth of the Swiss Technological Institute.

NTSC — Short for the National Television Standards Committee, the ruling body for television standards in the United States. Other countries also use this standard as is, or with a different frequency for the color subcarrier.

Orthogonal — Defined as being mutually perpendicular. The product of two orthogonal vectors is zero. In bit-mapped systems, the bit length of a word lies orthogonal to the plane itself. Hence, each plane supplies only one bit of information for each pixel.

Pixel — Short for "picture element". The smallest resolvable element on a graphics display. Each pixel usually corresponds to at least one bit. The entire display is made up of a map of pixels. The term bit-map comes from the bit association. There is no equivalent in television. What is seen is the true analog representation of what is being recorded by a camera and then retraced on horizontal lines.

Raster-Scan — The form of visual display transmission used in all television sets and in most monitors. It consists of an electron beam tracing a path from left-to-right while going top-to-bottom.

Saturation — The "deepness" of a color. Usually depends on the amplitude of the color signal in television systems. Red and pink are the same hue, but red is actually more saturated than pink. In graphics systems, there is no true equivalent. Changing bit-values changes the color itself. The closest analogy would be to raise or lower the voltages on all three color guns simultaneously (the BRIGHT function on the NE5150/51/52). This would, however, depending on the amplitude change, give the impression of brightening or dimming the color (changing luminance) rather than saturating it.

Sync — The voltage level specified in RS-343A as being 140 IRE (1V) below the enhanced white level (ground). It is also 40 IRE (286mV) below the blanking level. Generically it is also used to refer to vertical and horizontal sync pulses that synchronize the timing and movement of the electron beam on a CRT. It should not be confused with "composite sync".

Teletext — A form of data transmission via television signals. In many cases, digital information is sent during the vertical blanking interval (VBI). In some cases, it is sent during every retrace. This is known as full-field teletext.

TTL — Short for Transistor-Transistor Logic. It has a threshold voltage of approximately 1.4V and is the most widely-used form of logic in the world today.

DEFINITIONS FOR NE5150/51/52 TIMING DIAGRAMS

This section contains explanations for the NE5150/51/52 Video DAC's timing diagram specifications. For the typical, minimum, and maximum values, please refer to Signetics' data sheet.

t_{WAS} — Write Address Setup (NE5150/52)

t_{WAH} — Write Address Hold (NE5150/52)

t_{WDS} — Write Data Setup (NE5150/52)

t_{WDH} — Write Data Hold (NE5150/52)

t_{WEW} — Write Enable Pulse Width (NE5150/52)

t_{RCS} — Read Composite Setup (NE5150/52)

t_{RCH} — Read Composite Hold (NE5150/52)

t_{RAS} — Read Address Setup (NE5150/52)

t_{RAH} — Read Address Hold (NE5150/52)

t_{RSW} — Read Strobe Pulse Width (NE5150/52)

t_{RDD} — Read DAC Delay (NE5150/52)

t_{CS} — Composite Setup (NE5151)

t_{CH} — Composite Hold (NE5151)

t_{DS} — Data bits Setup (NE5151)

t_{DH} — Data bits Hold (NE5151)

t_{SW} — Strobe Pulse Width (NE5151)

t_{DD} — DAC Delay (NE5151)

t_R — DAC Rise Time (NE5151)

t_S — DAC Full-Scale Settling Time (NE5151)

REFERENCES

The following books, articles, notes, and correspondences were used in the preparation of this application note.

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2. "Trends in Graphics Hardware", paper by Randall R. Bird, Genisco Computers Corporation; presented at WESCON '85
3. *Basic Television and Video Systems*, 5th edition, by Bernard Grob, McGraw-Hill
4. *Getting the Best Performance from Video Digital-to-Analog Converters*, (AN-1) by Dennis Packard, Brooktree Corporation, San Diego
5. "A Cost-Effective Custom CAD System", paper by R.C. Burton, D.G. Brewer, R.E. Penman, and R. Schilimoeller, Computer Science Department, Brigham Young University and Signetics Corporation
6. "Lilith and Modula-2", by Richard Ohran, *Byte Magazine*, pgs. 181 – 192; August 1984
7. "Monolithic Color Palette Fills in the Picture for High-Speed Graphics", by Steven Sidman and John C. Kuklewicz, *Electronic Design*; November 29, 1984
8. *EIA Standard RS-343A: Electrical Performance Standards for High-Resolution Monochrome Closed-Circuit Television Camera*, by the Video Engineering Department of the Electronic Industries Association; September, 1969
9. "A Single-Chip RGB Digital-to-Analog Converter with High-Speed Color-Map Memory", by W. Mack and M. Horowitz, *Digest of the International Conference on Consumer Electronics*, p. 90; 1985

Comparators

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LM193A	low power dual voltage comparator	609
LM211	voltage comparator	593
LM219	dual voltage comparator	596
LM239	quad voltage comparator	602
LM239A	quad voltage comparator	602
LM293	low power dual voltage comparator	602
LM293A	low power dual voltage comparator	609
LM311	voltage comparator	593
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AU2901
Quad Voltage Comparator

Preliminary Specification

DESCRIPTION

The AU2901 consists of four independent precision voltage comparators, with an offset voltage specification as low as 2.0mV max for each comparator, which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though they are operated from a single power supply voltage.

The AU2901 was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the AU2901 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

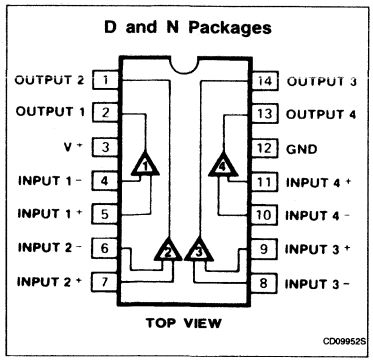
FEATURES

- **Wide single supply voltage range $2.0V_{DC}$ to $36V_{DC}$ or dual supplies $\pm 1.0V_{DC}$ to $\pm 18V_{DC}$**
- **Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at $5.0V_{DC}$)**
- **Low input biasing current 25nA**
- **Low input offset current $\pm$ 5nA and offset voltage**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems**

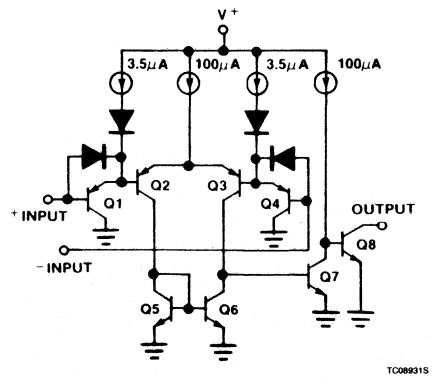
APPLICATIONS

- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATION



EQUIVALENT CIRCUIT



(1 Comparator Only)

Quad Voltage Comparator

AU2901

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	−40°C to +125°C	AU2901D
14-Pin Plastic DIP	−40°C to +125°C	AU2901N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	V_{CC} supply voltage	36 or ±18	V_{DC}
V_{DIFF}	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	−0.3 to +36	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[1] N package D package	 1420 1040	 mW mW
	Output short-circuit to ground[2]	Continuous	
I_{IN}	Input current ($V_{IN} < -0.3V_{DC}$)[3]	50	mA
T_A	Operating temperature range AU2901	 −40 to +125	 °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   N Package at 11.4mW/°C
   D Package at 8.3mW/°C
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$.

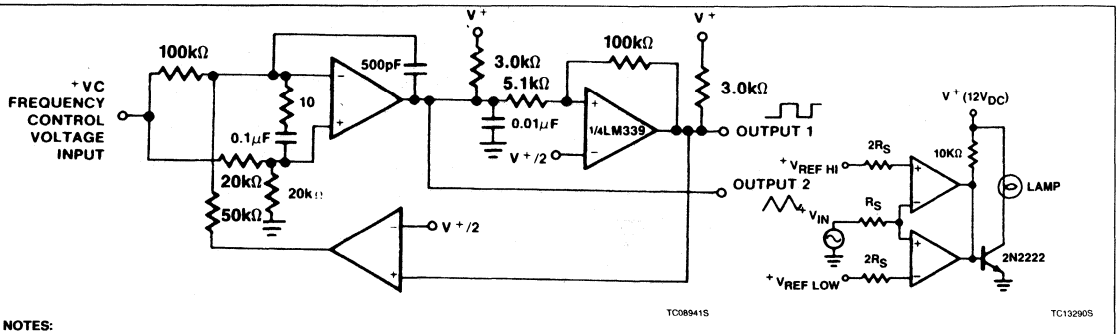
DC AND AC ELECTRICAL CHARACTERISTICS $V+ = 5V_{DC}$, AU2901: $-40°C \leq T_A \leq 125°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	AU2901			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±2.0 ±9	±7.0 ±15	mV
V_{CM}	Input common-mode voltage[3] range	$T_A = 25°C$ Over temp.	0 0		V+−1.5 V+−2.0	V
V_{iDR}	Differential input voltage[1]	Keep all V_{IN}s $\geq 0V_{DC}$ (or V− if need)			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25 200	250 500	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±5 ±50	±50 ±200	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN}(+) = 0$, $V_O \leq 1.5V_{DC}$, $T_A = 25°C$	6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN}(-) = 0$ $V_O = 5V_{DC}$, $T_A = 25°C$ $V_O = 30V_{DC}$, Over temp.		0.1	 1.0	nA μA
I_{CC}	Supply current	$V+ = 28V$, $R_L = \infty$ on comparators, $T_A = 25°C$ $V+ = 30V$		0.8 1.0	2.0 2.5	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15V_{DC}$	25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		 400	 400 700	mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$, $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300		ns
t_R	Response time[5]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3		μs

NOTES:

1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (or $0.3V_{DC}$ below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \cong 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from $5V_{DC}$ to $30V_{DC}$; and over the full input common-mode range ($0V_{DC}$ to V+ − $1.5V_{DC}$).
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to $30V_{DC}$ without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained (see Typical Performance Characteristics section).

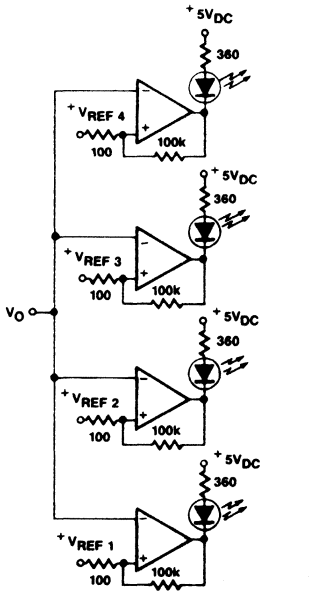
TYPICAL APPLICATIONS



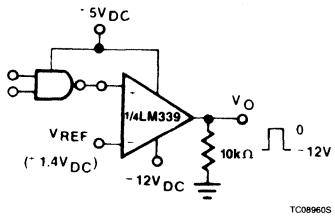
NOTES:
$V+ = +30V_{DC}$
$+250m\ V_{DC} \leq V_C + 50V_{DC}$
$700Hz \leq f_O \leq 100kHz$

Two-Decade High-Frequency VCO

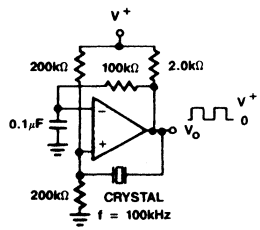
Limit Comparator



Visible Voltage Indicator



TTL-to-MOS Logic Converter

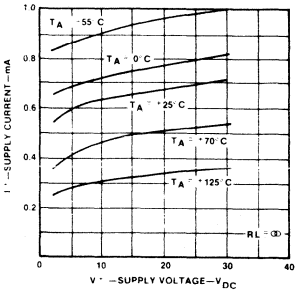


Crystal-Controlled Oscillator

NOTE:
Inputs of unused comparators should be grounded.

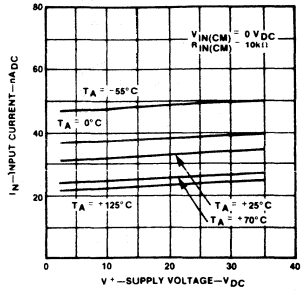
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current



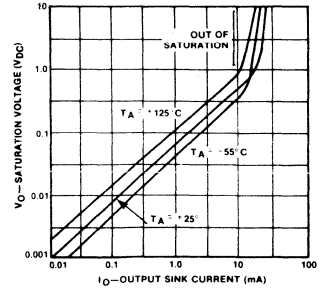
OP05570S

Input Current



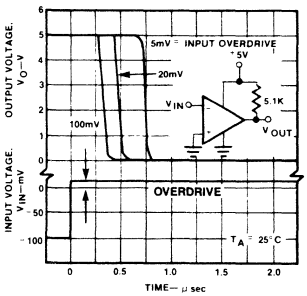
OP05580S

Output Saturation Voltage



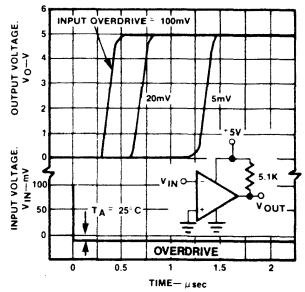
OP05590S

Response Time for Various Input Overdrives — Negative Transition



OP05600S

Response Time for Various Input Overdrives — Positive Transition



OP05610S

AU2903
Low Power Dual Voltage Comparator

Preliminary Specification

DESCRIPTION

The AU2903 consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max. for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

The AU2903 was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the AU2903 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

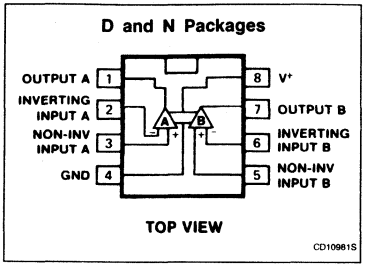
FEATURES

- **Wide single supply voltage range $2.0V_{DC}$ to $36V_{DC}$ or dual supplies $\pm 1.0V_{DC}$, to $\pm 18V_{DC}$**
- **Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/comparator at $5.0V_{DC}$)**
- **Low input biasing current 25nA**
- **Low input offset current $\pm$ 5nA and offset voltage $\pm$ 2mV**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems**

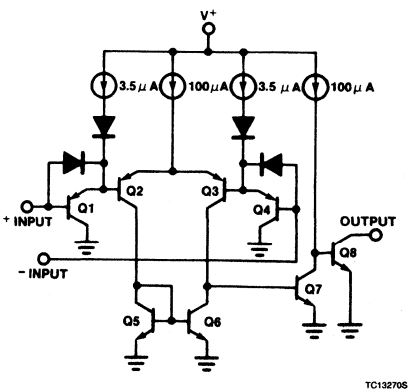
APPLICATIONS

- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATION



EQUIVALENT CIRCUIT



(One Comparator Only)

Low Power Dual Voltage Comparator

AU2903

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	−40°C to +125°C	AU2903D
8-Pin Plastic DIP	−40°C to +125°C	AU2903N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	36 or ±18	V_{DC}
	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	−0.3 to +36	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[3] N package D package	 1160 780	 mW mW
	Output short-circuit to ground[1]	Continuous	
I_{IN}	Input current ($V_{IN} < -0.3V_{DC}$)[2]	50	mA
T_A	Operating temperature range AU2903	 −40 to +125	 °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$.
3. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC AND AC ELECTRICAL CHARACTERISTICS $V+ = 5V_{DC}$, AU2903; $-40°C \leq T_A \leq +125°C$, unless otherwise specified.

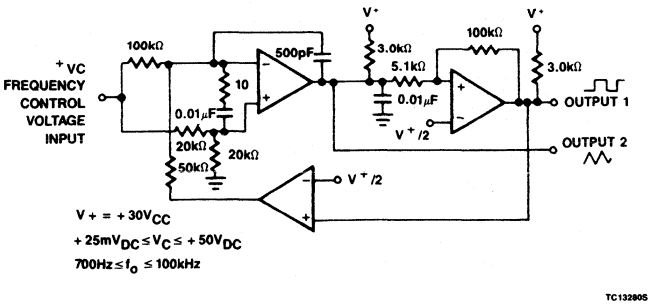
SYMBOL	PARAMETER	TEST CONDITIONS	AU2903			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±2.0 ±9	±7.0 ±15	mV
V_{CM}	Input common-mode voltage range[3, 6]	$T_A = 25°C$ Over temp.	0 0		V+−1.5 V+−2.0	V
V_{IDR}	Differential input voltage[1]	Keep all $V_{INS} \geq 0V_{DC}$ (or V− if need)			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25 200	250 500	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±5 ±50	±50 ±200	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $V_O \leq 1.5V_{DC}$ $T_A = 25°C$	6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN(-)} = 0$ $V_O = 5V_{DC}$, $T_A = 25°C$ $V_O = 30V_{DC}$, over temp.		0.1	 1.0	nA μA
I_{CC}	Supply current	$R_L = \infty$ on both comparators. $T_A = 25°C$ V+ = 30V, over temp.		0.8 1	1 2.5	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15V_{DC}$, $T_A = 25°C$	25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		400	400 700	mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$ $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300		ns
t_R	Response time[5]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$ $T_A = 25°C$		1.3		μs

NOTES:

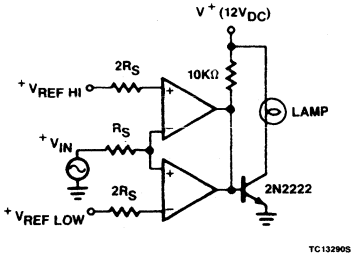
1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (V_{DC} below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \cong 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from $5V_{DC}$ to $30V_{DC}$ and over the full input common-mode range ($0V_{DC}$ to $V+ - 1.5V_{DC}$).
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to $30V_{DC}$ without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive.
6. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

Low Power Dual Voltage Comparator — AU2903

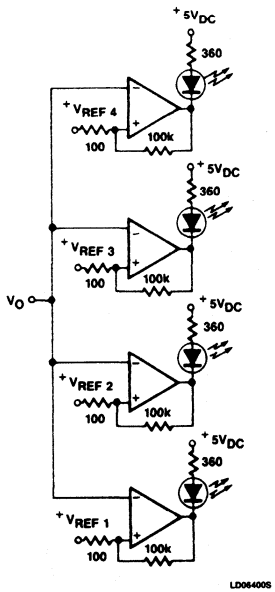
TYPICAL APPLICATIONS



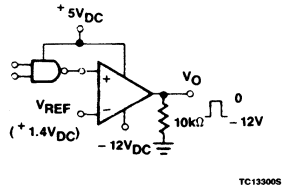
Two-Decade High-Frequency VCO



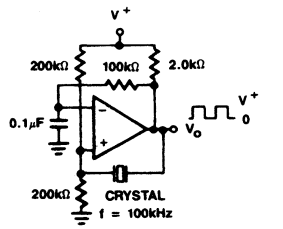
Limit Comparator



Visible Voltage Indicator



TTL-to-MOS Logic Converter



Crystal-Controlled Oscillator

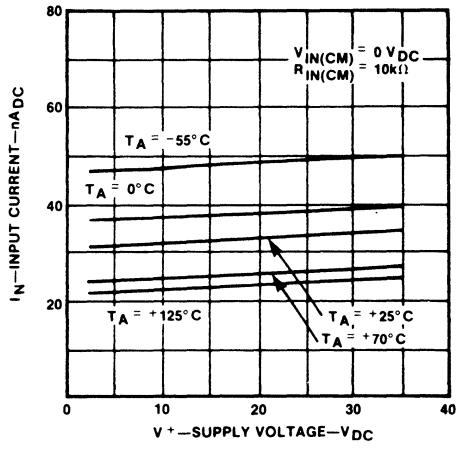
NOTE:
All pins of any unused comparators should be grounded.

Low Power Dual Voltage Comparator

AU2903

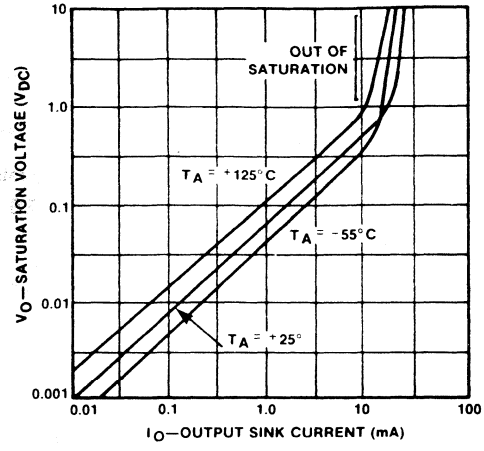
TYPICAL PERFORMANCE CHARACTERISTICS

Input Current



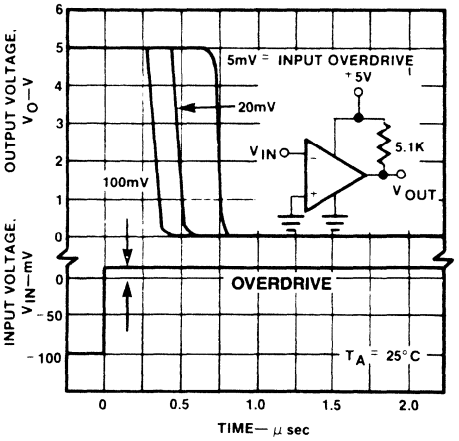
OP05580S

Output Saturation Voltage



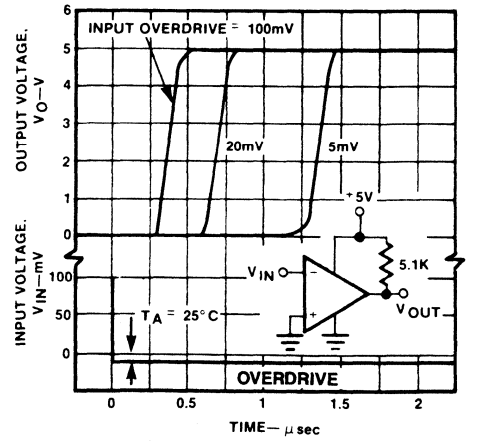
OP05590S

Response Time for Various Input Overdrives — Negative Transition



OP05600S

Response Time for Various Input Overdrives — Positive Transition



OP05610S

LM111/211/311
Voltage Comparator

Product Specification

DESCRIPTION

The LM111 series are voltage comparators that have input currents approximately a hundred times lower than devices like the μA710. They are designed to operate over a wider range of supply voltages; from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL, and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

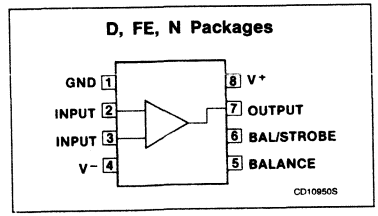
Both the inputs and the outputs of the LM111 series can be isolated from system ground, and the output can drive loads referred to ground, the positive supply, or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire-ORed.

Although slower than the μA710 (200ns response time vs 40ns), the devices are also much less prone to spurious oscillations. The LM111 series has the same pin configuration as the μA710 series.

FEATURES

- **Operates from single 5V supply**
- **Maximum input bias current: 150nA (LM311 — 250nA)**
- **Maximum offset current: 20nA (LM311 — 50nA)**
- **Differential input voltage range: ±30V**
- **Power consumption: 135mW at ±15V**
- **High sensitivity — 200V/mV**

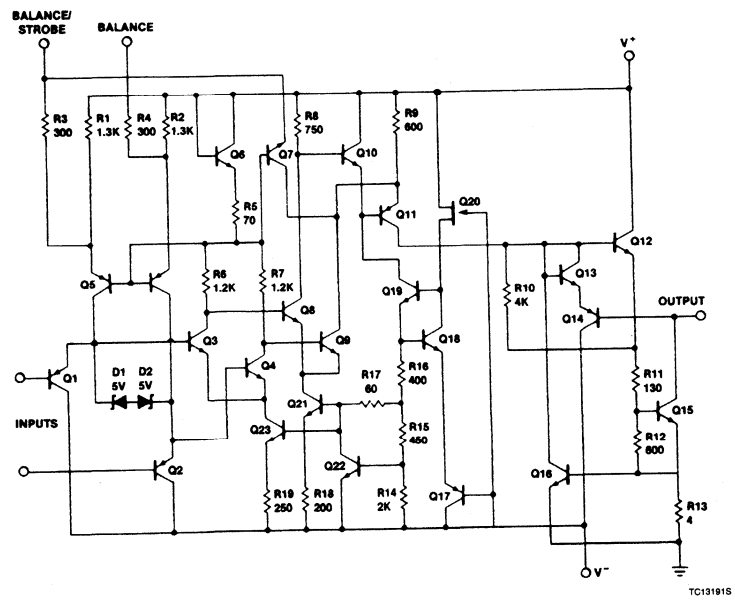
PIN CONFIGURATION



APPLICATIONS

- **Zero crossing detector**
- **Precision squarer**
- **Positive/negative peak detector**
- **Low voltage adjustable reference supply**
- **Switching power amplifier**

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Cerdip	−55°C to +125°C	LM111FE
8-Pin Cerdip	−25°C to +85°C	LM211FE
8-Pin Plastic DIP	−25°C to +85°C	LM211N
8-Pin Plastic SO	0 to +70°C	LM311D
8-Pin Cerdip	0 to +70°C	LM311FE
8-Pin Plastic DIP	0 to +70°C	LM311N
8-Pin Plastic SO	−25°C to +85°C	LM211D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Total supply voltage	36	V
	Output to negative supply voltage: LM111/LM211 LM311	 50 40	 V V
	Ground to negative supply voltage	30	V
	Differential input voltage	±30	V
V_{IN}	Input voltage[1]	±15	V
$P_{D\ MAX}$	Maximum power dissipation, T_A = 25°C (still-air)[1] F package N package D package	 810 1190 780	 mW mW mW
I	Output short-circuit duration	10	sec
T_A	Operating ambient temperature range LM111 LM211 LM311	 −55 to +125 −25 to +85 0 to +70	 °C °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 6.4mW/°C
   N package at 9.5mW/°C
   D package at 6.2m/W°C

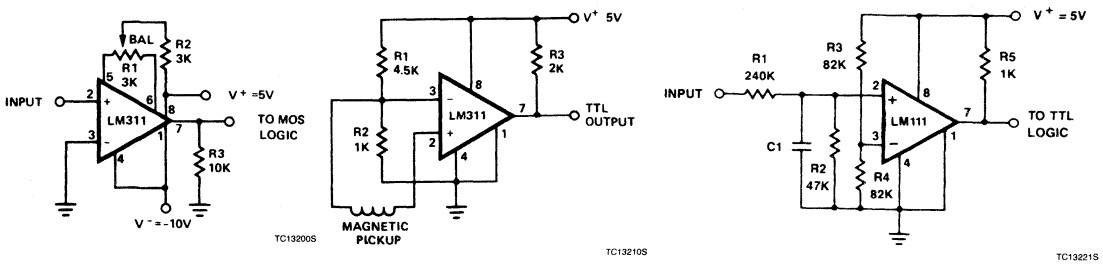
DC ELECTRICAL CHARACTERISTICS [1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LM111/LM211			LM311			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[3]	$T_A = 25°C$, $R_S \leq 50k\Omega$		0.7	3.0		2.0	7.5	mV
I_{OS}	Input offset current[3]	$T_A = 25°C$		4.0	10		6.0	50	nA
I_{BIAS}	Input bias current	$T_A = 25°C$		60	100		100	250	nA
A_V	Voltage gain	$T_A = 25°C$		200			200		V/mV
	Response time[4]	$T_A = 25°C$		200			200		ns
	Saturation voltage	$V_{IN} \leq -5mV$, $I_{OUT} = 50mA$							
V_{SAT}		$T_A = 25°C$		0.75	1.5		0.75	1.5	V
$I_{BAL/STR}$	Strobe on current	$T_A = 25°C$		3.0			3.0		mA
	Output leakage current	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$							
$I_{LEAKAGE}$		$T_A = 25°C$, $I_{STROBE} = 3mA$		0.2	10		0.2	50	nA
V_{OS}	Input offset voltage[3]	$R_S \leq 50k\Omega$			4.0			10	mV
I_{OS}	Input offset current[3]				20			70	nA
I_{BIAS}	Input bias current				150			300	nA
V_{IN}	Input voltage range	$V = \pm 15V$ (Pin 7 may go to 5V)	−14.5	13.8 −14.7	13.0	−14.5	13.8 −14.7	13.0	V
	Saturation voltage	$V=p0 \geq 4.5V$, $V- = 0$							
V_{OL}		$V_{IN} \leq -6mV$, $I_{SINK} \leq 8mA$		0.23	0.4		0.23	0.4	V
I_{OH}	Output leakage current	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$		0.1	0.5				μA
I_{CC}	Positive supply current	$T_A = 25°C$		5.1	6.0		5.1	7.5	mA
I_{EE}	Negative supply voltage	$T_A = 25°C$		4.1	5.0		4.1	5.0	mA

NOTES:

1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. These specifications apply for $V_S = \pm 15V$ and $0°C < T_A < 70°C$ unless otherwsie specified. With the LM211, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$ and for the LM111 is limited to $-55°C < T_A < 125°C$. The offset voltage, offset current, and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
4. The response time specified is for a 100mV input step with 5mV overdrive.
5. Do not short the strobe pin to ground; it should be current driven at 3mA to 5mA.

TYPICAL APPLICATIONS



* Values shown are for a 0 to 30V logic swing and a 15V threshold.
† May be added to control speed and reduce susceptibility to noise spikes.

Zero-Crossing Detector Driving MOS Logic | **Detector for Magnetic Transducer** | **TTL Interface with High Level Logic**

LM119/219/319
Dual Voltage Comparator

Product Specification

DESCRIPTION

The LM119 series are precision high-speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the μA710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL, and TTL as well as capable of driving lamps and relays at currents up to 25mA.

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ± 15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high-speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the μA711.

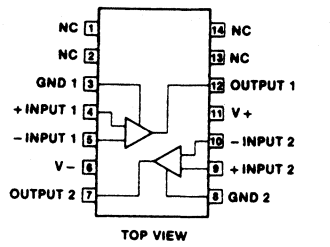
The LM119 is specified from −55°C to +125°C, the LM219 is specified from −25°C to +85°C, and the LM319 is specified from 0°C to +70°C.

FEATURES

- **Two independent comparators**
- **Operates from a single 5V supply**
- **Typically 80ns response time at ± 15V**
- **Minimum fanout of 3 (each side)**
- **Maximum input current of 1μA over temperature**
- **Inputs and outputs can be isolated from system ground**
- **High common-mode slew rate**
- **MIL-STD-883A, B, C available**

PIN CONFIGURATION

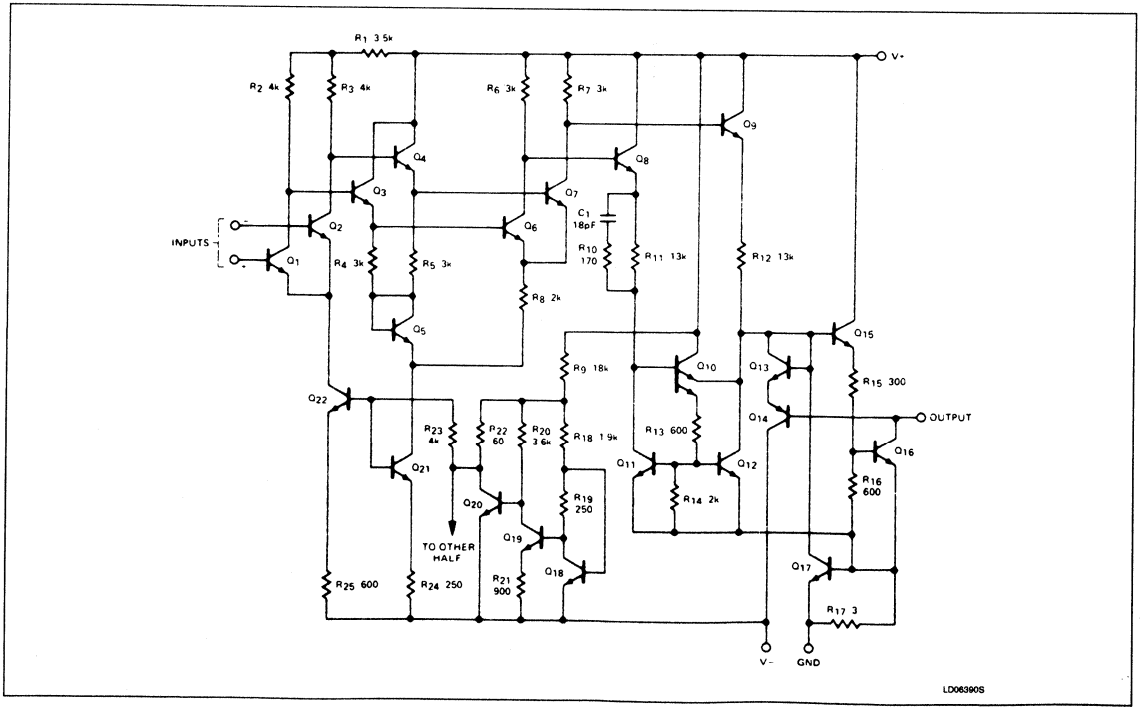
D, F, N Packages



TOP VIEW

CD10960S

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Cerdip	−55°C to +125°C	LM119F
14-Pin Cerdip	−25°C to +85°C	LM219F
14-Pin Plastic SO	0 to +70°C	LM319D
14-Pin Cerdip	0 to +70°C	LM319F
14-Pin Plastic DIP	0 to +70°C	LM319N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Total supply voltage	36	V
	Output to negative supply voltage	36	V
	Ground to negative supply voltage	25	V
	Ground to positive supply voltage	18	V
	Differential input voltage	±5	V
V_{IN}	Input voltage[1]	±15	V
	Maximum power dissipation, T_A = 25°C (still-air)[2]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
	Output short-circuit duration	10	s
T_A	Operating temperature range		
	LM119	−55 to +125	°C
	LM219	−25 to +85	°C
	LM319	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. For supply voltages less than ±15V, the absolute maximum rating is equal to the supply voltage.
2. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C

DC ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, for LM119, $-55°C \leq T_A \leq 125°C$
LM219, $-25°C \leq T_A \leq 85°C$
LM319, $0°C \leq T_A \leq 70°C$
} unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM119/219			LM319			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[1, 2]	$R_S \leq 5k\Omega$, $T_A = 25°C$ Over temp.		0.7	4.0 7		2.0	8.0 10	mV mV
I_{OS}	Input offset current[1, 2]	$T_A = 25°C$ Over temp.		30	75 100		80	200 300	nA nA
I_B	Input bias current[1]	$T_A = 25°C$ Over temp.		150	500 1000		250	1000 1200	nA nA
A_V	Voltage gain	$T_A = 25°C$	10	40		8	40		V/mV
V_{OL}	Saturation voltage	$V_{IN} \leq -5mV$, $I_{OUT} = 25mA$, $T_A = 25°C$ $V_{IN} \leq -10mV$, $I_{OUT} = 25mA$, $T_A = 25°C$ $V+ \geq 4.5V$, $V- = 0$ $V_{IN} \leq -6mV$, $I_{OUT} = 3.2mA$ $T_A \geq 0°C$ $T_A \leq 0°C$ $V_{IN} \leq -10mV$, $I_{OUT} = 3.2mA$		0.75 0.23	1.5 0.4 0.6		 0.75 0.3	 1.5 0.4	V V V V
I_{OH}	Output leakage current	$V- = 0V$, $V_{IN} \geq 5mV$ $V_{OUT} = 35V$, $T_A = 25°C$ Over temp. $V- = 0V$, $V_{IN} \geq 10mV$ $V_{OUT} = 35V$, $T_A = 25°C$		0.2 1	2 10		 0.2	 10	μA μA μA
V_{IN}	Input voltage range	$V_S = \pm 15V$ $V+ = 5V$, $V- = 0V$	 1	± 13	 3	 1	± 13	 3	V V
V_{ID}	Differential input voltage				± 5			± 5	V
$I+$	Positive supply current	$V+ = 5V$, $V- = 0V$, $T_A = 25°C$		4.3			4.3		mA
$I+$	Positive supply current	$V_S = \pm 15V$, $T_A = 25°C$		8.0	11.5		8.0	12.5	mA
$I-$	Negative supply current	$V_S = \pm 15V$, $T_A = 25°C$		3.0	4.5		3.0	5.0	mA

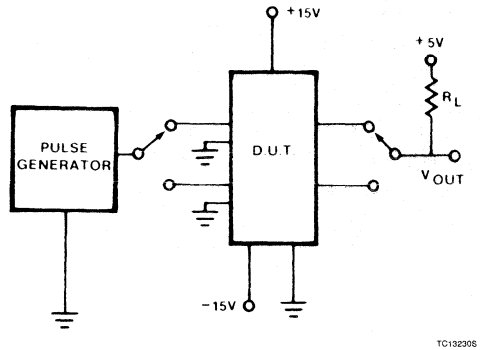
NOTES:
1. V_{OS}, I_{OS} and I_B specifications apply for a supply voltage range of $V_S = \pm 15V$ down to a single 5V supply.
2. The offset voltages and offset currents given are the maximum values required to drive the output to within 1V of either supply with a 1mA load. Thus these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_R	Response time[1]	$V_S = \pm 15V$, $T_A = 25°C$ $R_L = 500\Omega$ (see test figure)		80		ns

NOTE:
1. The response time specified is for a 100mV step with 5mV overdrive.

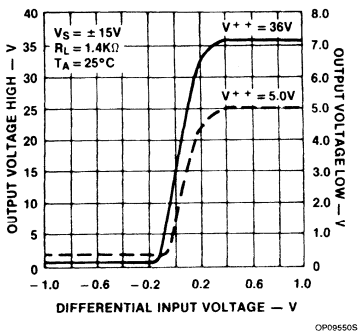
TEST CIRCUIT



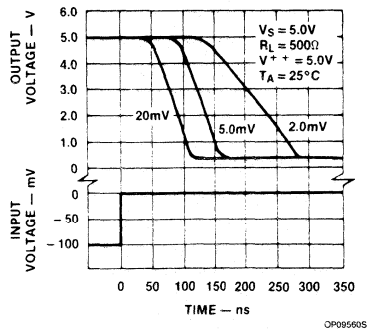
Response Time Measurement

TYPICAL PERFORMANCE CHARACTERISTICS

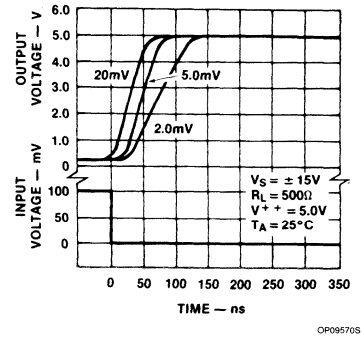
Transfer Function



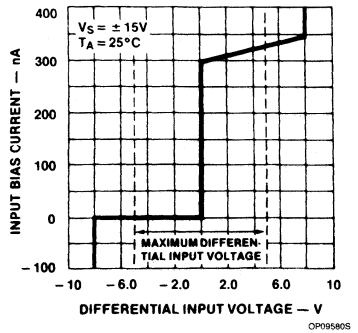
Response Time for Various Input Overdrives



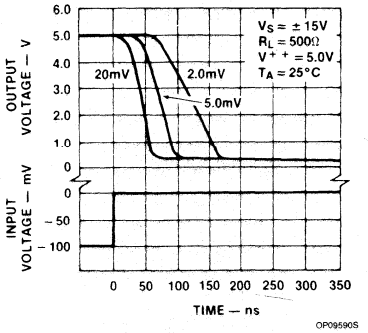
Response Time for Various Input Overdrives



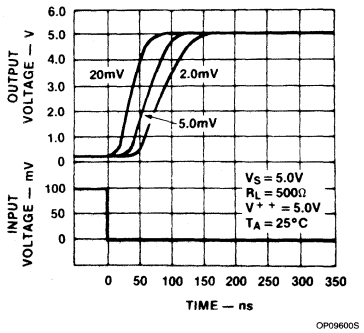
Input Characteristics



Response Time for Various Input Overdrives

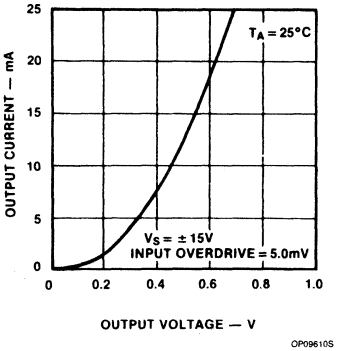


Response Time for Various Input Overdrives

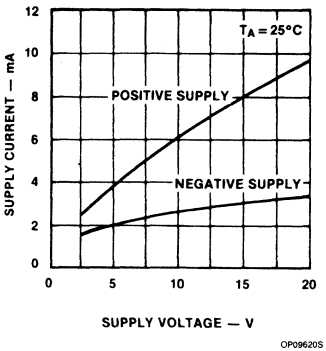


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

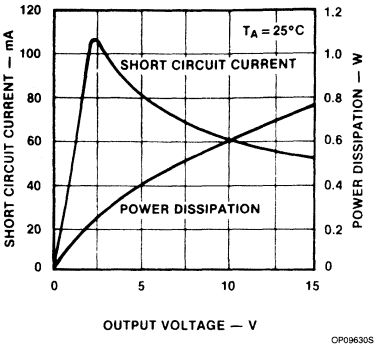
Output Saturation Voltage



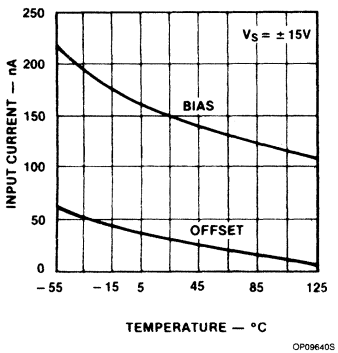
Supply Current



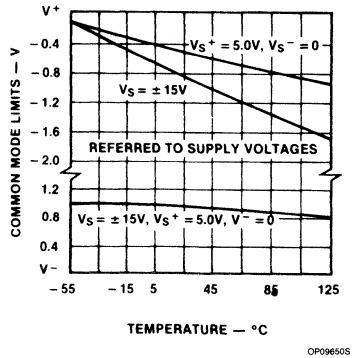
Output Limiting Characteristics



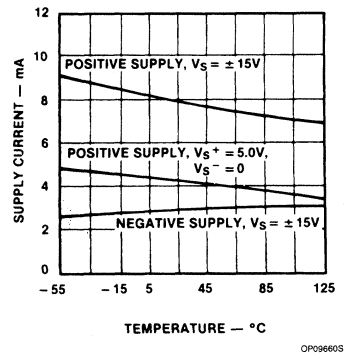
Input Currents (LM119/219)



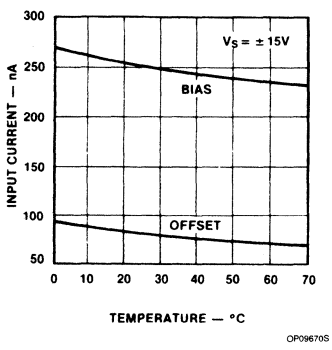
Common-Mode Limits (LM119/219)



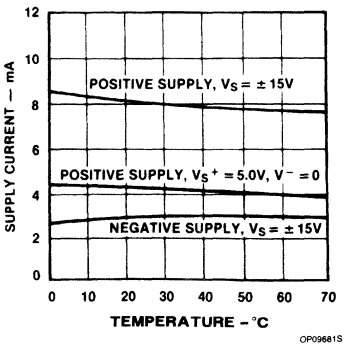
Supply Current (LM119/219)



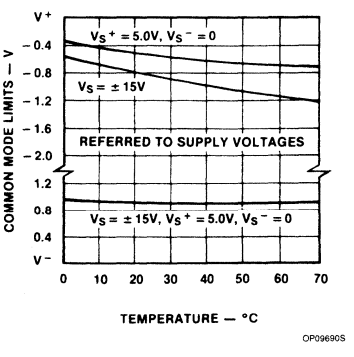
Input Currents (LM319)



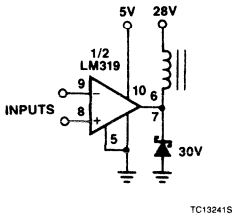
Supply Currents (LM319)



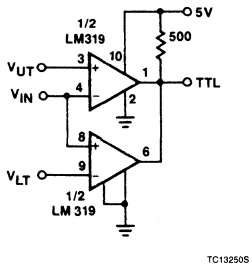
Common-Mode Limits (LM319)



TYPICAL APPLICATIONS

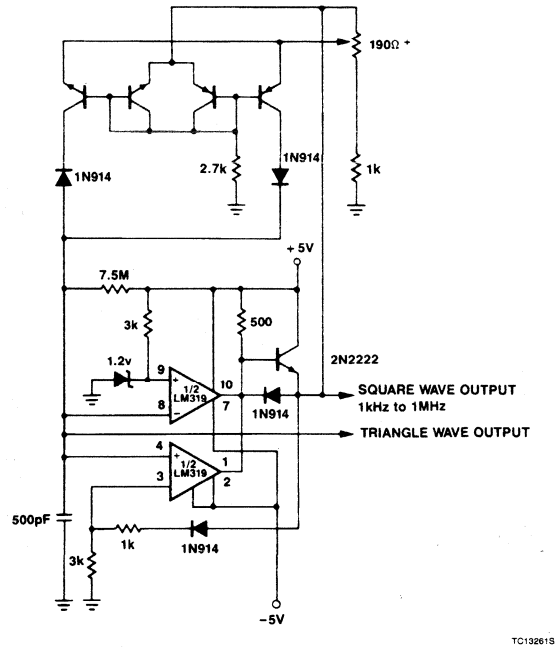


Relay Driver



Window Detector

NOTES:
V_{OUT} = 5V for $V_{LT} < V_{IN} < V_{UT}$
V_{OUT} = 0V for $V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$



NOTE:
Frequency adjust must be buffered for $R_L \leq 10\Omega$

Wide Range Variable Oscillator

LM139A/239A/339A/ LM139/239/339/ LM2901/MC3302 Quad Voltage Comparator

Product Specification

DESCRIPTION

The LM139 series consists of four independent precision voltage comparators, with an offset voltage specification as low as 2.0mV max for each comparator, which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though they are operated from a single power supply voltage.

The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

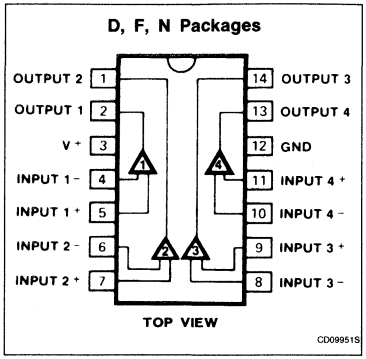
FEATURES

- **Wide single supply voltage range 2.0V_{DC} to 36V_{DC} or dual supplies ± 1.0V_{DC} to ± 18V_{DC}**
- **Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at 5.0V_{DC})**
- **Low input biasing current 25nA**
- **Low input offset current ± 5nA and offset voltage**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems**

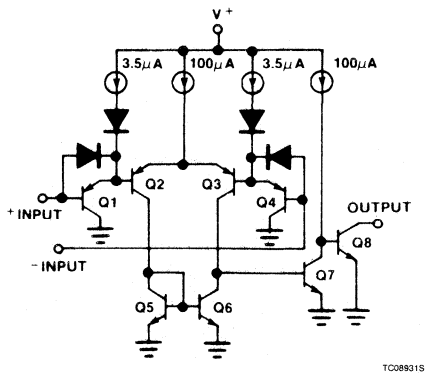
APPLICATIONS

- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATION



EQUIVALENT CIRCUIT



(1 Comparator Only)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Cerdip	0 to +125°C	LM139AF
14-Pin Cerdip	0 to +125°C	LM139F
14-Pin Plastic DIP	−25°C to +85°C	LM239AN
14-Pin Plastic DIP	−25°C to +85°C	LM239N
14-Pin Cerdip	−25°C to +85°C	LM239F
14-Pin Plastic SO	−25°C to +85°C	LM239D
14-Pin Cerdip	−40°C to +85°C	LM2901F
14-Pin Plastic DIP	−40°C to +85°C	LM2901N
14-Pin Plastic SO	−40°C to +85°C	LM2901D
14-Pin Plastic DIP	0 to +70°C	LM339AN
14-Pin Plastic SO	0 to +70°C	LM339D
14-Pin Plastic DIP	0 to +70°C	LM339N
14-Pin Cerdip	0 to +70°C	LM339AF
14-Pin Cerdip	0 to +70°C	LM339F
14-Pin Plastic SO	−40°C to +85°C	MC3302D
14-Pin Cerdip	−40°C to +85°C	MC3302F
14-Pin Plastic DIP	−40°C to +85°C	MC3302N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	V_{CC} supply voltage	36 or ±18	V_{DC}
V_{DIFF}	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	−0.3 to +36	V_{DC}
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1] F package N package D package	 1190 1420 1040	 mW mW mW
	Output short-circuit to ground[2]	Continuous	
I_{IN}	Input current (V_{IN} < −0.3V_{DC})[3]	50	mA
T_A	Operating temperature range LM139A LM239A LM339A LM2901/MC3302	 −55 to +125 −25 to +85 0 to +70 −40 to +85	 °C °C °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F Package at 9.5mW/°C
   N Package at 11.4mW/°C
   D Package at 8.3mW/°C
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is aproximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than −0.3V_{DC}.

DC AND AC ELECTRICAL CHARACTERISTICS $V+ = 5V_{DC}$, LM139A/LM139: $-55°C \leq T_A \leq 125°C$, unless otherwise specified.
LM239: $-25°C \leq T_A \leq 85°C$, unless otherwise specified.
LM339: $0°C \leq T_A \leq 70°C$, unless otherwise specified.

$V+ = 5V_{DC}$, LM339A: $0°C \leq T_A \leq 70°C$, unless otherwise specified.
LM239A: $-25°C \leq T_A \leq 85°C$, unless otherwise specified.
LM2901/LM3302: $-40°C \leq T_A \leq 85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM139A			LM239A/339A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±1.0	±2.0 ±4.0		±1.0	±2.0 ±4.0	mV mV
V_{CM}	Input common-mode voltage range[3]	$T_A = 25°C$ Over temp.	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	V
V_{IDR}	Differential input voltage[1]	Keep all $V_{INs} \geq 0V_{DC}$ (or V− if need)			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400	nA nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN}(+) = 0$, $V_O \leq 1.5V_{DC}$, $T_A = 25°C$ $V_O = 800mV$, over temp.	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN}(-) = 0$ $V_O = 5V_{DC}$, $T_A = 25°C$ $V_O = 30V_{DC}$, over temp.		0.1	 1.0		0.1	 1.0	nA μA
I_{CC}	Supply current	$V+ = 28V$, $R_L = \infty$ on comparators, $T_A = 25°C$ $V+ = 30V$		0.8	2.0		0.8	2.0	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15V_{DC}$	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700	mV mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$, $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
t_R	Response time[5]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3		μs

See notes at the end of the Electrical Characteristics.

DC AND AC ELECTRICAL CHARACTERISTICS $V+ = 5V_{DC}$, LM139A/LM139: $-55°C \leq T_A \leq 125°C$, unless otherwise specified.
LM239: $-25°C \leq T_A \leq 85°C$, unless otherwise specified.
LM339: $0°C \leq T_A \leq 70°C$ unless otherwise specified.

$V+ = 5V_{DC}$, LM339A: $0°C \leq T_A \leq 70°C$, unless otherwise specified
LM239A: $-25°C \leq T_A \leq 85°C$, unless otherwise specified.
LM2901/LM3302: $-40°C \leq T_A \leq 85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM139			LM239/339			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±2.0	±5.0 ±9.0		±2.0	±5.0 ±9.0	mV mV
V_{CM}	Input common-mode voltage range[3]	$T_A = 25°C$ Over temp.	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s $\geq 0V_{DC}$ (or V− if need)			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400	nA nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN}(+) = 0$, $V_O \leq 1.5V_{DC}$, $T_A = 25°C$ $V_O = 800mV$, over temp.	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN}(-) = 0$ $V_O = 5V_{DC}$, $T_A = 25°C$ $V_O = 30V_{DC}$, over temp.		0.1	 1.0		0.1	 1.0	nA μA
I_{CC}	Supply current	$V+ = 28V$, $R_L = \infty$ on comparators, $T_A = 25°C$ $V+ = 30V$		0.8	2.0		0.8	2.0	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15V_{DC}$	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700	mV mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$, $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
t_R	Response time[5]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3		μs

See notes on following page.

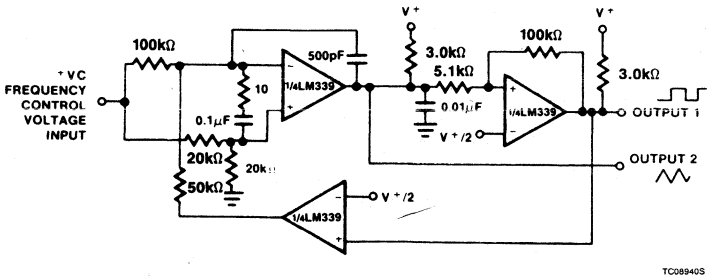
DC AND AC ELECTRICAL CHARACTERISTICS $V+ = 5V_{DC}$, LM139A/LM139: $-55°C \leq T_A \leq 125°C$, unless otherwise specified.
LM239: $-25°C \leq T_A \leq 85°C$, unless otherwise specified.
LM339: $0°C \leq T_A \leq 70°C$ unless otherwise specified.

$V+ = 5V_{DC}$, LM339A: $0°C \leq T_A \leq 70°C$, unless otherwise specified
LM239A: $-25°C \leq T_A \leq 85°C$, unless otherwise specified.
LM2901/LM3302: $-40°C \leq T_A \leq 85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM2901			MC3302			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±2.0 ±9	±7.0 ±15		±3.0	±20 ±40	mV mV
V_{CM}	Input common-mode voltage range[3]	$T_A = 25°C$ Over temp.	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s $\geq 0V_{DC}$ (or V− if need)			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25 200	250 500		25	500 1000	nA nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±5 ±50	±50 ±200		±5	±100 ±300	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN}(+) = 0$, $V_O \leq 1.5V_{DC}$, $T_A = 25°C$ $V_O = 800mV$, over temp.	6.0	16		2.0	6		mA mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN}(-) = 0$ $V_O = 5V_{DC}$, $T_A = 25°C$ $V_O = 30V_{DC}$, over temp.		0.1	 1.0		0.1	 1.0	nA μA
I_{CC}	Supply current	$V+ = 28V$, $R_L = \infty$ on comparators, $T_A = 25°C$ $V+ = 30V$		0.8 1.0	2.0 2.5		.8	1.8	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15V_{DC}$	25	100		2	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		400	400 700		150	400 700	mV mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$, $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
t_R	Response time[5]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3		μs

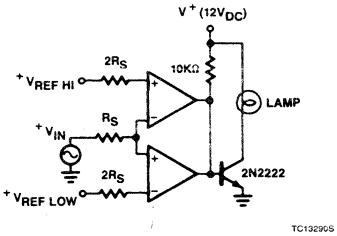
NOTES:
1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (or $0.3V_{DC}$ below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \cong 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from $5V_{DC}$ to $30V_{DC}$; and over the full input common-mode range ($0V_{DC}$ to V+ − $1.5V_{DC}$). Inputs of unused comparators should be grounded.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to $30V_{DC}$ without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained (see typical performance characteristics section).

TYPICAL APPLICATIONS

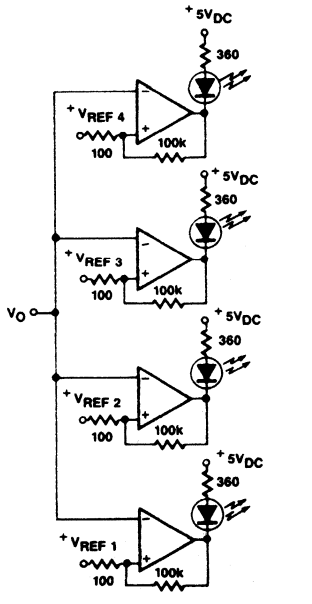


NOTES:
V+ = +30V_{DC}
+ 250m $V_{DC} \leq V_C + 50V_{DC}$
700Hz ≤ f_O ≤ 100kHz

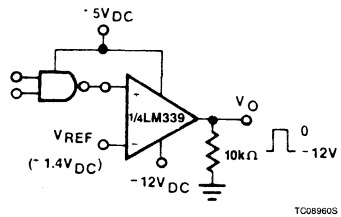
Two-Decade High-Frequency VCO



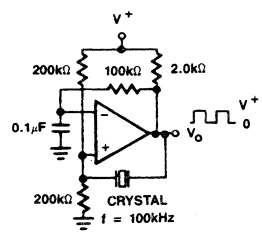
Limit Comparator



Visible Voltage Indicator



TTL-to-MOS Logic Converter

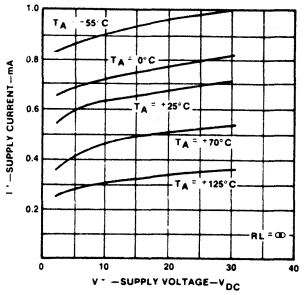


Crystal-Controlled Oscillator

NOTE:
Inputs of unused comparators should be grounded.

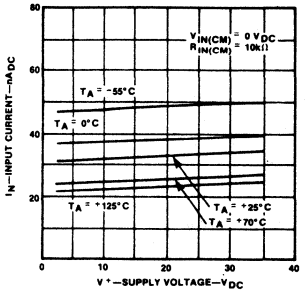
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current



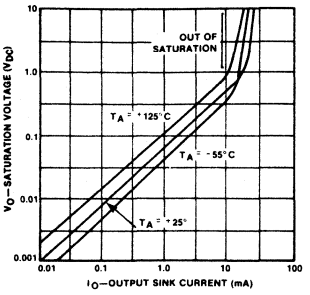
OP05570S

Input Current



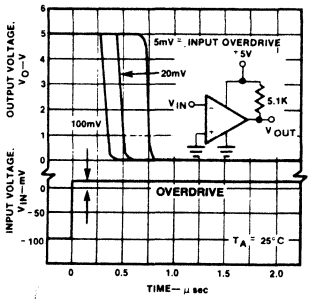
OP05580S

Output Saturation Voltage



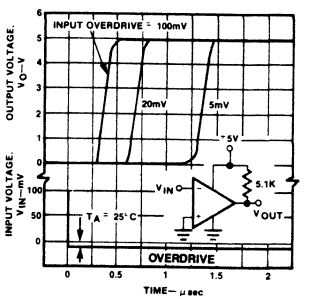
OP05590S

Response Time for Various Input Overdrives — Negative Transition



OP05600S

Response Time for Various Input Overdrives — Positive Transition



OP05610S

LM193/A/293/A/393/A/2903

Low Power Dual Voltage Comparator

Product Specification

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max. for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

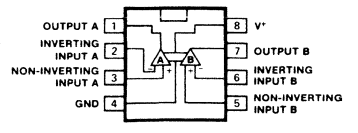
- **Wide single supply voltage range $2.0V_{DC}$ to $36V_{DC}$ or dual supplies $\pm 1.0V_{DC}$, to $\pm 18V_{DC}$**
- **Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/comparator at $5.0V_{DC}$)**
- **Low input biasing current 25nA**
- **Low input offset current $\pm$ 5nA and offset voltage $\pm$ 2mV**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems**

APPLICATIONS

- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATION

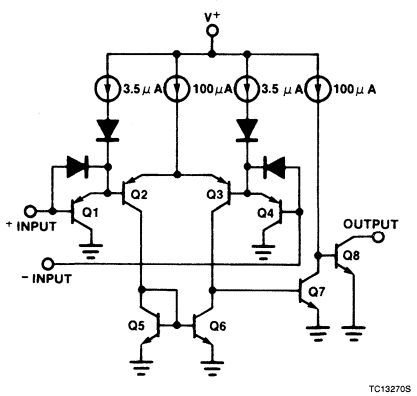
D, N, FE Packages



TOP VIEW

CD10980S

EQUIVALENT CIRCUIT



TC13270S

(One Comparator Only)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Cerdip	−55°C to +125°C	LM193AF
8-Pin Cerdip	−55°C to +125°C	LM193FE
8-Pin Cerdip	−25°C to +85°C	LM293AFE
8-Pin Cerdip	−25°C to +85°C	LM293FE
8-Pin Plastic DIP	−25°C to +85°C	LM293N
8-Pin Plastic SO	−25°C to +85°C	LM293D
8-Pin Plastic DIP	−25°C to +85°C	LM293AN
8-Pin Cerdip	0 to +70°C	LM393AFE
8-Pin Cerdip	0 to +70°C	LM393FE
8-Pin Plastic SO	0 to +70°C	LM393D
8-Pin Plastic DIP	0 to +70°C	LM393N
8-Pin Plastic DIP	0 to +70°C	LM393AN
8-Pin Plastic DIP	−40°C to +85°C	LM2903N
8-Pin Plastic DIP	−40°C to +85°C	LM2903D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	36 or ±18	V_{DC}
	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	−0.3 to +36	V_{DC}
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1] F package N package D package	 780 1160 780	 mW mW mW
	Output short-circuit to ground[2]	Continuous	
I_{IN}	Input current ($V_{IN} < -0.3V_{DC}$)[3]	50	mA
T_A	Operating temperature range LM193/193A LM293/293A LM393/393A LM2903	 −55 to +125 −25 to +85 0 to +70 −40 to +85	 °C °C °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$.

DC AND AC ELECTRICAL CHARACTERISTICS $V+ = 5V_{DC}$, LM193/193A: $-55°C \leq T_A \leq +125°C$, unless otherwise specified.
LM293/293A: $-25°C \leq T_A \leq +85°C$, unless otherwise specified.
LM393/393A: $0°C \leq T_A \leq +70°C$, unless otherwise specified.
LM2903: $-40°C \leq T_A \leq +85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM193A			LM293A/393A			LM2903			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±1.0	±2.0 ±4.0		±1.0	±2.0 ±4.0		±2.0 ±9	±7.0 ±15	mV mV
V_{CM}	Input common-mode voltage range[3, 6]	$T_A = 25°C$ Over temp.	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	V V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s $\geq 0V_{DC}$ (or V− if need)			V+			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400		25 200	250 500	nA nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150		±5 ±50	±50 ±200	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $V_O \leq 1.5V_{DC}$ $T_A = 25°C$	6.0	16		6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN(-)} = 0$ $V_O = 30V_{DC}$ Over temp. $V_O = 5V_{DC}$, $T_A = 25°C$		0.1	1.0		0.1	1.0		0.1	1.0	nA μA
I_{CC}	Supply current	$R_L = \infty$ on both comparators. $T_A = 25°C$ V+ = 30V, over temp.		0.8 1	1 2.5		0.8 1	1 2.5		0.8 1	1 2.5	mA mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15V_{DC}$, $T_A = 25°C$	50	200		50	200		25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700		400	400 700	mV mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$ $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300			300		ns
t_R	Response time[5]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$ $T_A = 25°C$		1.3			1.3			1.3		μs

DC ELECTRICAL CHARACTERISTICS (Continued)

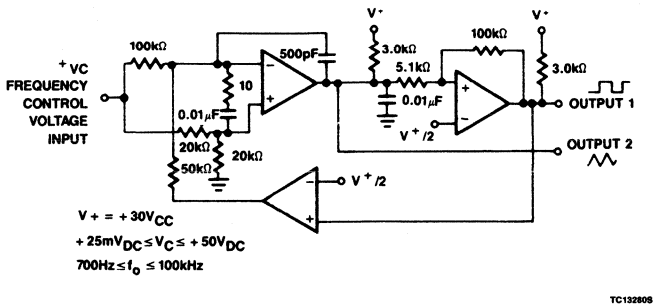
$V+ = 5V_{DC}$, LM193/193A: $-55°C \leq T_A \leq +125°C$, unless otherwise specified.
LM293/293A: $-25°C \leq T_A \leq +85°C$, unless otherwise specified.
LM393/393A: $0°C \leq T_A \leq +70°C$, unless otherwise specified.
LM2903: $-40°C \leq T_A \leq +85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM193			LM293/393			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±2.0	±5.0 ±9.0		±2.0	±5.0 ±9.0	mV mV
V_{CM}	Input common-mode voltage range[3, 6]	$T_A = 25°C$ Over temp.	0 0		V±−1.5 V±−2.0	0 0		V+−1.5 V+−2.0	V V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s $\geq 0V_{DC}$ (or V−if need)			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400	nA nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $V_O \leq 1.5V_{DC}$ $T_A = 25°C$	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN(-)} = 0$, $V_O = 5V_{DC}$ $T_A = 25°C$ $V_O = 30VDC$ over temp.		0.1	 1.0		0.1	 1.0	nA μA
I_{CC}	Supply current	$R_L = \infty$ on both comparators $T_A = 25°C$ V+ = 30V, over temp.		0.8	1 2.5		0.8	1 2.5	mA mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15V_{DC}$	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700	mV mV
t_{LSR}	Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$, $V_{RL} = 5V_{DC}$ $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
t_R	Response time[5]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$ $T_A = 25°C$		1.3			1.3		μs

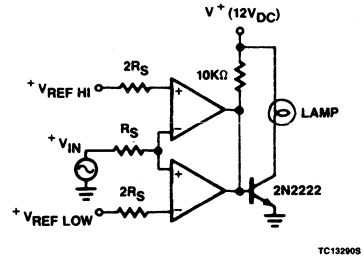
NOTES:

1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (V_{DC} below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \cong 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from $5V_{DC}$ to $30V_{DC}$ and over the full input common-mode range ($0V_{DC}$ to $V+ - 1.5V_{DC}$).
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to $30V_{DC}$ without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive.
6. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

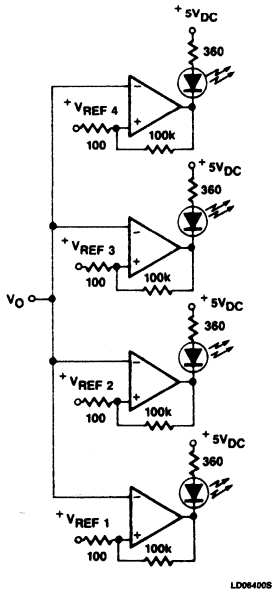
TYPICAL APPLICATIONS



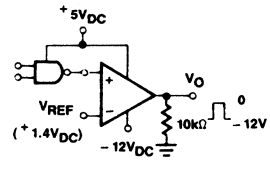
Two-Decade High-Frequency VCO



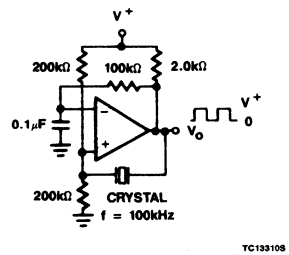
Limit Comparator



Visible Voltage Indicator



TTL-to-MOS Logic Converter

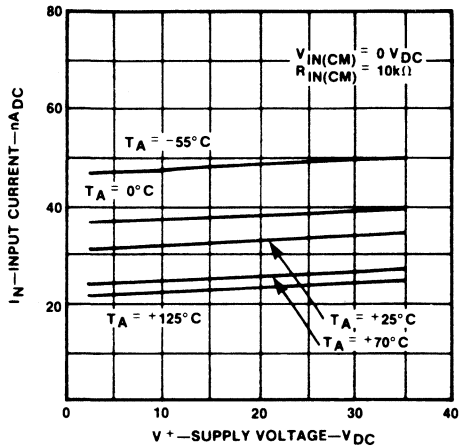


Crystal-Controlled Oscillator

NOTE:
All pins of any unused comparators should be grounded.

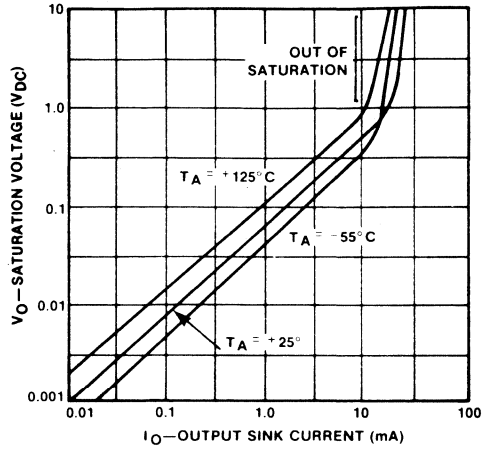
TYPICAL PERFORMANCE CHARACTERISTICS

Input Current



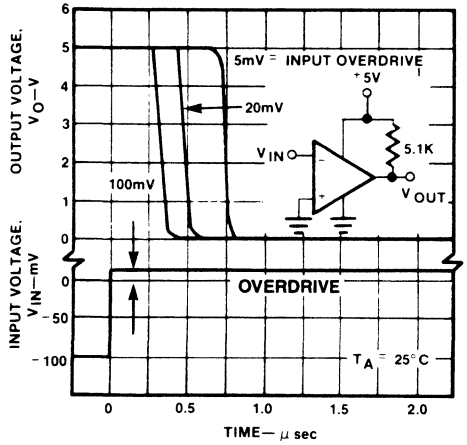
OP05580S

Output Saturation Voltage



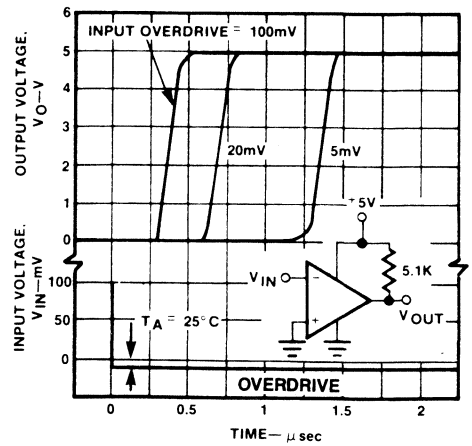
OP05590S

Response Time for Various Input Overdrives — Negative Transition



OP05600S

Response Time for Various Input Overdrives — Positive Transition



OP05610S

NE/SE521
High-Speed Dual-Differential Comparator/Sense Amp

Product Specification

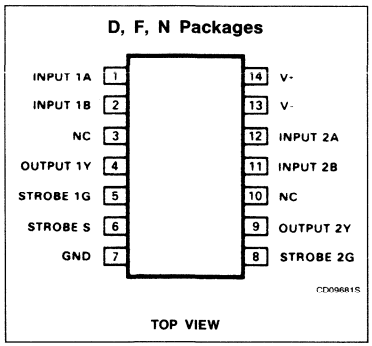
FEATURES

- 12ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

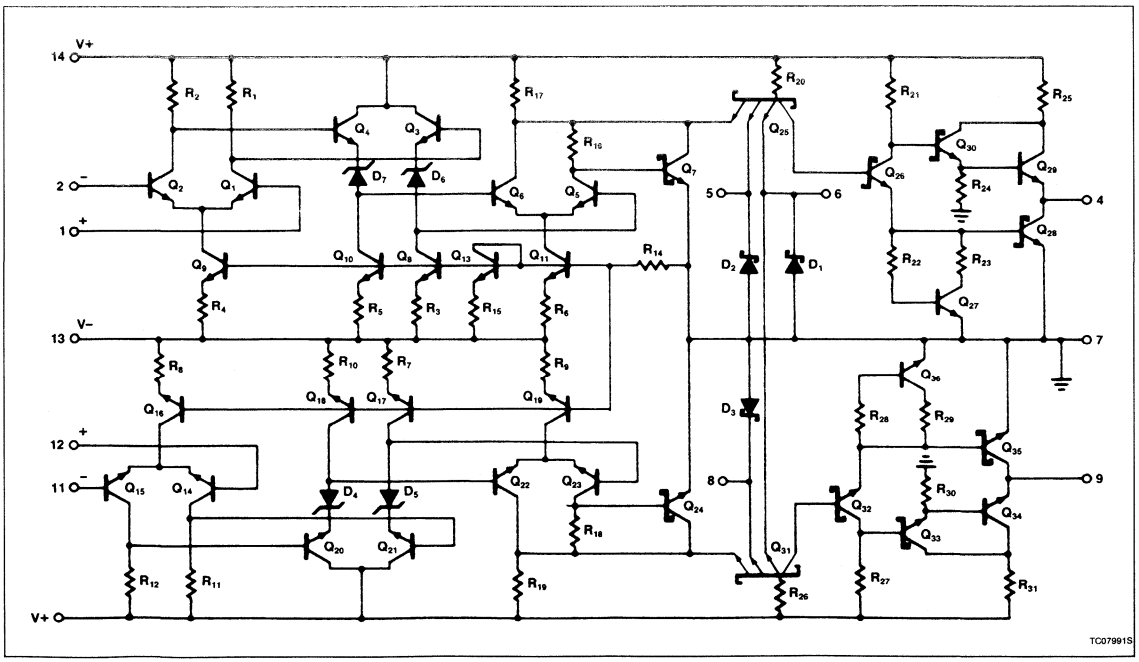
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE521N
14-Pin SO Package	0 to +70°C	NE521D
14-Pin Cerdip	0 to +70°C	NE521F
14-Pin Cerdip	−55°C to +125°C	SE521F

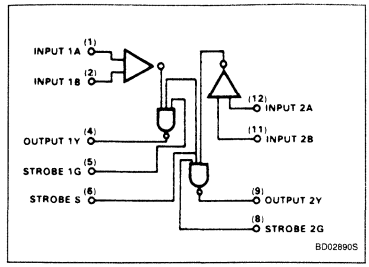
EQUIVALENT SCHEMATIC



LOGIC FUNCTIONS

V_{ID} A^+, B^-	STROBE S	STROBE G	OUTPUT (Y)
$V_{ID} \leqslant -V_{OS}$	H	H	L
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined
$V_{ID} \geqslant V_{OS}$	H	H	H
X	L	X	H
X	X	L	H

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage		
V+	Positive	+7	V
V–	Negative	–7	V
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		
	Common mode	±5	V
	Strobe/gate	+5.25	V
P_D	Maximum power dissipation[1] T_A = 25°C (still-air)		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range		
	NE521	0 to 70	°C
	SE521	–55 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	+300	°C

NOTE:

1. Derate above 25°C at the following rates:
   F package at 9.5mW/°C.
   N package at 11.4mW/°C.
   D package at 8.3mW/°C.

DC ELECTRICAL CHARACTERISTICS (SE521) V+ = +5V, V– = –5V, T_A = –55°C to +125°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage At 25°C Over temperature range	V+ = +4.5V, V– = –4.5V		6	7.5 15	mV
I_{BIAS}	Input bias current At 25°C Over temperature range	V+ = +5.5V, V– = –5.5V		7.5	20 40	μA
I_{OS}	Input offset current At 25°C Over temperature range	V+ = +5.5V, V– = –5.5V		1.0	5 12	μA
V_{CM}	Common-mode voltage range	V+ = +4.5V, V– = –4.5V	±3			V
V_{IL}	Low level input voltage At 25°C Over temperature				0.8 0.7	V
V_{IH}	High level input voltage		2.0			V
I_{IH}	Input current High	V+ = +5.5V, V– = –5.5V V_{IH} = 2.7V 1G or 2G strobe Common strobe S			 50 100	 μA μA
I_{IL}	Input Current Low	 V_{IL} = 0.5V 1G or 2G strobe Common strobe S			 –2.0 –4.0	 mA mA
V_{OH} V_{OL}	Output voltage High Low	$V_{I(S)}$ = 2.0V V+ = +4.5V, V– = –4.5V, I_{LOAD} = –1mA V+ = +4.5V, V– = –4.5V, I_{LOAD} = 10mA T_A = 25°C, I_{LOAD} = 20mA	2.5	3.4	 0.5 0.5	V
V+ V–	Supply voltage Positive Negative		4.5 –4.5	5.0 –5.0	5.5 –5.5	V
I_{CC+} I_{CC-}	Supply current Positive Negative	V+ = 5.5V, V– = –5.5V, T_A = 25°C		27 –15	35 –28	mA
I_{SC}	Short-circuit output current		–35		–115	mA

DC ELECTRICAL CHARACTERISTICS (NE521) V+ = +5V, V– = –5V, T_A = 0 to 70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage At 25°C Over temperature range	V+ = +4.75V, V– = –4.75V		6	7.5 10	mV
I_{BIAS}	Input bias current At 25°C Over temperature range	V+ = +5.25V, V– = –5.25V		7.5	20 40	μA
I_{OS}	Input offset current At 25°C Over temperature range	V+ = +5.25V, V– = –5.25V		1.0	5 12	μA
V_{CM}	Common-mode voltage range	V+ = +4.75V, V– = –4.75V	±3			V
I_{IH}	Input current High	V+ = +5.25V, V– = –5.25V V_{IH} = 2.7V 1G or 2G strobe Common strobe S			 50 100	 μA μA
I_{IL}	Input Current Low	 V_{IL} = 0.5V 1G or 2G strobe Common strobe S			 –2.0 –4.0	 mA mA
V_{OH} V_{OL}	Output voltage High Low	$V_{I(S)}$ = 2.0V V+ = +4.75V, V– = –4.75V, I_{LOAD} = –1mA V+ = +5.25V, V– = –5.25V, I_{LOAD} = 20mA	2.7	3.4	 0.5	V
V+ V–	Supply voltage Positive Negative		4.75 –4.75	5.0 –5.0	5.25 –5.25	V
I_{CC+} I_{CC-}	Supply current Positive Negative	V+ = 5.25V, V– = –5.25V, T_A = 25°C		27 –15	35 –28	mA
I_{SC}	Short-circuit output current		–40		–100	mA

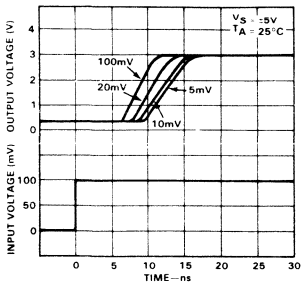
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, R_L = 280Ω C_L = 15pF V+ = 5V V– = 5V.

SYMBOL	PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
Large-signal switching speed							
$t_{PLH(D)}$ $t_{PHL(D)}$ $t_{PLH(S)}$ $t_{PHL(S)}$	Propagation delay Low to high[1] High to low[1] Low to high[2] High to low[2]	 Amp Amp Strobe Strobe	 Output Output Output Output		 8 6 4.5 3.0	 12 9 10 6	 ns
f_{MAX}	Max. operating frequency			40	55		MHz

NOTES:
1. Response time measured from 0V point of ±100mV_{P-P} 10MHz square wave to the 1.5V point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of the output.

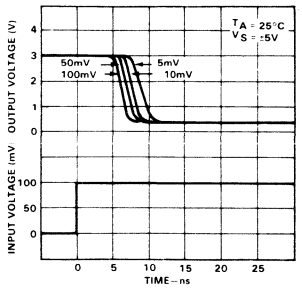
TYPICAL PERFORMANCE CHARACTERISTICS

Response Time for Various Input Overdrives



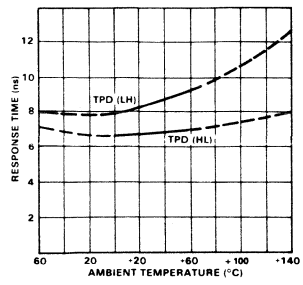
OP03890S

Response Time for Various Input Overdrives



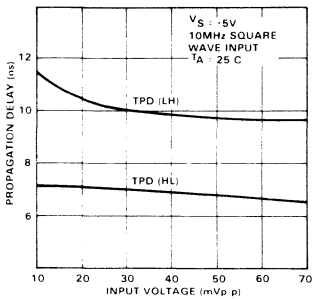
OP03900S

Response Time vs Temperature



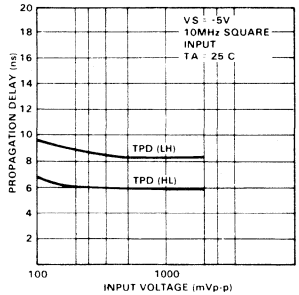
OP03910S

Propagation Delay for Various Input Voltage



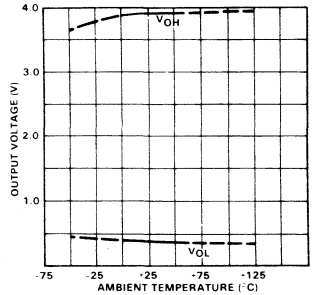
OP03920S

Propagation Delay for Various Input Voltages



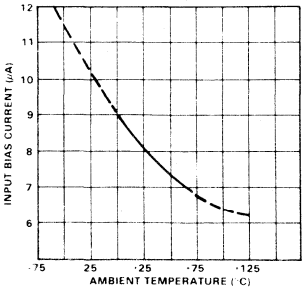
OP03930S

Output Voltage vs Ambient Temperature



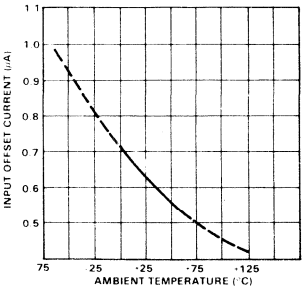
OP03940S

Input Bias Current vs Ambient Temperature



OP03950S

Input Offset Current vs Ambient Temperature



OP03960S

NE/SE522
High-Speed Dual-Differential Comparator/Sense Amp

Product Specification

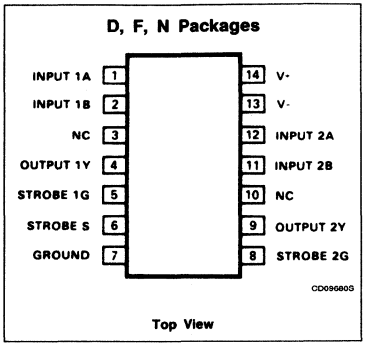
FEATURES

- **15ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **TTL-compatible strobes and outputs**
- **Large common-mode input voltage range**
- **Operates from standard supply voltages**

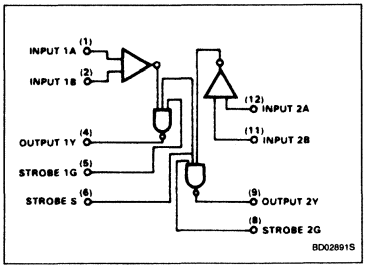
APPLICATIONS

- **MOS memory sense amp**
- **A-to-D conversion**
- **High-speed line receiver**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

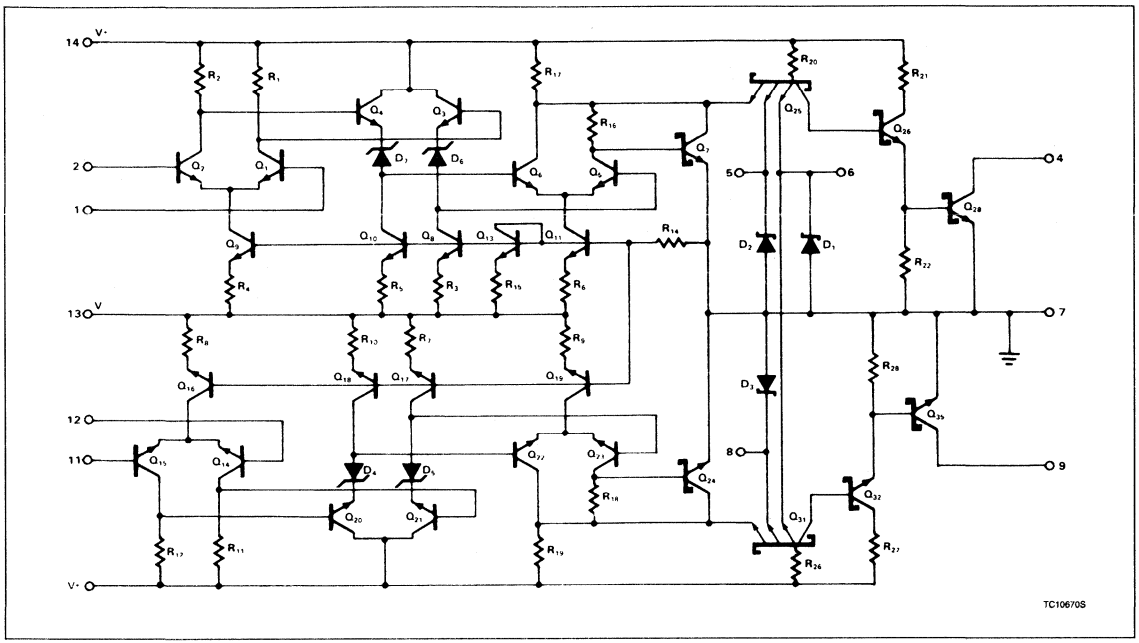
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Cerdip	0 to 70°C	NE522F
14-Pin Cerdip	−55°C to 125°C	SE522F
14-Pin Plastic DIP	0 to +70°C	NE522N
14-Pin Plastic SO	0 to 70°C	NE522D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage		V
V_+	Positive	+7	
V_-	Negative	−7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common-mode	±5	
	Strobe/gate	+5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range NE522	0 to 70	°C
	SE522	−55 to +125	
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

High-Speed Dual-Differential Comparator/Sense Amp NE/SE522

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS (SE522)± 5V ± 10%, T_A = −55 to +125°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage At 25°C Over temperature range	V+ = +4.5V, V− = −4.5V		6	7.5 15	mV
I_{BIAS}	Input bias current At 25°C Over temperature range	V+ = +5.5V, V− = −5.5V		7.5	20 40	μA
I_{OS}	Input offset current At 25°C Over temperature range	V+ = +5.5V, V− = −5.5V		1.0	5 12	μA
V_{CM}	Common-mode voltage range	V+ = +4.5V, V− = −4.5V	±3			V
V_{IL}	Low level input Voltage at 25°C Over temperature				0.8 0.7	V
V_{IH}	High level temperature		2.0			V
I_{IH}	Input current High	V+ = +5.5V, V− = −5.5V V_{IH} = 2.7V 1G or 2G strobe Common strobe S			 50 100	 μA μA
I_{IL}	Low input current	V_{IL} = 0.5V 1G 2G strobe Common strobe S			 −2 −4	 mA mA
V_{OL}	Output voltage Low	V+ = +4.5V, V− = −4.5V I_{OL} = 20mA, T_A = 25°C I_{OL} = 10mA			 0.5 0.5	V
I_{OH}	Output current High	V_{CC+} = +4.5, V_{CC-} = −4.5V, V_{OH} = 5.5V			250	μA
V+ V−	Supply voltage Positive Negative		4.5 −4.5	5.0 −5.0	5.5 −5.5	V
I_{CC+} I_{CC-}	Supply current Positive Negative	V+ = 5.5V, V− = −5.5V, T_A = 25°C		27 −15	35 −28	mA

DC ELECTRICAL CHARACTERISTICS (NE522)± 5V ±5%, T_A = 0 to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage At 25°C Over temperature range	V+ = +4.75V, V– = –4.75V		6	7.5 10	mV
I_{BIAS}	Input bias current At 25°C Over temperature range	V+ = +5.25V, V– = –5.25V		7.5	20 40	μA
I_{OS}	Input offset current At 25°C Over temperature range	V+ = +5.25V, V– = –5.25V		1.0	5 12	μA
V_{CM}	Common-mode voltage range	V+ = +4.75V, V– = –4.75V	±3			V
I_{IH}	Input current High	V+ = +5.25V, V– = –5.25V V_{IH} = 2.7V 1G or 2G strobe Common strobe S			 50 100	 μA μA
I_{IL}	Low	V_{IL} = 0.5V 1G 2G strobe Common strobe S			 –2.0 –4.0	 mA mA
V_{OL}	Output voltage low	V+ = +5.25V, V– = –5.25V, $V_{I(S)}$ = 2.0V I_{LOAD} = 20mA			0.5	V
I_{OH}	Output current high High	 V_{CC+} = +4.75 V_{CC-} = –4.75V, V_{OH} = 5.25V			 250	 μA
V+ V–	Supply Voltage Positive Negative		 4.75 –4.75	 5.0 –5.0	 5.25 –5.25	 V
I_{CC+} I_{CC-}	Supply current Positive Negative	V+ = 5.25V, V– = –5.25V, T_A = 25°C		 27 –15	 35 –28	 mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $R_L = 280\Omega$, $C_L = 15pF$

SYMBOL	PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
I_R	Input resistance				4		kΩ
I_C	Input capacitance				3		pF
Large-signal switching speed							
	Propagation delay						
$t_{PLH(D)}$	Low to high[1]	Amp	Output		10	15	
$t_{PHL(D)}$	High to low[1]	Amp	Output		8	12	ns
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		6	13	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		5	9	
f_{MAX}	Maximum operating frequency			25	35		MHz

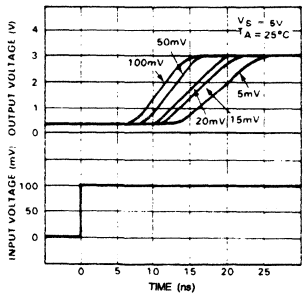
NOTES:
1. Response time measured from 0V point of $\pm 100mV_{P-P}$ 10MHz square wave to the 1.5V point of the output.
2. Response time measured from 1.5V point of the input to 1.5V point of the output.

LOGIC FUNCTION TABLE

V_{ID} (A^+, B^-)	STRS	STRG	Output Transistor
$< -V_{OS}$	H	H	ON
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined
$> V_{OS}$	H	H	OFF
X	L	X	OFF
X	X	L	OFF

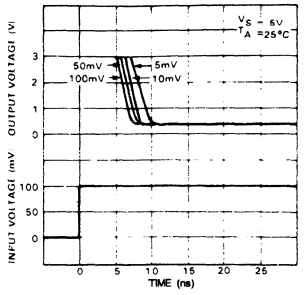
TYPICAL PERFORMANCE CHARACTERISTICS

Response Time for Various Input Overdrives



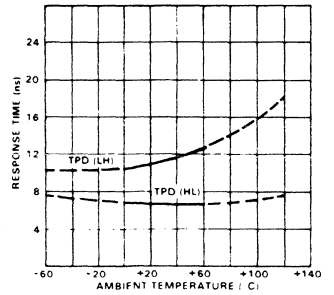
OP06701S

Response Time for Various Input Overdrives



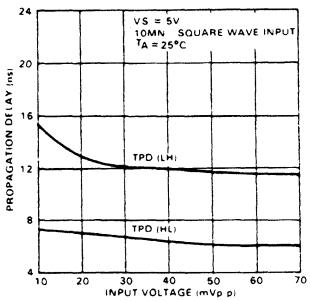
OP06711S

Response Time vs Temperature



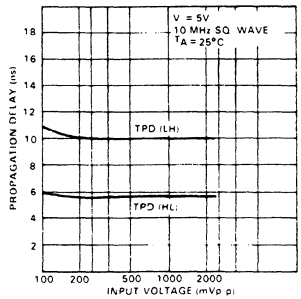
OP06721S

Propagation Delay for Various Input Voltages



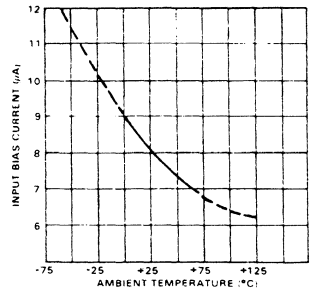
OP06731S

Propagation Delay for Various Input Voltages



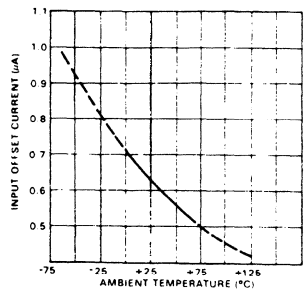
OP06741S

Input Bias Current vs Ambient Temperature



OP06751S

Input Offset Current vs Ambient Temperature



OP06761S

NE/SE527
Voltage Comparator

Product Specification

DESCRIPTION

The NE/SE527 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed TTL gates with a precision linear amplifier on a single monolithic chip. The NE/SE527 is similar in design to the Signetics NE/SE529 voltage comparator except that it incorporates an "Emitter-Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

FEATURES

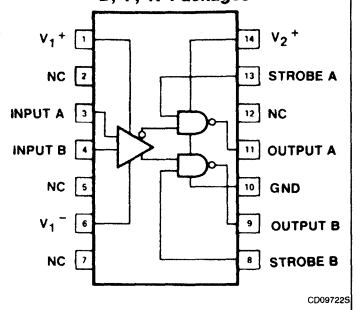
- **15ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common-mode and differential voltage range**
- **MIL-STD-883A, B, C available**
- **Typical gain of 5000**

APPLICATIONS

- **A/D conversion**
- **ECL-to-TTL interface**
- **TTL-to-ECL interface**
- **Memory sensing**
- **Optical data coupling**

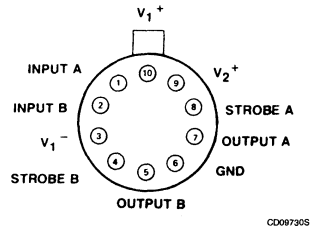
PIN CONFIGURATIONS

D, F, N Packages



CD09722S

H Package[1]



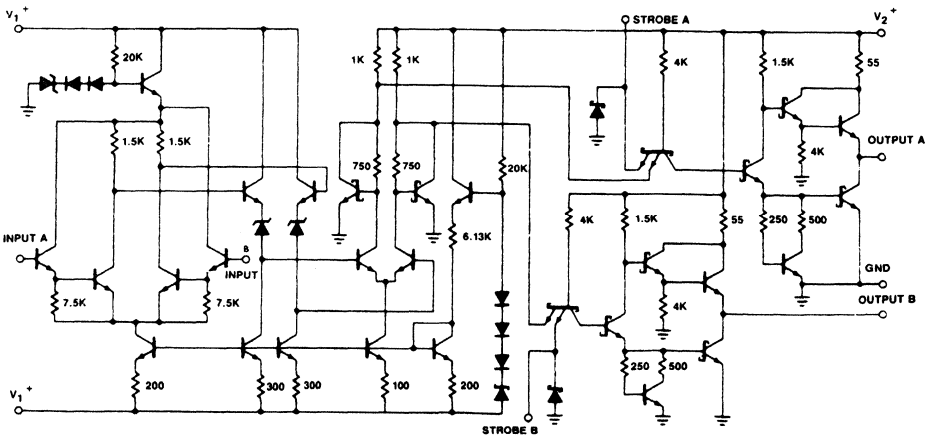
CD09730S

NOTE:
1. Metal cans (H) not recommended for new designs.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE527N
14-Pin Cerdip	0 to +70°C	NE527F
14-Pin SO	0 to +70°C	NE527D
14-Pin Cerdip	−55°C to +125°C	SE527F
10-Lead metal can	0 to +70°C	NE527H
10-Lead metal can	−55°C to +125°C	SE527H

EQUIVALENT SCHEMATIC



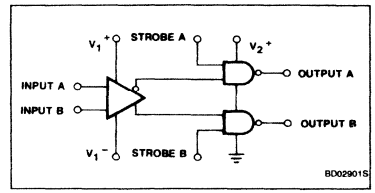
TC08004S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_1+	Positive supply voltage	+15	V
V_1-	Negative supply voltage	−15	V
V_2+	Gate supply voltage	+7	V
V_{OUT}	Output voltage	+7	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Input common mode voltage	±6	V
P_D	Max power dissipation[1] 25°C ambient (still air) F package N package D package	 1190 1420 1040	 mW mW mW
T_A	Operating temperature range NE527 SE527	 0 to +70 −55 to +125	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTE:
1. Derate above 25°C, at the following rates:
   F package 9.5mW/°C
   N package 11.4mW/°C
   D package 8.3mW/°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $V_1+ = 10V$, $V_1- = -10V$, $V_2+ = +5.0V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE527			NE527			UNIT
			Min	Typ	Max	Min	Typ	Max	
Input characteristics									
V_{OS}	Input offset voltage @ 25°C				4			6	mV
	over temperature range				6			10	mV
I_{BIAS}	Input bias current @ 25°C				2			2	μA
	over temperature range				4			4	μA
I_{OS}	Input offset current @ 25°C				0.5			0.75	μA
	over temperature range	$V_{IN} = 0V$			1			1	μA
	common-mode voltage range				±5			±5	V
Gate characteristics									
V_{OUT}	Output Voltage								
	"1" State	$V_2+ = 4.75V$, $I_{SOURCE} = -1mA$	2.5	3.3		2.7	3.3		V
	"0" State	$V_2+ = 4.75V$, $I_{SINK} = 10mA$			0.5			0.5	V
	Strobe inputs								
	"0" Input current[1]	$V_2+ = 5.25V$, $V_{STROBE} = 0.5V$			−2			−2	mA
	"1" Input current @ 25°C[1]	$V_2+ = 5.25V$, $V_{STROBE} = 2.7V$			50			100	μA
	Over temperature range	$V_2+ = 5.25V$, $V_{STROBE} = 2.7V$			200			200	μA
	"0" Input voltage	$V_2+ = 4.75V$			0.8			0.8	V
	"1" Input voltage	$V_2+ = 4.75V$	2.0			2.0			V
I_{SC}	Short-circuit output current	$V_2+ = 5.25V$, $V_{OUT} = 0V$	−18		−70	−18		−70	mA
Power supply requirements									
	Supply voltage								
V_1+			5		10	5		10	V
V_1-			−6		−10	−6		−10	V
V_2+			4.5	5	5.5	4.75	5	5.25	V
	Supply current	$V_1+ = 10V$, $V_1- = -10V$							
		$V_2+ = 5.25V$							
I_1+		Over temp.			5			5	mA
I_1-		Over temp.			10			10	mA
I_2+		Over temp.			20			20	mA

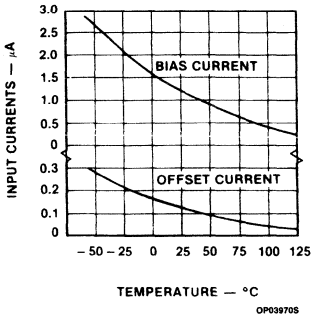
NOTE:
1. See Logic Function Table.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified. (See AC test circuit)

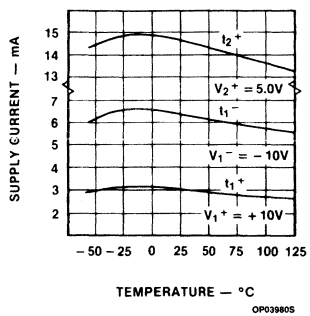
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Transient response propagation delay time					
t_{PLH}	Low-to-High	$V_{IN} = \pm 100mV$ step		16	26	ns
t_{PHL}	High-to-Low			14	24	ns
	Delay between output A and B			2	5	ns
	Strobe delay time					
t_{ON}	Turn-on time			6		ns
t_{OFF}	Turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS

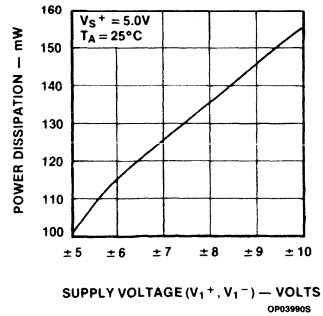
Input Currents vs Temperature



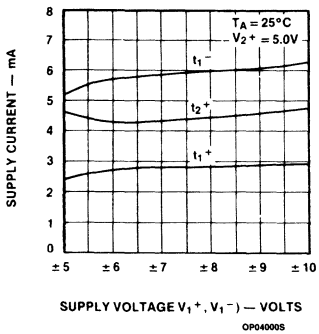
Supply Current vs Temperature



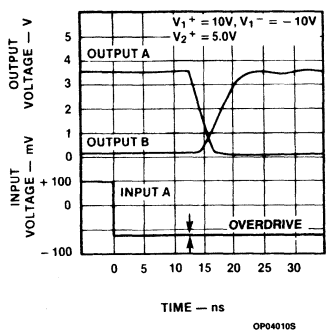
Power Dissipation vs Supply Voltage



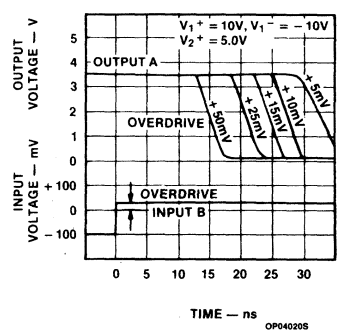
Supply Current vs Supply Voltage



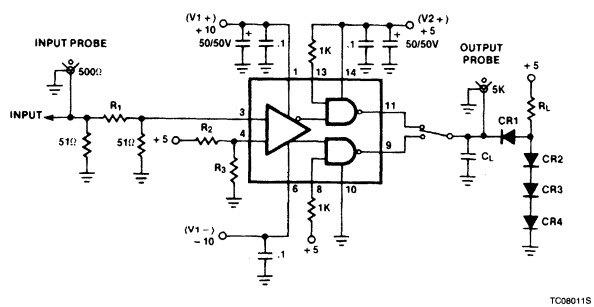
Output Propagation Delays



Response Time for Various Input Overdrives



RESPONSE TIME TEST CIRCUIT



NOTES:
CR1 – CR4 = IN914
R1 selected for 15:1 divider
R2, 3 selected for 100mV at Pin 4

Input
PRR = 1MHz
P_W = 50ns
$T_r = T_f$ = 2ns
Amplitude = 3.00V

Output
R_L = 390Ω
C_L = 25pF (including stray capacitance)

Voltage Comparator — NE/SE527

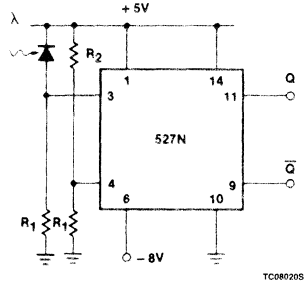
APPLICATIONS

One of the main features of the device is that supply voltages (V_1+, V_1-) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V_1-) should always be at least 6V more than the ground terminal (Pin 6). Input common-mode range should be limited to values of 2V less than the supply voltages (V_1+ and V_1-) up to a maximum of ±6V as supply voltages are increased. It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

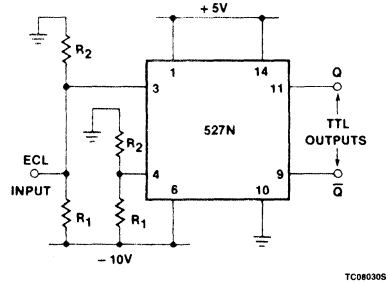
LOGIC FUNCTION

V_{ID} (A^+, B^-)	STROBE A	STROBE B	OUTPUT A	OUTPUT B	COMMENT
$V_{ID} \leq -V_{OS}$	H	X	L	H	Read I_{IHA}, I_{ILB}
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined	Undefined	
$V_{ID} \geq V_{OS}$	X	H	H	L	Read I_{ILA}, I_{IHB}
X	L	L	H	H	

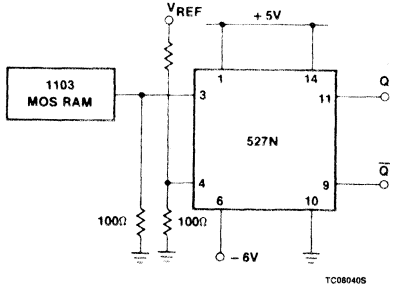
TYPICAL APPLICATIONS



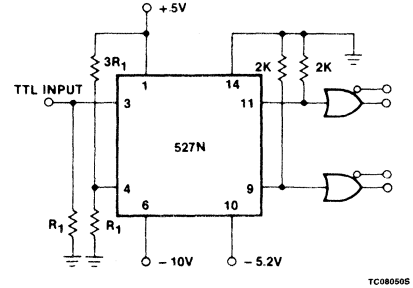
Photodiode Detector



ECL-to-TTL Interface



MOS Memory Sense AMP



TTL-to-ECL Interface

NE/SE529
Voltage Comparator

Product Specification

DESCRIPTION

The NE/SE529 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high-speed TTL gates with a precision linear amplifier on a single monolithic chip.

FEATURES

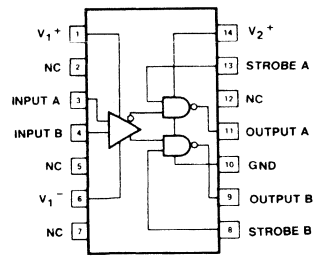
- **10ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common-mode and differential voltage range**
- **Typical gain 5000**

APPLICATIONS

- **A/D conversion**
- **ECL-to-TTL interface**
- **TTL-to-ECL interface**
- **Memory sensing**
- **Optical data coupling**
- **MIL-STD-883A, B, C available**

PIN CONFIGURATIONS

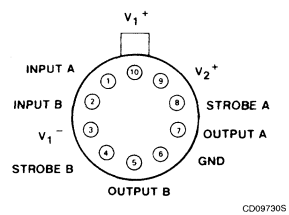
D, F, N Packages



TOP VIEW

CD09722S

H Package*



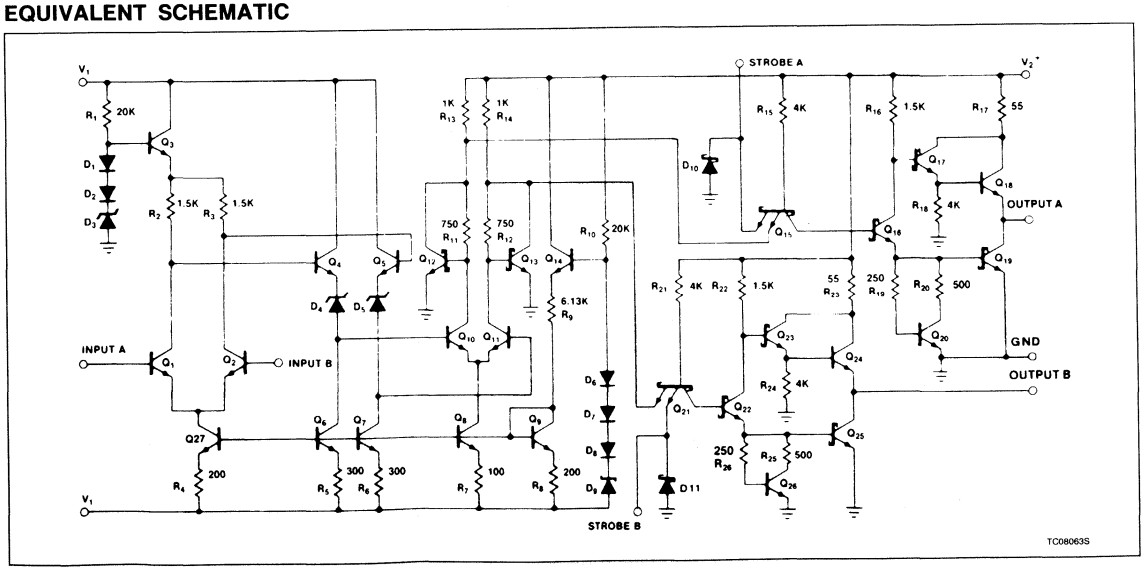
CD09730S

NOTE:
*Metal cans (H) not recommended for new designs.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE529N
14-Pin Cerdip	0 to +70°C	NE529F
14-Pin Cerdip	−55°C to +125°C	SE529F
14-Pin SO	0 to +70°C	NE529D
10-Lead Metal Can	0 to +70°C	NE529H
10-Lead Metal Can	−55°C to +125°C	SE529H

EQUIVALENT SCHEMATIC

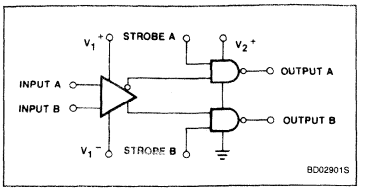


ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_1+	Positive supply voltage	+15	V
V_1-	Negative supply voltage	−15	V
V_2+	Gate supply voltage	+7	V
V_{OUT}	Output voltage	+7	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Input common mode voltage	±6	V
P_D	Maximum power dissipation[1] T_A = 25°C (still-air)		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range		
	NE529	0 to +70	°C
	SE529	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec max)	+300	°C

NOTE:
1. Derate above 25°C at the following rates:
   F package at 9.5mW/°C.
   N package at 11.5mW/°C.
   D package at 8.3mW/°C.

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $V_1+ = +10V$, $V_2+ = +5.0V$, $V_1- = -10V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE529			NE529			UNIT
			Min	Typ	Max	Min	Typ	Max	
Input characteristics									
V_{OS}	Input offset voltage @ 25°C				4			6	mV
	Over temperature range				6			10	mV
I_{BIAS}	Input bias current @ 25°C			5	12		5	20	μA
	Over temperature range	$V_{IN} = 0V$			36			50	μA
I_{OS}	Input offset current @ 25°C			2	3		2	5	μA
	Over temperature range	$V_{IN} = 0V$			9			15	μA
	Common-mode voltage range			0	±5		0	±5	V
Gate characteristics									
V_{OUT}	Output voltage								
	"1" state	$V_2+ = 4.75V$, $I_{SOURCE} = -1mA$	2.5	3.3		2.7	3.3		V
	"0" state	$V_2+ = 4.75V$, $I_{SINK} = 10mA$			0.5			0.5	V
	Strobe inputs								
	"0" Input current[1]	$V_2+ = 5.25V$, $V_{STROBE} = 0.5V$			-2			-2	mA
	"1" Input current @ 25°C[1]	$V_2+ = 5.25V$, $V_{STROBE} = 2.7V$			50			100	μA
	Over temperature range	$V_2+ = 5.25V$, $V_{STROBE} = 2.7V$			200			200	μA
	"0" input voltage	$V_2+ = 4.75V$			0.8			0.8	V
	"1" input voltage	$V_2+ = 4.75V$	2.0			2.0			V
I_{SC}	Short-circuit output current	$V_2+ = 5.25V$, $V_{OUT} = 0V$	-18		-70	-18		-70	mA
Power supply requirements									
	Supply voltage								
V_1+			5		10	5		10	V
V_1-			-6		-10	-6		-10	V
V_2+			4.5	5	5.5	4.75	5	5.25	V
	Supply current	$V_1+ = 10V$, $V_1- = -10V$, $V_2+ = 5.25V$							
I_1+		Over temp.			5			5	mA
I_1-		Over temp.			10			10	mA
I_2+		Over temp.			20			20	mA

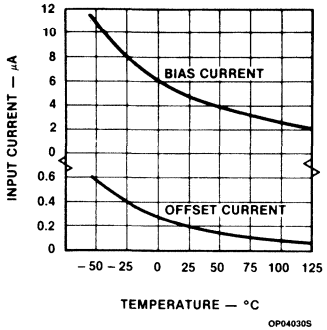
NOTES:
1. See logic function table.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ (See AC test circuit).

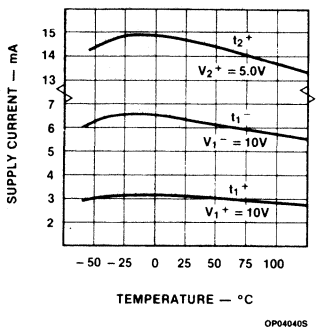
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_R	Transient response	$V_{IN} = \pm 100mV$ step				
	Propagation delay time					
t_{PLH}	Low-to-high			12	22	ns
t_{PHL}	High-to-low			10	20	ns
	Delay between output A and B			2	5	ns
	Strobe delay time					
t_{ON}	turn-on time			6		ns
t_{OFF}	turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS

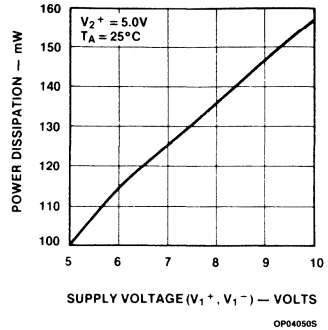
Input Currents vs Temperature



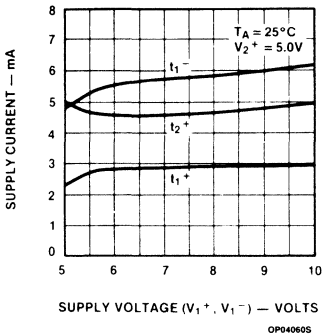
Supply Current vs Temperature



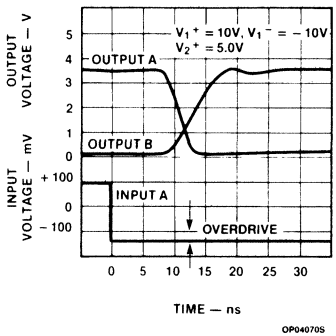
Power Dissipation vs Supply Voltage



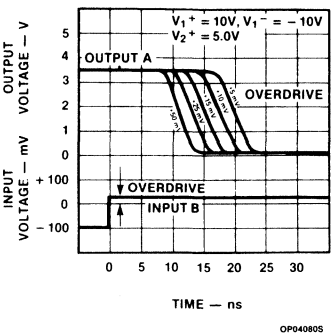
Supply Current vs Supply Voltage



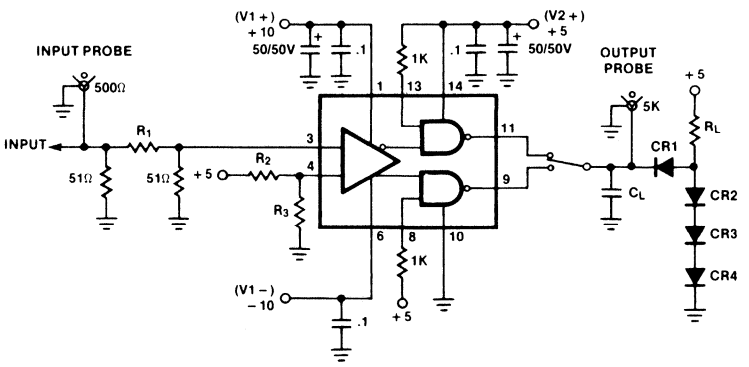
Output Propagation Delays



Response Time For Various Input Overdrives



RESPONSE TIME TEST CIRCUIT



NOTES:
CR1 – CR4 = IN914
R1 selected for 15:1 divider
R2, 3 selected for 100mV at Pin 4

Input
PRR = 1MHz
P_W = 50ns
$T_r = T_f$ = 2ns
Amplitude = 3.00V

Output
$R_L = 390Ω$
C_L = 25pF (including stray capacitance)

Voltage Comparator — NE/SE529

APPLICATIONS

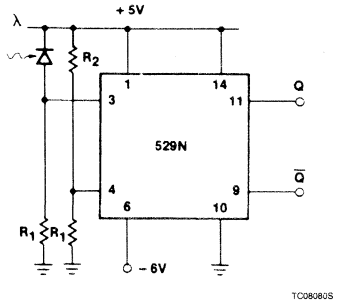
One of the main features of the device is that supply voltages (V+, V–) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V–) should always be at least 6V more than the ground terminal (pin 6). Input Common-Mode range should be limited to values of 2V less than the supply voltages (V+ and V–) up to a maximum of ±6V as supply voltages are increased.

It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

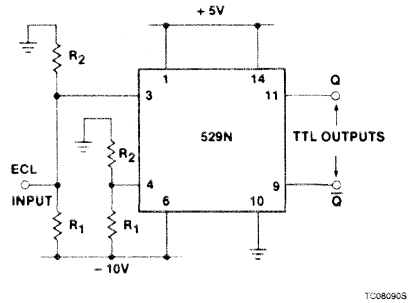
LOGIC FUNCTION

V_{ID} (A^+, B^-)	STROBE A	STROBE B	OUTPUT A	OUTPUT B
$V_{ID} \leq -V_{OS}$	H	X	L	H
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined	Undefined
$V_{ID} \geq V_{OS}$	X	H	H	L
X	L	L	H	H

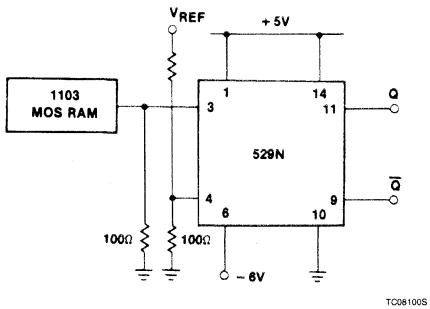
TYPICAL APPLICATIONS



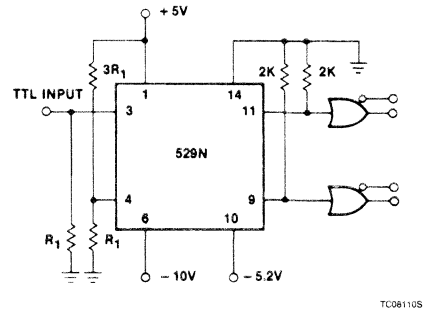
Photodiode Detector



ECL-to-TTL Interface



MOS Memory Sense AMP



TTL-to-ECL Interface

NE/SA/SE5105/A
Precision High-Speed Comparator With Latch

Product Specification

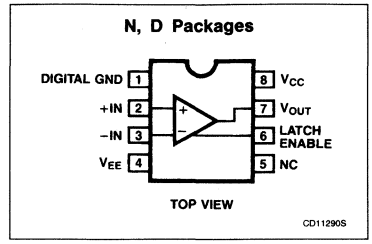
DESCRIPTION

The NE/SA/SE5105/A is a precision high-speed comparator ideally suited for applications requiring ultra-precision and speed. A typical application may be in a 12-bit successive approximation A/D converter. Input offset voltage is factory trimmed to typically 100μV (0.04 LSB for a 12-bit, 10V system); the 36ns response time (measured at 1.2mV overdrive), low input offset current, and high gain remain essentially constant over the entire operating temperature range. Thus, the same degree of precision and speed can be maintained over the specified temperature range. A latch function incorporated with the comparator allows added flexibility to the system designer. A TTL high input at the latch enable pin forces the output of the comparator to stay at its existing logical state irrespective of subsequent signal transitions at the input.

FEATURES

- **Precision input stage:**
  Input offset voltage 100μV
  Input offset current 3nA
- **Fast response time:**
  5mV overdrive 32ns
  1.2mV overdrive 36ns
- **High voltage gain 26,000V/V**
- **Low power dissipation 100mW**
- **TTL output capable of driving 10 TTL gates**
- **Latch function with TTL compatible input**

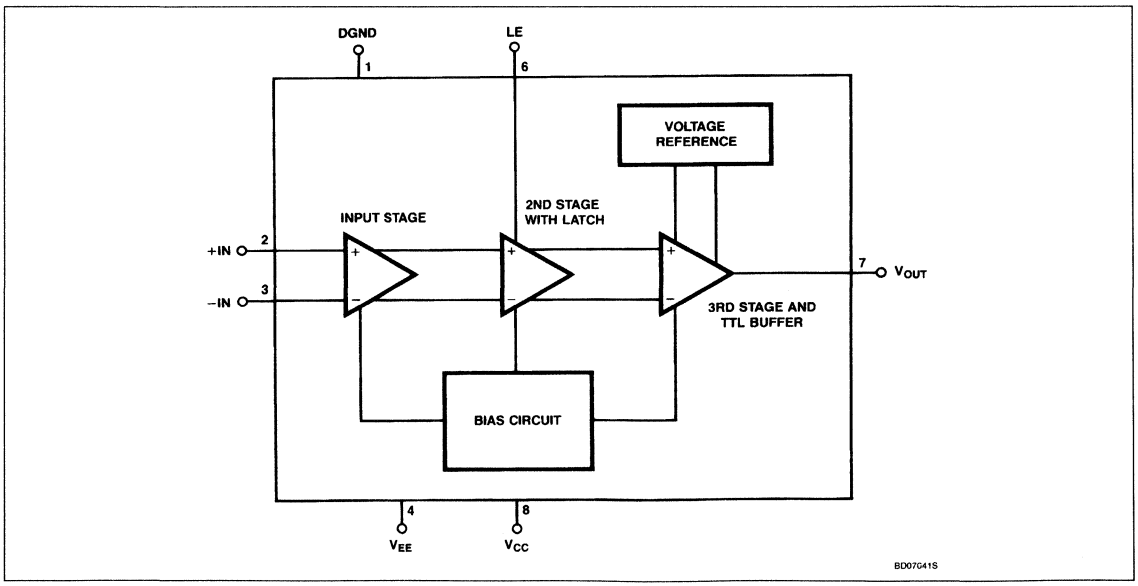
PIN CONFIGURATION



APPLICATIONS

- **High-speed, high-resolution successive approximation A/D converters**
- **Precision zero-crossing detectors**
- **Precision latching window comparators**
- **Fast latching ECL-to-TTL line translators**
- **Precision signal regenerators**

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5105AN
8-Pin Plastic DIP	0 to +70°C	NE5105N
8-Pin Plastic DIP	−40°C to +85°C	SA5105AN
8-Pin Plastic DIP	−40°C to +85°C	SA5105N
8-Pin Plastic SO	0 to +70°C	NE5105AD
8-Pin Plastic SO	0 to +70°C	NE5105D
8-Pin Plastic SO	−40°C to +85°C	SA5105AD
8-Pin Plastic SO	−40°C to +85°C	SA5105D
8-Pin Plastic DIP	−55°C to +125°C	SE5105AN
8-Pin Plastic DIP	−55°C to +125°C	SE5105N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	+6	V
V_{EE}	Power supply	−18	V
$P_{D\ MAX}$	Maximum power dissipation, T_A = 25°C (still-air)[1]		
	FE package	885	mW
	N package	1160	mW
	D package	780	mW
	Differential input voltage	±5	V
	LATCH ENABLE input voltage	V_{CC} to V_{EE}	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating temperature range		
	SE5105 (FE package)	−55 to +125	°C
	SA5105 (N and D package)	−40 to +85	°C
	NE5105 (N and D package)	0 to +70	°C
I_{SC}	Output short-circuit duration		
	To ground	Indefinite	
	To V_{CC}	1	Minute

NOTE:
1. Derate above 25°C, at the following rates:
   FE package at 6.75mW/°C.
   N package at 9.3mW/°C.
   D package at 6.2mW/°C.

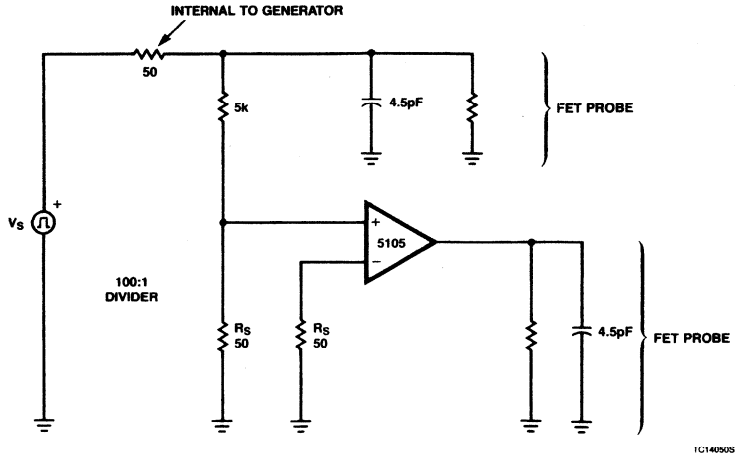
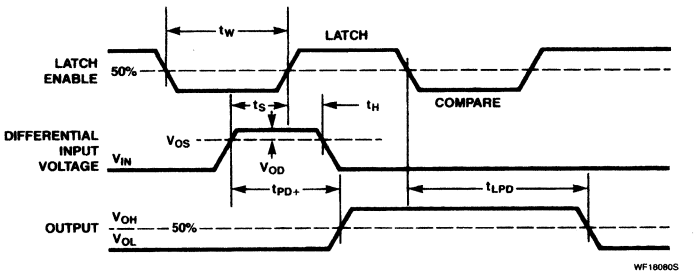


Figure 1. Test Setup for Delay Measurement

TIMING DIAGRAMS



SYMBOL	PARAMETER	CONDITIONS	MINIMUM LIMIT	UNIT
t_S	Setup time	V_{IN} = 100mV	28	ns
t_H	Hold time	V_{OD} = 5mV	10	
t_W	Latch pulse width		20	

DC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V$, $V_{EE} = -5V$, $T_A=25°C$; $V_{+IN} = V_{-IN} = 0V$ and Latch Enable grounded, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	5105A			5105			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 25\Omega$, $V_{CM} = 0V$ $R_S = 25\Omega$, $V_{CM} = \pm 3V$		100 140	250 400			600 750	μV
I_{OS}	Input offset current	$V_{LATCH} = V_{CC}$		3	20			40	nA
I_B	Input bias current	$V_{LATCH} = V_{CC}$		400	1200			1400	nA
A_{VO}	Voltage gain[1]		18	26		18	26		V/mV
CMVR	Input voltage range		± 3	± 3.3		± 3	± 3.3		V
CMRR	Common mode rejection ratio	$V_{CM} = \pm 3V$	86	99		84			dB
PSRR	Power supply rejection ratio	$V_{CC}/V_{EE} = \pm 4.5V$ to $\pm 5.5V$ $V_{CC} = +5V$ and $V_{EE} = -4.5V$ to $-15V$	78 86	94 104		78 84			dB dB
V_{OH}	Output high voltage	$V_{IN} \geq 10mV$, $I_{OH} = 0\mu A$ $V_{IN} \geq 10mV$, $I_{OH} = 400\mu A$	2.4 2.4	2.8 2.6		2.4 2.4	2.8 2.6		V V
V_{OL}	Output low voltage	$V_{IN} \leq 10mV$, $I_{OL} = 0\mu A$ $V_{IN} \leq 10mV$, $I_{OL} = 16mA$		0.2 0.3	0.4 0.4		0.2 0.3	0.4 0.4	V V
I_{CC}	Positive supply current	$V_O \leq 0.4V$, $I_O = 0\mu A$		11	14			16	mA
I_{EE}	Negative supply current	$V_O \leq 0.4V$, $I_O = 0\mu A$		9	12			14	mA
P_D	Power dissipation			100	130			150	mW
V_{LH}	Logic 1 at latch input		2			2			V
V_{LL}	Logic 0 at latch input				0.8			0.8	V
	Latch input current								
I_{LH}	Logic 1	$V_{LATCH} = 3V$		4	20		4	20	μA
I_{LL}	Logic 0	$V_{LATCH} = 0.8V$		1	5		1	5	μA
R_{IN}	Differential input resistance			1000			1000		MΩ

NOTE:
1. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +5V$, $V_{EE} = -5V$; $-55°C \leq T_A \leq +125°C$ for SE5105A/5105; $-40°C \leq T_A \leq +85°C$ for SA5105A/5105; and, $0°C \leq T_A \leq +70°C$ for NE5105A/5105. $V_{+IN} = V_{-IN} = 0V$ and Latch Enable grounded, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	5105A			5105			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 25\Omega$, $V_{CM} = 0V$ $R_S = 25\Omega$, $V_{CM} = \pm 3V$		0.25 0.3	0.6 0.75			1 1.2	mV
TC V_{OS}	Input offset voltage drift	$V_{CM} = 0V$		1.5	7.5			10	µV/°C
I_{OS}	Input offset current	$V_{LATCH} = V_{CC}$		4	25			60	nA
I_B	Input bias current	$V_{LATCH} = V_{CC}$		0.5	1.5			1.8	µA
A_{VO}	Voltage gain[1]		16	23		16	23		V/mV
CMVR	Input voltage range		±3	±3.2		±3	±3.2		V
CMRR	Common mode rejection ratio	$V_{CM} = \pm 3V$	83	93		80			dB
PSRR	Power supply rejection ratio	$V_{CC}/V_{EE} = \pm 4.5V$ to $\pm 5.5V$ $V_{CC} = +5V$ and $V_{EE} = -4.5V$ to $-15V$	75 75	94 94		72 72			dB dB
V_{OH}	Output high voltage	$V_{IN} \geq 10mV$, $I_{OH} = 0\mu A$ $V_{IN} \geq 10mV$, $I_{OH} = 320\mu A$	2.4 2.4			2.4 2.4			V V
V_{OL}	Output low voltage[2]	$V_{IN} \leq 10mV$, $I_{OL} = 9.6mA$ $V_{IN} \leq 10mV$, $I_{OL} = 12.8mA$		0.28 0.35	0.4 0.45		0.28 0.35	0.4 0.45	V V
I_{CC}	Positive supply current	$V_O < 0.4V$, $I_O = 0\mu A$		15	19			22	mA
I_{EE}	Negative supply current	$V_O \leq 0.4V$, $I_O = 0\mu A$		12	17			20	mA
P_D	Power dissipation			135	180			210	mW
V_{LH}	Logic 1 at latch input		2			2			V
V_{LL}	Logic 0 at latch input				0.8			0.8	V
	Latch input current								
I_{LH}	Logic 1	$V_{LATCH} = 3V$		6	20		6	20	µA
I_{LL}	Logic 0	$V_{LATCH} = 0.8V$		1	10		1	10	µA
R_{IN}	Differential input resistance			1000			1000		MΩ

NOTES:
1. Guaranteed by design.
2. $V_{OL} = 0.45V$ max at $T_A \leq -40°C$ and $I_{OL} = 12.8mA$.

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = +5V$; $V_{EE} = -5V$; $T_A = 25°C$ and Latch Enable grounded, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	5105A/5105			UNIT
			Min	Typ	Max	
t_{PD+}	Input to output high propagation delay[1, 2]	$V_{OD} = 1.2mV$ $V_{OD} = 5mV$		36 32	 50	ns ns
t_{PD-}	Input to output low propagation delay[1, 2]	$V_{OD} = 1.2mV$ $V_{OD} = 5mV$		34 32	 50	ns ns
t_{LPD}	Latch disable time[1, 2]			25	38	ns

NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs. See Timing Diagrams, Figures 3 and 4.

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = +5V$; $V_{EE} = -5V$; $-55°C \leq T_A \leq +125°C$ for SE5105A/5105; $-40°C \leq T_A \leq +85°C$ for SA5105/5105A, and, $0°C \leq T_A \leq +70°C$ for NE5105A/5105 Latch Enable grounded, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	5105A/5105			UNIT
			Min	Typ	Max	
t_{PD+}	Input to output high propagation delay[1, 2]	V_{OD} = 1.2mV V_{OD} = 5mV		50 45		ns ns
t_{PD-}	Input to output low propagation delay[1, 2]	V_{OD} = 1.2mV V_{OD} = 5mV		43 40		ns ns
t_{LPD}	Latch disable time[1, 2]			34		ns

NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs. See Timing Diagrams, Figures 3 and 4.

SYMBOLS AND DEFINITIONS

Common-Mode Rejection Ratio (CMRR)
The ratio of the change in common-mode voltage to the corresponding change in V_{OS}. CMRR is expressed in dB, CMRR = 20 log ($\Delta CMV/\Delta V_{OS}$).

Differential Input Resistance (R_{IN})
Resistance looking into either input terminal with the other referred to a specified voltage.

Input Bias Current (I_{BIAS})
The current into either input terminal with both inputs referred to a specified voltage.

Input Offset Current (I_{OS})
The difference between the two input bias currents with both inputs referred to a specified voltage

Input Offset Voltage (V_{OS})
The minimum potential difference required between the input terminals to force the output to a specified voltage.

Input Offset Voltage Drift (TCV_{OS})
The ratio of the change in V_{OS} to the change in temperature as that temperature deviates from a +25°C ambient.

Input to Output Propagation Delay (t_{PD+} and t_{PD-})
The propagation delay measured from the time the input signal crosses V_{OS} to the 50% transition point of the output signal. Delay is measured with a specified input step size (V_{IN}) and overdrive (V_{OD}).

Input Voltage Range (CMVR)
The range of common-mode voltage at the input for which operation within specifications is guaranteed.

Latch Disable Propagation Delay (t_{LPD})
The propagation delay measured between the 50% transition points of the LATCH ENABLE signal falling edge and the output signal transition point.

Latch Hold Time (t_H)
The minimum time after the positive transition of the LATCH ENABLE signal that the input signal must remain unchanged in order to be acquired and held at the output. Hold time is measured from the 50% transition point of the LATCH ENABLE signal to the point where comparator input signal crosses V_{OS}.

Latch Pulse Width (t_W)
The minimum time that the LATCH ENABLE signal must be low in order to acquire and subsequently hold the input signal change. Pulse width is measured between the 50% transition points of the falling and rising edges of the latch pulse.

Latch Setup Time (t_S)
The minimum time before the positive transition of the LATCH ENABLE signal that an input signal change must be present in order to be acquired and held at the output. Setup time is measured from the point the input signal crosses V_{OS} to the 50% transition point of the LATCH ENABLE signal.

Output High Current (I_{OH})
The current that the comparator output can source at a specified output voltage and input overdrive.

Output High Voltage (V_{OH})
The high output voltage with a specified source current and input overdrive.

Output Low Voltage (V_{OL})
The low output voltage with a specified sink current and input overdrive.

Output Sink Current (I_{OL})
The current that the comparator output can sink at a specified output voltage and input overdrive.

Overdrive (V_{OD})
The applied input differential voltage in excess of input offset voltage (V_{OS}).

Power Supply Rejection Ratio (PSRR)
The ratio of the change in input offset voltage to the specified change in power supply voltage.

Voltage Gain (A_V)
The ratio of the change in output voltage (over a specified range) to the change in differential input voltage.

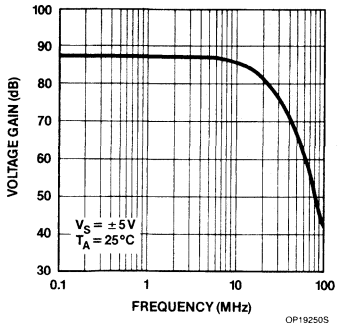
APPLYING THE NE/SA/SE5105/A

PC Board Layout

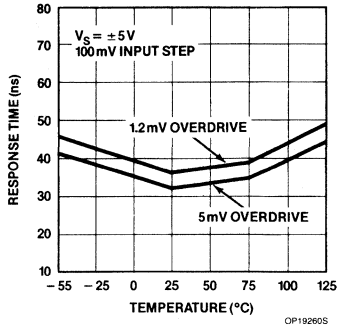
As with any high-speed circuit, layout of the PC board becomes critical for optimum performance. The supplies should be bypassed with good high frequency capacitors mounted as close to the IC as possible. A combination of high frequency ceramic and tantalum capacitors provide adequate suppression of transients on the supply lines. Since the comparator is an uncompensated amplifier with high gain, even a small amount of feedback from the output to the input can cause oscillation. A poor layout of the PC board not only increases the uncertainty region (due to oscillation) of the comparator, but also introduces hysteresis. Use of ground planes is essential since ground planes not only minimize inductance, but also reduce stray feedback capacitances by referring them to ground. Separate analog and digital ground planes should be used; the inputs are referred to the analog ground while the supplies and output are referred to the digital ground (Pin 1). Furthermore, the analog and digital ground planes should only meet at one point. Comparator output and input pins should be isolated from each other along with the traces from the respective pins. Stray capacitance from the IC pins to ground can be minimized by keeping the lead lengths and traces as short as possible.

TYPICAL PERFORMANCE CHARACTERISTICS

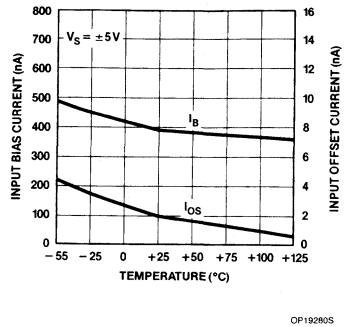
Voltage Gain vs Frequency



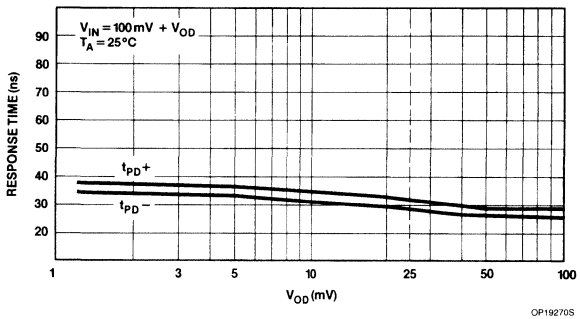
Response Time vs Temperature



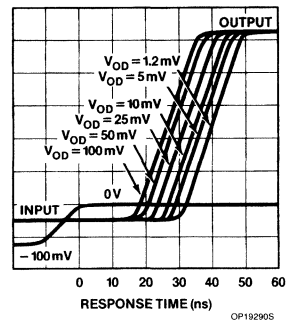
Input Current vs Temperature



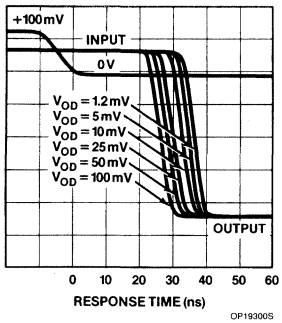
Response Time vs Overdrive Voltage



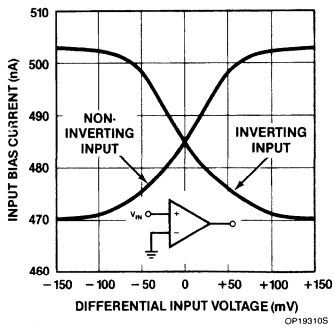
$t_{PD}+$ Response Time



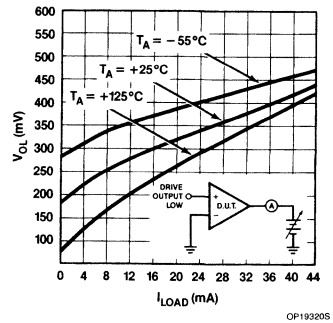
$t_{PD}-$ Response Time



Input Bias Current vs Differential Input Voltage

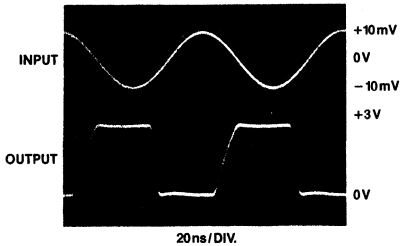


V_{SAT} vs Load Current



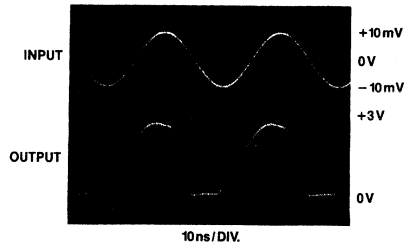
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Response to 10MHz Sine Wave



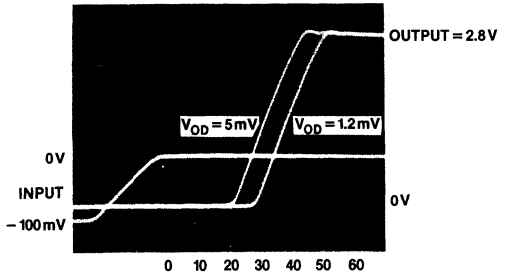
WF21060S

Response to 25MHz Sine Wave



WF21070S

Response Time to 5mV and 1.2mV Overdrive



WF21080S

AN116
Applications for the NE521/522/527/529

Application Note

COMPARATORS

Voltage comparators are high gain differential input-logic output devices. They are specifically designed for open-loop operation with a minimum of delay time. Although variations of the comparator are used in a host of applications, all uses depend upon the basic transfer function. Device operation is simply a change of output voltage dependent upon whether the signal input is above or below the threshold input.

Comparator inputs are customarily marked with plus or minus signs to indicate their polarity. For example, the circuit of Figure 1 produces a logic 1 level when the non-inverting input is more positive than the reference voltage.

DEFINITIONS

Many similarities exist between operational amplifiers and the amplifier section of voltage comparators. In fact, op amps can be used to implement the comparator function at low frequencies.

Thus, the characteristic definitions presented here are similar to those reviewed for op amps.

Input Offset Voltage

As with operational amplifiers, the non-ideal comparator possesses some offset voltage. The definition differs slightly in that the output structure of comparators is digital rather than linear. Hence, input offset voltage is defined for comparators as the DC voltage required at the input to force the output to the logic threshold of ensuing devices (1.2V for TTL).

Input Offset Current

Imbalances of input bias current arise from small variances of the junction geometry of the differential input amplifier. As for op amps, the imbalance is referred to as input offset current.

Bias Current

As with op amps the input structure of comparators is usually a differential bipolar stage. Input bias current is the average of the two input currents.

Common-Mode Range

When specifying voltage comparators, one of the key parameters is common-mode range, which is defined as the range of voltages over which both inputs can be varied simultaneously without abnormal output voltage transitions or device degradation. This parameter must be kept uppermost in the designer's mind because the reference and signal voltages become common-mode signals at threshold. All ranges of input signals thus must be within the common-mode range of the input amplifier.

Voltage Gain

Specifications of voltage gain refer to the overall gain of the device, the bulk of which occurs in the amplifier section.

In general, higher gains would be advantageous for resolving smaller input signals. Of course, the propagation delay suffers due to the more severe saturation of the transistors. Typical gains for TTL output devices are set for 5000V/V. This gain provides 5V of output swing with 1mV input signal change for reasonable accuracy, but does not contribute severely to the overload recovery delay.

Propagation Delay

Voltage comparisons of analog signals with a reference voltage usually require that the operation take as little time as possible. Long delays in the comparator cause a pulse position error at the output since the analog signal in the meantime has changed value. At low frequencies the delay is of small consequence, but at higher frequencies, transit time becomes intolerable. Design of voltage comparator devices includes, as a prime goal, the minimizing of transit times.

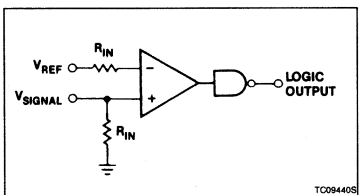


Figure 1. Basic Comparator Circuit

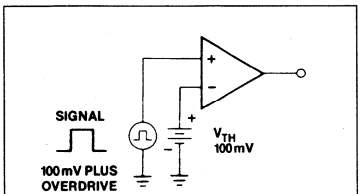


Figure 2. Propagation Delay Test Setup

Propagation delay testing is done under worst-case conditions. The recovery from saturation varies, depending upon the initial state of the amplifier and the overdrive. Worst-case conditions begin by applying a 100mV signal on the reference terminal. With no signal applied, the amplifier is in saturation in one direction. A step input pulse on the signal line of 100mV $\pm V_{OS}$ will bring the amplifier to a threshold level. Propagation delay at this point is undefined since the output has not switched.

To attain output switching, a small overdrive is necessary. Propagation delay is tested in a configuration such as Figure 2. The input is a step function of 100mV plus a specified excess or overdrive signal. This causes the amplifier to be exercised from saturation in one direction to saturation in the other for worst-case propagation delay. Note that larger overdrive reduces delay time as can be seen in Figure 3. An overdrive of 5mV causes 12ns delay, whereas a 100mV overdrive improves transit time to only 6ns.

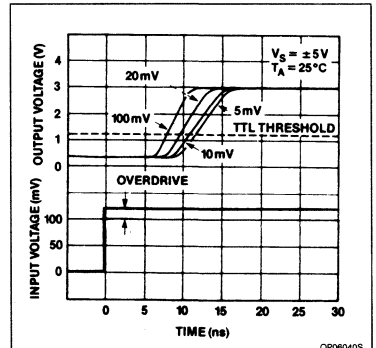


Figure 3. Response Time for NE/SE521 Comparator for Various Input Overdrives

If the measurement were made without initial saturation (less than 100mV/V threshold) the delay time would be less, due to the decreased storage times of unsaturated transistors.

STATE-OF-THE-ART

Comparator design has always been optimized for four basic parameters. They are:

1. High Speed
2. Wide Input Voltage Range
3. Low Input Current
4. Good Resolution

Unfortunately, these four parameters are not compatible. For instance, gain and input current can be improved by using thinner diffusions for higher beta, but only at the expense of input voltage range. Higher gain also means higher saturation for an increase in delay time. So it becomes obvious that older comparators such as the 710 were designed with the best compromises in mind using standard processing.

One method of improving overall response adds gold doping to the processing flow. The gold dopant causes a decrease in minority carrier lifetime which aids the recombination process and shortens the saturation recovery time. Unfortunately, the transistor beta is adversely affected by gold, causing slightly higher bias and offset currents.

It was not until the advent of the Schottky clamp that a vast improvement in speed without input degradation was possible. A very familiar term in the semiconductor industry, the Schottky barrier diode's (SBD) location is illustrated in Figure 4.

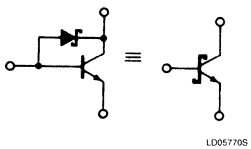


Figure 4. Schottky Clamped Transistor

The Schottky clamped transistor is formed by paralleling the Schottky diode with the base-collector junction of the NPN transistor. Without the clamp, as base drive is increased the collector voltage falls until hard saturation occurs. At this point the collector voltage is very near the emitter voltage, and stored charges in the junctions causes slow recovery from saturation after base drive has been removed. The forward voltage drop of the Schottky diode is 0.4V — less than the forward drop of silicon diodes. This difference in forward drop is used by placing the diode across the transistor base-collector junction.

The Schottky diode becomes forward-biased when the collector voltage falls 0.4V below the base voltage. Excess base drive is then shunted into the collector circuit, prohibiting the transistor from reaching classic saturation. With almost no stored charge in either the SBD or the transistor, there is a large reduction in storage time. Thus, transistor switching time is significantly reduced.

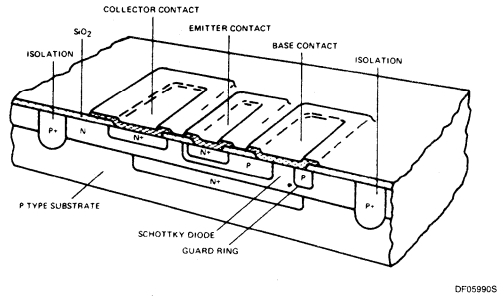


Figure 5. Schottky Clamped Transistor Geometry

A cross sectional area of the Schottky diode is shown in Figure 5.

DEVICE	PROP DELAY (ns)	V_{OS} (mV)	I_{OS} (μA)	I_{BIAS} (μA)	GAIN	CMR (V)	BENEFITS
NE521	12	7.5	5	20	5000	±3	Dual, very fast, standard supplies TTL compatible, individual & common strobe.
NE522	15	7.5	5	20	5000	±3	Same as NE521 plus open-collector outputs for additional decoding.
NE527	26	6	0.75	2	5000	±6	Fast, very low input current, differential outputs, flexible surplus wide common-mode range.
NE529	22	6	5	20	5000	±6	Same as NE527 but with faster response.
LM311	200	7.5	0.05	0.25	200k	±30	High common-mode input range, ±5V to ±15V supply, strobe input, open-collector output.
LM319	80	8	0.2	1.2	40k	±5	Low input bias, dual, +5V to ±15V supply, open-collector output.
LM339	1300	2	0.05	0.25	200k	V+ −1.5V	High common-mode input range, low input bias, quad, +5V to ±15V supply, open-collector output.
LM393	1300	2	0.05	0.25	200k	V+ −1.5V	Same as LM339 but dual.

NOTE:
Parameters are based on min/max limits at 25°C as defined in the individual data sheet.

Figure 6. Comparator Selection Guide

Applications for the NE521/522/527/529

COMPARING THE COMPARATORS

Presently available comparator ICs range from the ultra fast SE/NE521 to the general purpose comparator fashioned from an inexpensive op amp. Selection of the device depends upon the application in which it will be used. Speed of conversion is often of primary importance to minimize pulse position errors of high frequency signals. At other times the requirements are much less stringent, allowing the use of a general purpose comparator.

A handy reference guide to the major parameters is summarized in Figure 6. The necessary parameters can be chosen to select the proper device.

A general description of the comparator devices is included here to familiarize the user with available devices and their advantages.

NE/SE521/522 Comparators

Processed with state-of-the-art Schottky barrier diodes, the NE521/522 series devices provide good input characteristics while providing the fastest analog-to-TTL conversion to date. Total delay from input to output is typically 6ns with a guaranteed speed of 12ns. Additional features of this device include the dual configuration and individual output strobes to simplify system logic. The NE522, although sacrificing some speed, features open-collector outputs for party line or wired-OR configurations for additional system flexibility.

NE/SE527 Comparator

Featuring Darlington inputs for very low bias current, the NE527 is generically related to the NE529 comparator. Emitter-follower inputs to the differential amplifier are used to trade better input parameters for slightly less speed. As Figure 6 shows, a factor of 10 improvement in I_{BIAS} is gained with a propagation delay increase of only 4ns maximum.

NE529 Comparator

The NE529 is manufactured using Schottky technology. Although a few nanoseconds slower than the NE521, the NE529 features variable supplies from ± 5 to ± 10V with a high common-mode range of ± 6V. Both the NE527 and NE529 Schottky comparators boast complementary logic outputs with output A being in phase with input A. In addition, the supplies of both the NE527 and NE529 may be non-symmetrical to produce a desired shift in the common-mode range.

This technique is illustrated by the ECL-to-TTL and TTL-to-ECL transistor of Figures 16 and 17, respectively. The only major requirement of the supplies is that the negative supply be at least 5V more negative than the ground terminal of the gate. This is necessary to insure that the internal bias arrangement has sufficient voltage to operate normally.

APPLICATIONS

Today's state-of-the-art ultra high-speed comparators are capable of making logic decisions in less than 10ns. They are easily applied and possess good input and power supply noise rejection. As with all linear ICs, however, some preliminary steps should be taken in their use.

GENERAL PRECAUTIONS

Layout

The comparator is capable of resolving sub-millivolt signals. To prevent unwanted signals from appearing at signal ports, good physical layout is required. For any high-speed design, ground planes should be used to guard against ground loops and other sources of spurious signals. At high frequencies, hidden signal paths become dominant. Distributed capacitance is a particular nuisance. If care is not taken to isolate output from input, distributed capacitance can couple a few millivolts into the input, causing oscillation.

Another source of spurious signals is ground current. Input structures are relatively high impedance while the gate structures of comparators run with large signal and ground currents. If this gate ground current is allowed to pass near the input signal path, the small impedances of the ground circuit will cause millivolt changes in reference or signal voltages producing errors, sustained oscillation, ringing, or excessive V_{OS}. A ground plane arranged such that output currents do not flow near input areas is highly recommended.

Power Supplies

Another general precaution that should always be exercised is power supply bypassing. As mentioned, the name of the game is speed. Very high-speed gates are used to produce the desired output logic levels. Maximizing response speed also requires higher current levels, giving rise to power supply noise. For this reason, good power supply bypassing very close to the device itself is always mandatory. A tantalum capacitor of 1 to 10μF in parallel with 500 to 1000pF will prove effective in most cases. Lead lengths should be as short as physically possible to preserve low impedances at high frequency.

Unused Inputs

Some currently available comparators such as the NE521 and NE522 are dual devices. Most often both sections of these devices will be utilized. Should a system utilize one device, the unused inputs should be biased in a known condition. The high gain-bandwidth may otherwise cause oscillations in the unused comparator section. A low impedance should be provided from both unused inputs to ground. A resistor of relatively high impedance may then be used to supply a differential input on the order of 100mV to insure the comparator assumes a known state.

If the inverting input is tied to the positive differential voltage the gate output will be low. The strobe inputs then provide a means of utilizing the Schottky gate for other system logic functions.

If the strobe inputs are not used, they should be connected to the output of a logic gate that is always high, or to the +5V supply through a 5 to 10kΩ resistor. They should never be tied directly to the +5V supply as the relatively minor spiking on the supply may damage these inputs.

Common-Mode Signals

Manufacturers specify the maximum voltage range over which the inputs may be taken. In addition, the maximum differential voltage that may be safely applied to the inputs is specified. In the case of the NE529 comparator, the differential voltage is restricted to less than ± 5V, with a common-mode of ± 6V. That these two quantities interact cannot be overlooked. For instance, with both inputs at ± 4V the common-mode restriction is satisfied. If V_{REF} is now left at +4V the signal input may not be taken more than 1V below ground because the differential signal becomes 5V.

It is important to observe this maximum rating since exceeding the differential input voltage limit and drawing excessive current in breaking down the emitter-base junctions of the input transistors could cause gross degradation in the input offset current and bias current parameters.

It is also important to note that response time is specified for a common-mode voltage of zero and may degrade when the common-mode voltage approaches the common-mode specification limits.

Exceeding the absolute maximum positive input voltage limit of the device will saturate the input transistor and possibly cause damage through excessive current. However, even if the current is limited to a reasonable value so that the device is not damaged, erratic operation can result.

Input Impedance

The differential bias and offset currents of comparators are minimized by design. As was pointed out for op amps, the input resistance seen by both inputs should be equal. This reduces to a minimum the contribution of offset current to threshold error. Unbalanced input impedance also adds to the offset error due to the difference in voltage drop across the input resistances.

Applications for the NE521/522/527/529

BASIC APPLICATIONS

The basic comparator circuit and its transfer function were presented by Figure 1.

When the input exceeds the reference voltage, the output switches either positive or negative, depending on how the inputs are connected.

The vast majority of specific applications involve only the basic configuration with a change of reference voltage. A-to-D converters are realized by applying the signal to one terminal and the voltage derived from a ladder network to the other. Limit detectors are likewise made from only the very basic circuit. Both are only a small deviation from the basic level detector.

Hysteresis

Normally saturated high or low, the amplifiers used in voltage comparators are seldom held in their threshold region.

They possess high gain-bandwidth products and are not compensated to preserve switching speed. Therefore, if the compared voltages remain at or near the threshoid for long periods of time, the comparator may oscillate or respond to noise pulses. For instance, this is a common problem with successive approximation D/A converters where the differential voltage seen by the comparator becomes successively smaller until noise signals cause indecision. To avoid this oscillation in the linear range, hysteresis can be employed from output to input. Figure 7 defines the arrangement. Both positive and negative feedback is provided by R_{IN} and R_F.

Hysteresis occurs because a small portion of the "one" level output voltage is fed back in phase and added to the input signal. This feedback aids the signal in crossing the threshold. When the signal returns to the threshold, the positive feedback must be overcome by the signal before switching can occur. The switching process is then assured and oscillations cannot occur. The threshold "dead zone" created by this method, illustrated in Figure 8, prevents output chatter with signals having slow and erratic zero crossings.

As shown in Figure 7, the voltage feedback is calculated from the expression:

$$V_{HYST} = \frac{E_{OUT} \cdot R_{IN}}{R_{IN} + R_F}$$

where E_{OUT} is the gate high output voltage.

The hysteresis voltage is bounded by the common-mode range and the ability of the gate to source the current required by the feedback network. If symmetrical hysteresis is desired, an additional inverting gate is required if the comparator does not have differential outputs. The NE527 and NE529 devices provide inverted signals from differential outputs while the NE521 and NE522 devices will require the inverter. Care should be taken in the selection of the inverter that propagation delay is minimum, especially for very high-speed comparators such as the NE521.

Line Receiver

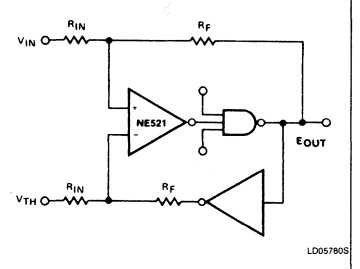
Retrieving signals which have been transmitted over long cables in the presence of high electrical noise is a perfect application for differential comparators. Such systems as automated production lines and large computer systems must transmit high frequency digital signals over long distances.

If the twisted-pair of the system is driven differentially from ground, the signals can be reclaimed easily via a differential line receiver.

Since the electrical noise imposed upon a pair of wires takes the form of a common-mode signal, the very high common-mode rejection of the NE521/522 makes the unit ideal for differential line receivers. Figure 9 depicts the simple schematic arrangement. The NE521 is used as a differential amplifier having a logic level output. Because common-mode signals are rejected, noise on the cable disappears and only the desired differential signal remains. Figure 10 illustrates the NE521 response to the 200mV$_{P-P}$ 10MHz differential signal. In Figure 11 the same signal has been buried in 5V$_{P-P}$ of 1HMz common-mode "noise."

The circuit suffers no degradation of signal. If desired, several NE522 comparators may be "wire-ORed," or a latched output can be built as shown in Figure 9.

The NE521 and NE529 comparators have the advantage of wider bandwidth to permit higher data rates.



NOTE: $V_{HYST} = \frac{E_{OUT} \cdot R_{IN}}{R_{IN} + R_F}$

Figure 7. Level Detector With Hysteresis

Double-Ended Limit (Window) Detector

Many system designs require that it be known when a signal level lies between two limits. This function is easily accomplished with a single NE522 package. The schematic and transfer curve of the circuit is shown in Figure 12.

Each half of the NE522 is referenced to the desired upper or lower voltage limit producing the desired transfer curve shown. Taking advantage of the dual configuration and the open-collectors of the NE522 minimizes external components and connections.

Crystal Oscillator

Any device with a reasonable gain can be made to oscillate by applying positive feedback in controlled amounts. The NE521 will lend itself to crystal control easily, provided the crystal is used in its fundamental mode. Figure 13 shows a typical oscillator circuit.

The crystal is operated in its series-resonant mode, providing the necessary feedback through the capacitor to the input of the NE521. The resistor R_{ADJ} is used to control the amount of feedback for symmetry. Oscillations will start whenever a circuit disturbance such as turning on the power supplies occurs. The NE521 will oscillate up to 70MHz. However, crystals with frequencies higher than about 20MHz are usually operated in one of their overtones. To build an oscillator for a specific overtone requires tuned circuits in addition to the crystal to provide the necessary mode suppression. If the spurious modes are not tuned out, the crystal will oscillate at the fundamental frequency. Higher frequency oscillators could be realized using input and output mode suppression or tuning. The NE522 is especially desirable since the open-collector topology allows the output to be collector-tuned readily.

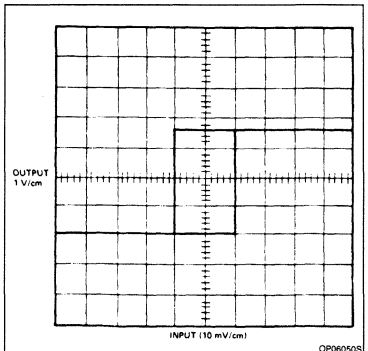


Figure 8. 0V Level Detector With ± 10mV Hysteresis

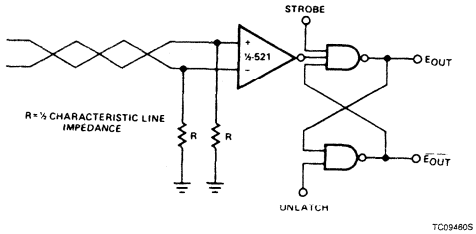


Figure 9. Line Receiver

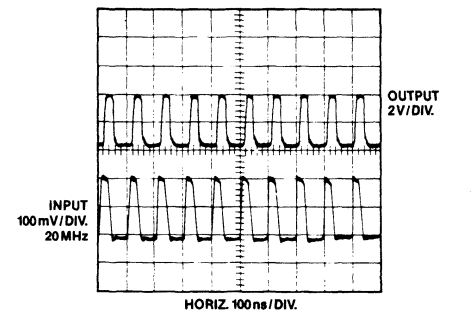


Figure 10. Line Receiver Response

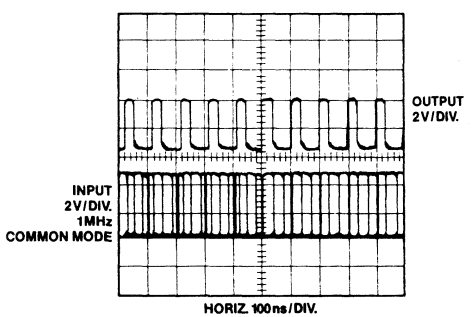


Figure 11. Response During Common-Mode Noise

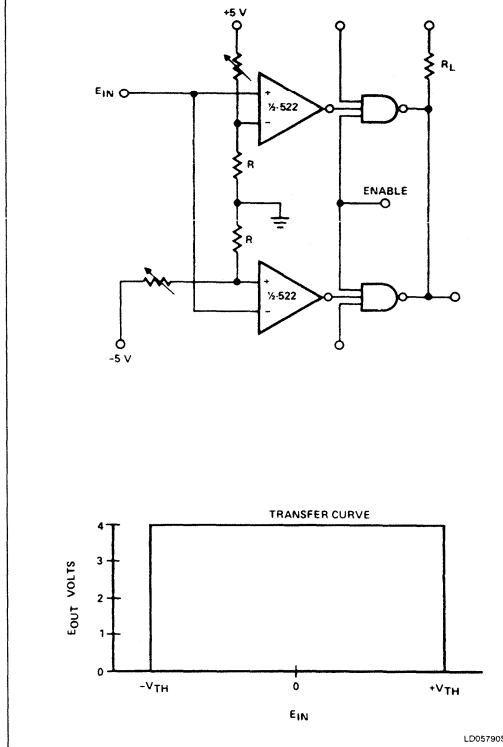


Figure 12. Double-Ended Limit Detector

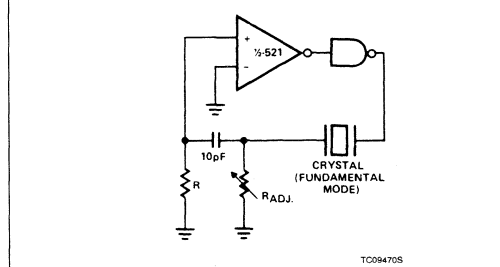


Figure 13. Crystal Oscillator

Analog-to-Digital Converter

There are many types of A-to-D converter designs, each having its own merits. However, where speed of conversion is of prime interest, the multi-threshold conversion type is used exclusively. It is apparent from Figure 14 that the conversion speed of this design is the sum of the delay through the comparator and the decoding gates.

The sacrifices which must be made to obtain speed are the number of components, bit accuracy and cost. The number of comparators needed for an N-bit converter is 2n-1. Although the NE521 provides two comparators per package, the length of parallel converters is usually limited to less than 4 bits. Accuracy of multi-threshold A-D converters also suffers since the integrity of each bit is dependent upon comparator threshold accuracy.

The implementation of a 3-bit parallel A/D converter is shown in Figure 15 with a 3-bit digital equivalent of an analog input shown in Figure 14.

Reference voltages for each bit are developed from a precision resistor ladder network. Values of R and 2R are chosen so that the threshold is one half of the least significant bit. This assures maximum accuracy of $\pm \frac{1}{2}$ bit.

It is apparent from the schematic that the individual strobe line and duality features of the NE521 have greatly reduced the cost and complexity of the design. The speed of the converter is graphically illustrated by the photo of Figure 14. All 3-bit outputs have settled and are true a mere 15ns after the input step of 3V has arrived. The output is usually strobed into a register only after a certain time has elapsed to insure that all data has arrived.

Logic Interface

During the design of the NE527 and NE529 devices, particular attention was paid to the biasing network so that balanced supplies need not be provided. For example, if the "ground" terminal is set at −5.2V and the other supplies are adjusted accordingly, the output logic 1 state will be at −1.5V and logic 0 will be at −5.0V. With this freedom of power supply voltage, the user may adjust the output swings to match the desired logic levels even if that logic is other than TTL levels.

ECL-to-TTL Interface

Emitter-coupled logic is very popular due to its speed. Systems are often built around standard TTL logic with those portions requiring higher speed being implemented with emitter-coupled logic. As soon as such a decision is made the problem of interfacing TTL-to-ECL logic levels is encountered.

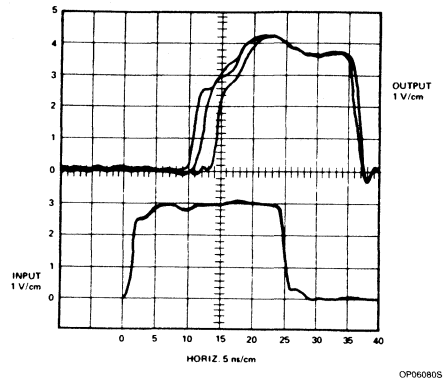


Figure 14. Parallel A/D Response

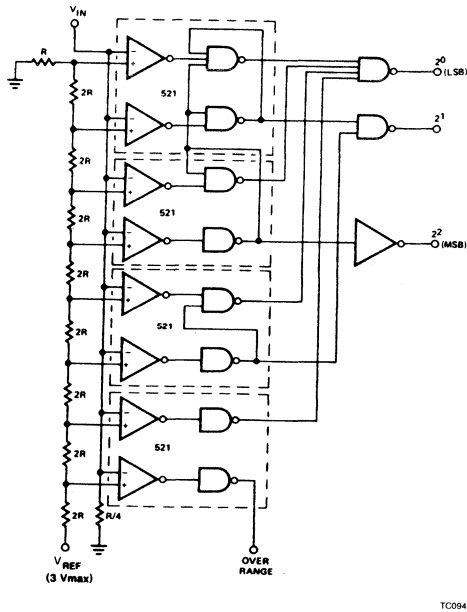


Figure 15. 3-Bit Parallel A/D Converter

The standard logic output swings of ECL are −0.8V to −1.8V at room temperature. Converting these signals to TTL levels is accomplished simply by using the basic voltage comparator circuit with slight modifications. Figure 16 reveals that the power supplies have been shifted in order to shift the common-mode range more negative. This insures that the common-mode range is not exceeded by the logic inputs. Since ECL is extremely fast, the NE529 is usually selected because of its superior speed so that a minimum of time is lost in translation.

TTL-to-ECL INTERFACE

Operating in the reverse, TTL levels can also be converted to ECL levels by the NE529. Again the NE529 is selected as the fastest converter with the necessary power supply flexibility to accomplish the level shifting with a minimum of effort and cost.

A check of output voltage for the NE529 reveals that the voltage is slightly less than

required by the ECL logic for fast switching. R2 and the diode of Figure 17 raises the gate supply voltage and therefore the NE529 output voltage by 0.7, sufficient to guarantee fast switching of the translator. Resistive pull-up from the NE529 output to V_{CC} can also be used with the gate supply grounded. This method is dependent upon RC time constants of distributed capacitance and is therefore much slower.

Photo Diode Detector

Responding to the presence or absence of light, the photo diode increases or decreases the current through it. Detecting the changes becomes a matter of converting light and dark currents to voltage across a resistor as shown in Figure 18. R1 is selected to be large enough to generate detectable differences between light and dark conditions. Once the signal levels are defined by R1 and the diode characteristics, the average between light and dark signals is used for V reference and is produced by the resistive divider consisting of R1 and R2. The comparator then produces an output dependent upon the presence or absence of light upon the diode.

SENSE AMPLIFIERS

Closely related to the comparator is the sense amplifier. Signals derived from the many sources, such as transducers, are not of sufficient amplitude to be compatible with subsequent logic. It then becomes necessary to amplify and convert the signal to TTL levels, which is the responsibility of the sense amplifier.

Some transducers produce an output current. It remains, then, for the user to convert these currents to TTL levels. A terminating resistor from the drain to ground provides a voltage output proportional to the current and the resistor size. Larger signals can be produced by larger resistors; but in practice, resistors larger than 1kΩ are avoided because of increasing access time. Distributed capacitance forms a time constant with this output resistance causing slow rise and fall times when the resistor is large, adding to the access time.

Virtually any voltage comparator or sense amplifier can be used. Since total time is the sum of all delays, the sense amplifier is most often the fastest available. Signetics comparators NE521 and NE522 are ideal in this application because of low input offset voltages and very fast response. Using these Schottky clamped comparators significantly reduces the total cycle time of the memory.

Design of the sense amplifier network depends upon the transducer used and the input characteristics of the sense amplifier. The significant specifications are given in Table 1.

Consideration must first be given to the differential input voltage requirements of the sense amplifier. The required reference voltage is calculated from the relationship:

$$V_{REF} \leqslant (I_T - I_B)R1 - V_{DIFF}$$

Where I_T is the transducer output current, I_B is sense amplifier bias current and V_{DIFF} is minimum differential voltage to switch the sense amplifier.

In large systems, noise coupled into the sense lines by stray capacitance can be very troublesome. Judicious layout patterns with sense lines as short as possible will help, but will not always be sufficient. One method of eliminating noise is to use a balance sense line as shown in Figure 19.

A dummy line should be run parallel to the actual sense line in as close proximity as possible. One end is connected to the sense amplifier at the V_{REF} point while the other end is left open. The normal sense line is connected as usual. Electrical noise imposed upon the pair of sense lines takes the form of a common-mode signal and will be rejected by the sense amplifier. Signal currents in the sense line, on the other hand, form differential signals at the sense amp, causing the output to switch.

Table 1. Important Sense Amplifier Parameters

DEVICE	V_{OS} (mV)	I_B (μA)	$V_{IN\ (MIN)}$ (mV)	SPEED (ns) (V_{IN} = 100mV)	GAIN
521	10	40	15	12	5000
522	10	40	15	15	5000

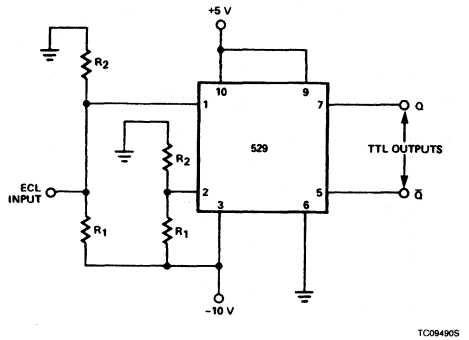


Figure 16. ECL-to-TTL Translator

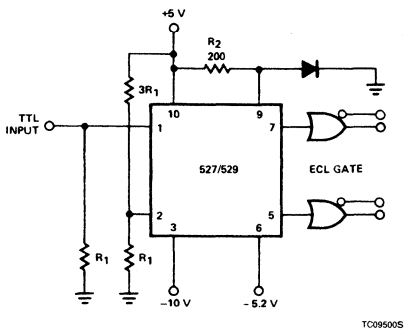


Figure 17. TTL-to-ECL Translator

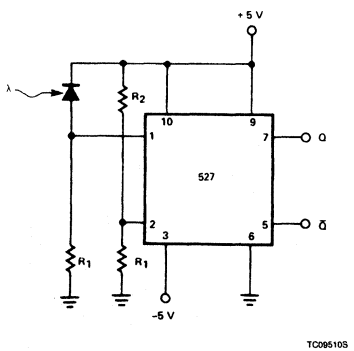


Figure 18. Photo Diode Detector

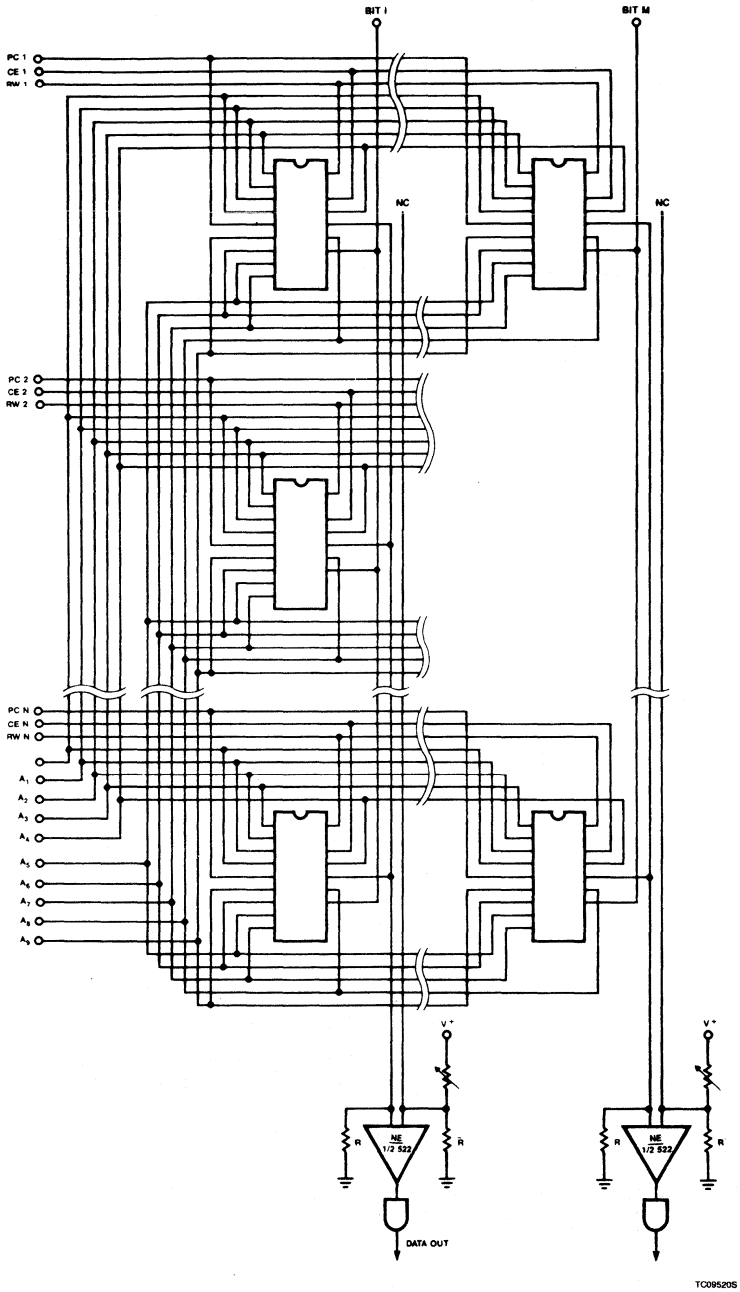


Figure 19. Balanced Sense Line to Reduce Noise

AN1161
12-Bit A/D Converter Using the NE5105 Comparator

Application Note

INTRODUCTION

Comparators play an important role in an analog to digital conversion system. The accuracy and speed of the comparator determine the overall performance of an A/D system. Ultraprecision comparators require low input offset voltage, low input offset current, and high gain for high accuracy. In a successive approximation type A/D system, the propagation delay through the comparator should be kept to a minimum value for fast conversion time.

A typical n-bit successive approximation type A/D system is shown in Figure 1. In a V volts full scale A/D system, the LSB is $V/2^{n-1}$ where n is the number of resolution bits. If a ½ LSB accuracy is desired, then the comparator should be able to resolve a $V/2^{n+1}V$ signal. If the comparator is to resolve a $V/2^{n+1}V$ signal, then the internal offset of the comparator should be much smaller than ½ LSB. The Successive Approximation Register (SAR) takes at least n + 1 clock cycles to resolve the input signal into n bits. If t_S is the settling time of the DAC, t_{PD} is the propagation delay through the comparator and t_{SD} is the delay through the SAR, then the time taken for each comparison t_1 is given by Equation 1.

$$t_1 = t_S + t_{PD} + t_{SD} \quad (1)$$

Thus, for a complete n-bit conversion, the total time t_N is (n + 1) times t_1 which is given by Equation 2.

$$t_N = (n + 1) \cdot (t_S + t_{PD} + t_S) \quad (2)$$

In order to decrease the conversion time, it is essential to have a fast settling DAC with low t_S, a fast SAR with low t_{SD}, and minimum propagation delay, t_{PD}, through the comparator. For comparators, it is also essential that the input offset voltage, input offset current, voltage gain, and propagation delay remain constant over the entire operating temperature range in order to maintain the speed and accuracy of the A/D system.

The block diagram of the NE5105 comparator is shown in Figure 2. It is composed of five major building blocks: the input stage, an intermediate stage with latch, an output stage with TTL buffer, a temperature-independent voltage reference, and a stable bias circuit. Typical gain of the input stage is 20, intermediate stage gain is 30, and the final stage gain is 45. This yields a total gain of 27,000 for the comparator. Also, the NE/SE5105 has typical input offset voltage of 100μV, input offset current of 3nA, input bias current of 270nA, and a propagation delay of 36ns. The 36ns response time is measured at 1.2mV overdrive; low offset current and high gain remain essentially constant over the operating temperature range. Thus, the same degree of speed and precision can be maintained over the specified temperature range.

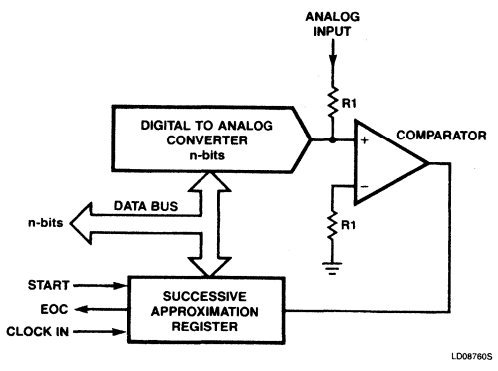


Figure 1. Block Diagram of a Typical SAR Type A/D System

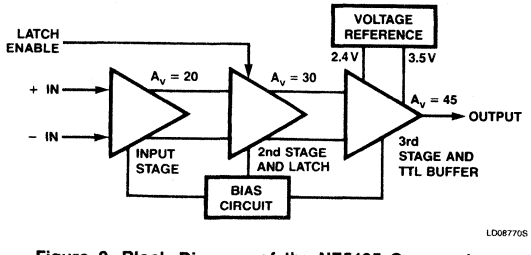


Figure 2. Block Diagram of the NE5105 Comparator

Figure 3 shows the simplified schematic of the input stage. The input transistors Q1 – Q2 have a constant collector current of 100μA which yields typical input bias current of 270nA without the need for super Beta transistors or complex circuitry for bias current cancellation. A further advantage is that the input offset current remains constant over the entire differential input voltage range. Because of this, the error due to input offset current remains constant over the entire differential input voltage range. The level shifting diodes D1 and D2 preserve the input common mode voltage range (CMVR) from the input transistors Q1 and Q2 to the bases of Q3 and Q4. The load resistors R1 and R2 are trimmed to achieve input offset voltage of 100μV.

Figure 4 shows the simplified schematic of the intermediate stage with latch. Transistors Q7 and Q8 form the difference amplifier which receives its inputs from the outputs of the input stage shown in Figure 3. The latch circuit is incorporated within the intermediate stage. A TTL high input at the latch enable pin (LE) forces the output of the comparator to stay at its existing logical state irrespective of subsequent signal transitions at the input of the device. This prevents the comparator from oscillating or changing states due to

12-Bit A/D Converter Using the NE5105 Comparator

noise glitch at the inputs during the latched state.

Figure 5 shows a simplified schematic of the final gain stage with TTL buffer. This stage provides additional gain while differential to single-ended conversion takes place at the output of the buffer. The 3.5V reference sets up the output high voltage V_{OH} while the 2.4V reference sets up the output low voltage V_{OL}.

The simplified schematic of the voltage reference of NE5105 is shown in Figure 6. This is a simple bandgap reference circuit. Voltages with near-zero temperature coefficients are generated at the emitters of Q20 and Q21 by cancelling the negative temperature coefficient of transistor VBEs with positive temperature coefficient voltages across the resistors R10 and R11. The fixed voltages V_{REF1} and V_{REF2} determine the TTL high and low levels at the output. A stable V_{REF1} keeps the V_{OH} stable over the temperature range and provides a good performance for narrow pulses at the input. A stable V_{REF2} yields an optimum base drive for the output transistor Q19 which maintains its high current sink capability over the operating temperature range.

TYPICAL APPLICATION

The NE5105 is well suited for high-accuracy, high-speed analog-to-digital conversion systems because of its low input offset current, low offset voltage, high gain, and low propagation delay. Figure 7 shows a typical application of NE5105 in a 12-bit fast successive approximation A/D system. The 12-bit DAC is a fast settling DAC800-I with current output; a 2504 type SAR is used for logic control. Schottky diodes D1 and D2 are used to limit the maximum differential input voltage at the comparator inputs. To cancel the effect of the input bias current, resistors R4 and R5 are necessary. The value of R4 should be equal to RA of the DAC and R5 equal to RB + RC. The switch connects R4 to ground in unipolar mode and in bipolar mode the total resistance is R4 + R5 — which is approximately equal to RA + RB + RC.

To use the system in unipolar mode, the bipolar offset resistor R_{BO} on DAC800-I should be connected to ground. When the bipolar offset resistor R_{BO} is connected to I_{OUT} on DAC800-I, the DAC will operate in a bipolar mode. This will allow the A/D to be used in a ± 5V range or ± 10V range depending on input voltage span selected. To adjust the full-scale for this 12-bit A/D system, set the input voltage on 10V span to 9.9964V which corresponds to full-scale minus ½ LSB and set up the CLOCK and START signals for continuous conversion. Adjust resistor R2 until all the bits are turned on and only the LSB flickers. To adjust the zero-scale, set 1.22mV at the input, which corresponds to ½ LSB, and adjust R1 until all the bits are turned off and only the LSB flickers. A similar approach can be taken for calibrating either in a bipolar mode or for the 20V span. This completes the calibration procedure for the A/D system.

The total conversion time can be calculated using Equation 2 with the settling time of DAC, propagation delay of the comparator, and the clock timing. If the settling time, t_S, for the DAC is 300ns, the propagation delay, t_{PD}, through the comparator is 36ns and the SAR delay, t_{SD} is 15ns, then from Equation 2 the total conversion time is 4.56μs. By using a faster settling DAC and an SAR with lower t_{SD}, together with a faster clock, the conversion time can be improved significantly.

Good board layout practice is essential for the design of a high-speed and high-accuracy A/D conversion system. A two-sided printed circuit board with good ground plane on both sides is recommended. Keeping the digital and analog ground planes separate will eliminate any clock feedthrough or digital noise in the analog section. However, it should be noted that both ground planes should meet at one – and only one – point on the board. Proper layout of the clock signal trace to the SAR with matching termination impedance will minimize any reflections and thus improve the overall performance. Power supply decoupling is also of prime importance to achieve high accuracy. Again, it is highly recommended that the digital and analog

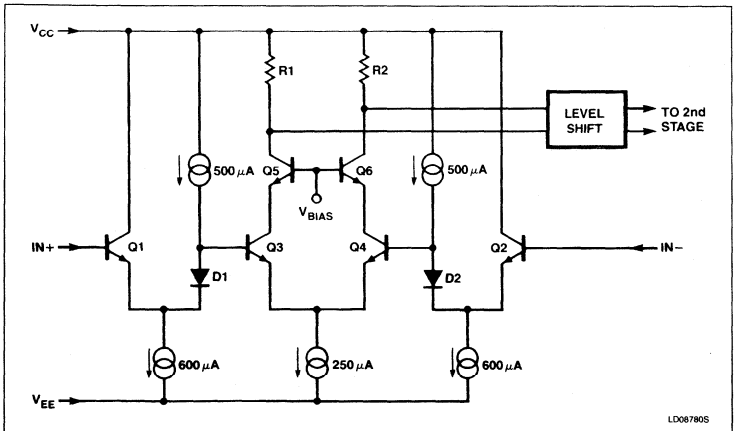


Figure 3. Simplified Schematic of Input Stage

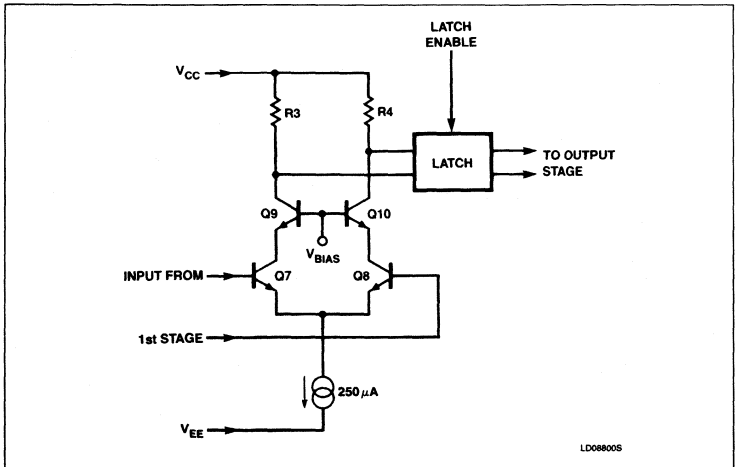


Figure 4. Schematic of the 2nd Stage

power supplies have sufficient decoupling and noise filtering and be kept separate.

ERROR BUDGET ANALYSIS

This section analyzes the errors contributed by the comparator in a successive approximation type A/D converter design. In a 12-bit A/D converter with 10V absolute full scale voltage and 4mA absolute full scale current, 1LSB is 2.44mV or 1μA. The error contributed by the comparator arises from the input offset voltage, input offset current, and voltage gain. The maximum input offset voltage at room temperature for NE5105A is 250μV. Since 2.44mV is 1LSB, 250μV is equal to 0.1LSB. The maximum input offset current at room temperature is 20nA and 1LSB is 1μA, so the error contributed by offset current is 0.02LSB. To understand how the gain of the comparator contributes to the error budget, consider the following case. The output of comparator changes from 0.4V to 2.4V. Therefore, $\Delta V = 2V$ and the gain of comparator is 18000 (minimum at room temperature for NE5105A), the necessary input voltage to cause the output to change is 2/18000 = 111μV. If the input threshold is at the midpoint of the input range of 111μV, then the excursion on each side of the threshold is 111μV/2 = 55μV. This 55μV due to gain contributes to the error budget. Again, 1LSB is 2.44mV, so 55μV is 0.02LSB. The worst case error is the sum of error contributed by offset voltage, offset current, and voltage gain. But the RMS error has more meaning because of the statistical nature of the offset and gain parameters. Table 1 shows the error contribution of NE/SE5105A in a 12-bit 10V/4mA A/D converter system at room temperature.

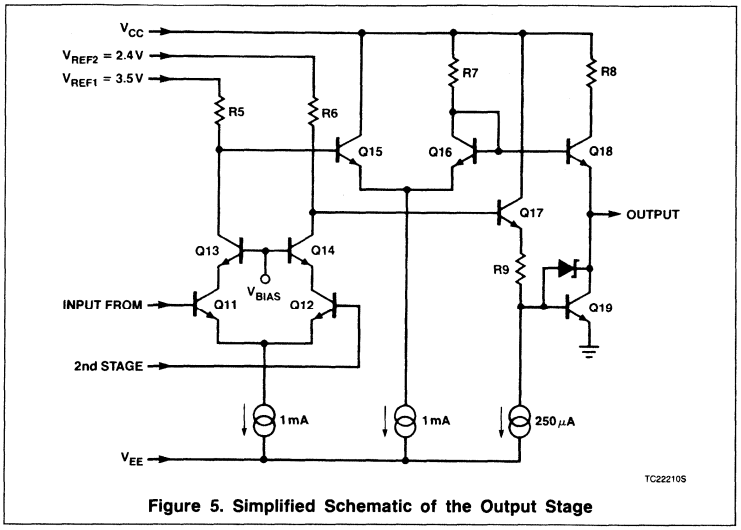


Figure 5. Simplified Schematic of the Output Stage

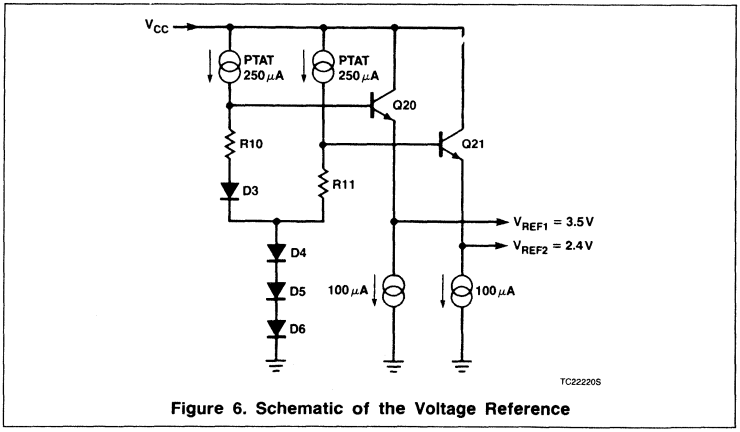


Figure 6. Schematic of the Voltage Reference

It can be seen from Table 1 that the RMS error contributed by the comparator at room temperature is 0.10LSB. If the 12-bit D/A converter is ¼ LSB accurate, then the complete system can be ½ LSB accurate at room temperature. Table 2 shows the error contribution of NE/SE5105A over the military temperature range.

The RMS error over the military temperature range is 0.25LSB, which is significantly higher than the RMS error at room temperature. If the 12-bit D/A converter is ¼ LSB accurate, then the total accuracy of the 12-bit A/D system will be ½ LSB. It is very hard to find 12-bit D/A converters which maintain ¼ accuracy over the entire operating temperature range. A ½ LSB accurate 12-bit D/A converter along with the NE5105A will yield a total system accuracy of ¾ LSB for 1 12-bit A/D converter over the entire military temperature range.

12-Bit A/D Converter Using the NE5105 Comparator

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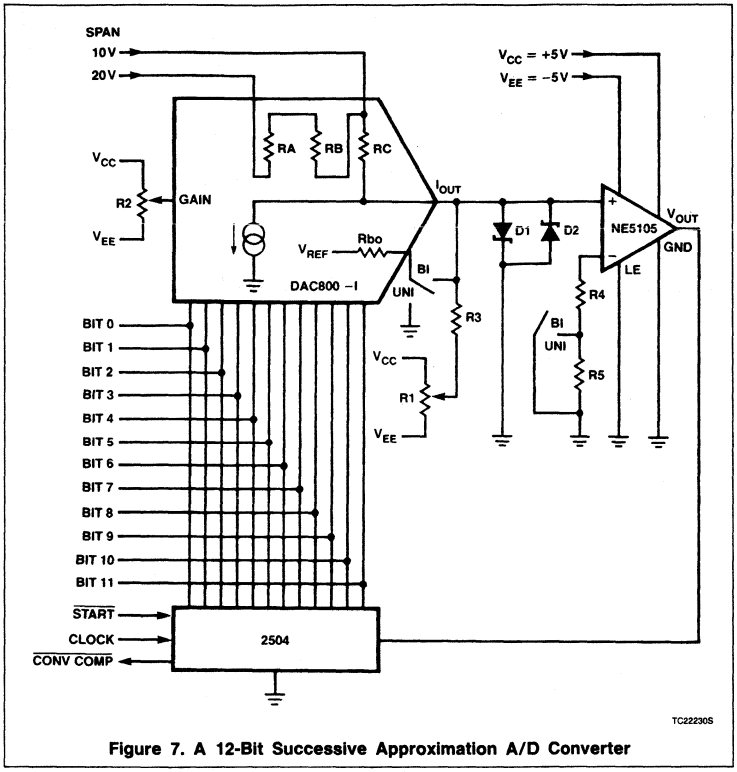


Figure 7. A 12-Bit Successive Approximation A/D Converter

Table 1. Error Budget Analysis for NE5105A (T_A = +25°C; V+ = 5V; V− = −5V)

SYMBOL	PARAMETER	TYP	MIN/MAX	UNIT
V_{OS}	Input offset voltage	100	250	μV
I_{OS}	Input offset current	3	20	nA
AV	Voltage gain	26,000	18,000	V/V
E_{VOS}	Error due to V_{OS}	0.04	0.10	LSB
E_{IOS}	Error due to I_{OS}	0.003	0.02	LSB
E_{AV}	Error due to gain	0.016	0.02	LSB
ΣE_I	Worst case error sum	0.06	0.14	LSB
E_t^2	RMS error sum	0.04	0.10	LSB

Table 2. Error Budget Analysis for SE5105A ($-55°C \leq T_A$; V+ = 5V; V– = –5V)

SYMBOL	PARAMETER	TYP	MIN/MAX	UNIT
V_{OS}	Input offset voltage	250	600	μV
I_{OS}	Input offset current	4	25	nA
AV	Voltage gain	23,000	16,000	V/V
E_{VOS}	Error due to V_{OS}	0.10	0.25	LSB
E_{IOS}	Error due to I_{OS}	0.004	0.025	LSB
E_{AV}	Error due to gain	0.018	0.026	LSB
Σ_{EI}	Worst case error sum	0.12	0.30	LSB
E_t^2	RMS error sum	0.10	0.25	LSB

INTERFACE

page

Position measurement 661

Peripheral drivers 715

Display drivers 783

Position measurement

		page
NE5520	linear variable differential transformer (LVDT) signal conditioner	663
NE5521	linear variable differential transformer (LVDT) signal conditioner	668
SA5521	linear variable differential transformer (LVDT) signal conditioner	668
SE5521	linear variable differential transformer (LVDT) signal conditioner	668
AN118	using the LVDT signal conditioner	673
AN1180	a microprocessor-based servo-loop for linear position control	688
AN1181	NE/SE5521 simplifies modulated light source design	698
AN1182	using the NE5521 signal conditioner in multi-faceted applications	702

NOT FOR NEW DESIGN

NE5520
LVDT Signal Conditioner

Product Specification

DESCRIPTION

The NE5520 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LVDT). The chip includes a low distortion amplitude stable sine wave oscillator with programmable frequency to drive the primary of the LVDT; a synchronous demodulator to convert the LVDT output amplitude and phase to position information; and an output amp to provide gain and filtering.

FEATURES

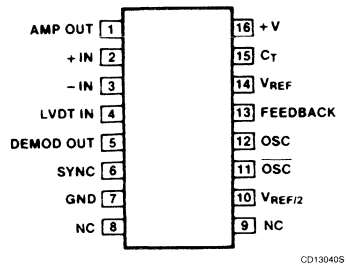
- **Oscillator frequency: 1kHz to 20kHz**
- **Low distortion**
- **Capable of ratiometric operation**
- **Single supply operation 5V to 20V or dual supply ±2.5V to ±10V**
- **Low power consumption**

APPLICATIONS

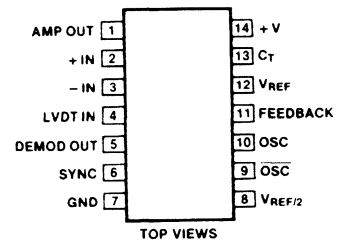
- **LVDT signal conditioning**
- **RVDT signal conditioning**

PIN CONFIGURATIONS

D[1], F Packages



N Package



NOTE:
1. SOL — Released in large SO package only.

ORDERING INFORMATION

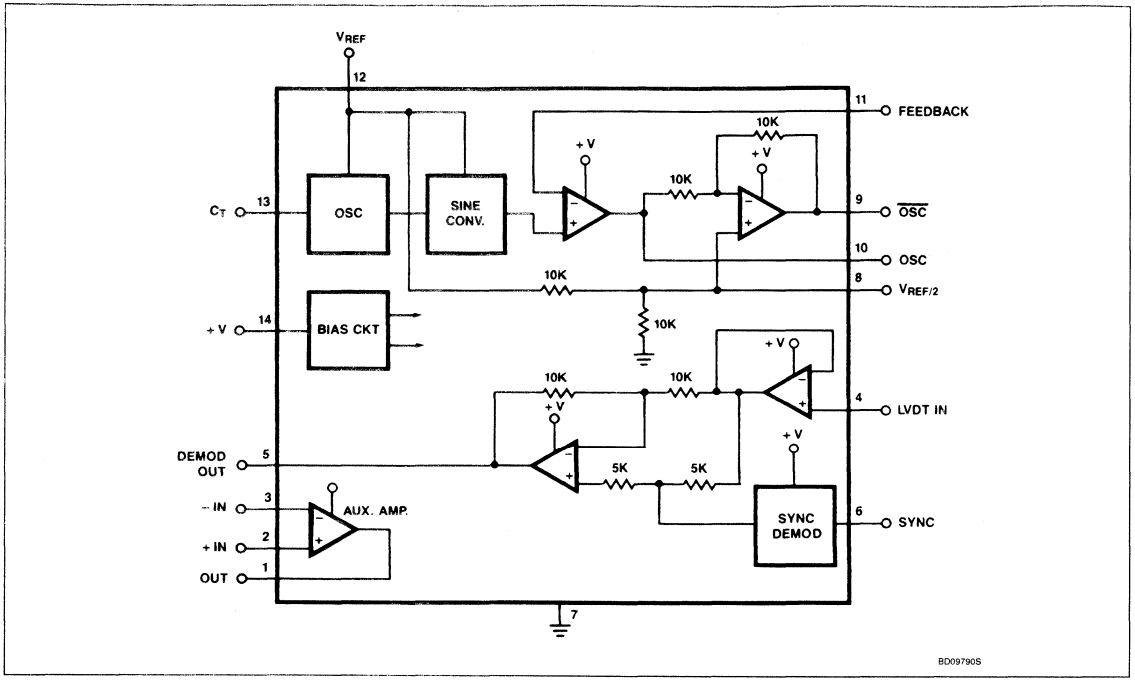
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5520N
16-Pin SOL Package	0 to +70°C	NE5520D
16-Pin Ceramic DIP	0 to +70°C	NE5520F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	+20	V
	Split supply voltage	±10	V
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +165	°C
P_D	Power Dissipation[1]	840	mW

NOTES:
1. Supplied only in large SO (Small Outline) package. See package diagram.
2. Pin numbers are for N package.

BLOCK DIAGRAM



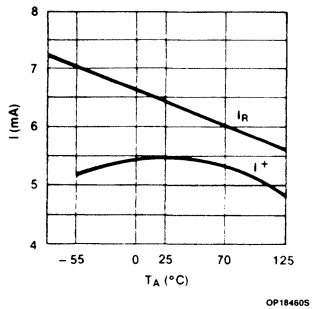
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_R = V+ = 10V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I_{CC}	Supply current	Over temperature		7.0	10	mA
I_{REF}	Reference current	Over temperature		5.5	10	mA
V_{REF}	Reference voltage range	Over temperature	5		V+	V
P_D	Power dissipation			120	220	mW
Oscillator section						
	Oscillator output			$\frac{V_R}{8.7}$		V_{RMS}
	Sine wave distortion			4		%
	Initial amplitude error				±3	%
	Tempco of amplitude				0.05	%/°C
	Voltage coefficient of amplitude error				2.5	%/V
	Initial accuracy of oscillator frequency				20	%
	Tempco of frequency error			0.05		%/°C
	Voltage coefficient of frequency			2.5		%/V(V_R)
	Oscillator output load current	Over temperature	8	15		mA_{RMS} mA_{RMS}
Demodulator section						
E_r	Linearity error	Over temperature		0.05	0.1	%
	Maximum demodulator input	Over temperature range	$\frac{V_R}{2} - 0.5$		$\frac{V_R}{2} + 0.5$	V
	Demodulator offset voltage	Over temperature range			65	mV
	Demodulator input current	Over temperature	−1000	−300		nA
	$V_{R/2}$ accuracy	Over temperature	−3	±0.5	+3	%
Auxiliary output amplifier						
V_{OS}	Input offset voltage	Over temperature	−10		10	mV
I_{BIAS}	Input bias current	Over temperature range	−500	−300		nA
I_{OS}	Input offset current		−100		100	nA
A_V	Gain	$R_L = 10k\Omega$ over temperature		100		V/mV
SR	Slew rate			1.5		V/μs
GBW	Gain bandwidth	$A_V = 1$		1		MHz
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$ over temperature	1.5		V+ − 1.5	V
I_{SC}	Output short-circuit current			50		mA

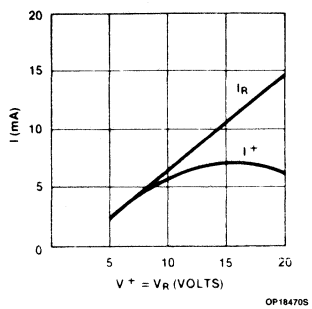
NOTE:
Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 7.6mW/°C for the plastic package and 7.3mW/°C for the cerdip package.

TYPICAL PERFORMANCE CHARACTERISTICS

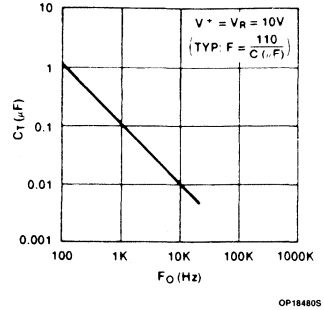
I_R and I^+ vs Temperature



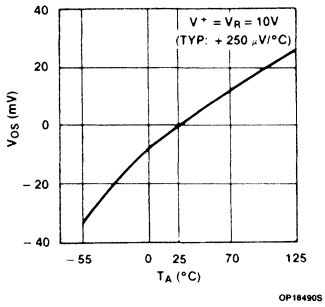
I_R and I^+ vs Voltage



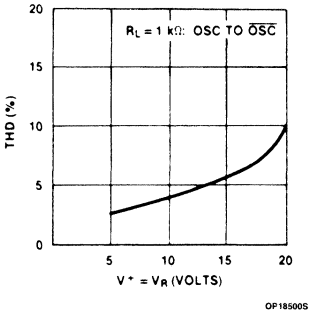
F_O vs C_T



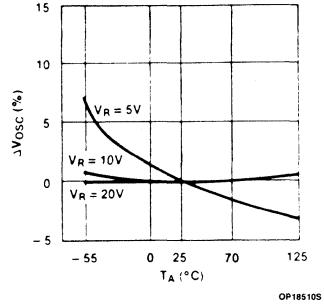
Demodulator Offset vs Temperature (Normalized to 25°C)



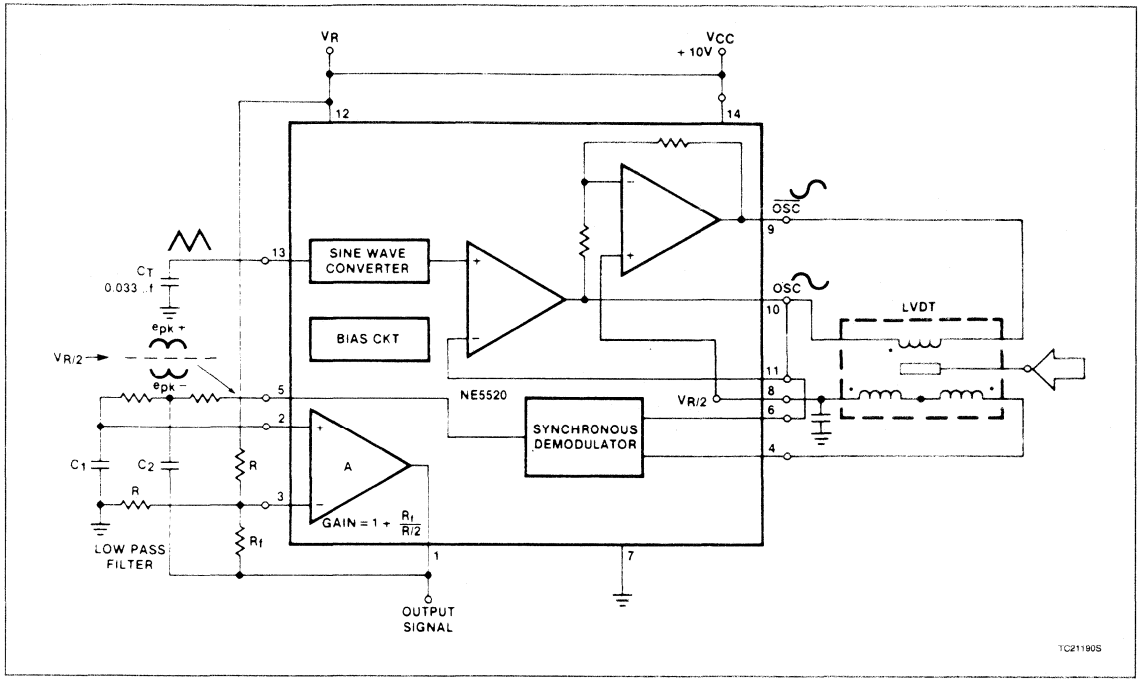
Distortion of Sine Wave vs Reference Voltage



Oscillator Amplitude Variation With Temperature



TYPICAL SINGLE SUPPLY LVDT CIRCUIT



NE/SA/SE5521
LVDT Signal Conditioner

Product Specification

DESCRIPTION

The NE/SA/SE5521 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LDVTs) and Rotary Variable Differential Transformers (RVDTs). The chip includes a low distortion, amplitude-stable sine wave oscillator with programmable frequency to drive the primary of the LVDT/RVDT, a synchronous demodulator to convert the LVDT/RVDT output amplitude and phase to position information, and an output amplifier to provide amplification and filtering of the demodulated signal.

FEATURES

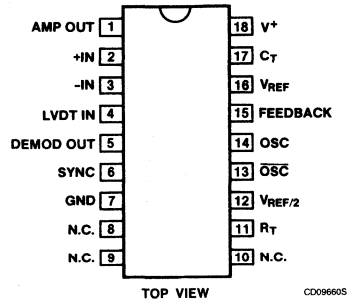
- **Low distortion**
- **Single supply 5V to 20V, or dual supply ±2.5V to ±10V**
- **Oscillator frequency 1kHz to 20kHz**
- **Capable of ratiometric operation**
- **Low power consumption (182mV typ)**

APPLICATIONS

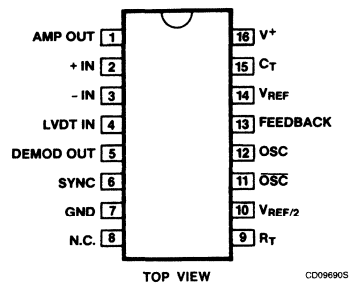
- **LVDT signal conditioning**
- **RVDT signal conditioning**
- **LPDT signal conditioning**
- **Bridge circuits**

PIN CONFIGURATIONS

F, N Packages



D[1] Package

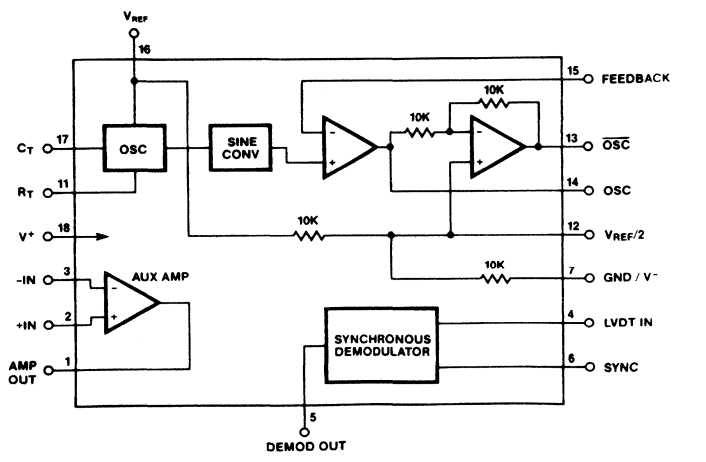


NOTE:
1. SOL — released in large SO package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP	0 to +70°C	NE5521N
18-Pin Cerdip	0 to +70°C	NE5521F
16-Pin SOL Package	0 to +70°C	NE5521D
18-Pin Plastic DIP	−40°C to +85°C	SA5521N
18-Pin Cerdip	−55°C to +125°C	SE5521F
16-Pin SOL Package	−40°C to +85°C	SA5521D

BLOCK DIAGRAM



NOTE:
Pin numbers are for F, N packages.

PIN DEFINITIONS FOR D, F AND N PACKAGES

PIN NO.		SYMBOL	DEFINITION
D	F, N		
1	1	Amp Out	Auxiliary Amplifier Output.
2	2	+IN	Auxiliary Amplifier non-inverting input.
3	3	-IN	Auxiliary Amplifier inverting input.
4	4	LVDT IN	Input to Synchronous Demodulator from the LVDT/RVDT secondary.
5	5	DEMOD OUT	Pulsating DC output from the Synchronous Demodulator output. This voltage should be filtered before use.
6	6	SYNC	Synchronizing input for the Synchronizing Demodulator. This input should be connected to the OSC or $\overline{OSC}$ output. Sync is referenced to $V_{REF}/2$.
7	7	GND	Device return. Should be connected to system ground or to the negative supply.
8	8	NC	No internal connection.
—	9	NC	No internal connection.
—	10	NC	No internal connection.
9	11	R_T	A temperature stable 18kΩ resistor should be connected between this pin and Pin 7.
10	12	$V_{REF}/2$	A high impedance source of one half the potential applied to V_{REF}. The LVDT/RVDT secondary return should be to this point. A bypass capacitor with low impedance at the oscillator frequency should also be connected between this pin and ground.
11	13	$\overline{OSC}$	Oscillator sine wave output that is 180° out of phase with the OSC signal. The LVDT/RVDT primary is usually connected between OSC and $\overline{OSC}$ pins.
12	14	OSC	Oscillator sine wave output. The LVDT/RVDT primaries are usually connected between OSC and $\overline{OSC}$ pins.
13	15	FEEDBACK	Usually connected to the OSC output for unity gain, a resistor between this pin and OSC, and one between this pin and ground can provide for a change in the oscillator output pin amplitudes.
14	16	V_{REF}	Reference voltage input for the oscillator and sine converter. This voltage MUST be stable and must not exceed +V supply voltage.
15	17	C_T	Oscillator frequency-determining capacitor. The capacitor connected between this pin and ground should be a temperature-stable type.
16	18	+V	Positive supply connection.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+20	V
	Split supply voltage	±10	V
T_A	Operating temperature range		
	NE5521	0 to +70	°C
	SA5521	-40 to +85	°C
	SE5521	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Power dissipation[1]	910	mW

NOTE:
1. For derating, see typical power dissipation versus load curves (Figure 1).

DC ELECTRICAL CHARACTERISTICS $V+ = V_{REF} = 10V$, $T_A = 0$ to 70°C for NE5521, $T_A = -55$ to +125°C for SE5521, $T_A = -40$ to +85°C for SA5521, Frequency = 1kHz, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NE5521			SA/SE5521			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply current			12.9	20		12.9	18	mA
I_{REF}	Reference current			5.3	8		5.3	8	mA
V_{REF}	Reference voltage range		5		V+	5		V+	V
P_D	Power dissipation			182	280		182	260	mW
Oscillator Section									
	Oscillator output	$R_L = 10k\Omega$		$\frac{V_{REF}}{8.8}$			$\frac{V_{REF}}{8.8}$		V_{RMS}
THD	Sine wave distortion	No load		1.5			1.5		%
	Initial amplitude error	$T_A = 25°C$		0.4	±3		0.4	±3	%
	Tempco of amplitude			0.005	0.01		0.005	0.01	%/°C
	Init. accuracy of oscillator freq.	$T_A = 25°C$		±0.9	±5		±0.9	±5	%
	Temperature coeff. of frequency[1]			0.05			0.05		%/°C
	Voltage coeff. of frequency			2.5			3.3		%/ $V(V_{REF})$
	Min OSC ($\overline{OSC}$) Load[2]		300	170		300	170		=0m
Demodulator Section									
ϵ_r	Linearity error	$5V_{P-P}$ input		±0.05	±0.1		±0.05	±0.1	%FS
	Maximum demodulator input			$\frac{V_{REF}}{2}$			$\frac{V_{REF}}{2}$		V_{P-P}
V_{OS}	Demodulator offset voltage			±1.4	±5		±1.4	±5	mV
TCV_{OS}	Demodulator offset voltage drift			5	25		5	25	µV/°C
I_{BIAS}	Demodulator input current		-600	-234		-500	-234		nA
	$V_{R/2}$ accuracy			±0.1	±1		±0.1	±1	%
Auxiliary Output Amplifier									
V_{OS}	Input offset voltage			±0.5	±5		±0.5	±5	mV
I_{BIAS}	Input bias current		-600	-210		-500	-210		nA
I_{OS}	Input offset current			10	50		10	50	nA
A_V	Gain		100	385		100	385		V/mV
SR	Slew rate			1.3			1.3		V/µs
GBW	Unity gain bandwidth product	$A_V = 1$		1.6			1.6		MHz
	Output voltage swing	$R_L = 10k\Omega$	7	8.2		7	8.2		V
	Output short circuit current to ground or to V_{CC}	$T_A = 25°C$		42	100		42	100	mA

NOTES:

1. This is temperature coefficient of frequency for the device only. It is assumed that C_T and R_T are fixed in value and C_T leakage is fixed over the operating temperature range.
2. Minimum load impedance for which distortion is guaranteed to be less than 5%.

DEFINITION OF TERMS

Oscillator Output	RMS value of the AC voltage available at the oscillator output pin. This output is referenced to $V_{REF/2}$ and is a function of V_{REF}.
Sine Wave Distortion	The Total Harmonic Distortion (THD) of the oscillator output with no load. This is not a critical specification in LVDT/RVDT systems. This figure could be 15% or more without affecting system performance.
Initial Amplitude Error	A measure of the interchangeability of NE/SA/SE5521 parts, *not* a characteristic of any one part. It is the degree to which the oscillator output of a number of NE/SA/SE5521 samples will vary from the median of that sample.
Initial Accuracy of Oscillator Frequency	Another measure of the interchangeability of individual NE/SA/SE5521 parts. This is the degree to which the oscillator frequency of a number of NE/SA/SE5521 samples will vary from the median of that sample with a given timing capacitor.
Tempco of Oscillator Amplitude	A measure of how the oscillator amplitude varies with ambient temperature as that temperature deviates from a 25°C ambient.
Tempco of Oscillator Frequency	A measure of how the oscillator frequency varies with ambient temperature as that temperature deviates from a 25°C ambient.
Voltage Coeffecient of Oscillator Frequency	The degree to which the oscillator frequency will vary as the reference voltage (V_{REF}) deviates from +10V.
Min OSC ($\overline{OSC}$) Load	Minimum load impedance for which distortion is guaranteed to be less than 5%.
Linearity Error	The degree to which the DC output of the demodulator/amplifier combination matches a change in the AC signal at the demodulator input. It is measured as the worst case nonlinearity from a straight line drawn between positive and negative fullscale end points.
Maximum Demodulator Input	The maximum signal that can be applied to the demodulator input without exceeding the specified linearity error.

APPLICATION INFORMATION

$$\text{OSC frequency} = \frac{V_{REF} - 1.3V}{V_{REF}(R_T + 1.5k)C_T}$$

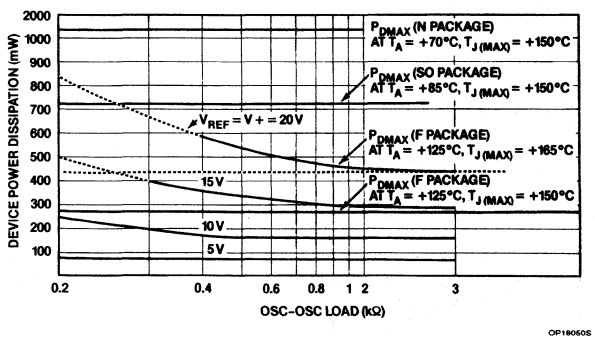


Figure 1. Device Power Dissipation vs OSC - $\overline{OSC}$ Load at +25°C

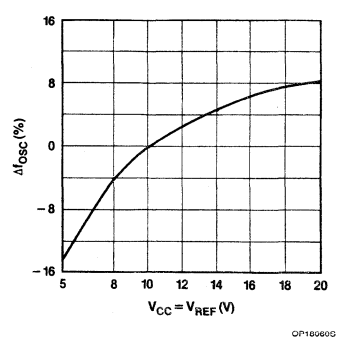


Figure 2. Oscillator Frequency Variation With Voltage (Normalized to $V_{REF} = V_{CC}$=10V) T_A = +25°C

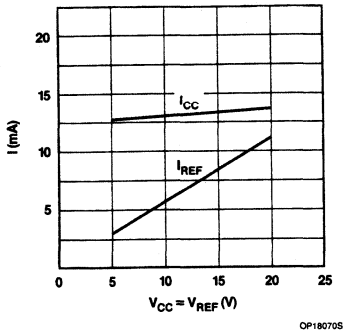


Figure 3. I_{REF} and I_{CC} vs Voltage ($T_A = +25°C$)

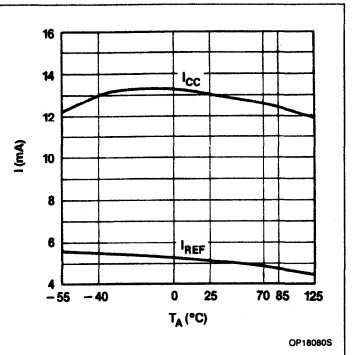


Figure 4. I_{REF} and I_{CC} vs Temperature ($V_{REF} = V_{CC} = 10V$)

AN118
Using the LVDT Signal Conditioner

Application Note

INTRODUCTION

An LVDT is an electromechanical transducer which makes possible the measurement of very small motion in a structure or mechanical device. Mechanical motion is translated to an electrical signal which contains position information much as a radio frequency carrier contains sound information. The position information from the LVDT is contained in the phase and amplitude of the output AC waveform. In order to remove the position information (demodulation), a system such as is shown in block form in Figure 1 must be used. Once signal demodulation is achieved, the position data may be read out on a meter or digital display in addition to being processed by microprocessor or computer. The Signetics NE5520 is a Monolithic LVDT Driver-Demodulator designed to interface with most LVDTs presently being used in the industry.

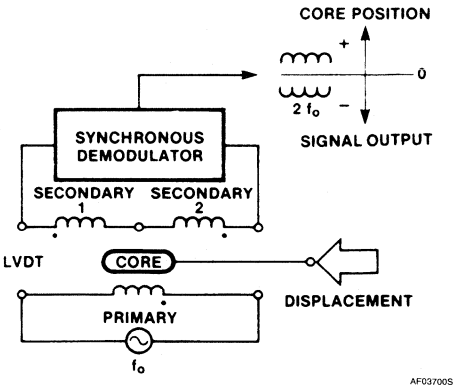


Figure 1. The LVDT With Sine Wave Excitation and Synchronous Demodulation

Uses will range over a large number of potential applications including the accurate measurement of position, pressure, load weight, angular position and even acceleration. Historically, LVDTs have been used in the following applications:

- Load cell
- Linear motion
- Torque cell
- Vibration
- Fluid pressure
- Accelerometer
- Inclinometer
- Seismic load cell

Motion may be

- Linear
- Rotary

The NE5520 provides sinusoidal drive to the Linear Variable Differential Transformer (LVDT), the output of which is buffered, rectified and phase-demodulated to obtain both direction and displacement information in the form of a DC output signal (Figure 2).

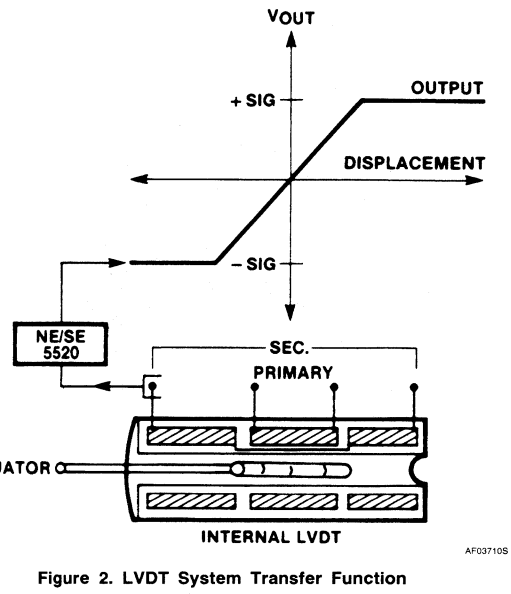


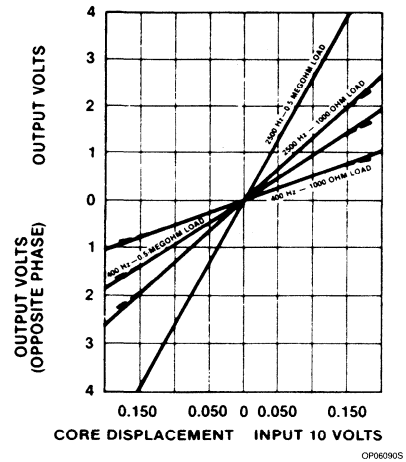
Figure 2. LVDT System Transfer Function

LVDT LOADING

Due to the loosely coupled characteristics of the typical LVDT, loading effects versus frequency may be critical to a successful design. The graph (Figure 3a) shows this relationship in the form of a family of curves relative to LVDT core displacement for 400Hz and 2500Hz. From the curves it is obvious that the linearity and output level versus displacement is superior for an LVDT operated at 2500Hz with a very high impedance load (0.5MΩ). The NE5520 demodulator presents a very high input impedance to the LVDT secondary for maximum linearity (Figure 3b).

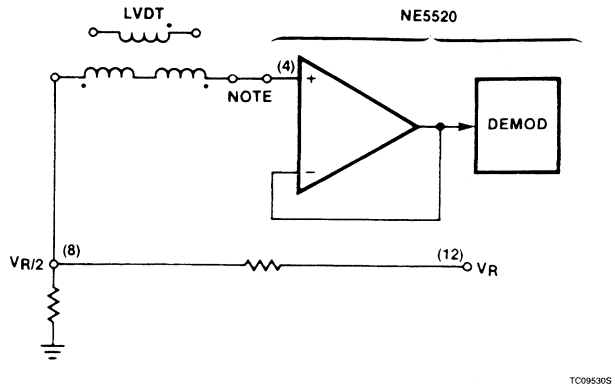
LVDT INTERFACING: SIGNAL CONDITIONING IS REQUIRED

In order to obtain usable information from the LVDT a series of signal-conditioning circuit operations are required. First, a stable source



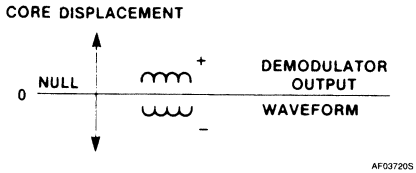
NOTE:
By permission Schaevitz Engineering
"Handbook of Measurement and Control" by Herceg.

a.



NOTE:
Internal buffer amp provides high impedance load to secondary.

b.



c.

Figure 3. Output Characteristics of a Typical LVDT for Various Loads and Excitation Frequencies

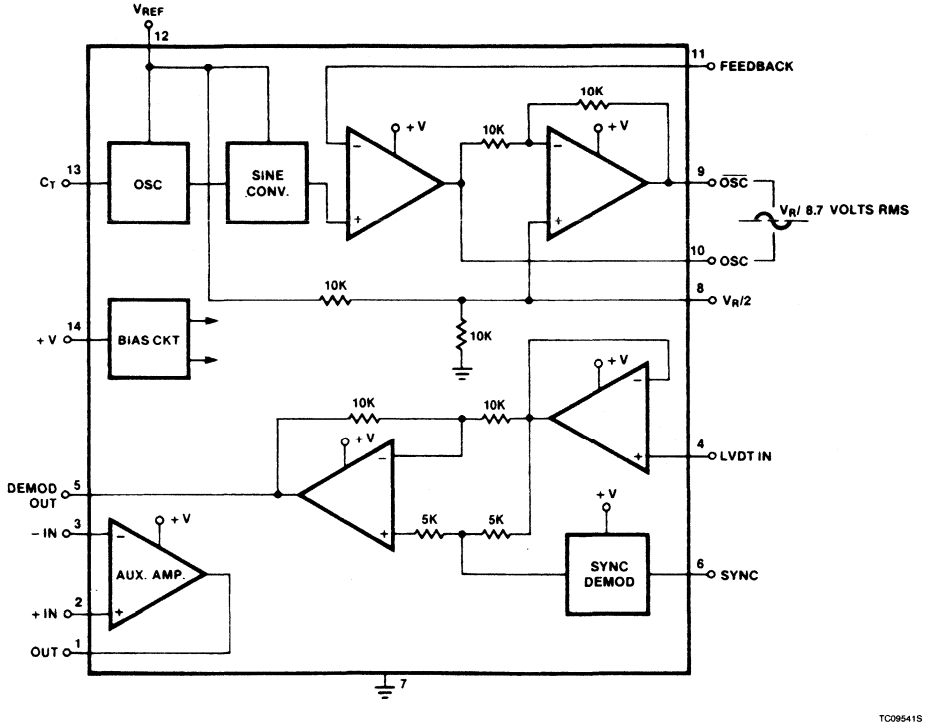
of constant frequency excitation voltage must be applied to the primary of the LVDT.

Next, some form of demodulator is needed to extract position information from the LVDT secondary output signal. A full-wave rectifier will provide usable amplitude information when adequately filtered; however, relative phase information is lacking. In order to obtain both phase and amplitude information, synchronous demodulation is needed. This type of demodulator exists in the Signetics NE5520. Once phase and amplitude information is obtained in the form of a polar full-wave rectified signal (see Figure 3c) from the synchronous demodulator, the carrier component (actually 2nd harmonic of the carrier plus higher-order spectral components) must be filtered out, leaving only the true position information. This is accomplished by passing the demodulated signal through a low-pass active filter. An auxiliary operational amplifier is provided for this purpose within the NE5520, in addition to adjustable signal gain for proper full-scale output (span adjustment). In addition, DC offsets are nulled by a simple offset adjustment at the auxiliary amplifier. The resulting system is a complete LVDT signal conditioner. Figure 4 shows a block diagram of the NE5520. The device will operate in a single supply range from 5 to $20V_{DC}$ or with split supplies of ± 5 to $\pm 10V_{DC}$. A device current, I_{CC}, of 10mA at an operating voltage of 10V is typical.

DESCRIPTION OF THE NE5520 (Figure 4)

The NE5520 oscillator consists of a triangle wave generator, a current source-sink circuit which switches when the capacitor voltage reaches discrete levels at $\frac{1}{4}$ and $\frac{3}{4}$ V_{REF}. The total swing being $V_{REF/2}$ V_{P-P}. The triangle wave is fed into a non-linear load which generates a sinusoidal waveform with low distortion. The sine wave output is then buffered by two op amps, the output of which appear on Pins 9 and 10 in phase opposition. This then is the excitation signal for the LVDT primary.

The second major functional portion of the NE5520 is the synchronous demodulator and this section performs full-wave rectification in phase synchronism (Pin 6) with the above oscillator output. In order to extract true position information, the phase relationship of the LVDT secondary must be obtained. This means that as the LVDT core passes through null an abrupt 180° phase change occurs. Once full-wave rectification is accomplished, the resulting signal carrier frequency must be removed by filtering. Demodulator output appears on Pin 5. This is accomplished by an active filter incorporating the auxiliary op amp (Pins 1, 2, 3). The original position information



NOTE:
Pin numbers for N package.

Figure 4. Block Diagram

then appears ripple-free on Pin 1 of the auxiliary amplifier.

Other functions include buffer amplifier feedback in the oscillator circuit. The loop is closed with negative feedback around both amplifiers (Pin 10 to 11) operating at unity gain.

The oscillator timing capacitor controls the frequency as shown in the graph, Figure 5. The frequency is related by the equation $f_{OSC} = 110C_T(\mu F)$. Absolute output frequency will vary slightly with supply voltage.

BIASING THE REFERENCE V_{REF} (Pin 12)

The manner in which the V_R pin is biased will effect the output voltage function of the NE5520 and consideration must be given to this in order to arrive at an optimum system design. There are two basic modes of operation involved as listed below:

1) Ratiometric

2) Fixed Reference

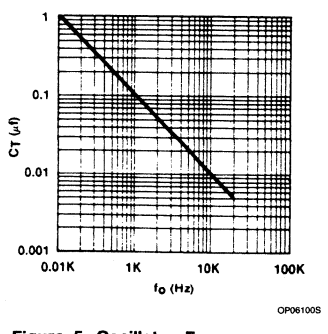


Figure 5. Oscillator Frequency vs Capacitance

With the ratiometric mode, Pin 12 (V_{REF}) is connected to Pin 14 (+V). Since V_R controls the DC common-mode voltage of the demodulator and the oscillator RMS output, these magnitudes will now change with supply voltage. The DC output from Pin 1, using a single ground-referenced supply, will be ratiometric with the supply voltage and centered within the common-mode range of the output amplifier when the LVDT transducer is at null. Single or dual supply operation will be ratiometric when +V is connected to V_R.

The alternate method of biasing is the fixed reference mode with Pin 12 (V_R) connected to a fixed reference voltage such as +10V and Pin 14 (+V) allowed to vary with an incoming poorly regulated supply. This might occur in automotive applications where battery voltage may vary from 10 to 14V. However, with a fixed reference driving V_R, DC voltage at the output will not vary with supply but will vary within the common-mode limits of the amplifier as the LVDT core traverses its path. Output voltage of Pin 1 at LVDT null will be $V_R/2$. Thus, for the case mentioned with V_R = 10V, the null voltage will be +5V. The maximum linear swing would be 1.5 – 8.5V around this value. The fixed reference mode may be used with single or dual supply operation.

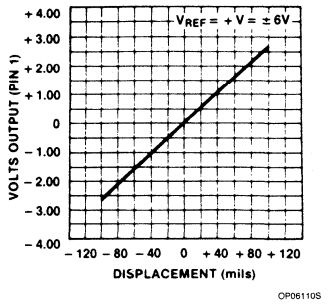
Using the LVDT Signal Conditioner

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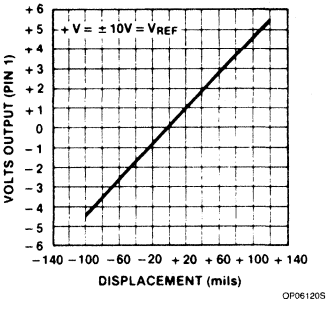
DUAL SUPPLY OPERATION

When connected to a typical LVDT transducer as shown in Figure 6, the NE5520 will exhibit an extremely linear transfer function. Very important to precision position measurement is the inherent repeatability of the system. The graphs in Figure 7a and b illustrate the highly linear transfer function and its repeatable accuracy with different supply voltages, in this case ±6V and ±10V. The transducer motion was over a range of ± 150 milliinches each side of the LVDT null. Typical DC output signal is Note that linearity remains constant, however, full-scale Note that linearity remains constant, however, full-scale output varies with supply voltage. This is due to the increased excitor drive to the LVDT with increased reference voltage. LVDT output is a linear function of excitor amplitude on the primary winding. The addition of a single gain control may easily be added between Pins 1 and 3 to reduce gain in order to retain constant output for different supply voltages (see Figure 8) or V_R may be connected to a fixed voltage. (See 'Biasing.')

It is strongly recommended that dual output tracking regulated supplies be used in this type of application in order to minimize system DC offset and impaired measurement accuracy due to power supply unbalance. An optional circuit capable of automatically tracking and nulling power supply offset is shown in Figure 9. The bipolar output signal is referenced to ground.



a. Transfer Function ±6V



b. Transfer Function ±10V

Figure 7

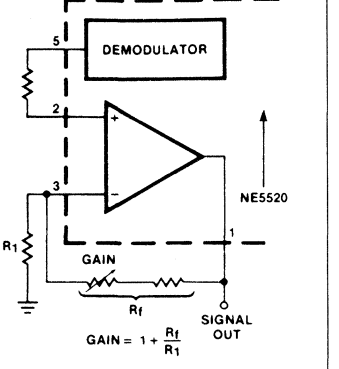


Figure 8. Typical Gain Adjust Circuit

NULLING PROCEDURE (Figure 9)

1. Null transducer position by observing Pin 4 waveform. Set supply voltage for ±6.00V.
2. Set offset adjust pot (feeds Pin 3 of NE5520) for 0.00V_{DC} at Pin 1 of NE5520.
3. Adjust offset null pot (NE5512) for zero output on Terminal A.
4. Check for equal voltage ± deflection when transducer is displaced equal distances from physical null position.
5. Adjust tracking control for minimum DC output change when either supply is varied over operating range at 'A'.

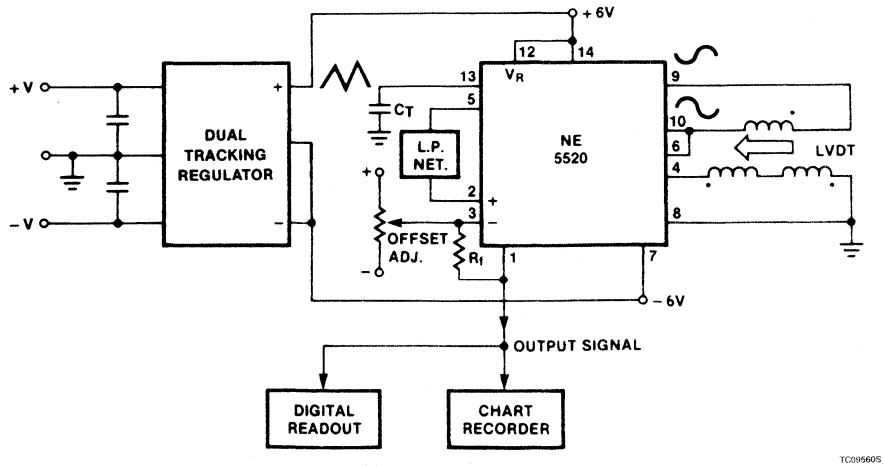


Figure 6. Typical Measuring System (Ratiometric Mode)

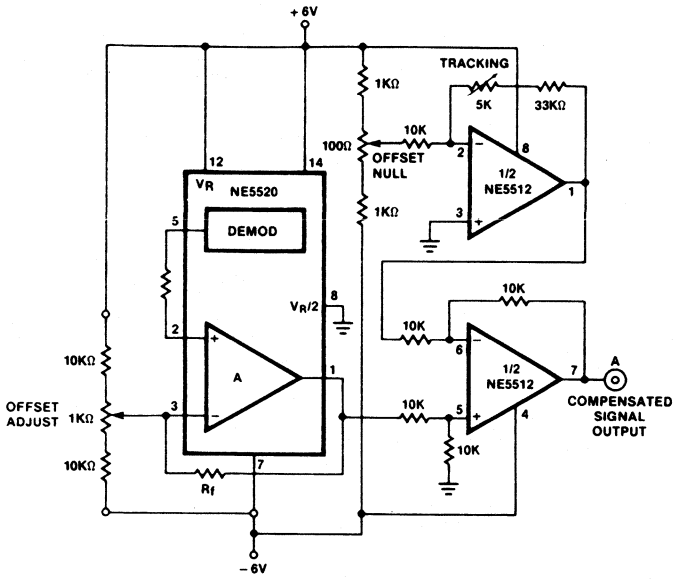


Figure 9. Auto PSRR for Use With Non-Tracking Supplies

SINGLE SUPPLY OPERATION

Single-ended supply operation requires a different circuit approach to obtain measurement system interface. Figure 10 shows a typical circuit using a single 10V supply. Note that the output (Pin 1) of the NE5520 is now floating above ground at approximately $V_R/2$. Simple measuring circuits may be realized (Figures 11a, b, c) by placing a DC microammeter between Pin 1 and a resistive divider creating a bridge readout which is ratiometric with supply voltage variations. In case more precision is necessary, a buffer amplifier may be added between the voltage divider or $V_R/2$ and the readout circuit in order to minimize offset due to measuring circuit loading. DC offset due to internal tracking error in the NE5520 may be reduced by using the nulling circuit shown in Figure 12. Offset sensitivity and its effect on system accuracy will be inversely proportional to full-scale signal output of the NE5520 which is a function of the DC gain of the auxiliary amplifier and LVDT output. A typical full-scale output with 10V supply operation is $V_R/2 \pm 3.5V$ with gain equal to 10.

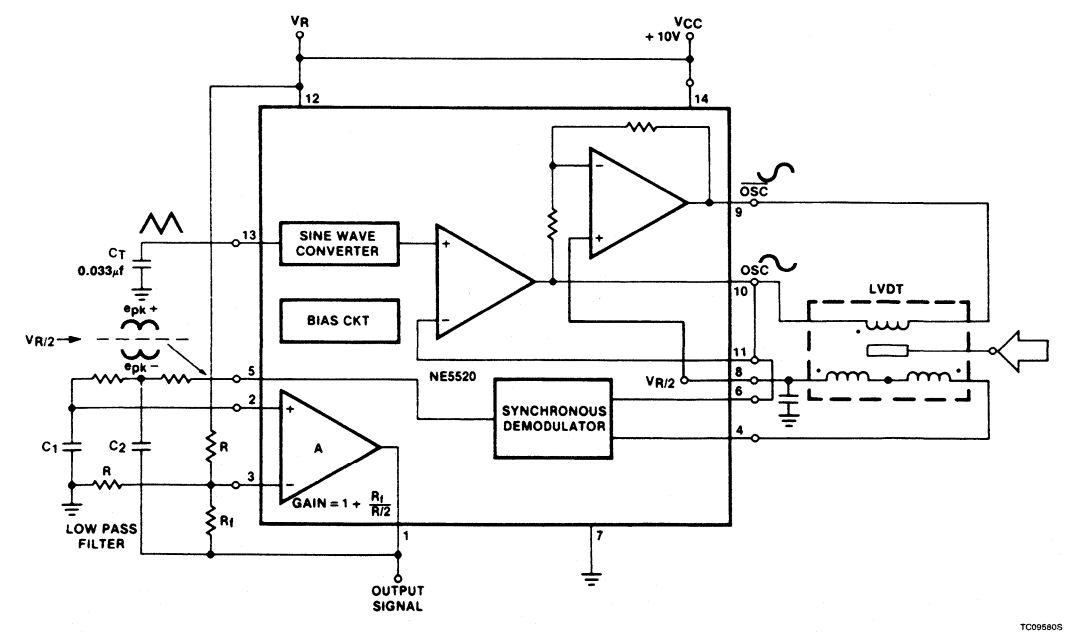


Figure 10. Typical Single Supply LVDT Circuit

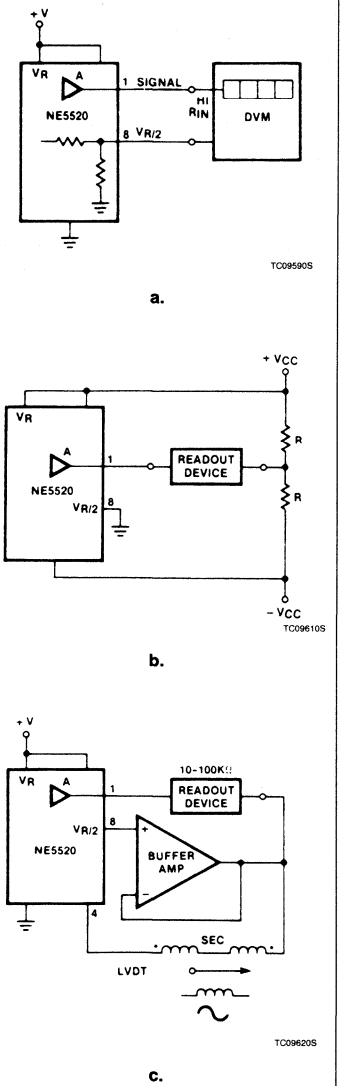


Figure 11. Output Interfacing Examples

MATCHING THE NE5520 TO LOW IMPEDANCE LVDTS

The NE5520 exciter output is capable of driving LVDT primary windings with a minimum impedance of 1kΩ. When a significantly lower impedance primary is driven by the device some form of step-down impedance matching or a power buffer is recommended. Figure 13 shows a step-down matching transformer approach. A transformer with primary impedance of approximately 1kΩ (audio type) with the proper secondary impedance to match the LVDT primary is used to couple oscillator excitation. Depending on the output efficiency of the LVDT, output signal losses may occur with a corresponding loss in measuring sensitivity. The auxiliary amplifier gain may be increased to offset this loss.

A second approach makes use of a power buffer amplifier constructed from discrete transistors (2N2222, 2N3644). This circuit (Figure 14) results in less signal loss and is inexpensive. A DC decoupling capacitor must be used to prevent DC offset currents from flowing in the LVDT primary winding. A 3dB signal reduction is noted when driving a 15Ω load to $6V_{P-P}$ (10V operation); and $12V_{P-P}$ for 20V supply.

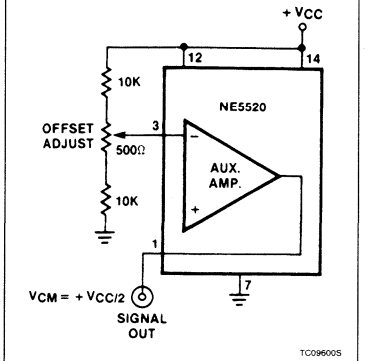


Figure 12. DC Offset Adjust

NE5520 TEMPERATURE COMPENSATION

Internal offset voltages originating in the NE5520 synchronous demodulator require external compensation to obtain best measurement accuracy when operating over the full temperature range. The circuits shown (Figures 15a, b) give a simple approach using a thermistor inserted in series with the offset null resistors to reduce voltage drift to a reasonable level. These tolerances are based on ± 3.5V full-scale output for LVDT displacements each side of physical null. A thermistor having a positive coefficient of +0.7%/°C is used. Obviously, if the total divider resistance is changed, a different thermistor resistance will be required.

DEMODULATOR DISTORTION (OVERDRIVE)

When the demodulator input exceeds $2V_{P-P}$ clipping distortion will increase and must be avoided by controlling oscillator drive to the primary of the LVDT. Figure 16 shows an example of a circuit for attenuating primary excitation using a 1kΩ potentiometer.

The procedure for adjusting the level is simply to:

1. Set LVDT core position for maximum output from the secondary.
2. Monitor the waveform on (Pin 5 demodulator output) and adjust oscillator level for the amplitude just below clipping. Normally, this should result in a maximum of 2 V_{P-P} at Pin 4 of the NE5520 (25°C).

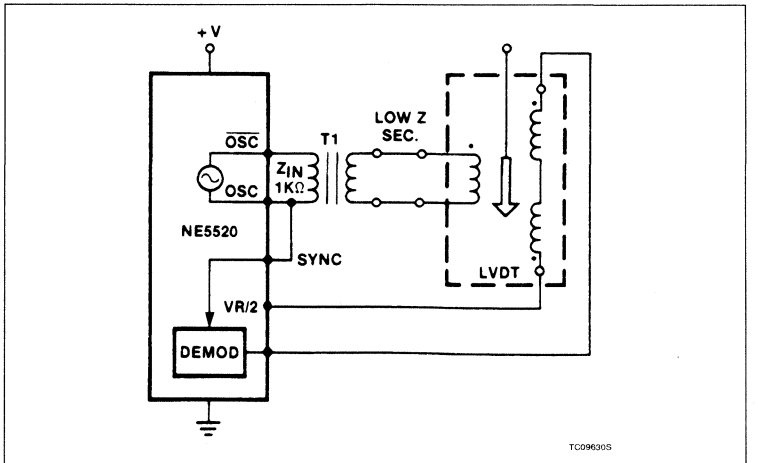


Figure 13. Driving Low-Z LVDTs With the NE/SE5520

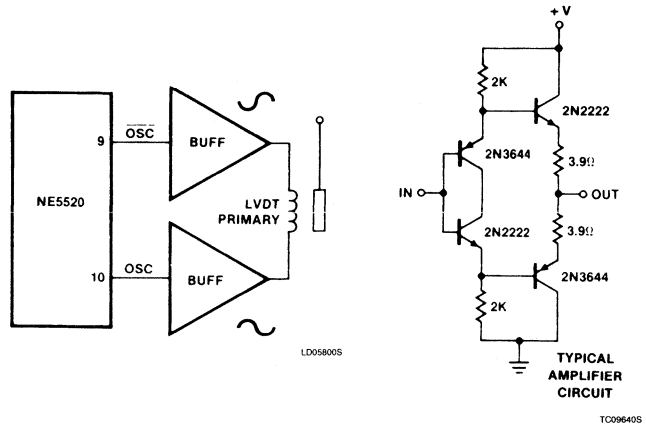
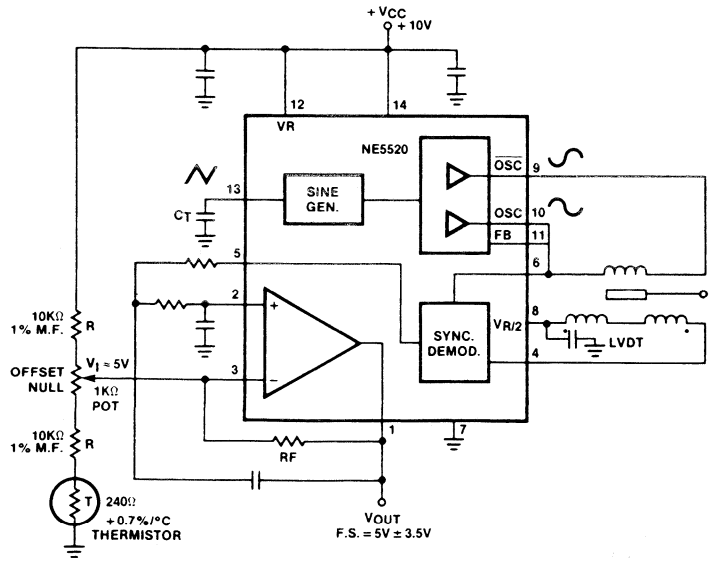


Figure 14. Low-Z LVDT

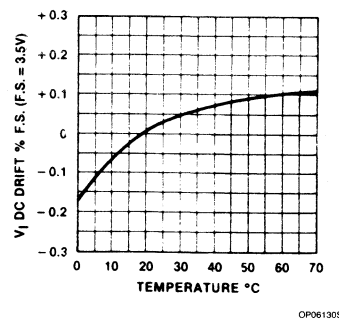
LVDT SECONDARY PHASE ANGLE COMPENSATION BY EXCITATION FREQUENCY

The LVDT has a frequency-dependent phase shift associated with the particular characteristics of the device and its excitation frequency. This phase shift is in addition to the 180° shift which occurs when passing through null position.

By adjusting the frequency of the sine wave excitation a condition results which causes secondary voltage to be in phase with primary excitation. The adjustment of relative primary and secondary phase angles has several effects. First, if the primary excitation is referenced to the synchronous demodulator, as in the NE5520, optimum rectification occurs at zero phase differential between secondary AC phase and demodulator switching relative to the waveform zero crossings. Second, "Exciting an LVDT at its zero phase angle frequency results in minimum sensitivity to frequency and temperature variations" (Schaevitz *Handbook of Measurement and Control*, 1976).



a. LVDT Driver Demodulator With Temperature Compensation 0 – 70°C



b. Thermistor Temperature Compensation

Figure 15

DEMODULATOR SYNC PHASE

A second method of phase compensation of the NE5520 versus the LVDT is to use a variable phase shift network between the oscillator output and the sync input to the NE5520. This is shown in Figure 17. The oscillator frequency remains fixed and the pot is tuned for optimum demodulator phasing.

It is emphasized that an external phasing adjustment as outlined above is not always necessary. Some LVDTs operating in the 1 – 5kHz range will be near zero phase and will need no phase compensation. Experimental evaluation of the prototype design combined with system specifications will be the best means of making this decision.

The waveform photo in Figures 18a and b shows the demodulator output signal when phasing of the synchronous demodulator is correct (a) and improperly adjusted (b).

Proper phasing of the sync signal to the demodulator results in optimum sensitivity and linearity.

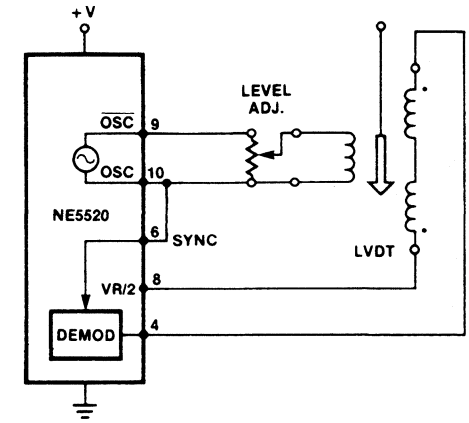


Figure 16. Limiting LVDT Excitation to Prevent Demodulator Distortion

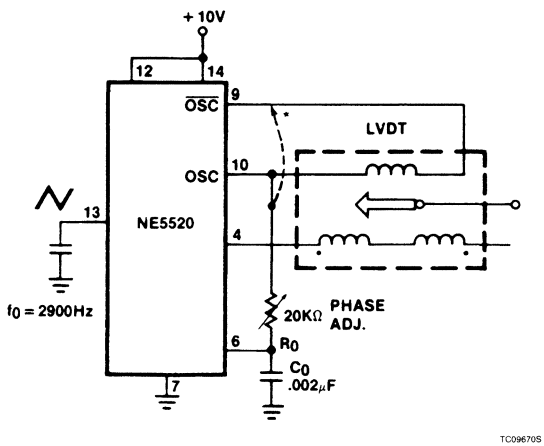
NE5520 LVDT DRIVER DEMODULATOR APPLICATIONS

Operated With a Single Power Supply

The NE5520 may be operated with a single-ended power supply ranging from +5 to 20V.

A very simple motion transducer may be constructed using the circuit shown in Figures 19a and b. The output is biased to one-half the supply voltage. This requires special interface circuitry for the signal readout. One simple method is to use a zero center meter in a bridge configuration, as shown. Displacement now may be measured as a positive or negative meter reading. Readout sensitivity is a function of the particular LVDT and of the gain of the error amplifier. DC offsets may be nulled by using a simple offset adjustment circuit as indicated.

The transducer is centered in its displacement and the offset adjust pot set for a zero meter reading. Once this procedure is completed, the circuit is capable of making measurements based on transducer displacement. Displacement sensitivity is a function of the LVDT transducer rated in volts-per-inch in addition to the transfer gain of the NE5520 demodulator. The input excitation is generally a fixed level as is the LVDT transducer transformer ratio. However, the auxiliary gain stage may be used to adjust the overall system sensitivity. This section of the device is also used to obtain a low-pass active filter for the smoothing of demodulator ripple. The design examples use a simple VCVS low-pass filter which allows gain and cut-off



NOTE:
*Alternate connection may be required for some LVDTs.

Figure 17. External Phase Adjustment

frequency to be adjusted independently. Gain equals ten in the example.

Note that using a single supply results in a DC common-mode voltage at the output of one-half the reference voltage on Pin 12. *This voltage, V_R, may be equal to but not greater than the supply voltage on Pin 14.*

LVDT Measuring Circuit Using a Dual Supply

A second mode of operation makes use of dual power supply. A common choice may be ±5, ±6, or ±10V. Special consideration must be made in properly biasing the internal circuitry to operate under these conditions. Figure 20 shows a simple design for working with ±6V supplies. Special provisions for minimizing DC power supply offsets may be made by using the NE5512 dual op amp as a tracking voltage source and difference amplifier-output buffer (see Figure 9). A second method is to use a dual tracking regulator to supply the NE5520.

LVDT in Closed-Loop Servo

The LVDT provides an excellent method of obtaining position information for closed-loop servo drive systems. Pressure rollers, hydraulic drivers, and motor driven linear motion

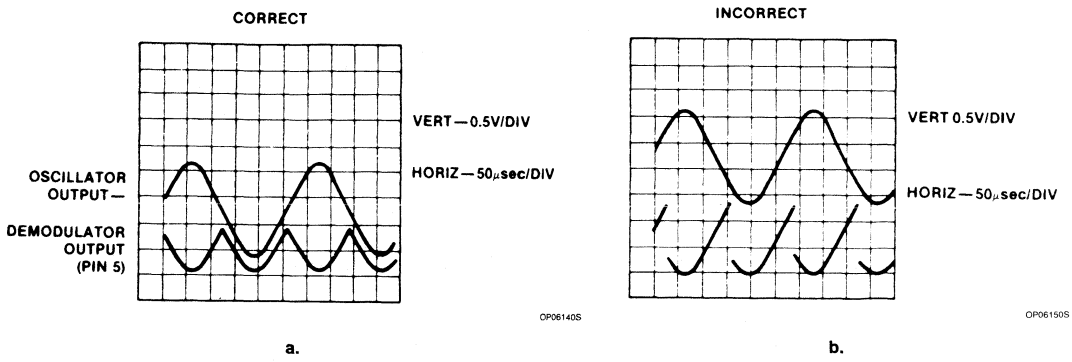


Figure 18. NE5520 Demodulator Phasing

transducers are a few of the general applications which may benefit from the accuracy and speed of response inherent in the LVDT sensor.

A simple block diagram (Figure 21a) shows one possible application in which the NE5520 with LVDT sensor provides accurate position control in a closed-loop servo. Linear motion from millimeters to inches of translational motion are possible using the LVDT technique.

In practice, the position voltage may be the output of a D/A converter which in turn is activated digitally from a controlling microprocessor. Keyboard information or software commands are translated directly into mechanical motion (Figure 21b).

LVDT SIGNAL TRANSMISSION BY CURRENT LOOP

In certain situations the demodulated output signal must be transmitted over long wires or cables before reaching the signal monitoring equipment. The receiver end may consist of chart recorders, digital panel meters and computers or microprocessors. In some systems, many LVDT signals must be monitored from different locations, thus requiring variable wire length between transmitter and receiver producing a different line resistance in each case. If voltage feed were used, signal accuracy would be affected by line resistance. This need for accurate signal transmission necessitates the use of a current loop. A current loop develops a current exactly in proportion to the demodulated LVDT output voltage. It is not affected by line resistance within certain limits governed by the current generator.

One method of current loop transmission uses the $V_{R/2}$ common-mode reference to create a null balance signal circuit which is converted to a bipolar current signal corresponding to the LVDT transducer null (i.e. physical displacement center null position at which zero current occurs). This method is shown in Figure 22 and requires the use of an external dual op amp, half of which is used to provide a buffered reference ($V_{R/2}$) voltage return for the current loop. With $R_2 = 200\Omega$, the current loop sensitivity is 5mA/V of input signal. In all cases, the current output to the loop receiver will remain constant with fixed input voltage (LVDT demodulator), even for varying line resistance up to 600Ω. This resistance must include all wire and load drops in the loop. Various full-scale current limits require different supply voltages and, without external supplies, will be limited by op amp swing characteristics, for to force a given current across $R_L + R_2$ results in an ultimate voltage limit from the op amp output in the current converter as total resistance increases.

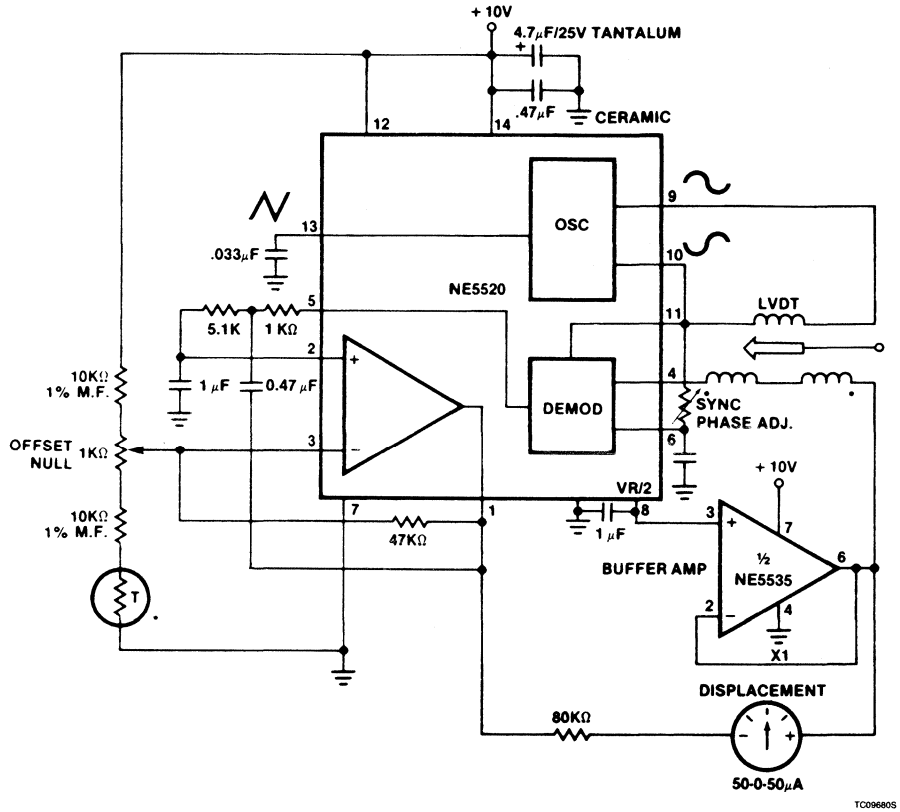
Another method uses an external supply and discrete transistor controlled by the closed-loop op amp referenced to shunt resistor R_{SH} in the emitter return circuit. This, of course, is a unipolar current loop. See Figure 23.

Some systems in common use require two-wire source to include both the device operating current and the signal loop current. Thus the quiescent device current must be nulled out at the receiver end, leaving the residual signal loop current. The NE5520 is not well suited to this particular application since the device standby current is approximately 10mA.

A current loop operated from supply voltage sources at the transducer location is a better choice for the operation of an output signal loop where long lines must carry locally-generated LVDT signals after demodulation back to the monitor site.

POSITIONING THE NE5520 LVDT 3-WIRE REMOTE DRIVER DEMODULATOR SENSING HEAD

The NE5520 may be placed in close proximity to the LVDT transducer, provided the environment stays within device specifications. This physical arrangement allows only DC supply and low frequency signal lines (3 wires) being run between the transducer-conditioner unit and the signal processing station as shown in Figure 24.



NOTE:
Thermistor 240Ω + 0.7%/°C

Figure 19a. LVDT Measuring Gauge

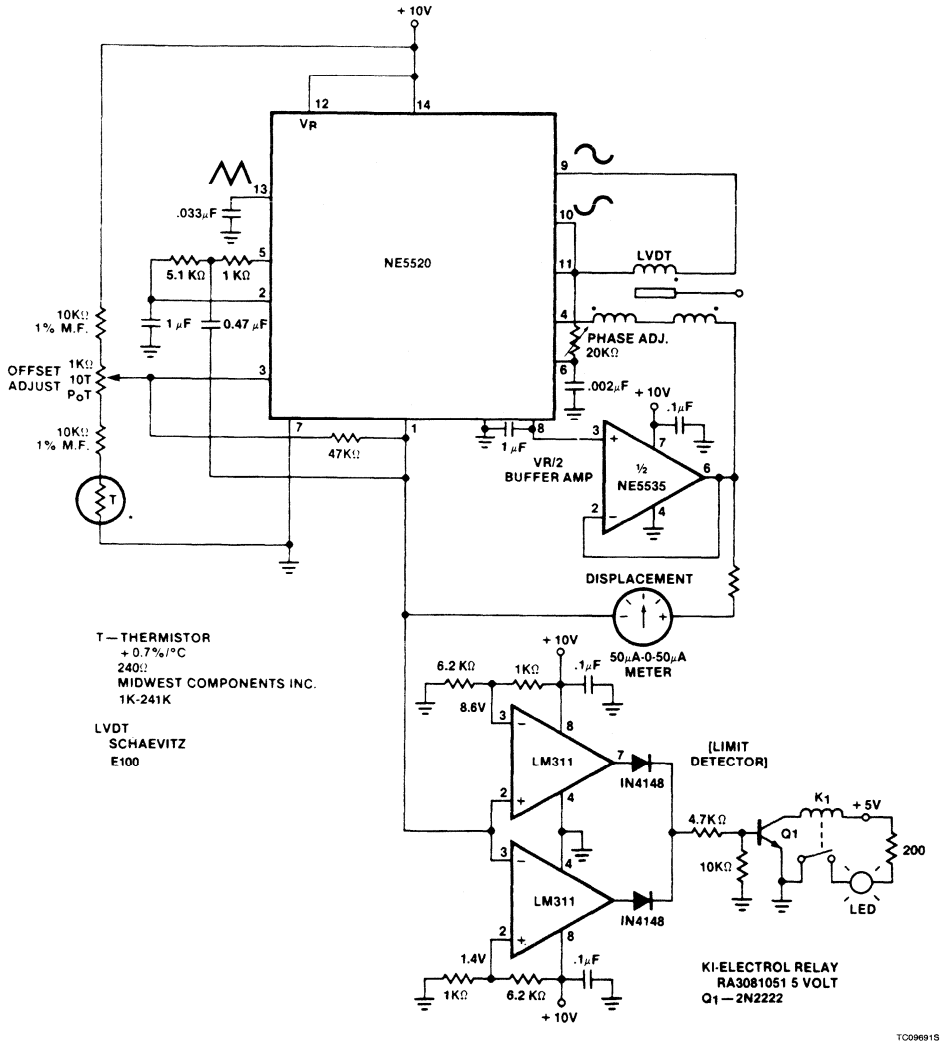


Figure 19b. NE5520 LVDT Measuring Circuit With Limit Detector

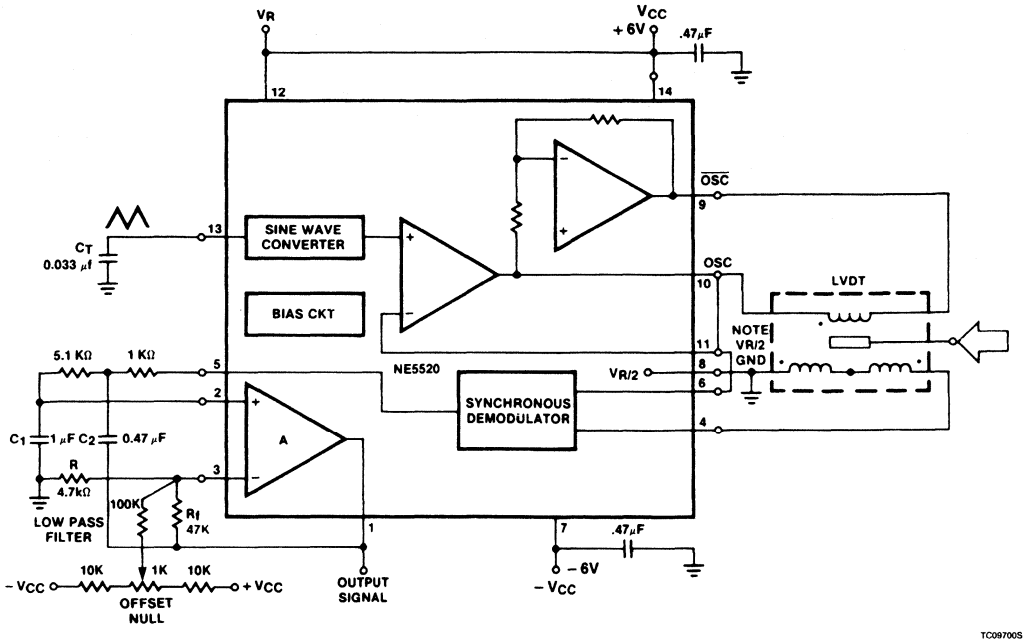
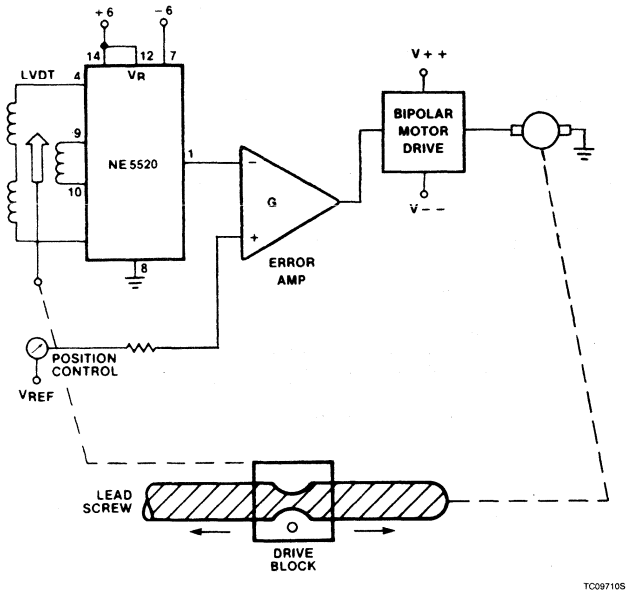
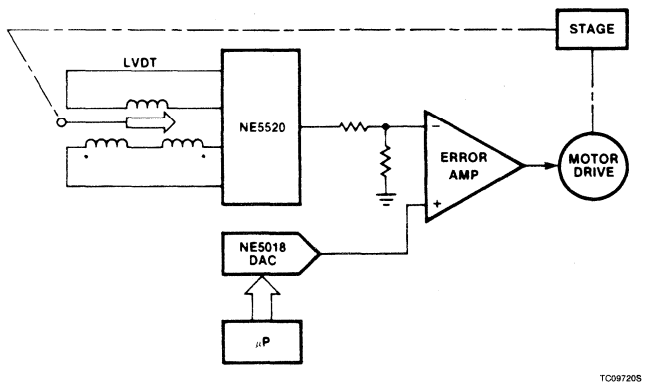


Figure 20. NE5520 LVDT Driver-Demodulator (f_O = 2900Hz)



a. NE5520 Position Servo With LVDT Sensor



b. Microprocessor Control Interface

Figure 21

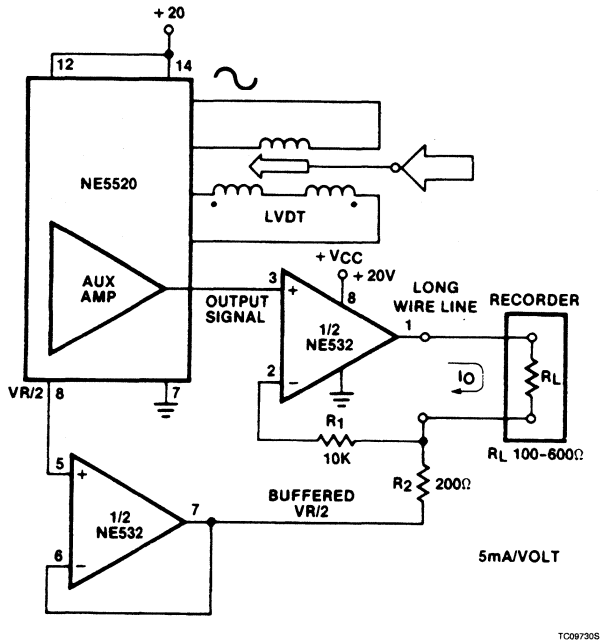
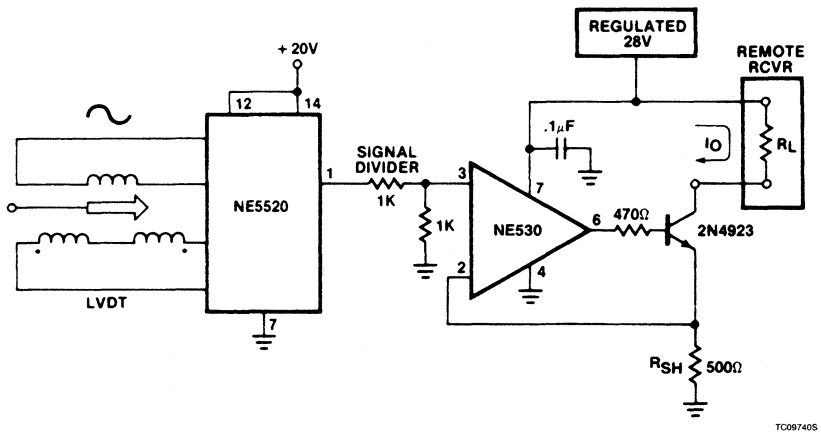


Figure 22. NE5520 With Bipolar Current Loop Output ± 10mA FS — Single Supply Operation



NOTES:
- Sensitivity 2mA/V.
- LVDT null occurs at 10mA outpt, i.e., half-scale.

Figure 23. NE5520 With Unipolar Current Source

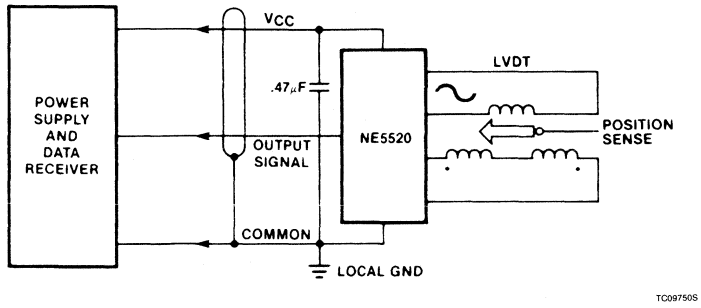


Figure 24. Positioning the NE/SE5520 LVDT 3-Wire Remote Demodulator Sensing Head

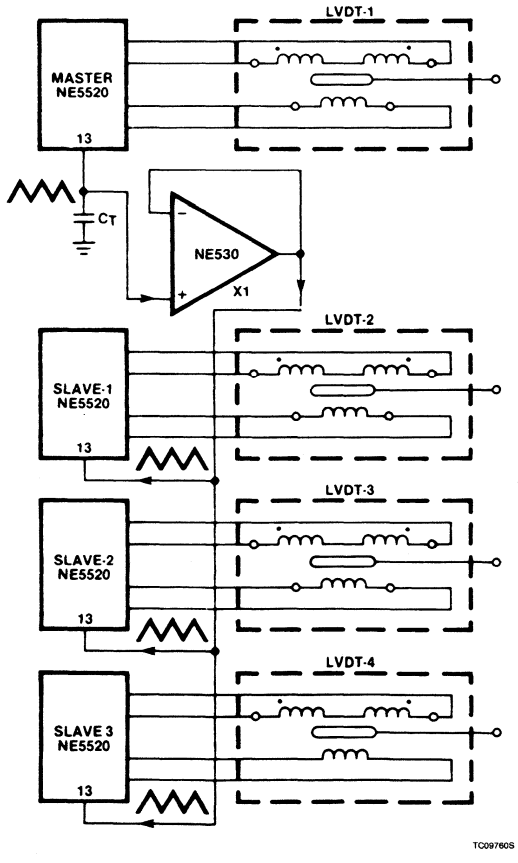


Figure 25. Multiple Transducer Operation — Synchronous Oscillator Mode

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Handbook of Integrated-Circuit Operational Amplifiers, by George B. Rutkowski, Prentice Hall 1975, Englewood Cliffs, New Jersey.

AN1180

A Microprocessor-Based Servo-Loop for Linear Position Control

Application Note

ABSTRACT

A simple linear position servo-loop control system using a small amount of specialized ICs and electro-mechanical hardware can control the position of a cutting blade, pointer, or other machine tool to within 0.010 inch over an effective range of several inches. The system uses a unique single-chip LVDT signal conditioning circuit and an 8-bit analog-to-digital converter on the front end for monitoring the linear position. An 8-bit DAC system and a novel switching motor drive circuit, on the back end, is used to turn-on/turn-off a fractional HP motor which repositions the lead screw assembly. Control is provided by a low-cost MOS microprocessor with a dedicated memory space, and a simplified software subroutine.

INTRODUCTION

Linear position servo-loop controllers have a wide range of industrial applications including machine tools, robotics and automated process control. Servo-loops may also be used in the control mechanisms of aircraft, as a way of programming and controlling the position of an aileron, or wing flap. In an industrial environment such as a machine shop, a linear position control could dictate the cutting position of a blade on a turning lathe. It could also dictate the position of a robot assembler's arm.

Up to now, the electronic package used to perform this electro mechanical function was large, cumbersome, and often very expensive. With the system shown here, the parts count — and consequently, the expense — is kept to a minimum. Apart from the electro-mechanical ends of the servo-control loop, the entire electronics package can fit comfortably into a 12 × 8 × 6 inch enclosure, with room left over for power supply components.

The system (Figure 1, Block Diagram) uses a Signetics NE5520 specialized LVDT signal conditioner, a Signetics NE5034 8-bit high speed analog-to-digital converter, a Signetics NE5018 8-bit D/A converter system, and a Signetics NE5560 switching regulator circuit which performs the motor control functions in conjunction with a matched pair of complementary power transistors. Loop control is performed by an industry-standard 8048 processor, also manufactured by Signetics, with very simple software subroutines. The outboard electro-mechanicaL elements are an E1000 LVDT manufactured by Schavitz Engineering (Pennsauken, NJ), and a 10-inch lead screw driven through a 15:1 speed reduction worm gear. The motor is a Globe 100A 565 permanent magnet field type rated at 12VDC.

Although the system is compact and low cost, linear position can be controlled down to 0.010 inches over a 2-inch range. With the motor turning at 200RPM, and a lead screw of 1mm pitch, the response time of the servo system is within 10 second max over its full 2-inch range. It should be noted that various elements in the system can be changed to provide a wider linear position control range, tighter resolution, or a faster response time. The system, as demonstrated, has many useful elements which can be taken together as a convenient control package, or as the basic applications model for more complex control systems.

THE SYSTEM IN BRIEF

As shown in Figure 1, the starting point of the control loop is the LVDT device. This, in conjunction with the NE5520 LVDT signal conditioner circuit, will provide a precise linear DC voltage representation of the linear position. The output voltage will vary over a range of 1.5 to 3.5V. This bipolar voltage output is translated into a current which feeds the NE5034 8-bit analog-to-digital converter. This will provide an 8-bit digital input code to the 8048 processor. Set point data for the loop control is provided by a separate keypad entry into the 8048.

The job of the 8048 processor, in turn, is to compare the set point data with the actual position data provided by the A/D. If the data is the same (within predetermined limits), the processor need do nothing. If the set point and A/D data is different, however, the processor will then latch in a new digital code in the input register of the NE5018 8-bit D/A converter. That new input code, essentially unipolar, will yield a linear voltage output. This voltage output, in turn, is fed to a switching regulator circuit, and is used to control the duty cycle of the regulator. The duty cycle of the regulator, through a power transistor switching scheme, will turn-on and control both the speed and direction of an outboard industrial motor. The motor will remain on until the position of its pointer conforms with the set point given the processor by keypad entry. Over a long travel, the motor pointer may overshoot its position. In that instance, the LVDT-A/D combination registers the new position to the processor, the processor puts a new code into the D/A, and the switching regulator starts on a new duty cycle, all designed to bring the position pointer back

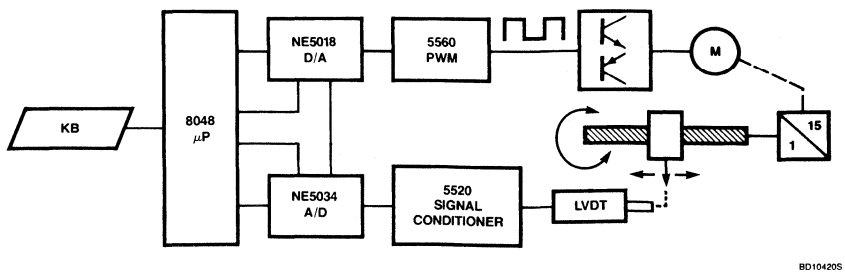


Figure 1

A Microprocessor-Based Servo-Loop for Linear Position Control AN1180

into line. In this manner the servo loop controller can dictate linear position down to hundredths of an inch, and with a very comfortable response time for machine tool applications.

The current software package is offered in the interest of simplicity. A more sophisticated program will alleviate overshoot in the motor response, as well as take full advantage of the capabilities of the 8048.

LVDT: PRECISE LINEAR POSITION SENSING

The key element of the system is the LVDT. As suggested in Figure 2, the Linear Variable Differential Transformer is essentially a transformer wound around a hollow metal cylinder, while the two secondaries — each wound 180° out-of-phase with each other — occupy opposite ends of the cylinder. The core of the transformer is a movable metal cylinder, which can slide horizontally (up-and-down or back-and-forth) through the inside of the transformer.

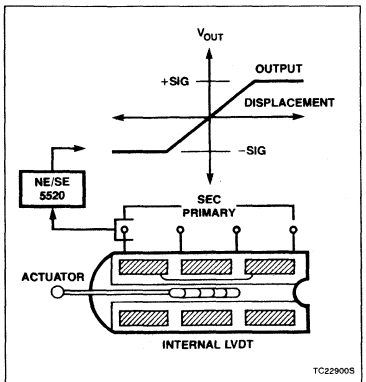


Figure 2. LVDT System Transfer Function

When an AC voltage is applied to the primary of this transformer, the magnetic flux will pass through the metal core to the secondaries. The amount of flux transferred to each secondary will vary with the position of the metal slug inside the cylinder. Where the metal slug is closer to one secondary coil, that coil will receive the greatest proportion of the primary voltage, while the other secondary, at the opposite end of the cylinder, will receive a minimal transfer. If the transformer core shifts to the opposite end of the cylinder, the secondary coil at that end will receive a greater voltage transfer, while the other secondary will experience a drop. With the transformer core at the exact center of the transformer — the null position — the voltage transferred to each secondary will be exactly equal, though opposite in phase, and their sum will be zero.

Because the position of the cylindrical core will affect the voltage rise or fall in each secondary, this system can be used to measure linear position with extreme precision and linearity. LVDTs manufactured by Schavitz Engineering, for example, can measure linear position over a range of 10 inches or more, with resolution in some cases down to 0.5 microns. Full scale accuracy is within 0.25% typical. Linearity is on the order of 0.1%, although linearity better than 0.05% is not uncommon in many position measurement systems.

Although the LVDT measurement technology has been with us for thirty years or more, its widespread use has been impeded by the complexity of the electronic signal conditioning package required to harness an LVDT. As a starting point, an LVDT requires a very stable AC voltage to drive the primary coils. This voltage must be relatively stable in frequency and amplitude, regardless of shifts in temperature and impedance of the LVDT primary coil. On the secondary coils, the LVDT would require a relatively sensitive voltage measuring system, including a synchronous demodulator to pull-out the AC component, and translate the voltage in each of the secondaries into a linear DC component. This DC component, in turn, must be amplified in order to register on a meter or some other measuring system. In operation, the AC drive voltage must have fairly low distortion components, and must be fairly stable in amplitude and frequency, regardless of the impedance shift the LVDT primary coil will likely exhibit over temperature. The synchronous demodulator, in turn, must track the oscillator shifts with temperature in order to maintain the same phase relationship between input and output voltages, and, therefore, retain the same relative linearity over temperature. Because of these requirements, the signal conditioning package for an LVDT device has traditionally been large, complex and expensive.

THE NE5520: A SINGLE-CHIP LVDT SIGNAL CONDITIONER

The NE5520, introduced by Signetics, is the very first monolithic LVDT signal conditioning device. As shown by the block diagram in Figure 3, the device includes a low-distortion sine wave oscillator, a synchronous demodulator circuit, a stable on-chip voltage reference, and a high-output auxiliary op amp. The device will function comfortably from a single supply rail in the range of 5 to 25, or dual supply rails in the range of ±5 to ±12, with less than 8.5mA current consumption.

The oscillator will provide an AC voltage up to $V_{REF/4}$ RMS in the frequency range of 1kHz to 20kHz (controlled by an external capacitor), with no more than 0.05%/°C variation in the temperature range from 0 to 70°C. Output voltage components will be DC in the range 1.5 to 8.5V depending on the supply voltage.

Hook up of the device in the servo-control loop is relatively easy: The on-chip auxiliary amplifier will provide a 0 to 10V output swing, centered at 5V, which can be fed to the input of an A/D converter, in most cases without additional amplification or signal conditioning. Figure 4, in fact, shows the NE5520 connected to a NE5034 8-bit A/D converter. The two components comprise the entire front end of the servo-loop controller. In the circuit shown, the LVDT signal conditioner is hooked up to a single +15V supply rail, with a separate +10V reference voltage input. In operation, the reference voltage at Pin 12 input should be provided by a closely regulated voltage to ensure accuracy of the LVDT measurement system.

Also in the circuit shown, the 20kΩ resistor in the feedback loop of the NE5520 auxiliary amplifier provides a gain of 5 for output voltage of 1.5 to 5.5V using a Schavitz E1000 LVDT over a range of ±1 from the null position. Offset adjustment of the auxiliary amplifier is provided by the 1kΩ trimmer.

THE NE5034: FAST 8-BIT CONVERSIONS

The output of the NE5520 is fed directly to the NE5034 through a 5k resistor. The NE5034 8-bit A/D converter has two special virtues: First, it is one of the few A/D converters available that seeks a current input. It will accept a wide range of analog voltage inputs, with the aid of a current scaling resistor. In the circuit shown, the reference resistor and the 5k input resistor should scale the current input to 1.0mA nominal at full scale. In other words, a 1.0mA current coming through Pin 15 of the NE5034 should produce a full scale digital code. The 10k resistor here will translate a 5V output voltage swing of the NE5520 into 1.0mA at the input of the NE5034.

A Microprocessor-Based Servo-Loop for Linear Position Control AN1180

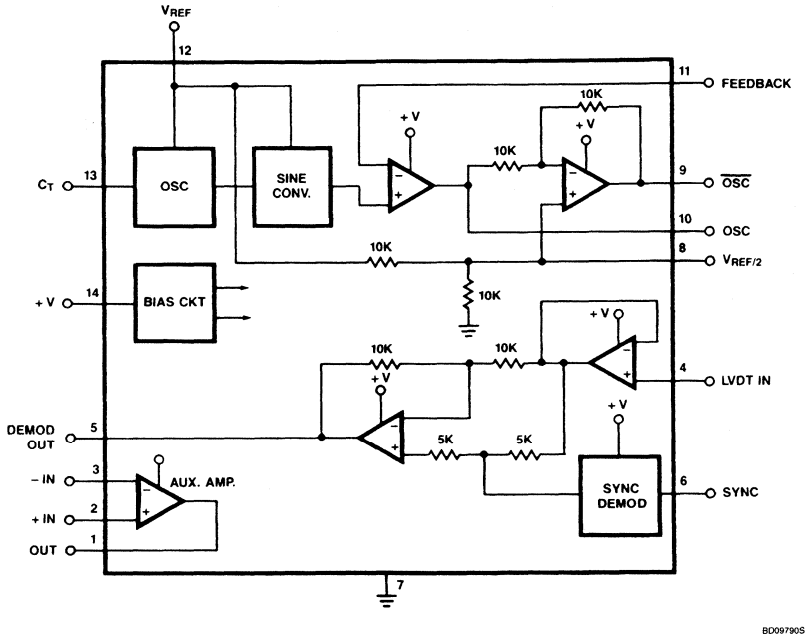


Figure 3. NE5520 Block Diagram

The second feature of the NE5034 is that its fast conversion speed, internal clock and relatively easy sequencing means it can be connected directly with a dedicated processor like the 8048. The NE5034 has a self-generating internal clock, which can provide a complete successive approximation 8-bit conversion in as little as 17μs. This means that the converter need not function on the same system clock as the processor. The processor must instruct the NE5034 to convert by putting a start pulse — high to low to high (trigger on the positive-going edge) — on Pin 10 of the converter. About 100ns before the end of conversion, the converter will raise a "data ready" flag, and the processor will respond with a latching pulse on Output Enable (OE). (See Timing Sequence, Figure 5). All eight bits will be latched at Pins 1 through 8 on the 5034.

The 8048 processor, in turn, will provide pulses to trigger the OE line, in addition to Read/Write strobes. The processor can be fed data through either one of its bidirectional ports, and stored on-chip in its resident RAM array, although the system demonstrated uses only one I/O port.

COMPLETING THE CONTROL LOOP

The complete control loop, using an NE5018 D/A converter system, an NE5560 switching regulator, and a set of Darlington-configured power transistors is shown in Figure 6. In operation, the real precision of the servo-loop control is in the sophistication of the monitoring front end. Here, an LVDT in conjunction with a specialized signal conditioning device and an 8-bit A/D converter, will recognize position variations with 0.010-inch over a 2-inch effective range. The control loop, however, need not be as precise. The basic response of the microprocessor to a discrepancy between the position indicated in its instructions, and the position actually measured, will be only one of three basic instructions to the motor: "On-Right", "On-Left", or "Hold". These instructions can be latched with a four-bit code and continually repeated until the servo-loop finds the position indicated in its instructions. A 6- or 8-bit code will not greatly affect the response time of the servo, but will increase its precision. (This will be largely dependent on the precision of the input sendor/converter combination.)

In the system shown, the NE5018 was selected for convenience. The single-chip DAC system includes D/A converter, input data latches, a voltage reference, and an output op amp. In operation, the data from the processor port is latched directly in the DAC register, using the Latch Enable (LE) Pin 10 of the 5018, and a binary instruction code from the 8048's output port. As an alternative, the 5018 latches can be latched permanently open and transparent by tying LE low. Zero scale adjustment of the DAC can be accomplished by a 20kΩ trimmer between the supply rails and the output pin of the DAC, while the full scale offset can be trimmed with a 10kΩ trimmer across Pins 12 and 14 of the 5018.

A Microprocessor-Based Servo-Loop for Linear Position Control AN1180

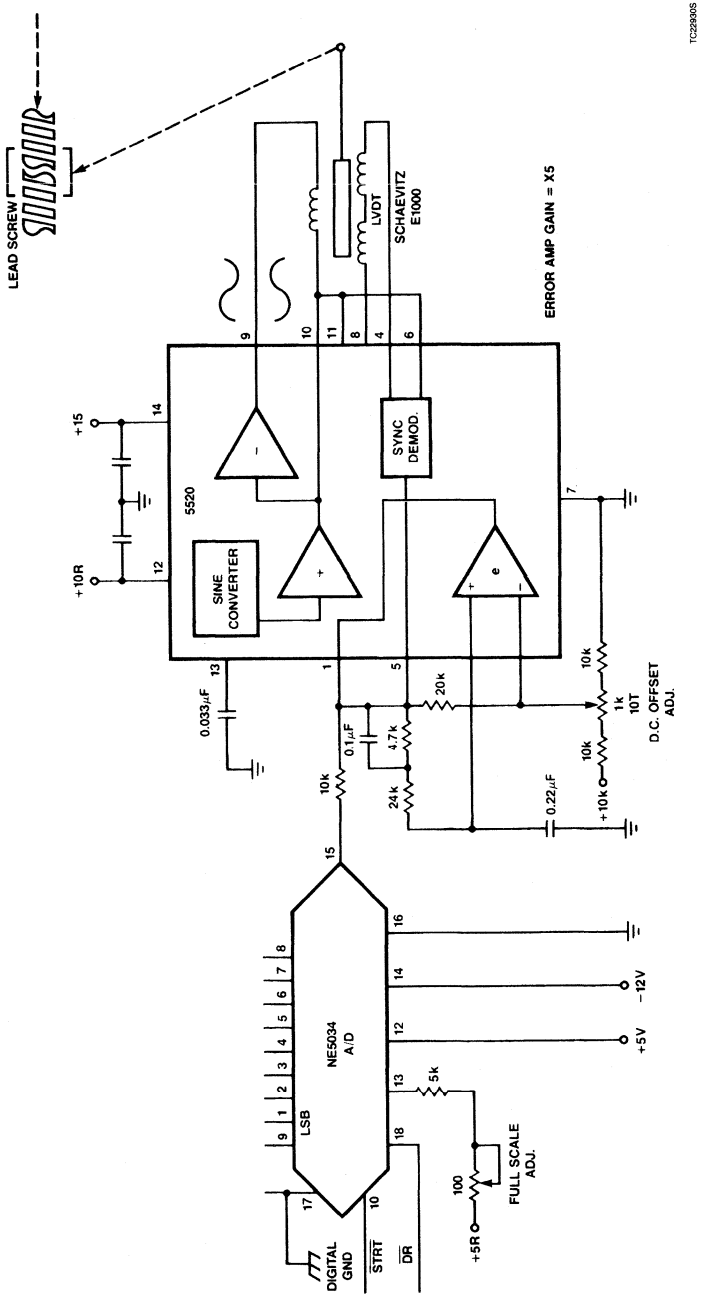


Figure 4

A Microprocessor-Based Servo-Loop for Linear Position Control AN1180

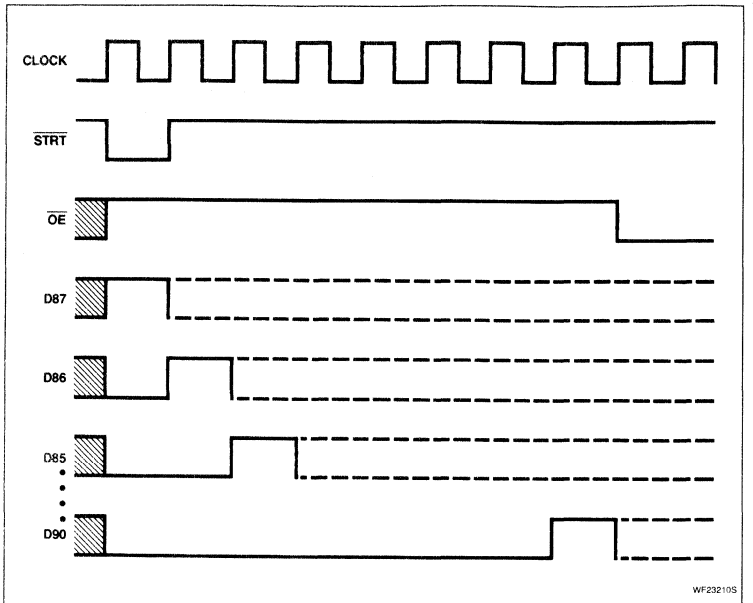
The output of the NE5018, a unipolar voltage between 0 and 7.3V, is fed into Pin 5 of the NE5560 switching regulator. The single-ended output of the switcher is fed into a pulsed bidirectional drive circuit which feeds the Darlington-configured power transistors. This bridge driver circuit puts a variable duty cycle on the motor coils, and will be sufficient to drive the permanent magnet motor, and control its direction. In operation, a voltage below 3.5V on Pin 5 of the regulator will turn the motor in one direction, while a voltage above the 3.5V null point on the input pin will turn the motor in the opposite direction. The 3.5V on the input, in the circuit shown, will match a 50% duty cycle in the 5560 and provide an active hold state on for the motor coils. In this "Hold" condition, the motor armature is driven in both directions at the same time and is effectively in a "brake" or "stall" condition. Because of this, restoring torque is immediately available the instant the voltage on Pin 5 changes from its 3.5V null point.

Safety features of the 5560, particularly overcurrent sensing and shut down, protect the motor/drive circuit from an overdrive condition. (Other safety features, such as soft start and over-voltage protection, are not used in this application.)

One of the techniques for harnessing a switching regulator to the problems of motor control is to match the duty cycle of the switcher with the RPM of the motor used. In all circuits of this kind, a duty cycle of 50% on the regulator will produce exactly zero RPM from the motor. Varying the duty cycle of the switcher either up or down from the 50% value will increase the other. The exact relationship for the components used is shown in Figure 7a. Also shown is the relationship to the Hexidecimal input codes to the D/A converters from the microprocessor.

SIMPLIFIED INSTRUCTION SET

In the system shown, the 8048 is given its instruction set by keypad entry. For simplicity, we are using a 2 digit Hexidecimal code. The actual relationship between the Hexidecimal input and the linear position is shown in Figure 7b. Because the 8048 processor carries its own resident ROM, which can be dedicated to a specific function, — for example, a look-up table which translates Hexidecimal codes into motor speed/position instructions to a D/A converter — the keyboard entry requirements and the input data the processor responds to can be extremely simple. The basic flow chart for the 8048 processor in this particular application is shown in Figure 8. As indicated, the processor will essentially loop up the appropriate duty cycle required, and bring set point (keypad entered) data in line with the actual position data indicated by the A/D converter.



NOTES:
1. $\overline{OE}$ = '0'.
2. See 'Short-Cycle' section.

Figure 5. NE5034 Timing Diagam

SUMMARY AND CONCLUSIONS

While the system shown represents a useful position control loop, it is actually the model for a wide variety of industrial control systems. Higher resolution, for example, down to one mil can be obtained simply by increasing the resolution of the A/D converter, although the costs of the system will begin to increase dramatically. The 8048 similarly can be programmed to accommodate wider input data bytes, and set point data from another port. A robot assembler, for example, can use set point data obtained from a visual pattern recognition system (e.g., an optical scanner, amplifier, and A/D converter combination) to control or dictate the position of the linear servo-loop.

Other types of measurement and control systems, in turn, can follow the same format and use practically the same components. A temperature measurement control system, for example, could harness a thermocouple junction, a specialized amplifier, 5034 A/D converter, an 8048 processor (with a new instruction set), a 5018 D/A converter and a set of heating/cooling coils (driven by power transistors) in the control loop. A similar measurement system can be harnessed to control pressure, etc.

In so far as the A/D converter, the dedicated μP and the D/A converter components remain the same, the system will have remarkable versatility for industrial control loops. But the additional benefits of a precise linear position sensing mechanism using an LVDT and the 5520, and the practical highly-efficient means of controlling motor speed/position with a 5560 switching regulator, give this system added benefits as a servo-position controller.

ACKNOWLEDGEMENTS

Thanks to Alex Goldberger and James Goodhart of Signetics for help and advice on the 8048 interface requirements.

(The complete system is shown in Figure 9.)

A Microprocessor-Based Servo-Loop for Linear Position Control AN1180

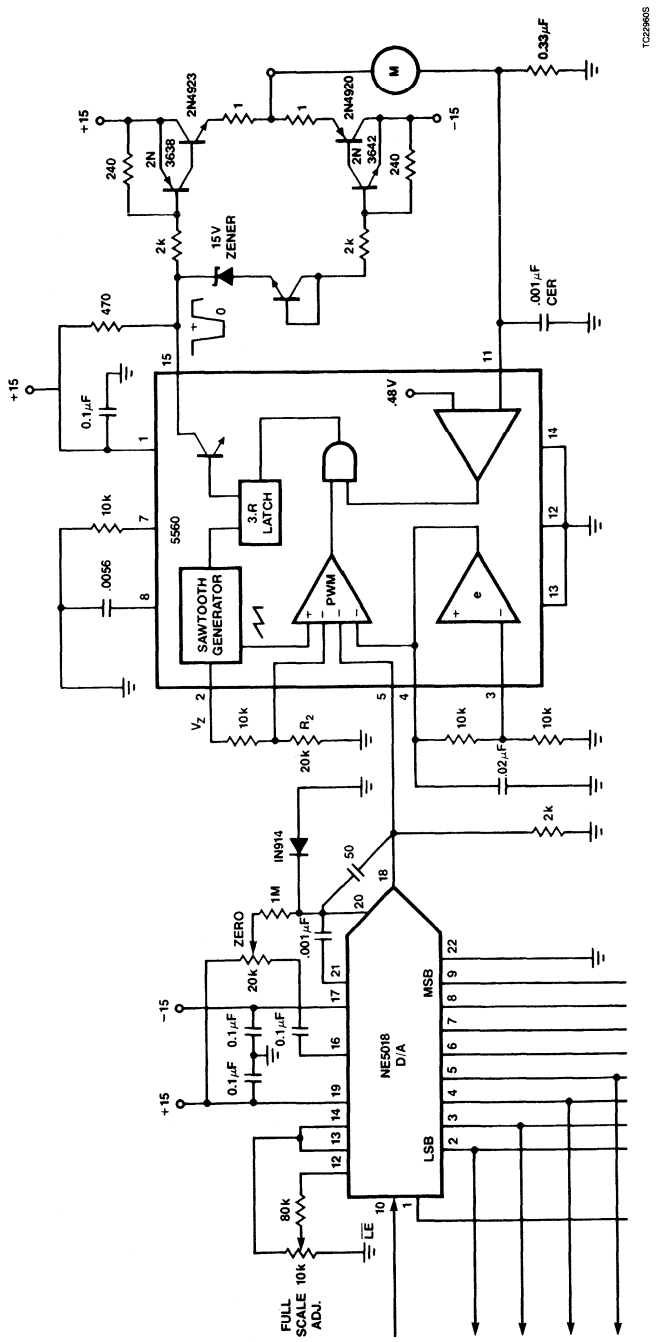
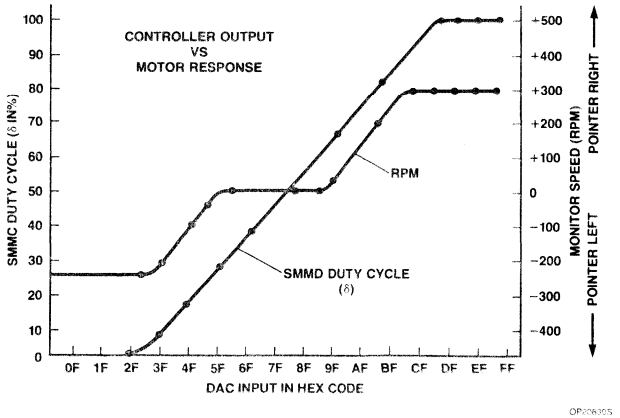
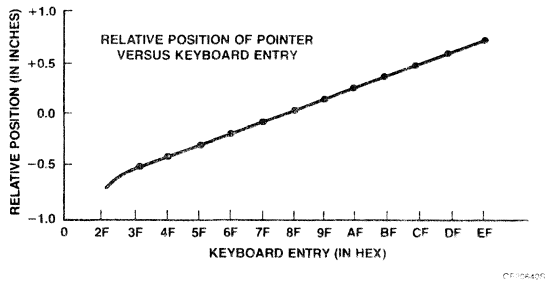


Figure 6


CONTROLLER OUTPUT
VS
MOTOR RESPONSE
SMMC DUTY CYCLE (δ IN%)
MONITOR SPEED (RPM)
POINTER RIGHT
POINTER LEFT
RPM
SMMD DUTY CYCLE
(δ)
100
90
80
70
60
50
40
30
20
10
0
+500
+400
+300
+200
+100
0
−100
−200
−300
−400
0F 1F 2F 3F 4F 5F 6F 7F 8F 9F AF BF CF DF EF FF
DAC INPUT IN HEX CODE

a.


RELATIVE POSITION OF POINTER
VERSUS KEYBOARD ENTRY
RELATIVE POSITION (IN INCHES)
+1.0
+0.5
0.0
−0.5
−1.0
0 2F 3F 4F 5F 6F 7F 8F 9F AF BF CF DF EF
KEYBOARD ENTRY (IN HEX)

b.

Figure 7

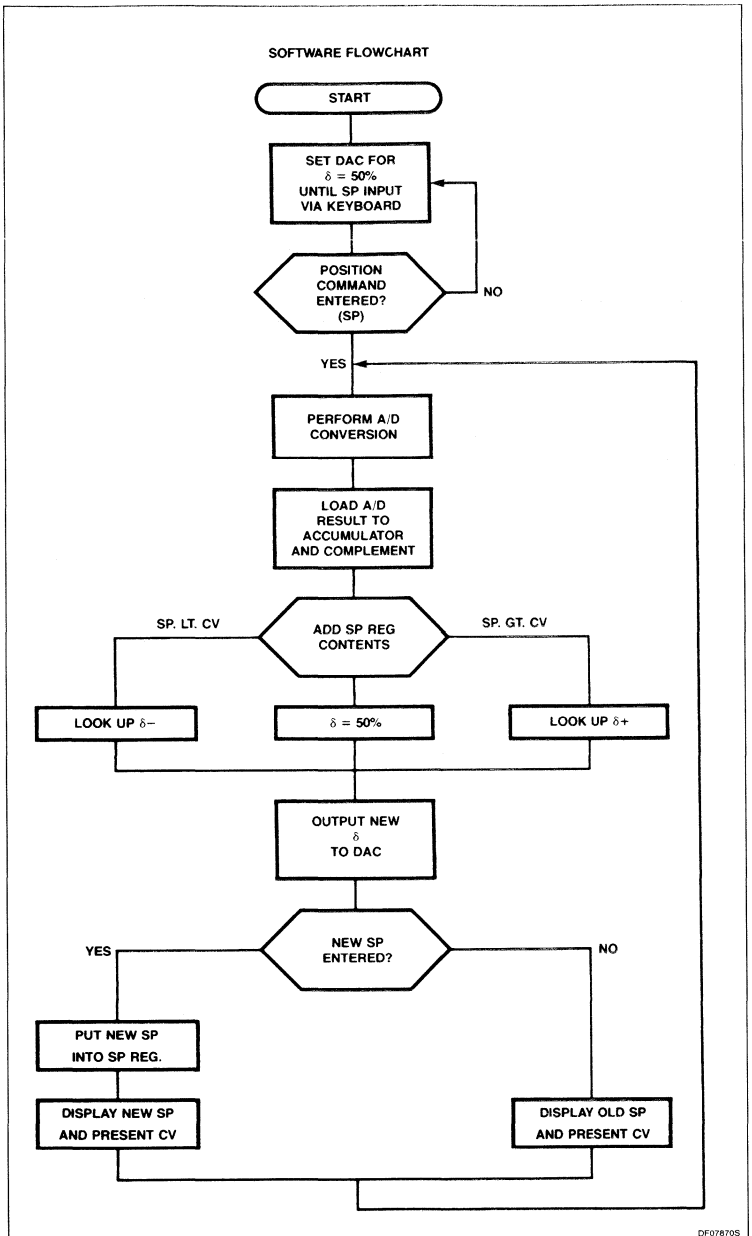

SOFTWARE FLOWCHART
START
SET DAC FOR
δ = 50%
UNTIL SP INPUT
VIA KEYBOARD
POSITION
COMMAND
ENTERED?
(SP)
NO
YES
PERFORM A/D
CONVERSION
LOAD A/D
RESULT TO
ACCUMULATOR
AND COMPLEMENT
SP. LT. CV
ADD SP REG
CONTENTS
SP. GT. CV
LOOK UP δ−
δ = 50%
LOOK UP δ+
OUTPUT NEW
δ
TO DAC
YES
NEW SP
ENTERED?
NO
PUT NEW SP
INTO SP REG.
DISPLAY NEW SP
AND PRESENT CV
DISPLAY OLD SP
AND PRESENT CV
DF07870S

Figure 8

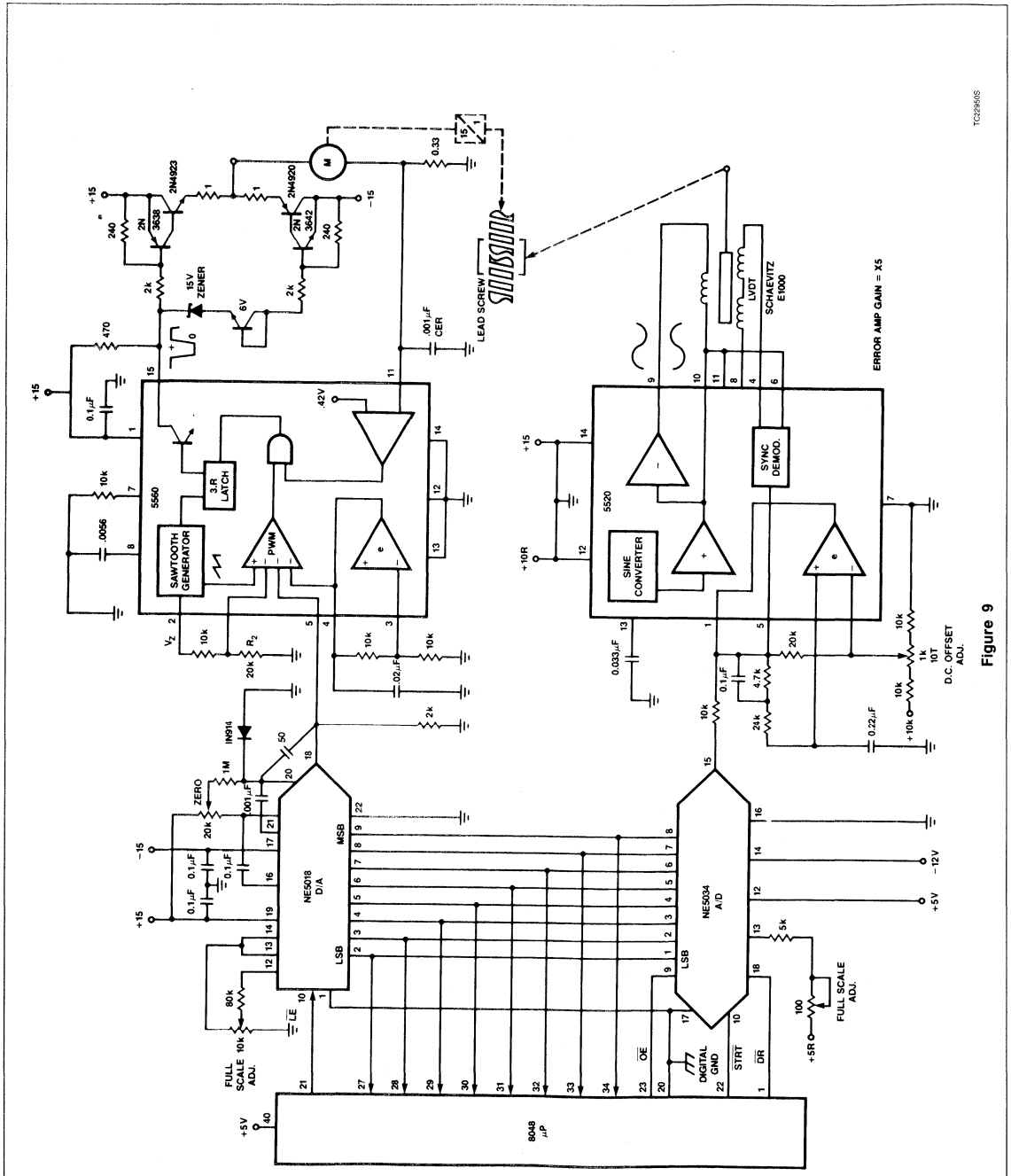

LEAD SCREW
SCHAEVITZ E100
LVDT
ERROR AMP GAIN = X5
5560
SAWTOOTH GENERATOR
PWM
3-R LATCH
5520
SINE CONVERTER
SYNC DEMOD.
NE5018 D/A
NE5034 A/D
8048 µP
MSB
LSB
ZERO
FULL SCALE ADJ.
D.C. OFFSET ADJ.
DIGITAL GND
TC22950S

Figure 9

A Microprocessor-Based Servo-Loop for Linear Position Control AN1180

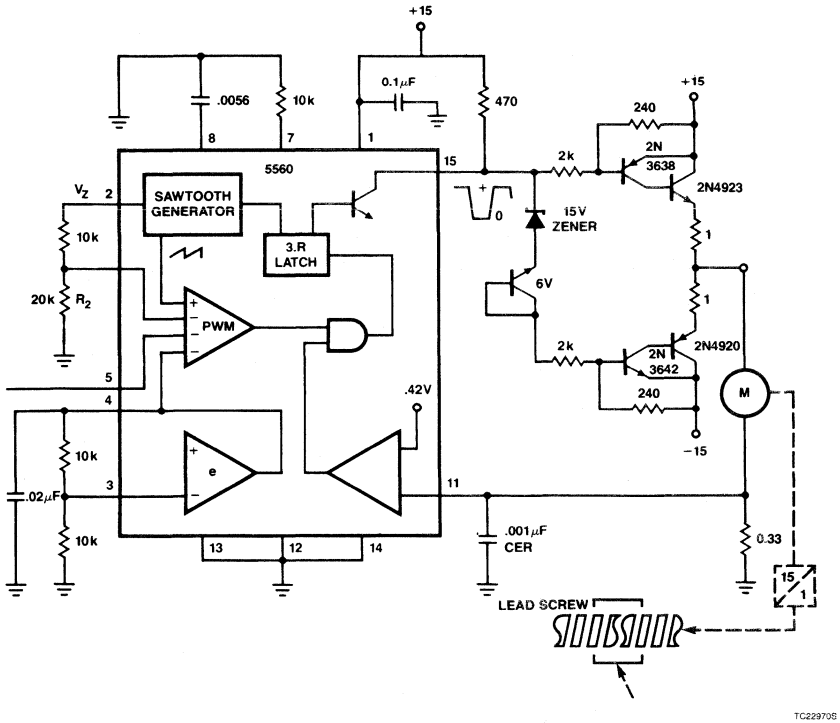


Figure 10

AN1181

NE/SE5521 Simplifies Modulated Light Source Design

Application Note

Photoelectric light sources and detectors are widely used for detecting motion and the absence or presence of objects. The major advantage with photoelectric sensors is that one can sense the target without making any physical contact with it. Although the NE5521 chip is designed to interface with position transducers, it is possible to take advantage of the chip's functional blocks to configure a transmitter and a receiver for a modulated light source device (see Figure 1).

By using an incandescent light source (or an LED because of its long life) and a photosensor which produces current in response to the infrared (IR) light striking it, a transimpedance amplifier will convert the photosensor current to voltage. However, there are several disadvantages with the above approach. Incandescent light source devices cannot be used outdoors in the sunlight or near high intensity sources such as welding arcs, strobe lamps, and mercury lamps, because the IR light radiated from such sources can provide a false output at the receiver. Also, they are generally not recommended for applications where vibration can cause misalignment between the emitter and the receiver.

By frequency modulating the transmitter and tuning the receiver to respond only to the modulating frequency, undesirable modulation frequencies can be electronically filtered out. Due to the high degree of ambient light rejection and noise immunity, the modulated light source devices are thus not significantly affected by direct or diffused exposure to sunlight or by indirect or diffused exposure to mercury lamps or welding arcs. Ambient light rejection can be increased further by tuning the receiver to look for the proper phase of the modulating signal. Modulated light source devices also offer the advantage of greater scanning distance, greater penetration through contaminated environments, and effective use for applications where the emitter and/or receiver may be subject to high vibration.

For the circuit in Figure 1, the oscillator output of the NE5521 chip produces a sine wave referenced to $V_{R/2}$ (in this case 5V) which causes the LM311 comparator to pulse the LED (Light Emitting Diode) at a high current level. In response to such an excitation, the LED produces high energy infrared pulses that can travel long distances and penetrate severely contaminated environments.

The photodiode in the photoreceiver produces pulsating currents in response to the IR light striking it. A pulsed signal thus appears at the anode of the photodiode. The uncommitted amplifier of the NE5521 chip is configured as an AC-coupled amplifier with gain. Keep in mind that ambient light produces a DC voltage at the photoreceiver; however, capacitor C_1 blocks the DC voltage and allows only AC signals to pass through. The cutoff frequency is given by the following equation:

$$f_{CO} = \frac{1}{(2\pi R_1 C_1)}$$

At the frequency of interest, you can consider the capacitor to be a short circuit. Thus the uncommitted amplifier operates as an inverter with gain, the gain being determined by the ratio of R_2 and R_1. Since the non-inverting input of the amplifier is connected to the $V_{R/2}$ pin, the AC signal arising from the photoreceiver is referenced to $V_{R/2}$.

The receiver part of the NE5521 chip is comprised of the synchronous demodulator which provides precise rectification of the amplified photoreceiver signal in sync with the modulating signal of the LED. The modulating signal of the LED also drives the demodulator's comparator, which compares the modulating signal with the $V_{R/2}$ reference voltage (Figure 2). When the demodulator's sync input signal is below $V_{R/2}$, the demodulator inverts the AC input signal. When the sync signal is above the $V_{R/2}$ voltage, however, the AC signal passes through the follower to the output. As a result, the demodulator's full wave rectification occurs in sync with the demodulator's input signal. Synchronously rectifying (demodulating) the square wave AC signal from the photoreceiver produces a DC signal at the demodulator output (Figure 3). A simple RC filter at the demodulator output filters out any spurious noise and transients generated at the switching points. When the IR light source is blocked, no AC signal arises from the photoreceiver. Thus, the demodulator output is biased at $V_{R/2}$ (5V in this case). For the circuit in Figure 1, the voltage at the output of the filter is 2.9V when the light source is uninterrupted. However, the output voltage changes to 5V when the light source is interrupted. One can thus apply the output signal to a level detector that energizes an external device, such as a switch or an alarm, whenever an object interrupts the light source.

A timing resistor of fixed value ($R_T = 18k\Omega$) and a variable timing capacitor (C_T) determine the frequency of the NE5521 chip's internal oscillator. The oscillator output signal's frequency (which is also the modulating signal of the LED) can be calculated from the equation below.

$$f_{OSC} = \frac{(V_R - 1.3V)}{[V_R(R_T + 1.5k\Omega)C_T]}$$

When the scanning distance between the emitter and the receiver is increased, the sensitivity of the receiver decreases. There are, however, two ways of increasing the receiver sensitivity — reducing R_3, which has the effect of increasing the intensity of the pulsed beam, or increasing the gain of the uncommitted amplifier, or using a combination of the two. When the gain of the amplifier is increased, keep in mind that the output swing of the amplifier should not be large enough to saturate the amplifier.

IMPROVE AMBIENT LIGHT REJECTION BY PHASE DETECTION

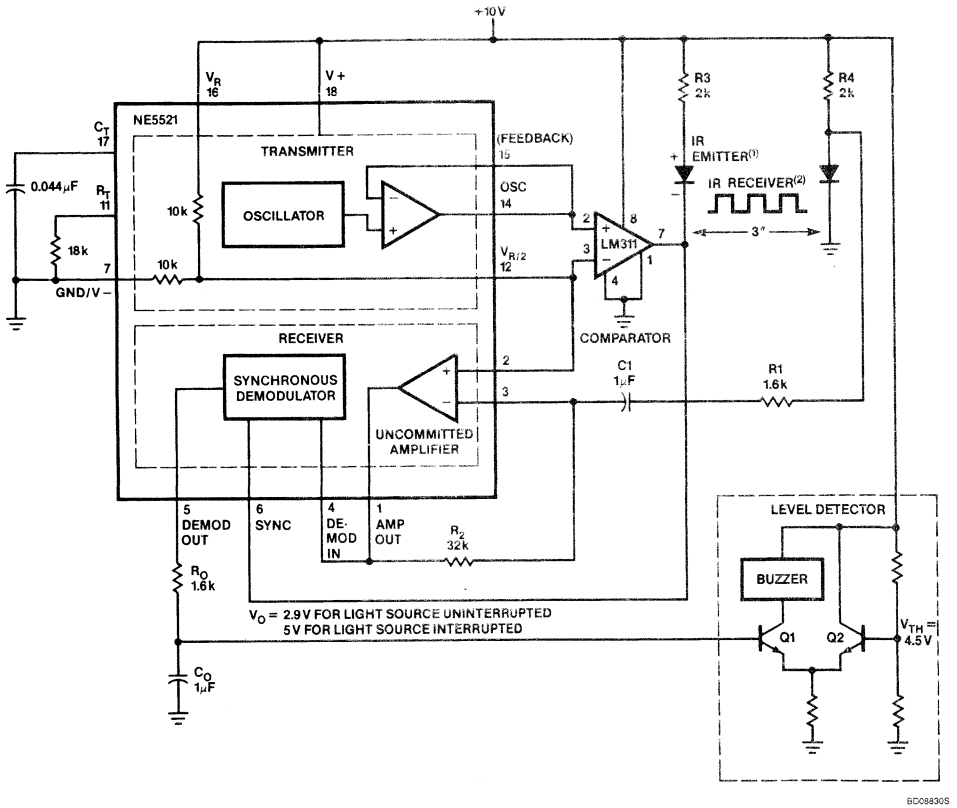
Nearly perfect rejection of ambient light can be achieved by tuning the receiver section of the NE5521 chip to look for the proper phase of the modulating signal (Figure 4). Here, the synchronous demodulator is operated as a phase detector. The sine wave signal from the oscillator (which is also the modulating signal of the LED) is the demodulator input signal. The amplified photoreceiver signal (referenced to 5.45V) is the sync input of the demodulator. When the light source is interrupted, the 5.45V at the sync input causes the demodulator's comparator to allow the AC signal at the demodulator's input to pass through to the output. The output filter puts out a 5V DC signal (zero-scale voltage).

When the light source is uninterrupted, however, the demodulator puts out a full-wave rectified signal of negative polarity (Figure 5). The DC signal at the output filter is the negative full-scale voltage ($-V_{FS}$) and is less than 5V. For any other modulation frequency (available from nearby IR sources such as welding arcs, strobe lamps, and mercury lamps), the output filter's voltage is close to

NE/SE5521 Simplifies Modulated Light Source Design

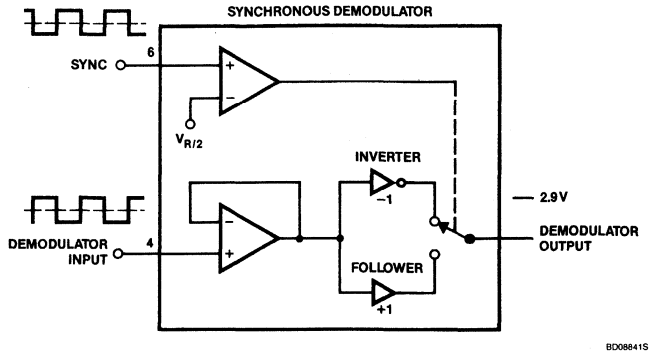
AN1181

$-V_{FS}$. False triggering of the receiver in the presence of undesirable modulation frequencies is thus eliminated since the demodulator puts out a 5V DC signal only when the light source is completely blocked. The level detector can be set up so that a relay or an alarm is energized only when the filter's output is at 5V. Keep in mind that the gain of the uncommitted amplifier should be large enough so that the pulsed signal at the sync input swings above and below the $V_{R/2}$ voltage so as to enable the demodulator's comparator to switch the demodulator input signal between the follower and the inverter.



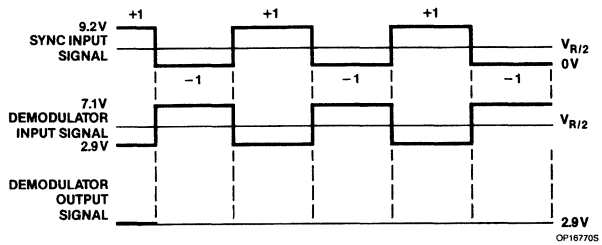
NOTES:
1. IR Emitter = FE-MTEI, microswitch.
2. IR Receiver = FE-MTRI, microswitch.

Figure 1. In a Typical Modulated Light Source Device, a High Degree of Ambient Light Rejection can be Achieved When the NE5521's Oscillator is Used to Frequency-Modulate an LED and the Demodulator is Used to Synchronously Rectify the Photoreceiver's AC Signal. DC Signal Produced by Ambient Light is Rejected by AC-Coupling NE5521's Uncommitted Amplifier



NOTE:
When the comparator's input is synchronized with the demodulator input signal, the circuit precisely rectifies the demodulator's input signal.

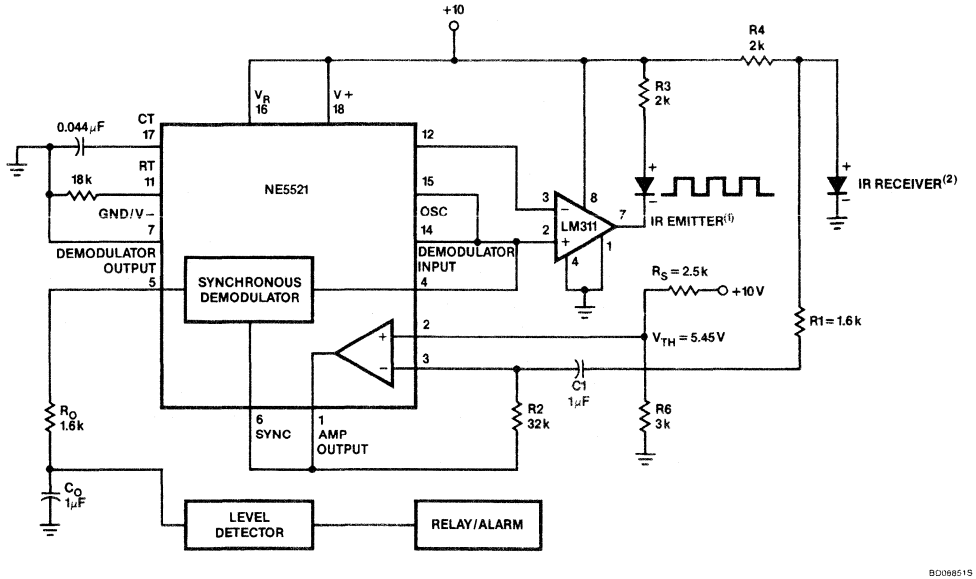
Figure 2. The NE5521's Demodulator Circuit Switches the Output Line Between an Inverter and a Follower



NOTE:
However, when the sync input signal is below $V_{R/2}$, the demodulator's input signal appears inverted at the output. By synchronously rectifying a square wave AC signal at the demodulator input, the circuit produces a DC signal at the demodulator output.

Figure 3. When the Demodulator's Sync Input Signal is Above $V_{R/2}$, the Demodulator's Output Follows the Demodulator's Input Signal

NE/SE5521 Simplifies Modulated Light Source Design AN1181



NOTES:
1. IR Emitter = FE-MTEI, microswitch.
2. IR Receiver = FE-MTRI, microswitch.

Figure 4. When the NE5521's Receiver is Tuned to Look for the Proper Phase of the Modulating Signal, Optimum Rejection of Undesirable Modulation Frequencies (Produced by High Intensity IR Light Sources Such as Welding Arcs, Strobe Lamps, and Mercury Lamps) Can be Achieved

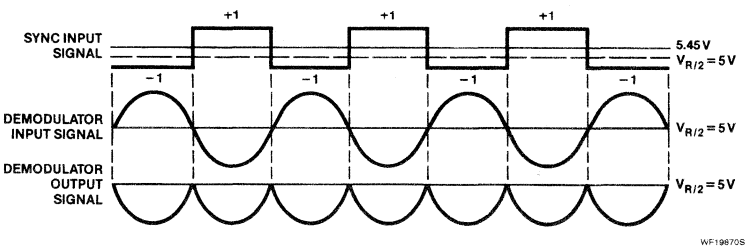


Figure 5. When a Sinusoidal Signal at the Demodulator Input That is 180° Out of Phase With the Sync Input Signal is Synchronously Rectified (as is the Case With the Circuit in Figure 4), the Circuit Puts Out a Full-Wave Rectified Signal of Negative Polarity. If the Phase Difference Between the Sync Input Signal and the Demodulator Input Signal Changes, the Demodulator Output Signal Also Changes Relative to the Phasing of the two Input Signals

AN1182
Using the NE5521 Signal Conditioner in Multi-Faceted Applications

Application Note

Position transducers call for a great deal of complex interface circuitry for input and output signal conditioning. The Signetics NE/SA/SE5521 packs all the interface circuitry on one chip and provides a complete monolithic solution to all the signal conditioning required for position transducers.

Position transducers are widely used in industrial and commercial applications for measuring very small displacement or rotation. In fact, such transducers can be used for any application where a given parameter can be converted to linear or angular motion. Weight, force, pressure, torque, and acceleration are often converted to linear displacement or linear rotation using position transducers. The displacement or rotation information is next conditioned to provide an accurate measurement of the parameter.

SE5521 can interface with all of the popular position transducers such as the LVDT, RVDT, and LPDT. In addition, by varying the arrangement of external components, you can also configure a phase detector, an AC bridge circuit, and an AC voltmeter. For a brief description of the IC, see the section entitled "A Look at the Signal Conditioning IC."

IC PROVIDES SINGLE-CHIP SOLUTION TO LVDT MEASUREMENTS

Figure 1a shows a typical single supply LVDT displacement measurement circuit. The uncommitted amplifier is configured as a second-order, low-pass Butterworth filter with gain. The gain of the amplifier is $1 + R_F/(R/2)$. The 1k offset adjust potentiometer is used to trim out the LVDT/signal conditioner system offset at null.

Exciting an LVDT at zero phase angle frequency results in minimum null voltage and optimum linearity (for a discussion, see "How an LVDT Works"). There are two ways of reducing null voltage — the first method is to adjust the oscillator frequency so that the secondary voltage is in phase with the primary excitation. The demodulator and oscillator voltage can be monitored on an oscilloscope for correct phasing as depicted in Figures 1b and 1c. A second method of phase compensation is to use a variable phase shift network between the oscillator output and the sync input to the device. An optional phase shift network in Figure 1a consists of a 20k phase adjust potentiometer in series with capacitor C_3. The potentiometer is adjusted for correct demodulator phasing as illustrated in Figures 1b and 1c. With $R_O = 10k$, $C_O = 2nF$, and at oscillator frequency, $f_{OSC} = 2900Hz$, the phase shift is $\varphi = -\tan^{-1}(\omega R_O C_O) = -20°$.

The LVDT output is referenced to $V_{R/2}$ by tying one end of the secondary to Pin 12 of the device. A capacitor between Pin 12 and ground provides an AC ground for $V_{R/2}$. Since the output of Pin 12 is a source of high impedance, Pin 12 may need to be buffered in some applications so as to prevent loading effects on the voltage divider. The common mode voltage and the RMS value of the oscillator signals are determined by V_R; consequently, V_R should be a fixed reference voltage. By making V+ greater than V_R, the output swing of the auxiliary amplifier is increased and the filter can accommodate higher closed-loop gain.

The demodulator output has positive polarity when the LVDT output signal is 180° out of phase with the primary excitation (see Figure 1d), and has negative polarity when the LVDT output is in phase with the primary excitation (see Figure 1e). The polarity of the demodulator signal indicates on which side of null the core is while the amplitude indicates the relative displacement of the core from the null position.

Filtered DC output appears at Pin 1 of the device. Measurements with 10-bit accuracy at −55°C to +125°C temperature range are easily achieved by the circuit in Figure 1.

PHASE DETECTOR MEASURES PHASE DIFFERENCE WITH 10-BIT ACCURACY

The synchronous demodulator easily lends itself to phase detection as illustrated in Figure 2a. If signals of identical frequency are applied to sync input (Pin 6) and to the demodulator input (Pin 4), respectively, the demodulator functions as a phase detector with output DC component being proportional to phase difference between the two inputs. The signals must be referenced to 0V for dual supply operation or to $V_{R/2}$ for single supply operation. At ±5V supplies, the demodulator can easily handle 7V peak-to-peak signals.

The low-pass network configured with the uncommitted amplifier provides DC output at Pin 1 of the device. The DC output is maximum (+ full-scale) when V_1 and V_2 are 180° out of phase (see Figure 1d) and minimum (− full-scale) when the signals are in phase (see Figure 1e). At quadrature ($\varphi = 90°$), the DC output is 0V as shown in Figure 2b. By calibrating the −FS, 0, and +FS points, any unknown phase difference may be determined by just measuring the DC output at Pin 1. A linear relationship between the DC output and phase difference is shown by the transfer curve in Figure 2c.

Even though the oscillator signals are not utilized in this particular application, the use of C_T and R_T is still recommended in order to prevent saturation of active devices in the IC.

SIGNAL CONDITIONER EASES LPDT MEASUREMENTS

Figure 3 shows a simple dual supply setup for LPDT measurements. Op amp IC_1 is configured as a low-pass filter with cut-off frequency equal to the oscillator frequency of 2900Hz. The filter attenuates the higher order spectral components of the oscillator signal and produces a low-distortion sine wave at the output. This sine wave excites one primary, while the other primary is excited by a cosine wave produced by amp IC_2. Amp IC_2 is configured as a constant amplitude lag circuit that preserves the amplitude of the sine wave input from IC_1, but phase shifts the signal by 90° at the output. The phase shift, φ, is given by $\varphi = -2\tan^{-1}(2\pi f_{OSC} R_5 C_3)$. Thus, at 90° phase shift, $f_{OSC} = 1/(2\pi R_5 C_3)$. R_5 is a 10k potentiometer with its center wiper tied to one end. The potentiometer is tweaked and the wave forms from IC_1 and IC_2 are observed on an ocilloscope for 90° phase difference and 0V at the output of the device (Pin 1). The system is now ready to make phase measurements as discussed earlier.

For dual supply operation, both the positive and negative supplies should be closely regulated since the oscillator common mode voltage varies with the supplies.

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

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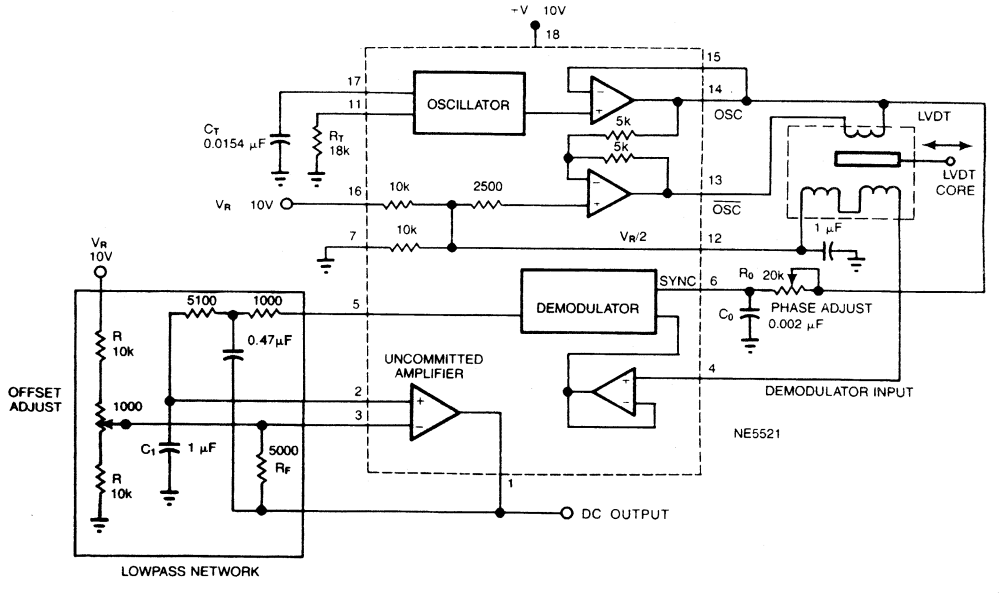
AC BRIDGE CALIBRATES RESISTORS AND CAPACITORS WITH 10-BIT ACCURACY

An AC bridge, shown in Figure 4, provides a simple and cost-effective solution to matching resistors and capacitors on production lines. Impedances Z_R and Z_X form a half-bridge, while OSC and $\overline{OSC}$ excite the bridge differentially. The external op amp is a JFET input amplifier (LF356) with very low input bias current on the order of 30pA (typical). C_1 allows AC coupling by blocking the DC common mode voltage from the bridge, while R_1 biases the output of LF356 to 0V at DC. Use of FET input op amp insures that DC offset due to bias current through R_1 is negligible. AC output of the demodulator is filtered via the uncommitted amp to provide DC voltage for the meter. The 10k potentiometer, R_5, limits the current into the meter to a safe level. Calibration begins by placing equal impedances at Z_R and Z_X, and the system offset is nulled by the offset adjust circuit so that Pin 1 is at 0V. Next, known values are placed at Z_X and the meter deviations are calibrated. The bridge is now ready to measure an unknown impedance at Z_X with ±0.05% accuracy or better.

RMS-TO-DC CONVERTER YIELDS 10-BIT ACCURACY

An AC voltmeter may be easily constructed as in Figure 5; the simplicity of the circuit and low component count make it particularly attractive. The demodulator output is a full-wave rectified signal from the AC input at Pin 4. DC component of the rectified signal at Pin 5 varies linearly with the RMS input at Pin 4 and thus provides an accurate RMS-to-DC conversion at the output of the filter (Pin 1). C_T is a variable capacitor that is tweaked until the oscillator signal to the sync input of the demodulator is in phase with the AC signal at Pin 4.

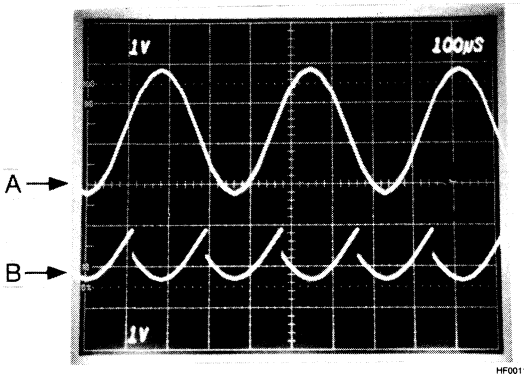
In many applications it may not be desirable to adjust C_T each time the AC signal frequency changes. An alternate approach is to use a zero-crossing detector to excite the sync input of the device. The LM311 comparator in Figure 6 produces a square wave (trace A in Figure 6b) in phase with the AC signal (trace B). Optimum rectification thus occurs at the demodulator output (trace C). For precision measurements at high frequencies, a fast, low offset comparator is recommended.



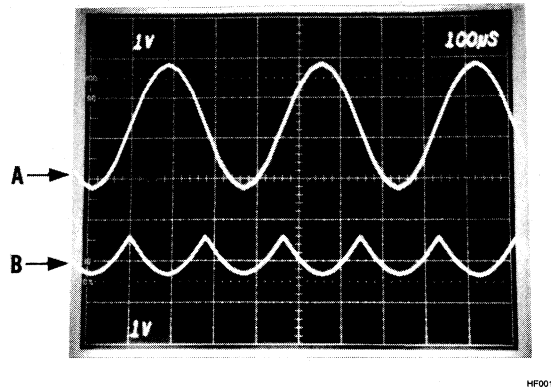
NOTE:
V_R is a fixed reference voltage. OSC frequency, $f_{OSC} = 2.9kHz$. Phase shift, $\phi = -\tan^{-1}(\omega R_O C_O)$.

a. Typical Single Supply LVDT Measuring Circuit

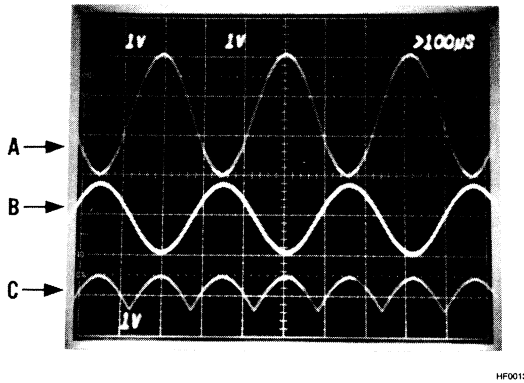
Figure 1



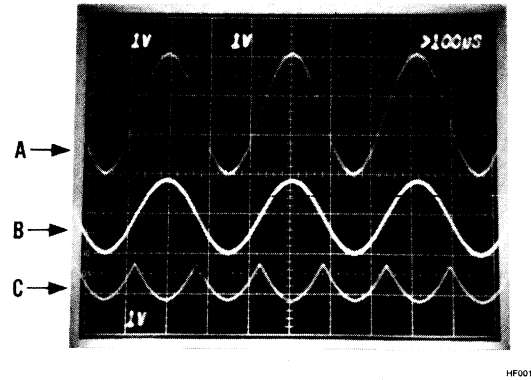
b. Trace A is the Oscillator Signal and Trace B is the Demodulator Output Resulting from LVDT Phase Shift



c. Trace B is the Demodulator Output After Proper Phase Adjustment

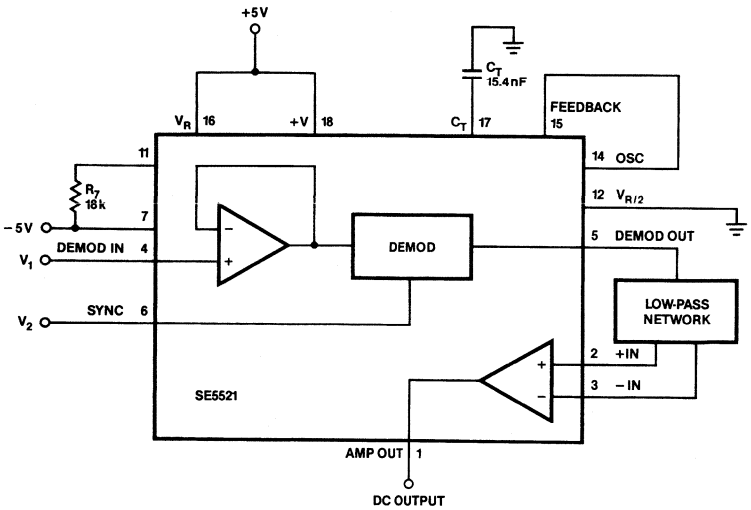


d. With LVDT Output (Trace B) at 180° Out of Phase With Excitation Signal (Trace A), the Demodulator Output has Positive Polarity (Trace C)

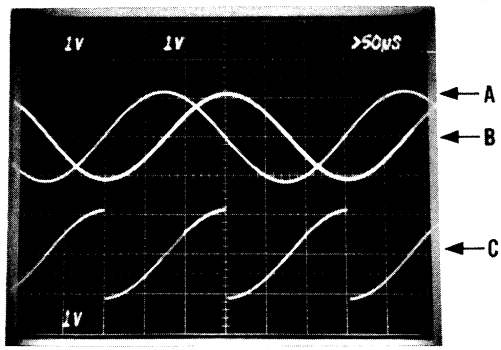


e. Demodulator Output has Negative Polarity (Trace C) When LVDT Output (Trace B) is in Phase With Primary Signal (Trace A)

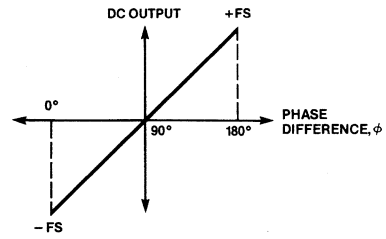
Figure 1 (Continued)



a. Phase Detector Measures Phase Difference Between Signals V_1 and V_2 and Provides DC Output at Pin 1



b. When V_1 and V_2 in (a) are at Quadrature (Traces A and B), the DC Component of Demodulator Output (Trace C) is at 0V



c. The DC Output and Phase Vary Linearly

Figure 2

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

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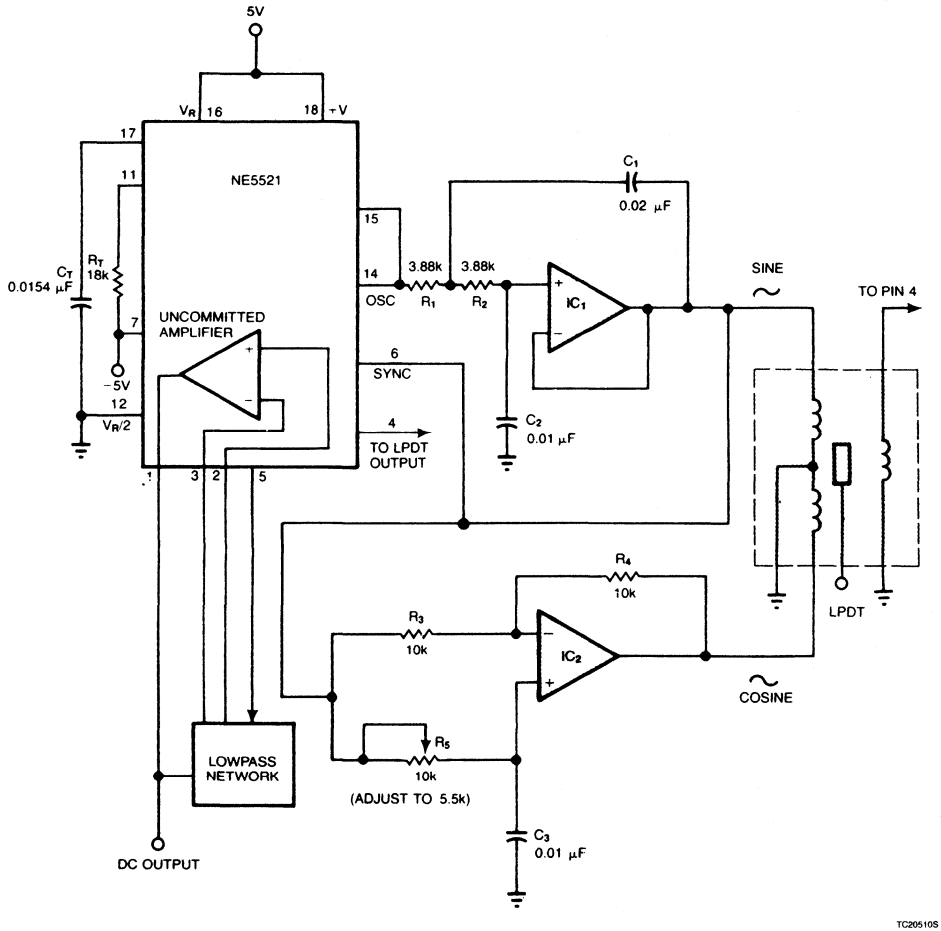


Figure 3. LPDT Interface

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

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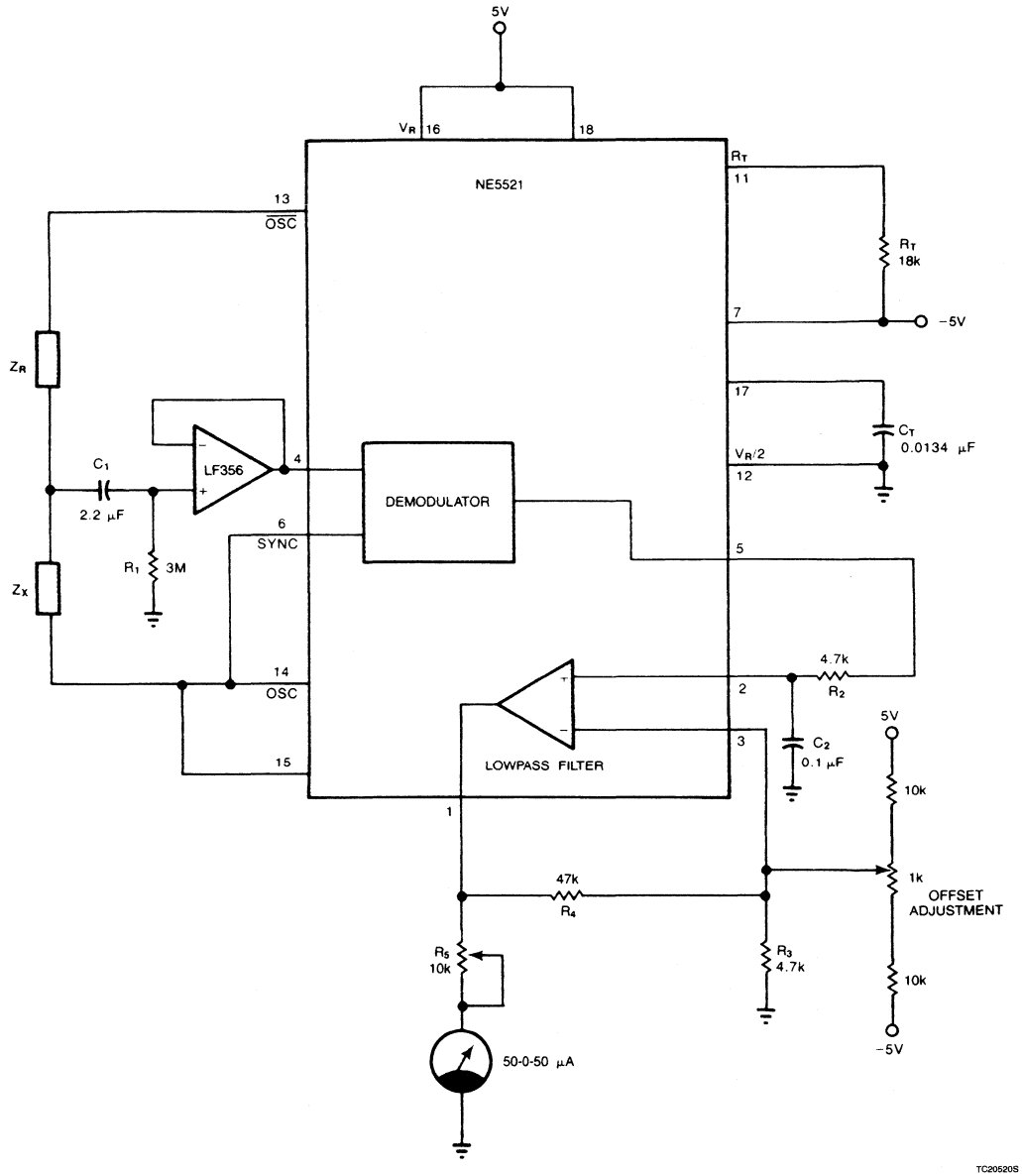
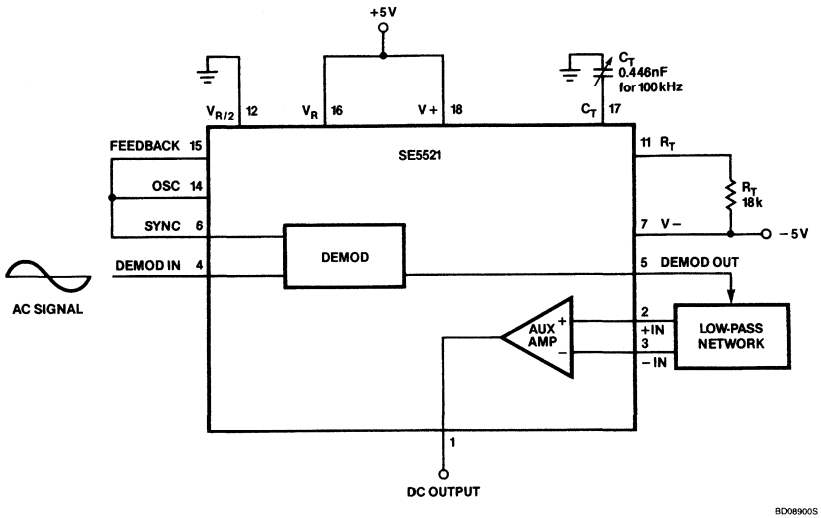


Figure 4. Signal Conditioner Used as an AC Bridge to Calibrate Resistors/Capacitors

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

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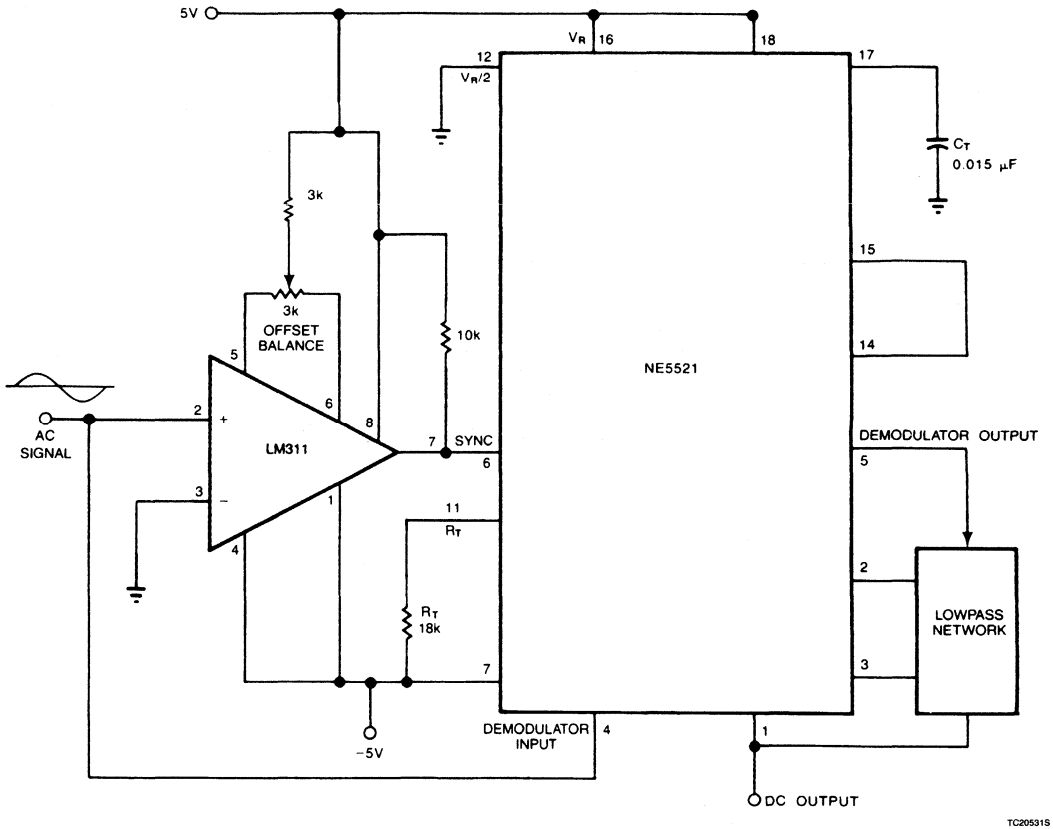


NOTE:
1. The DC output at Pin 1 varies linearly with the RMS input at Pin 4.
2. C_T is tweaked until the sync signal is in phase with the AC signal.

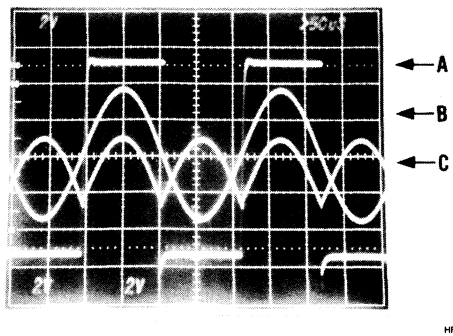
Figure 5. AC Voltmeter

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

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a. AC Voltmeter. Comparator CI (LM311), Used as a Zero-Crossing Detector, Produces a Constant Amplitude Square Wave to Excite the Sync Input of the Demodulator. DC Output Appears at Pin 1



b. Trace B is the AC Signal at the Comparator and Demodulator Input. The Output of the Zero-Crossing Detector (Trace A) at Sync Input Causes Synchronous Rectification at the Demodulator Output (Trace C). Auxiliary Amplifier Filter Produces DC Output at Pin 1

Figure 6

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

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APPENDIX I

A LOOK AT THE SIGNAL CONDITIONING IC

The signal conditioner essentially consists of three major blocks: an oscillator with programmable frequency, a synchronous demodulator, and an auxiliary amplifier (see Figure I).

The oscillator generates a stable amplitude sine wave with an RMS value determined by a fixed reference voltage, V_R, at Pin 16 of the device, and referenced to $V_{R/2}$. Next, the oscillator signal is buffered by two high-gain, low-offset op amps to produce the buffered oscillator signal, OSC, and the inverted signal, $\overline{OSC}$. The OSC and $\overline{OSC}$ signals exhibit less than 50ppm/°C amplitude drift (at −55°C to +125°C temperature range) with total harmonic distortion under 2%. OSC and $\overline{OSC}$ signals are used to differentially excite the primary of the LVDT/RVDT. A fixed 18k resistor, R_T (external to chip), and an external timing capacitor, C_T, determine the frequency of the oscillator. The oscillator frequency is given by the following: $f_{OSC} = (V_R - 1.3V)/[V_R(R_T + 1.5k\Omega)\ C_T]$.

The signal conditioner employs a synchronous demodulatorulation technique to extract position and phase information of the transducer core. The synchronous demodulator block not only conditions the transducer output to provide usable information, but also provides a very high impedance load to the transducer output (on the order of several MΩ for maximum linearity and for relative insensitivity to frequency drift (see "How an LVDT Works", Figure iii). Figure II shows how the demodulator functions. The oscillator signal, which is also the primary drive for the transducer, is tied to the sync input of the demodulator. Note that the OSC signal and the transducer output (demodulator input) are both referenced to $V_{R/2}$. The sync signal is compared to an internally-generated reference voltage, $V_{R/2}$. During the first half-cycle, as the sync signal goes above $V_{R/2}$, the demodulator functions as an inverter and, thus, the demodulator input appears inverted at the output. However, during the second half-cycle, as the sync signal goes below $V_{R/2}$, the demodulator functions as a follower and, thus, the demodulator input appears at the output with unity gain. Full-wave rectification thus occurs in synchronism with the primary drive signal. The amplitude of the rectified signal tells the position of the core, while the polarity of the output indicates on which side of null the core is. The demodulator offset is measured at less than 2mV with 5μV/°C offset drift, and linearity error is measured at ±0.05% full-scale (at −55°C to +125°C temperature range). A low offset is essential for transducer systems in precision applications since a high offset will not only mask the transducer null, but will also make position measurements inaccurate as the ambient temperature varies.

Since all readout devices (meters, recorders, etc.) are DC input devices, the AC output of the demodulator has to be converted to filtered DC before being applied to the readouts. Consequently, an on-chip amplifier may be used as an active filter with programmable gain for the demodulator output. The filter removes the carrier frequency and other higher-order harmonics from the demodulator output and produces a ripple-free DC output. The amplifier exhibits an open-loop gain of 380V/mV (typical) and 0.5mV input offset (typical). DC offsets from the transducer/signal conditioner system can be nulled by offset adjustment at the auxiliary amplifier. The device operates from 4.5V to 22V with single supply, or ±2.25V to ±11V with dual supplies.

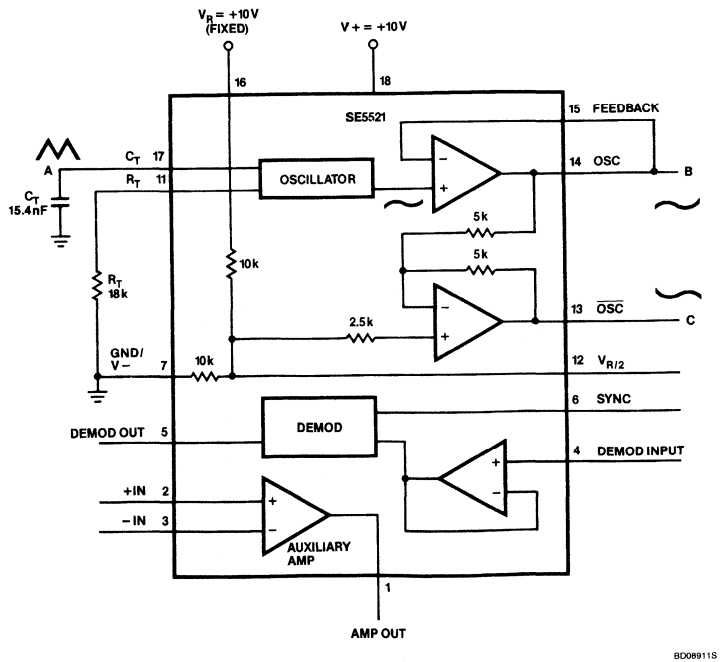


Figure I. SE5521 Block Diagram

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

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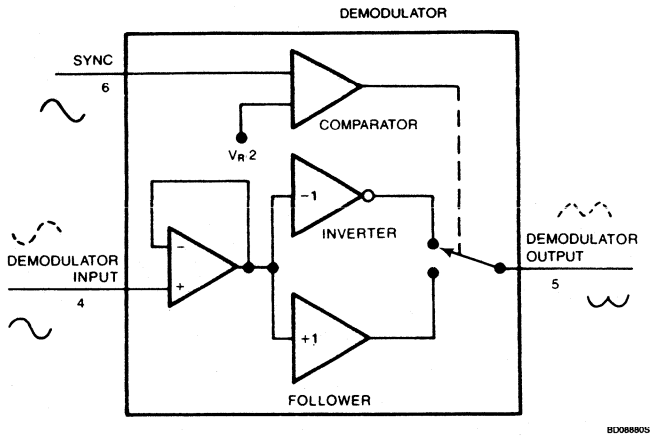


Figure II. Synchronous Demodulator Full-Wave Rectifies the Demodulator Input Signal in Synchronization With the Sync Signal at Pin 6

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

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APPENDIX II

HOW AN LVDT WORKS

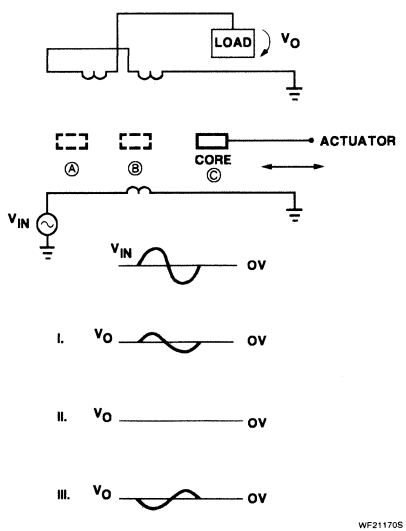
Linear Variable Differential Transformers (LVDTs) are position transducers that have long been used to measure very small displacement and any parameter that can be converted to linear motion. LVDTs are mutual inductance devices consisting of a primary winding and a pair of secondary windings that are wound on an insulated bobbin, and a non-contacting magnetic core capable of free motion inside the transformer. The secondaries are tied together externally in a series-opposing configuration.

With AC excitation at the primary, the core controls the coupling between the primary and the secondaries and produces a differential voltage across the secondaries. The magnitude of the voltage across the secondaries varies linearly with core displacement and contains both the position and phase information (direction of motion) of the core with respect to the center of the secondaries (null position).

With the core at null, the voltage induced at each secondary is equal and of opposite phase; thus cancellation occurs, resulting in a zero AC output. As the core traverses away from the null position, a sinusoidal voltage is developed across the secondaries, the amplitude of which contains the position information. Once the core moves through null, a 180° phase reversal occurs in the output signal with respect to the primary signal. Direction of the core (phase information) with respect to the null position is thus indicated as illustrated in Figure i.

In order to obtain any useful information, some form of signal conditioning is required. Figure ii shows the DC output of the LVDT as a linear function of the core position after proper signal conditioning. The output voltage of the LVDT is directly proportional to the excitation voltage; therefore, it is essential that the excitation signals have a constant amplitude over the operating temperature range. Output voltage also varies with the excitation frequency. However, the change is not directly proportional to frequency, as shown in Figure iii. Most LVDTs show a small amount of phase shift between the excitation signal at the primary and the output signal at the secondaries. The phase shift introduces a DC offset at null and thus tends to mask the LVDT null. The LVDT null voltage may be reduced by exciting the primary at a frequency where both the primary signal and the output signal are in phase — this is the zero phase angle frequency. Exciting the LVDT at its zero-phase angle frequency optimizes linearity and repeatability of the measurements, while a high impedance load at the LVDT output eliminates the need for frequency regulation, as can be observed from Figures iiia and iiib.

Another popular position transducer is the Rotary Variable Differential Transformer (RVDT). The RVDT operation is analogous to the LVDT, except that the core motion is rotary.



NOTES:
1. With core at a, output is in phase with input. Output amplitude decreases as core moves from A to B.
2. AC output is zero when core is at B (null).
3. Output amplitude increases as core moves from B to C. With core at C, output is 180° out of phase with respect to input.

Figure i. The LVDT Output Signal Changes Relative to Core Position

Using the NE5521 Signal Conditioner in Multi-Faceted Applications

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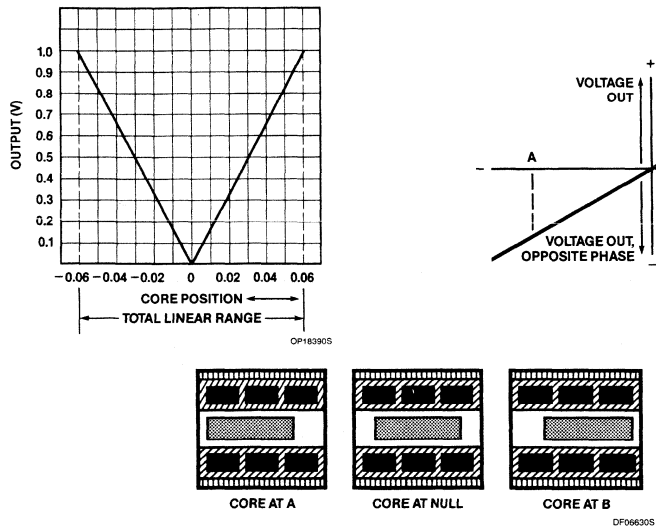
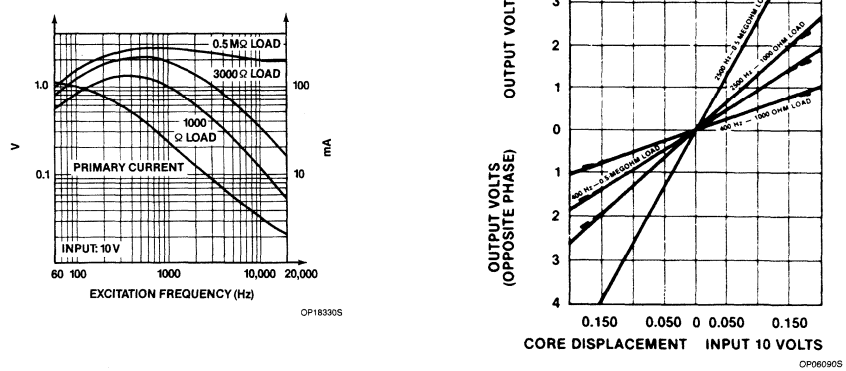


Figure ii. Absolute Magnitude of Output Voltage (Left) and Phase-Referenced Output Voltage (Right) as a Function of LVDT Core Position (Courtesy Schaevitz Engineering)



a. Nominal Full-Scale Output at Various Loads and Primary Current vs Excitation Frequency for a Typical LVDT

b. Output Characteristics of a Typical LVDT for Various Loads and Excitation Frequencies (Courtesy Schaevitz Engineering)

Figure iii

APPENDIX III

LPDT CHANGES PHASE INSTEAD OF AMPLITUDE

A recently developed linear position transducer, the LPDT (Linear Phase Differential Transformer), produces a phase output linear with the core motion. The transducer construction is similar to the LVDT, the main exception being that there are six primary coils which are wound on a bobbin at a slant. The excitation to the transducer primaries consists of a sine wave and a cosine wave of equal magnitude. The output at the secondary is an AC signal of constant amplitude, which is the vector sum of the sine and cosine excitation signals, with a phase angle that varies linearly with core position. Figure A shows how the transducer is energized.

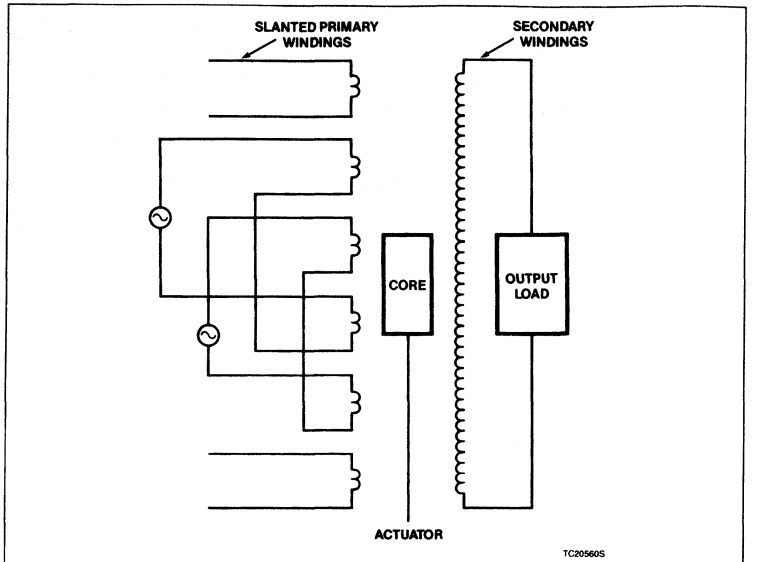


Figure A. LPDT with AC Excitation Signals at the Input

REFERENCES

1. *Handbook of Measurement and Control*, Revised Edition 1976, by Edward Herceg, Schaevitz Engineering Publication, Pennsauken, New Jersey.
2. *Signetics Linear LSI Data and Applications Manual*, 1985 Edition, pg 4-212, 9-41. Signetics Corporation, Sunnyvale, CA, 94086.
3. Frank Yeaple, "Linear Position Transducer Changes Phase Instead Of Amplitude", *Design News*, November 5, 1984, pg 180.

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Peripheral drivers

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NE590/591
Addressable Peripheral Drivers

Product Specification

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has eight Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line. A common clear input, $\overline{CLR}$, turns all outputs off when a logic low is applied.

The NE590 has eight open-collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin plastic or Cerdip package.

The NE591 has eight open-emitter Darlington outputs which source current to an external load from a common collector line, V_S. This V_S line need not necessarily be the same as the 5V V_{CC} supply. The device is packaged in an 18-pin plastic or Cerdip package.

FEATURES

- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **NE590 will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **NE590 is pin compatible with 54/74LS259**

APPLICATIONS

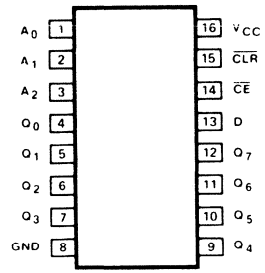
- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE590F
16-Pin Plastic	0 to +70°C	NE590N
18-Pin Cerdip	0 to +70°C	NE591F
18-Pin Plastic	0 to +70°C	NE591N

PIN CONFIGURATIONS

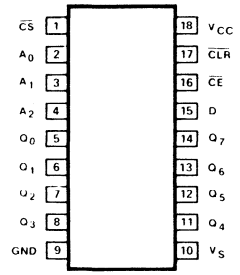
F, N Packages



TOP VIEW

NE590 CD10541S

F, N Packages



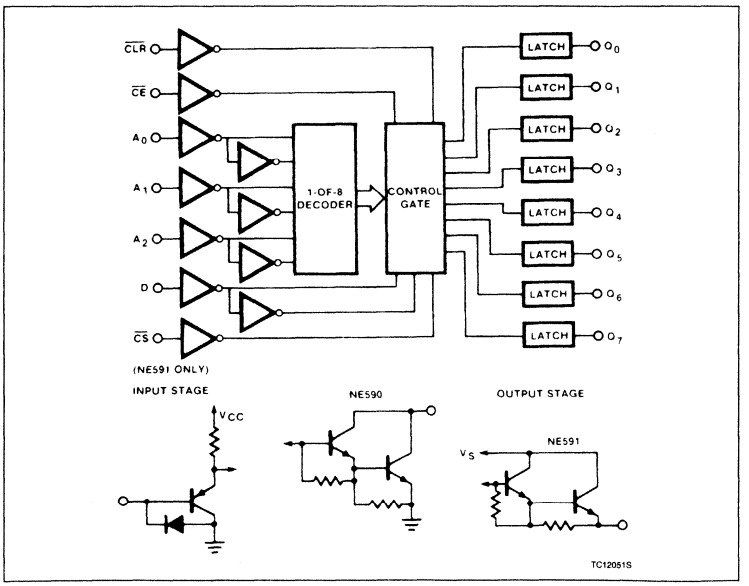
TOP VIEW

NE591 CD10551S

PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1 – 3	2 – 4	$A_0 - A_2$	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4 – 7, 9 – 12	5 – 8, 11 – 14	$Q_0 - Q_7$	The 8 device outputs. The NE590 has open-collector Darlington outputs. The NE591 has open emitter-follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF" Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output.
14	16	$\overline{CE}$	The chip enable. When this input is low, the output latches will accept data. When $\overline{CE}$ goes high, all outputs will retain their existing state regardless of address or data input conditions.
15	17	$\overline{CLR}$	The clear input. When $\overline{CLR}$ goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, $\overline{CLR}$ low will override any other condition.
–	1	$\overline{CS}$	The chip select input provides for an additional level of address decoding.
–	10	V_S	The V_S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V_{CC} or another supply.

BLOCK DIAGRAM



TRUTH TABLE (NE590)

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							Addressable Latch
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

NOTES:
X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"ON" output state
H = High voltage level/"OFF" output state

TRUTH TABLE (NE591)

INPUTS							OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	$\overline{CS}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	X	X	X	X	X	X	L	L	L	L	L	L	L	L	Clear
H	H	H	X	X	X	X	Q_{N-1} →								Memory
H	H	L	X	X	X	X	Q_{N-1} →								
H	L	H	X	X	X	X	Q_{N-1} →								
H	L	L	L	L	L	L	L	Q_{N-1} →							Addressable Latch
H	L	L	H	L	L	L	H	Q_{N-1} →							
H	L	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	L	L	H	H	H	Q_{N-1} →							L	
H	L	L	H	H	H	H	Q_{N-1} →							H	

NOTES:
X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"OFF" output state
H = High voltage level/"ON" output state

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage	−0.5 to +15	V
V_{OUT}	Output voltage NE590 NE591	 0 to +7 0 to V_{CC}	V
V_S	Source bus voltage NE591 only	−0.5 to +7	V
$V_S - V_{CC}$	Source/supply differential voltage NE591 only	−5 to +2	V
I_{OUT}	Output current Each output All outputs	 300 1000	mA
P_D	Maximum power dissipation $T_A = 25°C$ (still air) NE590[1] F package N package NE591[2] F package N package	 1190 1450 1500 1690	mW
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature	165	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec max)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   F package at 9.5mW/°C.
   N package at 11.6mW/°C.
2. Derate above 25°C at the following rates:
   F package at 12mW/°C.
   N package at 13.5mW/°C.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 to 5.25V, 0°C ≥ T_A ≤ 70°C, unless otherwise specified. [1,2]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					
V_{IH}	High		2.0			V
V_{IL}	Low				0.8	
	Output voltage					
V_{OL}	Low (NE590 only)	I_{OL} = 250mA, T_A = 25°C		1.0	1.3	
		Over temperature			1.5	V
V_{OH}	High (NE591 only)	I_{OH} = −250mA, V_{CC} = V_S = 5V	2.9			
	Input current					
I_{IH}	High	V_{IN} = V_{CC}		0.1	10	
I_{IL}	Low	V_{IN} = 0V				
	$\overline{CE}$ input			−25	−60	μA
	All other inputs			−15	−50	
I_{OH}	Leakage current	V_{OUT} = 5.25V		10	250	μA
	Supply current[3]	V_S = V_{CC} = 5V				
I_{CCL}	All outputs low					
	NE590			33	50	
	NE591			15	50	
I_{CCH}	All outputs high					mA
	NE590			15	50	
	NE591			30	50	
P_D	Power dissipation	No output load			350	mW

NOTES:
1. All typical values are at V_{CC} = 5V and T_A = 25°C.
2. For the NE591 V_S = V_{CC} in all tests.
3. Supply current for the NE591 is measured with no output load.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C.

SYMBOL	PARAMETER	TO	FROM	NE590			NE591			UNIT
				Min	Typ	Max	Min	Typ	Max	
	Propagation delay time									
t_{PLH}	Low-to-High[1]	Output	$\overline{CE}$		65	150		50	80	ns
t_{PHL}	High-to-Low[1]				115	230		70	120	
t_{PLH}	Low-to-High[2]	Output	Data		65	130		45	70	ns
t_{PHL}	High-to-Low[2]				120	240		65	100	
t_{PLH}	Low-to-High[3]	Output	Address		100	200		45	80	ns
t_{PHL}	High-to-Low[3]				130	260		75	140	
t_{PLH}	Low-to-High[4]	Output	$\overline{CLR}$		65	130				ns
t_{PHL}	High-to-Low[4]							45	140	
t_{PLH}	Low-to-High[1]	Output	$\overline{CS}$					40	80	ns
t_{PHL}	High-to-Low[1]							70	120	
Switching setup requirements										
$t_{S(H)}$[5]		Chip enable	High data	210			100			ns
$t_{S(L)}$[5]		Chip enable	Low data	210			100			ns
$t_{S(A)}$[6]		Chip enable	Address	30			30			ns
$t_{H(H)}$[5]		Chip enable	High data	40			10			ns
$t_{H(L)}$[5]		Chip enable	Low data	30			10			ns
$t_{S(CS)}$[5]		Chip enable	Low chip select				100			ns
$t_{PW(E)}$	Chip enable pulse width[1]			120			120			ns

NOTES:
1. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
4. See Turn-Off Delay, Clear to Output timing diagram.
5. See Setup and Hold Time, Data to Enable timing diagram.
6. See Setup Time, Address to Enable timing diagram.

FUNCTIONAL DESCRIPTION

These peripheral drivers have latched outputs which hold the input data until cleared. The NE590 has active-Low, open-collector outputs, while the NE591 has active-High, uncommitted (open) emitter outputs. All outputs are cleared when power is first applied.

Addressable Latch Function

Any given output can be turned on or off by presenting the address of the output to be set or cleared to the three address pins, by holding the "D" input High to turn on the selected input, or by holding it Low to turn off, holding the $\overline{CLR}$ input High, and bringing the $\overline{CE}$ input Low. Once an output is turned on or off, it will remain so until addressed again, or until all outputs are cleared by bringing the $\overline{CLR}$, $\overline{CE}$, and "D" inputs Low. For NE591, $\overline{CS}$ must be brought Low any time CE is Low if any outputs are to be changed.

Demultiplexer Operation

By bringing the $\overline{CLR}$ and $\overline{CE}$ inputs Low and the "D" input High, the addressed output will remain on and all other outputs will be off. This condition will remain only as long as the output is addressed. For the NE591, the $\overline{CS}$ input must also be Low.

High Current Outputs

The obvious advantage of these devices over the 9334 and N74LS259 (which provide a similar function) is the fact that the NE590 and NE591 are capable of output currents of 250mA at each of their eight outputs. It should be noted, however, that the load power dissipation would be over 2.5W if all 8 outputs were to carry their full rated load current at one time. Since the total power dissipation is limited by the package to 1W, and since the power dissipation due to supply current is 0.25W, the total load power dissipation by the device is limited to 0.75W, and decreases as ambient temperature rises.

The maximum die junction temperature must be limited to 165°C, and the temperature rise above ambient and the junction temperature are defined as:

$$t_R = \theta_{JA} \times P$$
$$t_J = t_A + t_R$$

where

θ_{JA} is die junction to ambient thermal resistance
P_D is total power dissipation
t_R is junction temperature rise above ambient
t_J is die junction temperature
t_A is ambient (surrounding medium) temperature

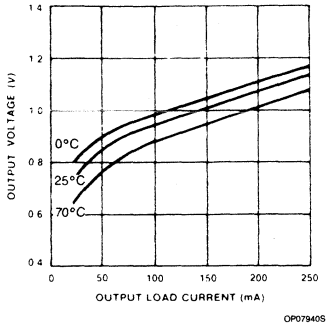
For example, if we are using the NE5090 in a plastic package in an application where the ambient temperature is never expected to rise above 50°C, and the output current at the 8 outputs, when on, are 100, 40, 50, 200, 15, 30, 80, and 10mA, we find from the graph of output voltage vs load current that the output voltages are expected to be about 0.92, 0.75, 0.78, 1.04, 0.5, 0.7, 0.9, and 0.4V, respectively. Total device power due to these loads is found to be 473.5mW. Adding the 250mW due to the power supply brings total device power dissipation to 723.5mW. The thermal resistances are 83°C per W for plastic packages and 100°C per W for Cerdips. Using the equations above we find:

Plastic $t_R = 83 \times 0.7235 = 60°C$
Plastic $t_J = 50 + 60 = 100°C$
Cerdip $t_R = 100 \times 0.7235 = 72.4°C$
Cerdip $t_J = 50 + 72.4 = 122.4°C$

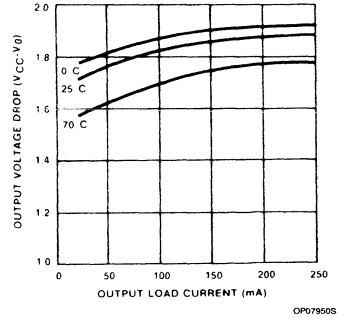
Thus we find that t_J for either package is below the 165°C maximum and either package could be used in this application. The graphs of total load power vs ambient tem-

perature would also give us this same information, although interpreting the graphs would not yield the same accuracy.

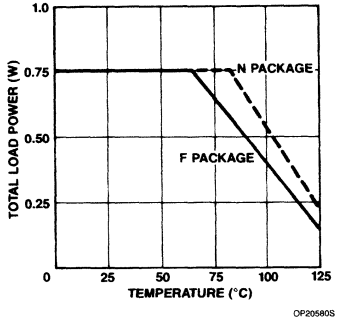
TYPICAL PERFORMANCE CHARACTERISTICS



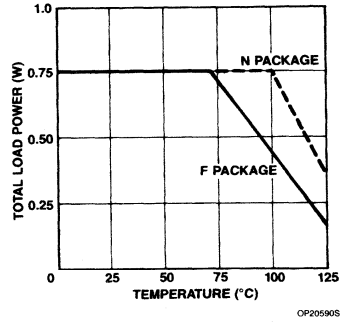
Output Voltage vs Load Current (NE590)



Output Voltage Drop vs Load Current (NE591)

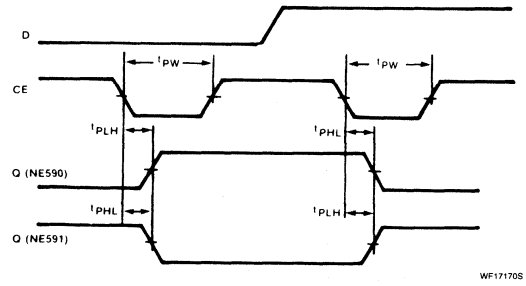


Total Load Power vs Temperature (NE590)



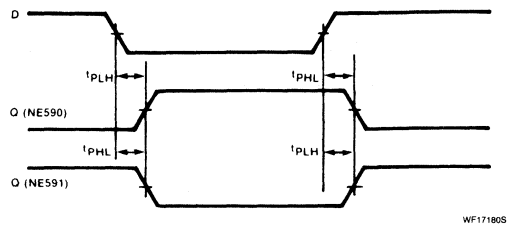
Total Load Power vs Temperature (NE591)

TIMING DIAGRAMS



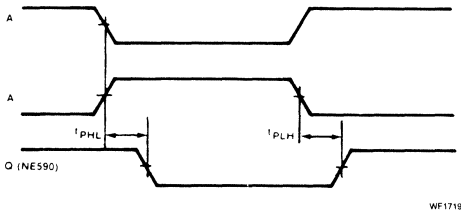
NOTE:
Other Inputs $\overline{CLR}$ = H. A = Stable. $\overline{CS}$ = L.

Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width



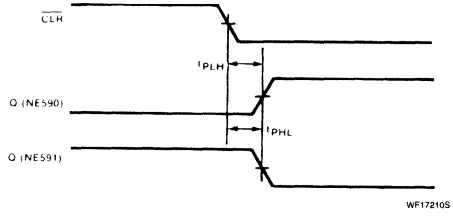
NOTE:
Other Inputs $\overline{CE}$ $\overline{CS}$ = L. $\overline{CLR}$ = H. A = Stable.

Turn-On and Turn-Off Delays, Data-to-Output



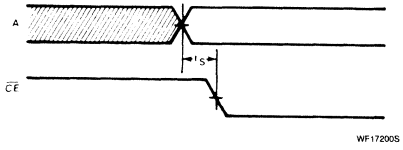
NOTE:
Other Inputs: $\overline{CE}$ = L. $\overline{CLR}$ = L. D = H.

Turn-On and Turn-Off Delays, Address to Output



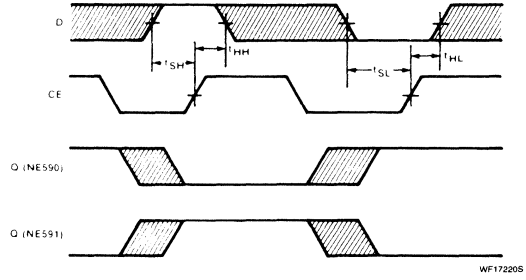
NOTE:
Other Inpputs: $\overline{CE}$ = H. $\overline{CS}$ = H.

Turn-Off Delay, Clear to Output



NOTE:
Other Inputs: $\overline{CLR}$=H. $\overline{CS}$=L.

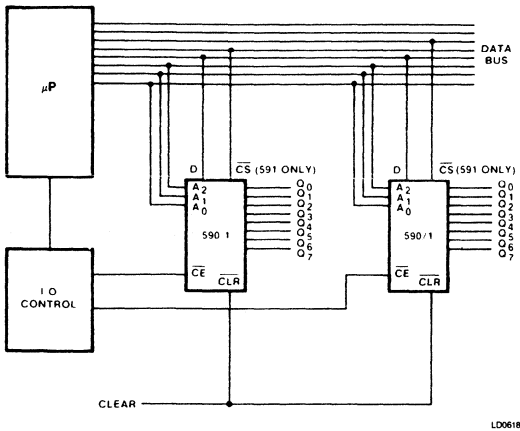
Setup Time, Address to Enable



NOTE:
Other Inputs: $\overline{CLR}$=H. A=Stable. $\overline{CS}$=L.

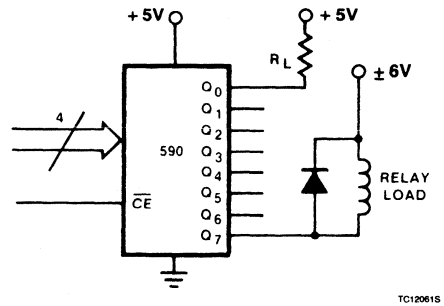
Setup and Hold Time, Data to Enable

TYPICAL APPLICATIONS

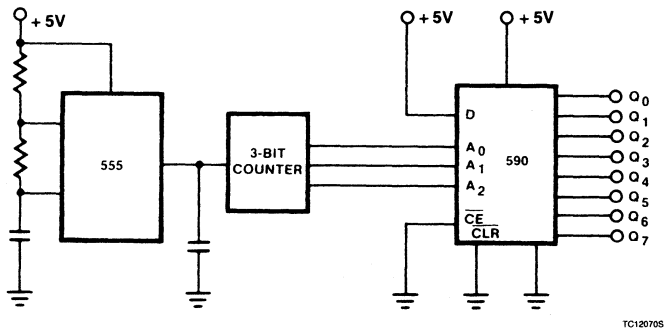


NOTE:
A_0, A_1, A_2, and $\overline{CS}$ may be connected to the address bus if permitted by system design.

Interfacing the 590/591 with a Microprocessor System



NE590 Driving Simple Loads



NE590 Operating in Demultiplex Mode

NE/SA5090
Addressable Relay Driver

Product Specification

DESCRIPTION

The NE/SA5090 addressable relay driver is a high-current latched driver, similar in function to the 9934 address decoder. The device has 8 open-collector Darlington power outputs, each capable of 150mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic "0" is applied. The device is packaged in a 16-pin plastic or Cerdip package.

FEATURES

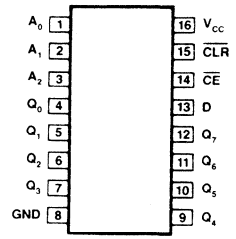
- **8 high-current outputs**
- **Low-loading bus-compatible inputs**
- **Power-on clear ensures safe operation**
- **Will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **Pin-compatible with 9334 (Siliconix or Fairchild)**

APPLICATIONS

- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATION

D[1], F, N Packages

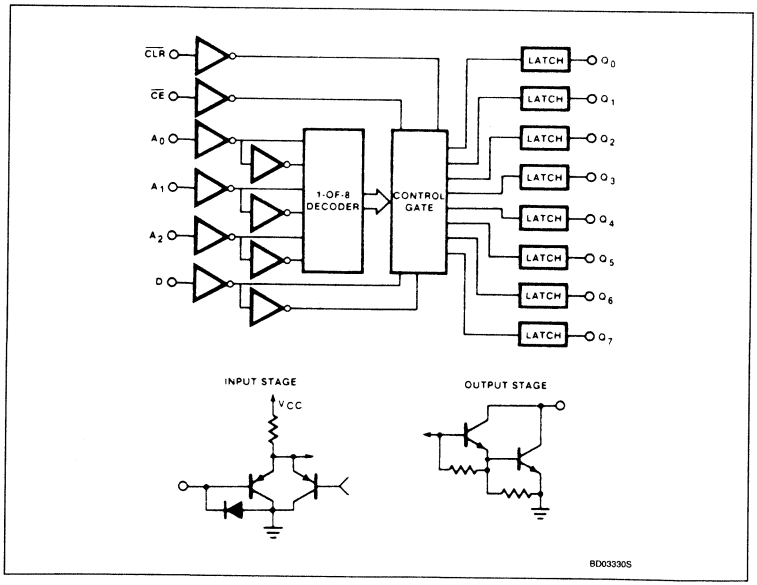


TOP VIEW

CD10060S

NOTE:
1. SOL-Released in Large SO package only.

BLOCK DIAGRAM



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1 – 3	$A_0 - A_2$	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4 – 7, 9 – 12	$Q_0 - Q_7$	The 8 device outputs.
13	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	CE	The chip enable. When this input is low, the output latches will accept data. When CE goes high, all outputs will retain their existing state, regardless of address of data input condition.
15	CLR	The clear input. When CLR goes low all output switches are turned "OFF". The high data input will override the clear function on the addressed latch.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE5090D
16-Pin Plastic DIP	0 to +70°C	NE5090N
16-Pin Cerdip	0 to +70°C	NE5090F
16-Pin Plastic DIP	−40 to +85°C	SA5090N

TRUTH TABLE

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							Addressable Latch
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

NOTES:
X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"ON" output state
H = High voltage level/"OFF" output state

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage	−0.5 to +15	V
V_{OUT}	Output voltage	0 to +30	V
I_{GND}	Ground current	500	mA
I_{OUT}	Output current Each output	200	mA
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package N package D package	 1388 1712 1315	 mW mW mW
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec. max)	300	°C

NOTE:
1. Derate above 25°C at the following rates:
   F package at 11.1mW/°C.
   N package at 13.7mW/°C.
   D package at 10.5mW/°C.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 4.75V$ to 5.25V, $0°C \leq T_A \leq +70°C$, unless otherwise specified.[1]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IH} V_{IL}	Input voltage High Low		2.0		 0.8	V
V_{OL}	Output voltage Low	$I_{OL} = 150mA$, $T_A = 25°C$ Over temperature		1.05	1.30 1.50	V
I_{IH} I_{IL}	Input current High Low	$V_{IN} = V_{CC}$ $V_{IN} = 0V$		< 1.0 −3.0	10 −250	μA
I_{OH}	Leakage current	$V_{OUT} = 28V$,		5	250	μA
I_{CCL} I_{CCH}	Supply current All outputs low All outputs high	$V_{CC} = 5.25V$		35 22	60 50	mA
P_D	Power dissipation	No output load			315	mW

NOTE:
1. All typical values are at $V_{CC} = 5V$ and $T_A = 25°C$.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C, V_{OUT} = 5V, I_{OUT} = 100mA, V_{IL} = 0.8V, V_{IH} = 2.0V.

SYMBOL	PARAMETER	TO	FROM	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time Low-to-high[1] High-to-low[1]	Output	$\overline{CE}$		900 130	1800 260	ns
t_{PLH} t_{PHL}	Low-to-high[2] High-to-low[2]	Output	Data		920 130	1850 260	ns
t_{PLH} t_{PHL}	Low-to-high[3] High-to-low[3]	Output	Address		900 130	1800 260	ns
t_{PLH} t_{PHL}	Low-to-high[4] High-to-low[4]	Output	$\overline{CLR}$		920	1850	ns
Switching setup requirements							
$t_{S(H)}$[5] $t_{S(L)}$[5]	Setup time high Setup time low	Chip enable Chip enable	High data Low data	40 50			ns
$t_{S(A)}$[6]	Address setup time	Chip enable	Address	40			ns
$t_{H(H)}$[5] $t_{H(L)}$[5]	Hold time high Hold time low	Chip enable Chip enable	High data Low data	10 10			ns
$t_{PW(E)}$[1]	Chip enable pulse width[1]			40			ns

NOTES:
1. See Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data-to-Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address-to-Output timing diagram.
4. See Turn-Off Delay, Clear-to-Output timing diagram.
5. See Setup and Hold Time, Data-to-Enable timing diagram.
6. See Setup Time, Address-to-Enable timing diagram.

FUNCTIONAL DESCRIPTION

This peripheral driver has latched outputs which hold the input date until cleared. The NE5090 has active-Low, open-collector outputs, all of which are cleared when power is first applied. This device is identical to the NE590, except the outputs can withstand 28V.

Addressable Latch Function

Any given output can be turned on or off by presenting the address of the output to be set or cleared to the three address pins, by holding the "D" input High to turn on the selected output, or by holding it Low to turn off, holding the $\overline{CLR}$ input High, and bringing the $\overline{CE}$ input Low. Once an output is turned on or off, it will remain so until addressed again, or until all outputs are cleared by bringing the $\overline{CLR}$ input Low while holding the $\overline{CE}$ input High.

Demultiplexer Operation

By holding the $\overline{CLR}$ and $\overline{CE}$ inputs Low and the "D" input High, the addressed output will remain on and all other outputs will be off.

High Current Outputs

The obvious advantage of this device over other drivers such as the 9334 and N74LS259 is the fact that the outputs of the NE5090 are each capable of 250mA and 28V. It must be noted, however, that the total power dissipation would be over 2.5W if all 8 outputs were on together and carrying 250mA each. Since the total power dissipation is limited by the package to 1W, and since power dissipation due to supply current is 0.25W, the total load power dissipation by the device is limited to 0.75W at room temperature, and decreases as ambient temperature rises.

The maximum die junction temperature must be limited to 165°C, and the temperature rise above ambient and the junction temperature are defined as:

$$T_R = \theta_{JA} \times P_D$$
$$T_J = T_A + t_R$$

where

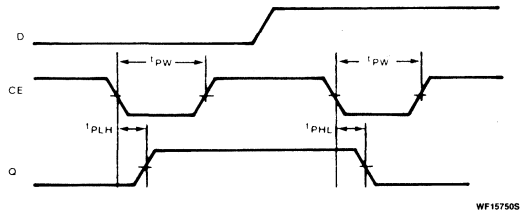
- θ_{JA} is die junction to ambient thermal resistance
- P_D is total power dissipation
- T_R is junction temperature rise above ambient
- T_J is die junction temperature
- T_A is ambient (surrounding medium) temperature

For example, if we are using the NE5090 in a plastic package in an application where the ambient temperature is never expected to rise above 50°C, and the output current at the 8 outputs, when on, are 100, 40, 50, 200, 15, 30, 80, and 10mA, we find from the graph of output voltage vs load current that the output voltages are expected to be about 0.92, 0.75, 0.78, 1.04, 0.5, 0.7, 0.9, and 0.4V, respectively. Total device power due to these loads is found to be 473.5mW. Adding the 250mW due to the power supply brings total device power dissipation to 723.5mW. The thermal resistances are 83°C per W for plastic packages and 100°C per W for Cerdips. Using the equations above we find:

Plastic $T_R = 83 \times 0.7235 = 60°C$
Plastic $T_J = 50 + 60 = 100°C$
Cerdip $T_R = 100 \times 0.7235 = 72.4°C$
Cerdip $T_J = 50 + 72.4 = 122.4°C$

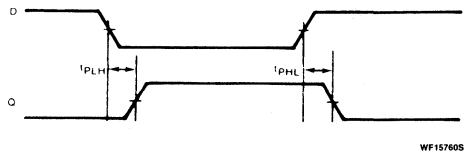
Thus we find that T_J for either package is below the 165°C maximum and either package could be used in this application. The graphs of total load power vs ambient temperature would also give us this same information, although interpreting the graphs would not yield the same accuracy.

TIMING DIAGRAMS



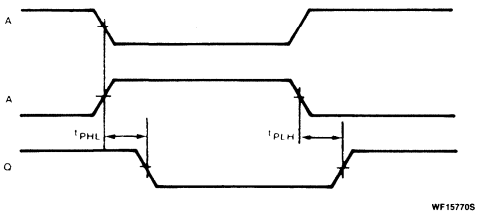
NOTE:
Other Inputs: $\overline{CLR}$ = H, A = Stable

Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width



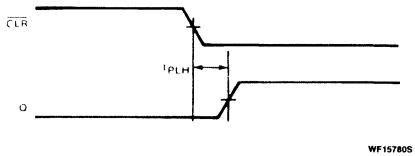
NOTE:
Other Inputs: $\overline{CE}$ = I, $\overline{CLR}$ = H, A = Stable

Turn-On and Turn-Off Delays, Data-to-Output



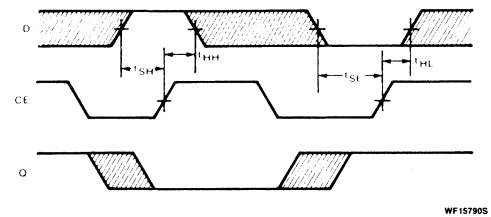
NOTE:
Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

Turn-On and Turn-Off Delays, Address-to-Output



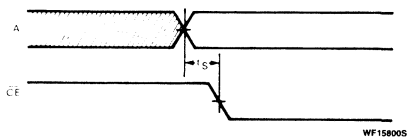
NOTE:
Other Inputs: $\overline{CE}$ = H

Turn-Off Delay, Clear-to-Output



NOTE:
Other Inputs: $\overline{CLR}$ = H, A = Stable

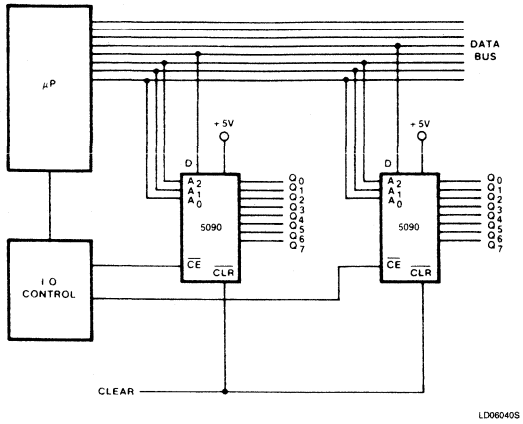
Setup and Hold TIme, Data-to-Enable



NOTE:
Other Inputs: $\overline{CLR}$ = H

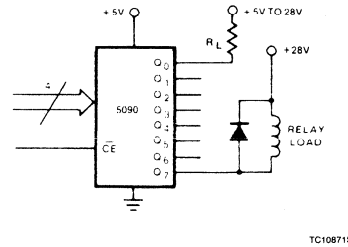
Setup Time, Address-to-Enable

TYPICAL APPLICATIONS

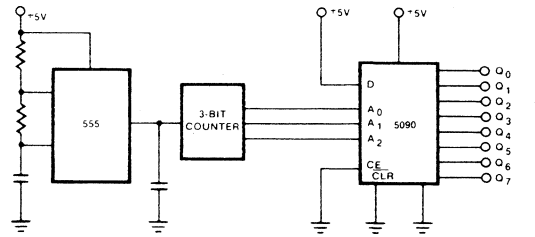


NOTE:
A_0, A_1, A_2 may be connected to the address bus if permitted by system design.

Interfacing With a Microprocessor System



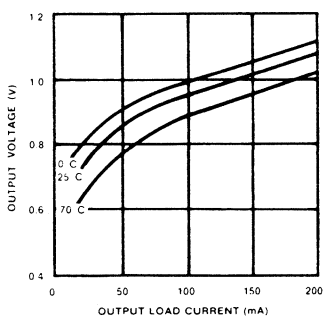
Driving Simple Loads



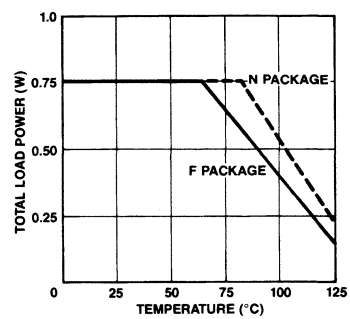
Operating in Demultiplex Mode

TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage vs Load Current



Total Load Power vs Temperature



UNIVERSAL INDUSTRIAL LOGIC AND INTERFACE CIRCUIT

GENERAL DESCRIPTION

The SAA1029 is a universal bipolar logic and interface IC with high noise immunity and operational stability for industrial control applications. The most fundamental industrial control functions can be accomplished with only one SAA1029 IC. Figure 1 shows the logic configuration.

The IC comprises,
(1) Gate 1: 4-input AND gate with 1 inverted input,
(2) Gate 2: 3-input AND gate with 1 inverted input and adjustable propagation delay,
(3) Gate 3: 2-input AND gate with 1 inverted input.
The SAA1029 can be used as direct interface with LOCMOS (CMOS) ICs for realizing more complex functions. Therefore, the output signal can be limited to the voltage level of the common output clamping pin Z.

The propagation delay of NAND gate 2 is adjustable from microseconds to seconds by using an external capacitor at pin C. This makes it possible to adapt the control frequency limits to the system, so the optimum dynamic noise immunity can be achieved.

All the static and dynamic circuit values (including the output voltage) are independent of the supply voltage over a wide operating range. This allows the use of a simple unstabilized power supply.

The output is held to the LOW state automatically during switching on the power supply, so a special reset pulse can be omitted.

Features

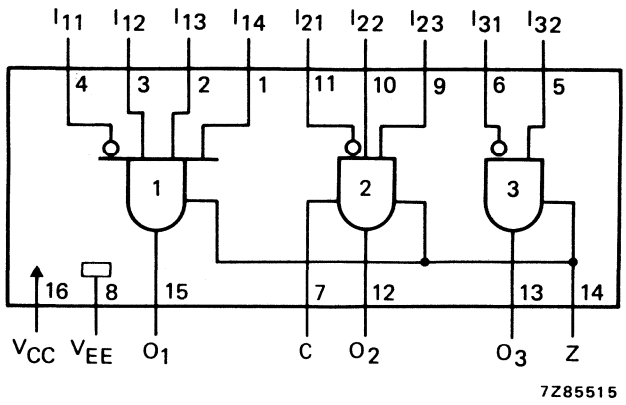
- Simple realization of the basic industrial control functions (logic functions, timing functions, memory functions).
- High dynamic and static noise immunity.
- High operation stability.
- Short-circuit protection of inputs and outputs to both V_{EE} and V_{CC}.
- Wide supply voltage range, so a simple power supply can be used.
- Wire interruption results in a safe input LOW state.
- LOCMOS (CMOS) compatible.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	14 to 31,2	V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Input voltage HIGH	V_{IH}	6,5 to 44	V
Output voltage HIGH (without clamping)	V_{OH}	13 to 30	V
Output voltage HIGH (with clamping at pin Z)	V_{OH}	2,0 to (V_{CC} −0,7)	V
Input current	I_I	max. 10	mA
Quiescent supply current	I_{CC}	typ. 7,8	mA

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).



Logic equations:

$O_1 = \overline{I_{11}} \cdot I_{12} \cdot I_{13} \cdot I_{14}$

$O_2 = \overline{I_{21}} \cdot I_{22} \cdot I_{23}$

$O_3 = \overline{I_{31}} \cdot I_{32}$

Fig. 1 Logic diagram.

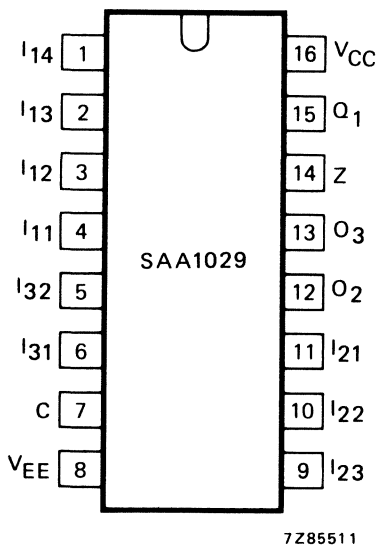


Fig. 2 Pinning diagram.

PINNING

4	I_{11}	inputs of gate 1
3	I_{12}	
2	I_{13}	
1	I_{14}	
15	O_1	output of gate 1
11	I_{21}	inputs of gate 2
10	I_{22}	
9	I_{23}	
12	O_2	output of gate 2
6	I_{31}	inputs of gate 3
5	I_{32}	
13	O_3	output of gate 3
7	C	external delay capacitor
14	Z	common output clamping
16	V_{CC}	positive supply voltage
8	V_{EE}	ground

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}		0 to + 35 V
Input voltage (independent of V_{CC})	V_I		−0,15 to + 44 V
Output clamping voltage (pin 14)	V_Z		0 to + 35 V
Voltage at any output (pins 12, 13 and 15)			
pin 14 (Z) open	V_O		−0,15 to V_{CC} V
pin 14 (Z) at V_Z	V_O	max.	V_Z V or V_{CC} if $V_{CC} < V_Z$
Current into any input			
d.c.	$\pm I_I$	max.	10 mA
t_p = 0,5 μs; δ = 0,1% (peak value)	$\pm I_{IM}$	max.	100 mA
Sum of input currents			
d.c.	ΣI_I		−90 to + 10 mA
t_p = 0,5 μs; δ = 0,1% (peak value)	ΣI_{IM}		−900 to + 300 mA
External applied current at any output (pins 12, 13 and 15)			
pin 14 (Z) open			
d.c.	$\pm I_O$	max.	30 mA
t_p = 0,5 μs; δ = 0,1% (peak value)	$\pm I_{OM}$	max.	500 mA
External applied current at any output (pins 12, 13 and 15)			
pin 14 (Z) at V_Z			
d.c.	I_O		−30 to + 10 mA
t_p = 0,5 μs; δ = 0,1% (peak value)	I_O		−500 to + 100 mA
Voltage at pin 7 (C)	V_C		−0,15 to + 6 V
External capacitor at pin 7 (C)	any value		
Short-circuit of outputs (pins 12, 13 and 15)			
pin 14 (Z) open	allowed to V_{CC} and V_{EE} (0 V)		
at $V_Z < V_{CC}$	allowed only to V_{EE} (0 V)		
Total power dissipation (see also Fig. 3)			
at T_{amb} = 50 °C; continuous	P_{tot}	max.	1100 mW
at T_{amb} = 65 °C; max. 1000 hours	P_{tot}	max.	1100 mW
Storage temperature range	T_{stg}		−40 to + 150 °C

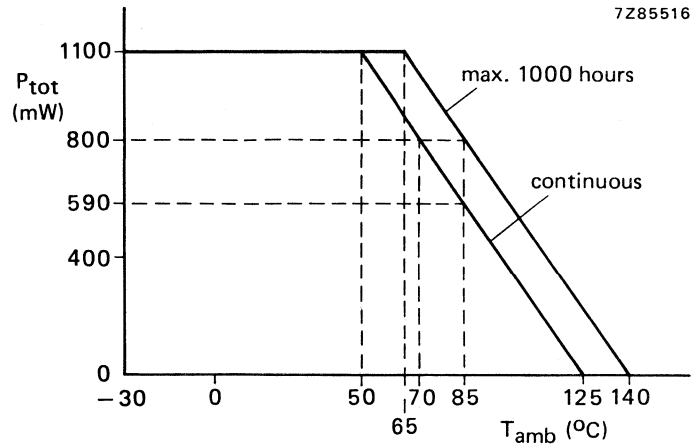


Fig. 3 Power derating curves; $R_{th\ j\text{-}a}$ = 70 K/W.

CHARACTERISTICS

At $T_{amb} = -30$ to $+85$ °C; $T_j \leqslant 125$ °C; $V_{CC} = 14$ to 31,2 V; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{CC}	14	24	31,2	V
Quiescent supply current		I_{CC}	–	7,8	–	mA
	$V_{CC} = 31$ V; $T_{amb} = 25$ °C	I_{CC}	–	–	12,2	mA
Quiescent current ratio	$I_{CC1} = I_{CC}$ at $T_j = 125$ °C $I_{CC2} = I_{CC}$ at $T_j = 25$ °C	$\frac{I_{CC1}}{I_{CC2}}$	–	0,67	–	
Input voltage LOW		V_{IL}	–	–	5	V
Input voltage HIGH		V_{IH}	6,5	–	–	V
		V_{IH}	6,55	–	–	V
Input current LOW		$-I_{IL}$	–	–	100	μA
		$-I_{IL}$	–	–	95	μA
Input current HIGH		I_{IH}	300	–	–	μA
Rate of change of input signal		dV/dt	3	–	–	V/ms
Input current*	$V_I = 1$ V	$-I_I$	–	–	120	μA
	$V_I = 35$ V	I_I	–	–	280	μA
Output clamping voltage*	$V_Z = V_{CC} - 1$ V	V_Z	–	–	30	V
Output voltage without clamping (pin 14 open)* non-inverting input: $V_I = 5,1$ V inverting input: $V_I = 6,3$ V	$V_{CC} = 14$ V					
LOW	$I_O = 1,32$ mA	V_{OL}	–	–	1	V
	$I_O = 2,91$ mA	V_{OL}	–	–	1,5	V
HIGH	$-I_O = 5$ mA	V_{OH}	$V_{CC}-1,4$	–	–	V
Output voltage with clamping (pin 14 at V_Z)*	$V_{CC} = 31,2$ V $V_Z < V_{CC}-1$ V					
LOW	$I_O = 1,32$ mA	V_{OL}	–	–	1	V
	$I_O = 1,91$ mA	V_{OL}	–	–	1,5	V

* At $T_{amb} = 25$ °C; $V_{CC} = 24$ V; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
HIGH	I_O = 0 mA	V_{OH}	(V_Z −0,475)	–	(V_Z + 0,225)	V
	$-I_O$ = 1 mA	V_{OH}	(V_Z −0,455)	–	(V_Z + 0,12)	V
	$-I_O$ = 3 mA	V_{OH}	(V_Z −0,41)	–	(V_Z + 0,055)	V
Output short-circuit current*						
LOW-signal	output at V_{CC}	I_{OscL}	2,95	–	9,6	mA
HIGH-signal	output at V_{EE} (0 V)	$-I_{OscH}$	10,1	–	21,9	mA
Capacitor charging current*		I_C	–	30	–	μA
Propagation delays*						
gates 1, 2 and 3						
HIGH to LOW	C = 0 (at gate 2)	t_{PHL}	–	3,5	–	μs
LOW to HIGH		t_{PLH}	–	3,5	–	μs
gate 2						
HIGH to LOW	C = 47 nF ± 1%	t_{PHL}	1,85	–	5,2	ms
LOW to HIGH	$R_{insulation} > 100$ MΩ	t_{PLH}	7,5	–	14	ms

* At T_{amb} = 25 °C; V_{CC} = 24 V; unless otherwise specified.

CHARACTERISTICS (worst case conditions)

At T_j = + 125 to + 140 °C; maximum 1000 hours

parameter	conditions	symbol	min.	typ.	max.	unit
Input voltage LOW		V_{IL}	–	–	5	V
Input voltage HIGH		V_{IH}	6,55	–	–	V
Input current	V_I = 1 to 44 V	I_I	95	–	300	μA
Change of input current overdrive of other inputs $\Sigma(-I_I) < 10$ mA	$V_I < V_{CC} - 1$ V	ΔI_I	–	–	120	μA
	$V_I > V_{CC} - 1$ V	ΔI_I	–	–	158	μA
overdrive of other inputs $\Sigma(-I_I) < 90$ mA	$V_I < V_{CC} - 1$ V	ΔI_I	–	–	280	μA
	$V_I > V_{CC} - 1$ V	ΔI_I	–	–	320	μA
Input voltage by current overdrive	$\Sigma(-I_I)$ = 10 mA	V_I	46	–	65	V
Output voltage without clamping (pin 14 open) LOW	$I_{OL} \leqslant 0{,}095$ mA	V_{OL}	–	–	0,35	V
	I_{OL} = 0,095 to 1 mA	V_{OL}	–	–	1	V
	I_{OL} = 1 to 2,5 V	V_{OL}	–	–	1,5	V
HIGH	$-I_{OH} \leqslant 5$ mA	V_{OH}	$V_{CC}-1{,}5$	–	–	V
Output voltage with clamping (pin 14 at V_Z)	V_Z = 2,5 to V_{CC} − 1 V					
HIGH	I_{OH} = 0 mA	V_{OH}	$(V_Z - 0{,}5)$	–	$(V_Z + 0{,}245)$	V
	I_{OH} = 1 mA	V_{OH}	$(V_Z - 0{,}5)$	–	$(V_Z + 0{,}15)$	V
	I_{OH} = 3 mA	V_{OH}	$(V_Z - 0{,}5)$	–	V_Z	V
	I_{OH} = 0 mA; V_Z = 0 V	V_{OH}	–	–	0,75	V
Output short-circuit current						
LOW-signal	output at V_{CC}	I_{OscL}	–	–	11	mA
HIGH-signal	output at V_{EE} (0 V)	$-I_{OscH}$	5	–	28,5	mA
HIGH-signal	output at V_{EE} (0 V); T_j = 140 °C	$-I_{OscH}$	–	–	10	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Current out of pin 14 (Z) when currents are forced into outputs	$-I_O \leqslant 3$ mA	$-I_Z$	–	–	2,2	mA
	$\Sigma I_O = (I_{O1} + I_{O2} + I_{O3})$	$-I_Z$	ΣI_O	–	–	mA
Current into pin 14 (Z) when inputs are set for output to be LOW	$-I_O = 30$ mA; $V_O \leqslant V_{EE}$	I_Z	–	–	300	μA
Supply current change	input and/or output voltages are negative with respect to V_{EE}	ΔI_{CCmax}	$(0{,}3 \times \lvert I_I \rvert) + (0{,}55 \times \lvert I_O \rvert)$			mA
Propagation delays gates 1 and 3						
HIGH to LOW		t_{PHL}	1	–	7	μs
LOW to HIGH		t_{PLH}	1	–	7	μs
gate 2						
HIGH to LOW	without capacitor	t_{PHL}	0,1	–	4	μs
LOW to HIGH	without capacitor	t_{PLH}	0,3	–	6	μs
HIGH to LOW	with capacitor; C in μF	t_{PHL}	38 x C	–	113 x C	μs
LOW to HIGH	with capacitor; C in μF	t_{PLH}	142 x C	–	334 x C	μs
Voltage spikes output LOW	see note 1	V_{OL}	–	–	2	V

Note to the characteristics

1. V_{CC} rising from 0 to 14 V; all inputs open; internally it is guaranteed that the input threshold voltage $V_{IL} > V_{OL}$.

APPLICATION INFORMATION

The following figures (Figs 4 to 11) give some examples of the basic industrial control functions.

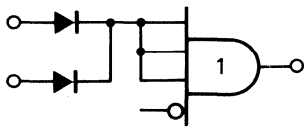


Fig. 4 OR function.

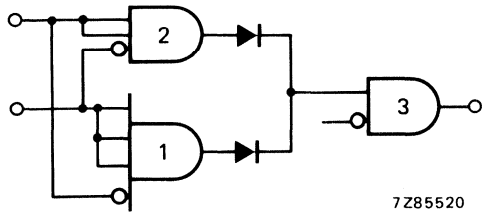


Fig. 5 EXCLUSIVE-OR function.

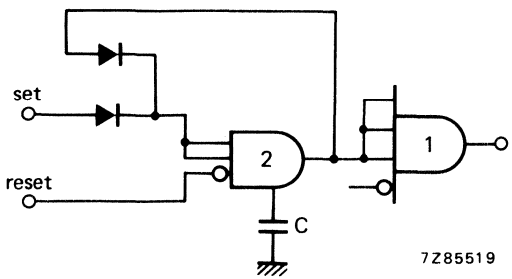


Fig. 6 Delayed memory; reset is dominating.

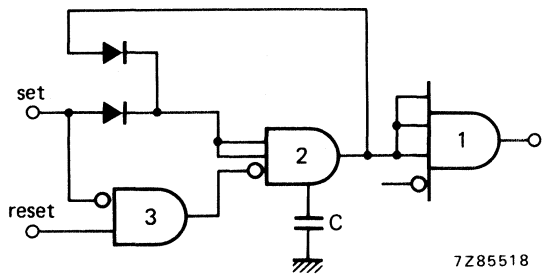


Fig. 7 Delayed memory; set is dominating.

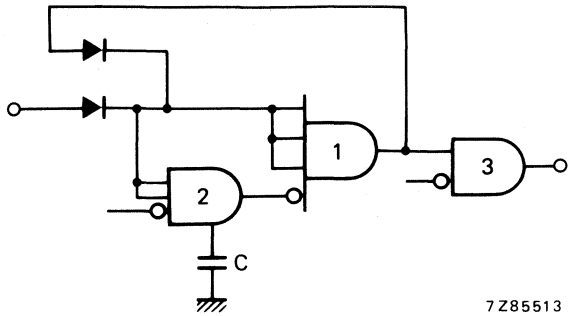


Fig. 8 Monostable flip-flop; for C = 4,7 μF, 1 s no reaction.

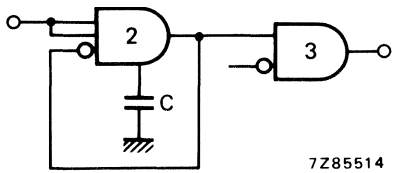


Fig. 9 Start delay function.

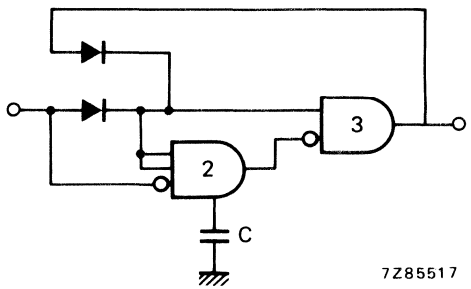


Fig. 10 Decay delay function.

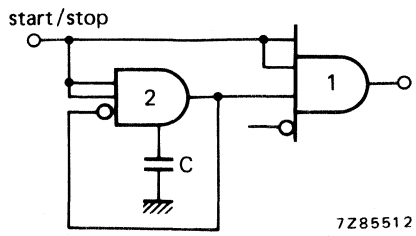


Fig. 11 Square-wave oscillator.

13-BIT SERIES-PARALLEL CONVERTER

GENERAL DESCRIPTION

The TEA1017 is a bipolar integrated circuit intended to drive displays, triacs and relays and small stepper motors. The data is serially shifted into the device and is stored in 13 latches that drive the outputs.

Features

- TTL and CMOS compatible inputs
- Outputs drive load in both directions
- Power-on reset makes outputs floating
- Wide supply voltage range

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4,5 to 18	V
Output current, each output	I_{OL}; $-I_{OH}$	max.	80	mA
Clock frequency	f_{CLK}	max.	50	kHz
Operating ambient temperature range	T_{amb}		0 to +80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

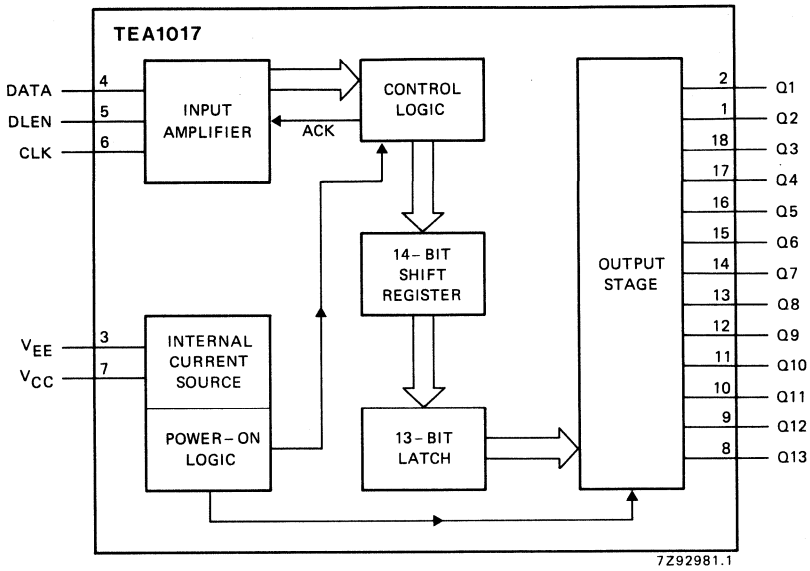


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The control logic performs a key function in this device. It checks whether the input information has the correct format: a DLEN signal that has been HIGH during 14 clock pulses, and a DATA signal with its first bit LOW.
When the format is found to be correct, the 15th clock pulse makes the control logic generate a signal that loads the content of the first 13 bits of the shift register into 13 latches. These drive the output stages.

"Acknowledge" (pin 4)

After the 15th clock pulse an acknowledge signal drives the DATA pin to LOW. To use this information the DATA should be programmed HIGH and an open collector-device, or a series resistor should be used on the DATA-input. This signal is valid till the next clock pulse, LOW-to-HIGH transition, see Fig. 3.

Supply V_{CC} (pin 7)

The supply current of the TEA1017 is regulated internally. This permits the circuit to be used over a very wide range of supply voltages, viz. 4,5 to 18 V, with little variation of supply current.

The circuit has a power-on reset arrangement that resets the circuit and sets the outputs to a high-impedance state. It requires a rise-time of the supply larger than 3 us/V.

DATA input (pin 4)

The circuit requires input information on the DATA input consisting of 14 bits, the first bit being LOW. This information should be synchronous with the clock pulse.
Data is loaded into the shift register at HIGH-to-LOW transitions of the clock pulse.

Data line enable input DLEN (pin 5)

A HIGH level on the DLEN input enables the shift register. This HIGH level should have a duration of 14 clock pulses (see Fig. 3).
After the DLEN input has returned to LOW the subsequent (15th) clock pulse transfers the contents of the shift register to the latches and then to the outputs.

Clock input CLK (pin 6)

The shift register shifts at the HIGH-to-LOW transitions of the clock pulse. The clock signal may be a continuously running clock or a clock burst of 15 clock pulses.

Outputs Q1 to Q13

The outputs are capable of supplying a load current in both directions, i.e. they can drive a load to the supply (V_{CC}) or to ground (V_{EE}).

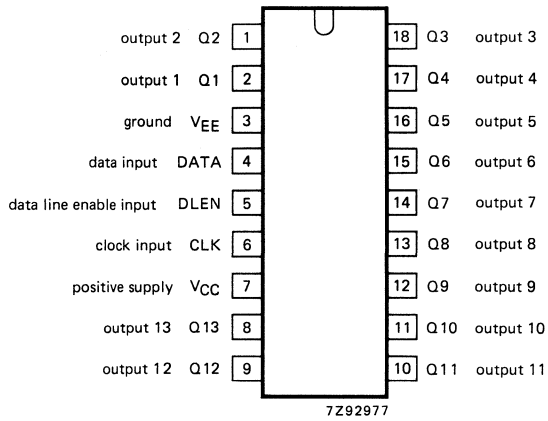


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	18	V
Input voltage range, all inputs	V_I	$-0,3$ to V_{CC}	$+0,3$	V
Output current, all outputs				
HIGH	$-I_{OH}$	max.	150	mA
LOW	I_{OL}	max.	150	mA
Total power dissipation *	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}	-40 to	$+150$	°C
Operating ambient temperature range	T_{amb}	0 to +	80	°C

* See Fig. 4.

CHARACTERISTICS

V_{CC} = 4,5 to 18 V; V_{EE} = 0 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7)					
Supply current					
during normal operation, unloaded					
at V_{CC} = 4,5 V	I_{CC}	–	45	60	mA
at V_{CC} = 18 V	I_{CC}	–	50	70	mA
during power-on blanking, unloaded					
at V_{CC} = 4,5 V	I_{CC}	–	1,5	2	mA
at V_{CC} = 18 V	I_{CC}	–	5	7	mA
Supply voltage rise time to ensure power on reset		3	–	–	μs/V
Clock input CLK (pin 6)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,8	V
Input current					
HIGH at V_{CLKH} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{CLKL} = 0,4 V	$-I_{IL}$	–	–	10	μA
Clock pulse duration					
HIGH	t_{WH}	8	–	–	μs
LOW	t_{WL}	10	–	–	μs
DATA input (pin 4)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,8	V
Input current					
HIGH at V_{IH} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{IL} = 0,4 V	$-I_{IL}$	–	–	10	μA
DATA input in sink current					
ACK = TRUE	I_{DACK}	1	–	–	mA
Data line enable input DLEN (pin 5)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,8	V
Input current					
HIGH at V_{5-3} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{5-3} = 0,4 V	$-I_{IL}$	–	–	10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Outputs Q1 to Q13					
Output voltage during normal operation					
HIGH at $-I_{OH}$ = 80 mA	V_{OH}	$V_{CC}-1,5$	–	–	V
LOW at I_{OL} = 80 mA	V_{OL}	–	–	1	V
Output current during power-on reset					
HIGH	$-I_{OH}$	–	–	10	μA
LOW	I_{OL}	–	–	10	μA
Rise and fall times: no maximum					
Minimum times as V_{CC} = 4,5 volts (see Fig. 3)					
Set-up time ENABLE	t_{SUDL}	2,8	–	–	μs
Hold time ENABLE	t_{HDL}	5,0	–	–	μs
Set-up time DATA	t_{SDA}	0	–	–	μs
Hold time DATA	t_{HDA}	2,8	–	–	μs
Set-up time LOAD	t_{SLO}	1,4	–	–	μs
Pulse width LOW	t_{WL}	10	–	–	μs
Pulse width HIGH	t_{WH}	8	–	–	μs
Max. clock input frequency = $1/(t_{WH} + t_{WL})$	f_{max}	–	–	50	kHz
Propagation delay					
clock to outputs	t_{PCQ}	–	–	8,5	μs
acknowledge	t_{PCA}	–	–	6	μs
acknowledge release	t_{PCAR}	–	–	6	μs

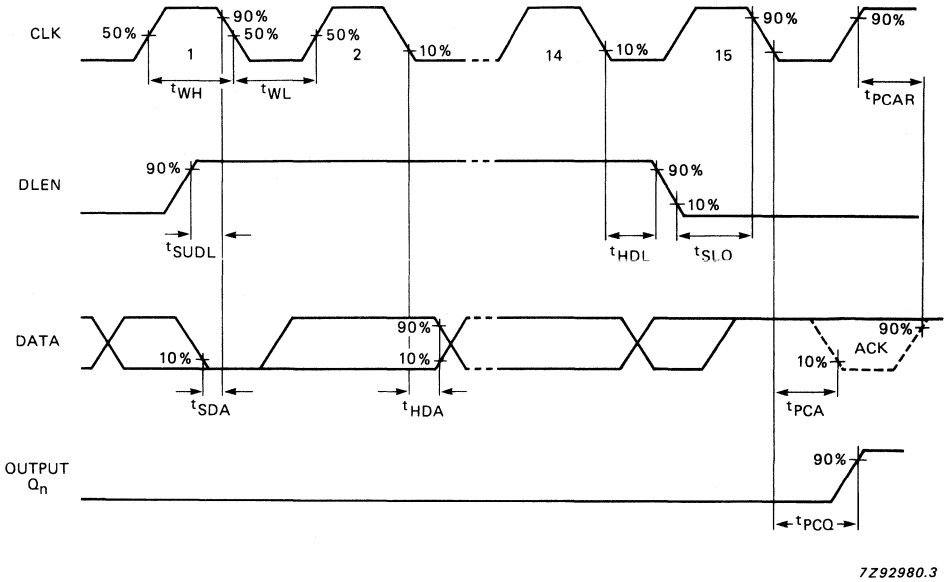


Fig. 3 Bus timing characteristics.

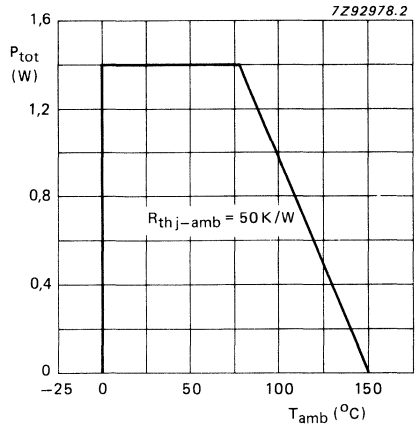


Fig. 4 Derating curve.

APPLICATION INFORMATION

1. From the buffer-capacitors C1 of the power supply the supply connections to the TEA1017 and the loads should be separated. An extra capacitor of 10 μF with good high-frequency characteristics should be mounted across the V_{CC} and V_{EE} connections as close as possible to the TEA1017.
2. If no use is made of the acknowledge information it is advised to program the data-output from the controller to LOW during the time ACK is valid. To use the acknowledge information the data-output has to be programmed HIGH. When a push-pull controller device is used a series resistor has to be connected in the data-line between the controller and TEA1017.
   The ACK may be sensed on the TEA1017-side of this resistor. See Fig. 5.

Note. ACK is removed from the data-line after the next LOW-to-HIGH transition of the clock-line with a maximum delay of 6 μs. (t_{PCA} maximum).

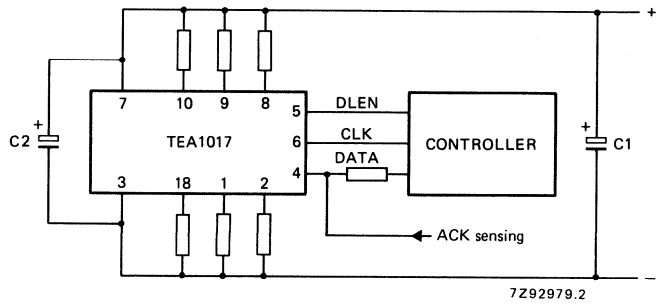


Fig. 5 TEA1017 with 3 loads to V_{CC} Q = 0 and 3 loads to V_{EE} Q = 1.

PROPORTIONAL-CONTROL TRIAC TRIGGERING CIRCUIT

GENERAL DESCRIPTION

The TDA1023 is a bipolar integrated circuit for controlling triacs in the time proportional or burst firing mode. It permits very precise temperature control of heating equipment and is especially suited for the control of panel heaters. The circuit generates positive-going trigger pulses and complies with the regulations on radio interference and mains distortion.

Features

- Adjustable proportional range width
- Adjustable hysteresis
- Adjustable trigger pulse width
- Adjustable firing burst repetition time
- Control range translation facility
- Failsafe operation
- Supplied from the mains
- Provides supply for external temperature bridge

QUICK REFERENCE DATA

Supply voltage (derived from mains voltage)	V_{CC}	typ.	13,7	V
Stabilized supply voltage for temperature bridge	V_Z	typ.	8	V
Supply current (average value)	$I_{16(AV)}$	typ.	10	mA
Trigger pulse width	t_w	typ.	200	μs
Firing burst repetition time at $C_T = 68\ \mu F$	T_b	typ.	41	s
Output current	$-I_{OH}$*	max.	150	mA
Operating ambient temperature range	T_{amb}	−20 to + 75		°C

* Negative current is defined as conventional current flow out of a device. A negative output current is suited for positive triac triggering.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

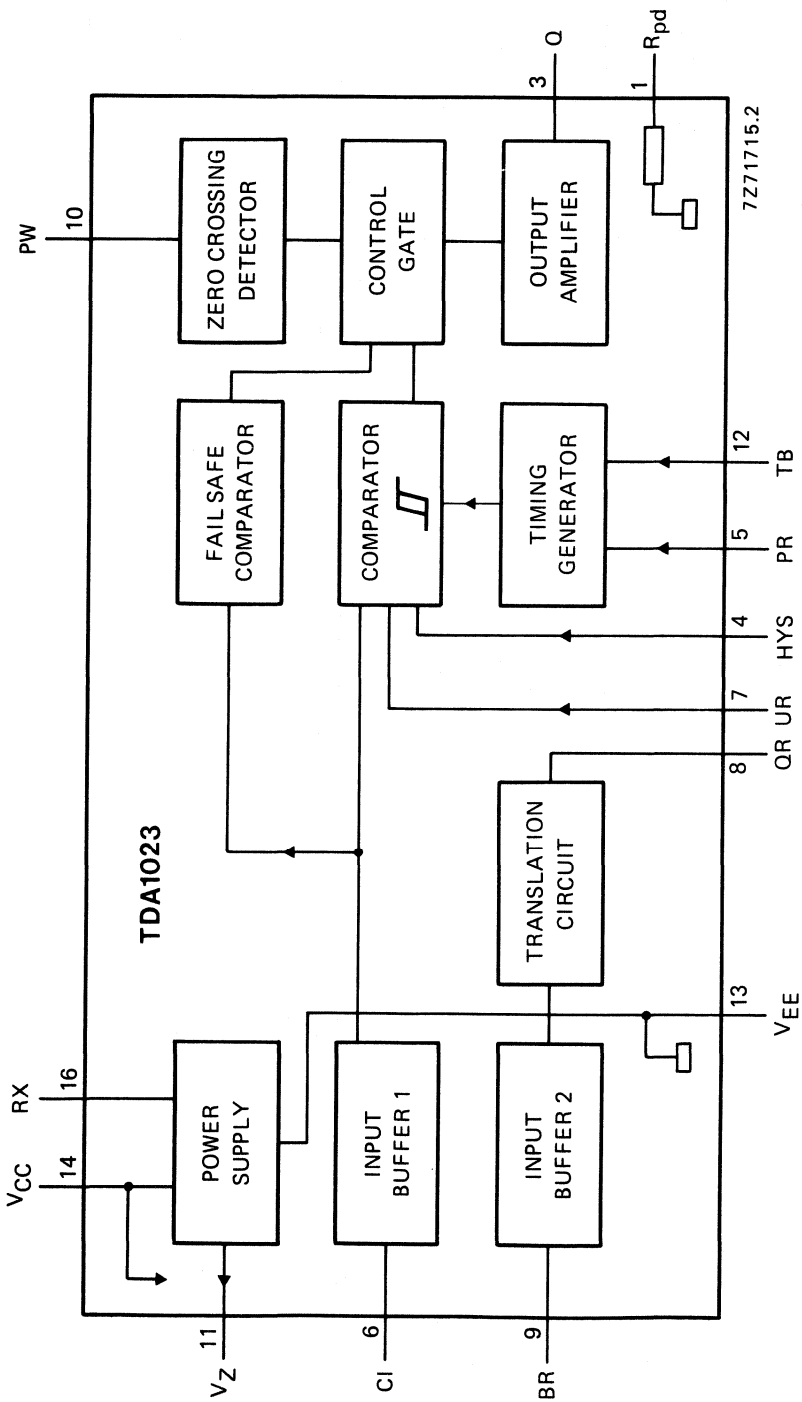


Fig. 1 Block diagram.

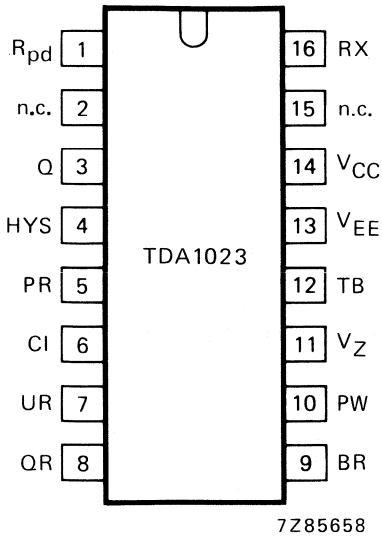


Fig. 2 Pinning diagram.

PINNING

1	R_{pd}	internal pull-down resistor connection
2	n.c.	not connected
3	Q	output
4	HYS	hysteresis control input
5	PR	proportional range control input
6	CI	Control input
7	UR	unbuffered reference input
8	QR	output of reference buffer
9	BR	buffered reference input
10	PW	pulse width control input
11	V_Z	reference supply output
12	TB	firing burst repetition time control input
13	V_{EE}	ground connection
14	V_{CC}	positive supply connection
15	n.c.	not connected
16	RX	external resistor connection

FUNCTIONAL DESCRIPTION

The TDA1023 generates pulses to trigger a triac. These trigger pulses coincide with the zero crossings of the mains voltage. This minimizes r.f. interference and transients on the mains supply. The trigger pulses come in bursts, with the net effect that the load is periodically switched on and off. This further minimizes mains pollution. The average power in the load is varied by varying the duration of the trigger pulse burst, in accordance with the voltage difference between the control input CI and the reference input, either UR or BR.

Power supply: V_{CC}, RX and V_Z (pins 14, 16 and 11)

The TDA1023 is supplied from the a.c. mains via a resistor R_D to the RX connection (pin 16); the V_{EE} connection (pin 13) is connected to the neutral line (see Fig. 4a). A smoothing capacitor C_S has to be connected between the V_{CC} and V_{EE} connections.

The circuit contains a string of stabilizer diodes between the RX and V_{EE} connections that limit the d.c. supply voltage, and a rectifier diode between the RX and V_{CC} connections (see Fig. 3).

At pin 11 the device provides a stabilized reference voltage V_Z for an external temperature sensing bridge.

The operation of the supply arrangement is as follows. During the positive half of the mains cycles the current through external voltage dropping resistor R_D charges the external smoothing capacitor C_S until RX reaches the stabilizing voltage of the internal stabilizer diodes. R_D should be chosen such that it can supply the current I_{CC} for the TDA1023 itself plus the average output current $I_{3(AV)}$ plus the current required from the V_Z connection for an external temperature bridge, and recharge the smoothing capacitor C_S (see Figs 9 to 12). Any excess current is bypassed by the internal stabilizer diodes. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles external smoothing capacitor C_S has to supply the sum of the currents mentioned above. Its capacitance must be high enough to maintain the supply voltage above the minimum specified limit.

FUNCTIONAL DESCRIPTION (continued)

Dissipation in resistor R_D is halved by connecting a diode in series (see Fig. 4b and 9 to 12).

A further reduction of dissipation is possible by using a high-quality voltage dropping capacitor C_D in series with a resistor R_{SD} (see Figs 4c and 14). Asuitable VDR connected across the mains provides protection of the TDA1023 and of the triac against mains-borne transients.

Control and reference inputs CI, BR and UR (pins 6, 9 and 7)

For room temperature control (5 °C to 30 °C) the best performance is obtained by using the translation circuit. The buffered reference input BR (pin 9) is used as a reference input, and the output of the reference buffer QR (pin 8) is connected to the unbuffered reference input UR (pin 7). In this arrangement the translation circuit ensures that most of the potentiometer rotation can be used to cover the room temperature range. This provides an accurate temperature setting and a linear temperature scale.

If the translation circuit is not required, the unbuffered reference input UR (pin 7) is used as a reference input. The buffered reference input BR (pin 9) must be connected to the reference supply output V_Z (pin 11).

For proportional power control the unbuffered reference input UR (pin 7) must be connected to the firing burst repetition time control input TB (pin 12) and the buffered reference input BR (pin 9), which is inactive now, must be connected to the reference supply output V_Z (pin 11).

In all arrangements the train of output pulses becomes longer when the voltage at the control input CI (pin 6) becomes lower.

Proportional range control input PR (pin 5)

With the proportional range control input PR open the output duty factor changes from 0% to 100% by a variation of 80 mV at the control input CI (pin 6). For temperature control this corresponds with a temperature difference of only 1 K.

This range may be increased to 400 mV, i.e. 5 K, by connecting the proportional range control input PR (pin 5) to ground. Intermediate values are obtained by connecting the PR input to ground via a resistor R5, see Table 1.

Hysteresis control input HYS (pin 4)

With the hysteresis control input HYS (pin 4) open the device has a built-in hysteresis of 20 mV. For temperature control this corresponds with 0,25 K.

Hysteresis is increased to 320 mV, corresponding with 4 K, by grounding HYS (pin 4). Intermediate values are obtained by connecting pin 4 to ground via a resistor R4. See Table 1 for a set of values for R4 and R5 giving a fixed ratio between hysteresis and proportional range.

Trigger pulse width control input PW (pin 10)

The trigger pulse width may be adjusted to the value required for the triac by choosing the value of the external synchronization resistor R_S between the trigger pulse width control input PW (pin 10) and the a.c. mains. The pulse width is inversely proportional to the input current (see Fig. 13).

Output Q (pin 3)

Since the circuit has an open-emitter output, it is capable of sourcing current, i.e. supplying a current out of the output. Therefore it is especially suited for generating positive-going trigger pulses. The output is current-limited and protected against short-circuits. The maximum output current is 150 mA and the output pulses are stabilized at 10 V for output currents up to that value.

FUNCTIONAL DESCRIPTION (continued)

A gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Figs 5 to 8). This minimizes the total supply current and the power dissipation.

Pull-down resistor R_{pd} (pin 1)

The TDA1023 includes a 1,5 kΩ pull-down resistor R_{pd} between pins 1 and 13 (V_{EE}, ground connection), intended for use with sensitive triacs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC}	max.	16	V
Supply current				
average	$I_{16(AV)}$	max.	30	mA
repetitive peak	$I_{16(RM)}$	max.	100	mA
non-repetitive peak	$I_{16(SM)}$	max.	2	A
Input voltage, all inputs	V_I	max.	16	V
Input current, CI, UR, BR, PW input	$I_{6;7;9;10}$	max.	10	mA
Voltage on R_{pd} connection	V_1	max.	16	V
Output voltage, Q, QR, V_Z output	$V_{3;8;11}$	max.	16	V
Output current				
average	$-I_{OH(AV)}$	max.	30	mA
peak, max. 300 μs	$-I_{OH(M)}$	max.	700	mA
Total power dissipation	P_{tot}	max.	500	mW
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−20 to +	75	°C

CHARACTERISTICS

V_{CC} = 11 to 16 V; T_{amb} = −20 to + 75 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply: V_{CC} and RX (pins 14 and 16)					
Internally stabilized supply voltage at I_{16} = 10 mA	V_{CC}	12	13,7	15	V
Variation with I_{16}	$\Delta V_{CC}/\Delta I_{16}$	–	30	–	mV/mA
Supply current at $V_{16\text{-}13}$ = 11 to 16 V; I_{10} = 1 mA; f = 50 Hz; pin 11 open; $V_{6\text{-}13} > V_{7\text{-}13}$; pins 4 and 5 open	I_{16}	–	–	6	mA
pins 4 and 5 grounded	I_{16}	–	–	7,1	mA
Reference supply output V_Z (pin 11) for external temperature bridge					
Output voltage	$V_{11\text{-}13}$	–	8	–	V
Output current	$-I_{11}$	–	–	1	mA
Control and reference inputs CI, BR and UR (pins 6, 9 and 7)					
Input voltage to inhibit the output	$V_{6\text{-}13}$	–	7,6	–	V
Input current at V_I = 4 V	$I_{6;7;9}$	–	–	2	μA
Hysteresis control input HYS (pin 4)					
Hysteresis, pin 4 open	ΔV_6	9	20	40	mV
pin 4 grounded	ΔV_6	–	320	–	mV
Proportional range control input PR (pin 5)					
Proportional range, pin 5 open	ΔV_6	50	80	130	mV
pin 5 grounded	ΔV_6	–	400	–	mV
Pulse width control input PW (pin 10)					
Pulse width at $I_{10(RMS)}$ = 1 mA; f = 50 Hz	t_w	100	200	300	μs
Firing burst repetition time control input TB (pin 12)					
Firing burst repetition time, ratio to capacitor C_T	T_b/C_T	320	600	960	ms/μF
Output of reference buffer QR (pin 8)					
Output voltage at input voltage $V_{9\text{-}13}$ = 1,6 V	$V_{8\text{-}13}$	–	3,2	–	V
$V_{9\text{-}13}$ = 4,8 V	$V_{8\text{-}13}$	–	4,8	–	V
$V_{9\text{-}13}$ = 8 V	$V_{8\text{-}13}$	–	6,4	–	V

	symbol	min.	typ.	max.	unit
Output Q (pin 3)					
Output voltage HIGH at $-I_{OH}$ = 150 mA	V_{OH}	10	–	–	V
Output current HIGH	$-I_{OH}$	–	–	150	mA
Internal pull-down resistor R_{pd} (pin 1)					
Resistance to V_{EE}	R_{pd}	1	1,5	3	kΩ

Table 1 Adjustment of proportional range and hysteresis.
Combinations of resistor values giving hysteresis > ¼ proportional range.

proportional range mV	proportional range resistor R5 kΩ	minimum hysteresis mV	maximum hysteresis resistor R4 kΩ
80	open	20	open
160	3,3	40	9,1
240	1,1	60	4,3
320	0,43	80	2,7
400	0	100	1,8

Table 2 Timing capacitor C_T values.

effective d.c. value	marked a.c. specification		catalogue number*
μF	μF	V	
68	47	25	2222 016 90129
47	33	40	– – 90131
33	22	25	– 015 90102
22	15	40	– – 90101
15	10	25	– – 90099
10	6,8	40	– – 90098

* Special electrolytic capacitors recommended for use with TDA1023.

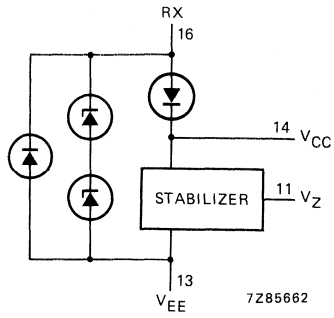


Fig. 3 Internal supply connections.

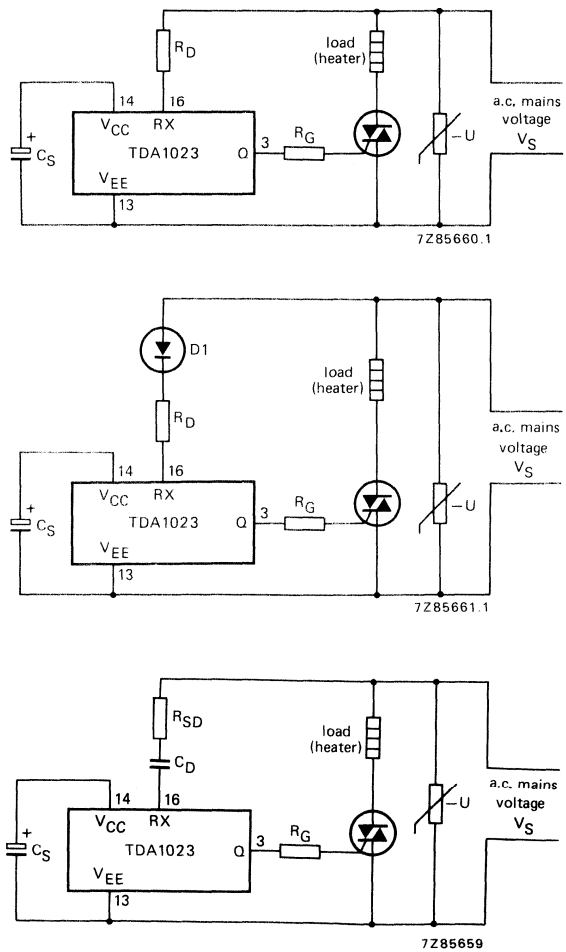


Fig. 4 Alternative supply arrangements.

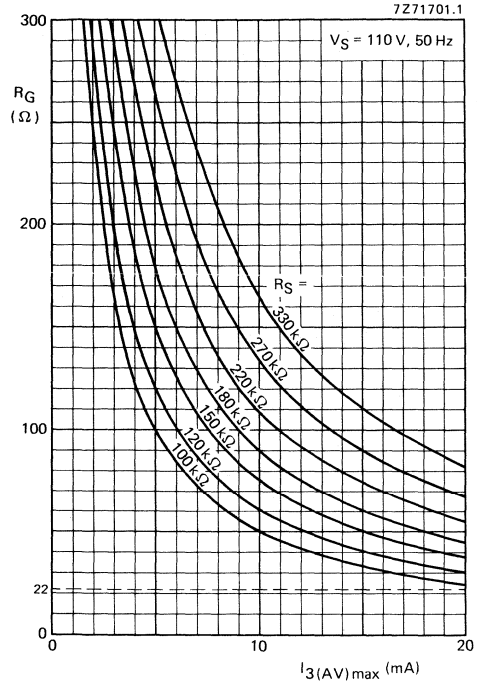


Fig. 5.

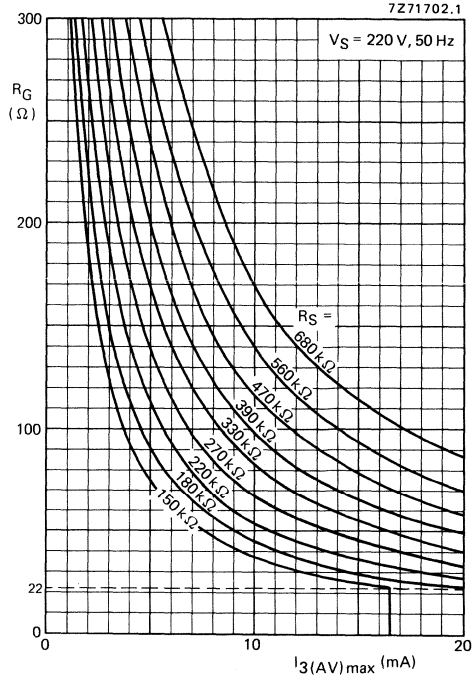


Fig. 6.

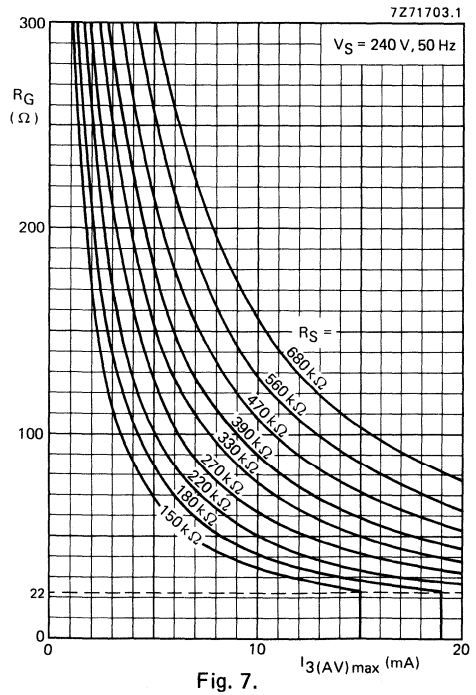


Fig. 7.

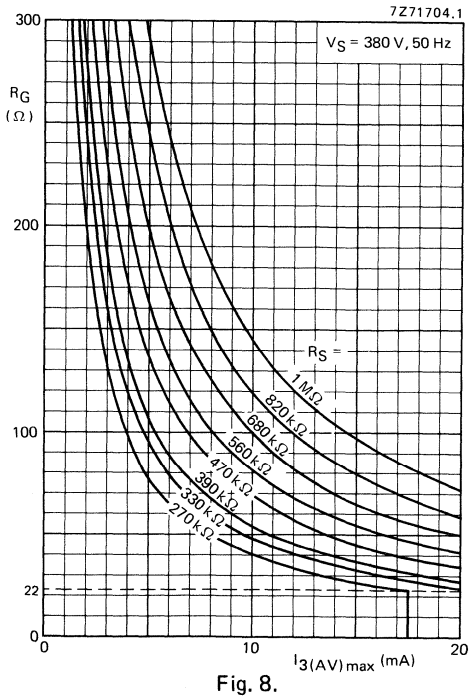


Fig. 8.

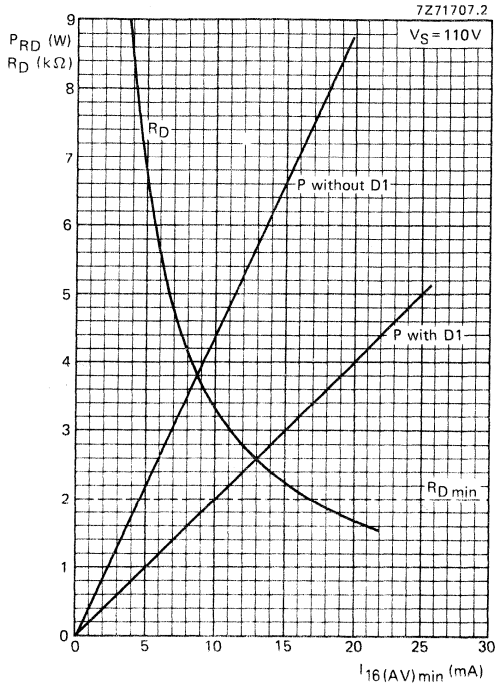


Fig. 9.

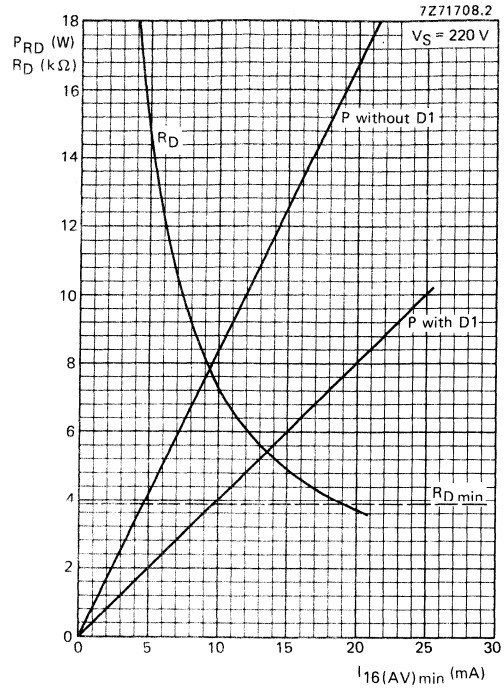


Fig. 10.

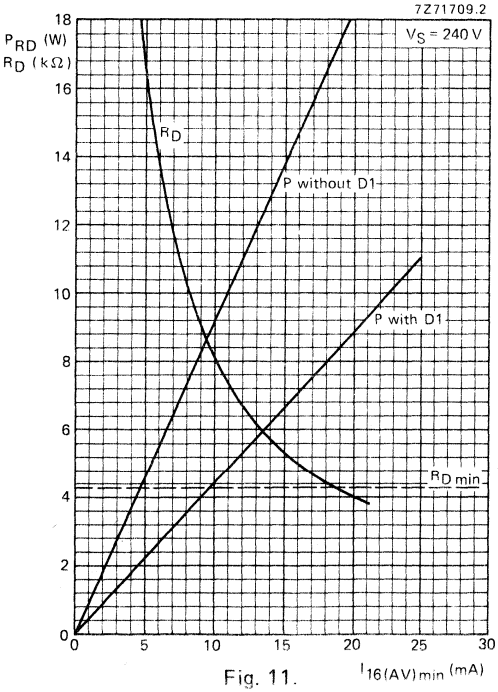


Fig. 11.

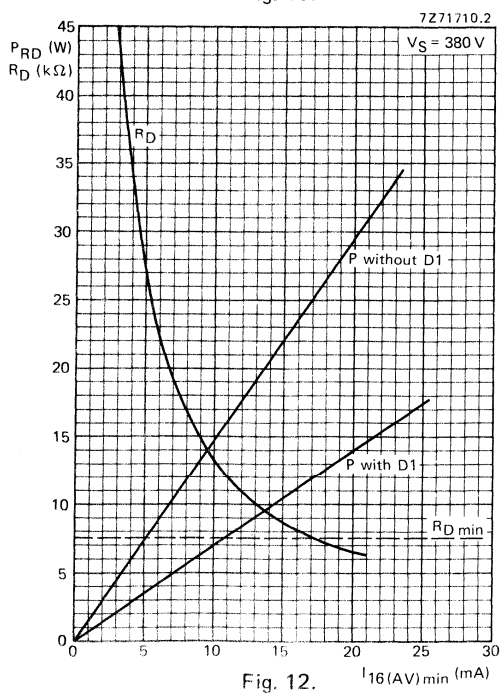


Fig. 12.

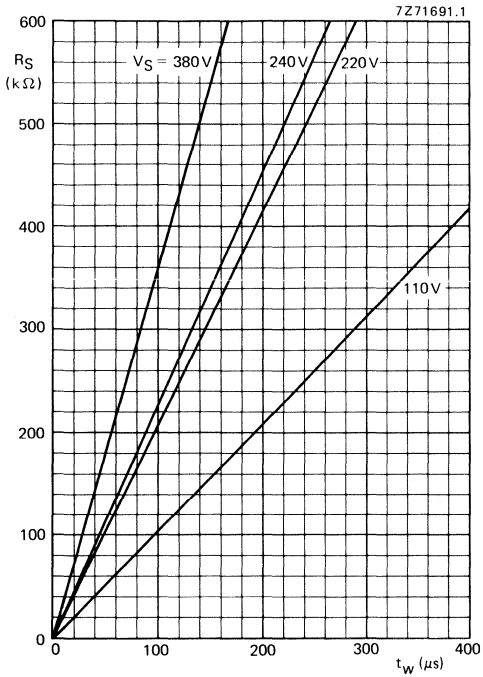


Fig. 13 Synchronization resistor R_S as a function of required trigger pulse width t_w with mains voltage V_S as a parameter.

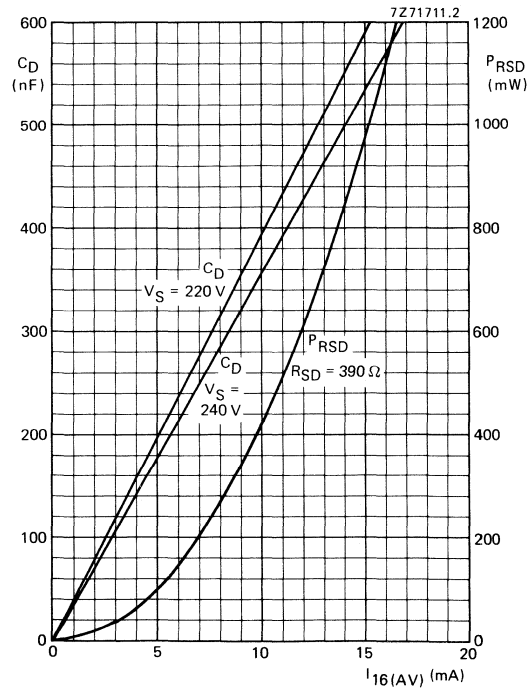


Fig. 14 Nominal value of voltage dropping capacitor C_D and power P_{RSD} dissipated in voltage dropping resistor R_{SD} as a function of the average supply current $I_{16(AV)}$ with the mains supply voltage V_S as a parameter.

APPLICATION INFORMATION

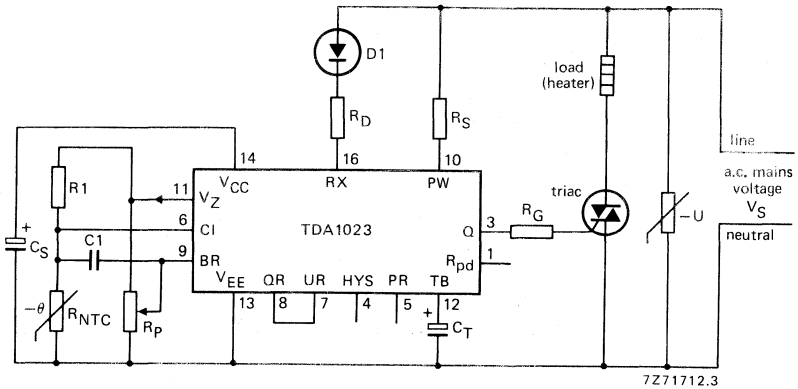


Fig. 15 The TDA1023 used in a 1200 to 2000 W heater with triac BT139. For component values see Table 3.

Conditions

Mains supply: V_S = 220 V

Temperature range = 5 to 30 °C

BT139 data: $V_{GT} < 1{,}5$ V
$I_{GT} > 70$ mA
$I_L < 60$ mA
} at T_j = 25 °C

Table 3 Temperature controller component values (see Fig. 15).

parameter	symbol	value	remarks
Trigger pulse width	t_w	75 μs	see BT139 data sheet
Synchronization resistor	R_S	180 kΩ	see Fig. 13
Gate resistor	R_G	110 Ω	see Fig. 6
Max. average gate current	$I_{3(AV)}$	4,1 mA	see Fig. 8
Hysteresis resistor	R4	n.c.	see Table 1
Proportional band resistor	R5	n.c.	see Table 1
Min. required supply current	$I_{16(AV)}$	11,1 mA	
Mains dropping resistor	R_D	6,2 kΩ	see Fig. 10
Power dissipated in R_D	P_{RD}	4,6 W	see Fig. 10
Timing capacitor (eff. value)	C_T	68 μF	see Table 2
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 593 62512
Rectifier diode	D1	BYW56	
Resistor to pin 11	R1	18,7 kΩ	1% tolerance
NTC thermistor (at 25 °C)	R_{NTC}	22 kΩ	B = 4200 K cat. no. 2322 642 12223
Potentiometer	R_P	22 kΩ	
Capacitor between pins 6 and 9	C1	47 nF	
Smoothing capacitor	C_S	220 μF; 16 V	
If R_D and D1 are replaced by C_D and R_{SD}			
Mains dropping capacitor	C_D	470 nF	see Fig. 14
Series dropping resistor	R_{SD}	390 Ω	
Power dissipated in R_{SD}	P_{RSD}	0,6 W	
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 594 62512

Notes

1. ON/OFF control: pin 12 connected to pin 13.
2. If translation circuit is not required: slider of R_P to pin 7; pin 8 open; pin 9 connected to pin 11.

APPLICATION INFORMATION SUPPLIED ON REQUEST

AN1291
Design of Time-Proportional Temperature Controls Using the TDA1023

Application Note

Electronic temperature control is no longer new; phase and on/off controls for room heaters have been widely used to replace mechanical switches. However, both phase and on/off control have disadvantages. Phase control produces RF interference and transients on the mains supply, while the hysteresis required to prevent oscillation of the output for on/off control systems prevents accurate control of the temperature.

Time-proportional control, with zero-crossing switching, eliminates these disadvantages, giving accurate temperature control and no RF interference or supply transients. The TDA1023 has been designed to provide time-proportional control using a minimum number of external components. It incorporates additional features to provide fail-safe operation and fine control of the temperature in the range 5°C to 35°C.

The design of the TDA1023 is such that it may also be usefully employed as a time-proportional power regulator for heating elements in electric cookers.

THE PRINCIPLE OF TIME-PROPORTIONAL CONTROL

Conventional phase control allows fully-proportional control of the power dissipated in the load, but the high rates of change of current and voltage cause RF interference. Because of this effect, phase control is not allowed to be used for domestic heaters. Simple on/off control with zero-voltage switching avoids generation of RFI but does not possess the required accuracy when stabilized with a small amount of hysteresis.

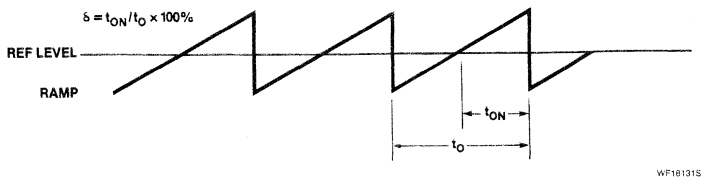
Time-proportional control combines the zero-voltage switching of on/off control with the accuracy of proportional control. Figures 1 and 2 illustrate the principle: the load is switched on once and off once in a fixed repetition period, the ratio of the on and off periods providing the proportional control. This method of control can cause mains flicker; the mains voltage will change slightly each time the load is switched on or off.

CENELEC, the European Committee for Electro-technical Standardization, has published rules which limit the rate at which domestic heating apparatus may be switched on and off. Table 1 gives the minimum repetition period for a range of load powers and common mains voltages from CENELEC publication EN50.006.

There are three states of operation when using time-proportional control.

- load switched fully off
- load power proportional to the difference between actual and desired temperatures, while within the proportional range
- load switched fully on.

Clearly, this system of control will regulate the load power such that there will be no overshoot or undershoot of the desired temperature as is the case with normal on/off systems (see Figure 2). The minimum range over which there is proportional control is about 1°C, corresponding to about 80mV at the input to the comparator. This allows extremely accurate control of the temperature.



NOTE:
A change in the reference level will cause a change in t_{ON} and the load power.

Figure 1. Load Power is Proportional to the Duty Factor

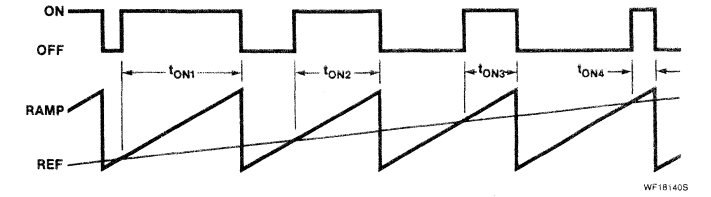


Figure 2. An Increase in Temperature Raises the Reference Voltage, Causing a Decrease in the Duty Factor and Average Load Power

DESCRIPTION OF THE TDA1023

The TDA1023 is a 16-pin dual in-line integrated circuit designed to provide time-proportional power control of electrical heating elements, particularly panel heaters. Its time-proportional control system allows accurate temperature stabilization with the minimum of external components. Apart from panel heaters, the TDA1023 is ideally suited for the control of:

- Cooker elements
- Electric irons
- Water heaters
- Industrial temperature control, e.g., oil baths, air conditioners, etc.

It incorporates the following functions:

- A stabilized power supply. The TDA1023 may be connected directly to the AC mains using either a dropping resistor or capacitor. It provides a stabilized reference voltage for the temperature-sensing network.
- A zero-crossing detector to synchronize the output trigger pulses to the zero-crossings of the mains supply. The detector produces a pulse, the duration of which is determined by an external resistor, centered on the zero-crossing of the mains voltage.
- A comparator with adjustable hysteresis, preventing spurious triggering of the output. This compares a thermistor voltage, a function of the room

Design of Time-Proportional Temperature Controls Using the TDA1023

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Table 1. Minimum Repetition Periods for Domestic Heater Applications

APPLIANCE POWER (W)	REPETITION PERIOD t_O (s)		
	220V	240V	380V (AC)
600	0.2	0.2	
800	0.8	0.3	0.1
1000	2.0	1.0	0.2
1200	4.6	2.0	0.2
1400	7.0	4.3	0.2
1600	10	6.3	0.3
1800	16	8.9	0.5
2000	24	13	0.9
2200	32	17	1.3
2400	40	24	1.9
2600		31	2.6
2800			3.6

temperature, with the voltage from the temperature selection dial.

- A voltage translation circuit for the potentiometer input. Normally, the relatively small temperature variation in a room (5°C to 30°C) corresponds to a narrow angle of rotation of the potentiometer shaft. Use of this circuit doubles the angle of rotation of the potentiometer shaft for the same temperature range.
- A sensor fail-safe circuit to prevent triggering if the thermistor input becomes open or short-circuited.
- A timing generator with an adjustable proportional band. This allows a full 100% control of the load current over a temperature range of only 1°C. It can be adjusted to work over a range of 5°C. The repetition period of the timing generator may be set by an external capacitor to conform to the CENELEC specifications for mains load switching.
- An output amplifier with a current-limited output. The amplifier has an output current capability of at least 200mA and is stabilized to 10V while the current limit is not exceeded.
- Two input buffers, to isolate the voltage translation circuit and comparator from external influences.
- A control gate circuit to activate the output if there is a mains zero-crossing, the comparator is ON and the fail-safe comparator is OFF.

Although designed specifically for time-proportional control, the TDA1023 is also suitable for applications requiring on/off control if the timing generator is not used. In that case, Pin 12 must be connected to ground to inhibit the timing waveform.

SELECTION OF EXTERNAL COMPONENTS

The external components required by the TDA1023 determine the operating characteristics of the device. The following paragraphs describe the selection of these components to ensure reliable operation under worst-case conditions.

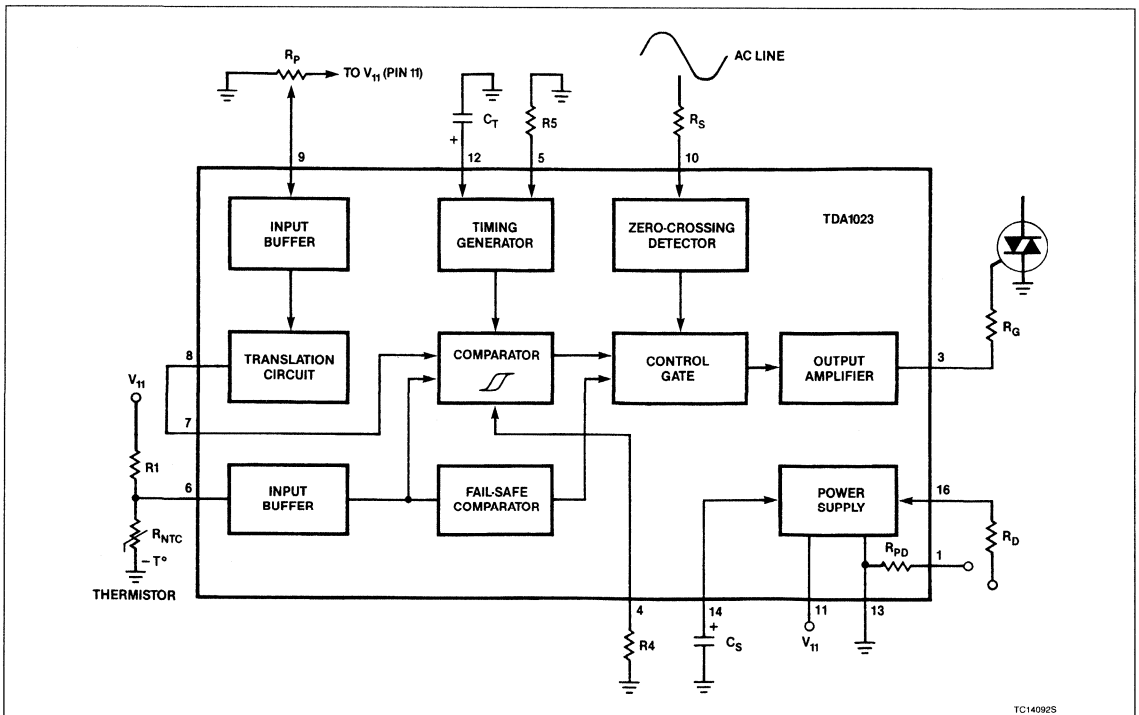


Figure 3. Block Diagram of the TDA1023 and the Required External Components

Design of Time-Proportional Temperature Controls Using the TDA1023

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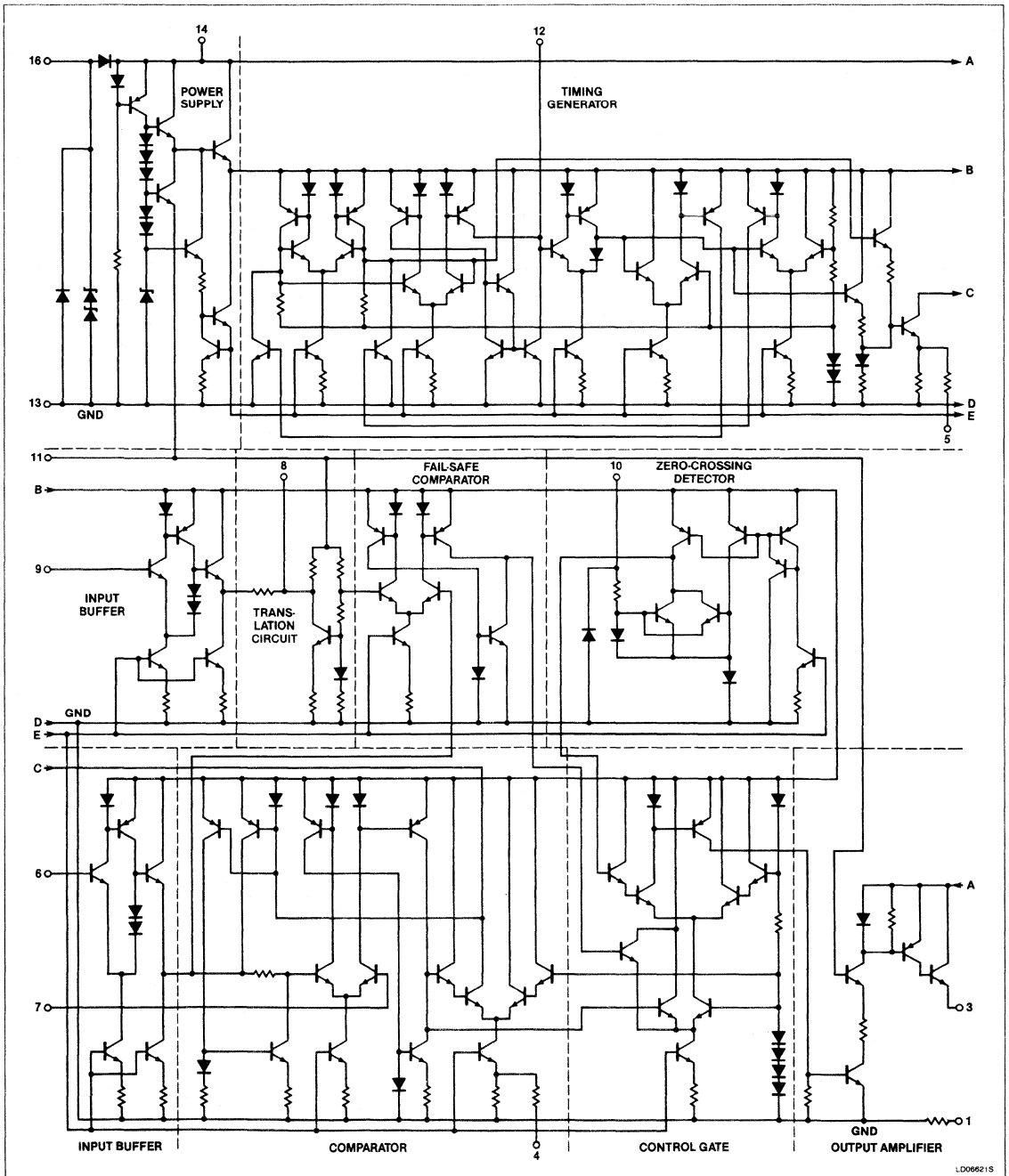


Figure 4. Circuit Diagram of the TDA1023

Design of Time-Proportional Temperature Controls Using the TDA1023

Required Duration of Triac Trigger Pulse

The main advantage of triggering at the instant when the applied voltage passes through zero is that this mode of operation renders the use of RF suppression components unnecessary. For time-proportional control, continuous conduction of the triac may be required for many cycles of the mains supply. To maintain conduction while the load current is approaching the zero-crossing, the trigger pulse must last from the time when the load current falls to the value of the triac holding current (I_H), until the time when the load current reaches the triac latching current (I_L). In general, the latching current of a triac is 20% higher than the holding current, so the minimum trigger pulse duration may be taken as twice the time for the load current in the triac (I_T) to rise from zero to the triac's latching current (see Figure 5).

The current passed by the triac is a function of its on-state voltage, the load resistance, and the applied AC voltage. The required trigger pulse width (t_P) is therefore a function of:

- The triac latching current (I_L)
- The applied AC voltage ($v = V \sin \omega t$)
- The load resistance (R)
- The on-state voltage of the triac (V_T) at I_L.

The following equation can be derived:

$$t_P = \frac{2(I_L R + V_T)}{dv/dt} \text{ at } t = 0.$$

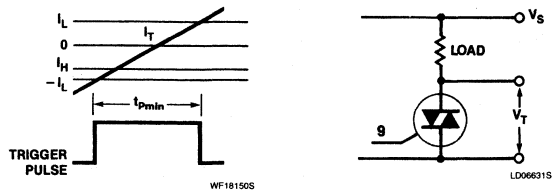


Figure 5. Definition of Minimum Trigger Pulse Width for Mains Zero-Voltage Triggering

Assuming that the load resistance has a tolerance of 5% and the AC voltage variation is 10%, the minimum required width of the trigger pulse in the worst case is:

$$t_{P\ MIN} = \frac{2(1.05RI_L + V_T)}{0.9\omega\sqrt{2V_S}}$$

in which $R = \frac{V_S^2}{P}$, where P is the nominal heater power and V_S is the nominal supply voltage.

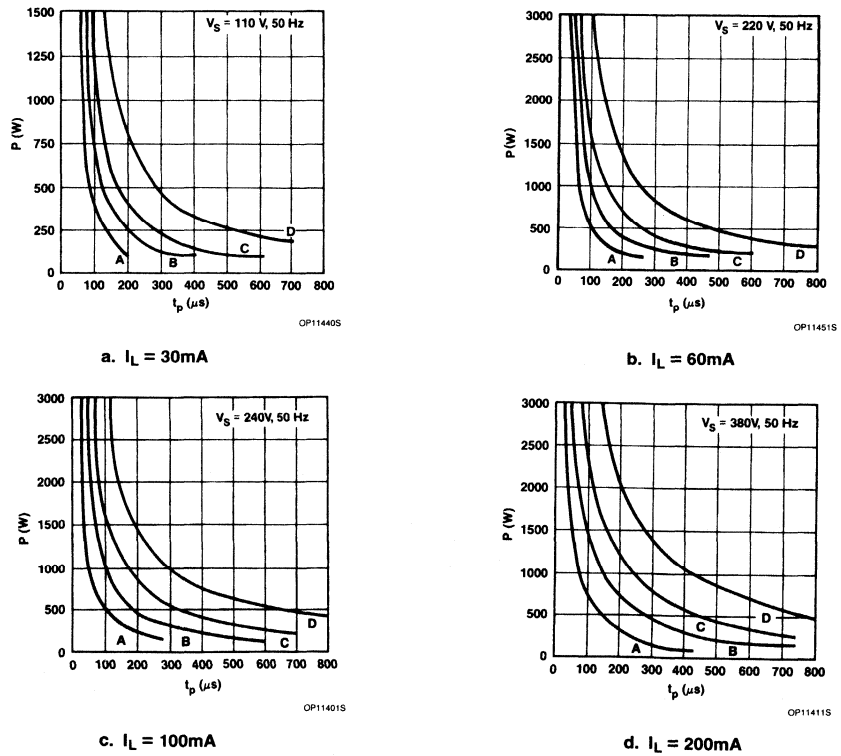


Figure 6. Minimum Pulse Width as a Function of Switched Power for Four Supply Voltages, with Latching Current as a Parameter

Design of Time-Proportional Temperature Controls Using the TDA1023

Using this equation, with values of 30mA, 60mA, 100mA, and 200mA for the triac latching current I_L, and a maximum on-state voltage of 1.2V at I_L, the graphs of Figure 6 were computed. These show $t_{P\ MIN}$ as a function of P, with I_L as a parameter, for four common mains voltages.

Synchronization Resistor

the zero-crossing detector used to provide trigger pulse synchronization is a current comparator. It compares the current through the synchronization resistor (R_S) with a fixed internal reference current. As the supply voltage passes through zero, the current in the synchronization resistor becomes less than the reference current and a trigger pulse is given until the current in R_S increases above the reference current.

Thus, the duration of the trigger pulse depends upon the rate of change of current in R_S at the supply voltage zero-crossing point. This rate of change is affected by:

- the AC supply voltage
- the supply frequency
- the value of the synchronization resistor.

The general expression for the width of the trigger pulse is:

$$t_P = t_P^* \times \frac{1mA}{I_{10}}$$

where I_{10} is the RMS current flowing into Pin 10 in mA, at 50Hz, and t_P^* is the specified trigger pulse at $I_{10} = 1mA$.

When the frequency of the supply is not 50Hz, the value of t_P may be found by multiplying the right-hand side of the equation by the factor:

$$\frac{50}{f_{SUPPLY}}$$

The minimum width of the trigger pulse available from Pin 3 of the TDA1023 is specified in the published data as 100μs with a synchronization current into Pin 10 of 1mA at 50Hz.

Assuming a tolerance of 10% for the mains supply voltage and 5% for the synchronization resistor, the worst-case minimum trigger pulse duration for the TDA1023 appears to be:

$$t_{P\ MIN} = 0.1\,\frac{0.95R_S}{1.1V_S}\,\mu s.$$

This, however, is not realistic because the longest trigger pulse is required when the rate of change of the triac current is slowest, i.e., when the applied voltage is minimum (see Figure 5). The true worst-case therefore occurs when the applied voltage is minimum and the pulse due to R_S is minimum. This is given by:

$$t_{P\ MIN} = 0.1\,\frac{0.95R_S}{0.9V_S}\,\mu s.$$

Figure 7 shows the value of R_S as a function of the required trigger pulse width with the AC supply voltage as a parameter.

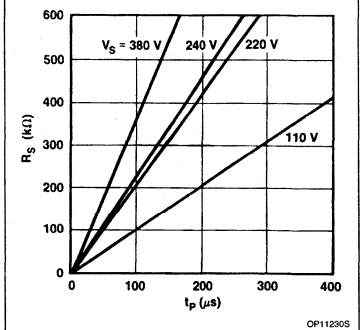


Figure 7. Synchronization Resistor Values as a Function of Required Trigger Pulse Width with Applied AC Voltage as a Parameter

Gate Resistor Value

The guaranteed minimum amplitude of the output trigger pulse at Pin 3 of the TDA1023 is specified as 10V at an output current of 200mA. The output voltage is at least 10V for all values of output current less than 200mA. The output stage is protected against damage due to short-circuits by current-limiting action when the current rises above 200mA.

Although the output is current-limited, it is still advantageous to include a gate series resistor in the circuit. Inclusion of a gate resistor to limit the gate current to the minimum value required reduces the overall current consumption and the power dissipation in the mains dropping resistor. Furthermore, the point at which current limiting occurs is subject to considerable variation between samples of the TDA1023: a gate resistor will reduce the effect of this in production circuits.

The rectangular output V/I characteristic of the TDA1023 is shown in Figure 8. Load lines for various values of gate resistor (with a worst-case tolerance of +5%) have been plotted on this diagram so that the maximum value of gate resistor can be selected by plotting horizontal and vertical lines to represent the required minimum gate current and voltage. The following example illustrates the use of Figure 8.

The triac to be triggered is a type BT139. The trigger pulse requirements for reliable triggering of all devices at 0°C are:

$I_{GT\ MIN}$ = 72mA;

$V_{GT\ MIN}$ = 1.6V.

The lines representing $V_{GT} = 1.6V$ and $I_3 = 72mA$ cross between the load lines for gate resistor values of 100Ω and 120Ω. The maximum value of gate resistor is thus 100Ω for this example.

If gate resistor values are to be calculated more accurately, Figure 9 shows that:

$$R_{G\ MAX} = \frac{V_3 - V_{GT\ MIN}}{1.05I_3}$$

where V_3 is stabilized to 10V and the resistor tolerance is 5%.

Gate Termination Resistor R_{PD}

The TDA1023 has a resistor of approximately 1.5kΩ between Pin 1 and Pin 13. This is intended for use as a pull-down resistor when sensitive triacs are being used.

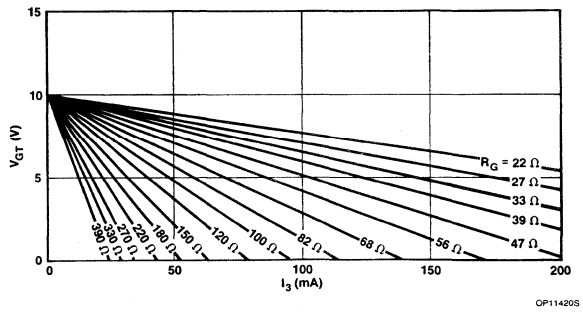


Figure 8. Gate Voltage as a Function of Output Current with Gate Resistor Load Lines

Design of Time-Proportional Temperature Controls Using the TDA1023

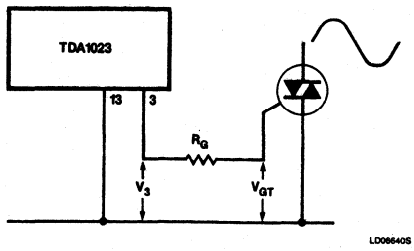


Figure 9. Inclusion of a Gate Series Resistor to Limit Trigger Current

Hysteresis Resistor R_4

The comparator of the TDA1023 is designed with built-in hysteresis to eliminate instability and oscillation of the output which would cause spurious triggering of the triac. Apart from providing a stable two-state output, the hysteresis gives the comparator increased noise immunity and prevents half-waving.

Figure 10 shows the application of hysteresis to the comparator and the transfer characteristic obtained. The comparator switches when the voltage at point A becomes equal to the reference voltage, V_7. The current source I_H is switched on when the voltage at Pin 6 is Low. As the voltage at Pin 6 rises, corresponding to a drop in temperature, the voltage at point A also rises, but, because of the current I_H being drawn through R_H, V_A is $I_H R_H$ less than V_6. For the comparator to switch, V_6 must increase to a value of $V_7 + I_H R_H$, corresponding to V_A equal to V_7. At this point the circuit switches and the current I_H is turned off, resulting in an increase of $I_H R_H$ volts at point A. For the circuit to switch back to its original state, the voltage V_6 must decrease by $I_H R_H$ volts.

The built-in hysteresis is 20mV; this may be increased by adding a resistor (R_4) from Pin 4 to ground which increases the current I_H. Pin 4 shorted to ground gives a maximum of 320mV. Table 2 gives the value of R_4 for a range of hysteresis settings.

Table 2. Choice of Hysteresis According to Proportional Band Setting

PROP. BAND (mV)	R_5 (kΩ)	MIN HYST (mV)	MAX R_4 (kΩ)
80		20	
160	3.3	40	9.1
240	1.1	60	4.3
320	0.43	80	2.7
400	0	100	1.8

The Proportional Band Resistor R_5

The proportional band is the voltage range at Pin 6 that provides control from 0% to 100% of the load power. The TDA1023 has a built-in proportional band of 80mV (corresponding to about 1°C) which can be increased by the addition of resistor R_5 between Pin 5 and ground. The maximum proportional band of 400mV is obtained by shorting Pin 5 to ground. The proportional band is derived from the triangular timing waveform, Figures 11 and 12.

When the proportional band (V_{pb}) is increased, it may be necessary to increase the hysteresis voltage (V_h) according to the requirement:

$$V_h \geq \frac{V_{pb}}{4}$$

In accordance with this requirement, Table 2 gives a range of proportional band settings, the values of R_5 required for these, the corresponding minimum hysteresis voltage and the maximum value of hysteresis resistor R_4.

Timing Capacitor C_T

The minimum repetition period required for a particular application can be found in Table 1. This timing is selected using the external capacitor C_T connected between Pin 12 and ground. Typical electrolytic capacitors have wide tolerances: +50% to −10%. Moreover, the effective DC capacitance is different from the marked (AC) value, usually 20% greater. Thus, the use of standard capacitors may lead to repetition periods far in excess of those required.

Special capacitors

A special range of electrolytic capacitors has been developed for use with the TDA1023. These have the following advantages:

- Effective DC capacitance is known for each marked AC value
- Tolerance for the DC capacitance is ±20%
- Very low leakage current (< 1μA)
- Long lifetime (> 100,000 hours at 40°C).

Table 3 gives details of these capacitors. In all further references to C_T, the use of the special capacitors is assumed.

The timing circuit

The TDA1023 employs a triangular waveform for timing purposes. This gives two advantages over the conventional sawtooth waveform:

- For a given capacitor value, the triangular waveform provides twice the repetition period that the sawtooth gives, allowing the use of smaller capacitors.
- The effects of the capacitor leakage current are minimized, reducing the spread in repetition periods.

Figure 11 shows the generation of the triangular waveform using two current sources.

The published data for the TDA1023 specifies the repetition period as 0.6 ±0.2s/μF. The special capacitors have ±20% tolerances. The value of a capacitor required for a particular minimum repetition period is given by:

$$0.8C_T = \frac{t_{O\ MIN}}{0.4},$$

where C_T is in μF and t_O in seconds.

The maximum value, $t_{O\ MAX}$, resulting from the use of the capacitor to achieve the required $t_{O\ MIN}$ may be derived from the equation:

$$t_{O\ MAX} = 1.2C_T \times 0.8$$

where C_T is in μF and t_O in seconds.

Figure 13 shows the repetition period as a function of the timing capacitor for nominal and worst-case conditions. Table 4 is derived from Figure 13 and shows the minimum preferred value of C_T (DC value) to provide the required minimum repetition time for a range of appliance powers operating at 220V AC. The resulting nominal, minimum, and maximum repetition times are also given. In the case of 1.8 and 2kW appliances, the minimum time is slightly less than that required. However, this situation is unlikely to occur in practice; if larger capacitors are used, the nominal repetition times become very long.

Design of Time-Proportional Temperature Controls Using the TDA1023

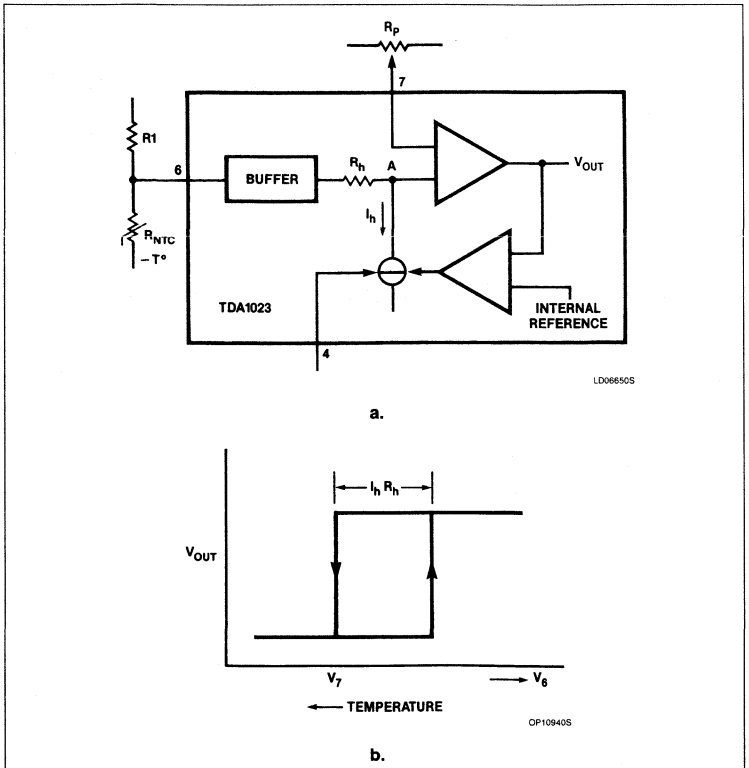


Figure 10. Hysteresis is Included in the Circuit of (a) Giving the Transfer Characteristic in (b)

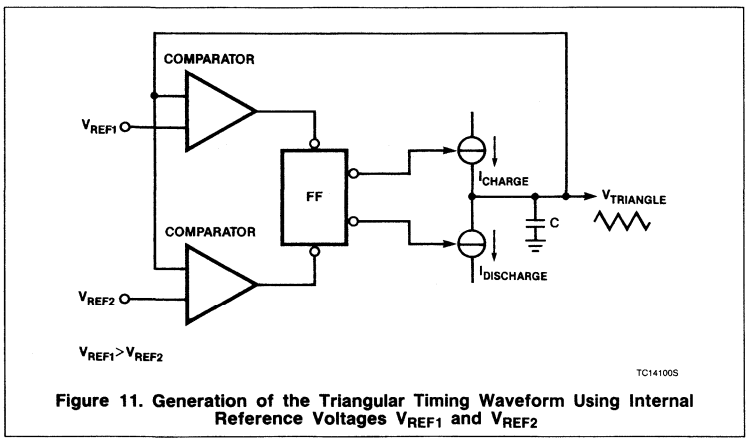


Figure 11. Generation of the Triangular Timing Waveform Using Internal Reference Voltages V_{REF1} and V_{REF2}

INFLUENCE OF THE INPUT VOLTAGE TRANSLATION CIRCUIT ON THE DESIGN OF THE TEMPERATURE SENSING BRIDGE

Many arrangements of temperature sensing networks are possible; the circuit of Figure 14 requires a minimum of components and possesses the advantage of eliminating performance spreads due to potentiometer tolerances. When room heaters are to be controlled, the voltage variation at the NTC thermistor will be very much less than the available voltage variation at the potentiometer. This will result in the required temperature range being controlled by a very small angle of rotation of the potentiometer shaft. The voltage translation circuit incorporated in the TDA1023 allows the use of 80% of the potentiometer rotation for the normal range of room temperatures, allowing far more accurate control of the temperature. If the voltage translation circuit is not used, Pins 9 and 11 must be shorted together to disable the circuit.

The transfer characteristic of the translation circuit is shown in Figure 15. Because only 80% of the potentiometer is used, the midpoint of the slider voltage range is at 60% of V_{11}, which must correspond to the thermistor voltage at 20°C. From Figure 14:

$$\frac{V_6}{V_{11}} = \frac{R_{20}}{R_{20} + R_1} = 0.6$$

giving:

$$R_1 = \frac{2R_{20}}{3}$$

where R_{20} is the thermistor resistance at 20°C.

The resistance of an NTC thermistor at a given temperature is determined by the equation:

$$R_{NTC} = A \exp (B/T)\ \Omega$$

where $A = R_{25}/\{\exp(B/298)\}$, B is a constant for the device type, and T is the temperature in degrees Kelvin.

The characteristics of a suitable NTC thermistor (catalog number 2322 642 12223) are:

$R_{25} = 22k\Omega \pm 10\%$;

$B = 4200 \pm 5\%$.

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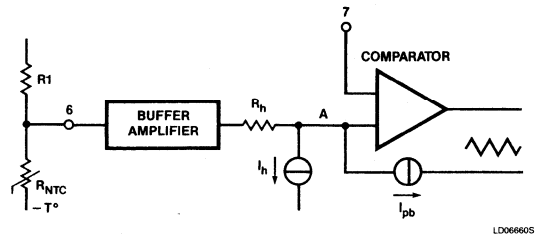


Figure 12. The Proportional Band is Produced by a Triangular Current Waveform I_{pb}

Table 3. Special Capacitors for use with TDA1023

MARKED AC SPECIFICATION (μF)	(V)	EFFECTIVE DC VALUE (μF)	CATALOG NUMBER
47	25	68	2222 016 90129
33	40	47	2222 016 90131
22	25	33	2222 015 90102
15	40	22	2222 015 90101
10	25	15	2222 015 90099
6.8	40	10	2222 015 90098

Table 4. Repetition Time Capacitor Values for 220V Operation

APPLIANCE POWER (W)	t_O (CENELEC) (sec)	C_T (DC) (μF)	t_O NOM (sec)	t_O MIN (sec)	t_O MAX (sec)
2000	24	68	41	22	65
1800	16	47	28	15	45
1600	10	33	20	11	32
1400	7	22	13	7	21
1200	4.6	15	9	4.8	14
1000	2	10	6	3.2	9.6
800	0.8	10	6	3.2	9.6
600	0.3	10	6	3.2	9.6

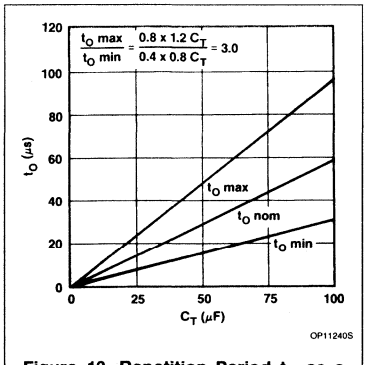


Figure 13. Repetition Period t_O as a Function of the Timing Capacitor for Nominal and Worst-Case Values

A thermistor with these values is chosen to provide a compromise between low current consumption and noise sensitivity: high impedance reduces current but increases noise sensitivity.

The thermistor resistance at 20°C is thus:

$$R_{20} = R_{25} \exp (4200/293 - 4200/298)\Omega = 27.982k\Omega.$$

This gives a value of 18.654kΩ for R_1; a practical value is 18.7kΩ ±1%.

LIMITATION IMPOSED UPON THE VALUE OF RESISTOR R_1 DUE TO THE FAIL-SAFE CIRCUIT

The TDA1023 is fail-safe for both short-circuit and open-circuit conditions. Either of these conditions will prevent production of trigger pulses for the triac.

Short-circuit sensing is automatically obtained from the normal temperature sensing circuit. When the thermistor input voltage is zero, the triac will never be triggered because the potentiometer slider voltage will be higher. Normally the use of the voltage translation circuit gives a minimum slider voltage of 20% of V_{11}.

To sense the open-circuit thermistor condition, an extra comparator is used. This fail-safe comparator will inhibit output pulses if the thermistor input voltage rises above 0.95 V_{11} (see Figure 16).

From Figure 16 the maximum permissible value of R_{NTC} is given by:

$$V_{11} \frac{R_{NTC}}{R_{NTC} + R_1} < 0.95 V_{11}$$

which gives,

$$R_{NTC\,MAX} < 19 R_1.$$

For normal operating conditions, even at very low temperatures, the NTC thermistor resistance will not increase sufficiently to violate the condition specified above for the value of R_1 determined in the previous section.

VALUE OF POTENTIOMETER R_P

It is desirable to keep the current consumption of the temperature sensing bridge as low as possible to avoid excessive power dissipation in the mains dropping circuit components. A reasonable limit to the bridge current is 1mA. The current in the bridge, I_{BR}, is given by:

$$I_{BR} \approx \frac{V_{11}}{R_1 + R_{NTC}} + \frac{V_{11}}{R_P}.$$

The reference voltage V_{11} will never exceed 9V (nominally 8V). The maximum value of I_{BR} will occur when R_{NTC} is a minimum, giving the approximate condition:

$$\frac{V_{11}}{R_1} + \frac{V_{11}}{R_P} < 1mA.$$

Assuming the value of R_1 that was determined in the previous sections, a suitable value of R_P is found to be 22kΩ.

DETERMINATION OF MAXIMUM AVERAGE OUTPUT CURRENT

Before any calculations concerning the required supply current can be made, the maximum average output current of the TDA1023 must be determined. For the worst-case conditions, a 5% tolerance for R_S and R_G and a 10% variation of the mains is assumed. The maximum value of the trigger pulse, $t_{P\,MAX}$, is specified in the published data as 300μs at

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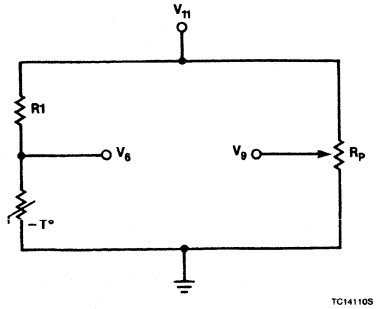
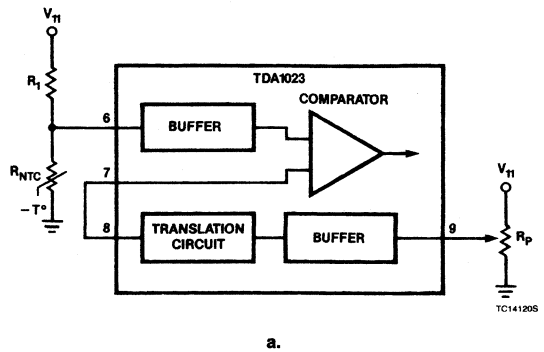
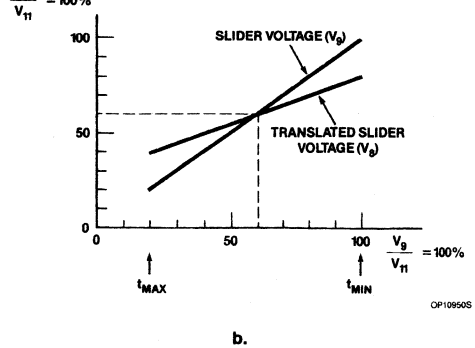


Figure 14. Temperature-Sensing Bridge Circuit



a.



b.

Figure 15. Voltage Translation Circuit (a) and its Transfer Characteristics (b)

I_{10} = 1mA$_{RMS}$ at a frequency of 50Hz; $V_{3\ MAX}$ is specified as 15V.

The maximum average output current, $I_{3(AVG)\ MAX}$, can be determined from the equation:

$$I_{3(AVG)\ MAX} = I_{3\ MAX}\ t_{P\ MAX}\ N$$

where $t_{P\ MAX}$ is expressed in seconds and N is the number of pulses/second.

Under the worst-case conditions, assuming that V_{GTmin} for the triac is zero, the maximum trigger current is:

$$I_{3\ MAX} = \frac{V_{3\ MAX}}{0.95R_G}$$

and the maximum pulse length at 50Hz is:

$$t_{P\ MAX} = 0.3\,\frac{1.05\ R_S}{0.9V_S}\,10^{-6}\text{s}.$$

The final equation for $I_{3(AVG)\ MAX}$ is:

$$I_{3(AVG)\ MAX} = 5.53\,\frac{R_S}{V_S R_G}\,10^{-4}\ \text{A}.$$

Figure 17 shows graphs of $I_{3(AVG)\ MAX}$ as a function of R_G with R_S as a parameter, for four 50Hz supply voltages. When the curves reach the value of 22Ω for R_G, there is no further increase in I_3 if R_G is decreased as the output current is limited to 700mA.

MINIMUM REQUIRED SUPPLY CURRENT I_{16}

The minimum supply current required at Pin 16 of the TDA1023 is the sum of the following currents:

- the maximum average output current
- the current drawn by the external temperature-sensing circuit
- the current required by the integrated circuit.

The maximum average output current has been determined in the previous section. The current drawn by the temperature-sensing circuit must not be greater than 1mA.

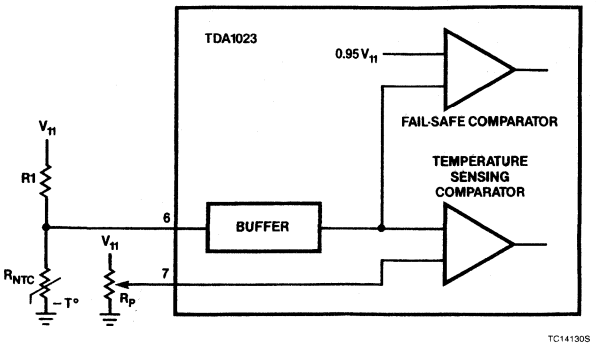
The current consumption of the internal circuits of the TDA1023 depends upon the hysteresis and proportional band settings and whether the circuit is in the ON or OFF state. The circuit draws more current in the ON state to provide the output current pulse. With Pins 4 and 5 open-circuit (hysteresis and proportional band at minimum) the maximum current consumption is 6mA. When Pins 4 and 5 are connected to ground, the current consumption increases by 1.1mA. Figure 18 shows the minimum required supply current as a function of the maximum average output current for maxima and minima of hysteresis and proportional band settings.

DETERMINATION OF THE VALUE OF THE MAINS DROPPING RESISTOR R_D

The value of the mains dropping resistor must be chosen such that the average supply current to Pin 16 of the TDA1023 is at least equal to the required minimum.

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NOTE:
An extra comparator is included to provide fail-safe action should the thermistor input become open-circuit.

Figure 16

Figure 19 shows the supply circuit and the mains voltage waveform. The shaded area denotes a positive voltage across the dropping resistor providing supply current.

During the positive half-cycle of the mains voltage, the current supplied through R_D is given by:

$$I_{16(AVG)} = \frac{1}{2\pi}\int_{a1}^{a2} \frac{\sqrt{2}V_S \sin a - V_{16}}{R_D}\,da.$$

Assuming 10% mains voltage variation, 10% tolerance for R_D and a maximum of 16V at Pin 16, the worst-case condition is given by:

$$I_{16(AVG)\ MIN} = \frac{1}{2\pi}\int_{a1}^{a2} \frac{0.9\sqrt{2}V_S \sin a - 16}{1.1R_D}\,da.$$

in which $a_1 = \pi - a_2 = \arcsin 16/(0.9\sqrt{2}V_S) = \arcsin 12.58/V_S$. Using this equation, graphs of $I_{16(AVG)\ MIN}$ as a function of R_D have been drawn for four supply voltages and are shown in Figure 20.

MINIMUM PERMISSIBLE VALUE FOR R_D

The maximum value of the resistor R_D is defined by the maximum current that can flow into Pin 16, the maximum peak mains voltage, and the minimum voltage at Pin 16. The published data for the TDA1023 specifies the absolute limit for I_{16} as:

$I_{16(AVG)\ MAX}$ = 30mA
and $I_{16M\ MAX}$ = 100mA.

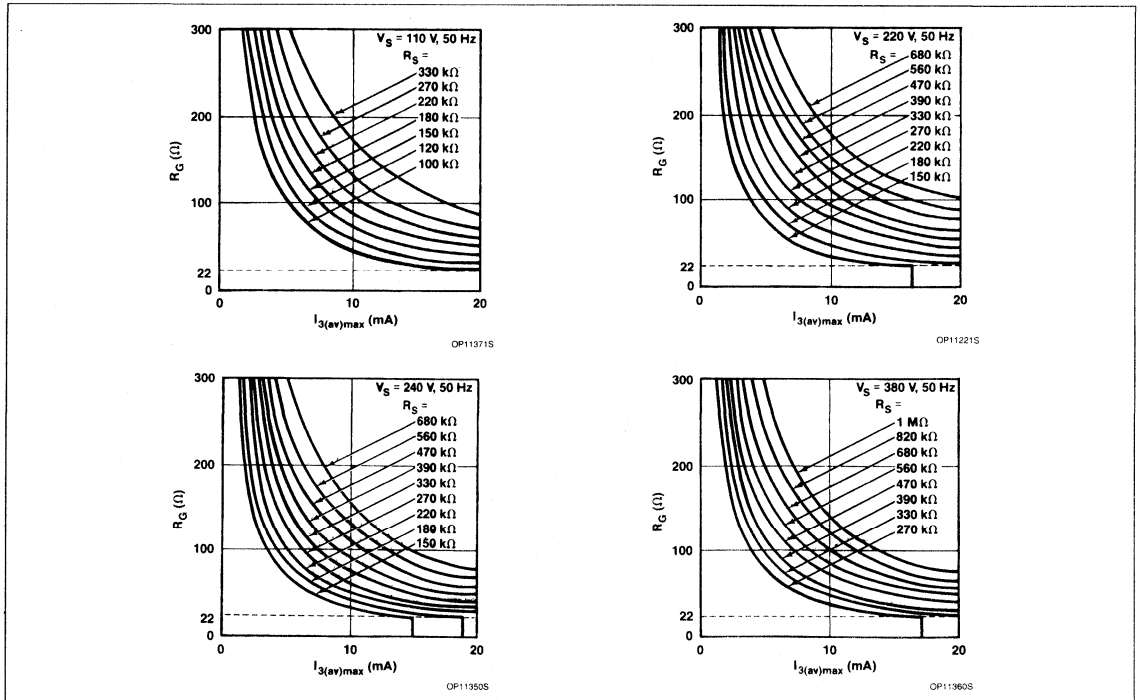


Figure 17. $I_{3(AVG)\ MAX}$ as a Function of Resistor R_G with Synchronization Resistor R_S and Mains Voltage as Parameters

Design of Time-Proportional Temperature Controls Using the TDA1023

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The peak current flowing into Pin 16 is given by:

$$I_{16\ MAX} = \frac{\sqrt{2V_S - V_{16\ MIN}}}{R_D}$$

For a sinusoidal supply voltage, the relationship between the peak and average current into Pin 16 is:

$$\frac{I_{16\ MAX}}{I_{16(AVG)}} = \pi.$$

Because the ratio of the specified limits for the peak and average supply current, 100/30, is greater than π, the minimum value of R_D is defined by $I_{16(AVG)\ MAX}$:

$$R_{D\ MIN} = \frac{\sqrt{2V_{S\ MAX} - V_{16\ MIN}}}{\pi I_{16(AVG)\ MAX}}$$

Assuming a 10% variation in the supply voltage and R_D, the minimum value for the dropping resistor is:

$$0.9R_{D\ MIN} = \frac{1.1V_S\sqrt{2} - 12.5}{0.03\pi}$$

Table 5 shows practical values for $R_{D\ MIN}$ for four common mains supply voltages.

Table 5. Practical Mains Dropping Resistor Values

SUPPLY VOLTAGE V_S (V)	$R_{D\ MIN}$ (Ω)	PRACTICAL VALUE OF $R_{D\ MIN}$ (kΩ)
110	1870	2.0
220	3887	3.9
240	4254	4.3
380	6821	7.5

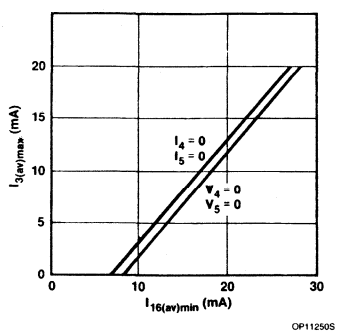


Figure 18. Minimum Required Supply Current as a Function of Average Trigger Current, with Hysteresis and Proportional Band Settings as Parameters

DETERMINATION OF POWER DISSIPATED IN MAINS DROPPING RESISTOR R_D

The general expression for the power dissipated by resistor R_D in Figure 19 is:

$$P = \frac{V^2_{RMS}}{R_D}$$

in which,

$$V^2_{RMS} = \frac{1}{2\pi}\int_{a1}^{a2}(\sqrt{2V_S \sin a - V_{16}})^2 da$$

$$+ \frac{1}{2\pi}\int_{\pi}^{2\pi}(\sqrt{2V_S \sin a})^2\, da.$$

If supply voltage variations of 10% and a tolerance of 10% for R_D are assumed, the maximum power dissipated by R_D is given by:

$$P_{MAX} = \frac{1}{2\pi} \times \frac{1}{0.9R_D}\int_{a1}^{a2}$$

$$(1.1\sqrt{2V_S \sin a - 12.5})^2 da$$

$$+ \frac{1}{2\pi} \times \frac{1}{0.9R_D}\int_{\pi}^{2\pi}(1.1\sqrt{2V_S \sin a})^2\, da.$$

Values of P_{MAX} have been computed for four mains voltages as a function of R_D and the results plotted on the graphs of Figure 20.

The power dissipated in R_D may be considerably reduced by the addition of a series diode as in Figure 23. In this case there is no conduction through R_D during the negative half-cycle of the supply voltage, giving a reduction of more than 50% of the power dissipated in R_D. For worst-case conditions, the power dissipation when a series diode is included in the mains dropping circuit is given by:

$$P_{MAX} = \frac{1}{2\pi} \times \frac{1}{0.9R_D}\int_{a1}^{a2}$$

$$(1.1\sqrt{2V_S \sin a - 12.5})^2 da.$$

Values of P_{MAX} as a function of R_D, with the series diode present, have also been calculated and plotted in Figure 20 to allow easy comparison with the values obtained without the series diode.

USE OF A CAPACITOR TO REDUCE POWER DISSIPATION

It is possible to replace the mains dropping resistor and series diode with a capacitor (Figure 21), and thereby reduce the power dissipation in the voltage reduction components still further. However, for mains voltages below 220V, the power dissipated by the dropping resistor is comparatively small and the use of a capacitor is not considered to be necessary. For mains voltages above 240V, the additional cost of the required high-voltage capacitor is not justified. For these reasons, it is recommended that capacitive voltage reduction is only used with mains supplies of $200V_{RMS}$ or $240V_{RMS}$.

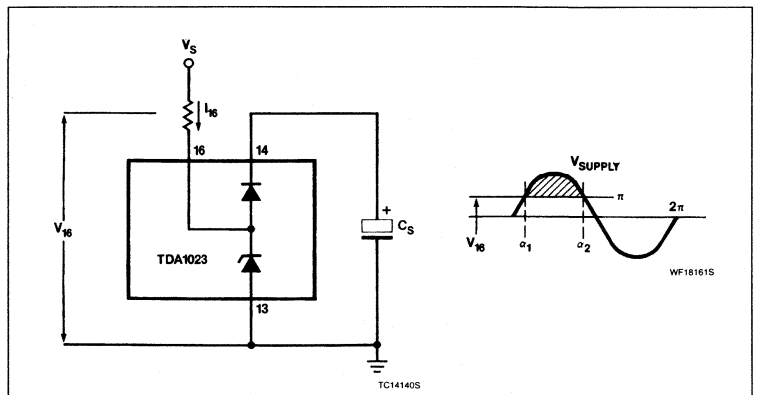


Figure 19. Mains Supply Circuit and Voltage Waveform

Design of Time-Proportional Temperature Controls Using the TDA1023

When selecting a capacitor for mains voltage reduction, the following points must be considered:

- The specified maximum AC voltage for the capacitor must be compatible with the mains supply voltage;
- Inrush current must be limited to less than 2A by a series resistor (R_{SD});
- Mains-borne transients must be suppressed to limit the maximum current to Pin 16 to less than 2A;
- The value of the capacitor must be calculated as a function of the required average current at Pin 16 of the TDA1023, using the mains voltage as a parameter. The maximum permissible value of the capacitor must be calculated to ensure that, under worst-case conditions, the maximum permissible current into Pin 16 is not exceeded.

Suppression of mains-borne transients

A voltage-dependent resistor must be connected across the mains input to limit mains-borne transients to:

$$V_{TRANS} = I_{16SM} \times 0.95R_{SD}$$

where I_{16SM} is the maximum permitted non-repetitive peak current at Pin 16 (2A).

For $R_{SD} = 390\Omega$, this yields a maximum transient voltage of about 740V. For 220V operation, a VDR (catalog number 2322 594 13512) will limit the supply voltage to the required level during current transients of up to about 200A. For 240V operation, a VDR (catalog number 2322 594 13912) will limit the supply voltage to the required level during current transients of up to about 80A.

Limit of Inrush Current

Resistor R_{SD} must also limit the peak value of the inrush current to less than 2A under worst-case operating conditions. With a $240V_{RMS}$ supply, the value of 390Ω will limit the worst-case peak value of the in rush current to:

$$\frac{240 \times 1.1}{0.95 \times 390}\sqrt{2} = 1.01 \text{ A.}$$

Dropping Capacitor Value

The average current supplied to Pin 16 of the TDA1023 via capacitor C_D is given approximately by:

$$I_{16(AVG)} = \frac{1}{\pi}\frac{\sqrt{2V_S - V_{16}}}{\sqrt{\left(R^2_{SD} + \frac{1}{\omega^2 C^2_D}\right)}}$$

When worst-case tolerances are taken into account, the minimum average current through the capacitor is given by:

$$I_{16(AVG)\,MIN} = \frac{1}{\pi}\frac{0.9\sqrt{2V_S - V_{16\,MAX}}}{\sqrt{\left\{1.1R^2_{SD} + \left(\frac{1}{0.9\omega C_D}\right)^2\right\}}}$$

where $V_{16\,MAX} = 16V$ and $R_{SD} = 390\Omega$.

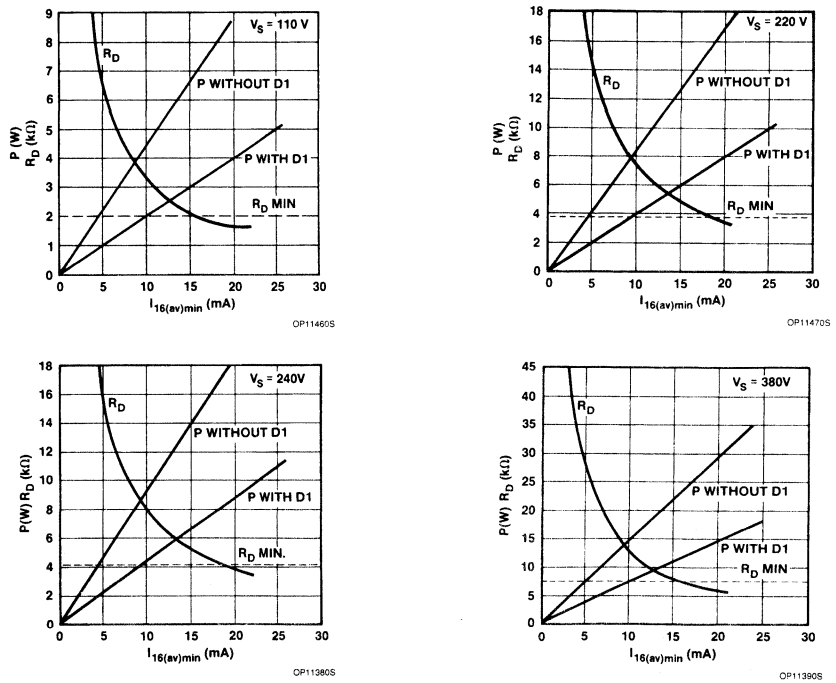


Figure 20. $I_{16(AVG)\,MIN}$ as a Function of Mains Dropping Resistor R_D, and the Power Dissipation in that Resistor, with and without a Series Diode, with Supply Voltage as a Parameter

Design of Time-Proportional Temperature Controls Using the TDA1023

Using this equation, values of C_D have been computed as a function of the minimum required average current into Pin 16 for mains voltages of $220V_{RMS}$ and $240V_{RMS}$. The results have been plotted in the graphs of Figure 21, allowing simple selection of the capacitor value once the minimum required average current is known.

Maximum Permissible Value for the Capacitor C_D

The capacitor C_D must not be chosen so large that the current into Pin 16 of the TDA1023 violates the absolute maximum specified in the published data. Assuming a 10% tolerance for C_D and a 10% variation in the mains voltage, the maximum value of C_D that may be used is given by:

$$1.1C_{D\ MAX} = \frac{\pi I16\ AV_{MAX}}{1.1\omega V_S\sqrt{2}}$$

where the effect of R_{SD} on the calculation of $C_{D\ MAX}$ is so small that it may be ignored. The values of $C_{D\ MAX}$ obtained from this equation are given in Table 6.

Power Dissipated by the Series Resistor R_{SD}

The power dissipated by the 390Ω resistor R_{SD} is given by:

$$P = I^2_{16\ RMS}\ R_{SD}$$

where $I_{16\ RMS}$ may be approximated to:

$$I_{16\ RMS} = \omega C_D V_S.$$

Assuming tolerances of 10% for R_{SD} and C_D and a mains variation of 10%, the worst-case maximum power dissipation in resistor R_{SD} is given by:

$$P_{MAX} = 1.1R_{SD}\,(1.21\omega C_D V_S)^2.$$

The power dissipated in R_{SD} has been plotted as a function of the supply current $I_{16(AVG)}$ and is shown in Figure 21.

SMOOTHING CAPACITOR C_S

The smoothing capacitor is required to provide the supply current to the TDA1023 during the negative half-cycles of the mains voltage waveform. As the TDA1023 possesses an internal voltage stabilization circuit, a high ripple voltage can be tolerated at Pin 14.

The value of the smoothing capacitor is given by:

$$C_S > \frac{It}{V_R}$$

where: I = the maximum average current consumption during the half-cycle. This is never more than 20mA.

t = the time for which the current must be supplied; 10ms for 50Hz mains supplies.

V_R = the maximum acceptable ripple voltage at Pin 14; 1V.

Using these figures, the required value for C_S is 200μF. A practical preferred value is 220μF, 16V.

TRIAC PROTECTION

If the mains dropping circuit consists of capacitor C_D and resistor R_{SD}, a VDR must be included in the circuit as described in the section dealing with the use of a dropping capacitor. This VDR will also protect the triac against current surges in the mains supply.

However, if the mains dropping circuit consists of resistor R_D and diode D_1, the VDR may be connected directly across the triac, giving improved protection due to the series resistance of the heater. Current surges in the supply will not harm the TDA1023 as the dropping resistor will limit the current to a safe level.

EFFECT OF BRIDGE COMPONENT TOLERANCES ON THE ACCURACY OF TEMPERATURE CONTROL

The general expression for the voltage across the thermistor at a temperature of T°C is:

$$V_T = \frac{R_{25}\ \exp\ \{B/(273+T) - B/298\}}{R_1 + R_{25}\ \exp\ \{B/(273+T) - B/298\}} V_{11}.$$

In order to calculate the maximum and minimum values of V_T, tolerances of 10% for R_{25}, 5% for B and 1% for R_1 have been assumed. Table 7 shows the combination of tolerances used to calculate the worst-case values of V_T for temperatures above and below 25°C.

The ratios V_6/V_{11} and V_9/V_{11}, as functions of temperature, are plotted in Figure 22 for nominal and worst-case values of V_T.

If it is assumed that the potentiometer has a linear temperature scale, represented by the broken line in Figure 22, then the maximum deviation of the actual temperature from the selected temperature is found by drawing a horizontal line intersecting the broken line at the given temperature. The intersection points with the worst-case curves then give the maximum temperature deviation. Table 8 shows the possible worst-case temperature errors for a series of temperatures in the range of application.

REDUCTION OF TEMPERATURE ERROR BY SCALE CALIBRATION

The error of a temperature control unit built on the described principles can be considered mainly as an offset, which can be corrected by shifting the temperature scale on the potentiometer. Scale calibration can best be accomplished by maintaining the thermistor at a constant, known temperature and adjusting the potentiometer until trigger pulses just occur. The scale is then fixed so that the control pointer indicates the known temperature of the thermistor. To minimize errors, the calibration should be performed with the thermistor at 20°C (mid-point of the range) and the timing generator inhibited (Pin 12 connected to 0V).

Use of this scale calibration technique results in a temperature control accuracy of +0.2 to −0.1°C over the range 10°C to 30°C as shown in Table 9.

SENSITIVITY OF THE TEMPERATURE-SENSING BRIDGE

To determine the choice of hysteresis and proportional band, the sensitivity of the temperature-sensing network must be known. As the thermistor is not a linear device, the sensitivity will vary according to the temperature. The sensing network is shown in Figure 14. The voltage at Pin 6 is given by:

$$V_6 = \frac{A\ \exp\ (B/T)}{R_1 + A\ \exp\ (B/T)} V_{11}.$$

From which the sensitivity is:

$$\frac{dV_6}{dT} = \frac{-BR_1A\ \exp\ (B/T)}{T^2\{R_1 + A\ \exp\ (B/T)\}^2} V_{11}.$$

Table 10 is based on this equation and shows the effect of sensitivity on the hysteresis and proportional band for the temperature range 10°C to 30°C.

APPLICATION EXAMPLES

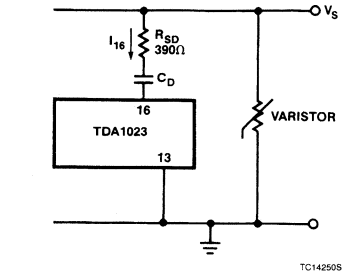
The TDA1023 is intended primarily for room temperature control using electric panel heaters. The controllable heater power range is from 400W to 2000W, although the upper limit may be increased by suitable choice of triacs and/or heatsinks. The TDA1023 may also be used as a time-proportional switch for cooker elements and similar devices, giving 100% control of the power dissipation.

Design of Time-Proportional Temperature Controls Using the TDA1023

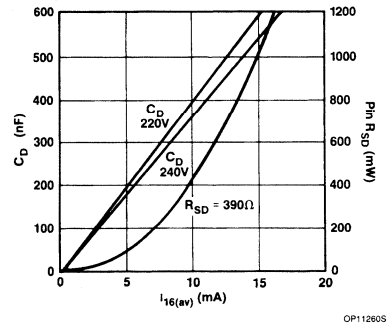
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A Design For Temperature Control Of Domestic Panel Heaters

Figure 23 shows the design for a time-proportional heater control using the TDA1023. Because of the economies that may be gained by the use of smaller or lower power components, two versions are described. Version A, for heaters from 400W to 1200W, uses triac BT138 and a 15μF timing capacitor; version B, for heaters from 1200W to 2000W, uses triac BT139 and a 68μF timing capacitor.



a.



b.

NOTE:
The circuit is shown in (a) and the power dissipated by the dropping resistor and the capacitor value as functions of the current into Pin 16, with the mains supply voltage as a parameter is shown in (b).

Figure 21. Using a Capacitor for Mains Voltage Dropping

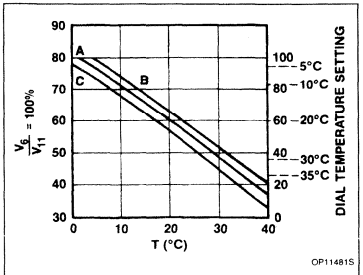
Table 6. Practical Dropping Capacitor Values

SUPPLY VOLTAGE V_S (V)	$C_{D\ MAX}$ (nF)	PRACTICAL VALUE OF $C_{D\ MAX}$ (nF)
220	797	680
240	730	680

Table 7. Tolerance Combinations for Thermistor Voltage Calculations

TEMPERATURE	FOR $V_{T\ MAX}$	FOR $V_{T\ MIN}$
T < 25°C	R_{25} + 10% B + 5% R_1 – 1%	R_{25} – 10% B – 5% R_1 + 1%
t > 25°C	R_{25} + 10% b – 5% R_1 – 1%	R_{25} – 10% b+ 5% R_1 + 1%

Design of Time-Proportional Temperature Controls Using the TDA1023



NOTES:
A = Nominal Curve, B = Maximum Curve,
C = Minimum Curve.
The broken line represents the ideal linear function.

Figure 22. Nominal and Worst-Case Values of V_6 as a Function of Temperature

Table 8. Maximum Deviation From Selected Temperature

SELECTED TEMP. (°C)	DEVIATION	
	Upper (°C)	Lower (°C)
5	+2.3	−3.6
10	+2.6	−2.8
14	+2.6	−2.7
20	+2.4	−2.7
26	+2.3	−2.6
30	+2.6	−2.6
35	+3.0	−3.0

Table 11 gives the necessary component values for each of these versions for use with mains supplies of 220V, 50Hz. All figures in Table 11 have been calculated using the equations given in the previous sections, allowing for worst-case conditions. Because each version is designed to control a range of heater powers, it follows that each may not be ideal for all load powers in the range. If the ideal circuit is required, then this must be calculated as shown in the earlier sections.

The capacitor C_1 has been included in the circuit of Figure 23 to minimize the effects of any interference picked up in the sensor lines. This is only necessary when the sensor is remote from the control circuit. The built-in hysteresis and proportional band have been designed to provide optimum performance for panel heaters, so Pins 4 and 5 are not connected.

Design Of Temperature Control For 220V, 50Hz Operation With 2kW Load

For a load power of 2kW the triac BT139 must be used. The relevant data for this triac (also applicable to move the BT138) are given in Table 9.

Table 9. Maximum Deviation From Selected Temperature Scale Calibrated at 20°C

SELECTED TEMP. (°C)	DEVIATION	
	Upper (°C)	Lower (°C)
5	−0.1	−0.9
10	+0.2	−0.1
14	+0.1	0
20	0	0
26	−0.1	+0.1
30	+0.2	+0.1
35	+0.6	+0.3

- I_{GT} to trigger, all devices = 72mA;
- V_{GT} to trigger all devices = 1.6V;
- I_L = 60mA

} at 0°C

The circuit used will be that of Figure 23. Pins 4 and 5 are not connected as the built-in hysteresis and proportional band will give the optimum performance.

Value of R_S

The required trigger pulse width can be found from Figure 6 as a function of the load power, latch current, and supply voltage (2000W, 60mA, and 220V, 50Hz, respectively): $t_{P\ MIN} = 64\mu s$.

From Figure 6, the value of R_S to provide a trigger pulse of the required duration is then: $R_S = 135k\Omega$. The next preferred value above this is 150kΩ, providing a $t_{P\ MIN}$ of approximately 70μs.

Value of R_G

The maximum value of R_G that may be used is determined by the minimum voltage and current to reliably trigger all samples of the triac. In Figure 8 it can be seen that the operation point of 1.6V and 72mA lies between the load lines for 100Ω and 120Ω. The lesser of these two values, $R_G = 100\Omega$, must be chosen. By calculation, it is found that this resistor may be 110Ω.

Value of C_T

For a load of 2kW, the repetition period must be at least 24 seconds (from Table 1). From Table 3 the minimum preferred value of C_T to provide this period is 68μF. However, due to the different performance under AC and DC conditions, the actual capacitor used should be a 47μF, 25V, catalog number 2222 016 90129 (see Table 2).

Value of R_1 and R_P

For control over the range 5°C to 35°C and thermistor characteristics of B = 4200 and $R_{25} = 22k\Omega$, the value of R_1 has previously been shown to be 18.7kΩ ±1%. A suitable value for R_P is 22kΩ.

Value of R_D

First, the maximum average output current must be found. Figure 17 gives $I_{3(AVG)\ MAX}$ as a function of the values of resistors R_S and R_G. For this circuit $I_{3(AVG)\ MAX} = 3.5mA$.

Once the maximum average output current is known, the minimum required supply current can be found from Figure 18. With minimum hysteresis and proportional band, the average value of the supply current is 10.5mA.

Using this value of $I_{16(AVG)}$, the required value of R_D can be found from Figure 20: $R_D = 6.8k\Omega$. The power dissipation in the resistor, when diode D_1 is present in the circuit, is then 4.3W.

Final component list

Table 12 gives a summary of the component values for the 2kW, 220V, 50Hz temperature controller.

Time-Proportional Power Control

The TDA1023 may be used to provide proportional control of devices such as electric cooker elements. The temperature-sensing bridge is replaced by a potentiometer, the power in the load being proportional to the potentiometer setting (see Figure 24).

The inputs to the comparator are:

- Pin 7: the triangular waveform at the timing capacitor
- Pin 6: the potentiometer voltage.

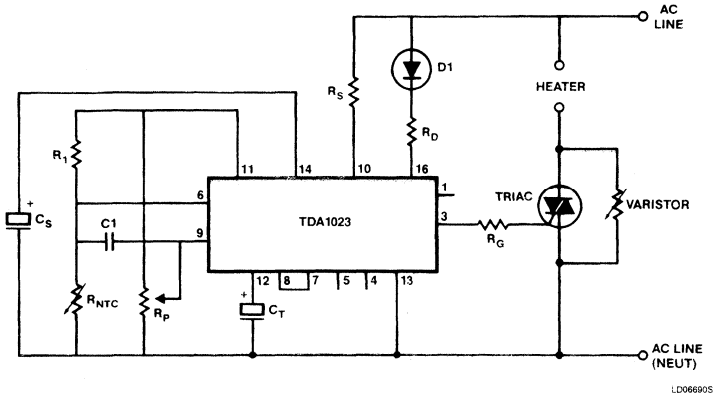
Proportional power control is thus obtained while the potentiometer voltage lies between the upper and lower limits of the triangular waveform. As the timing capacitor is charged and discharged by current sources, the voltage across it will never reach zero, so that load power will be zero before the potentiometer reaches its minimum setting. Similarly, maximum load power is reached before the maximum setting of the potentiometer. This effect can be reduced by the addition of resistors R_1 and R_2. To ensure that 0% and 100% load power can be selected by the potentiometer setting, the values of R_1 and R_2 should each be limited to 10% of the value of R_P.

All the circuit components are calculated in the same way as for the temperature controller, including the timing capacitor C_T. An example circuit, with components suitable for the control of loads from 1 to 2kW from 220V, 50Hz supplies, is shown in Figure 25. Pins 9 and 11 are shorted together as the voltage translation circuit is not used.

Design of Time-Proportional Temperature Controls Using the TDA1023

Table 10. Sensitivity of Temperature-Sensing Network NTC Thermistor: Catalog Number 2322 642 12223 Resistor: 18.7kΩ

TEMP (°C)	SENS (mV/°C)	HYSTERESIS (°C/20mV)	PROP BAND (°C/80mV)
10	86	0.23	0.93
15	91	0.22	0.88
20	94	0.21	0.85
25	94	0.21	0.85
30	91	0.22	0.88



NOTE:
Refer to Table 11 for component values for use with 220V, 50Hz supplies.

Figure 23. Circuit Diagram of Time-Proportional Heater Control Using the TDA1023

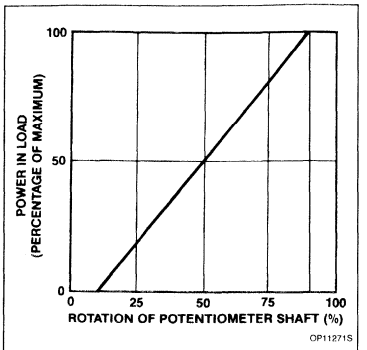


Figure 24. Typical Load Power as a Function of Potentiometer Shaft Rotation for a Time-Proportional Power Regulator

Table 11. Temperature Controller Component Values Mains supply: 220V, 50Hz
Version A: Heater Powers 400 – 1200W Version B: Heater Powers 1200 – 2000W

COMPONENT	VERSION A	VERSION B	REMARKS
Triac	BT138	BT139	
VDR	350V, 1mA	350V, 1mA	Cat. No. 2322 594 13512 (Varistor)
D_1	BYX10	BYX10	
R_1	18.7kΩ	18.7kΩ	1% tolerance
R_{NTC}	R_{25} = 22kΩ B = 4200k	R_{25} = 22kΩ B = 4200k	Cat. No. 2322 642 12223 (Thermistor)
R_P	22kΩ	22kΩ	Potentiometer
R_D	4.3kΩ	6.2kΩ	Power in R_D: A = 6.8W B = 4.8W
R_G	110Ω	110Ω	
R_S	430kΩ	180kΩ	
C_1	47nF	47nF	
C_S	220μF, 16V	220μF, 16V	
C_T	15μF (DC)	68μF (DC)	See Table 3
C_D*	680nF	470nF	
R_{SD}*	390Ω	390Ω	Power in R_{SD}: A = 1.2W B = 0.6W

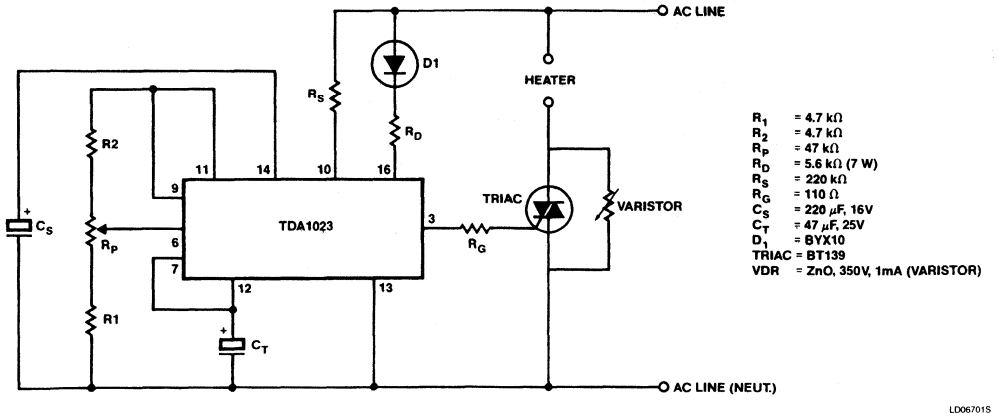
NOTE:
*C_D and R_{SD} only required if used in place of D_1 and R_D.

Table 12. Temperature Controller Component Value
Mains Supply: 220V, 50Hz Heater Power: 2000W

COMPONENT	TYPE/VALUE	REMARKS
Triac	BT139	
VDR	350V, 1mA	Cat. No. 2322 594 13912 (Varistor)
D_1	BYX10	
R_1	18.7kΩ	1% tolerance
R_{NTC}	R_{25} = 22kΩ B = 4200k	Cat. No. 2322 642 12223 (Thermistor)
R_P	22kΩ	Potentiometer
R_D	6.8kΩ	Power in R_D = 4.3W
R_G	110Ω	
R_S	150kΩ	
C_1	47nF	
C_S	220μF, 16V	
C_T	47μF	Cat No. 2222 016 90129

Design of Time-Proportional Temperature Controls Using the TDA1023

AN1291



R_1 = 4.7 kΩ
R_2 = 4.7 kΩ
R_P = 47 kΩ
R_D = 5.6 kΩ (7 W)
R_S = 220 kΩ
R_G = 110 Ω
C_S = 220 μF, 16V
C_T = 47 μF, 25V
D_1 = BYX10
TRIAC = BT139
VDR = ZnO, 350V, 1mA (VARISTOR)

NOTE:
Component values are for a load power of 2kW from 220V, 50Hz supplies.

Figure 25. Circuit Using the TDA1023 for Time-Proportional Power Regulation

Design of Time-Proportional Temperature Controls Using the TDA1023

AN1291

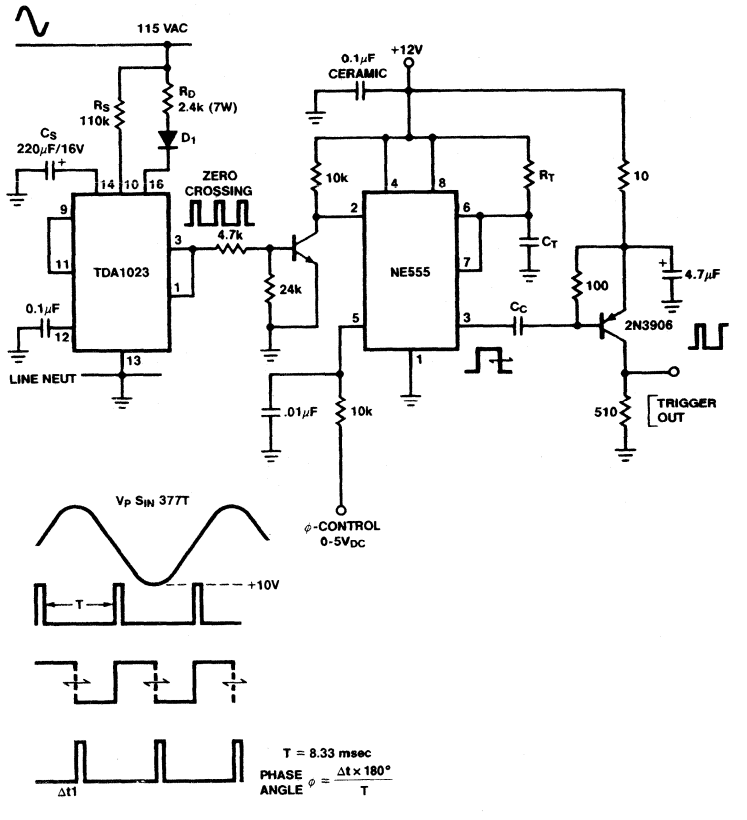


Figure 26. Adjustable Phase SCR/Triac Trigger

NOTE:
Previously published as Technical Information 025, March 1, 1977, ELCOMA, the Netherlands.

Display drivers

		page
NE587	LED decoder/driver	785
NE589	LED decoder/driver	795
NE594	vacuum fluorescent display driver	804
SA594	vacuum fluorescent display driver	804
AN112	LED decoder/drivers: using the NE587 and NE589	809

NE587
LED Decoder/Driver

Product Specification

DESCRIPTION

The NE587 is a latch/decoder/driver for 7-segment common anode LED displays. The NE587 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

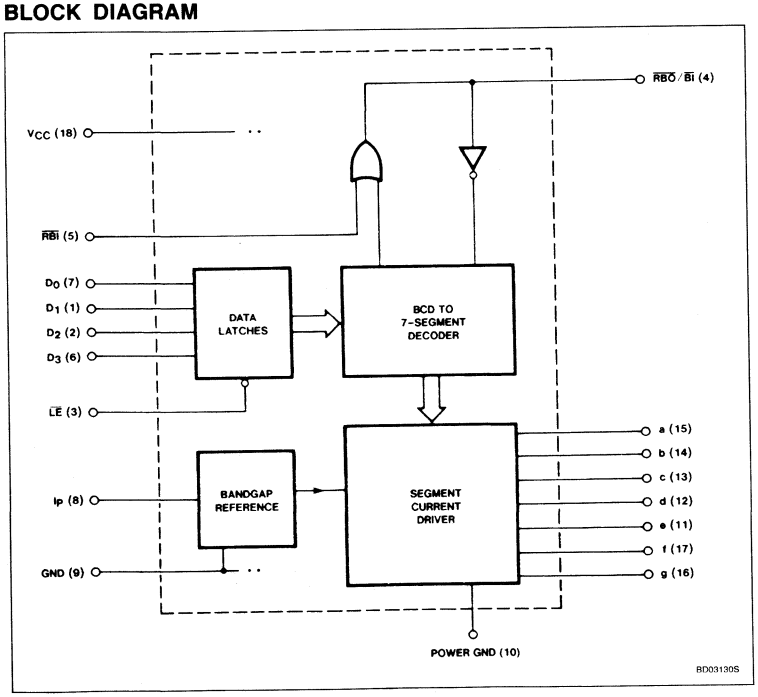
FEATURES

- **Latched BCD inputs**
- **Low loading bus-compatible inputs**
- **Ripple-blanking on leading- and/or trailing-edge zeros**

APPLICATIONS

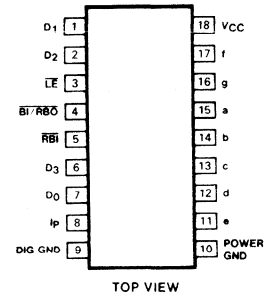
- **Digital panel motors**
- **Measuring instruments**
- **Test equipment**
- **Digital clocks**
- **Digital bus monitoring**

BLOCK DIAGRAM



PIN CONFIGURATIONS

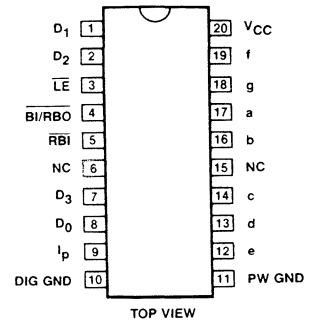
F, N Packages



TOP VIEW

CD09990S

D Package[1]



TOP VIEW

CD10000S

NOTE:
1. SOL and non-standard pinout.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL	0 to +70°C	NE587D[1]
18-Pin Plastic DIP	0 to +70°C	NE587N
18-Pin Cerdip	0 to +70°C	NE587F

NOTE:
1. SOL and non-standard pinout

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage ($D_0 - D_3$, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a − g, RBO)	−0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Soldering temperature (10sec max)	300	°C

NOTE:
1. Derate power dissipation as indicated
   N package — 95°C/W above 55°C
   F package — 100°C/W above 50°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C < T_A < 70°C. Typical values are at V_{CC} = 5V, T_A = 25°C, R_P = 1kΩ (±1%), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All inputs except $\overline{BI}$ $\overline{BI}$	2.0 2.0		15 5.5	V
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	I_{IN} = −12mA, T_A = 25°C			−1.5	V
I_{IH}	Input high current	Inputs $D_0 - D_3$, $\overline{LE}$, $\overline{RBI}$ V_{IN} = 2.4V V_{IN} = 15V Input $\overline{BI}$ (Pin 4) $\overline{RBI}$ = H V_{IN} = V_{CC} = 5.25V		1.0 15 10	10 15 100	μA μA
I_{IL}	Input low current	V_{IN} = 0.4V, Inputs $D_0 - D_3$ $\overline{LE}$, $\overline{RBI}$		−5 −200		μA
		Input $\overline{BI}$ V_{CC} = 5.25V $\overline{RBI}$ = H, V_{IN} = 0.4V		−0.7		mA
V_{OL}	Output low voltage	Output $\overline{RBO}$ I_{OUT} = 3.0mA		0.2	0.5	V
V_{OH}	Output high voltage	Output $\overline{RBO}$ I_{OUT} = −50μA $\overline{RBI}$ = H	3.5	4.5		V
I_{OUT}	Output segment "ON" current	Outputs "a" through "g" V_{OUT} = 2.0V	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment V_{OUT} = 2.0V	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current	Outputs "a" through "g" V_{OUT} = 5.0V		20	250	μA
I_{CCO}	Supply current	V_{CC} = 5.25V All outputs "ON" V_{OUT} > 1V		33	55	mA
I_{CCI}	Supply current	V_{CC} = 5.25V All outputs blanked		50	70	mA

NOTE:
NE587 Programming:
The NE587 output current can be programmed, provided a program resistor, R_P, be connected between I_P (Pin 8) and Ground (Pin 9). The voltage at I_P (Pin 8) is constant (≈1.3V). Thus, a current through R_P is $I_P \approx \frac{1.3V}{R_P}$, as shown in Figure 5. $\frac{I_O}{I_P}$ is 20 in the 15 to 50mA output current range.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C, R_L = 130Ω, C_L = 30pF including probe capacity.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{DAV}	Propagation delay Figure 2	From data to output		135		ns
t_{DAV}	Propagation delay Figure 3	From $\overline{LE}$ to output		135		ns
t_W	Latch enable pulse width Figure 4		30			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	20			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

NOTE:
$t_{DAV} = ½ (t_{HL} + t_{LH})$

TRUTH TABLE

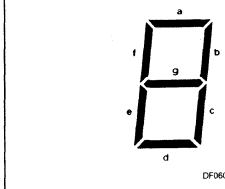
BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
–	H	*	X	X	X	X	STABLE							**	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	–
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	Blank
**BI	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	Blank

NOTES:
H = HIGH voltage level, output is "OFF"
L = LOW voltage level, output is "ON"
X = Don't care
* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
** $\overline{RBO}/\overline{BI}$ used as an input overrides all other input conditions.

NE587 PROGRAMMING

NE587 output current can be programmed by using a programming resistor, R_P, connected between R_P (Pin 8) and GND (Pin 9). The voltage at R_P (Pin 8) is constant ($\approx$ 1.40V). A partial schematic of the voltage reference used in the NE587 is shown in Figure 1.

Output current to program current ratio, I_O/I_P, is 20 in the 15mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high-impedance source such as an I_{OUT} DAC used to control display brightness.



Segment Identification

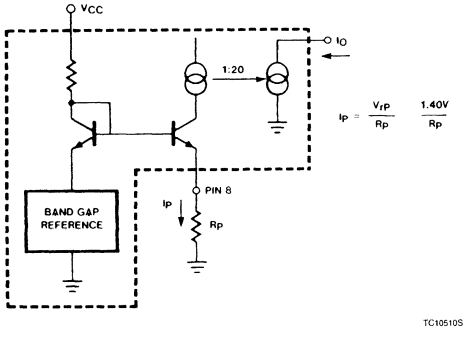


Figure 1

TIMING DIAGRAMS

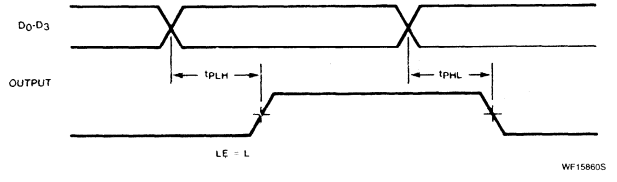


Figure 2. Propagation Delay, Data-to-Output

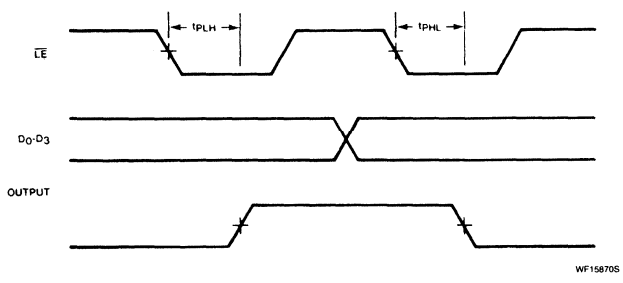


Figure 3. Propagation Delay, Latch Enable-to-Output

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably, somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation; but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large-size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant-current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible, consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to Figure 6, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC}	Supply voltage to driver
V_S	Supply voltage to display
I_{CC}	Quiescent supply current of driver
I_{SEG}	LED segment current
V_F	LED segment forward voltage at I_{SEG}
K_{DC}	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

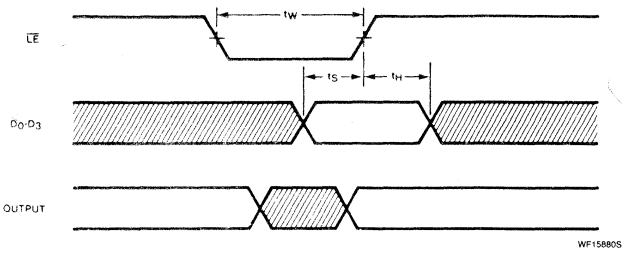


Figure 4

These voltages are all for single-diode displays. Some early red displays had 2 series LEDs per segment; hence the forward voltage drop was around 3.5V.

Thus, a maximum power dissipation calculation when all segments are on, is:

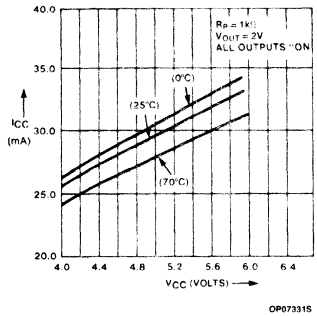
$P_D = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{SEG} \times K_{DC}mW$

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$

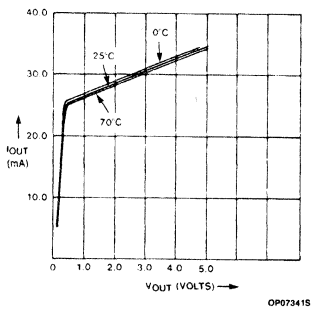
$P_{D\ MAX} = 5.25 \times 50 + 3.25 \times 7 \times 30mW$
$= 945mW$

TYPICAL PERFORMANCE CURVES

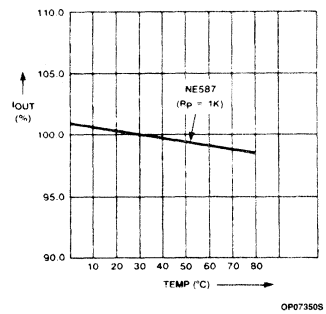
Supply Current vs Supply Voltage



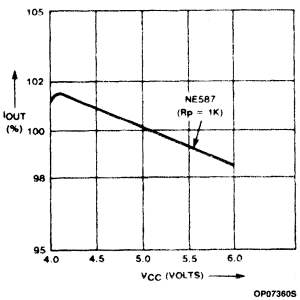
Output Current vs Output Voltage $R_P = 1k\Omega$



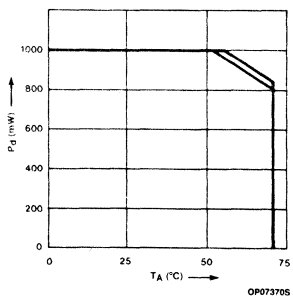
Normalized Output Current vs Temperature $V_{CC} = 5.0V$



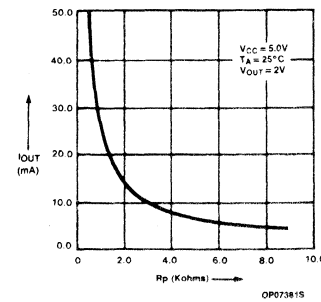
Normalized Output Current vs Supply Voltage $V_O = 2V$, $T_A = 25°C$

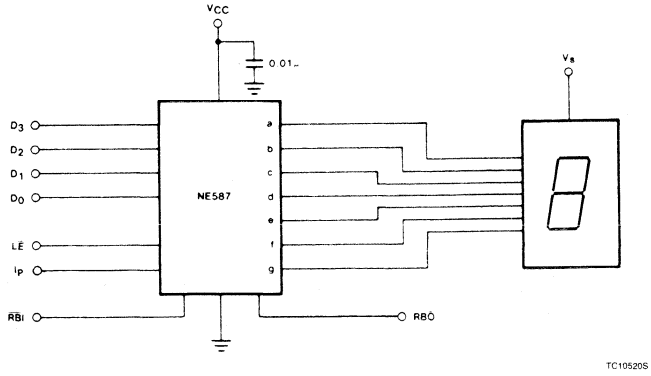


Maximum Power Dissipation vs Temperature



Output Current vs Program Resistor





NOTE:
Decoupling capacitor on V_{CC} should be 0.01µF ceramic.

Figure 6. Driving a Single Digit

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{D\ MAX} = 5.0 \times 30 + 3.00 \times 5 \times 25mW$$
$$= 525mW$$

Operating temperature range limitations can be deduced from the power dissipation graph. (See Typical Performance Characteristics.)

However, a major portion of this power dissipation ($P_{D\ MAX}$) is because the current source output is operating with 3.25V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst-case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{SEG}} \simeq 10\Omega\ (\tfrac{1}{2}\,W\ rating)$$

assuming worst case I_{SEG} of 30mA.

Hence now

$$P_{D\ MAX} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{SEG}) \times 7 \times I_{SEG} \times K_{DC}$$
$$\simeq 5.25 \times 50 + 1.25 \times 7 \times 30mW$$
$$\simeq 525mW$$

and

$$P_{D\ av} = 5.0 \times 30 + 1.25 \times 5 \times 25$$
$$= 306\ mW.$$

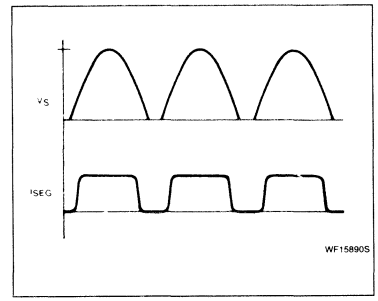
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_d,\ V_D \simeq 0.8V$$

Where n is the number of diodes used, power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in Figure 9. For example a Darlington PNP or NPN emitter-follower may be preferable. Figure 8 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact, a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about $3 - 4.5V_{RMS}$ works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
$V_S = 4.9V$ peak
$V_F = 2.0V$

The duty cycle is approximately 60%.

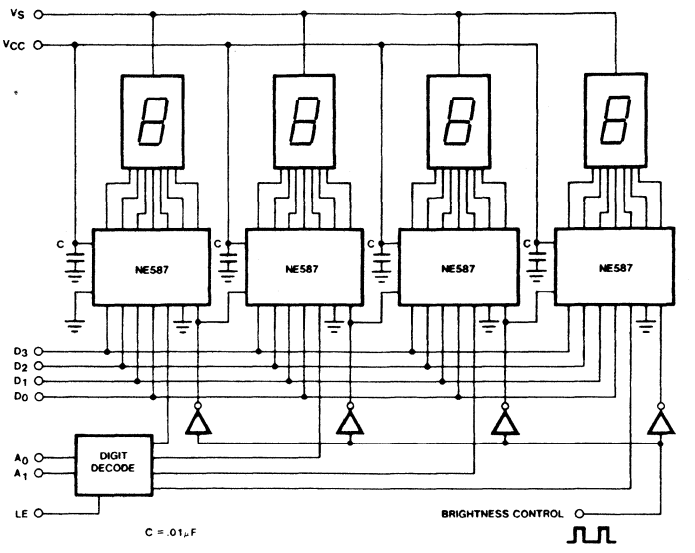


Figure 7. 4-Digit Display with Brightness Control and Leading-Edge Ripple Blanking

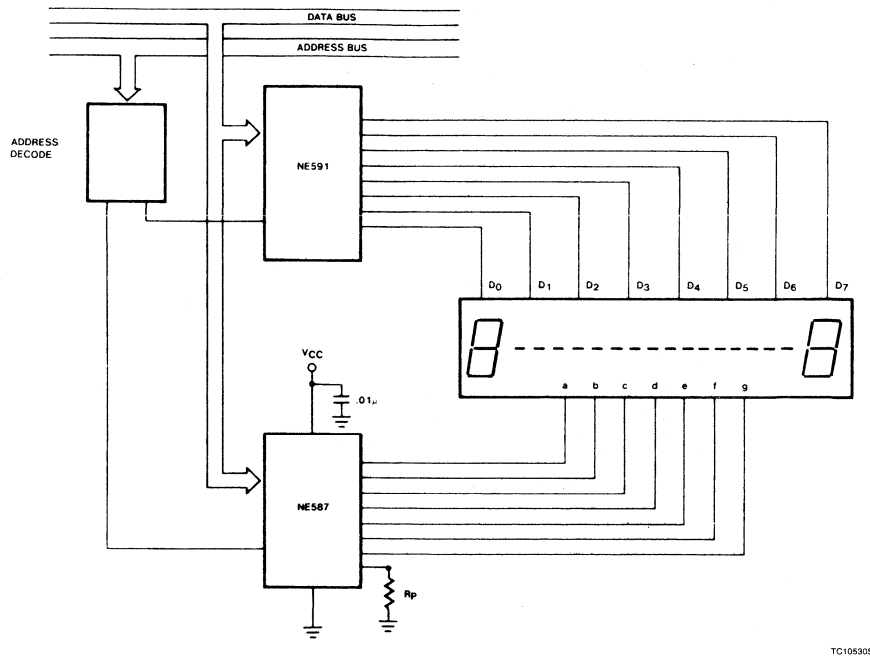


Figure 8. Interfacing 8-Digit LED Display with μP Bus

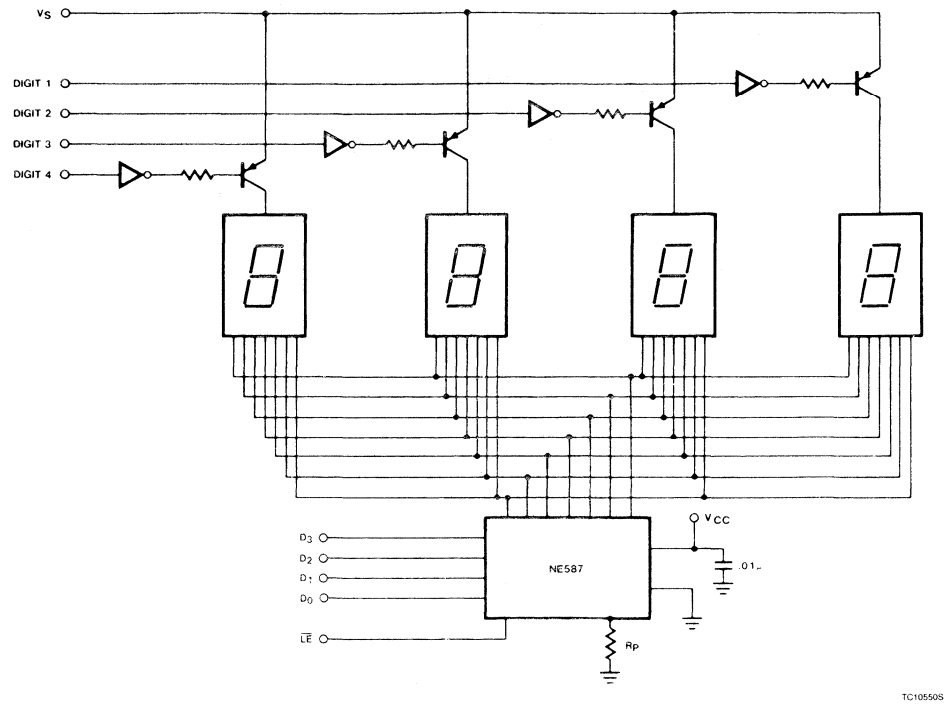


Figure 9. 4-Digit Multiplexed LED Display

NE589
LED Decoder/Driver

Product Specification

DESCRIPTION

The NE589 is a latch/decoder/driver for 7-segment common cathode LED displays. The NE589 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

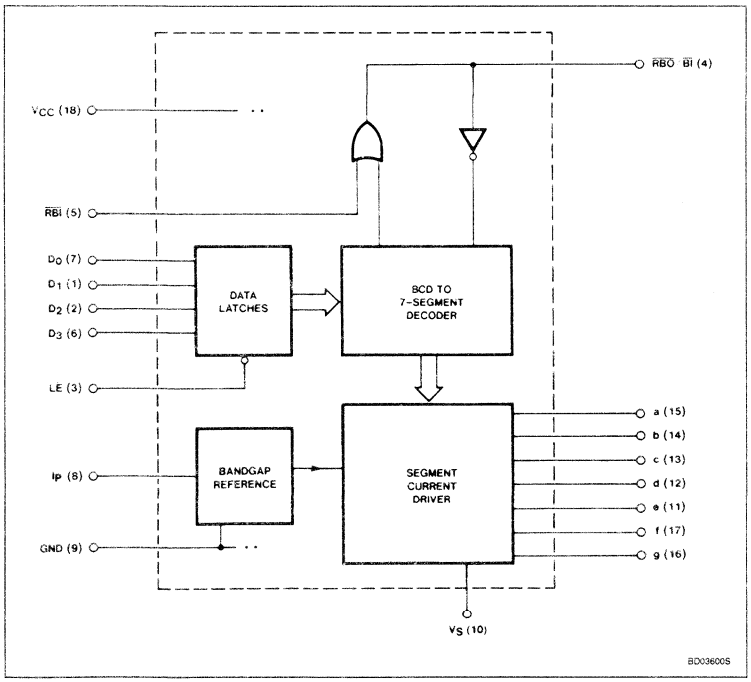
FEATURES

- **Latched BCD inputs**
- **Low loading bus-compatible inputs**
- **Ripple-blanking on leading and/or trailing-edge zeroes**

APPLICATIONS

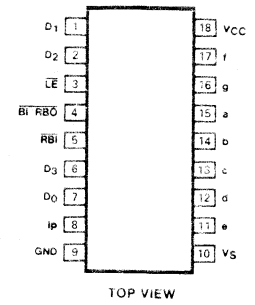
- **Digital panel meters**
- **Measuring instruments**
- **Test equipment**
- **Digital clocks**
- **Digital bus monitoring**

BLOCK DIAGRAM

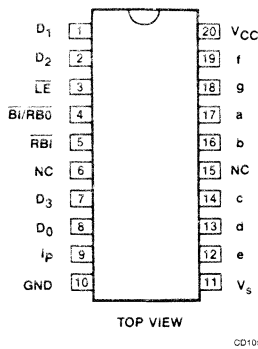


PIN CONFIGURATIONS

N Package



D Package[1]



NOTE:
1. SOL and non-standard pinout.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL, non-standard	0 to +70°C	NE589D
18-Pin Plastic DIP	0 to +70°C	NE589N

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}, V_S	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage ($D_0 - D_3$, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a − g, RBO)	−0.5 to +7	V
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] N package D package	 1690 1390	 mW mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C

NOTES:
1. Derate above 25°C, at the following rates:
   N package at 13.5mW/°C
   D package at 11.1mW/°C

DC ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 to 5.25V, 0°C < T_A < 70°C. Typical values are at V_{CC} = V_S = 5V, T_A = 25°C, R_P = 7kΩ (± 1%), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}, V_S	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All inputs except $\overline{BI}$ $\overline{BI}$	2.0 2.0		15 5.5	V
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	I_{IN} = −12mA, T_A = 25°C			−1.5	V
I_{IH}	Input high current	Inputs $D_0 - D_3$, $\overline{LE}$, $\overline{RBI}$ V_{IN} = 2.4V V_{IN} = 15V		0.1 10	10 15	μA μA
I_{IH}	Input high current	Input $\overline{BI}$ (Pin 4) $\overline{RBI}$ = H V_{IN} = V_{CC} = 5.25V		10		μA
I_{IL}	Input low current	V_{IN} = 0.4V, Inputs $D_0 - D_3$ $\overline{LE}$, $\overline{RBI}$		−5 −200		μA
I_{IL}	Input low current	Input $\overline{BI}$ V_{CC} = 5.25V $\overline{RBI}$ = H, V_{IN} = 0.4V		−0.7		mA
V_{OL}	Output low voltage	Output $\overline{RBO}$ I_{OUT} = 3.0mA		0.2	0.5	V
V_{OH}	Output high voltage	Output $\overline{RBO}$ I_{OUT} = −50μA $\overline{RBI}$ = H	3.5	4.5		V
I_{OUT}	Output segment "ON" current	Outputs "a" through "g" V_{OUT} = 2.0V	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment V_{OUT} = 2.0V	0.90	1.00	1.10	mA
I_{OFF}	Output segment "OFF" current	Outputs "a" through "g"		20	250	μA
I_{CCO}	Supply current	V_{CC} = 5.25V All outputs "ON" V_{OUT} > 1V		25	55	mA
I_{CCI}	Supply current	V_{CC} = 5.25V All outputs blanked		30	65	mA

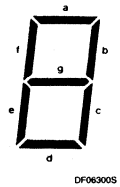
AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_S = 5V$, $T_A = 25°C$, $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation delay Figure 2	From data to output		135		ns
t_{PLH}, t_{PHL}	Propagation delay Figure 3	From $\overline{LE}$ to output		135		ns
t_W	Latch enable pulse width Figure 4		85			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	75			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
–	H	*	X	X	X	X	STABLE								STABLE
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	L	L	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	H	L	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	H	L	H	H	H	9
10	L	X	H	L	H	L	H	H	H	L	H	H	H	H	a
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	b
12	L	X	H	H	L	L	H	L	L	H	H	H	L	H	c
13	L	X	H	H	L	H	L	H	H	H	H	L	H	H	d
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	e
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	f
**BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L**	blank

NOTES:
H = HIGH voltage level, output is "ON".
L = LOW voltage level, output is "OFF".
X = Don't care.
* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
** $\overline{RBO}/\overline{BI}$ used as an input overrides all other input conditions.



DF06300S

Segment Identification

NE589 PROGRAMMING

Output current can be programmed by using a programming resistor, R_P, connected between r_P (Pin 8) and GND (Pin 9). The voltage at r_P (Pin 8) is constant (≈1.3V). A partial schematic of the voltage reference used in the NE589 is shown in Figure 1.

Output current to program current ratio, I_O/I_P, is 120 in the 10mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high-impedance source such as an I_{OUT} DAC used to control display brightness.

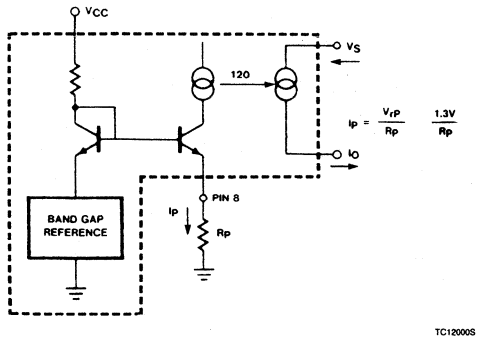


Figure 1

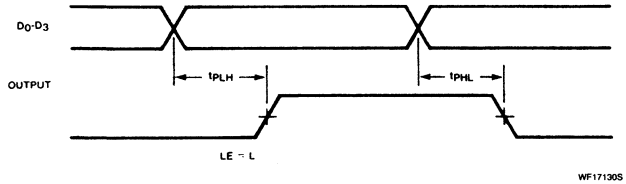


Figure 2. Propagation Delay, Data-to-Output

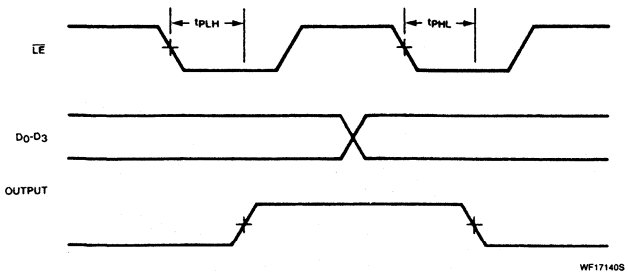


Figure 3. Propagation Delay, Latch Enable-to-Output

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant-current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to Figure 5, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC} Supply voltage to driver
V_S Supply voltage to display
I_{CC} Quiescent supply current of driver
I_{SEG} LED segment current
V_F LED segment forward voltage at I_{SEG}
K_{DC} % Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red 1.6 to 2.0V
Orange 2.0 to 2.5V
Yellow 2.2 to 3.5V
Green 2.5 to 3.5V

TIMING DIAGRAMS (Continued)

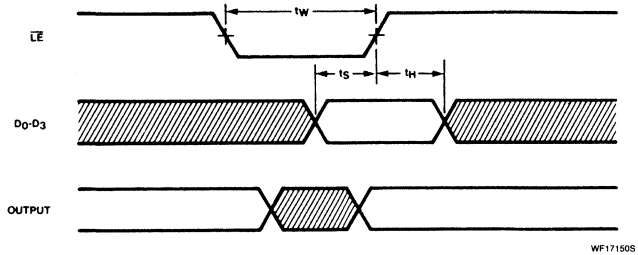


Figure 4. Latch Enable Pulse Width, Setup and Hold Times

These voltages are all for single diode displays. Some early red displays had 2 series LEDs per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation, when all segments are on, is:

$$P_D = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{SEG} \times K_{DC}mW$$

Assuming $V_S = V_{CC} = 5.25V$

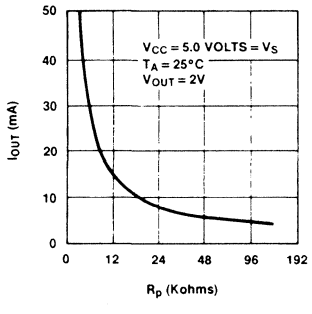
$V_F = 2.0V$

$K_{DC} = 100\%$

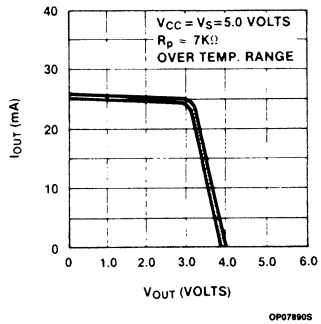
$$P_D \text{ max} = 5.25 \times 50 + 3.25 \times 7 \times 30mW = 945mW$$

TYPICAL PERFORMANCE CURVES

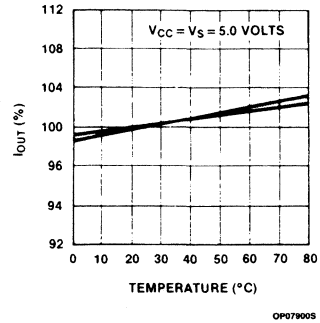
Output Current vs Program Resistor



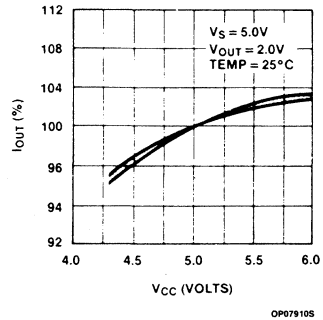
Output Current vs Output Voltage



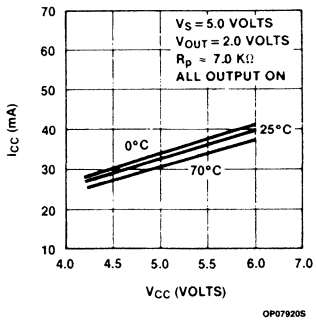
Normalized Output Current vs Temperature



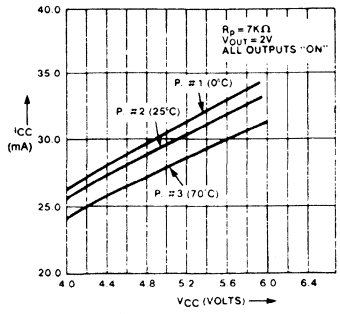
Normalized Output Current vs Supply Voltage

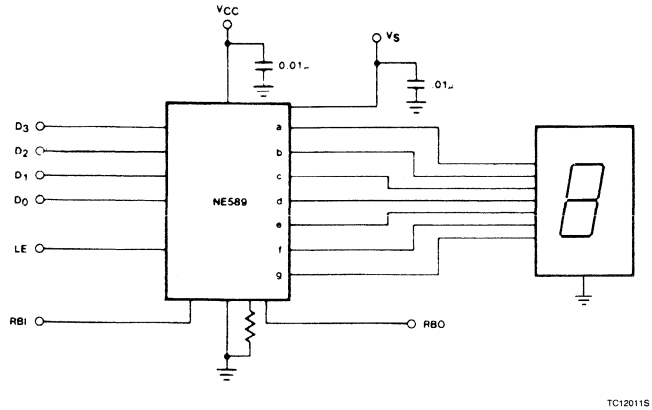


Supply Current vs Supply Voltage



Supply Current vs Supply Voltage





NOTE:
Decoupling capacitor on V_{CC} should be 0.0μF ceramic.

Figure 5. Driving a Single Digit

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{DAV} = 5.0 \times 30 + 3.00 \times 5 \times 25mW$$
$$= 525mW$$

A major portion of this power dissipation (P_D max) is because the current source output is operating with 3.25V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst-case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{SEG}} \simeq 10\Omega \ (\tfrac{1}{2}W \text{ rating})$$

assuming worst-case I_{SEG} of 30mA

Hence now

$$P_D \text{ max} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{SEG}) \times 7 \times XI_{SEG} \times K_{DC}$$
$$= 5.25 \times 50 + 1.25 \times 7 \times 30mW$$
$$= 525mW$$

and

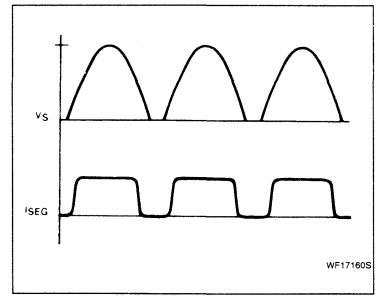
$$P_{DAV} = 5.0 \times 30 + 1.25 \times 5 \times 25$$
$$= 306mW$$

If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to $V_S - V_F - nV_D$, $V_D \simeq 0.8V$

Where "n" is the number of diodes used, power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in Figure 8. For example a Darlington PNP or NPN emitter-follower may be preferable. Figure 7 shows the NE590 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated A transformer voltage of about $3 - 4.5V_{RMS}$ works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver. With

$$V_S = 4.9V_{pk}$$
$$V_F = 2.0V$$

The duty cycle is approximately 60%.

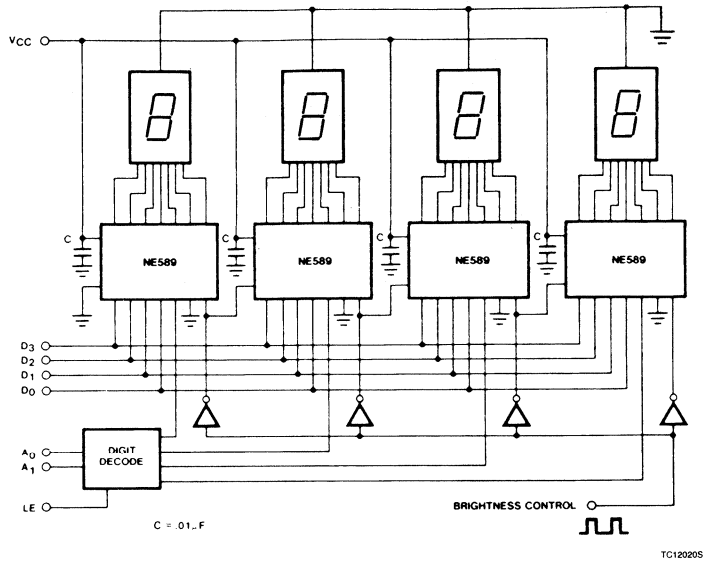


Figure 6. 4-Digit Display With Brightness Control and Leading Edge Ripple Blanking

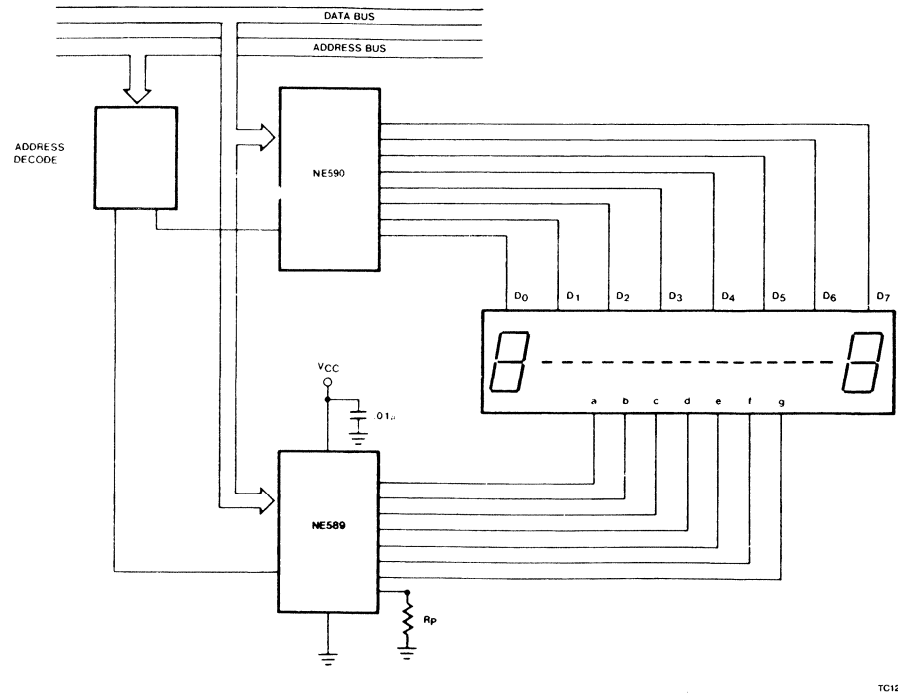


Figure 7. Interfacing 8-Digit LED Display With μP Bus

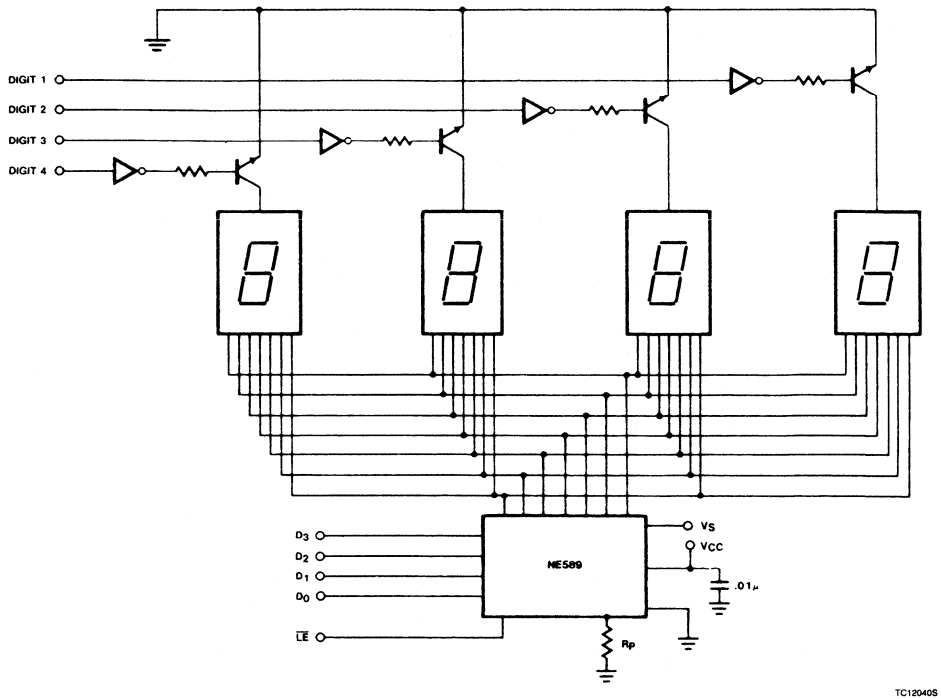


Figure 8. 4-Digit Multiplexed LED Display

NE/SA594
Vacuum Fluorescent Display Driver

Product Specification

DESCRIPTION

The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network, and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

FEATURES

- **Digit and/or segment drivers**
- **Active output pull-down circuitry**
- **High output breakdown voltage**
- **Low supply voltage**
- **Input compatible with all logic outputs**

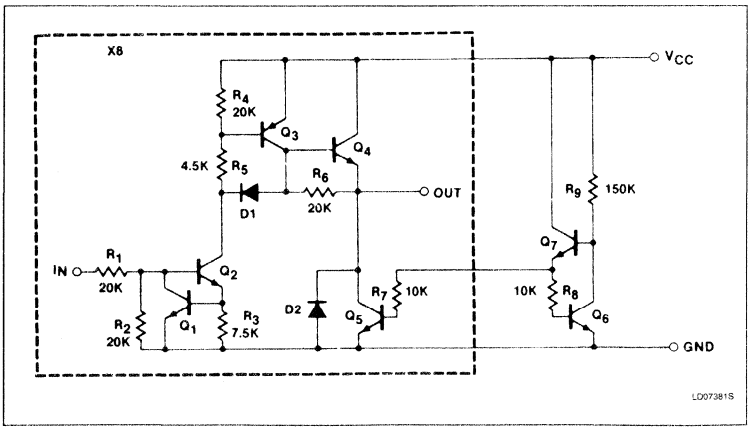
APPLICATIONS

- **Digital clocks**
- **Dashboard displays**
- **Panel displays**

ORDERING INFORMATION

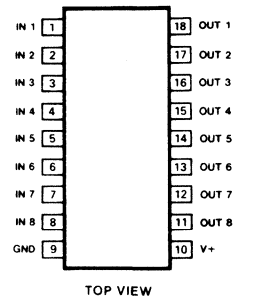
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP	0 to +70°C	NE594N
18-Pin Ceramic DIP	0 to +70°C	NE594F
20-Pin Plastic SO	0 to +70°C	NE594D
18-Pin Plastic DIP	−40°C to +85°C	SA594N
18-Pin Ceramic DIP	−40°C to +85°C	SA594F

EQUIVALENT SCHEMATIC



PIN CONFIGURATIONS

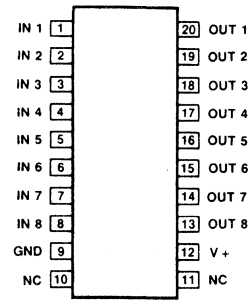
N, F Packages



TOP VIEW

CD11640S

D Package[1]



TOP VIEW

CD11650S

NOTE:
1. SOL – Released in large SO package only.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise noted)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	45	V
V_{OUT}	Output voltage	V_{CC}	
V_{IN}	Input voltage	−0.3, +20	V
I_{OUT}	Output current Each output All outputs	 50 200	 mA mA
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1] F package N package D package	 1500 1690 1390	 mW mW mW
T_A	Operating ambient temperature range NE594 SA594	 0 to 70 −40 to +85	 °C °C
T_{STG}	Storage temperature range	+65 to +150	°C
T_J	Maximum junction temperature	−150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 12.0mW/°C
   N package at 13.5mW/°C
   D package at 11.1mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.75 to +40V, T_A = 0 to 70°C (NE), T_A = −40 to +85°C (SA), unless otherwise stated.

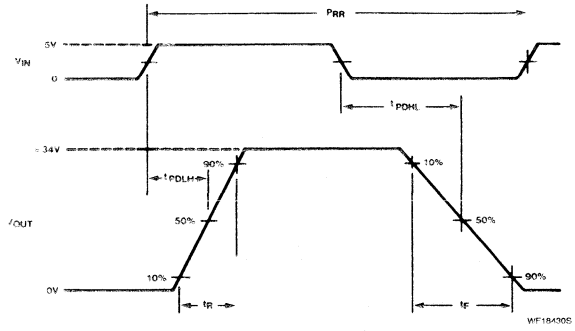
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{CC}	Supply voltage range			4.75	35	40	V
I_{CCH} I_{CCL}	Supply current (all outputs high) Supply current (all outputs low)	V_{CC} = 40V, V_{IN} = 3.5V V_{CC} = 40V, V_{IN} = 0.4V			3 0.4	6 1	mA mA
V_{IN} V_{IH} V_{IL}	Input voltage range Input voltage to ensure logic '1' Input voltage to ensure logic '0'			0 2.6		15 0.8	V V V
I_{IH} I_{IL} I_{IN}	Input current to ensure logic '1' Input current to ensure logic '0' Input current	 V_{IN} = 2.6V V_{IN} = 5.0V V_{IN} = 15.0V		100	 60 180 .68	 10 130 330 1.3	μA μA μA μA mA
V_{OH}	Output high voltage	V_{IN} = 3.5V, I_{OUT} = −25mA, V_{OUT} with respect to V_{CC}	T_A = 25°C	V_{CC}−1.5	V_{CC}−1.1		V
			Over temp.	V_{CC}−2	V_{CC}−1.3		V
V_{OH}	Output high, no load voltage	V_{IN} = 3.5V, I_{OUT} = 0, T_A = 25°C, V_{OUT} with respect to V_{CC}		V_{CC}−1	V_{CC}−0.8		V
V_{OFF}	Output 'OFF' voltage level	V_{IN} = 0.8V, I_{OUT} = 0			10	200	mV
I_{OH}	Available output current	V_{CC} = 35V, V_{IN} = 3.5V, V_{OUT} = 30V, T_A = 25°C		−35			mA
I_{OUT}	Output pulldown current	V_{CC} = V_{OUT} = 35V, Inputs open		100	200	400	μA
I_{CEX}	Output leakage current	T_A = 25°C, V_{IN} = 0.4V V_{CC} = 40V, V_{OUT} = 0V			−1 −1		μA

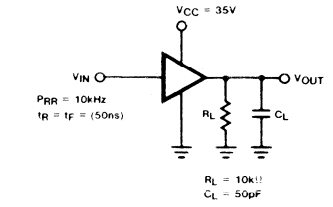
AC ELECTRICAL CHARACTERISTICS

V_{CC} = 35V, T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_{PLH}	Propagation delay — low-to-high output transition	50% V_{IN} to 50% V_{OUT}		1	5	μs
t_{PHL}	Propagation delay — high-to-low output transition	50% V_{IN} to 50% V_{OUT}		3	10	μs
t_R t_F	Output rise time Output fall time	10% V_{OUT} to 90% V_{OUT} 90% V_{OUT} to 10% V_{OUT}		0.5 1.5	3 5	μs μs

SWITCHING TIMES OF DRIVERS



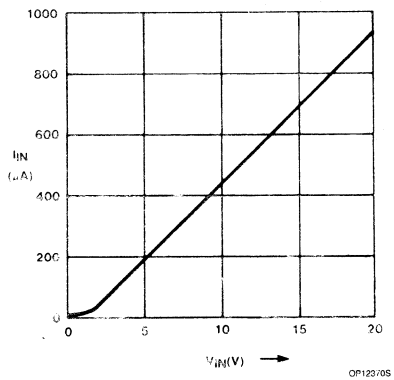


NOTE:
Includes probe and fixture capacitance.

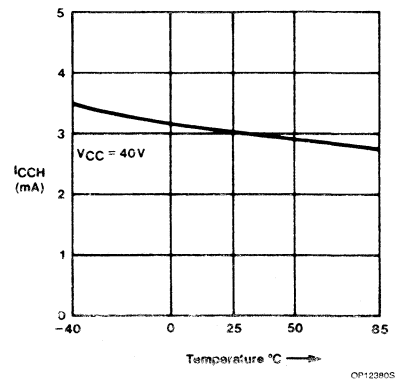
Figure 1. Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

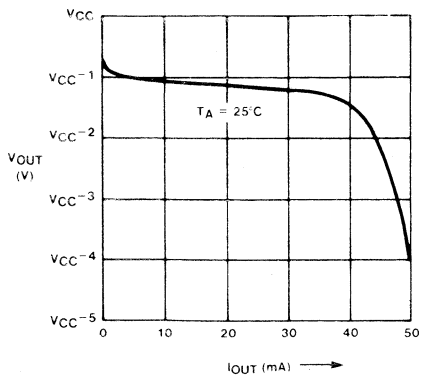
I_{IN} vs V_{IN}



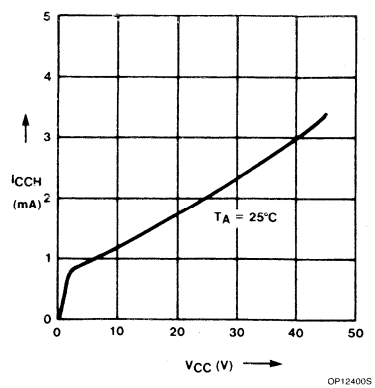
I_{CCH} vs Temperature



Output Voltage vs Output Current



I_{CC} vs V_{CC} (All inputs High)



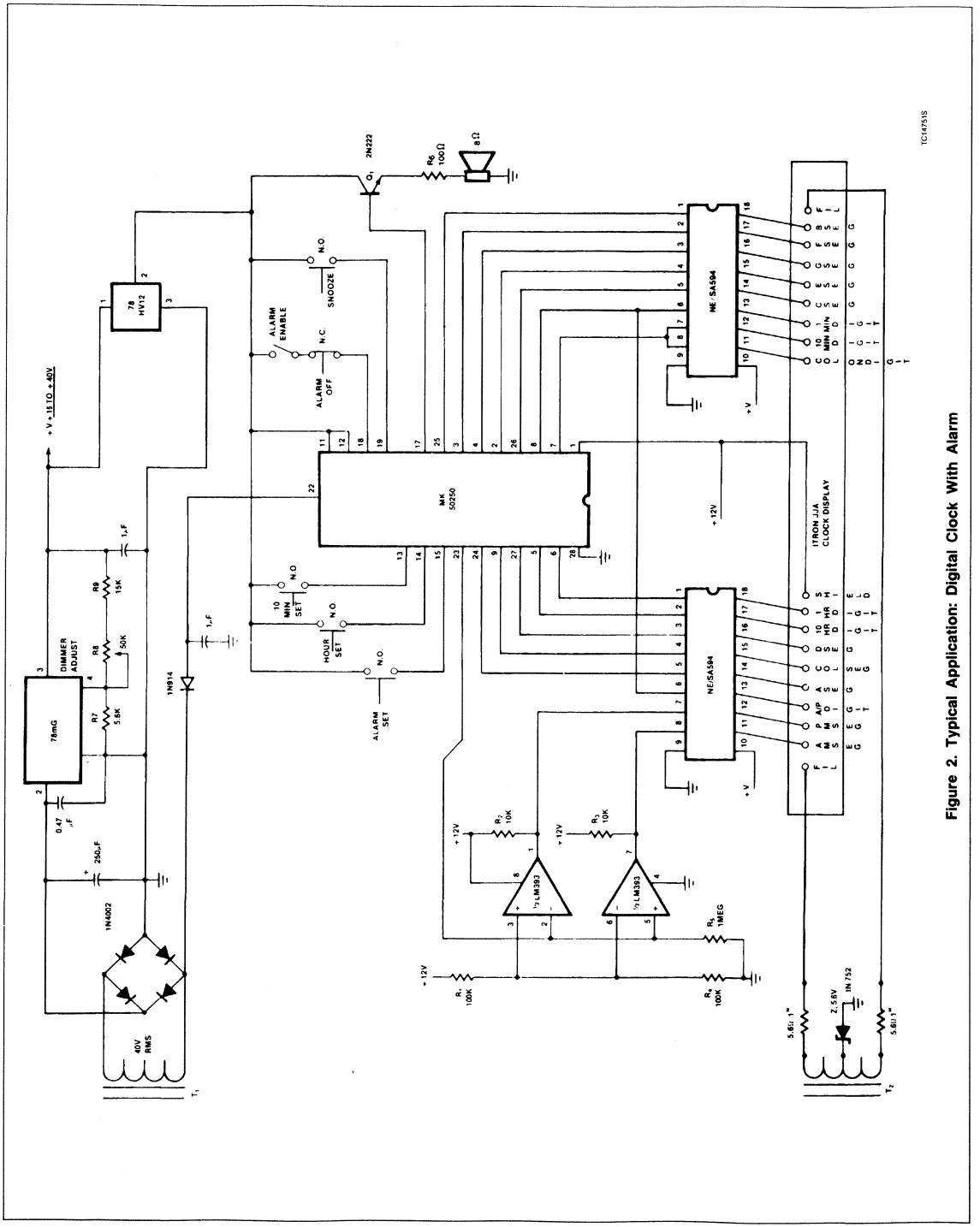


Figure 2. Typical Application: Digital Clock With Alarm

AN112
LED Decoder Drivers: Using the NE587 and NE589

Application Note

- **Strobed latch**
- **Inputs compatible with NMOS, CMOS, DMOS, TTL**
- **Single 5V supply**
- **Inputs are compatible with microprocessor bus**
- **BCD inputs — hexadecimal outputs**
- **Programmable segment current**

Figure 1. NE587/589 LED Drivers

LED DECODER DRIVER NE587 AND 589

The NE587 and 589 are latchable decoder drivers for LED displays. Figure 1 provides a summary of their features.

The programmable constant-current supplies (fixed or adjustable) are essentially independent of output voltage, power supply voltage, and temperature.

The data (BCD) and $\overline{LE}$ (latch enable) inputs are low loading and thus are compatible with a data bus system.

Figure 2 shows a block diagram of the NE587/589. Seven-segment decoding is implemented using a ROM.

LED DRIVERS AND POWER DISSIPATION CONSIDERATION

The following discussion refers to the NE587, but is also applicable for the 589.

LED displays are power hungry devices, and, inevitably, somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the NE587 output is a constant programmed current source, all the remaining supply voltage which is not dropped across the LED (and the digit driver, if used) will appear across the output of the NE587. Thus, the power dissipation in the NE587 will go up sharply if the display power supply voltage rises. Clearly then, it is good design practice to keep the display supply voltage as low as possible, consistent with proper operation of the output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, total system power remains the same.

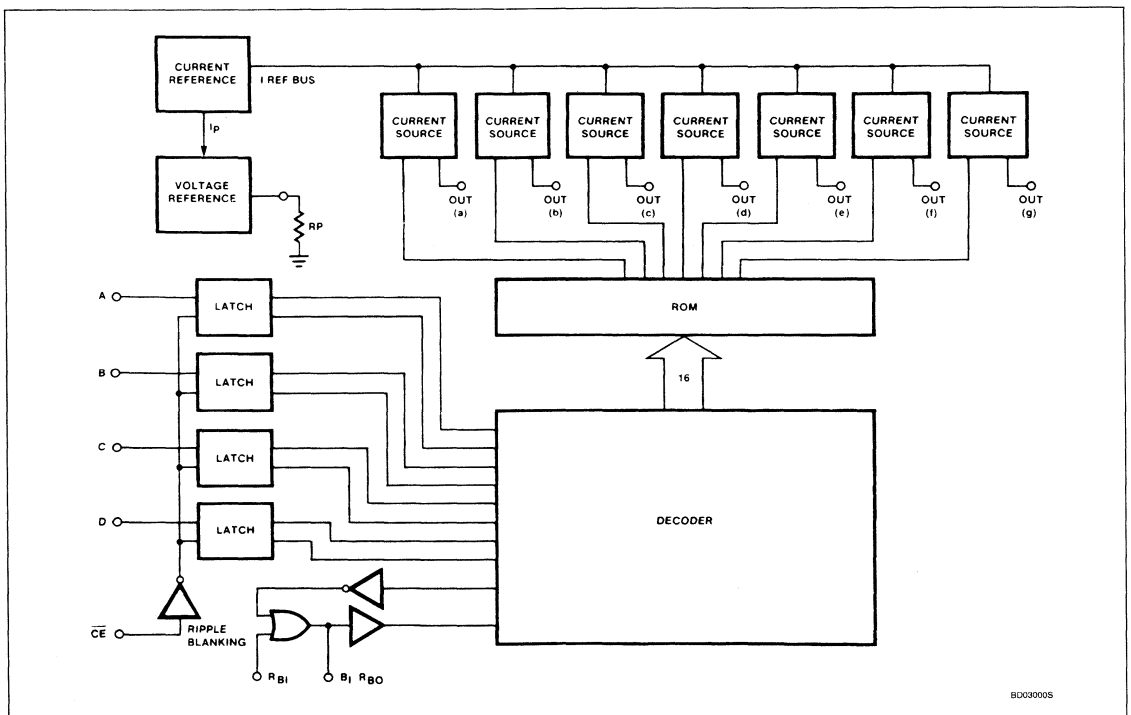


Figure 2. NE587/589 LED Drivers Block Diagram

LED Decoder Drivers: Using the NE587 and NE589

AN112

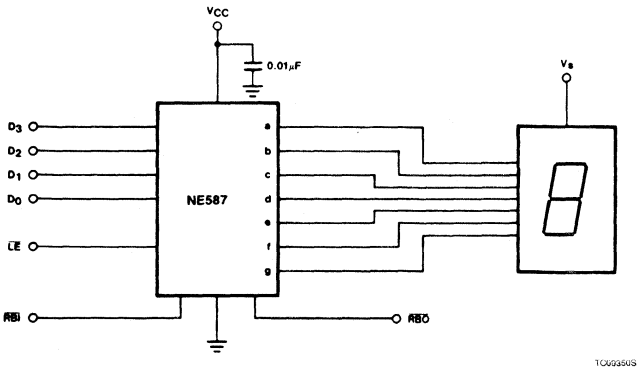


Figure 3. Typical Applications Driving a Single Digit

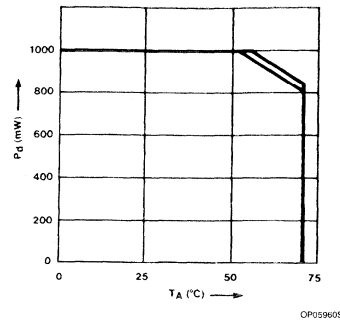


Figure 4. Maximum Power Dissipation vs Temperature

Power dissipation within the NE587 may be calculated as follows. Referring to Figure 3, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

- V_{CC} Supply voltage to driver
- V_S Supply voltage to display
- I_{CC} Quiescent supply current of driver
- I_{SEG} LED segment current
- V_F LED segment forward voltage at I_{SEG}
- K_{DC} % Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected. However, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

These voltages are all for single diode displays. Some early red displays had 2 series LEDs per segment, hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

$$P_D = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{SEG} \times K_{DC}\ mW \quad (1)$$

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$
$I_{SEG} = 30mA$

$$P_{D\ MAX} = 5.25 \times 50 + 3.25 \times 7 \times 30mW = 945mW$$

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{D\ AV} = 5.0 \times 30 + 3.00 \times 5 \times 25mW = 525\ mW$$

Operating temperature range limitations can be deduced from the power dissipation graph in Figure 4.

However, a major portion of this power dissipation ($P_{D\ MAX}$) is because the current source output is operating with 3.25V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst-case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_F for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by using equation 2.

$$R_S = \frac{V_{DROP}}{I_{SEG} \times \#\ \text{of SEG}} \quad (2)$$

or

$$R_S = \frac{2.0}{7 \times I_{SEG}} \simeq 10\Omega\ (\tfrac{1}{2}W\ \text{rating})$$

assuming worst-case I_{SEG} of 30mA, now:

$$P_{D\ MAX} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{SEG}) \times 7 \times I_{SEG} \times K_{DC}$$
$$= 5.25 \times 50 + 1.25 \times 7 \times 30mW = 525mW \quad (3)$$

and $P_{D\ AV} = 5.0 \times 30 + 1.25 \times 5 \times 25 = 306mW$

If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$V_S - V_F - nV_D$, $V_D \simeq 0.8V$

Where n is the number of diodes used, and so power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in Figure 5. For example, a Darlington PNP or NPN emitter-follower may be preferable. Figure 6 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V, which means that the power dissipation is evenly distributed between the two integrated circuits.

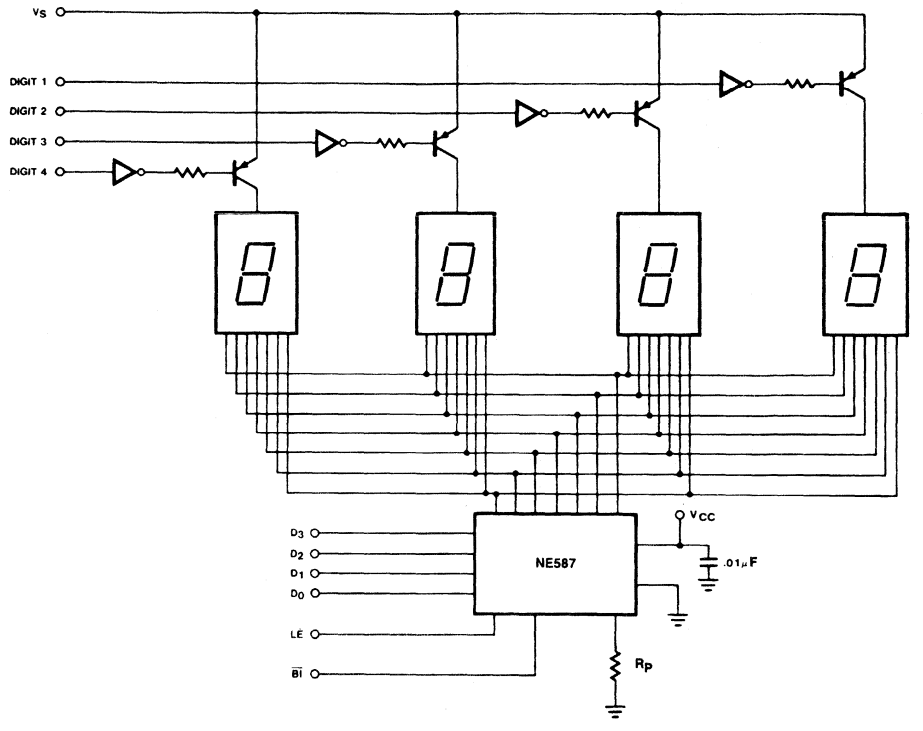


Figure 5. 4-Digit Multiplexed LED Display

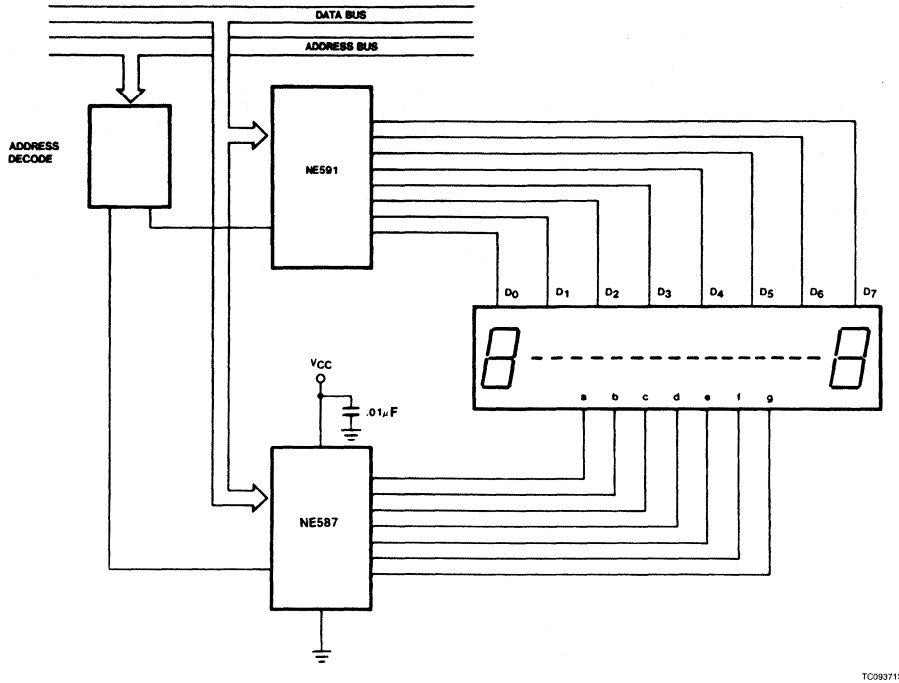


Figure 6. Interfacing 8-Digit LED Display With Microprocessor Bus

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact, a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about $3-4.5V_{RMS}$ works well in most LED display systems. Waveforms are shown in Figure 7.

The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With $V_S = 4.9V$ peak
$V_F = 2.0V$

The duty cycle is approximately 60%.

V_S in this example was derived by the circuit shown in Figure 7. Remember that the forward voltage drop of the rectifying diode must be subtracted to arrive at the exact peak of the V_S voltage.

Figure 8 shows other typical application schemes for multiplexing LED displays.

ADDRESSABLE PERIPHERAL DRIVERS SUPPORT MICROPROCESSOR-BASED SYSTEMS

The Signetics NE590, NE5090 and NE591 addressable peripheral drivers (APDs) greatly facilitate interfacing a variety of support circuits to microprocessor-based systems.

The APDs are designed to eliminate the need for many of the buffers, latches, TTL ICs, and discrete transistors currently needed to drive peripheral devices.

Figure 9 shows that each driver includes a set of input latches, a 1-of-8 demultiplexer, and a set of high current drive outputs together with the assorted chip enable and clear logic.

The low loading inputs of these drivers (typically $I_{IL} = 15\mu A$ and $I_{IH} = 1\mu A$) allow direct interfacing to the microprocessor bus. Eight addressable latches, which are addressed by a three bit binary code and (set/reset) by a single binary bit, allow storage of each output condition (ON/OFF), allowing the microprocessor to continue processing after the APD has been addressed.

Driver selection is accomplished with a low active chip enable which may be derived from

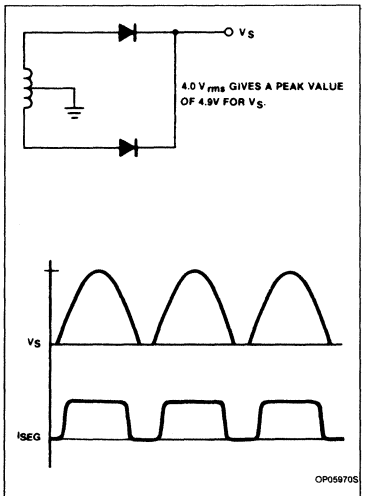


Figure 7

the I/O decoder common to all I/O devices. A low active master clear is also provided to reset all outputs simultaneously. This signal

LED Decoder Drivers: Using the NE587 and NE589

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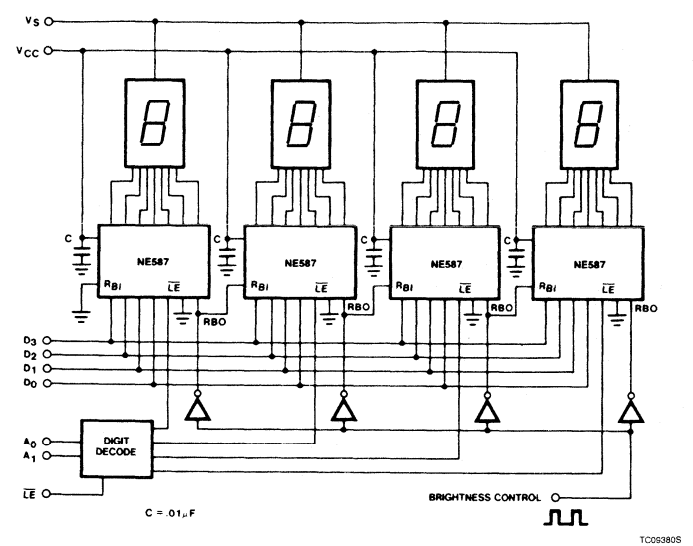


Figure 8. 4-Digit Display With Brightness Control and Leading-Edge Ripple Blanking

may be generated from the I/O decoder or set high when not required.

The high current outputs of the drivers (250mA sinking with the NE590, 150mA sinking with the NE5090 and 250mA sourcing with the NE591) allow direct interfacing to relays, motors, lamps, LEDs, and other devices or systems requiring high current drive capabilities.

Figure 10 demonstrates the use of APDs in a microprocessor-based system. When driving LED displays, a single 8-bit word contains all the data required for defining both digit location and segment selection. The APD uses four bits — three to address one of 8 outputs and one to set the output to an ON or OFF state.

When using the NE590 or NE5090, ON refers to the output low state in which the output is capable of sinking a maximum of 250mA for the NE590, or 150mA for the NE5090. The clear ($\overline{CL}$) pin may be tied high and would normally not be required in this application.

The four remaining data bits are required by the NE587 which supplies segment data. These four BCD data bits are converted into seven-segment data used for driving the

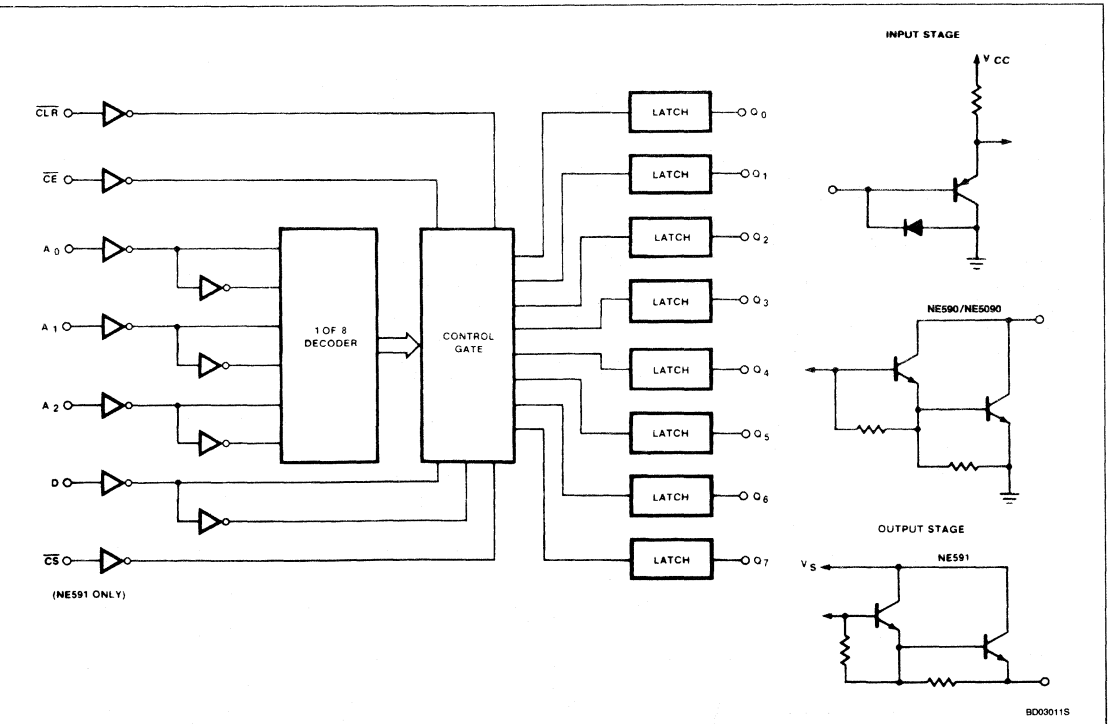


Figure 9. NE590/591/5090 Block Diagram

LED Decoder Drivers: Using the NE587 and NE589

AN112

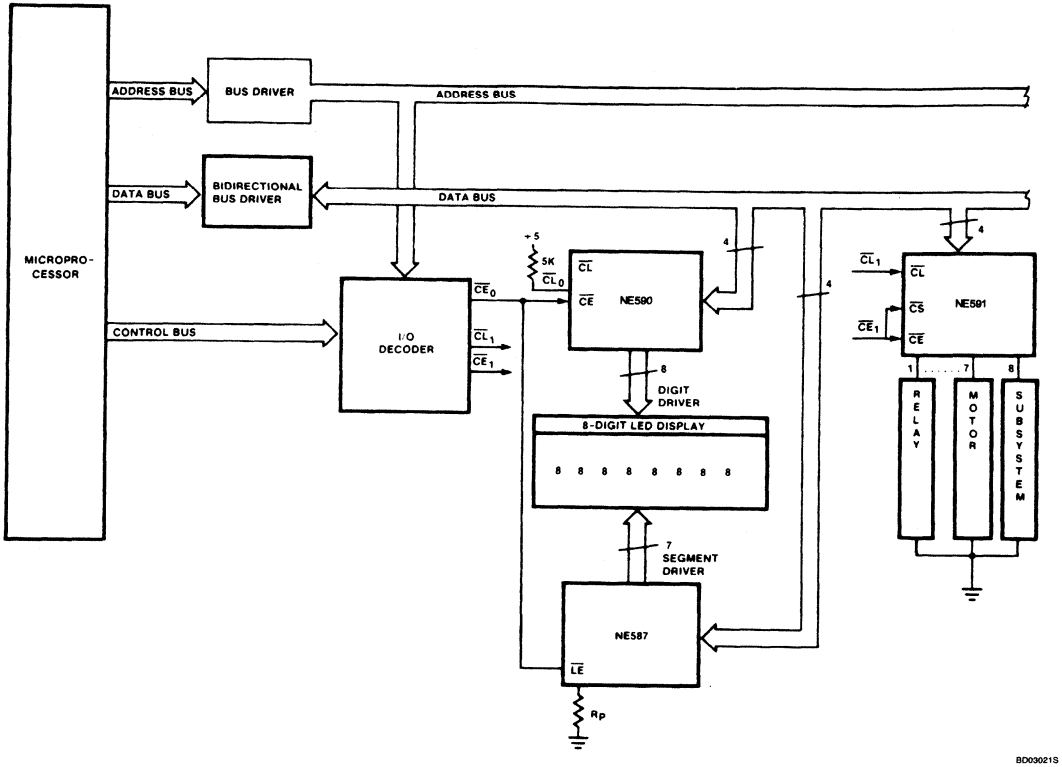


Figure 10. Microprocessor-Based System

anodes of the LEDs. Data is strobed into the latches by the LATCH ENABLE INPUT at the same time that information is being supplied to the NE590. Since the NE587 provides a constant-current sink, uniform brightness is obtained from each segment in the display. The NE587 is capable of supplying up to 50mA/segment. Segment currents are set by a single programming resistor.

Figure 10 shows several devices connected to the NE591: a relay, a motor, and a D-C subsystem. Each device is selected in the same manner as the LED digits; that is, three bits are used to select the output and one bit is used to turn the output ON or OFF.

An output may be cleared in one of two ways:

1) By direct selection and clearing of the individual latch,
   or
2) By clearing all outputs through the use of the clear input.

The latter method does not require addressing.

The examples shown in Figure 10 clearly demonstrate the advantages that can be derived from using the NE590 and NE591 APDs in microprocessor-based systems. These devices provide easy interfacing and minimize the number of interfacing components; they also provide the logic interface to the microprocessor and the switch function and high current drive required by the peripheral units.

TIMERS

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Timers

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ICM7555
General Purpose CMOS Timer

Product Specification

DESCRIPTION

The ICM7555 is a CMOS timer providing significantly improved performance over the standard NE/SE555 timer, while at the same time being a direct replacement for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$, and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher-frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

The ICM7555 is a stable controller capable of producing accurate time delays or frequencies.

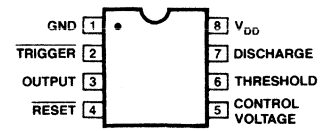
In the one-shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the bipolar 555 device, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuit is triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads or provide minimal offsets to drive CMOS loads.

FEATURES

- **Exact equivalent in most applications for NE/SE555**
- **Low supply current — 80μA (typ)**
- **Extremely low trigger, threshold, and reset currents — 20pA (typ)**
- **High-speed operation — 500kHz guaranteed**
- **Wide operating supply voltage range guaranteed 2 to 18V**
- **Normal reset function — no crowbarring of supply during output transition**
- **Can be used with higher-impedance timing elements than the bipolar 555 for longer time constants**
- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **High output source/sink driver can drive TTL/CMOS**
- **Typical temperature stability of 0.005%/°C at 25°C**
- **Outputs have very low offsets, HI and LO**

PIN CONFIGURATION

D, FE, and N Packages



TOP VIEW

CD12800S

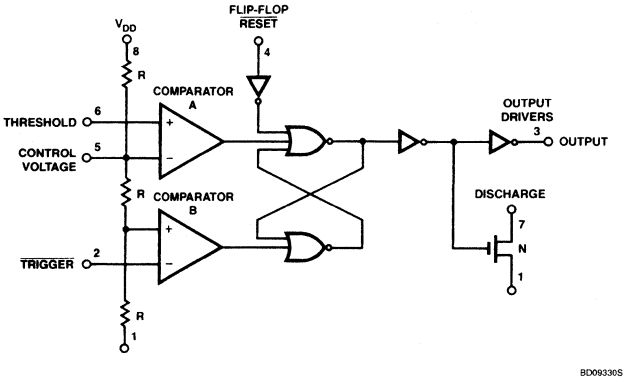
APPLICATIONS

- **Precision timing**
- **Pulse generation**
- **Sequential timing**
- **Time delay generation**
- **Pulse width modulation**
- **Pulse position modulation**
- **Missing pulse detector**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	ICM7555CN
8-Pin Plastic SO	0 to +70°C	ICM7555CD
8-Pin Plastic DIP	-40°C to +85°C	ICM7555IN
8-Pin Plastic SO	-40°C to +85°C	ICM7555ID
8-Pin Plastic DIP	-55°C to +125°C	ICM7555MN
8-Pin Ceramic DIP	-55°C to +125°C	ICM7555MFE

EQUIVALENT BLOCK DIAGRAM



NOTE:
Unused inputs should be connected to appropriate voltage from Truth Table.

TRUTH TABLE

THRESHOLD VOLTAGE	TRIGGER VOLTAGE	$\overline{\text{RESET}}$[1]	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
> 2/3(V+)	> 1/3(V+)	HIGH	LOW	ON
V_{TH} < 2/3	V_{TR} > 1/3	HIGH	STABLE	STABLE
DON'T CARE	< 1/3(V+)	HIGH	HIGH	OFF

NOTE:
1. $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage	+18	V
V_{TRIG} [1] V_{CV} V_{TH} V_{RST}	$\overline{\text{Trigger}}$ input voltage Control voltage Threshold input voltage $\overline{\text{RESET}}$ input voltage	> −0.3 to < V_{DD} + 0.3	V
I_{OUT}	Output current	100	mA
	Maximum power dissipation T_A = 25°C (still-air)[2, 3] F package N package D package	 780 1160 780	 mW mW mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead temperature (Soldering 60s)	300	°C

NOTES:
1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} + 0.3V or less than GND − 0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555 must be turned on first.
2. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
3. See "Power Dissipation Considerations" section.

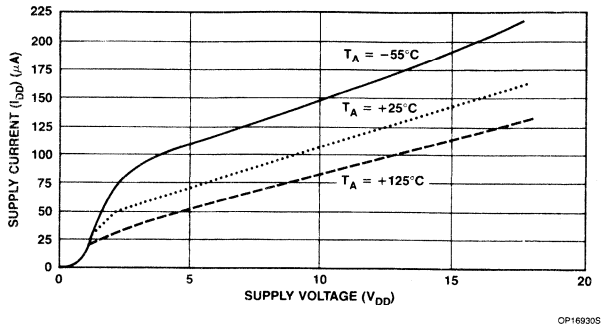
DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	ICM7555M			ICM7555I/C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply voltage	$T_{MIN} \leq T_A \leq T_{MAX}$	3		16	2		18	V
I_{DD}	Supply current[1]	$V_{DD} = V_{MIN}$ $V_{DD} = V_{MAX}$		50 180	200 300		50 180	120 300	μA μA
	Astable mode timing[2] R_A, R_B = 1k to 100k, C = 0.1μF $5V \leq V_{DD} \leq 15V$								
	Initial accuracy			1.0	5.0		1.0	5.0	%
	Drift with supply voltage			0.1	3.0		0.1	3.0	%/V
	Drift with temperature[3]								
		V_{DD} = 5V		50			50		ppm/°C
		V_{DD} = 10V		75			75		ppm/°C
		V_{DD} = 15V		100			100		ppm/°C
V_{TH}	Threshold voltage	V_{DD} = 5V	0.63	0.65	0.67	0.63	0.65	0.67	× V_{DD}
V_{TRIG}	Trigger voltage	V_{DD} = 5V	0.29	0.31	0.34	0.29	0.31	0.34	× V_{DD}
I_{TRIG}	Trigger current	$V_{DD} = V_{TRIG} = V_{MAX}$ $V_{DD} = V_{TRIG}$ = 5V $V_{DD} = V_{TRIG} = V_{MIN}$		50 10 1			50 10 1		pA pA pA
I_{TH}	Threshold current	$V_{DD} = V_{TH} = V_{MAX}$ $V_{DD} = V_{TH}$ = 5V $V_{DD} = V_{TH} = V_{MIN}$		50 10 1			50 10 1		pA pA pA
I_{RST}	Reset current	$V_{DD} = V_{RST} = V_{MAX}$ $V_{DD} = V_{RST}$ = 5V $V_{DD} = V_{RST} = V_{MIN}$		100 20 2			100 20 2		pA pA pA
V_{RST}	Reset voltage	$V_{DD} = V_{MIN}$ and V_{MAX}	0.4	0.7	1.0	0.4	0.7	1.0	V
V_{CV}	Control voltage	V_{CC} = 5V	0.62	0.65	0.67	0.62	0.65	0.67	V
V_{OL}	Output voltage (low)	$V_{DD} = V_{MAX}$, I_{SINK} = 3.2mA V_{DD} = 5V, I_{SINK} = 3.2mA		0.1 0.2	0.4 0.4		0.1 0.2	0.4 0.4	V V
V_{OH}	Output voltage (high)	$V_{DD} = V_{MAX}$, I_{SOURCE} = 1.0mA V_{DD} = 5V, I_{SOURCE} = 1.0mA	15.25 4.0	15.7 4.5		17.25 4.0	17.8 4.6		V V
V_{DIS}	Discharge output voltage	V_{DD} = 5V, I_{DIS} = 10.0mA		0.2	0.4		0.2	0.4	V
t_R	Rise time of output[3]	R_L = 10MΩ, C_L = 10pF, V_{DD} = 5V		45	75		45	75	ns
t_F	Fall time of output[3]	R_L = 10MΩ, C_L = 10pF, V_{DD} = 5V		20	75		20	75	ns
f_{MAX}	Maximum oscillator frequency (astable mode)		500			500			kHz

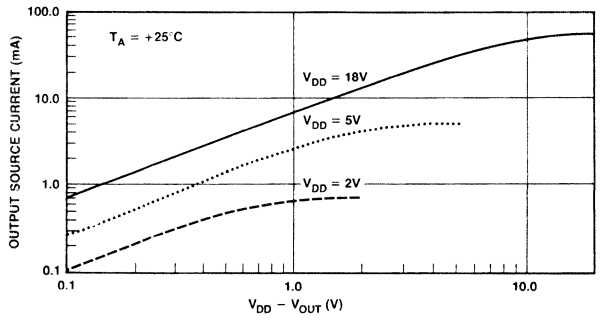
NOTES:

1. The supply current value is essentially independent of the $\overline{\text{TRIGGER}}$, THRESHOLD, and $\overline{\text{RESET}}$ voltages.
2. Astable timing is calculated using the following equation: $f = \frac{1.38}{(R_A + 2R_B)C}$. The components are defined in Figure 2.
3. Parameter is not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

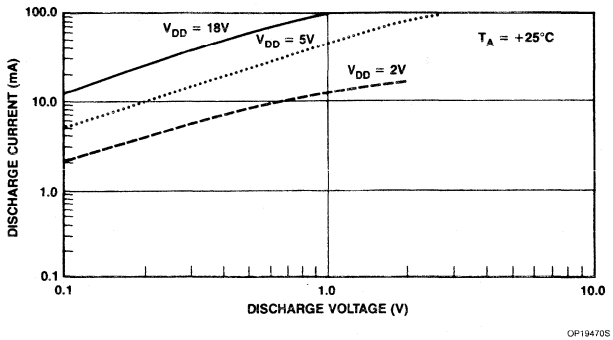


Supply Current vs. Supply Voltage

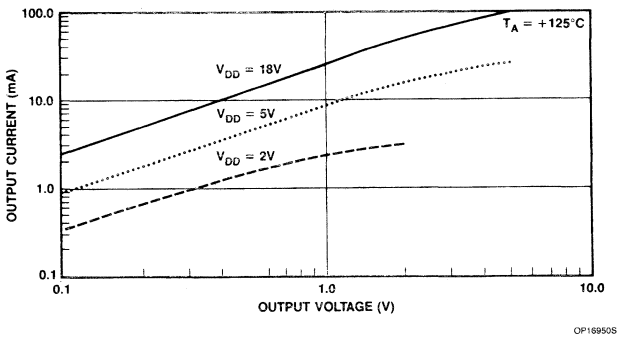


High Output Voltage Drop Vs Output Source Current

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

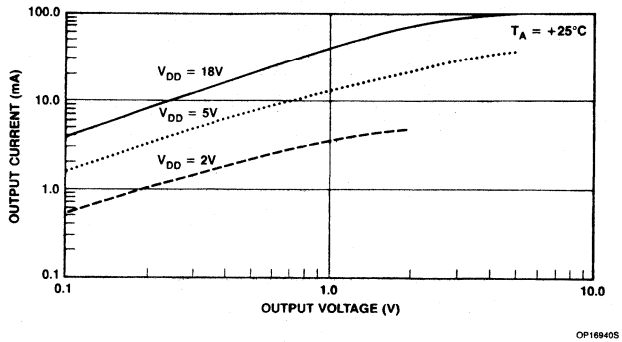


Discharge Low Output Voltage vs Discharge Sink Current

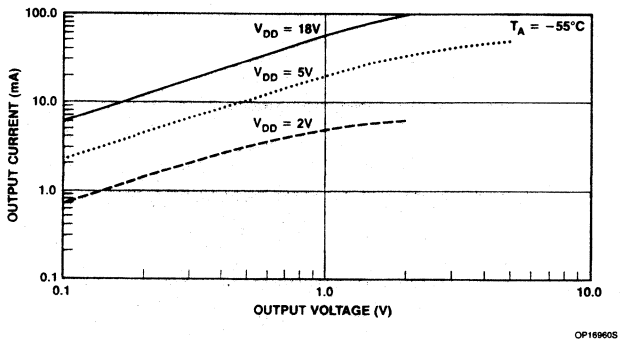


Low Output Voltage vs Output Sink Current

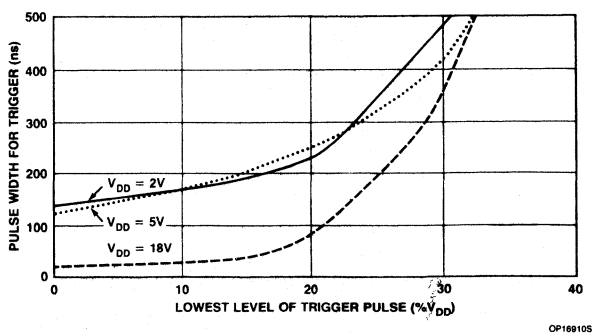
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Low Output Voltage vs Output Sink Current

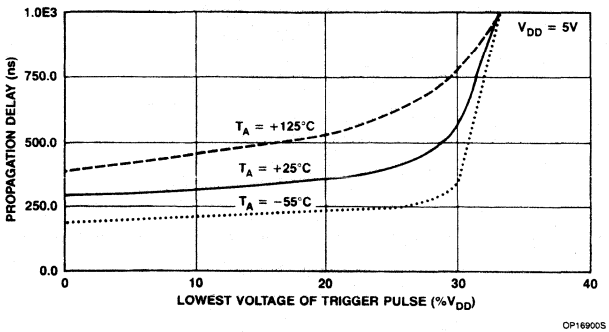


Low Output Voltage vs Output Sink Current

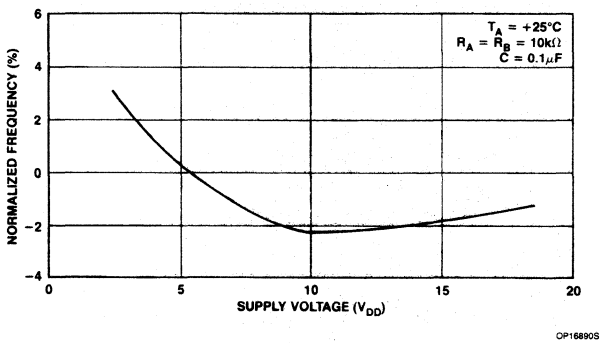


Minimum Pulse Width for Triggering

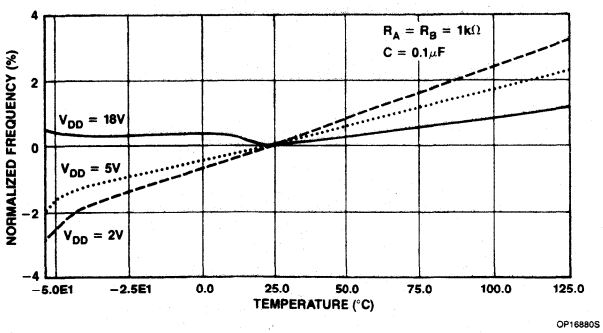
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Propagation Delay vs Voltage Level of Trigger Pulse

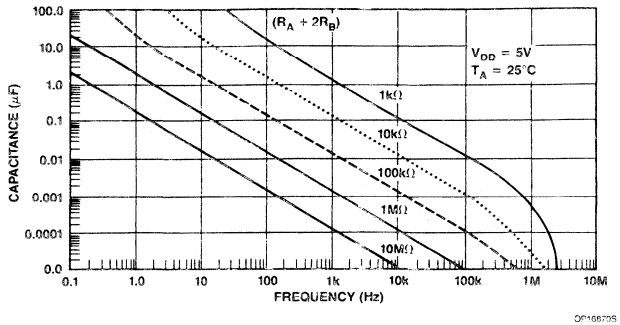


Normalized Frequency Stability as a Function of Supply Voltage Astable Mode)

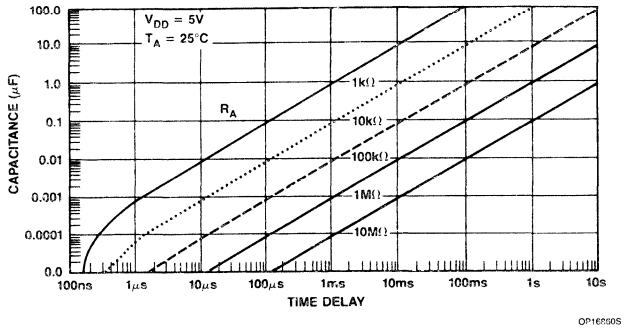


Normalized Frequency Stability as a Function of Temperature (Astable Mode)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Free-Running Frequency as a Function of R_A, R_B, and C



Monostable Time Delay vs R_A and C

APPLICATION NOTES

General

The ICM7555 device is, in most instances, a direct replacement for the NE/SE555 device. However, it is possible to effect economies in the external component count using the ICM7555. Because the bipolar 555 device produces large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555 device produces no such transients. See Figure 1.

The ICM7555 produces supply current spikes of only 2 – 3mA instead of 300 – 400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications, 2 capacitors can be saved using an ICM7555.

Power Supply Considerations

Although the supply current consumed by the ICM7555 device is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 2 and 3.

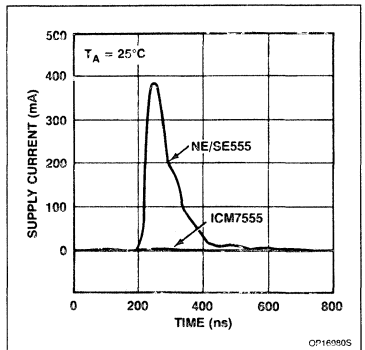


Figure 1. Supply Current Transient Compared With a Standard Bipolar 555 During an Output Transition

Output Drive Capability

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5V or more, the ICM7555 will drive at least 2 standard TTL loads.

Astable Operation

If the circuit is connected as shown in Figure 2, it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus, the duty cycle (D) may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 V_{DD} and 2/3 V_{DD}. Since the charge rate and the threshold levels are directly proportional to the supply voltage, the frequency of oscillation is independent of the supply voltage.

$$F = \frac{1.38}{(R_A + 2R_B)C} \qquad D = \frac{R_A + R_B}{R_A + 2R_B}$$

Monostable Operation

In this mode of operation, the timer functions as a one-shot. Initially, the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to Pin 2, the internal flip-flop is set which releases the short circuit across the external capacitor and drives the OUTPUT High. The voltage across the capacitor now increases exponentially with a time constant $t = R_A C$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

Control Voltage

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode, or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555, i.e., 0.6 to 0.7V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555 in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

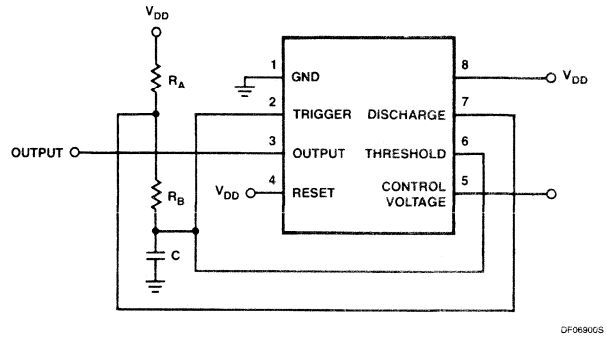


Figure 2. Astable Operation

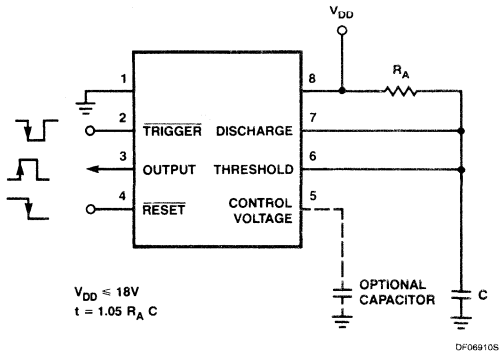


Figure 3. Monostable Operation

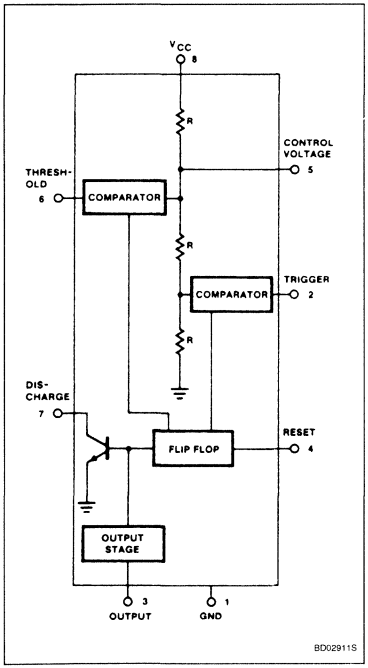
NE/SA/SE555/SE555C
Timer

Product Specification

DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

BLOCK DIAGRAM



FEATURES

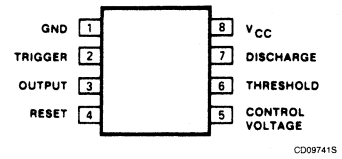
- **Turn-off time less than 2μs**
- **Max. operating frequency greater than 500kHz**
- **Timing from microseconds to hours**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **TTL compatible**
- **Temperature stability of 0.005% per °C**

APPLICATIONS

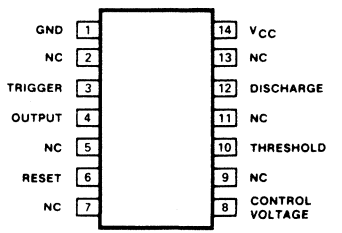
- **Precision timing**
- **Pulse generation**
- **Sequential timing**
- **Time delay generation**
- **Pulse width modulation**
- **Pulse position modulation**
- **Missing pulse detector**

PIN CONFIGURATIONS

D, N, FE Packages

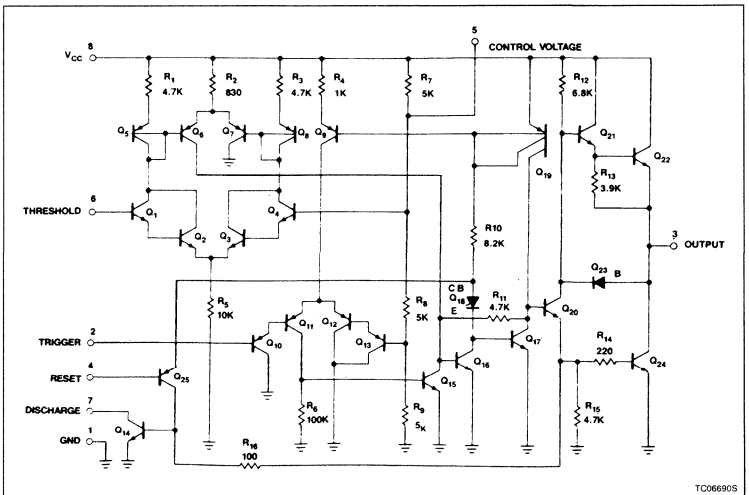


F Package



TOP VIEW

EQUIVALENT SCHEMATIC



NOTE:
Pin numbers are for 8-Pin package.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Hermetic Cerdip	0 to +70°C	NE555FE
8-Pin Plastic SO	0 to +70°C	NE555D
8-Pin Plastic DIP	0 to +70°C	NE555N
8-Pin Plastic DIP	−40°C to +85°C	SA555N
8-Pin Plastic SO	−40°C to +85°C	SA555D
8-Pin Hermetic Cerdip	−55°C to +125°C	SE555CFE
8-Pin Plastic DIP	−55°C to +125°C	SE555CN
14-Pin Plastic DIP	−55°C to +125°C	SE555N
8-Pin Hermetic Cerdip	−55°C to +125°C	SE555FE
14-Pin Ceramic DIP	0 to +70°C	NE555F
14-Pin Ceramic DIP	−55°C to +125°C	SE555F
14-Pin Ceramic DIP	−55°C to +125°C	SE555CF

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage SE555 NE555, SE555C, SA555	 +18 +16	 V V
P_D	Maximum allowable power dissipation[1]	600	mW
T_A	Operating ambient temperature range NE555 SA555 SE555, SE555C	 0 to +70 −40 to +85 −55 to +125	 °C °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTE:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the FE, N and F packages. At ambient temperatures above 25°C, where this limit would be derated by the following factors:
   D package 160 °C/W
   FE package 150 °C/W
   N package 100 °C/W
   F package 105 °C/W

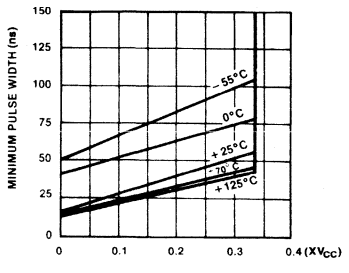
DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$ to $+15$ unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	$V_{CC} = 5V$, $R_L = \infty$ $V_{CC} = 15V$, $R_L = \infty$		3 10	5 12		3 10	6 15	mA mA
t_M $\Delta t_M/\Delta T$ $\Delta t_M/\Delta V_S$	Timing error (monostable) Initial accuracy[2] Drift with temperature Drift with supply voltage	$R_A = 2k\Omega$ to $100k\Omega$ $C = 0.1\mu F$		 0.5 30 0.05	 2.0 100 0.2		 1.0 50 0.1	 3.0 150 0.5	 % ppm/°C %/V
t_A $\Delta t_A/\Delta T$ $\Delta t_A/\Delta V_S$	Timing error (astable) Initial accuracy[2] Drift with temperature Drift with supply voltage	R_A, $R_B = 1k\Omega$ to $100k\Omega$ $C = 0.1\mu F$ $V_{CC} = 15V$		 4 0.15	 6 500 0.6		 5 0.3	 13 500 1	 % ppm/°C %/V
V_C	Control voltage level	$V_{CC} = 15V$ $V_{CC} = 5V$	9.6 2.9	10.0 3.33	10.4 3.8	9.0 2.6	10.0 3.33	11.0 4.0	V V
V_{TH}	Threshold voltage	$V_{CC} = 15V$ $V_{CC} = 5V$	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	V V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	μA
V_{TRIG}	Trigger voltage	$V_{CC} = 15V$ $V_{CC} = 5V$	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67	5.6 2.2	V V
I_{TRIG}	Trigger current	$V_{TRIG} = 0V$		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[4]		0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current Reset current	$V_{RESET} = 0.4V$ $V_{RESET} = 0V$		0.1 0.4	0.4 1.0		0.1 0.4	0.4 1.5	mA mA
V_{OL}	Output voltage (low)	$V_{CC} = 15V$ $I_{SINK} = 10mA$ $I_{SINK} = 50mA$ $I_{SINK} = 100mA$ $I_{SINK} = 200mA$ $V_{CC} = 5V$ $I_{SINK} = 8mA$ $I_{SINK} = 5mA$		 0.1 0.4 2.0 2.5 0.1 0.05	 0.15 0.5 2.2 0.25 0.2		 0.1 0.4 2.0 2.5 0.3 0.25	 0.25 0.75 2.5 0.4 0.35	 V V V V V V
V_{OH}	Output voltage (high)	$V_{CC} = 15V$ $I_{SOURCE} = 200mA$ $I_{SOURCE} = 100mA$ $V_{CC} = 5V$ $I_{SOURCE} = 100mA$	 13.0 3.0	 12.5 13.3 3.3	 	 12.75 2.75	 12.5 13.3 3.3	 	 V V V
t_{OFF}	Turn-off time[5]	$V_{RESET} = V_{CC}$		0.5	2.0		0.5	2.0	μs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	ns

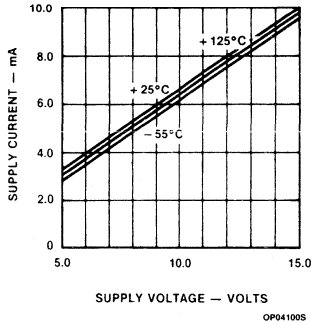
NOTES:
1. Supply current when output high typically 1mA less.
2. Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
3. This will determine the max value of $R_A + R_B$, for 15V operation, the max total $R = 10M\Omega$, and for 5V operation, the max. total $R = 3.4M\Omega$.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to $0.8 \times V_{CC}$ into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

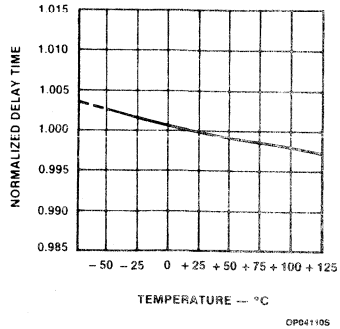
Minimum Pulse Width Required for Triggering



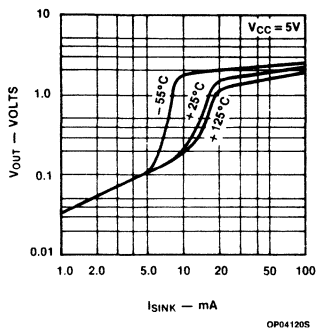
Supply Current vs Supply Voltage



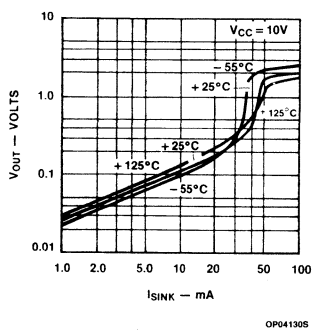
Delay Time vs Temperature



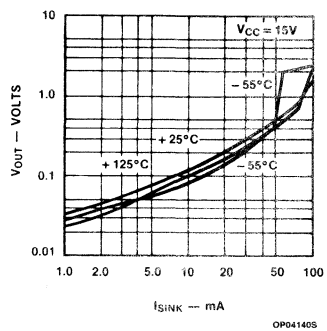
Low Output Voltage vs Output Sink Current



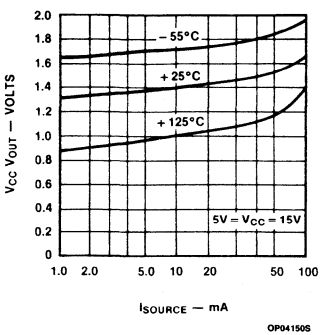
Low Output Voltage vs Output Sink Current



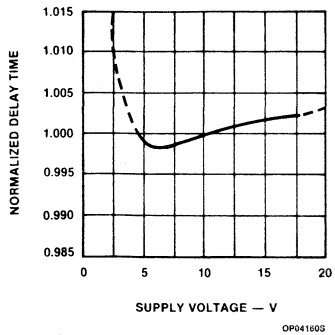
Low Output Voltage vs Output Sink Current



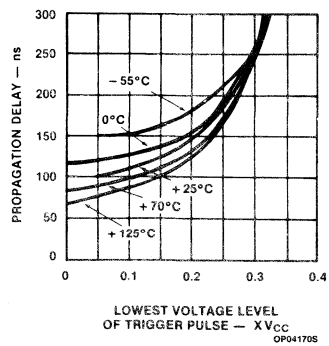
High Output Voltage Drop vs Output Source Current



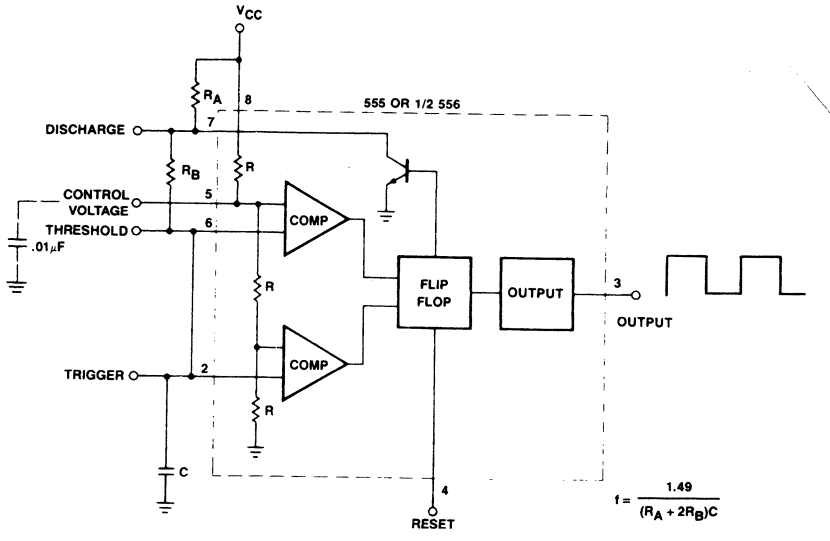
Delay Time vs Supply Voltage



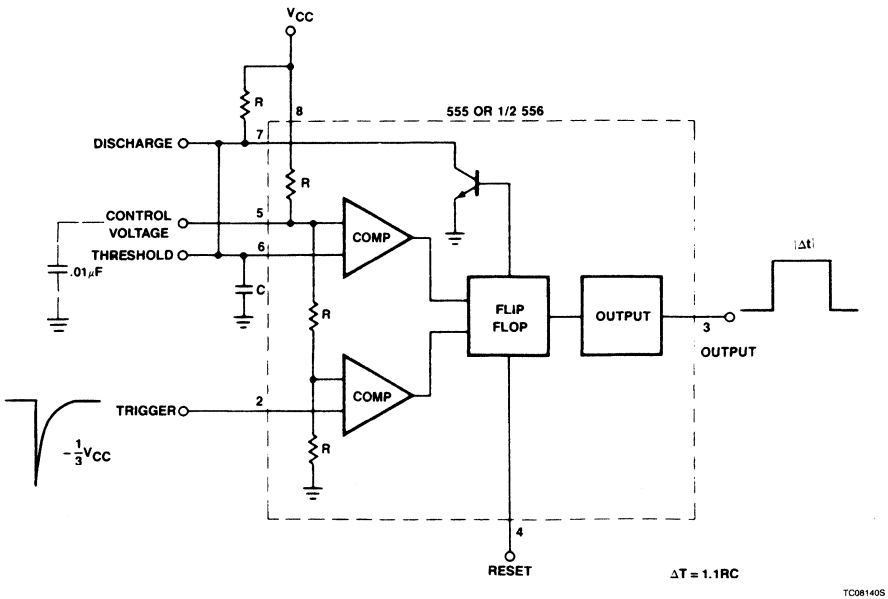
Propagation Delay vs Voltage Level of Trigger Pulse



TYPICAL APPLICATIONS

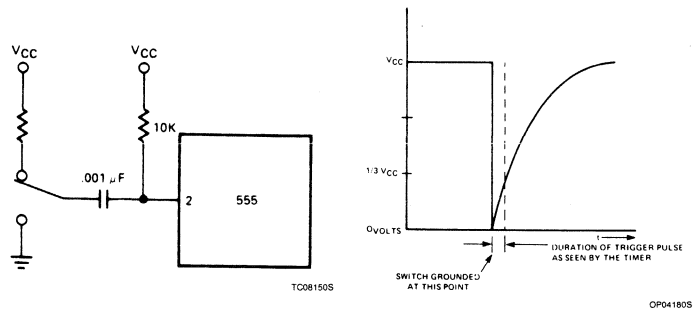


Astable Operation



Monostable Operation

TYPICAL APPLICATIONS



NOTE: All resistor values are in Ω.

Figure 1. AC Coupling of the Trigger Pulse

Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 1, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn-off time". This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q_5, which turns on Q_6. Current from Q_6 turns on Q_{16} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to given an output low. These steps cause the 2μs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15}. Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24}, which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

NE/SA/SE556/NE/SA/ SE556-1/SE556-1C
Dual Timer

Product Specification

DESCRIPTION

Both the 556 and 556-1 Dual Monolithic timing circuits are highly stable controllers capable of producing accurate time delays or oscillation. The 556 and 556-1 are a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other, sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

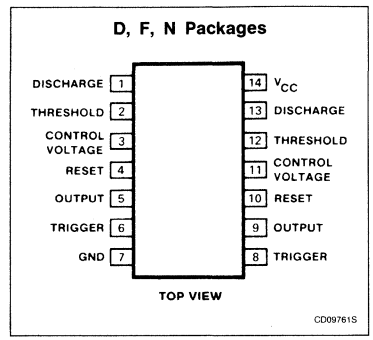
FEATURES

- **Turn-off time less than 2μs (556-1, 1C)**
- **Maximum operating frequency > 500kHz (556-1, 1C)**
- **Timing from microseconds to hours**
- **Replaces two 555 timers**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **TTL compatible**
- **Temperature stability of 0.005%/°C**
- **SE556-1 compliant to MIL-STD or JAN available from Signetics' Military Division**

APPLICATIONS

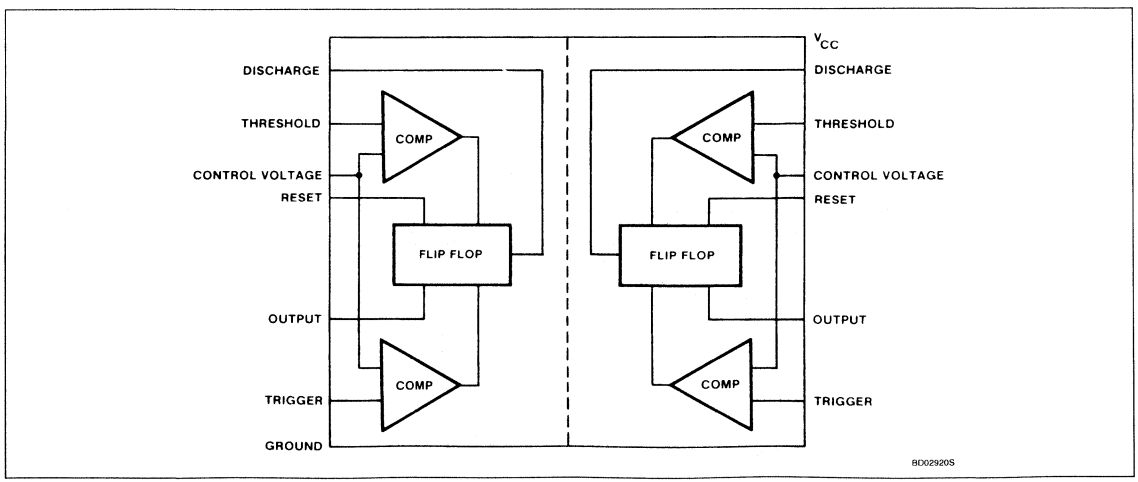
- **Precision timing**
- **Sequential timing**
- **Pulse shaping**
- **Pulse generator**
- **Missing pulse detector**

PIN CONFIGURATION



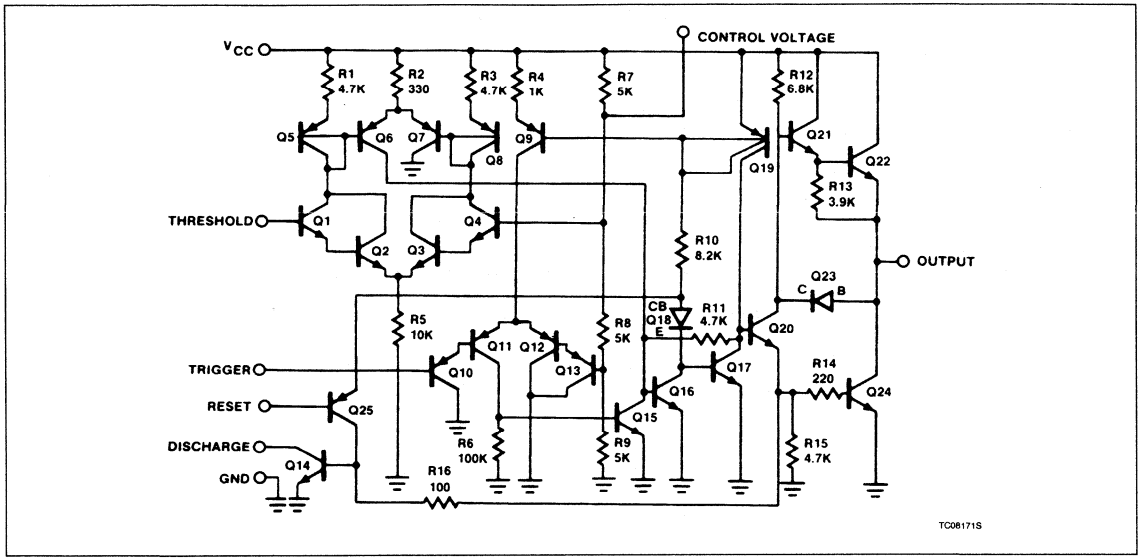
- **Tone burst generator**
- **Pulse width modulation**
- **Time delay generator**
- **Frequency division**
- **Industrial controls**
- **Pulse position modulation**
- **Appliance timing**
- **Traffic light control**
- **Touch-Tone® encoder**

BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT&T

EQUIVALENT SCHEMATIC (Shown for one circuit only)



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE556D
14-Pin Cerdip	0 to +70°C	NE556F
14-Pin Plastic DIP	0 to +70°C	NE556N
14-Pin Cerdip	0 to +70°C	NE556-1F
14-Pin Plastic DIP	0 to +70°C	NE556-1N
14-Pin Plastic DIP	−40°C to +85°C	SA556N
14-Pin Cerdip	−40°C to +85°C	SA556-1F
14-Pin Plastic DIP	−40°C to +85°C	SA556-1N
14-Pin Cerdip	−55°C to +125°C	SE556F
14-Pin Plastic DIP	−55°C to +125°C	SE556N
14-Pin Plastic DIP	−55°C to +125°C	SE556CN
14-Pin Cerdip	−55°C to +125°C	SE556-1F
14-Pin Plastic DIP	−55°C to +125°C	SE556-1N
14-Pin Cerdip	−55°C to +125°C	SE556-1CF
14-Pin Plastic DIP	−55°C to +125°C	SE556-1CN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage NE/SA556, 556-1, SE556C, SE556-1C SE556-1, SE556	 +16 +18	 V V
P_D	Maximum allowable power dissipation[1]	800	mW
T_A	Operating temperature range NE556-1, NE556 SA556-1, SA556 SE556-1, SE556-1C, SE556, SE556C	 0 to +70 −40 to +85 −55 to +125	 °C °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTE:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the N and F packages. At ambient temperatures above 25°C, where this limit would be exceeded, the Maximum Allowable Power Dissipation must be derated by the following:
   D package 115 °C/W
   N package 80 °C/W
   F package 100 °C/W

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE556/556-1			NE/SA556/SE556C NE556-1/SE556-1C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	$V_{CC} = 5V$, $R_L = \infty$ $V_{CC} = 15V$, $R_L = \infty$		6 20	10 24		6 20	12 30	mA mA
t_M $\Delta t_M/\Delta T$ $\Delta t_M/\Delta V_S$	Timing error (monostable) Initial accuracy[2] Drift with temperature Drift with supply voltage	$R_A = 2k\Omega$ to $100k\Omega$ $C = 0.1\mu F$ $T = 1.1\ RC$		 0.5 30 0.05	 100 0.2		 0.75 50 0.1	 3.0 150 0.5	 % ppm/°C %/V
t_A $\Delta t_A/\Delta T$ $\Delta t_A/\Delta V_S$	Timing error (astable) Initial accuracy[2] Drift with temperature Drift with supply voltage	R_A, $R_B = 1k\Omega$ to $100k\Omega$ $C = 0.\mu F$ $V_{CC} = 15V$		 4 400 0.15	 6 500 0.6		 5 400 0.3	 13 500 1	 % ppm/°C %/V
V_C	Control voltage level	$V_{CC} = 15V$ $V_{CC} = 5V$	9.6 2.9	10.0 3.33	10.4 3.8	9.0 2.6	10.0 3.33	11.0 4.0	V V
V_{TH}	Threshold voltage	$V_{CC} = 15V$ $V_{CC} = 5V$	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	V V
I_{TH}	Threshold current[3]			30	250		30	250	nA
V_{TRIG}	Trigger voltage	$V_{CC} = 15V$ $V_{CC} = 5V$	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67	5.6 2.2	V V
I_{TRIG}	Trigger current	$V_{TRIG} = 0V$		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[5]		0.4	0.7	1.0	0.4	0.7	1.0	V
I_{RESET}	Reset current Reset current	$V_{RESET} = 0.4V$ $V_{RESET} = 0V$	0.4	0.1 0.4	0.4 1.0	0.4	0.1 0.4	0.6 1.5	mA mA
V_{OL}	Output voltage (low)	$V_{CC} = 15V$ $I_{SINK} = 10mA$ $I_{SINK} = 50mA$		0.1 0.4	0.15 0.5		0.1 0.4	0.25 0.75	V V
	SE556 SE556-1 NE/SA556/SE556C NE556-1/SE556-1C	$I_{SINK} = 100mA$		2.0 0.8	2.25 1.2		 2.0 2.0	 3.2 2.5	V V V V

ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE556/556-1			NE/SA556/SE556C NE556-1/SE556-1C			UNIT
			Min	Typ	Max	Min	Typ	Max	
		$I_{SINK} = 200mA$ $V_{CC} = 5V$ $I_{SINK} = 8mA$ $I_{SINK} = 5mA$		2.5 0.1 0.05	 0.2 0.15		2.5 0.25 0.15	 0.3 0.25	V V V
V_{OH}	Output voltage (high)	$V_{CC} = 15V$ $I_{SOURCE} = 200mA$ $I_{SOURCE} = 100mA$ $V_{CC} = 5V$ $I_{SOURCE} = 100mA$	 13.0 3.0	12.5 13.3 3.3	 	 12.75 2.75	12.5 13.3 3.3	 	V V V
t_{OFF}	Turn-off time[6] NE556-1/SE556-1/SE556-1C	$V_{RESET} = V_{CC}$		0.5	2.0		0.5		μs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA
	Matching characteristics[4] Initial accuracy[2] Drift with temperature Drift with supply voltage			 0.5 10 0.1	 1.0 0.2		 1.0 ±10 0.2	 2.0 0.5	 % ppm/°C %/V

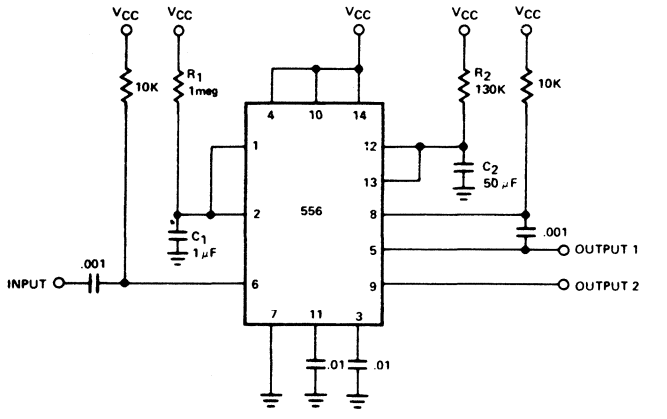
NOTES:

1. Supply current when output is high is typically 1.0mA less.
2. Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
3. This will determine maximum value of $R_A + R_B$. For 15V operation, the max total $R = 10M\Omega$, and for 5V operation, the maximum total $R = 3.4M\Omega$.
4. Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high. In order to guarantee reset the voltage at reset pin must be less than or equal to 0.4V. To disable reset function, the voltage at reset pin has to be greater than 1V.
6. Time measured from a positive-going input pulse from 0 to 0.4 V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL APPLICATIONS

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a 0.001μF coupling capacitor sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay.

The first half of the timer is started by momentarily connecting Pin 6 to ground. When it is timed out (determined by $1.1R_1C_1$) the second half begins. Its duration is determined by $1.1R_2C_2$.

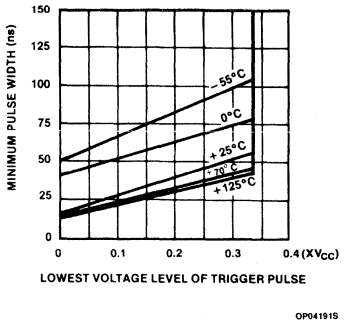


NOTE:
All resistor values are in Ω.

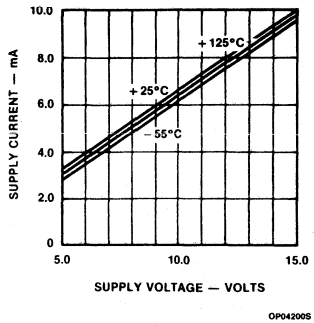
Sequential Timer

TYPICAL PERFORMANCE CHARACTERISTICS

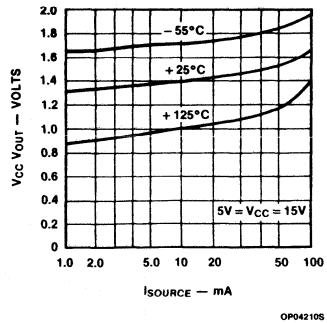
Minimum Pulse Width Required for Triggering



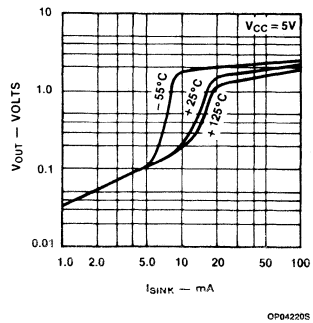
Supply Current vs Supply Voltage



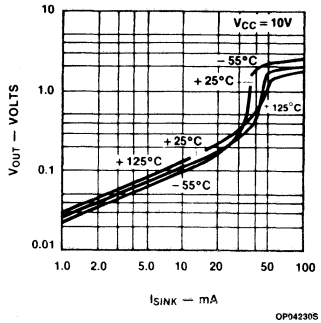
High Output Voltage Drop vs Output Source Current



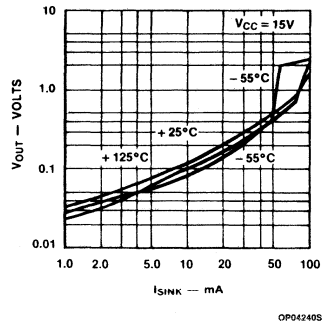
Low Output Voltage vs Output Sink Current



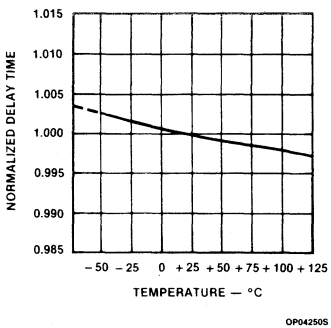
Low Output Voltage vs Output Sink Current



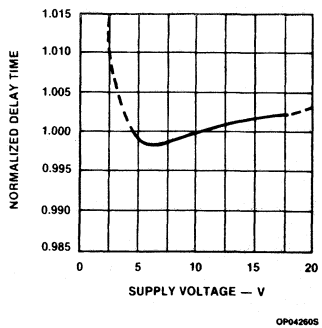
Low Output Voltage vs Output Sink Current



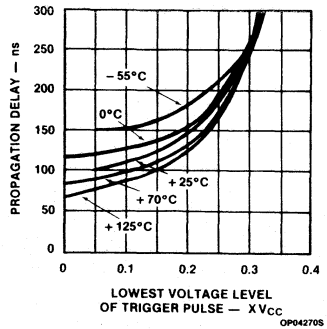
Delay Time vs Temperature



Delay Time vs Supply Voltage



Propagation Delay vs Voltage Level of Trigger Pulse



NE/SA/SE558
Quad Timer

Product Specification

DESCRIPTION

The 558 Quad Timers are monolithic timing devices which can be used to produce four independent timing functions. The 558 output sinks current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays; from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. A stable operation can be achieved by using two of the four timer sections.

The four timer sections in the 558 are edge-triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100mA is provided in both devices.

FEATURES

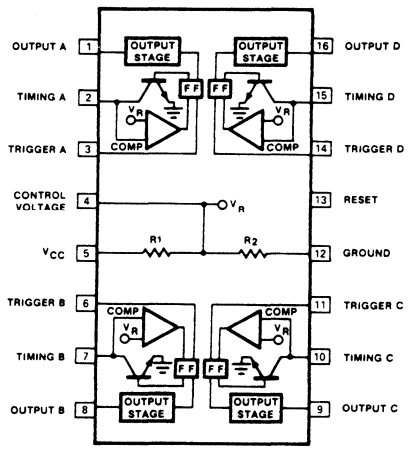
- **100mA output current per section**
- **Edge-triggered (no coupling capacitor)**
- **Output independent of trigger conditions**
- **Wide supply voltage range 4.5V to 18V**
- **Timer intervals from microseconds to hours**
- **Time period equals RC**
- **Military qualifications pending**

APPLICATIONS

- **Sequential timing**
- **Time delay generation**
- **Precision timing**
- **Industrial controls**
- **Quad one-shot**

PIN CONFIGURATION

D[1] F, N Packages



TOP VIEW

CD11140S

NOTE:
1. SOL released in large SO package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE558D
16-Pin Cerdip	0 to +70°C	NE558F
16-Pin Plastic DIP	0 to +70°C	NE558N
16-Pin Cerdip	−40°C to +85°C	SA558F
16-Pin Plastic DIP	−40°C to +85°C	SA558N
16-Pin Cerdip	−55°C to +125°C	SE558F
16-Pin Plastic DIP	−55°C to +125°C	SE558N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	NE/SA558	+16	V
	SE558	+18	V
P_D	Maximum power dissipation T_A = 25°C ambient (still-air)[1]		
	F package	1190	mW
	N package	1450	mW
	D package	1090	mW
T_A	Operating ambient temperature range		
	NE558	0 to +70	°C
	SA558	−40 to +85	°C
	SE558	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

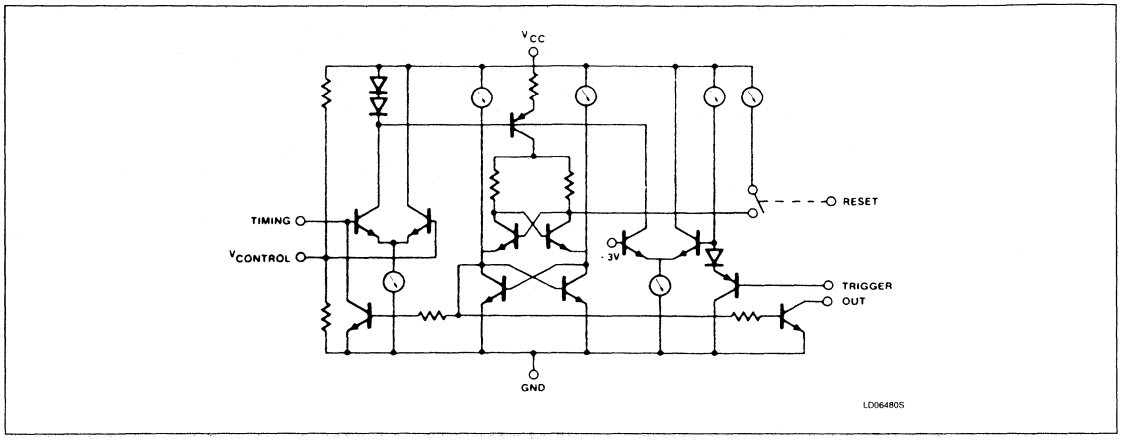
NOTE:
1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.6mW/°C
   D package at 8.7mW/°C

DC AND AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE558			NE/SA558			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current	V_{CC} = Reset = 15V		16	32		16	36	mA
	Timing accuracy (t = RC)	R = 2kΩ to 100kΩ, C = 1μF							
t_A	Initial accuracy			±1.0	3		±2	5	%
$\Delta t_A/\Delta T$	Drift with temperature			30	100		30	150	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.1	0.9		0.1	0.9	%/V
V_{TRIG}	Trigger voltage[1]	V_{CC} = 15V	0.8		2.4	0.8		2.4	V
I_{TRIG}	Trigger current	Trigger = 0V		5	30		5	100	μA
V_{RESET}	Reset voltage[2]		0.8		2.4	0.8		2.4	V
I_{RESET}	Reset current	Reset		50	300		50	500	μA
V_{TH}	Threshold voltage			0.63			0.63		× V_{CC}
	Threshold leakage			15			15		nA
V_{OUT}	Output voltage[3]	I_L = 10mA		0.1	0.2		0.1	0.4	V
		I_L = 100mA		0.7	1.5		1.0	2.0	V
	Output leakage			10	500		10	500	nA
t_{PD}	Propagation delay			1.0			1.0		μs
t_R	Rise time of output	I_L = 100mA		100			100		ns
t_F	Fall time of output	I_L = 100mA		100			100		ns

NOTES:
1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset, the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8V, outputs set low and trigger inhibited. For reset above 2.4V, trigger enabled.
3. The 558 output structure is open-collector which requires a pull-up resistor to V_{CC} to sink current. The output is normally low sinking current.

558 EQUIVALENT CIRCUIT



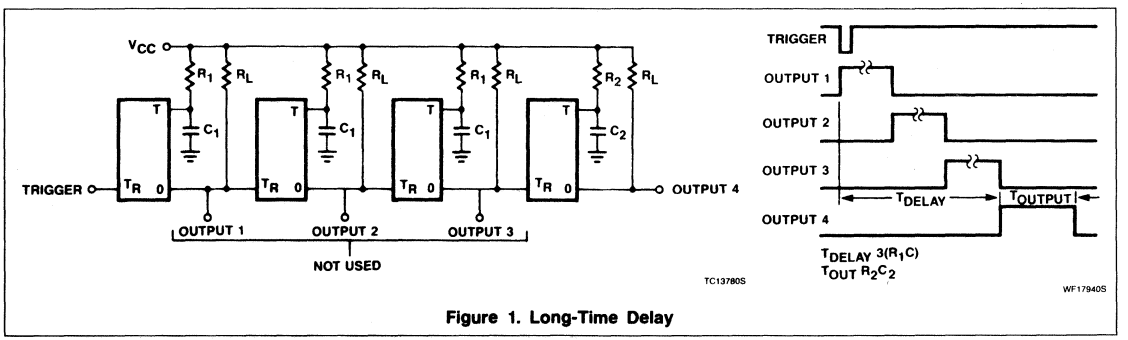
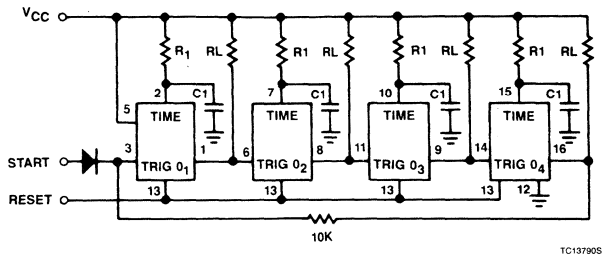
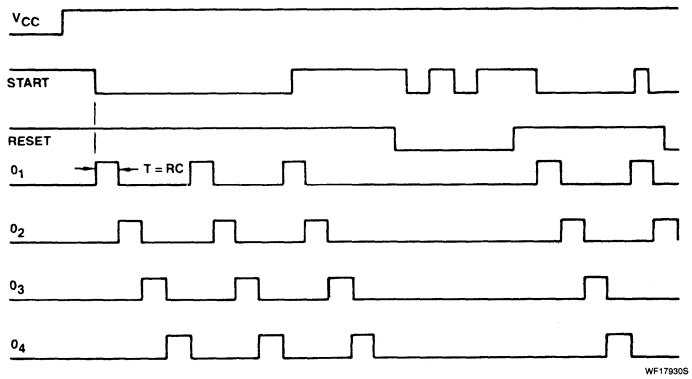


Figure 1. Long-Time Delay



a. Ring Counter



b. Expected Waveforms

Figure 2

AN170
NE555 and NE556 Applications

Application Note

INTRODUCTION

In mid 1972, Signetics introduced the 555 timer, a unique functional building block that has enjoyed unprecedented popularity. The timer's success can be attributed to several inherent characteristics foremost of which are versatility, stability and low cost. There can be no doubt that the 555 timer has altered the course of the electronics industry with an impact not unlike that of the IC operational amplifier.

The simplicity of the timer, in conjunction with its ability to produce long time delays in a variety of applications, has lured many designers from mechanical timers, op amps, and various discrete circuits into the ever increasing ranks of timer users.

DESCRIPTION

The 555 timer consists of two voltage comparators, a bistable flip-flop, a discharge transistor, and a resistor divider network. To understand the basic concept of the timer let's first examine the timer in block form as in Figure 1.

The resistive divider network is used to set the comparator levels. Since all three resistors are of equal value, the threshold comparator is referenced internally at $\frac{2}{3}$ of supply voltage level and the trigger comparator is referenced at $\frac{1}{3}$ of supply voltage. The outputs of the comparators are tied to the bistable flip-flop. When the trigger voltage is moved below $\frac{1}{3}$ of the supply, the comparator changes state and sets the flip-flop driving the output to a high state. The threshold pin normally monitors the capacitor voltage of the RC timing network. When the capacitor voltage exceeds $\frac{2}{3}$ of the supply, the threshold comparator resets the flip-flop which in turn drives the output to a low state. When the output is in a low state, the discharge transistor is "on", thereby discharging the external timing capacitor. Once the capacitor is discharged, the timer will await another trigger pulse, the timing cycle having been completed.

The 555 and its complement, the 556 Dual Timer, exhibit a typical initial timing accuracy of 1% with a 50ppm/°C timing drift with temperature. To operate the timer as a one-shot, only two external components are necessary; resistance & capacitance. For an oscillator, only one additional resistor is necessary. By proper selection of external components, oscillating frequencies from one cycle per half hour to 500kHz can be realized. Duty cycles can be adjusted from less than one percent to 99 percent over the frequency spectrum. Voltage control of timing and oscillation functions is also available.

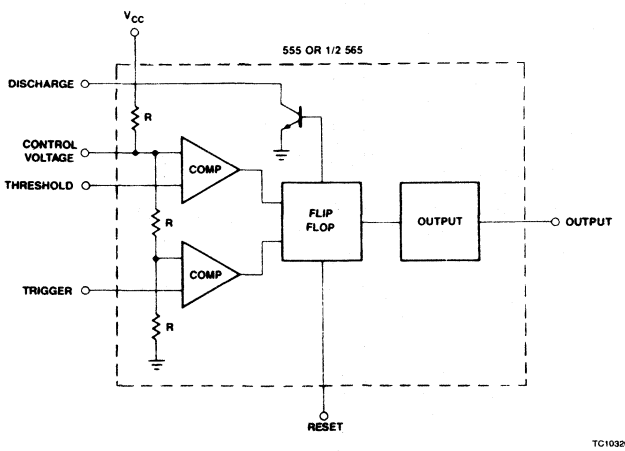


Figure 1. 555/556 Timer Functional Block Diagram

Timer Circuitry

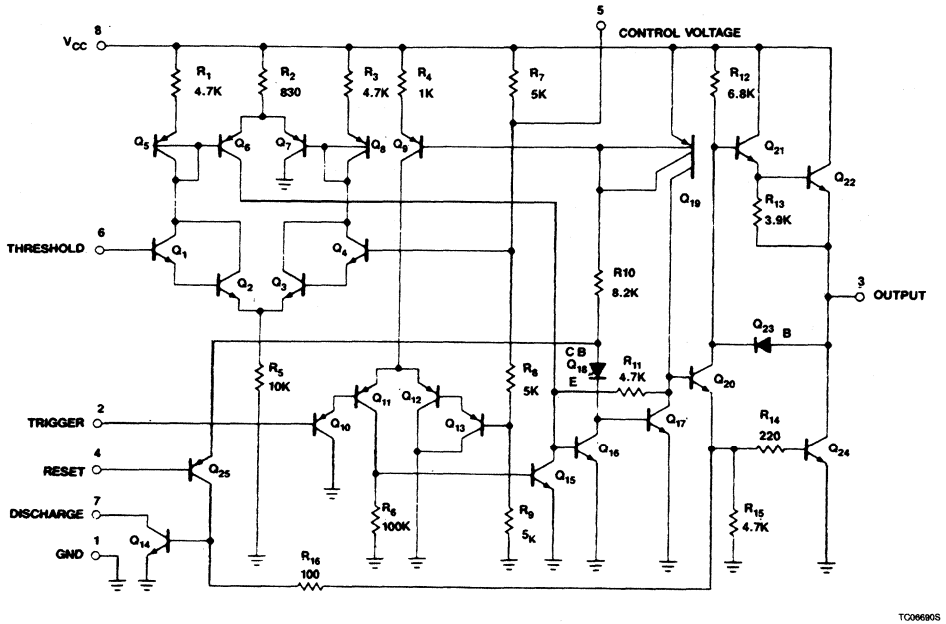
The timer is comprised of five distinct circuits: two voltage comparators; a resistive voltage divider reference; a bistable flip-flop; a discharge transistor; and an output stage that is the "totem-pole" design for sink or source capability. $Q_{10} - Q_{13}$ comprise a Darlington differential pair which serves as a trigger comparator. Starting with a positive voltage on the trigger, Q_{10} and Q_{11} turn on when the voltage at Pin 2 is moved below one third of the supply voltage. The voltage level is derived from a resistive divider chain consisting of R_7, R_8 and R_9. All three resistors are of equal value (5kΩ). At 15V supply, the triggering level would be 5V. When Q_{10} and Q_{11} turn on, they provide a base drive for Q_{15}, turning it on. Q_{16} and Q_{17} form a bistable flip-flop. When Q_{15} is saturated, Q_{16} is 'off' and Q_{17} is saturated. Q_{16} and Q_{17} will remain in these states even if the trigger is removed and Q_{15} is turned 'off'. While Q_{17} is saturated, Q_{20} and Q_{14} are turned off.

The output structure of the timer is a "totem-pole" design, with Q_{22} and Q_{24} being large geometry transistors capable of providing 200mA with a 15V supply. While Q_{20} is 'off', base drive is provided for Q_{22} by Q_{21}, thus providing a high output.

For the duration that the output is in a high state, the discharge transistor is 'off'. Since the collector of Q_{14} is typically connected to the external timing capacitor, C, while Q_{14} is off, the timing capacitor now can charge through the timing resistor, R_A.

The capacitor voltage is monitored by the threshold comparator ($Q_1 - Q_4$) which is a Darlington differential pair. When the capacitor voltage reaches two thirds of the supply voltage, the current is directed from Q_3 and Q_4 thru Q_1 and Q_2. Amplification of the current change is provided by Q_5 and Q_6. $Q_5 - Q_6$ and $Q_7 - Q_8$ comprise a diode-biased amplifier. The amplified current change from Q_6 now provides a base drive for Q_{16} which is part of the bistable flip-flop, to change states. In doing so, the output is driven "low", and Q_{14}, the discharge transistor, is turned "on", shorting the timing capacitor to ground.

The discussion to this point has only encompassed the most fundamental of the timer's operating modes and circuitry. Several points of the circuit are brought out to the real world which allow the timer to function in a variety of modes. It is essential that one understands



NOTE:
All resistor values are in ohms.

Figure 2. Schematic of 555 or ½ 556 Dual Timer

all the variations possible in order to utilize this device to its fullest extent.

Reset Function

Regressing to the trigger mode, it should be noted that once the device has triggered and the bistable flip-flop is set, continued triggering will not interfere with the timing cycle. However, there may come a time when it is necessary to interrupt or halt a timing cycle. This is the function that the reset accomplishes.

In the normal operating mode the reset transistor, Q_{25}, is off with its base held high. When the base of Q_{25} is grounded, it turns on, providing base drive to Q_{14}, turning it on. This discharges the timing capacitor, resets the flip-flop at Q_{17}, and drives the output low. The reset overrides all other functions within the timer.

Trigger Requirements

Due to the nature of the trigger circuitry, the timer will trigger on the negative-going edge of the input pulse. For the device to time-out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the timeout period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger (see Figure 3), a short negative-going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Control Voltage

One additional point of significance, the control voltage, is brought out on the timer. As mentioned earlier, both the trigger comparator, $Q_{10} - Q_{13}$, and the threshold comparator, $Q_1 - Q_4$, are referenced to an internal resistor divider network, R_7, R_8, R_9. This network establishes the nominal two thirds of supply voltage (V_{CC}) trip point for the threshold comparator and one third of V_{CC} for the trigger comparator. The two thirds point at the junction of R_7, R_8 and the base of Q_4 is brought out. By imposing a voltage at this point, the comparator reference levels may be shifted either higher or lower than the nominal levels of one third and two thirds of the supply voltage. Varying the voltage at this point will vary the timing. This feature of the timer opens a multitude of application possibilities such as using the timer as a voltage-controlled oscillator, pulse-width modulator, etc. For applications where the control voltage function is not used, it is strongly recommended that a bypass capacitor (0.01μF) be placed across the control voltage pin and ground. This will increase the noise immunity of the timer to high frequency trash which may monitor the threshold levels causing timing error.

Monostable Operation

The timer lends itself to three basic operating modes:

1. Monostable (one-shot)
2. Astable (oscillatory)
3. Time delay

By utilizing one or any combination of basic operating modes and suitable variations, it is possible to utilize the timer in a myriad of applications. The applications are limited only to the imagination of the designer.

One of the simplest and most widely used operating modes of the timer is the monostable (one-shot). This configuration requires only two external components for operation (see Figure 4). The sequence of events starts when a voltage below one third V_{CC} is sensed by the trigger comparator. The trigger is normally applied in the form of a short negative-going pulse. On the negative-going edge of the pulse, the device triggers, the output goes high and the discharge transistor turns off. Note that prior to the input pulse, the discharge transistor is on, shorting the timing capacitor to ground. At this point the timing capacitor, C, starts charging through the timing resistor, R. The voltage on the capacitor increases exponentially with a time constant T = RC. Ignoring capacitor leakage, the capacitor will reach the two thirds V_{CC} level in 1.1 time constants or

$$T = 1.1\ RC \qquad (1)$$

Where T is in seconds, R is in ohms, and C is in Farads. This voltage level trips the threshold comparator, which in turn drives the output low and turns on the discharge transistor. The transistor discharges the capacitor, C, rapidly. The timer has completed its cycle and will now await another trigger pulse.

Astable Operation

In the astable (free-run) mode, only one additional component, R_B, is necessary. The trigger is now tied to the threshold pin. At power-up, the capacitor is discharged, holding the trigger low. This triggers the timer, which establishes the capacitor charge path through R_A and R_B. When the capacitor reaches the threshold level of $^2/_3$ V_{CC}, the output drops low and the discharge transistor turns on.

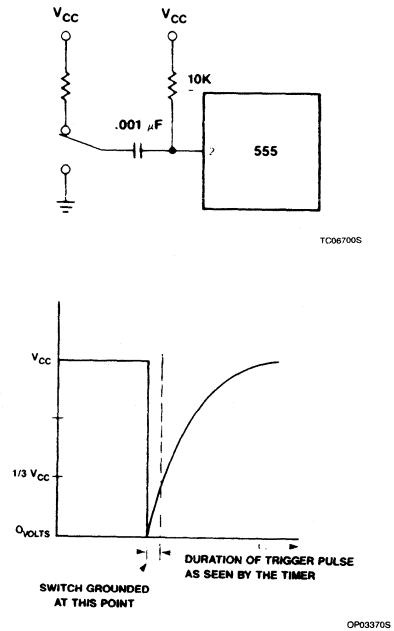


Figure 3. AC Coupling of the Trigger Pulse

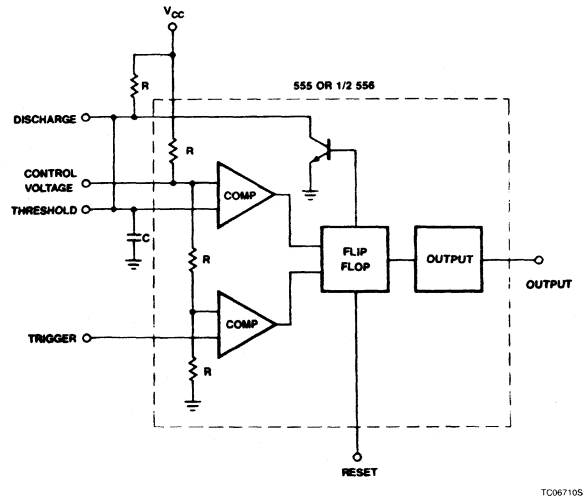


Figure 4. Monostable Operation

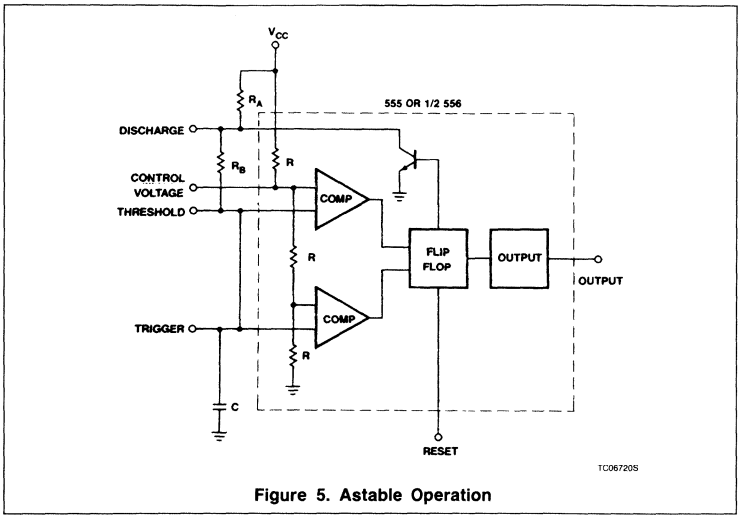


Figure 5. Astable Operation

The timing capacitor now discharges through R_B. When the capacitor voltage drops to $\frac{1}{3}$ V_{CC}, the trigger comparator trips, automatically retriggering the timer, creating an oscillator whose frequency is given by:

$$f = \frac{1.49}{(R_A + 2R_B)\,C} \qquad (2)$$

Selecting the ratios of R_A and R_B varies the duty cycle accordingly. Lo and behold, we have a problem. If a duty cycle of less than fifty percent is required, then what? Even if $R_A = 0$, the charge time cannot be made smaller than the discharge time because the charge path is $R_A + R_B$ while the discharge path is R_B alone. In this case it becomes necessary to insert a diode in parallel with R_B, cathode toward the timing capacitor. Another diode is desirable, but not mandatory (this one in series with R_B), cathode away from the timing capacitor. Now the charge path becomes R_A, through the parallel diode into C. Discharge is through the series diode and R_B to the discharge transistor. This scheme will afford a duty cycle range from less than 5% to greater than 95%. It should be noted that for reliable operation a minimum value of 3kΩ for R_B is recommended to assure that oscillation begins.

Time Delay

In this third basic operating mode, we aim to accomplish something a little different from monostable operation. In the monostable mode, when a trigger was applied,

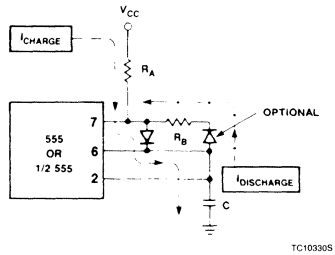


Figure 6. Method of Achieving Duty Cycles Less Than 50%

immediately changed to the high state, timed out, and returned to its pre-trigger low state. In the time delay mode, we require the output not to change state upon triggering, but at some precalculated time after trigger is received.

The threshold and trigger are tied together, monitoring the capacitor voltage. The discharge function is not used. The operation sequence begins as transistor (T_1) is turned on, keeping the capacitor grounded. The trigger sees a low state and forces the timer output high. When the transistor is turned off, the capacitor commences its charge cycle. When the capacitor reaches the threshold level, only then does the output change from its normally high state to the low state. The output will remain low until T_1 is again turned on.

GENERAL DESIGN CONSIDERATIONS

The timer will operate over a guaranteed voltage range of 4.5V to $15V_{DC}$ with $16V_{DC}$ being the absolute maximum rating. Most of the devices, however, will operate at voltage levels as low as $3V_{DC}$. The timing interval is independent of supply voltage since the charge rate and threshold level of the comparator are both directly proportional to supply. The supply voltage may be provided by any number of sources, however, several precautions should be taken. The most important, the one which provides the most headaches if not practiced, is good power supply filtering and adequate bypassing. Ripple on the supply line can cause loss of timing accuracy. The threshold level shifts, causing a change of charging current. This will cause a timing error for that cycle.

Due to the nature of the output structure, a high power totem-pole design, the output of the timer can exhibit large current spikes on the supply line. Bypassing is necessary to eliminate this phenomenon. A capacitor across the V_{CC} and ground, directly across the device, is necessary and ideal. The size of a capacitor will depend on the specific application. Values of capacitance from 0.01μF to 10μF are not uncommon, but note that the bypass capacitor would be as close to the device as physically possible.

Selecting External Components

In selecting the timing resistor and capacitor, there are several considerations to be taken into account.

Stable external components are necessary for the RC network if good timing accuracy is to be maintained. The timing resistor(s) should be of the metal film variety if timing accuracy and repeatability are important design criteria. The timer exhibits a typical initial accuracy of one percent. That is, with any one RC network, from timer to timer only one percent change is to be expected. Most of the initial timing error (i.e., deviation from the formula) is due to inaccuracies of external components. Resistors range from their rated values by 0.01% to 10% and 20%. Capacitors may have a 5% to 10% deviation from rated capacity. Therefore, in a system where

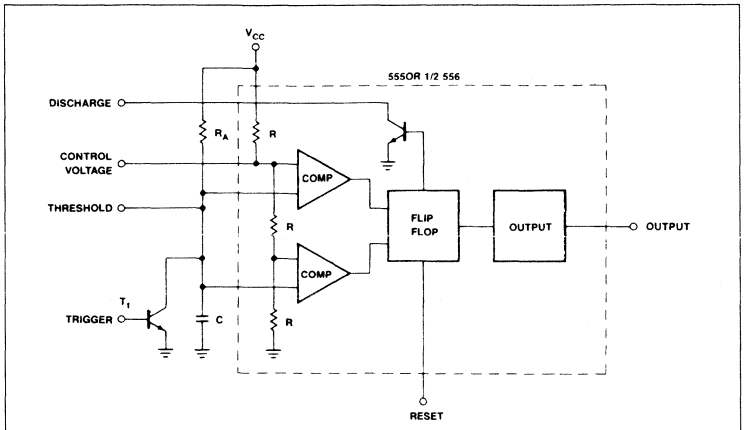


Figure 7. Time Delay Operation

timing is critical, an adjustable timing resistor or precision components are necessary. For best results, a good quality trim pot, placed in series with the largest feasible resistance, will allow for best adjustability and performance.

The timing capacitor should be a high quality, stable component with very low leakage characteristics. *Under no circumstances should ceramic disc capacitors be used in the timing network!* Ceramic disc capacitors are not sufficiently stable in capacitance to operate properly in an RC mode. Several acceptable capacitor types are: silver mica, mylar, polycarbonate, polystyrene, tantalum, or similar types.

The timer typically exhibits a small negative temperature coefficient (50ppm/°C). If timer accuracy over temperature is a consideration, timing components with a small positive temperature coefficient should be chosen. This combination will tend to cancel timing drift due to temperature.

In selecting the values for the timing resistors and capacitor, several points should be considered. A minimum value of threshold current is necessary to trip the threshold comparator. This value is 0.25μA. To calculate the maximum value of resistance, keep in mind that at the time the threshold current is required, the voltage potential on the threshold pin is two thirds of supply. Therefore:

$$V_{potential} = V_{CC} - V_{capacitor}$$

$$V_{potential} = V_{CC} - \tfrac{2}{3}\ V_{CC} = \tfrac{1}{3}V_{CC}$$

Maximum resistance is then defined as

$$R_{MAX} = \frac{V_{CC} - V_{cap}}{I_{thresh}} \qquad (3)$$

Example: $V_{CC} = 15V$

$$R_{MAX} = \frac{15 - 10}{0.25(10^{-6})} = 20M\Omega$$

$V_{CC} = 5V$

$$R_{MAX} = \frac{5 - 3.33}{0.25(10^{-6})} \quad 6.6M\Omega$$

NOTE:
If using a large value of timing resistor, be certain that the capacitor leakage is significantly lower than the charging current available to minimize timing error.

On the other end of the spectrum, there are certain minimum values of resistance that should be observed. The discharge transistor, Q_{14}, is current-limited at 35mA to 55mA internally. Thus, at the current limiting values, Q_{14} establishes high saturation voltages. When examining the currents at Q_{14}, remember that the transistor, when turned on, will be carrying two current loads. The first being the constant current through timing resistor, R_A. The second will be the varying discharge current from the timing capacitor. To provide best operation, the current contributed by the R_A path should be minimized so that the majority of discharge current can be used to reset the capacitor voltage. Hence it is recommended that a 5kΩ value be the minimum feasible value for R_A. This does not mean lower values cannot be used successfully in certain applications, yet there are extreme cases that should be avoided if at all possible.

Capacitor size has not proven to be a legitimate design criteria. Values ranging from picofarads to greater than one thousand microfarads have been used successfully. One precaution need be utilized, though. (It should be a cardinal rule that applies to the usage of all ICs.) Make certain that the package power dissipation is not exceeded. With extremely large capacitor values, a maximum duty cycle which allows some cooling time for the discharge transistor may be necessary.

The most important characteristic of the capacitor should be as low a leakage as possible. Obviously, any leakage will subtract from the charge count, causing the calculated time to be longer than anticipated.

Control Voltage

Regressing momentarily, we recall that the control voltage pin is connected directly to the threshold comparator at the junction of R_7, or R_8. The combination of R_7, R_8 and R_9 comprises the resistive voltage divider network that establishes the nominal $\frac{1}{3}$ V_{CC} trigger comparator level (junction R_8, R_9) and the $\frac{2}{3}$ V_{CC} level for the threshold comparator (junction R_7, R_8).

For most applications, the control voltage function is not used and therefore is bypassed to ground with a small capacitor for noise filtering. The control voltage function, in other applications, becomes an integral part of the design. By imposing a voltage at this pin, it becomes possible to vary the threshold comparator "set" level above or below the $\frac{2}{3}$ V_{CC} nominal, thereby varying the timing. In the *monostable mode*, the control voltage may be varied from 45% to 90% of V_{CC}. The 45 – 90% figure is not firm, but only an indication to a safe usage. Control voltage levels below and above those stated have been used successfully in some applications.

In the oscillatory (free-run) mode, the control voltage limitations are from 1.7V to V_{CC}. These values should be heeded for reliable operation. Keep in mind that in this mode the trigger level is also important. When the control voltage raises the threshold comparator level, it also raise the trigger comparator level by one-half that amount due to R_8 and R_9 of Figure 2. As a voltage-controlled oscillator, one can expect ±25% around center frequency (f_O) to be virtually linear with a normal RC timing circuit. For wider linear variations around f_O it may be desirable to replace the charging resistor with a constant-current source. In this manner, the exponential charging characteristics of the classical configuration will be altered to linear charge time.

Reset Control

The only remaining function now is the reset. As mentioned earlier, the reset, when taken to ground, inhibits all device functioning. The output is driven low, the bistable flip-flop is reset, and the timing capacitor is discharged. In the astable (oscillatory) mode, the reset can be used to gate the oscillator. In the monostable, it can be used as a timing abort to either interrupt a timing sequence or establish a standby mode (i.e., device off during power-up). It can also be used in conjunction

with the trigger pin to establish a positive edge-triggered circuit as opposed to the normal negative edge-trigger mode. One thing to keep in mind when using the reset function is that the reset voltage (switching) point is between 0.4V and 1.0V (min/max). Therefore, if used in conjunction with the trigger, the device will be out of the reset mode prior to reaching 1V. At that point the trigger is in the "turn on" region, below $\frac{1}{3}$ V_{CC}. This will cause the device to trigger immediately, effectively triggering on the positive-going edge if a pulse is applied to Pins 4 and 2 simultaneously.

FREQUENTLY ASKED APPLICATIONS QUESTIONS

The following is a harvest of various maladies, exceptions, and idiosyncrasies that may exhibit themselves from time to time in various applications. Rather than cast aspersions, a quick review of this list may uncover a solution to the problem at hand.

1. In the oscillator mode when reset is released the *first time constant* is approximately *twice as long as the rest.* Why?
   Answer: In the oscillator mode the capacitor voltage fluctuates between $\frac{1}{2}$ and $\frac{2}{3}$ of the supply voltage. When reset is pulled down, the capacitor discharges completely. Thus for the first cycle it must charge from ground to $\frac{2}{3}$ V_{CC}, which takes twice as long.

2. What is *maximum frequency of oscillations?*
   Answer: Most devices will oscillate about 1MHz. However, in the interest of temperature stability, one should operate only up to about 500kHz.

3. What is *temperature drift* for *oscillator mode?*
   Answer: Temperature drift of oscillator mode is 3 times that of one-shot mode due to the addition of a second voltage comparator. Frequency always increases with an increasing temperature. Therefore it is possible to partially offset this drift with an offsetting temperature coefficient in the external resistor/capacitor combination.

4. Oscillator exhibits spurious *oscillations on crossover points.* Why?
   Answer: The 555 can oscillate due to feedback from power supply. Always bypass with sufficient capacitance close to the device for all applications.

5. Trying to drive a *relay* but 555 *hangs up.* How come?
   Answer: Inductive feedback. A clamp diode across the coil prevents the coil from driving Pin 3 below a negative 0.6V. This negative voltage is sufficient in some cases to cause the timer to malfunction. The solution is to drive the relay through a diode, thus preventing Pin 3 from ever seeing a negative voltage.

6. Double triggering of the TTL loads sometimes occurs. Why?
   Answer: Due to the high current capability and fast rise and fall times of the output, a totem-pole structure different from the TTL classical structure was used. Near TTL threshold this output exhibits a crossover distortion which may double trigger logic. A 1000pF capacitor from the output to ground will eliminate any false triggering.

7. What is the longest time I can get out of the timer?
   Answer: Times exceeding an hour are possible, but not always practical. Large capacitors with low leakage specs are quite expensive. It becomes cheaper to use a countdown scheme (see Figure 15) at some point, dependent on required accuracy. Normally 20 to 30 min. is the longest feasible time.

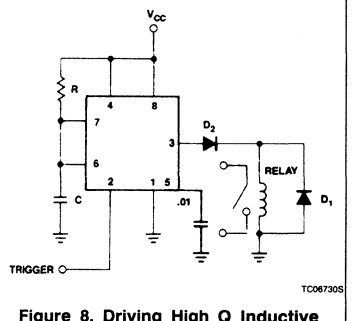


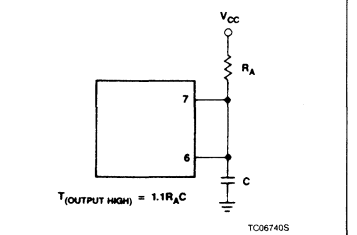
Figure 8. Driving High Q Inductive Loads

DESIGN FORMULAS

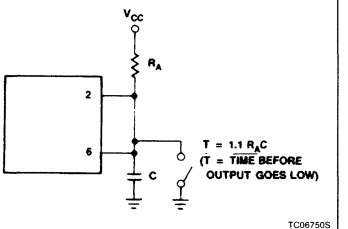
Before entering the section on specific applications it is advantageous to review the timing formulas. The formulas given here apply to the 555 and 556 devices.

APPLICATIONS

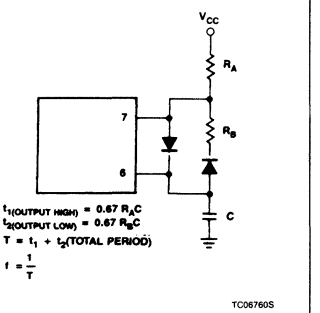
The timer, since introduction, has spurred the imagination of thousands. Thus, the ways in which this device has been used are far too numerous to present each one. A review of the basic operation and basic modes has previously been given. Presented here are some ingenious applications devised by our applications engineers and by some of our customers.



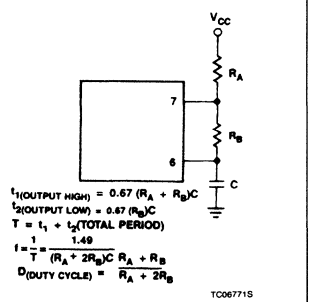
a. Monostable Timing



b. True Time Delay



c. Modified Duty Cycle (Astable)

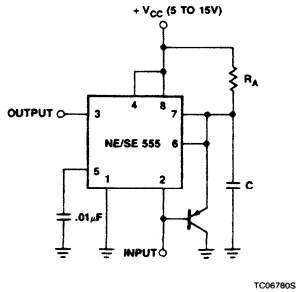


d. Astable Timing

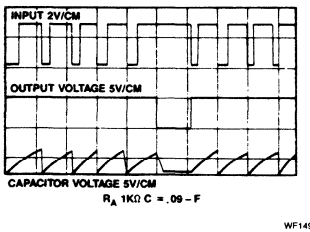
Figure 9

Missing Pulse Detector

Using the circuit of Figure 10a, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure 10b shows the actual waveforms seen in this mode of operation.



a. Schematic Diagram



b. Expected Waveforms

Figure 10

Frequency Divider

If the input frequency is known, the timer can easily be used as a frequency divider by adjusting the length of the timing cycle.

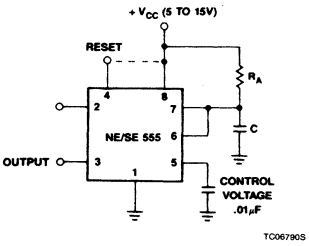


Figure 11a. Schematic Diagram

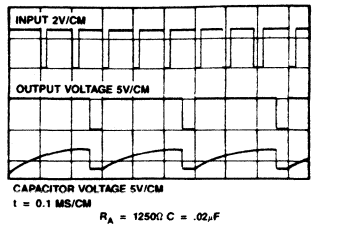
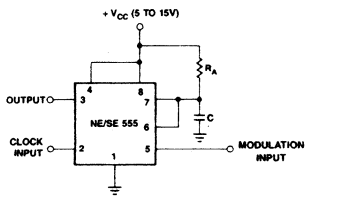


Figure 11b. Expected Waveforms

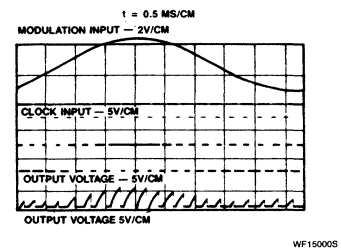
Figure 11b shows the waveforms of the timer in Figure 11a when used as a divide-by-three circuit. This application makes use of the fact that this circuit cannot be retriggered during the timing cycle.

Pulse Width Modulation (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 12a. The circuit is triggered with a continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (Pin 5). This has the effect of modulating the pulse width as the control voltage varies. Figure 12b shows the actual waveform generated with this circuit.



a. Device Schematic

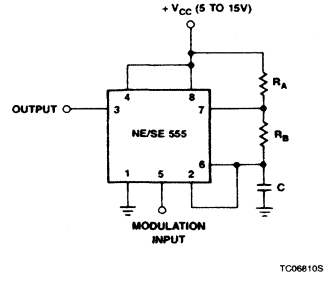


b. Expected Waveforms

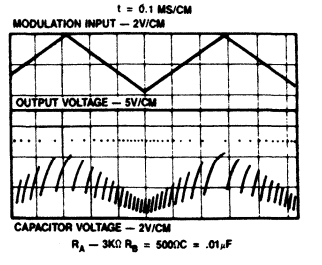
Figure 12

Pulse Position Modulation (PPM)

This application uses the timer connected for astable (free-running) operation, Figure 13a, with a modulating signal again applied to the control voltage terminal. Now the pulse position varies with the modulating signal, since the threshold voltage, and hence the time delay, is varied. Figure 13b shows the waveform generated for triangle-wave modulation signal.

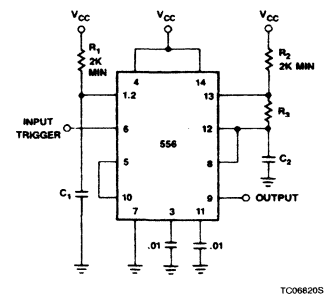


a. Schematic Diagram



b. Expected Waveform

Figure 13



NOTE:
All resistor values are in ohms.

Figure 14. Tone Burst Generator

Tone Burst Generator

The 556 Dual Timer makes an excellent tone burst generator. The first half is connected as a one-shot and the second half as an oscillator (Figure 14).

The pulse established by the one-shot turns on the oscillator, allowing a burst to be generated.

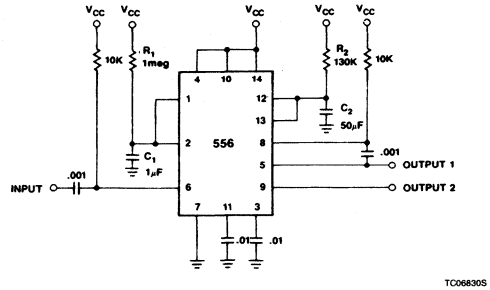
Sequential Timing

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a 0.001μF coupling capacitor, sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay (Figure 15).

The first half of the timer is started by momentarily connecting Pin 6 to ground. When it is timed-out (determined by 1.1 R_1C_1) the second half begins. Its duration is determined by 1.1 R_2C_2.

Long Time Delays

In the 556 timer the timing is a function of the charging rate of the external capacitor. For long time delays, expensive capacitors with extremely low leakage are required. The practicality of the components involved limits the time between pulses to around twenty minutes.



NOTE:
All resistor values are in ohms.

Figure 15. Sequential Timer

To achieve longer time periods, both halves may be connected in tandem with a "divide-by" network in between.

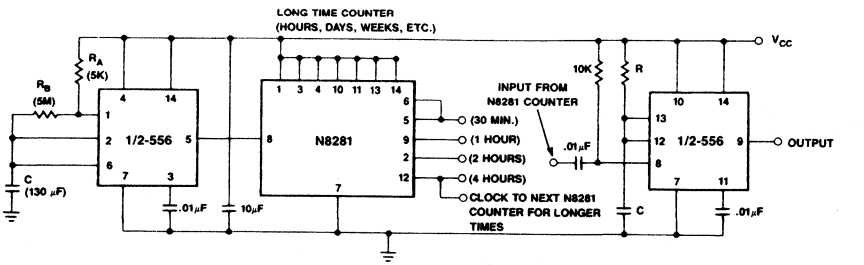
The first timer section operates in an oscillatory mode with a period of $1/f_O$. This signal is then applied to a "divide-by-N" network to give an output with the period of N/f_O. This can then be used to trigger the second half of the 556. The total time is now a function of N and f_O (Figure 16).

Speed Warning Device

Utilizing the "missing pulse detector" concept, a speed warning device, such as depicted, becomes a simple and inexpensive circuit (Figure 17a).

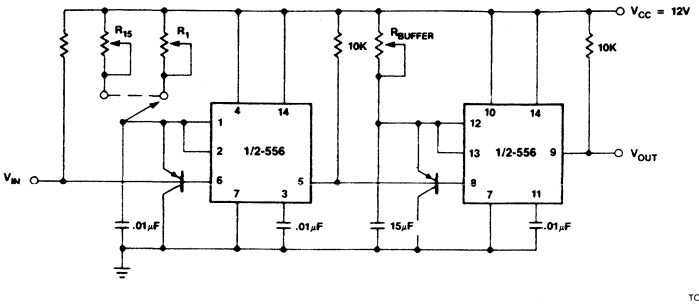
Car Tachometer

The timer receives pulses from the distributor points. Meter M receives a calibrated current thru R_6 when the timer output is high. After time-out, the meter receives no current for that part of the duty cycle. Integration of the variable duty cycle by the meter movement provides a visible indication of engine speed (Figure 18).

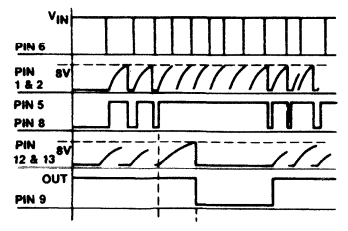


NOTE:
All resistor values are in ohms.

Figure 16. Method of Achieving Long Time Delays

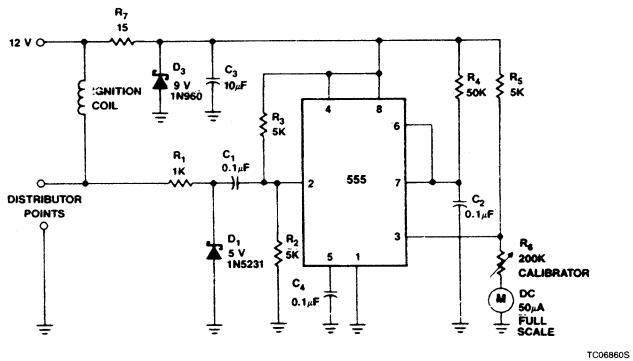


a. Schematic of Speed Warning Device



b. Operating Waveforms Speed Warning Device

Figure 17



NOTE:
All resistor values are in ohms.

Figure 18. Tachometer

Oscilloscope-Triggered Sweep

The 555 timer holds down the cost of adding a triggered sweep to an economy oscilloscope. The circuit's input op amp triggers the timer, setting its flip-flop and cutting off its discharge transistor so that capacitor C can charge. When capacitor voltage reaches the timer's control voltage ($0.33V_{CC}$), the flip-flop resets and the transistor conducts, discharging the capacitor (Figure 19).

Greater linearity can be achieved by substituting a constant-current source for the frequency adjust resistor (R).

Square Wave Tone Burst Generator

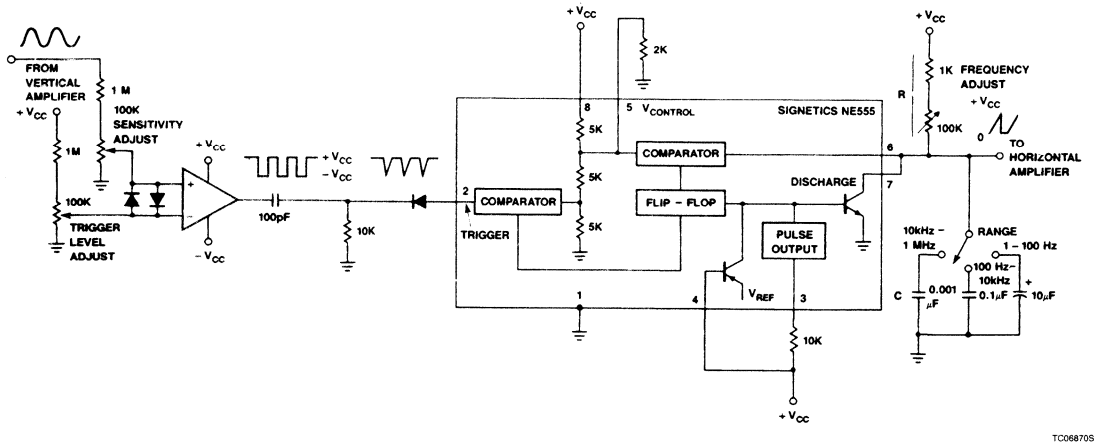
Depressing the pushbutton provides square wave tone bursts whose duration depends on the duration for which the voltage at Pin 4 exceeds a threshold. Components R_1, R_2 and C_1 cause the astable action of the timer IC (Figure 20).

Regulated DC-to-DC Converter

Regulated DC-to-DC converter produces $15V_{DC}$ outputs from a $+5V_{DC}$ input. Line and load regulation is 0.1% (Figure 21).

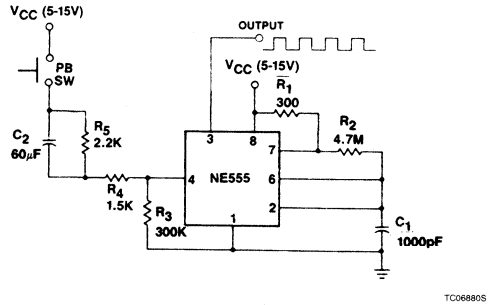
Voltage-to-Pulse Duration Converter

Voltage levels can be converted to pulse durations by combining an op amp and a timer IC. Accuracies to better than 1% can be obtained with this circuit (a), and the output signals (b) still retain the original frequency, independent of the input voltage (Figure 22).



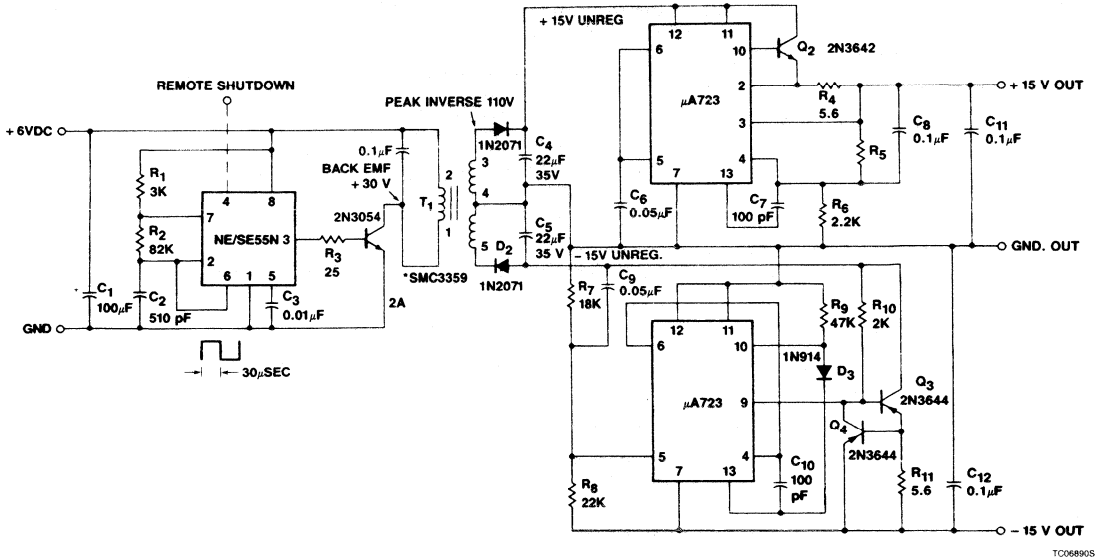
NOTE:
All resistor values are in ohms.

Figure 19. Schematic of Triggered Sweep



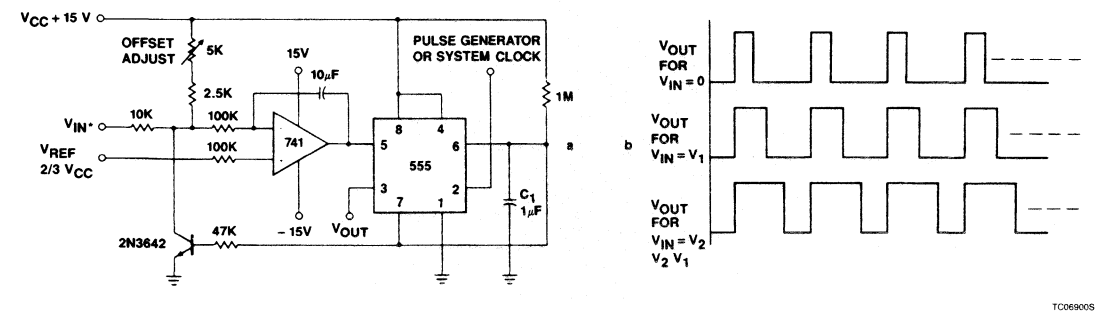
NOTE:
All resistor values are in ohms.

Figure 20. Square Wave Tone Burst Generator



NOTES:
All resistor values are in ohms.
*Shafer Magnetics
Covina, Calif,
(213) 331-3115

Figure 21. Regulated DC-to-DC Converter



NOTES:
All resistor values in ohms
*V_{IN} is limited to 2 diode drops within ground or below V_{CC}

Figure 22. Voltage-to-Pulse Duration Converter

Servo System Controller

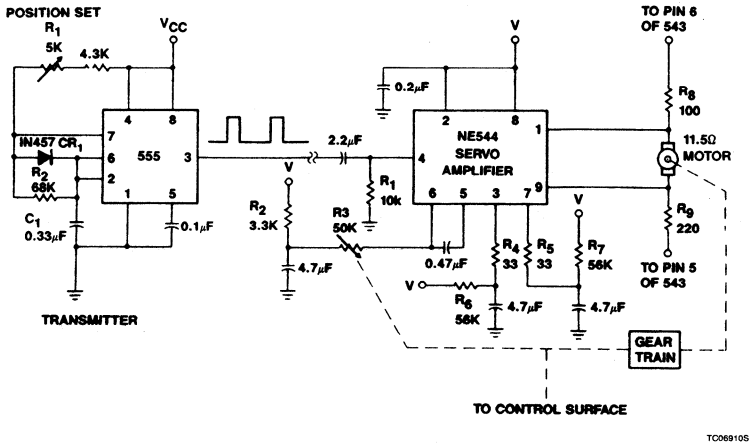
To control a servo motor remotely, the 555 needs only six extra components (Figure 23).

Stimulus Isolator

Stimulus isolator uses a photo-SCR and a toroid for shaping pulses of up to 200V at 200μA (Figure 24).

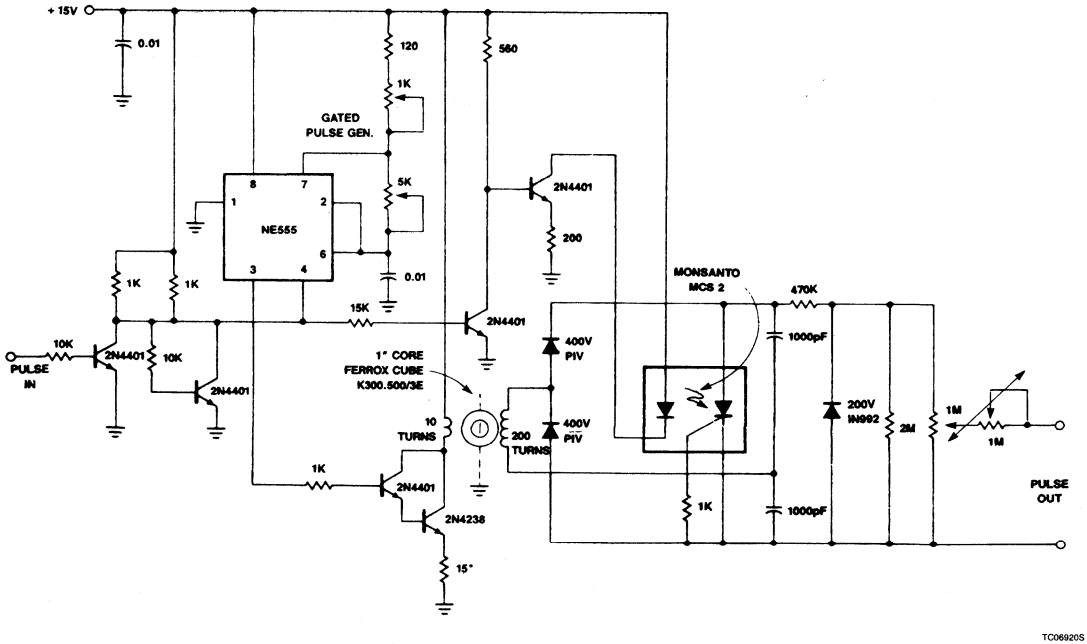
Voltage-to-Frequency Converter (0.2% Accuracy)

Linear voltage-to-frequency converter (a) achieves good linearity over the 0 to −10V range. Its mirror image (b) provides the same linearity over the 0 to +10V range, but is not DTL/TTL compatible (Figure 25).



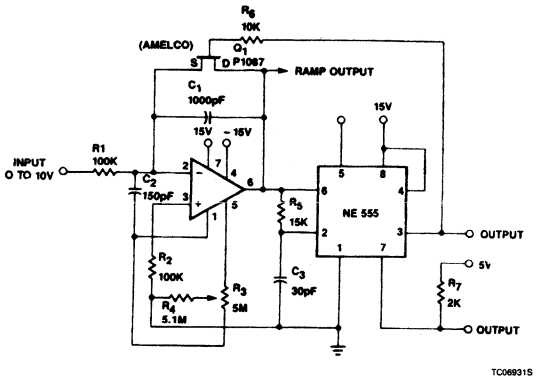
NOTE:
All resistor values in ohms.

Figure 23. Servo System Controller

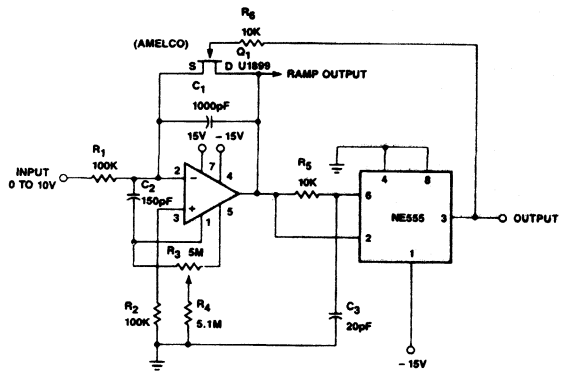


NOTES:
All resistor values in ohms
*Power rating depends on duty cycle from 1/2W for 20-25% duty cycle to 15-20W for 75-90% duty cycle

Figure 24. Stimulus Isolator



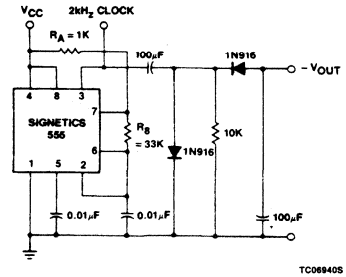
a.



b.

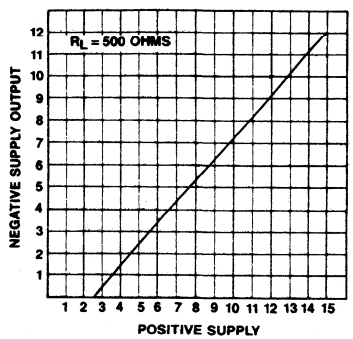
NOTE:
All resistor values in ohms

Figure 25

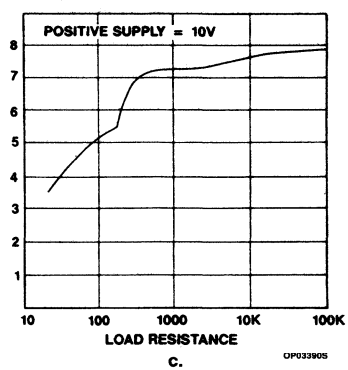


NOTE:
All resistor values are in ohms

a. Positive-to-Negative Converter



b.



c.

Figure 26

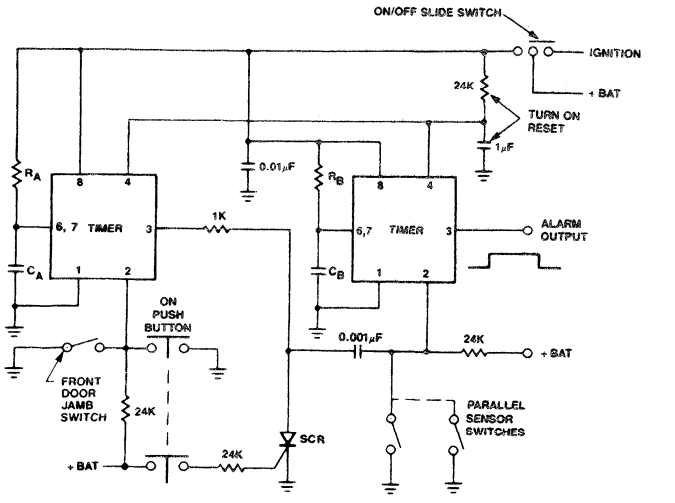
Positive-to-Negative Converter

Transformerless DC – DC converter derives a negative supply voltage from a positive. As a bonus, the circuit also generates a clock signal.

The negative output voltage tracks the DC input voltage linearity (a), but its magnitude is about 3V lower. Application of a 500Ω load, (b), causes 10% change from the no-load value (Figure 26).

Auto Burglar Alarm

Timer A produces a safeguard delay, allowing driver to disarm alarm and eliminating a vulnerable outside control switch. The SCR prevents timer A from triggering timer B, unless timer B is triggered by strategically-located sensor switches (Figure 27).



NOTES:
Timer Signetics NE555
All resistor values in ohms

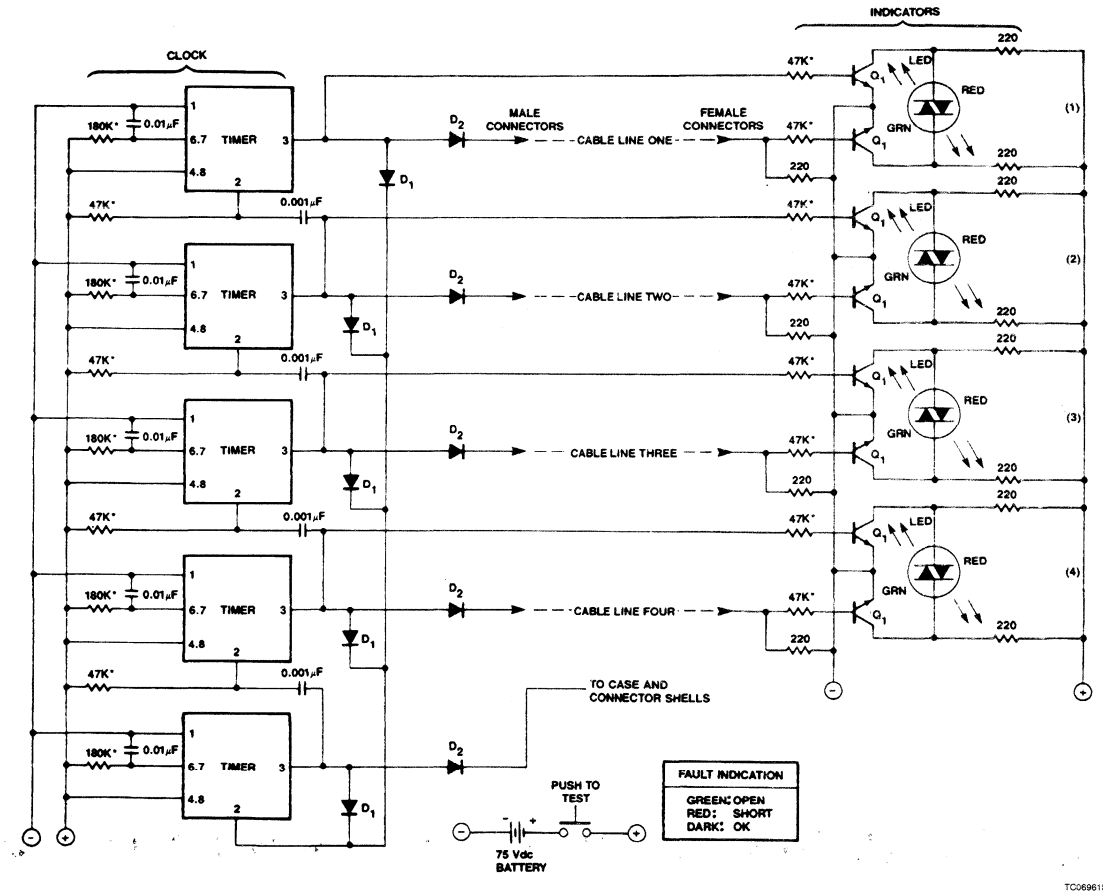
Figure 27. Auto Burglar Alarm

Cable Tester

Compact tester checks cables for open-circuit or short-circuit conditions. A differential transistor pair at one end of each cable line remains balanced as long as the same clock pulse-generated by the timer IC appears at both ends of the line. A clock pulse just at the clock end of the line lights a green light-emitting diode, and a clock pulse only at the other end lights a red LED (Figure 28).

Low Cost Line Receiver

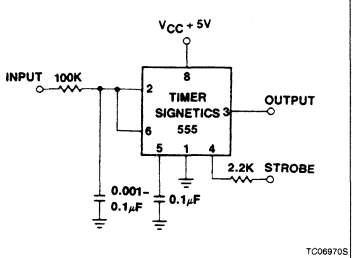
The timer makes an excellent line receiver for control applications involving relatively slow electromechanical devices. It can work without special drivers over single unshielded lines (Figure 29).



NOTES:
D_1 Silicon Signal Diode
D_2 1-A Silicon Diode
Q_1 200mW NPN Silicon, 2N2926 or ½ 2N2903

Timer Signetics NE555V
LED Monsanto MV5491
*½W Resistors

Figure 28. Cable Tester



NOTE:
All resistor values are in ohms.

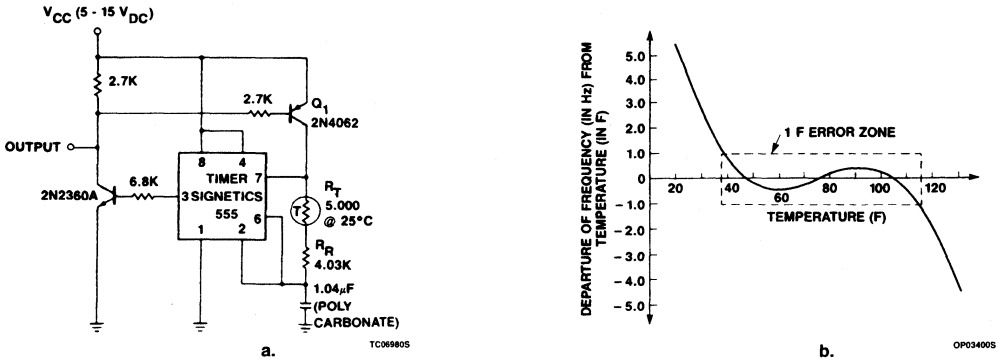
Figure 29. Low Cost Line Receiver

Temperature Control

A couple of transistors and thermistor in the charging network of the 555-type timer enable this device to sense temperature and produce a corresponding frequency output. The circuit is accurate to within ± 1Hz over a 78°F temperature range (Figure 30).

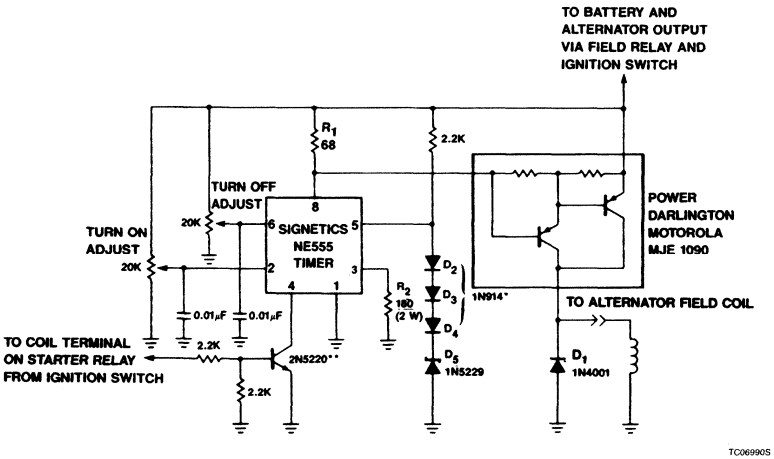
Automobile Voltage Regulator

A monolithic 555-type timer is the heart of this simple automobile voltage regulator. When the timer is off so that its output (Pin 3) is low, the power Darlington transistor pair is off. If battery voltage becomes too low (less than 14.4V in this case), the timer turns on and the Darlington pair conducts (Figure 31).



NOTE:
All resistor values are in ohms.

Figure 30. Temperature Control



NOTES:
* Can be any general purpose Silicon diode or 1N4157 device.
**Can be any general purpose Silicon transistor.
All resistor values are in ohms.

Figure 31. Automobile Voltage Regulator

DC-to-DC Converter

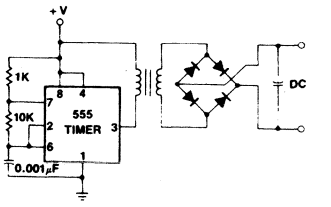


Figure 32. DC-to-DC Converter

Ramp Generator

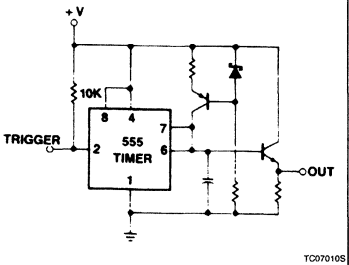


Figure 33. Ramp Generator

Audio Oscillator

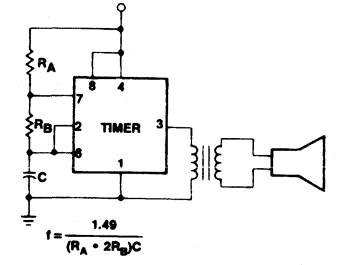


Figure 34. Audio Oscillator

Low Power Monostable Operation

In battery-operated equipment where load current is a significant factor, Figure 35 can deliver 555 monostable operation at low standby power. This circuit interfaces directly with CMOS 4000 series and 74L00 series. During the monostable time, the current drawn is 4.5mA for T = 1.1RC. The rest of the time the current drawn is less than 50μA. (Circuit submitted by Karl Imhof, Executone Inc., Long Island City, NY.)

In other low power operations of the timer where V_{CC} is removed until timing is needed, it is necessary to consider the output load. If the output is driving the base of a PNP transistor, for example, and its power is not removed, it will sink current into Pin 3 to ground and use excessive power. Therefore, when driving these types of loads, one should recall this internal sinking path of the timer.

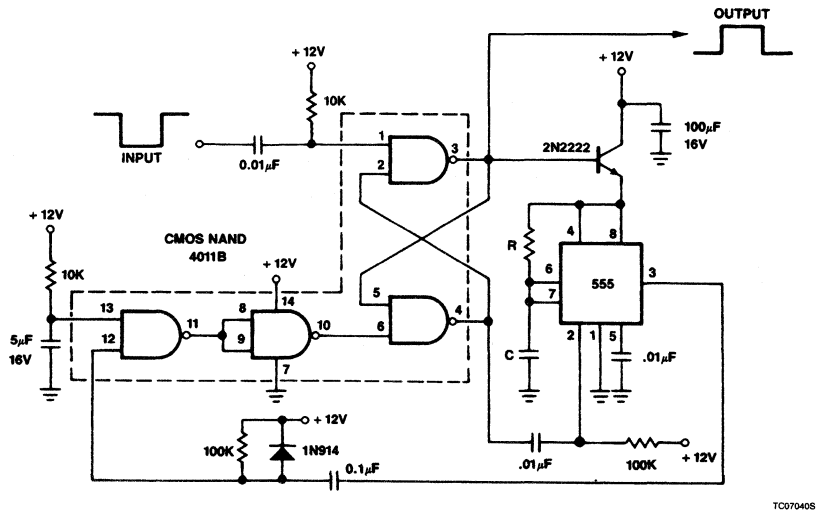


Figure 35. Low Power Monostable

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2. **"DC-to-DC Converter Uses the IC Timer"**, Robert Soloman and Robert Broadway, *EDN*, September 5, 1973, pp. 87 – 91.
3. **"Oscilloscope–Triggered Sweep: Another Job for IC Timer"**, Robert McDermott, *Electronics*, October 11, 1973, p. 125.
4. **"Get Square Wave Tone Bursts With a Single Timer IC"**, Sol Black, *Electronic Design*, September 1973, p. 148.
5. **"Toroid and Photo-SCR Prevent Ground Loops in High-Isolation Biological Pulser"**, Joseph Sonsino, *Electronic Design*, June 21, 1973. p. 128.
6. **"Voltage-to-Frequency Converter Constructed With Few Components is Accurate to 0.2%"**, 'Chaim Klement, *Electronic Design*, June 21, 1973, p. 124.
7. **"Positive Voltage Changed into Negative and No Transformer is Required"**, Bert Pearl, *Electronic Design*, May 24, 1973, p. 164.
8. **"Pair of IC Timers Sounds Auto Burglar Alarm"**, Michael Harvey, *Electronics*, June 21, 1973, p. 131.
9. **"Timer ICs and LEDs Form Cable Tester"**, L.W. Herring, *Electronics*, May 10, 1973, p. 115.
10. **"IC Timer can Function as Low Cost Line Receiver"**, John Pate, *Electronics*, June 21, 1973, p. 132.
11. **"IC Timer Plus Thermister can Control Temperature"**, Donald Dekold, *Electronics*, June 21, 1973, p. 132.
12. **"IC Timer Makes Economical Automobile Voltage Regulator"**, T.J. Fusar, *Electronics*, September 21, 1974, p. 100.
13. **"Switching Regulators, the Efficient Way to Power"**, Robert Olla, *Electronics*, August 16, 1973, pp. 94 – 95.
14. **"Put the IC Timer to Work in a Myriad of Ways"**, Eugene Hnatek, *EDN*, March 5, 1973, pp. 54 – 58.

AN171
NE558 Applications

Application Note

INTRODUCTION

The 558 is a monolithic Quad Timer designed to be used in the timing range from a few microseconds to a few hours. Four entirely independent timing functions can be achieved using a timing resistor and capacitor for each section. Two sections of the quad may be interconnected for astable operation. All four sections may be used together, in tandem, for sequential timing applications up to several hours. No coupling capacitors are required when connecting the output of one timer section to the input of the next.

FEATURES

- **100mA output current per section**
- **Edge-triggered (no coupling capacitor)**
- **Output independent of trigger conditions**
- **Wide supply voltage range 4.5V to 16V**
- **Timer intervals from microseconds to hours**
- **Time period equals RC**

CIRCUIT OPERATIONS

In the one-shot mode of operation, it is necessary to supply a minimum of two external components (the resistor and capacitor) for timing. The time period is equal to the product of R and C. An output load must be present to complete the circuit due to the output structure of the 558.

For astable operation, it is desirable to cross-couple two devices from the 558 Quad. The outputs are direct-coupled to the opposite trigger input. The duty cycle can be set by the ratio of R_1C_1 to R_2C_2, from close to zero to almost 100%. An astable circuit using one timer is shown in Figure 5b.

OUTPUT STRUCTURE 558

The 558 structure is open-collector which requires a pull-up resistor to V_{CC} and is capable of sinking 100mA per unit, but not to exceed the power dissipation and junction temperature rating of the die and package. The output is normally low and is switched high when triggered.

RESET

A reset function has been made available to reset all sections simultaneously to an output low state. During reset the trigger is disabled. After reset is finished, the trigger voltage must be taken high and then low to implement triggering.

The reset voltage must be brought below 0.8V to insure reset.

THE CONTROL VOLTAGE

The control voltage is also made available on the 558 timer. This allows the threshold voltage to be modulated, therefore controlling the output pulse width and duty cycle with an external control voltage. The range of this control voltage is from about 0.5V to V_{CC} minus 1V. This will give a cycle time variation of about 50:1. In a sequential timer with voltage-controlled cycle time, the timing periods remain proportional over the adjustment range.

TEST BOARD FOR 558

The circuit layout can be used to test and characterize the 558 timer. S_2 is used to connect the loads to either V_{CC} or ground. The main precaution, in layout of the 558 circuit, is the path of the discharge current from the timing capacitor to ground (Pin 12). The path must be direct to Pin 12 and not on the ground bus. This is to prevent voltage spikes on the ground bus return due to current switching transient. It is also wise to use good power supply bypassing when large currents are being switched.

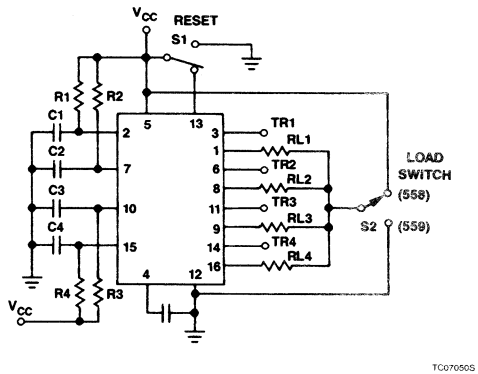
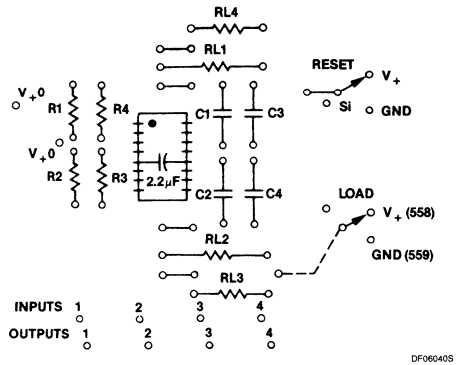
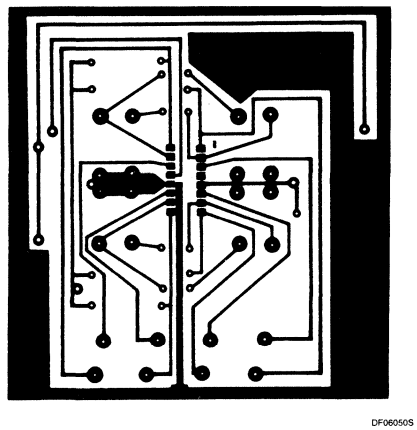


Figure 1. 558 Test Circuit



a. Test Board Layout



b. Foil Side

Figure 2

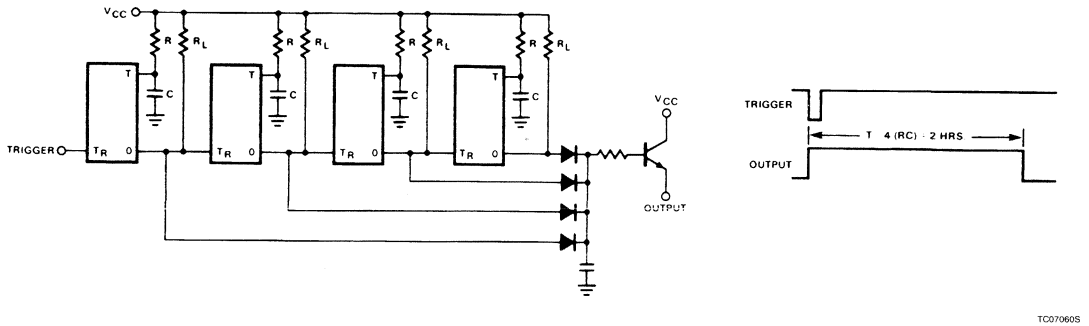
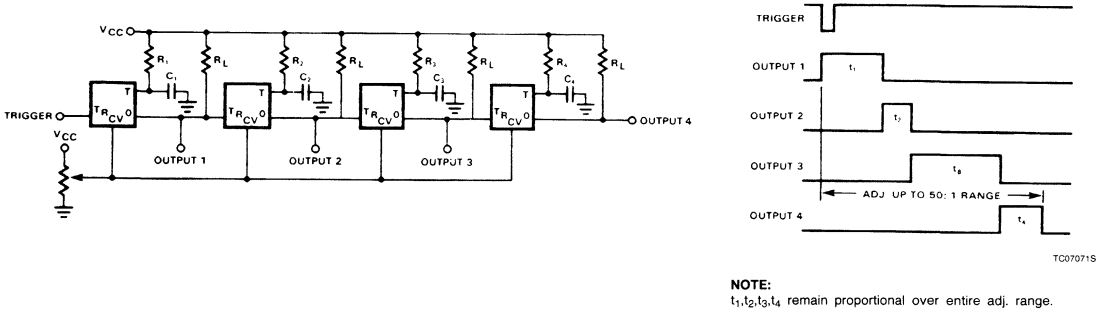
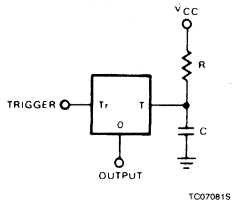


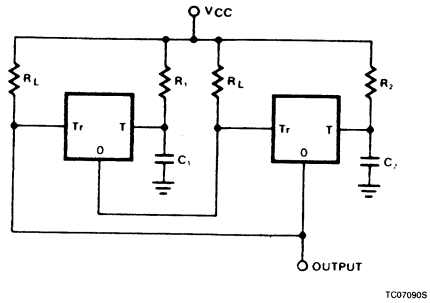
Figure 3. 558 Two-Hour Timer



NOTE:
t_1, t_2, t_3, t_4 remain proportional over entire adj. range.

Figure 4. 558 Sequential Timer With Voltage-Controlled Cycle Time (50:1 Range)

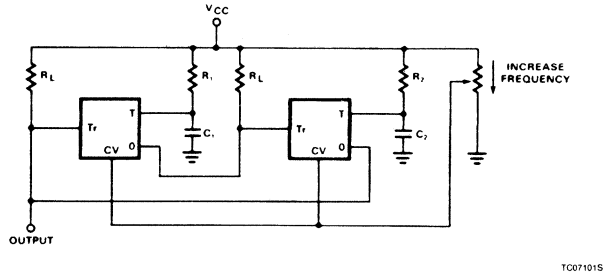




NOTE:
T = RC

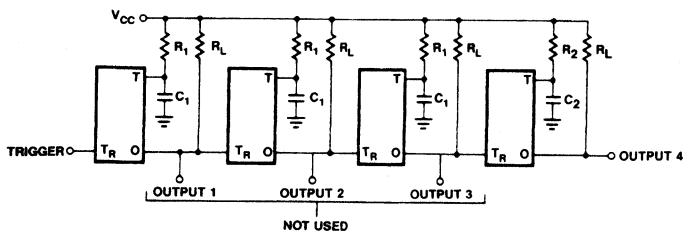
a. Monostable Operation (One-Shot)

b. 558 Astable Operation (Oscillator)



c. 558 Variable Frequency Oscillator with Fixed Duty Cycle

Figure 5



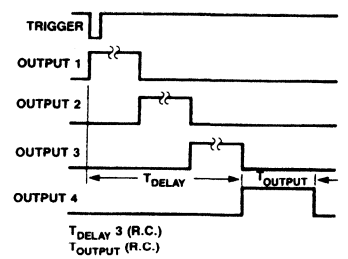
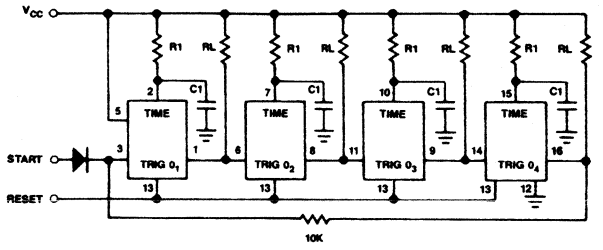
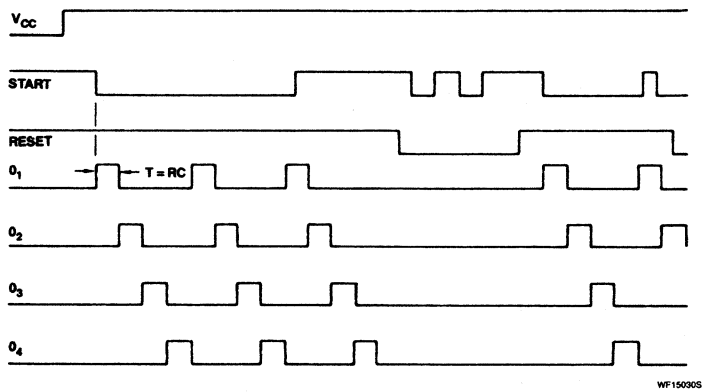


Figure 6. 558 Long Time Delay



a. 558 Ring Counter



b. Expected Waveforms

Figure 7

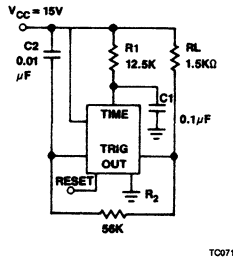


Figure 8. NE558 400Hz Square Wave Oscillator

A single section of the quad time may be used as a non-precision oscillator. The values given are for oscillation at about 400Hz. $T_1 \approx R_1C_1$ and $T_2 \approx 2.25\ R_2C_2$ for V_{CC} of 15V. The frequency of oscillation is subject to the changes in V_{CC}.

POWER CONVERSION AND CONTROL

page

Motor control 871

Switched-mode power supply circuits 931

Motor control

		page
NE544	servo amplifier	873
NE5044	programmable seven-channel RC encoder	879
NE5045	seven-channel RC decoder	886
NE5570	brushless DC motor controller	892
SA5570	brushless DC motor controller	892
SE5570	brushless DC motor controller	892
AN131	applications using the NE5044 encoder	897
AN132	applications using the NE5045 decoder	899
AN133	applications using the NE544 servo amplifier	900
AN1281	NE5570: a theory of operation and applications	904
AN1311	low cost A/D conversion using the NE5044	918
AN1341	control system for home computer and robotics applications	920

NE544
Servo Amplifier

Product Specification

DESCRIPTION

The NE544 is a servo amplifier and pulse-width demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed-loop position control applications. It incorporates a linear one-shot for improved positional accuracy and outputs for external PNP motor drive transistors.

FEATURES

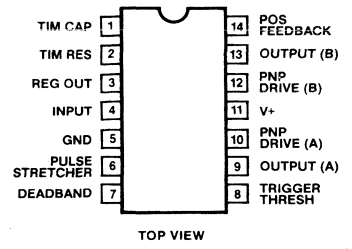
- **500mA load current capability**
- **Bidirectional bridge output with single power supply**
- **Low standby power drain**
- **Adjustable deadband and trigger thresholds**
- **High linearity, 0.5% maximum error**
- **Output drive for external PNP transistors (optional)**
- **Wide supply voltage range**

APPLICATIONS

- **Miniature position servo**
- **Robotics**
- **Control devices**
- **Remote positioning**

PIN CONFIGURATIONS

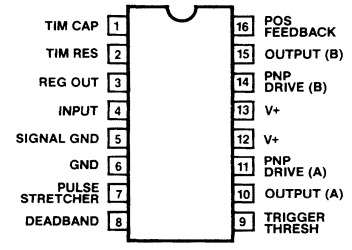
N Package



TOP VIEW

CD10480S

D Package[1]



TOP VIEW

CD10490S

NOTE:
1. SOL and non-standard pinout.

ORDERING INFORMATION

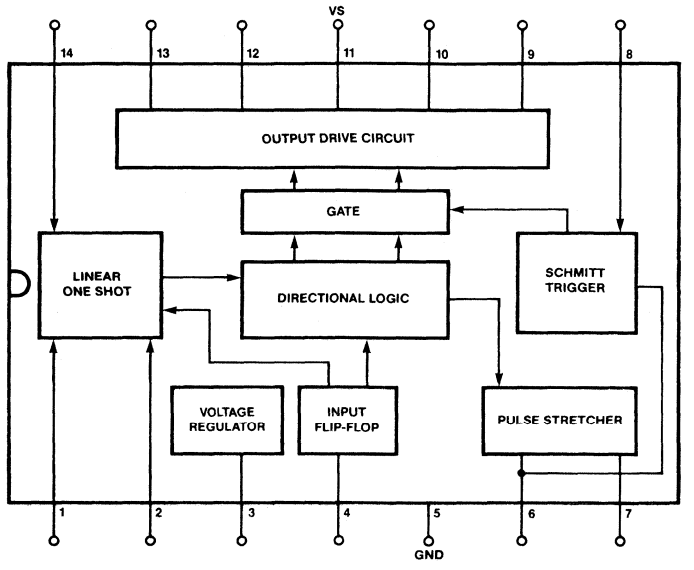
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE544N
16-Pin Plastic SOL Package	0 to +70°C	NE544D

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

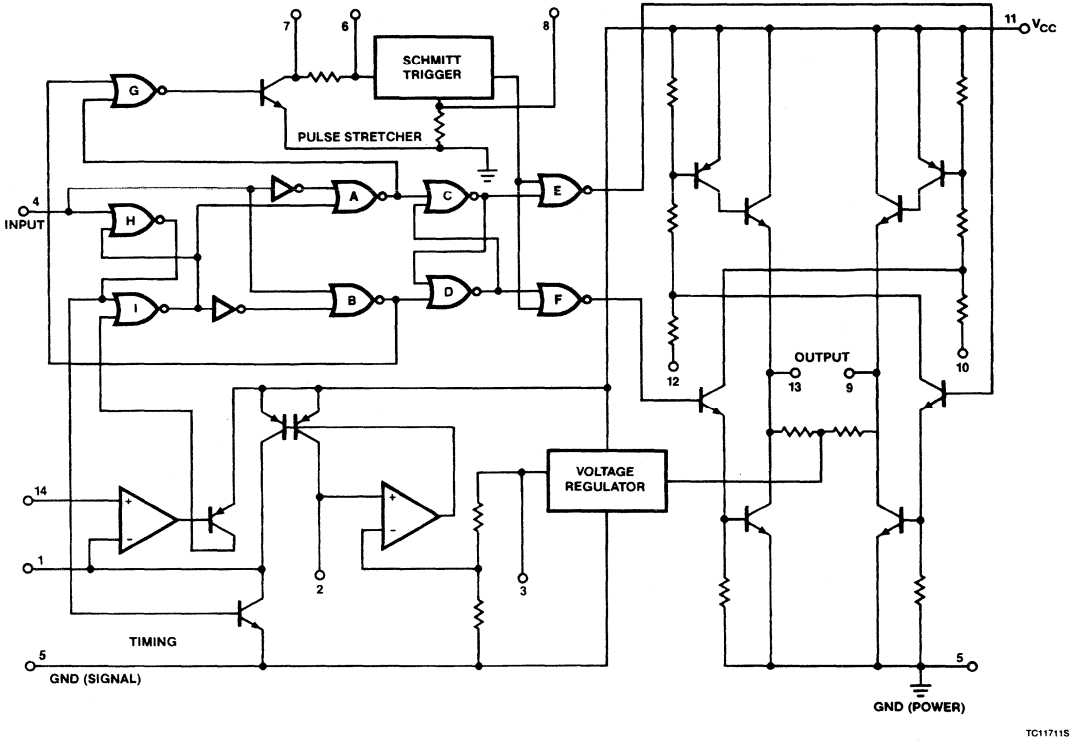
SYMBOL	PARAMETER	RATING	UNIT
V+	Supply voltage	6.0	V
I_O	Output current D package N package	 400 500	mA
T_A	Operating temperature	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

BLOCK DIAGRAM



NOTE:
Pinout for N package.

EQUIVALENT SCHEMATIC

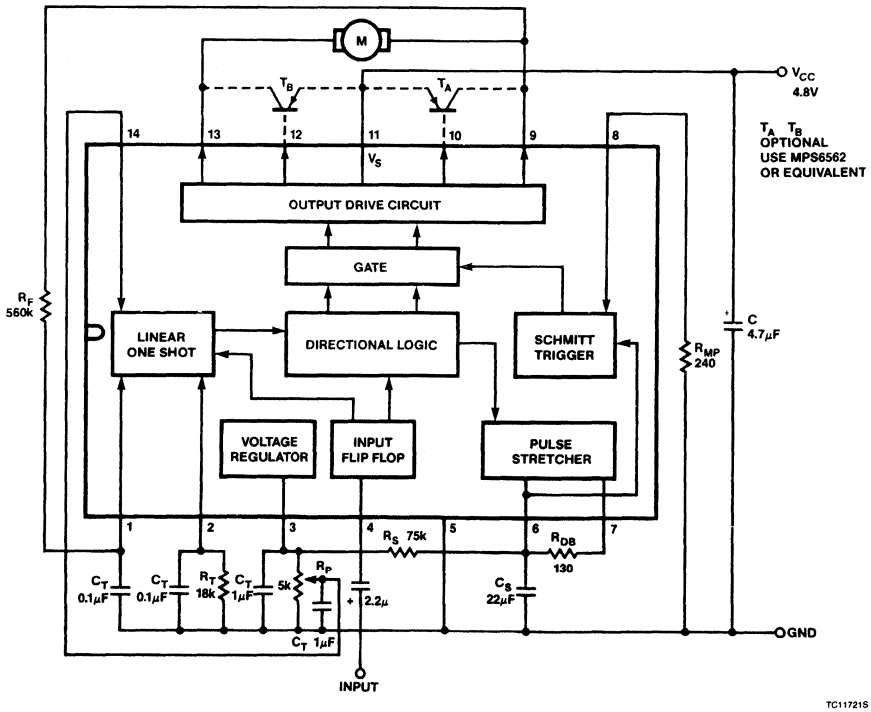


NOTE:
Pinout for N package.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = 4.8V$ unless otherwise specified.

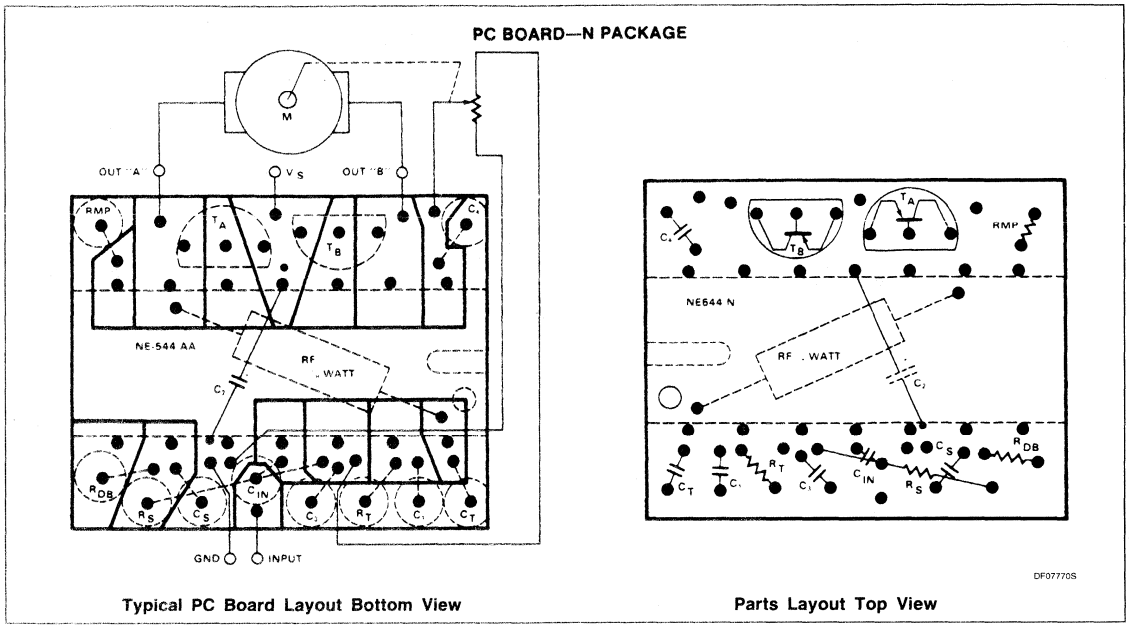
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC} I_{CC}	Supply voltage Supply current, Pin 11	Quiescent	3.2 4.2	4.8 5.5	6 10	V mA
V_{TH}	Input threshold, Pin 4 On Off			 1.5 1.4		V
Z_{IN}	Input resistance, Pin 4			18		kΩ
 V_{OL} V_{OH}	Output voltage Low High	Pin 9 or 13. $I_L = 400mA$		 0.3 3.9		V
V_{REG}	Regulated voltage, Pin 3		2.1	2.5	2.9	V
ΔV_{REG}	Regulation, Pin 3 Minimum deadband, Pin 7 One-shot temperature coefficient	$3.9V \leqslant V_{CC} \leqslant 6V$ $R_{DB} = 0$		10 1 0.01		mV/V μs %/°C
	Standby output voltage PNP drive current	Pins 9 and 13 Pins 10 and 12		2.5 20		V mA

TYPICAL CONNECTION OF NE544N FOR LINEAR ONE-SHOT TIMING



NOTE:
Pinout for N package

PC BOARD — N PACKAGE

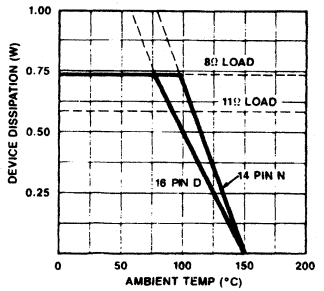


Typical PC Board Layout Bottom View

Parts Layout Top View

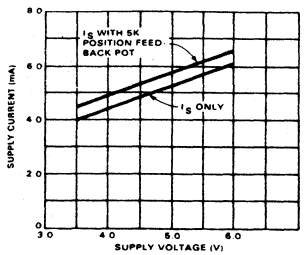
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Dissipation vs Ambient Temperature



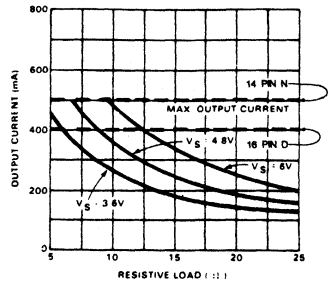
OP19481S

Supply Current vs Supply Voltage



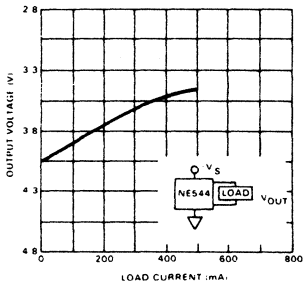
OP19490S

Output Current vs Load Resistance



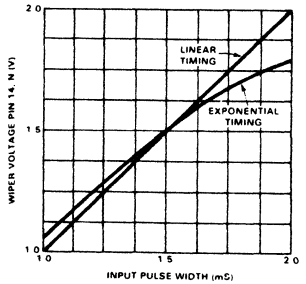
OP19501S

Output Voltage vs Load Current



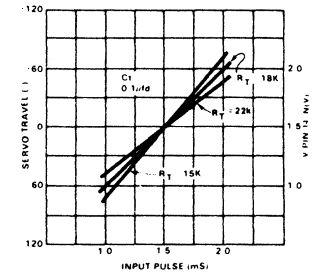
OP19510S

Input Pulse Width vs Feedback Pot Output



OP19520S

Input Pulse vs Servo Travel



OP19530S

NE5044
Programmable Seven-Channel RC Encoder

Product Specification

DESCRIPTION

The NE5044 is a programmable parallel input, serial output pulse width encoder. A multiplexed dual linear ramp technique is used to allow up to 7 inputs to be converted to a serial pulse width modulated signal with excellent linearity and minimal crosstalk. Fixed or variable frame rates can be used, externally controlled, for ease of demodulation. An onboard 5V regulator eliminates power supply sensitivities and provides up to 20mA current capability for driving external loads.

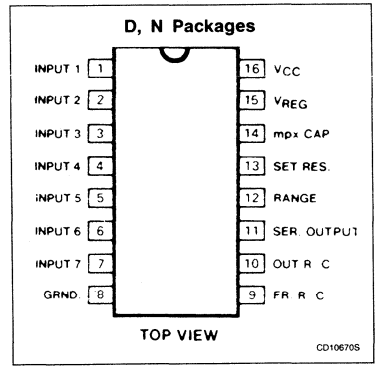
FEATURES

- **3 to 7 channels, externally selectable**
- **Constant-current dual linear ramp for linearity better than 0.3%**
- **Internal voltage regulator for low drift**
- **Wide supply range 4.5 – 12V**
- **Fixed or variable frame rate set by external RC**
- **External control for channel gain or range**
- **Versatile applications: exponential rates, mixing, dual rate, reversing, etc.**
- **Compatible with all transmission mediums**

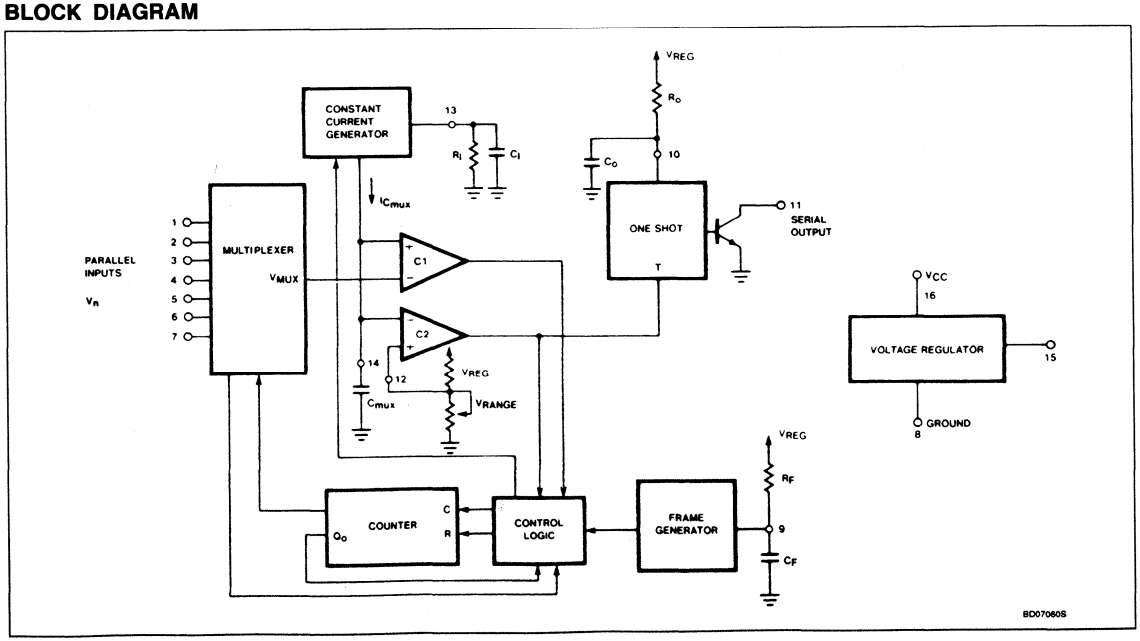
APPLICATIONS

- **Radio-controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote-controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/ controls**
- **Remote analog/digital data transmission**
- **Automotive sensor systems**
- **Robotics**
- **Telemetry**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO Package	0 to +70°C	NE5044D
16-Pin Plastic DIP	0 to +70°C	NE5044N

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	13	V
I_{OUT}	Regulator output current	−25	mA
	Serial output peak current	30	mA
	Constant-current generator	−1	mA
	Parallel inputs, range input	0-V_{REG}	V
	One-shot input, frame generator input	0-V_{REG}	V
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:
1. T_A = 25°C unless otherwise stated.

DC ELECTRICAL CHARACTERISTICS Test Conditions T_A = 25°C, V_{CC} = 10V using Test Circuit, unless otherwise stated.

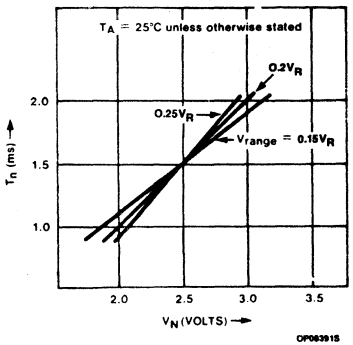
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Power supply requirements						
V_{CC}	Power supply voltage range		4.5		12	V
I_{CC}	Power supply current	Excluding control pots and serial output currents		11	15	mA
Voltage regulator						
V_{REG}	Output voltage		4.5	5.0	5.5	V
I_{OUT}	Output current	$V_R \geq 4.5V$			−20	mA
	Line regulation	$7 \leq V_{CC} \leq 12$		0.005	0.02	V/V
Multiplexer						
I_{IN}	Input current	V_n = 2.5V		±30	±200	nA
V_{IN}	Input voltage range	$V_n - V_{Range} \geq 0.75V$	1.5		5	V
	Crosstalk			±1	±5	μs

AC ELECTRICAL CHARACTERISTICS Test conditions $T_A = 25°C$, $V_{CC} = 10V$ using Test Circuit, unless otherwise stated.

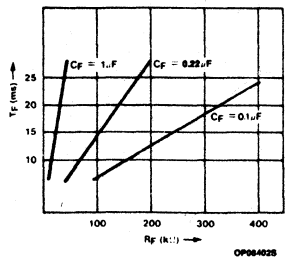
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Output pulse						
t_n	Position	$R_I \bullet C_{MUX} = 1.25ms$ $V_n = 0.5V_{REG}$; $V_{RANGE} = 0.2V_{REG}$	1350	1500	1650	μs
	Position linearity error			5		μs
	Position tempco	$0°C \leqslant T_A \leqslant 70°C$		0.15		μs/°C
	Position PSR	$6V \leqslant V_{CC} \leqslant 12V$		0.5	1	μs/V
t_O	Width	$R_OC_O = 300\mu s$	240	285	330	μs
	Saturation voltage	$I_O = 25mA$		0.6	1	V
I_{11}	Leakage current			0.05	50	μA
R_I	Range input voltage	$R_I = 50k\Omega$ $R_I = 25k\Omega$	0.75 1.00			V V
	Frame time (fixed)	$R_FC_F = 30ms$	17	20	23	ms
	Inhibit threshold				0.4	V

TYPICAL PERFORMANCE CHARACTERISTICS

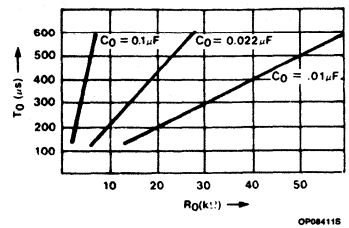
Output Pulse Width (T_n) vs Input Voltage (V_n)



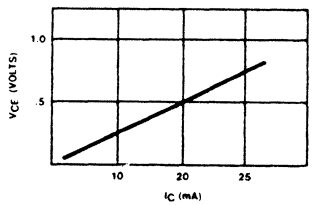
Frame Time (t_F) vs R_F



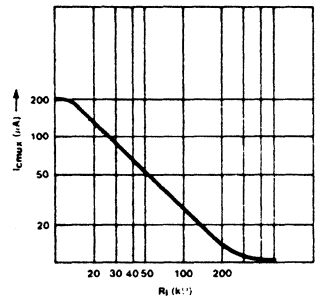
Output One-Shot Time (t_O) vs R_O



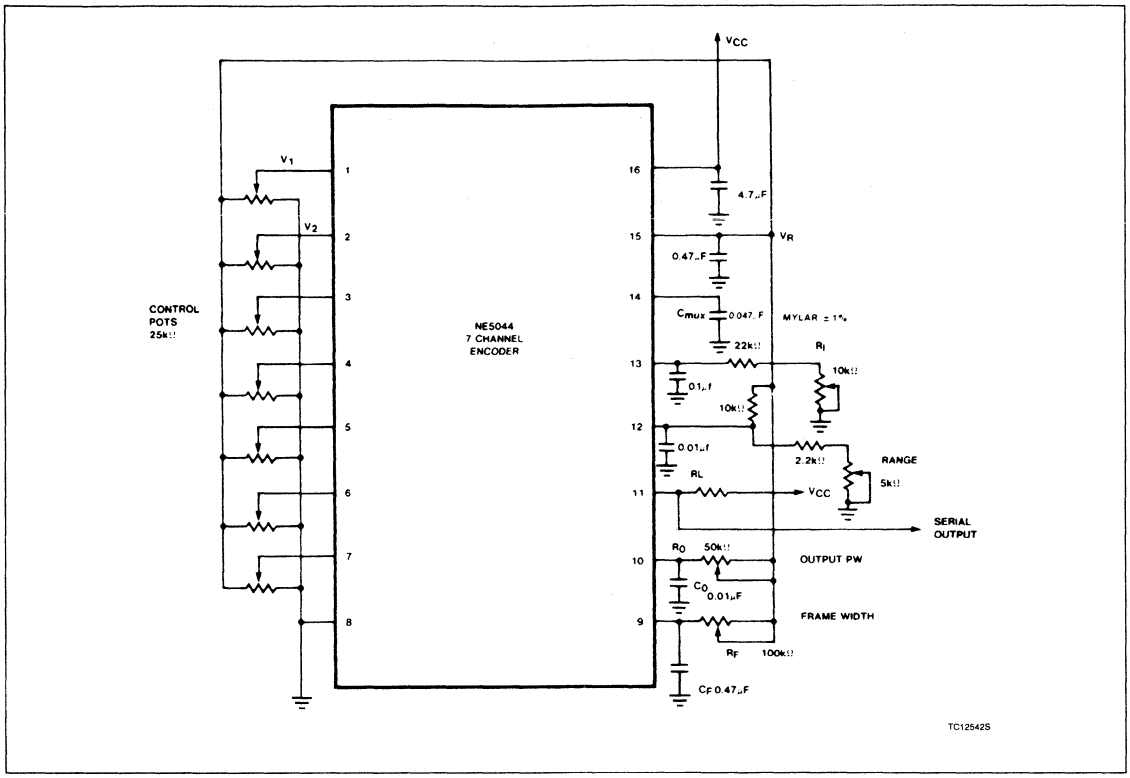
Output Saturation Voltage vs Output Current



Constant-Current vs R_I



TEST CIRCUIT



CIRCUIT OPERATION

The NE5044 is a programmable parallel input, serial output encoder containing all the active circuitry necessary to generate a precise pulse width modulated signal with 3 to 7 channels. The number of channels is externally programmable by grounding unused control inputs. A multiplexed dual linear ramp technique is used to provide excellent linearity, minimal crosstalk and low temperature drift. An on-board 5V regulator eliminates power supply sensitivities and has up to 20mA current capability for driving external loads. The encoder can be used in the fixed-frame mode or, with the addition of one external NPN transistor, as a variable-frame encoder.

The multiplexer functions as a strobed voltage-follower so that each input, when active, appears as a high-impedance input (> 1MΩ) and transfers the input voltage to the output. Only one of the seven inputs is active at any time and when a given input is inactive, it appears as an open circuit. The high-impedance multiplexer inputs eliminate loading on control inputs and simplify mixing circuits where several controls may be mixed onto one input.

Channel 4, 5, 6 and 7 inputs may also be used to select the desired number of output pulses by grounding one or more of these pins. That is, by grounding Pin 4 (Channel 4 input) only the first three inputs of the encoder will be used and a 3-channel encoder results. Grounding Pin 5 results in a 4-channel encoder, and so on. Thus, any number of channels between 3 and 7 may be selected. Internal voltage clamping prevents encoder malfunction if any input is shorted to supply, ground or open-circuited. The remaining channels will continue to be encoded except as noted above. This feature eliminates catastrophic failures due to control pot open- or short-circuits.

The constant-current generator is a bidirectional current source whose current is set by an external resistor R_I, where:

$$I_C = \pm\frac{V_R}{2R_I}$$

The current generator alternately charges and discharges the capacitor C_{MUX}. An internal feedback loop maintains a constant current and very high output impedance. This yields a typical linearity error of voltage input to pulse width output for the encoder of less than 0.1%. An external capacitor, C_I, is required to insure stability of the feedback loop.

Two high gain comparators, C1 and C2, compare the voltage across C_{MUX} with the multiplexer output voltage and the range input voltage. The input bias currents and offset voltages of these comparators are sufficiently low so as to not influence the overall accuracy of the encoder. The comparators feed the counter control logic which in turn controls the counter and current generator. The operation of this loop is as follows: When I_C is positive (sourced from the current generator into C_{MUX}) the capacitor linearly charges up until it reaches a voltage equal to the multiplexer output voltage; assume this to be the voltage at Pin 1, V1. At this time the output of C1 goes high, which reverses the direction of I_C (sinking into current generator from C_{MUX}). C_{MUX} now linearly discharges until it reaches the voltage set on Pin 12, V_{RANGE}. At this time the output of C2 goes high, which again reverses the polarity of I_C, clocks the counter,

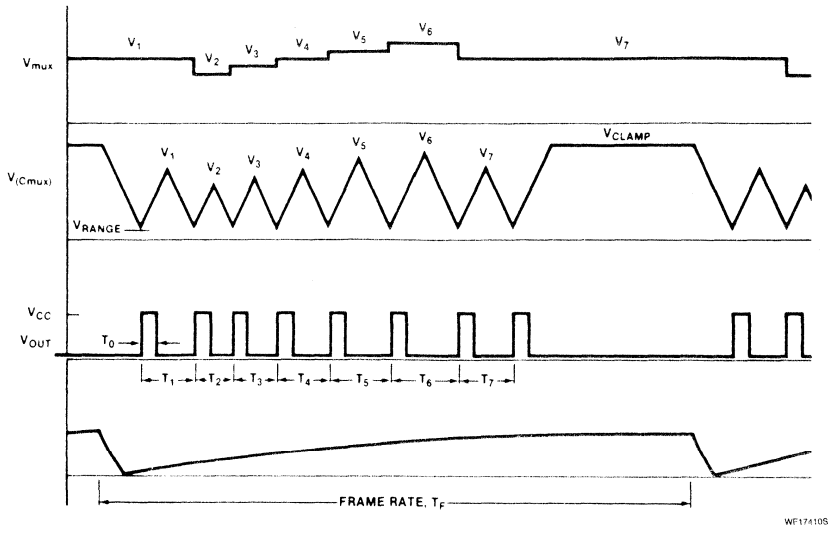


Figure 1. Encoder Timing Diagram — Fixed-Frame

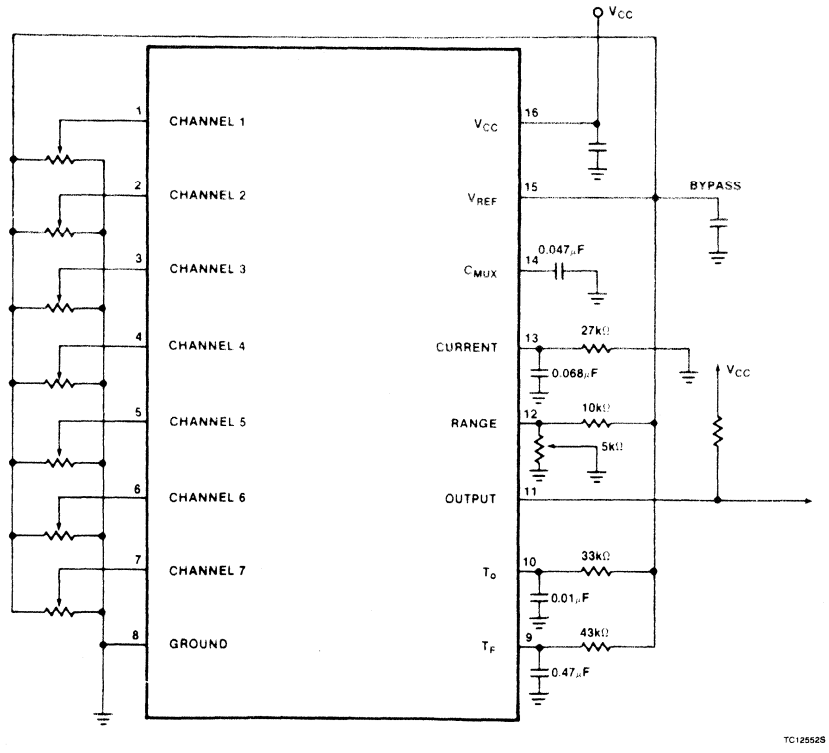


Figure 2

and triggers the output one-shot. C_{MUX} again charges up but now C1 goes high when C_{MUX} reaches V2, the voltage on Pin 2. The resulting voltage waveform on C_{MUX} is a triangle wave whose positive peaks correspond to the voltages on Pins 1 through 7 for the first through seventh peaks and whose negative peaks are constant and equal to V_{RANGE}. This waveform is shown in the first portion of Figure 1.

Independent control of I_C and V_{RANGE} allows the encoder to be tailored to virtually any combination of input voltage changes and output pulse width changes. The functional relationships between these variables will be defined in the next section.

The frame generator controls the encoder frame time. It can operate as an astable or monostable multivibrator whose period is $0.66 \times R_F C_F$. The encoder will generate a synchronizing pulse at the end of each frame. When C_{MUX} reaches the seventh positive peak it reverses and discharges to V_{RANGE}. The counter is clocked to the state where Q_O is high when $VC_{MUX} = V_{RANGE}$. C_{MUX} again charges up, but now the output of C1 is ignored, due to Q_O being high, and charges up to V_{CLAMP} and remains there. The encoder will remain in this state until a pulse from the frame generator is received. If R_F and C_F are connected as shown in the Block Diagram, then the frame generator operates in the astable mode, producing a narrow pulse output. This pulse allows C_{MUX} to start discharging again. When C_{MUX} reaches V_{RANGE}, the counter is clocked to the state where Q_1 is high (channel 1) and the entire process starts over. The frame period in this mode is $0.66 \times R_F C_F$ and is referred to as the fixed-frame mode. The variable-frame mode will be discussed in the application section.

The output one-shot generates a positive pulse whose width is equal to $R_O C_O$. The output is an open-collector, NPN transistor capable of sinking 25mA. This configuration allows the encoder to drive a wide variety of RF stages as well as providing current pulses in 2-wire communications applications.

ENCODER DESIGN EQUATIONS

The triangular waveform on C_{MUX} has a fixed slope (constant current) and variable positive peak voltages. The time between the negative peaks of C_{MUX}, which is equal to the output period for that channel, is given by:

$$t_n = \frac{2 (V_n - V_{RANGE}) C_{MUX}}{I_C}$$

I_C is given by:

$$I_C = \frac{V_R}{2R_I},$$

where V_R = Reference Voltage.

Additionally, V_n, the voltage on Pin n, which is the control voltage for Channel n, is typically the wiper voltage on a pot connected between V_R and ground. Thus $V_n = X_n V_R$.

V_{RANGE} is also derived from V_R so that $V_{RANGE} = Y\ V_R$. The resulting channel time period is:

$$t_n = \frac{2 (X_n - Y)\ V_R \cdot C_{MUX}}{(V_R/2R_I)}$$

$$\boxed{t_n = 4R_I\, C_{MUX}(X_n - Y)}$$

Thus, each channel pulse width, t_n, is independent of supply voltage and depends only on external passive components.

The conversion rate, CR, for each channel is the change in output period, Δt_n, divided by the change in input voltage for that channel, ΔV_n.

$$CR = \frac{\Delta t_n}{\Delta V_n} = \frac{\Delta t_n}{\Delta X_n} = 4\ R_I\ C_{MUX}$$

In most applications, the input variable X_n will have some neutral or center value about which it will vary, thus

$X_n = X_o + x_n$,

and

$$\boxed{CR = \frac{\Delta t_n}{\Delta X_n} = 4R_I C_{MUX}}$$

Where X_O is the neutral value for X and is assumed to be the same for all n. Now

$$t_n = 4R_I C_{MUX}\ (X_O - Y + X_n)$$

If we let $t_{NEUTRAL} = 4R_I C_{MUX}\ (X_O - Y)$ be the neutral value for t_n, then

$$\boxed{t_n = t_{NEUTRAL} + 4R_I C_{MUX}\ (X_n)}$$

Consider the following example to see how these design equations are used.

Assume:

$t_{NEUTRAL} = 1.5ms$

$X_O = 0.5$ — Control pot in center at

$t_n = t_{NEUTRAL}$

$\Delta x_n = \pm 0.1$ — Control pot resistance varies ± 10% (of total resistance) around neutral. This should include mechanical trim if used.

$\Delta t_n = \pm 0.5ms$

For this example, the conversion rate is

$$CR = \frac{\Delta t_n}{\Delta X_n} = \frac{0.5ms}{0.1} = 5ms,$$

so

$4R_I C_{MUX} = 5ms.$

If we let $C_{MUX} = 0.047\mu F$ then

$$R_I = \frac{5ms}{4 \times 0.047\mu F} = 26.5k\Omega = 27k\Omega$$

and

$t_{NEUTRAL} = 1.5ms = 4R_I C_{MUX}(X_o - Y)$

$$Y = 0.5 - \frac{1.5ms}{5ms} = 0.2.$$

The output pulse width is given by

$t_O = R_O C_O$

so if $t_O = 330\mu s$ and $C_O = 0.01\mu F$ then

$$R_O = \frac{330\mu s}{0.01\mu F} = 33k\Omega$$

The frame time constant, t_F, is given by

$t_F = 0.66\ R_F C_F.$

If $t_F = 20ms$ and $C_F = 0.47\mu F$

$$R_F = \frac{20ms}{0.66 \times 0.47\mu F} = 62k$$

Figure 2 shows the external connections for this example.

It should be noted that the temperature stability of all the encoded times depend on the temperature coefficients of the respective external R_C time constants. No internal temperature compensation is used on the chip. The typical temperature sensitivity of t_n using wirewound resistors and polycarbonate capacitors is less than 100ppm/°C in the −20°C to +70°C temperature range. For the above example, this corresponds to a change in t_n of ±7.5μs for a change in temperature of ±50°C.

NE5045
Seven-Channel RC Decoder

Product Specification

DESCRIPTION

The NE5045 is a serial input, parallel output, decoder intended for applications in pulse width or pulse position modulation systems. The serial input pulse, either positive or negative, is shaped and amplified before being fed to the counter/decoder. An integrating type sync. separator detects pulses greater than $t_W = R_S C_S$. The amplified input pulse triggers an internal one-shot (minimum pulse) which in turn clocks the counter-decoder, thereby enhancing system noise rejection. A missing pulse detector resets the decoder during the sync. pause. An internal voltage regulator supplies power for the radio receiver, providing excellent isolation from the power supply as well as the decoder logic.

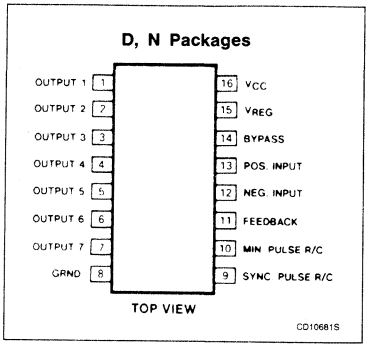
FEATURES

- **Decodes up to 7 channels**
- **High gain input amplifier**
- **Externally set sync. pause and minimum pulse**
- **Wide supply voltage range, 3.6V – 8V**
- **Positive or negative pulse inputs**
- **Noise and flutter rejection**
- **Outputs reset to zero without inputs**
- **Compatible with all transmission mediums**

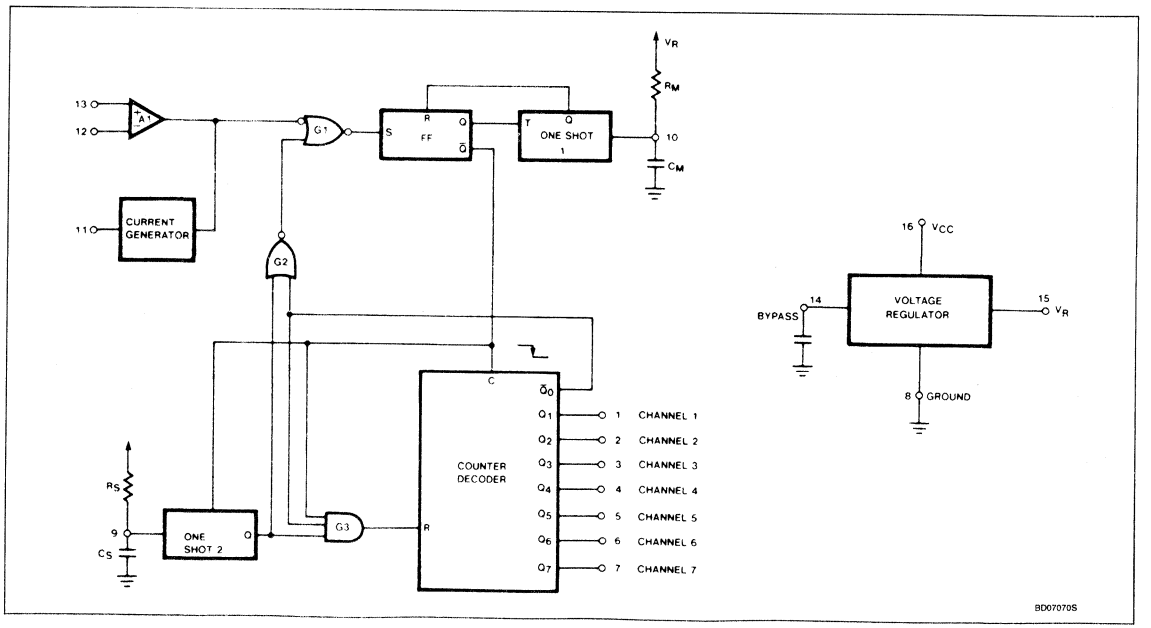
APPLICATIONS

- **Radio-controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote-controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/ controls**
- **Remote analog/digital data transmission**
- **Automotive sensor systems**
- **Robotics**
- **Telemetry**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5045D
16-Pin Plastic DIP	0 to +70°C	NE5045N

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	10	V
I_{OUT}	Regulator output current	−25	mA
	Decoded output current	±5	mA
	Pause input voltage	0 to V_R	V
V_{IN}	Input amplifier voltage	0 to V_R	V
T_A	Operating temperature	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

NOTE:
1. T_A = 25°C unless otherwise stated.

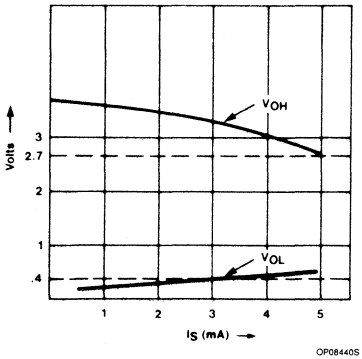
DC ELECTRICAL CHARACTERISTICS

Standard conditions: T_A = 25°C, V_{CC} = 5.0V, unless otherwise stated, using Test Circuit.

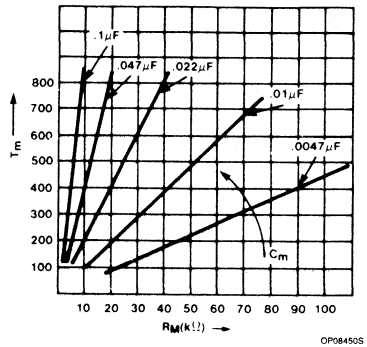
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Power supply requirements						
V_{CC}	Power supply voltage range	Test circuit	3.6		8.0	V
I_{CC}	Power supply current	Excluding input bias current		9.0	14.0	mA
Voltage regulator						
V_R	Output voltage		3.7	4.1	4.5	V
I_R	Output current	$V_R \geqslant 3.7V$			−15	mA
	Line regulation	V_{CC} = 6V to 8V		0.01	0.05	V/V
	Voltage drop	V_{CC} = 4V, I_R = −10mA			1.3	V
Input amplifier						
I_{BIAS}	Input bias current			10	100	nA
V_{IN}	Input voltage range		2.0		4.0	V
	Open-loop gain			60		dB
	Feedback current		100	200	400	μA
	Detection threshold	Test circuit, ΔV12 & 13		8	20	mV
t_S	Sync. pause time	R_S C_S = 6.0ms	5.1	6.0	6.9	ms
t_M	Minimum pulse time	R_M C_M = 500μs	405	475	545	μs
Outputs — all channels						
V_{OL}	Output voltage LOW	I_{SINK} = 1mA		0.25	0.5	V
V_{OH}	Output voltage HIGH	I_{SOURCE} = 2mA	2.7			V

TYPICAL PERFORMANCE CHARACTERISTICS

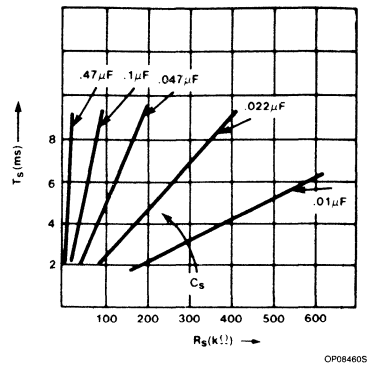
V_{OL} vs Sink Current and V_{OH} vs Source Current



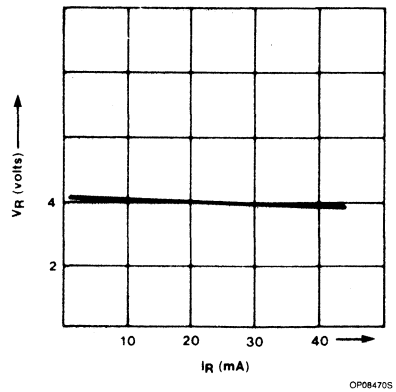
Minimum Pulse Time, t_M vs R_M, C_M



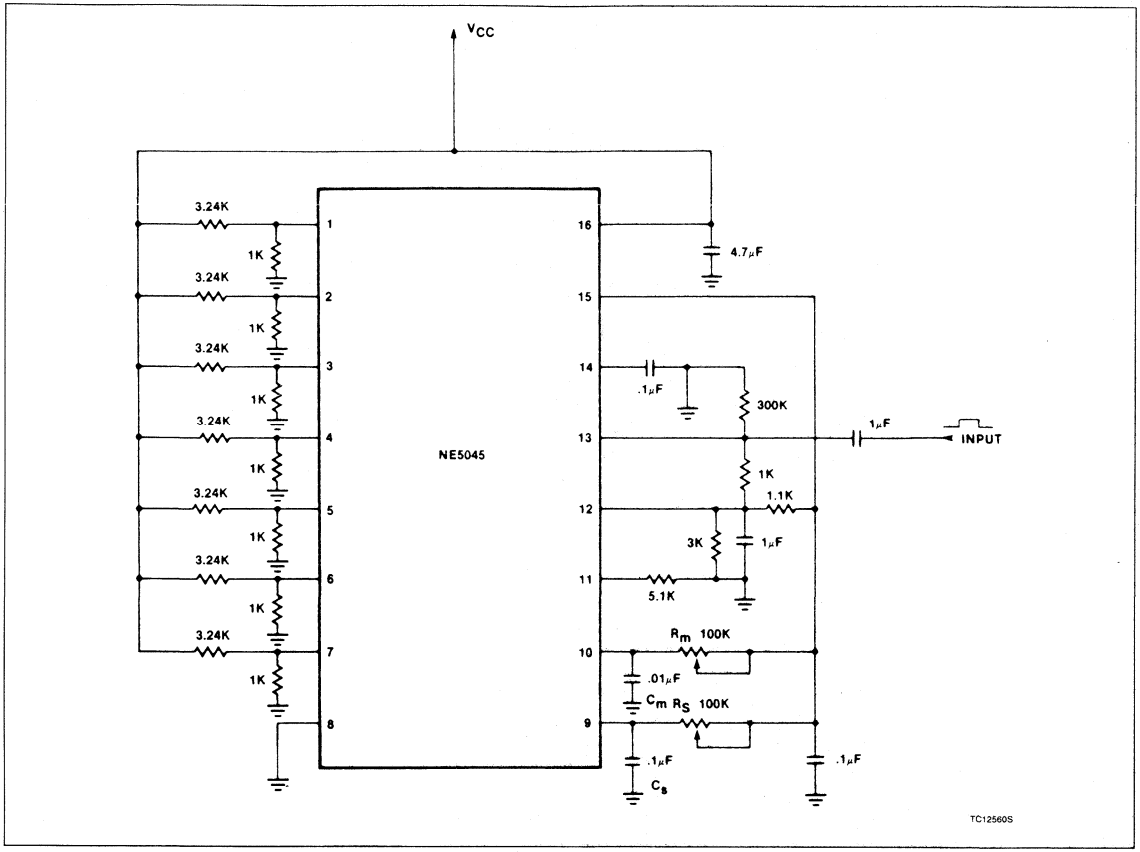
Sync Pause Time, t_S vs R_SC_S



Regulator Voltage vs Load Current



TEST CIRCUIT



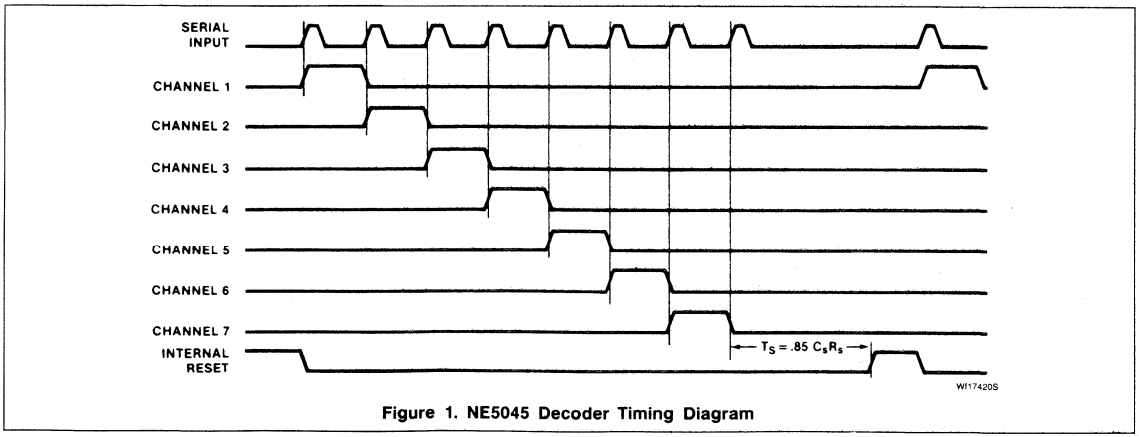


Figure 1. NE5045 Decoder Timing Diagram

CIRCUIT OPERATION

The NE5045 is a serial input, parallel output decoder containing all the active circuitry necessary to separate up to 7 channels of information in a pulse width modulated system. An internal voltage regulator provides excellent power supply rejection for the decoder as well as a regulated output for a radio receiver, if used.

The high gain input amplifier, A1 (A_V > 60dB), allows either positive or negative pulses to be used and has input bias currents less than 10nA. Signals as low as $10mV_{P-P}$ can easily be demodulated. The feedback current generator can be used to provide positive feedback, thereby creating hysteresis in the input switching levels. Hysteresis prevents false triggering due to noise or IF amplifier distortion. If positive input pulses are used, the signal would be connected to the non-inverting input, Pin 13. In this case, the input threshold would be set by the voltage difference between Pin 12 and Pin 13, established externally with a resistive divider network. Design of the divider will be covered later. Negative input signals would be coupled to Pin 12, the inverting input.

The amplified signal from A1 is gated by G1 and in turn sets the flip-flop. Assume, for the time, that G2 is low. The combination of the flip-flop and One-Shot 1 produces a minimum pulse to clock the counter-decoder for each positive *edge* at Pin 13 which exceeds the voltage on Pin 12. The width of this pulse is: $t_M = R_M C_M$. With this arrangement, the system will not respond to any pulse after the first edge and before the end of t_M. In effect the input is turned off for a period equal to t_M following the leading edge of each input pulse. The noise immunity of the decoder is thus enhanced by the ratio of t_M to the period between input pulses. Obviously t_M must be less than the shortest period between input pulses.

The counter is clocked and One-Shot 2 is reset (capacitor C_S is discharged) each time the flip-flop is set. When the flip-flop is reset, C_S begins to charge up through R_S. The time constant $t_S = 0.85\ R_S C_S$ is normally much larger than the time between input pulses so that the output of One-Shot 2 remains low until the last pulse of a given frame is received. Figure 1 shows the timing diagram for the decoder. After the last pulse in a frame (system synchronized) $\overline{Q}_O$ will go low and G2 will go high. The input is now disabled by G1 until One-Shot 2 times out, at which time G2 will go low.

This connection serves two purposes:

(1) establishes synchronization in no more than one frame and (2) prevents the counter-decoder from overflowing due to extra noise pulses in a given frame. Thus, any noise pulses in a frame will only affect those channels after that pulse and only in that frame.

If fewer than 7 channels of input are used then $\overline{Q}_O$ is high after the last pulse and the counter-decoder is reset when One-Shot 2 goes high.

Each channel has a totem-pole output stage capable of sourcing 2mA and sinking 1mA.

The voltage regulator operates in two modes, depending on the power supply voltage. If V_{CC} is greater than 5V, the voltage regulator acts as a series pass regulator with a nominal output voltage of 4.1V. When V_{CC} is less than 5V, the regulator acts as a dynamic decoupler where the bypass capacitor on Pin 14 filters out line transients. The internal pass transistor acts like an emitter-follower whose base is decoupled by the bypass capacitor. The value of capacitance will depend upon the degree of smoothing required and the amplitude of the line transients. If the regulator provides power for the radio receiver, this capacitor may have to be as large as 33μF. However, if this is not done, 1μF should be sufficient.

DECODER DESIGN EQUATIONS

The design of the decoder's external circuitry is quite simple. The minimum pulse One-Shot (#1) and the synchronization One-Shot (#2) each have time periods given by:

$$t_M = R_M C_M$$ and

$$t_S = 0.85\ R_S C_S$$

respectively. The constraints on these time periods are $t_M <$ the minimum input pulse width or time between leading edges of the input and $t_S >$ maximum input pulse width but $t_S <$ the sync pause (time between last pulse in frame and first pulse of the following frame).

The design of the input amplifier biasing network depends upon a number of factors, including:

1. Pulse polarity
2. Pulse amplitude
3. Variations in amplitude and noise
4. Detection threshold and hysteresis levels

For a very simple case, assume the input is a positive pulse train and the threshold of detection is desired to be 400mV without hysteresis. Figure 2 shows the input amplifier along with the associated biasing circuits. The resistors R_1 and R_2 set the voltage on Pin 12, which should be between 2V to 5V.

$$V_{12} = V_R \frac{1}{1 + R_1/R_2}$$

The threshold is set by the voltage drop across R_3, that is, the decoder will not be triggered until the voltage on Pin 13 exceeds the voltage on Pin 12.

$$V_{THRESHOLD} = V_{12} - V_{13}$$

$$V_{THRESHOLD} = V_{12} \left(\frac{1}{1 + R_4/R_3} \right)$$

If we assume $V_R = 4.1V$ and let $V_{12} = 3V$ then

$R_1 = 1.1k$

$R_2 = 3.0k$

The threshold is then set to 400mV by setting

$R_4/R_3 = 6.5$

R_4 should be sufficiently large so as to not load the input signal. If we let $R_3 = 51k$ then $R_4 = 330k$. Figure 3 shows the external connections for a complete decoder. Note that this circuit does not have provisions for noise filtering or rejection of amplitude variations.

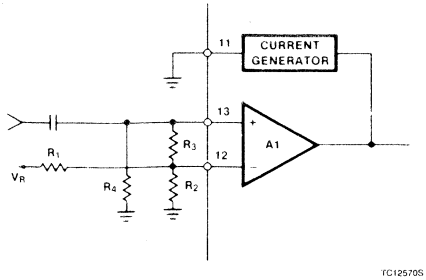


Figure 2. Input Amplifier Biasing NE5045

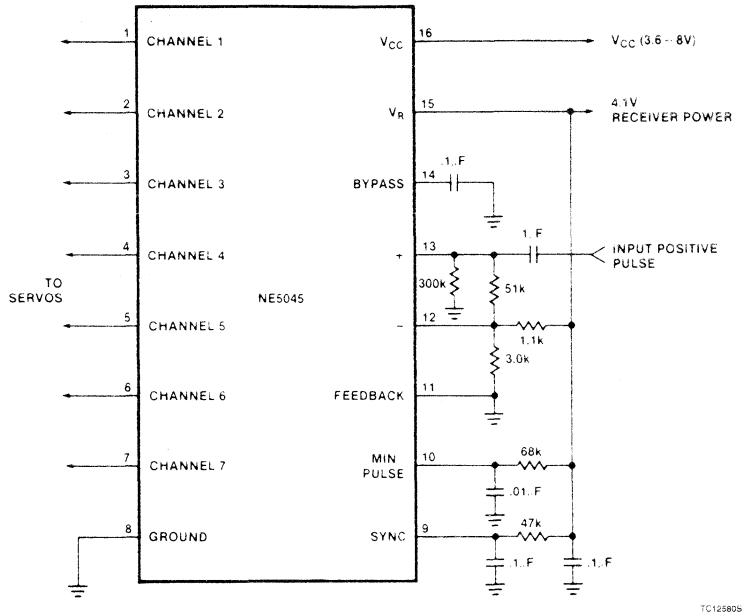


Figure 3. NE5045 Decoder External Connections: t_M = 0.68ms; t_S = 4ms, $V_{THRESHOLD}$ = 400mV

NE/SA/SE5570
Brushless DC Motor Controller

Product Specification

DESCRIPTION

The NE/SA/SE5570 is a three-phase brushless DC motor controller with a microprocessor-compatible serial input data port; 8-bit monotonic digital-to-analog converter; PWM comparator; oscillator; three Hall sensor inputs and six source/sink phase pre-drivers.

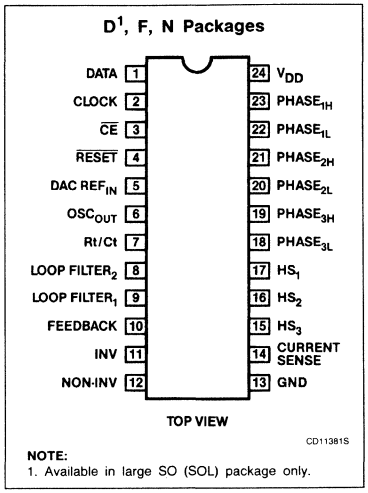
FEATURES

- **8-bit DAC**
- **Serial-to-parallel converter**
- **Output pre-drivers**
- **Entire switch mode conversion**
- **Adaptable to 60° or 120° commutation**
- **Overcurrent protection**

APPLICATIONS

- **Motor controller for three-phase brushless DC motor**
- **Robotics**
- **Computer peripherals**

PIN CONFIGURATION

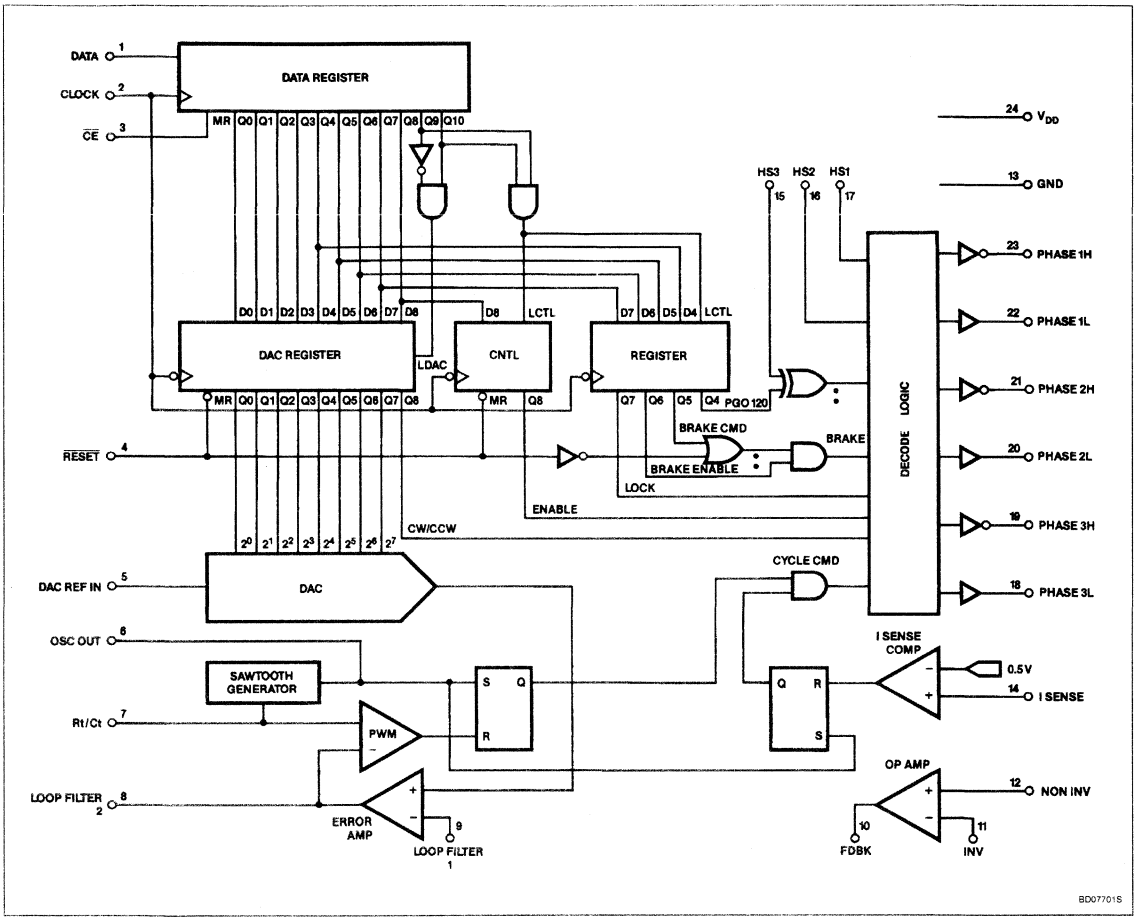


NOTE:
1. Available in large SO (SOL) package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin SOL	0 to +70°C	NE5570D
24-Pin Cerdip	0 to +70°C	NE5570F
24-Pin Plastic	0 to +70°C	NE5570N
24-Pin Cerdip	−40°C to +85°C	SA5570F
24-Pin Plastic	−40°C to +85°C	SA5570N
24-Pin Cerdip	−55°C to +125°C	SE5570F
24-Pin Plastic	−55°C to +125°C	SE5570N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING			UNIT
		NE5570	SA5570	SE5570	
	Temperature range				
T_A	Operating ambient	0 to 70	−40 to 85	−55 to 125	°C
T_J	Operating junction	−55 to 150	−55 to 150	−55 to 150	°C
T_{STG}	Storage	−65 to 150	−65 to 150	−65 to 150	°C
V_{DD}	Power supply	16	16	16	V
	Logic inputs, all	−0.3 to 15	−0.3 to 15	−0.3 to 15	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient temperature range		
	NE Grade	0 to 70	°C
	SA Grade	−40 to 85	°C
	SE Grade	−55 to 125	°C
T_J	Junction temperature range		
	NE Grade	0 to 90	°C
	SA Grade	−40 to 105	°C
	SE Grade	−55 to 145	°C
V_{DD}	Supply voltage	9.6 to 14.4	V

DC ELECTRICAL CHARACTERISTICS

Limits apply at V_{DD} = 12V ±10%, V_{REF} = 5V and over operating temperature range unless otherwise specified. Typical data applies at T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	SA/NE5570			SE5570			UNIT
			Min	Typ	Max	Min	Typ	Max	
Oscillator									
f_O	Frequency initial accuracy	T_A = 25°C, R_T = 2.49kΩ, C_T = 22nF	18.5	20	21	18.5	20	21	kHz
f_C	Frequency drift over temp	R_T = 2.49kΩ, C_T = 22nF	18		22	18		22	kHz
	Supply voltage sensitivity	T_A = 25°C		±2			±2		%/V
	Output pulse width	T_A = 25°C, R_T = 2.49kΩ, C_T = 22nF		500	1000		500	1000	ns
Motor Phase Pre-Drivers									
t_R	Rise time	R_L = 2kΩ to Gnd, C_L = 2nF [1V to 11V]			500			500	ns
t_F	Fall time	R_L = 2kΩ to V_{CC}, C_L = 2nF [1V to 11V]			500			500	ns
I_{OUT}	I_{SOURCE}	V_{OH} = 8V	80			80			mA
	I_{SINK}	V_{OL} = 3.1V	80			80			mA
V_{OUT}	V_{OH}	I_{SOURCE} = 5mA	11	11.8		11	11.8		V
		I_{SOURCE} = 80mA (over temp)	8	10		8	10		V
	V_{OL}	I_{SINK} = 5mA		0.4	1		0.4	1	V
		I_{SINK} = 80mA (over temp)		2	3.1		2	3.1	V
PWM Comparator									
I_{BIAS}	Input bias current				1			1	μA
Current Sense Comparator									
I_{BIAS}	Input bias current				1			1	μA
V_{TH}	Current sense trip level		350	500	600	350	500	600	mV
t_{PD}	Propagation delay to output drivers	C_L = 2nF		250			250		ns

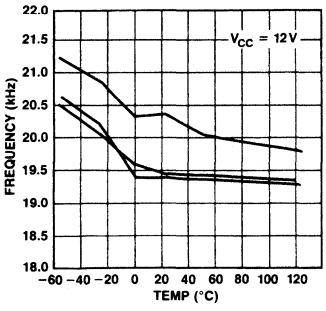
DC ELECTRICAL CHARACTERISTICS (Continued) **Limits apply at V_{DD} = 12V ±10%, V_{REF} = 5V and over operating temperature range unless otherwise specified. Typical data applies at T_A = 25°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	SA/NE5570			SE5570			UNIT
			Min	Typ	Max	Min	Typ	Max	
Error Amplifier									
I_{BIAS}	Input bias current				1			1	μA
V_{CM}	Input common-mode voltage range		0		5	0		5	V
V_{OL}	Large-signal voltage gain	V_{OUT} = 1V to 11V	70	90		70	90		dB
PSRR	Power supply rejection ratio		60			60			dB
V_O	Output voltage swing	V_{IN} = +50mV, I_L = −150μA V_{IN} = −50mV, I_L = +150μA	11.5	11.7 0.2	 0.5	11.5	11.7 0.2	 0.5	V V
Operational Amplifier									
V_{OS}	Offset voltage		−20	3	+20	−20	3	+20	mV
I_{BIAS}	Input bias current				1			1	μA
V_{CM}	Input common-mode voltage range	T_A = 25°C Over temp.	−0.3 0		5 5	−0.3 0		5 5	V
V_{OL}	Large signal voltage gain	V_{OUT} = 1V to 11V	70	90		70	90		dB
PSRR	Power supply rejection ratio		60	90		60	90		dB
V_O	Output voltage swing	V_{IN} = +50mV, I_L = −150μA V_{IN} = −50mV, I_L = +150μA	11.5	11.7 0.2	 0.5	11.5	11.7 0.2	 0.5	V V
CMRR	Common-mode rejection ratio	R_S = 10kΩ	60	80		60	80		dB
GBW	Gain bandwidth	R_F = 100kΩ		250			250		kHz
V_{NN}	Input noise voltage	F = 1kHz							nV/√Hz
Digital-to-Analog Converter									
	Resolution				8			8	bits
INL	Integral non-linearity error			±1	±2		±1	±2	LSB
DNL	Differential non-linearity error[1]			±0.5	±1		±0.5	±1	LSB
V_{FS}	Full-scale gain error	Error amp. A_V = 1		±0.2	±0.8		±0.2	±0.8	%FS
	Full-scale temperature drift	$V_{REF}T_C$ = 0ppm/°C		20			20		ppm/°C
V_{ZS}	Zero-scale offset error	Error amp. A_V = 1		±1	±2		±1	±2	LSB
Z_{IN}	Input impedance (DAC ref. in)		30	45	60	30	45	60	kΩ
t_S	Settling time to ±0.5 LSB			5			5		μs
t_{PLH}	Propagation delay time (high)	Through DAC		200			200		ns
t_{PHL}	Propagation delay time (low)	Through DAC		200			200		ns
Logic Inputs									
V_{IH}	Input voltage: TTL high		2.0		12	2.0		12	V
V_{IL}	Input voltage: TTL low		0		0.8	0		0.8	V
I_{IH}	Input current: TTL high				±1			±1	μA
I_{IL}	Input current: TTL low				±1			±1	μA
Supply Current									
I_{DD}				1.8	5.0		1.8	5.0	mA

NOTE:
1. Monotonicity guaranteed over operating temperature range.

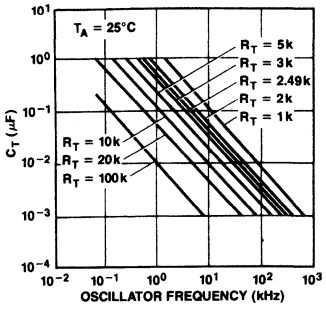
TYPICAL PERFORMANCE CHARACTERISTICS

NE5570 Oscillator Frequency vs Temperature



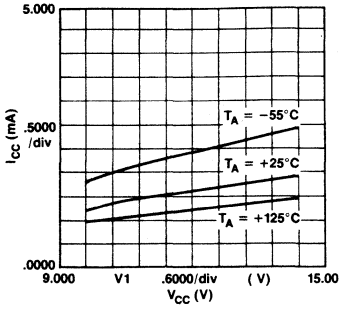
OP20700S

Oscillator Frequency vs R_T and C_T



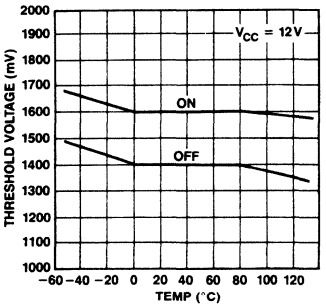
OP20710S

NE5570 Oscillator Frequency vs Supply Voltage



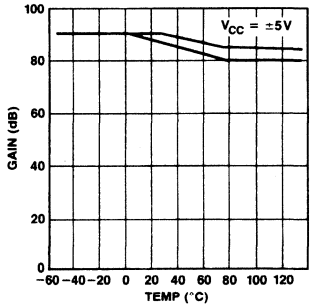
OP20720S

NE5570 Oscillator Output Pulse Width



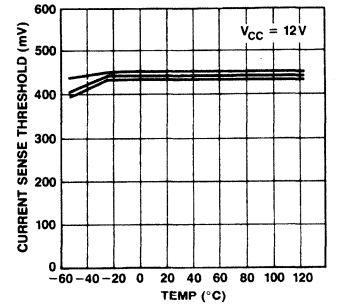
OP20730S

NE5570 Op Amp Gain vs Temperature



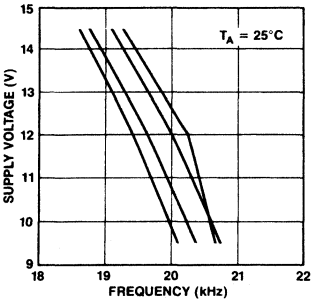
OP20740S

NE5570 Current Sense Comparator Threshold vs Temperature



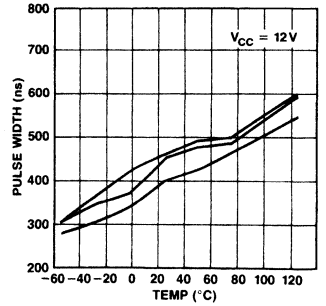
OP20750S

I_{CC} vs V_{CC}



OP20760S

NE5570 Logic Threshold Voltage vs Temperature



OP20770S

AN131
Applications Using the NE5044 Encoder

Application Note

The encoder inputs have been designed to accept a wide variety of signal sources. This can range from simple systems using as an input the wiper of a control pot which is connected between V_R and ground, to complex systems incorporating mixing, exponential processing and/or control polarity reversing. In all cases, it must be remembered that the control inputs to the encoder look like voltage-followers, that is, they draw only very small currents (>200nA). The voltage range for these inputs is +1.5V to +5V; however, internal clamps limit the linear control to approximately +1.5V to +3.5V. These clamps prevent interaction between channels if one input is open-circuited or shorted to supply or ground.

An example was worked out previously which utilized mechanical fine trim of the inputs (where the control pot body is rotated a small amount). In some applications, it is desirable to implement this fine trim electrically with the use of an additional pot. Many methods exist to achieve this and two are shown below.

In Figure 1 the series resistors R_T and R_C are much larger than the control pots so as to minimize non-linearity errors, and the ratio of R_T to R_C controls the relative sensitivity of the control and trim pots. This scheme allows the control pot to be centered at neutral so polarity reversing can be achieved by reversing V_R and ground on the pots.

The second approach, shown in Figure 2, is a simpler method for achieving electrical trim.

$$T_n = 4R_iC_{MUX}\left(\frac{R_T + X_nR_C}{R_T + R_C} - Y\right)$$

$$CR = 4R_iC_{MUX}\left(\frac{1}{1 + R_T/R_C}\right)$$

Interfacing the 5044 encoder to the modulator of an RF transistor can be done in several ways, depending on the desired output power, frequency stability and oscillator leakage. The simplest method is to use the 5044 output to directly modulate the bias current of a crystal-controlled oscillator. Figure 3 shows an example of such a connection.

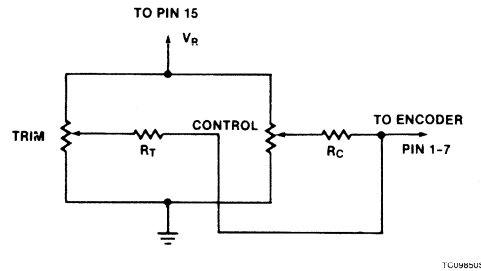


Figure 1

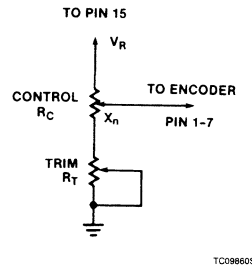


Figure 2

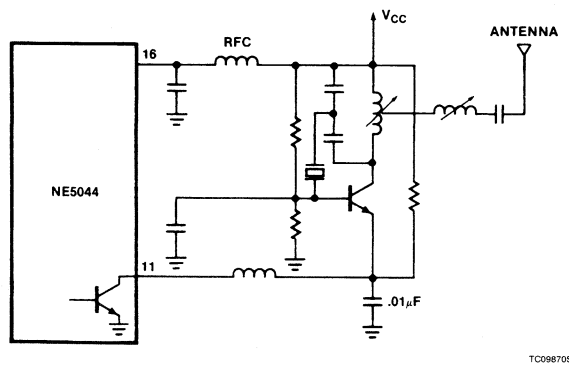


Figure 3. Modulated Oscillator Output Stage RF Transmitter

Applications Using the NE5044 Encoder

AN131

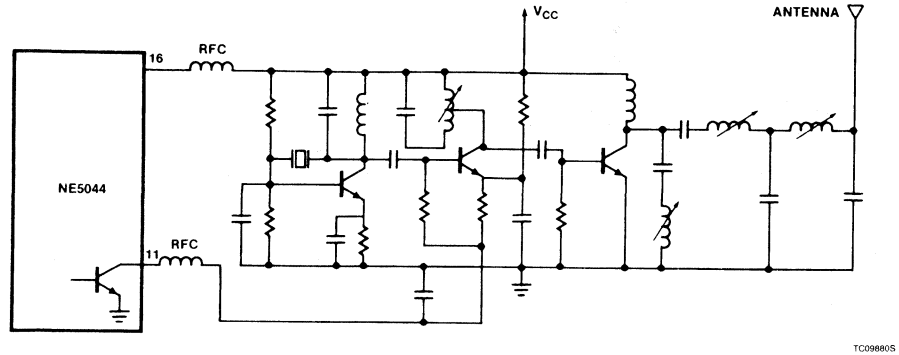


Figure 4. 5044 With High Performance RF Transmitter

In a high performance system, separate oscillator, modulator and RF output stages may be required. An example of such a circuit is shown in Figure 4. In some systems, it may be required to provide additional filtering between the encoder output (Pin 11) and the RF modulator to comply with FCC regulations.

In the previous section, a design example was given for a fixed-frame encoder (T_F constant). In some applications, it may be desirable to make the frame time variable, allowing the synchronization pulse, which follows the last channel, to remain constant. The variable-frame mode simplifies the synchronization pulse detector in the receiver since the pulse does not vary with the control inputs. However, the variable frame time may complicate the design of the pulse stretchers in the servos. The 5044 can be operated as a variable-frame encoder by discharging the capacitor C_F each time the output goes high. After the last output pulse, C_F is allowed to charge fully and the frame generator resets the encoder to channel 1. In this mode, the frame generator operates as a monostable multivibrator. Figure 5 shows the external connection. The sync pulse width (time between the falling edge of the last output pulse and the rising edge of the first pulse) is given by

$$t_S = 0.85\ R_F C_F + R_I C_{MUX}.$$

So if a sync of 6ms is desired and $C_F = 0.1\mu F$, then

$$R_F = \frac{0.85 \times 6ms - 0.047\mu F \times 27k\Omega}{0.1\mu F} \cong 39k\Omega.$$

Some applications may require an RF bypass on each of the multiplexer inputs, depending on PC board layout and the wiring between the control pots and the board. If such is the case, a $0.001\mu F$ capacitor is sufficient. Pin 12 may also require a bypass capacitor of $0.1\mu F$.

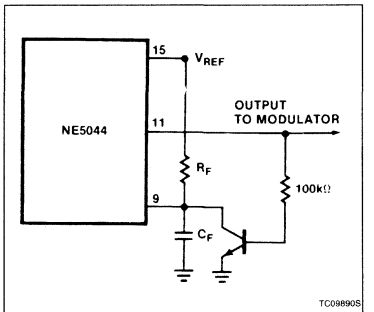


Figure 5. 5044 Variable-Frame Encoder

AN132
Applications Using the NE5045 Decoder

Application Note

DECODER APPLICATIONS

In most applications, the decoder input will be derived from the decoder of a radio receiver and will have the following characteristics:

1. Contain thermal noise at low levels
2. Will vary in level depending on RF signal strength and may contain flutter

The thermal noise can be filtered with a simple RC circuit. This filter should have a cut-off frequency of about 3kHz which is approximately the bandwidth of the receiver IF amplifier. A lower cut-off frequency would limit the information rate and resolution of the system. Figure 1 shows the external connections for the decoder input amplifier in which the abovementioned conditions are handled. Diodes D_1 and D_2 charge the 1μF coupling capacitor to the peak input voltage minus the fixed voltage at Pin 12 and the diode drops. D_2 also clamps the input signal reaching A1. The 0.2μF capacitor forms a filter which allows the amplitude of the input to vary over a wide range and at high rates (as a result of RF flutter in the receiver) without false-triggering the decoder. When flutter occurs, the baseline of the positive input pulses varies as shown in Figure 2. The 0.2μF charges up to the average baseline voltage but the 10k resistor does not allow it to be charged by the information pulses. Thus, so long as the pulse peaks exceed the baseline voltage by greater than the drop across diode D_2, the system will be unaffected by baseline flutter no matter what its rate is.

Positive feedback has also been incorporated in the connection of Figure 1 to provide 100mV of hysteresis on the threshold. When the input (Pin 13) is low, the current generator is off and Pin 11 is near ground. However, when Pin 13 goes positive, the current generator turns on and approximately 150μA is sourced. This raises Pin 11 by 150μA $\times$ 4.7kΩ = 0.7V. The threshold is now given by

$$V_{THRESHOLD\ (ON)} = V_{12} - V_{13}$$
$$\simeq (V_{12} - V_{11}) \left(\frac{1}{1 + R_4/R_3} \right)$$
$$\simeq (3 - 0.7) \left(\frac{1}{1 + 330k/51k} \right)$$
$$= 0.3V$$

So the threshold has been reduced by 100mV or the amplifier will not turn off until the input drops below 0.3V. A low pass filter is also used in the circuit of Figure 1. The 5.6kΩ and 0.01μF form a 2.8kHz low pass filter to improve the noise rejection characteristics of the detector.

A particular application of the NE5045 may not require all the components shown in Figure 1, however this circuit demonstrates all the features of the decoder which may be utilized.

Figure 3 shows a decoder connected for negative input pulses without hysteresis or flutter rejection. In this case, V_{13} is set to 3V and V_{12} is set to 3V + $V_{THRESHOLD}$.

If $V_{THRESHOLD}$ = 0.4V

$$R_4 = \frac{V_R - V_{12}}{V_{THRESHOLD}/51k} = \frac{4.1 - 3.4}{0.4/51k}$$
$$= 89k\Omega \simeq 91k\Omega.$$

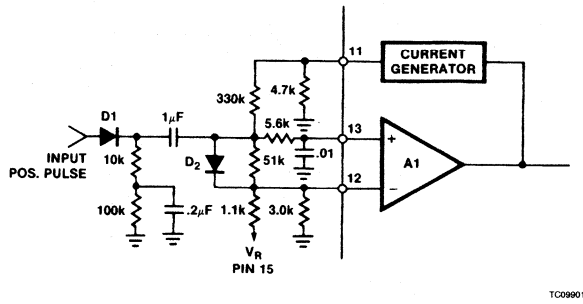


Figure 1. NE5045 Decoder Input Circuit With Flutter and Noise Filtering

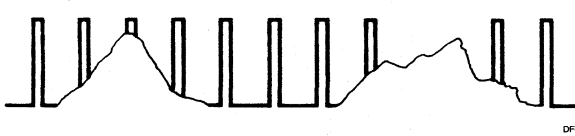


Figure 2. Input Signal With Fast Flutter

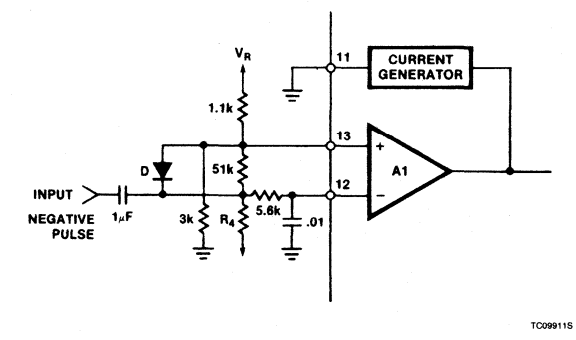


Figure 3. NE5045 Decoder With Negative Pulse Input

AN133
Applications Using the NE544 Servo Amplifier

Application Note

DESCRIPTION

The NE544 is a new servo amplifier design for digital proportional RC systems which incorporates the latest state-of-the-art in integrated circuit technology. The basic systems concept was developed in close cooperation with a number of leading manufacturers of radio control equipment.

The design philosophy behind the NE544 was to provide the RC servo systems designer with maximum flexibility in adapting the amplifier performance characteristic to his particular servo system and at the same time to keep the external components count low. To achieve this goal, all the basic servo amplifier functions, such as motor drive, deadband and minimum output pulse, are integrated into the IC, but can be modified over a wide range by using external transistors or padding resistors, respectively. This makes it possible to use the IC for extremely low cost applications as well as for the most sophisticated RC servo systems. Additional features of the circuit are very low standby power drain (typically less than 6mA), an internal voltage regulator for improved power supply rejection and a highly accurate monostable multivibrator. This circuit may be used in 2 different charging modes: linear and exponential. In the linear charging mode, the internally-generated charging current is programmable over a wide range with a resistor to ground. Usable currents range from below 10μA to above 1mA. In the exponential charging mode, the internal current source is simply bypassed with an external resistor from Pin 1 to the regulator output.

The bidirectional power output stage can supply load currents up to 500mA (NE544N package only). Output drive pins for external PNP transistors provide the user with the option of increasing the motor drive by bypassing the internal compound PNP transistors.

The NE544 also provides external pins to adjust deadband and to vary the hysteresis of the Schmitt trigger. This gives the user maximum flexibility in adapting the servo amplifier to a large variety of servo motor and gear train combinations. A dynamic brake integrated into the output stage serves to suppress inductive noise spikes and helps to improve the dynamic performance.

IC PACKAGE

The NE544 has sufficient power dissipation to handle motors with a minimum of 8Ω impedance with the integrated power transistors.

OPERATION

The basic building blocks of the NE544 servo driver are shown in Figure 1.

A positive input signal applied to the input pin (4) sets the input flip-flop and starts the one-shot time period. The directional logic compares the length of the input pulse to that of the internal one-shot and stores the result of this comparison in a directional flip-flop. The exact difference in pulse width between input and internal one-shot pulse, called the error pulse, is also fed to a pulse stretcher, deadband and trigger circuit. These circuits determine 3 important parameters:

1. **Deadband** — The minimum difference between input pulse and internally-generated pulse to turn on the output.
2. **Minimum output pulse** — The smallest output pulse that can be generated from the trigger circuit.
3. **Pulse stretcher gain** — The relationship between error pulse and output pulse.

Proper adjustment of these parameters can be achieved with external resistors and capacitors at Pins 6, 7 and 8. The trigger circuit activates the gate for a precise length of time to provide drive to the bridge output circuitry in proportion to the length of the error pulse.

TYPICAL APPLICATION AS A LINEAR SERVO AMPLIFIER

Figure 2 shows a typical connection of the NE544 as a high performance servo amplifier for remote control servo applications using the 14-pin dual in-line package. The input pulse may be DC-coupled if a reset is used in the receiver decoder. Output drive to the servo motor is applied through Pins 9 and 13 with PNP transistors T_A and T_B optional for high performance applications. The wiper of potentiometer RP is mechanically-coupled to the servo control surface, providing positional feedback. The internal one-shot in this application is operating in the linear charging mode.

LINEAR ONE-SHOT TIMING

In contrast to most conventional servo drivers which use exponential one-shots, the NE544 uses a linear one-shot. This makes it possible to design servo systems with very high positional accuracy and linear pulse width to position transfer functions. The timing of the linear one-shot can best be explained with the help of Figure 3.

The timing cycle starts after the input pulse sets the input flip-flop and releases the reset transistor T_R. This allows current I_C to charge up capacitor C_T in a linear fashion. Current I_R is programmed by resistor R_T. The op amp serves as a linear voltage-to-current converter, with the current through R_T and C_T matched identically. The inverting input of the

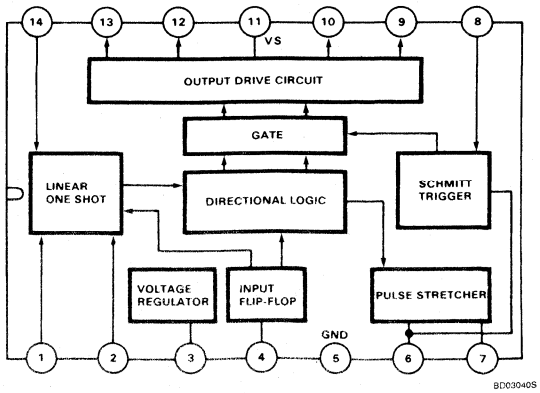


Figure 1. Block Diagram of NE544 Servo Amplifier

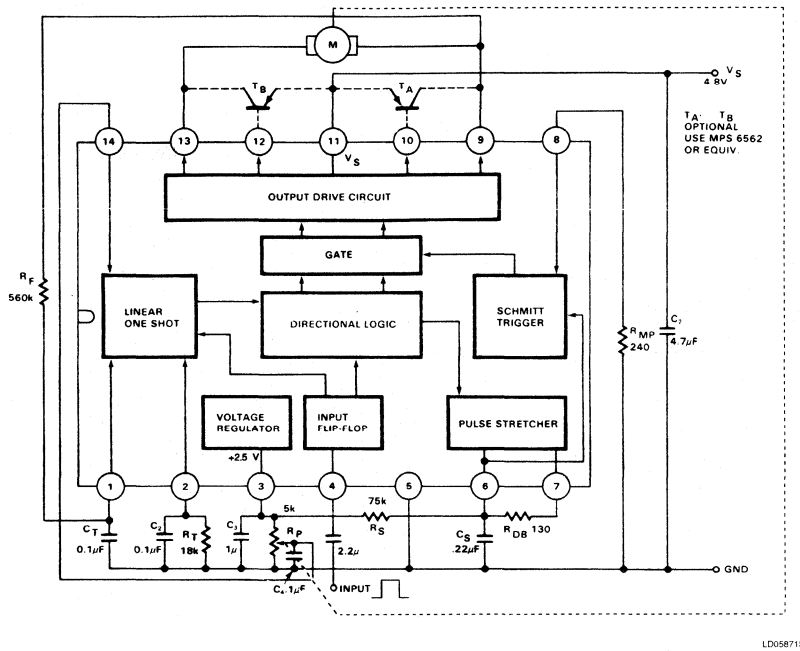


Figure 2. Typical Connection of NE544 for Linear One-Shot Timing

op amp is internally referenced to 1.8V so that the current I_R is given by this equation:

$$I_R = \frac{V_I}{R_T} = \frac{1.8V}{R_T} = I_C$$

The timing period of the internal one-shot is complete when the voltage ramp at Pin 1 reaches the threshold set at Pin 14. This time is given by this equation:

$$T = \frac{C_T V_{14}}{I_R}$$

If we substitute the typical values given in Figure 2 we obtain this equation: (V_{14} = 1.5V)

$$T = \frac{(0.1 \times 10^{-6})(1.5V)}{0.1 \times 10^{-3}A} = 1.5 \times 10^{-3}\text{sec}$$

When the internal one-shot has timed-out, the input flip-flop is reset. The reset transistor T_R is clamped to ground as soon as the input pulse goes to zero. Figure 4 shows the relationship of the input pulse, the internal one-shot pulse, the ramp at Pin 1 and the error pulse for a condition where the input pulse is longer than the internal pulse.

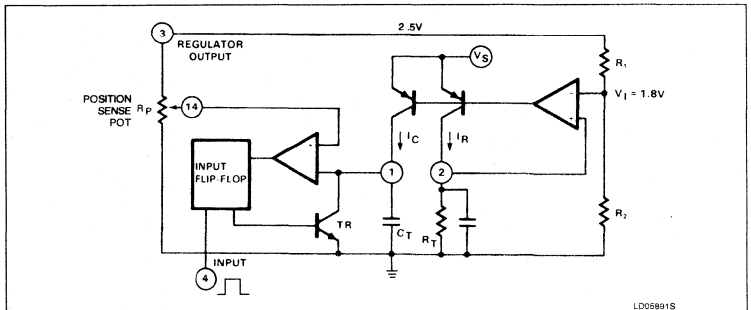


Figure 3. Simplified Circuit Diagram of Linear One-Shot

In contrast to most conventional designs, the total value of the feedback pot R_P is no longer important, since it serves only as a voltage divider. A reasonable lower limit is 1.5kΩ to keep power consumption low and to prevent loading of the voltage regulator. In the typical application, a 5k pot is used.

ADJUSTMENT OF SERVO TRAVEL

The amount of angular rotation of the feedback pot R_P (or of the servo control surface) can be changed by simply changing the charging current. Figure 5 shows a plot of the servo travel as a function of input pulse width for 3 different values of current setting resistors R_T.

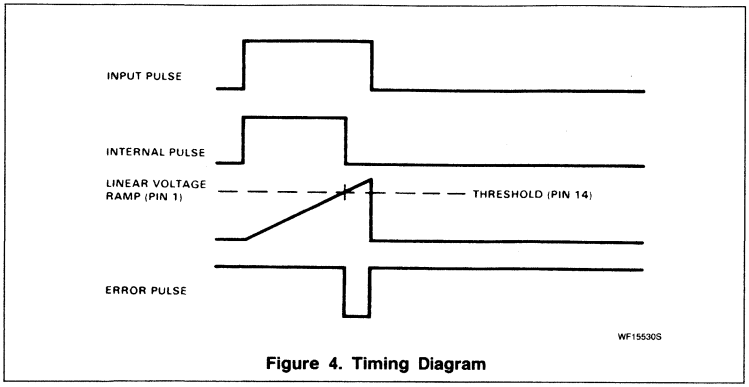


Figure 4. Timing Diagram

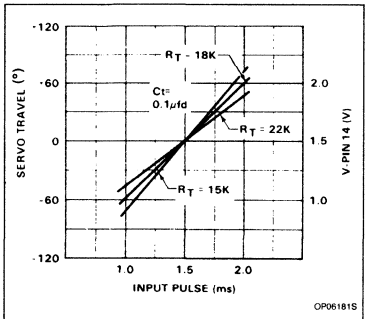


Figure 5. Servo Travel as a Function of Input Pulse for 3 Different Charging Currents

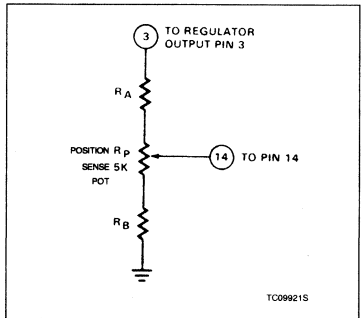


Figure 6. Increased Servo Travel Schematic

It should be noted that the center position of the wiper (1.5ms) will also shift when the amount of travel is changed. This shift may be compensated by mechanical wiper adjustment or by the addition of padding resistors as described in the next paragraph.

INCREASING SERVO TRAVEL TO MORE THAN 180°

Servo travel may be increased up to the maximum active area of the feedback pot by using padding resistors R_A and R_B as shown in Figure 6.

Figure 7 shows the values of resistors which are required to obtain a desired amount of servo travel.

EXPONENTIAL TIMING OPTION

If an exponential timing characteristic is desired, the circuit shown in Figure 8 may be used.

The time constant of the one-shot in this case is given by this equation:

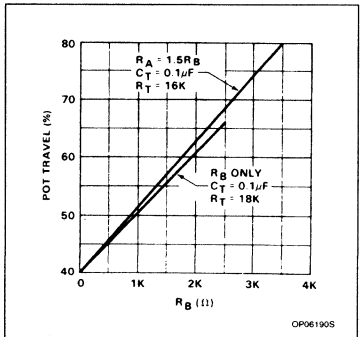


Figure 7. Pot Travel vs R_B

$$T_E = R_{TE}C_T \ln\frac{V_3}{V_3 - V_{14}}$$

Substituting the values shown in Figure 8, where V_3 = 2.5V and V_{14} = 1.5V at the center position, we obtain this equation:

$$T = (16k\Omega)(0.1\mu F)\ln\frac{2.5V}{2.5V - 1.5V} = 1.47ms$$

The center position and servo travel can be changed as described in the previous section for linear operation.

PULSE-STRETCHER

The pulse-stretcher and associated circuitry shown in Figure 9 determine important servo parameters such as minimum output pulse, deadband and error pulse-to-output pulse conversion gain.

Initially, transistor Q_S is off and capacitor C_S is charged to the regulator voltage. An error pulse from gate G turns on transistor Q_S and discharges capacitor C_S to ground through the parallel combination of R_{DB} and R_I. The deadband is determined by the time it takes for the voltage at Pin 6 to reach the trigger threshold (V_1) as shown in Figure 10.

As soon as the Schmitt trigger threshold is reached, transistor Q_S is turned off and the capacitor is discharged through a constant current source I_S until the error pulse disappears.

After the error pulse disappears, capacitor C_S is charged up through resistor R_S. The output remains turned on until the upper threshold (V_2) of the Schmitt trigger is reached. The minimum output pulse is determined by the hysteresis in the Schmitt trigger. This hysteresis may be varied over a wide range by connecting an external resistor R_{MP} from Pin 8 to ground or positive supply.

DEADBAND

Referring to Figure 10, the deadband can be calculated using the equations where T_{DB} is deadband in microseconds, C_S is the pulse stretching capacitor, I_T is the total discharge current, and ΔV is approximately 0.65V. The deadband is determined by the time it takes to discharge capacitor C_S from its initial voltage to the Schmitt trigger threshold.

$$T_{DB} \approx \frac{C_S \Delta V}{I_T}, \text{ and } I_T \approx I_S + \frac{2.2V(R_I\ R_{DB})}{R_I + R_{DB}}$$

The value of the internal deadband resistor R_I is approximately 150Ω. I_T can be calculated with this equation:

$$I_T = 3mA + \frac{2.2V(150R_{DB})}{150 + R_{DB}}$$

For the typical values shown in Figure 2, we obtain this equation:

$$I_T = 3 + 27 = 30mA$$

The deadband can then be calculated using the first equation to obtain this equation:

$$T_{DB} = \frac{(0.22 \times \mu F)\ 0.65V}{30mA} = 4.8\mu s$$

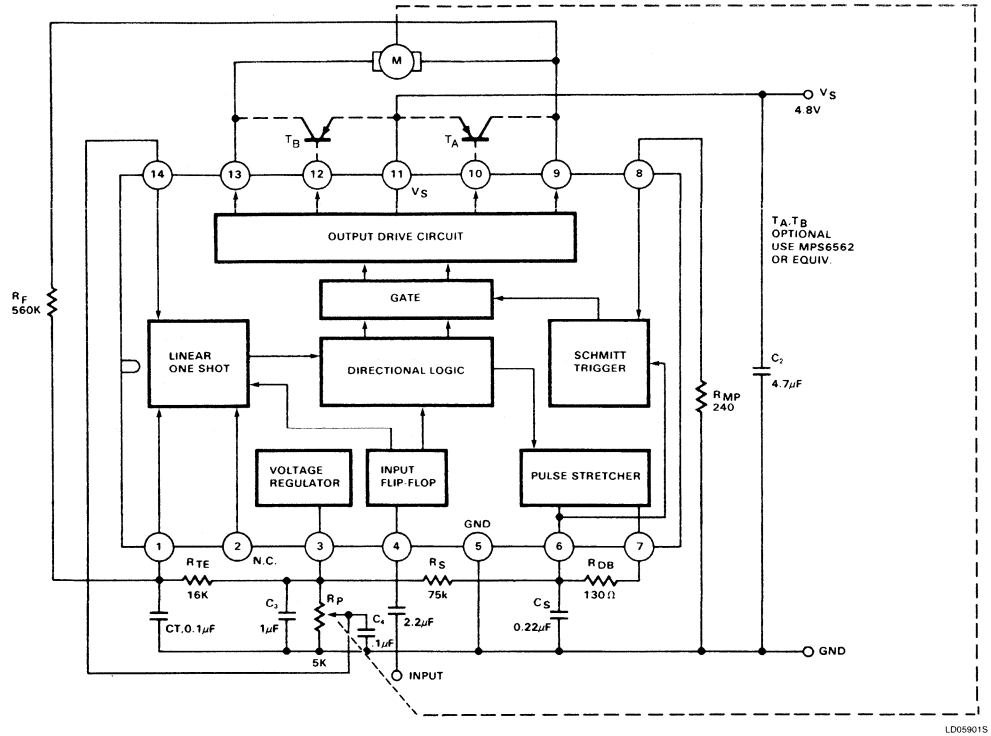


Figure 8. Typical Connection for Exponential Timing Characteristic

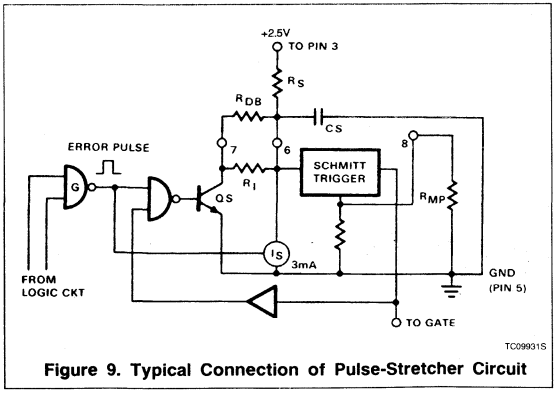


Figure 9. Typical Connection of Pulse-Stretcher Circuit

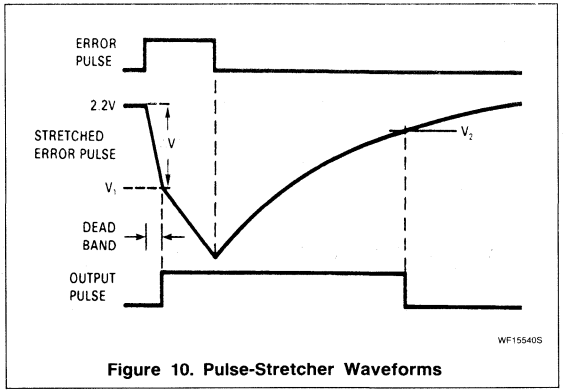


Figure 10. Pulse-Stretcher Waveforms

AN1281
NE5570: A Theory of Operation and Applications

Application Note

INTRODUCTION

The three-phase brushless DC motor must be commutated by external logic which operates from Hall sensors. In addition, torque and velocity are required.

The Signetics NE5570 monolithic CMOS controller is described with basic applications showing its adaptation to microprocessor-controlled servo systems. The controller (NE5570) is adaptable to general three-phase brushless motor control by means of a serial data input command format which provides multiple function addressing within the chip. These functions include rotational directions, 60 or 120 degrees commutation select, and current mode control to each phase on a dynamic basis by continuously programmed pulse width modulator.

INTRODUCTION TO CIRCUIT FEATURES

An 8-Bit Digital-to-Analog Converter

The internal register drives an 8-bit digital-to-analog converter (DAC). The voltage output of this converter is applied to the positive input of the error amp. This op amp is normally used for integrating the current measure at the output of op amp one. The error amplifier output drives the pulse width modulator (PWM).

For ease of use, the DAC voltage is continuously present to the error amplifier input. Even during changes of value, the transition is smooth to a new set point of the pulse width modulator. This is achieved through use of precision ratio resistors and CMOS transmission gates. The DAC can be quickly up-

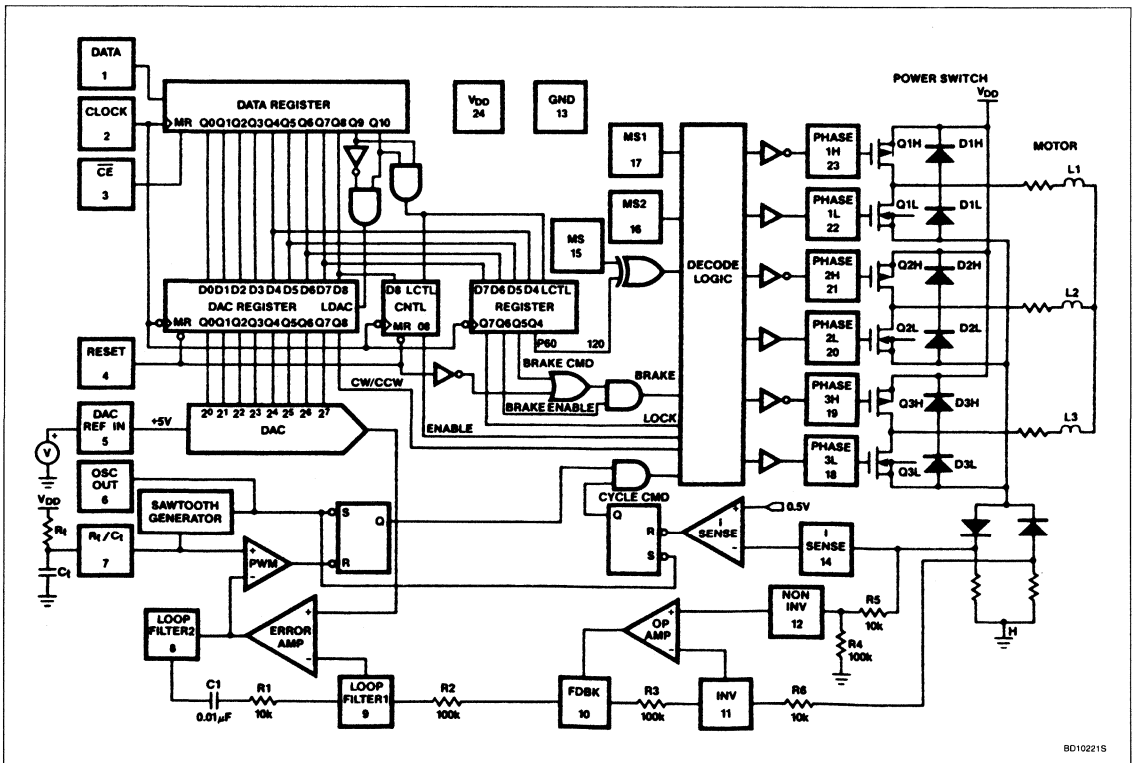


Figure 1. NE5570 Block Diagram

dated through the serial interface. The integrator time constant should be chosen to complement the motor dynamics, i.e., transient response, gain, and phase margin.

The accuracy of the DAC features excellent differential linearity. This is helpful for precision control. Integral linearity is very good; this allows consistent production tolerance for the overall system. The DAC reference input directly drives the resistor string of the DAC. The nominal reference voltage is 5V, and this is the voltage at which accuracy is specified. For consistent system performance, the reference voltage should be well filtered. Because the DAC is a CMOS design, voltages other than precisely 5V can be tolerated, however.

The Operational Amplifier

The op amp used for current sense must have a common-mode range which includes ground and negative down to 0.5V. A special design was required to meet this performance objective. The input is level-shifted with a source-follower pair and applied to a p-channel differential pair. This technique preserves the very high input impedance of a CMOS input down to −0.5V. At this voltage, the input protection network begins to draw current, and inputs should be current limited if negative spikes are present.

Output Stage

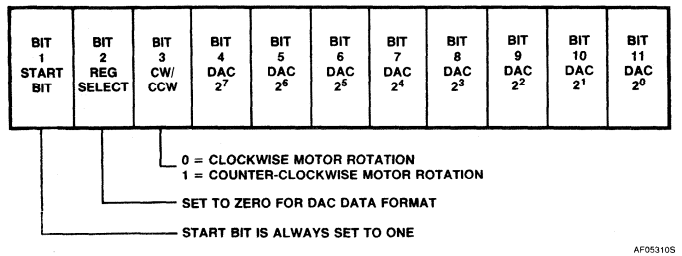
The output stage is an inverter design. It features moderate idle current with good capacitive drive capability and stability. For high resistance loads, the output can swing very nearly rail-to-rail. Outputs are tested at 100mA source-sink. (See Figure 1.)

Serial Data Entry – DAC Input

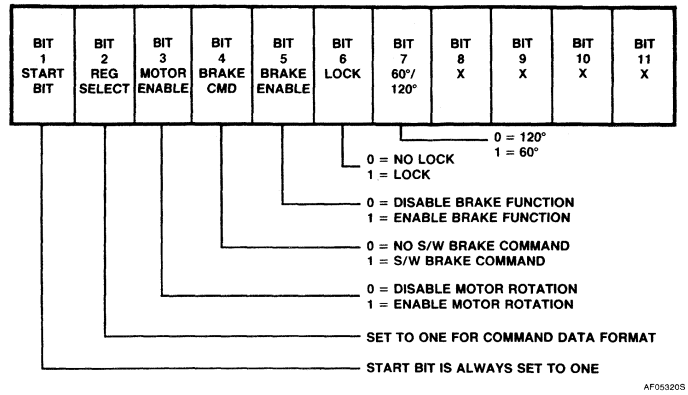
Three pins are used to allow the input of a serial word into an 11-bit serial-to-parallel data register. When CE is active, data may be clocked into the DATA pin using a rising edge clock into pin CLOCK. These three pins (DATA, CLOCK, CHIP ENABLE) are compatible with standard TTL input levels. The first two bits of the serial word select either the DAC data register or the Command control register.

In order to select the DAC register, the first two data bits must be 1 followed by a 0. The remaining nine bits are used to set the DAC to the desired level and control the direction of the motor rotation (CW or CCW). All eleven data bits must be shifted in before the DAC can be selected. The DAC register has an internal serial address of 10. (See Figure 2a.)

NOTE:
Output change will occur on the falling edge of the 11th clock bit.



a. DAC Serial Data Format



b. Command Data Format

Figure 2

The Control and Command Registers

The control register has an internal binary address of 11 (see Figure 2b). When the control register has been selected by clocking in an 11-bit serial word with the first two bits equal to 11 in binary, the command register can select any of five different motor control commands. This register can direct the outputs to switch at the oscillator frequency in order to drive the motor, lock the motor in a fixed position, smoothly brake the motor, disable the driving outputs, or switch between 60 degree and 120 degree commutating mode. When the run command is selected, the output phase pre-drivers will generate pulse width-modulated signals that can drive the gates of a six transistor FET bridge which in turn can drive the phases of the motor. The purpose of the decode logic is to take the rotor position information (from Hall effect devices) at HS1, HS2, HS3 (Figure 3a), Pins 17, 16, and 15, together with the active state of ENABLE, CW/CCW, LOCK, BRAKE, and CYCLE to determine which of six outputs to turn on or off. The PWM duty cycle is then varied to regulate the current through the motor to a preset level controlled by the previous state of the DAC register.

Command Data Format

1. The RUN command is the normal mode of operation for driving the motor. The input format for selecting run mode is shown below (Bit 3 High):

clk cycles	1	2	3	4	5	6	7	8	9	10	11
cmd data	1	1	1	0	0	0	0	0	0	0	0

Active on falling edge of 11th clock.

2. BRAKE ENABLE: The brake enable command function allows a versatile way to brake the motor during a fault or power failure condition. For example, assume that previous commands have given the DAC a value above 0. The run command can be issued with the brake enable (Bit 5) register set to 1. The outputs will switch until RESET (Pin 4) is set to a Low state. This will reset the DAC register to 0 and cause the low-phase (sink) outputs P1L, P2L, and P3L to the High state, braking the motor to a halt.

clk cycles	1	2	3	4	5	6	7	8	9	10	11	
cmd data	1	1	1	0	1	0	0	0	0	0	0	

Active on falling edge of 11th clock.

3. BRAKE COMMAND: When set High, the brake command bit (Bit 4) forces the phase outputs to go into the brake condition immediately. This may be used to gently brake the motor when a fault is detected by a software routine or a loss of motor control. When activated, the brake signal causes the 6 FET pre-driver outputs to go to the High state. This turns the p-channel drivers off and the n-channel drivers on. A moving motor will generate back EMF and current will flow through the n-channel drivers. The motor torque generated by this current opposes the motion of the motor, thus slowing it.

clk cycles	1	2	3	4	5	6	7	8	9	10	11	
cmd data	1	1	1	1	1	0	0	0	0	0	0	

Active on falling edge of 11th clock.

4. LOCK: When the lock bit (Bit 6) of the command register is set High, the outputs Phase 1H and Phase 3L will be pulse width-modulated regardless of the state of the Hall effect sensor inputs. The detent torque created will force the motor into a fixed position.

clk cycles	1	2	3	4	5	6	7	8	9	10	11	
cmd data	1	1	1	1	1	1	0	0	0	0	0	

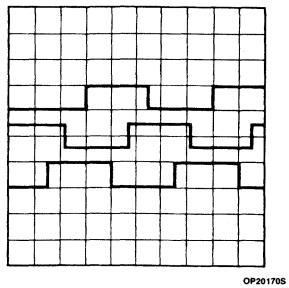
Active on falling edge of 11th clock.

5. ENABLE: Enable is a digital on/off switch (Bit 3) and can be used to insure that the outputs are completely off when no drive is required.

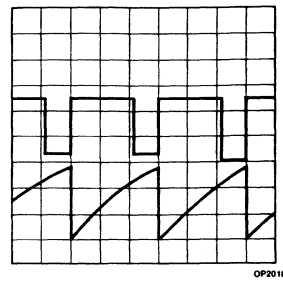
clk cycles	1	2	3	4	5	6	7	8	9	10	11	
cmd data	1	1	1	0	0	0	0	0	0	0	0	
enable)												
cmd data	1	1	0	0	0	0	0	0	0	0	0	
disabled)												

6. 60° or 120° Commutation Select (60 – 120): Setting this bit Low allows the Hall effect sensor inputs to commutate at 120 electrical degrees. When set High, the sensor inputs can be reconfigured for driving motors with 60 degree commutation cycles. This is done by connecting Hall sensor 2 to the Pin HS3. Hall sensor 3 is connected to Pin HS2. HS1 is unchanged.

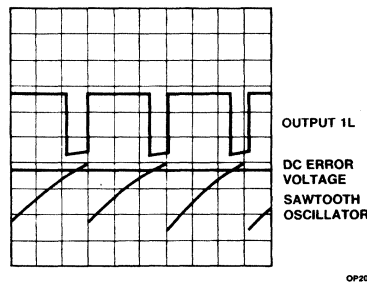
clk cycles	1	2	3	4	5	6	7	8	9	10	11	
cmd data	1	1	1	0	0	0	1	0	0	0	0	



a. Hall Sensor Commutation



b. PWM Duty Cycle Generation



c. Error Amplifier Output vs Sawtooth and Duty Cycle

Figure 3

The Sawtooth Oscillator

The oscillator develops a sawtooth waveform on pin R_T/C_T (Pin 7) by charging a capacitor C_T through the resistor R_T. The internal DC trip points of the oscillator are at $\frac{1}{3}$ V_{DD} and $\frac{2}{3}$ V_{DD}. At the end of each timing cycle, a low duty cycle output pulse is generated on "OSC OUT" (Pin 6). This output pulse sets the output of two internal R/S latches High, which makes the "CYCLE COMMAND" (internal) Active-High. This will allow the outputs to go to the last programmed state with respect to the condition of the Hall sensor inputs.

The Pulse Width Modulator (PWM) Comparator

Under current mode control, instantaneous current in the motor is summed at the input of the op amp (Pin 12) to obtain the current mode feedback signal. Thus the error loop controlling the PWM duty cycle is normally responsive to motor current (see Figure 4).

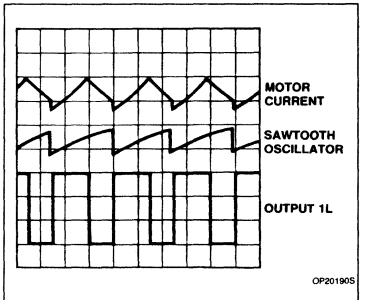


Figure 4. Motor Current vs Ramp and Duty Cycle

The output of the error amplifier (Pin 8) is compared by the PWM to the analog ramp of the oscillator. When the ramp voltage exceeds the voltage at the output of the error amplifier, one R/S latch is reset, the "Cycle Command"

is then Low and the output drivers are turned off. This condition is maintained until the next "OSC OUT" pulse is again generated by the oscillator. This prevents double pulsing at the outputs due to switching noise at the inputs of the PWM within a cycle (see Figures 3b and c).

Overcurrent Protection

The current sense comparator input (Pin 14) allows the outputs to be shut off by resetting the other R/S (overcurrent) latch. Overcurrent protection is provided by the I-sense comparator with the input connected to a voltage node that is sensitive to the forward motor current. When the voltage at Pin 14 exceeds 0.5V, the R/S latch is reset and the outputs will be turned off until the next oscillator cycle. This provides cycle-by-cycle current limiting. The 0.5V reference voltage is derived from the external 5V reference at $DAC_{REF\ IN}$ (Pin 5).

NE5570 APPLICATIONS

Driving the Brushless Motor Commutation

Today's DC brushless motor is the result of an effort to improve overall DC motor reliability by eliminating contact brushes to the armature. A secondary result is that RFI is greatly reduced. Motor manufacturers are now working to improve the rotor magnetics with rare earth materials such as neodymium iron and samarium cobalt. Inherent in the process of removing brush-type mechanical commutation to the rotating magnetics is the introduction of some method of electrically switching field polarity synchronously with rotor position. Hall effect magnetic field sensors and the necessary logic for commutation are now built as an integral part of the motor. TTL-compatible outputs make interfacing to external controllers a simple matter. With just a few logic gates driven by the Hall signals (as shown in Figure 5), an electrically-commutated brushless motor may be made to run on a single DC supply.

A Hall element gives a positive output when in close proximity to the north pole of a rotor magnet. The three-phase windings are connected in a star configuration with a 6-switch drive as shown in Figure 6. Programming the switches in the proper sequence will create a rotating vector field, driving the rotor in a clockwise or counter-clockwise direction. Phase signals are programmed as shown in the example.

PWM Controls Motor Current

With the motor commutation provided from shaft position, field coils are switched in the proper manner to develop self-synchronous rotation. This differs from the AC induction motor which is dependent on line frequency and so operates at fixed speeds that are submultiples of 50, 60, or 400Hz. For example: the brushless motor, which is synchronous with the commutation signals, develops rotational velocity based on its speed-torque characteristics much as does a DC brush motor. Speed then must be approached as a function of torque, average current, acceleration and load inertia in addition to supply voltage. High efficiency results from controlling speed by means of pulse width-modulated drive to the field windings of the motor. Normally PWM frequency is set at a rate orders of magnitude above the commutation rate. Generally, this is determined by the motor inductance and field resistance. Ideal switching rates are above the audio range, that is, 15 to 20kHz and greater.

With a fixed supply voltage, a change in the PWM duty cycle controls the average current in the motor. This develops a control variable capable of determining motor torque under varying load conditions.

Instantaneous control of duty cycle allows acceleration modeling, making an algorithm under microprocessor control a repeatably accurate technique for various ramp-up/ramp-down subroutines.

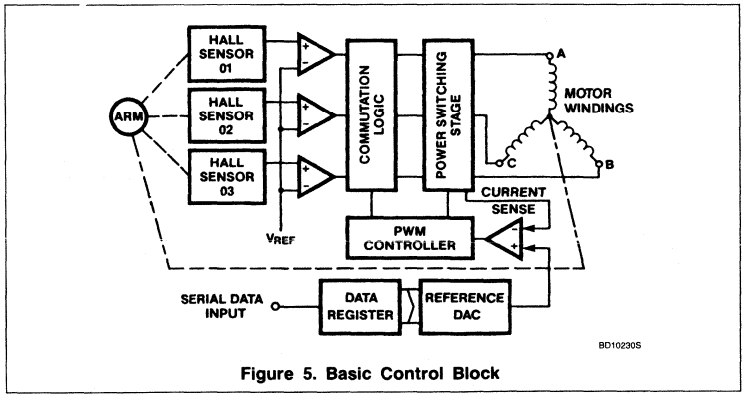


Figure 5. Basic Control Block

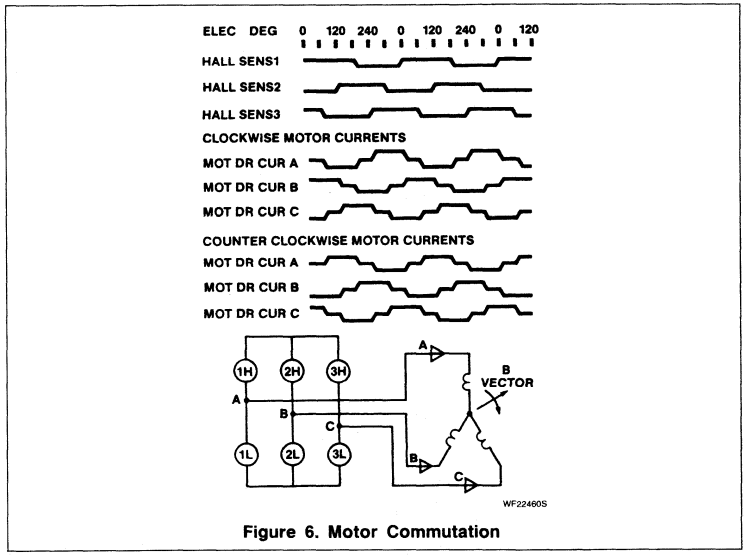


Figure 6. Motor Commutation

Constant Torque with the NE5570

Using current sense feedback to force the brushless motor switching currents to null at some average fixed level results in a constant torque output. (See Figure 7.)

With the NE5570, input commands to the current control DAC force the PWM duty cycle to generate a fixed output current to the motor. Once a current control command is received by the NE5570, the DAC latches the data into an 8-bit register and the motor is under local closed-loop control. With this configuration, a remotely located microprocessor or serial command module can generate new torque control commands and the controller will instantaneously respond with the required output current level. The NE5570 also contains internal automatic cycle-by-cycle overcurrent protection to limit the duty cycle in case of an overload such as a stalled rotor condition. This feature is independent of the DAC control signal to the PWM. Current monitoring may be carried out by use of a simple resistive shunt in the driver current return leads, or a current transformer may be implemented for developing step-up voltage gain and lower impedance.

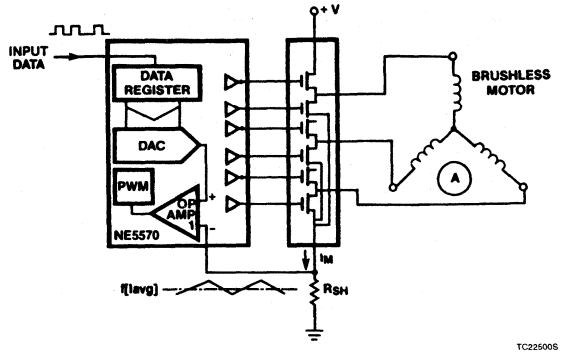


Figure 7. Current Mode Feedback Provides Constant Torque

Constant Velocity (Voltage Mode) and Acceleration Control Programming

By providing velocity feedback in addition to a motor drive current loop, an additional degree of control may be added. Velocity feedback may be derived from the commutation signals in cases where low cost is of primary concern or a tach generator may be added if increased inertia is not prohibited. A shaft encoder may also be utilized if a direct microprocessor control loop is required.

Velocity feedback may be addressed in either of two ways: Digital, where the shaft speed and position are under constant monitoring by the microprocessor; Analog loop, in which case direct voltage feedback is summed within the PWM control loop as shown in Figures 8, 9, and 10.

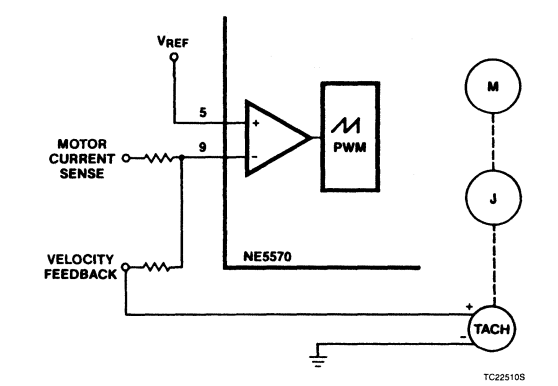


Figure 8. Summing Current and Velocity Signals in Local Analog Loop

Multiple Motors Under Serial Bus Control

The requirement to control a number of brushless motors of various sizes and at different physical locations represents an interesting challenge. An ideal solution is demonstrated in an example which uses the Inter-IC (I^2C) bus in modified form. The NMOS SCN8400 provides serial bus control using standard two-wire bus architecture, data plus clock; however, the NE5570 requires an additional chip enable signal input line (CE) in order to operate. As shown in Figure 11, this is easily implemented by using a separate I/O

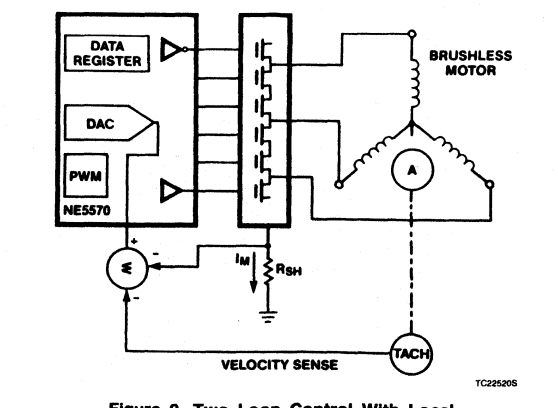


Figure 9. Two Loop Control With Local Feedback-Torque/Velocity

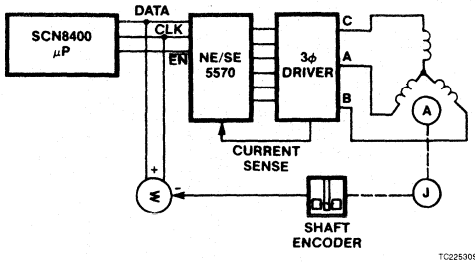


Figure 10. Velocity Feedback With Microprocessor Controller Response - Serial Bus

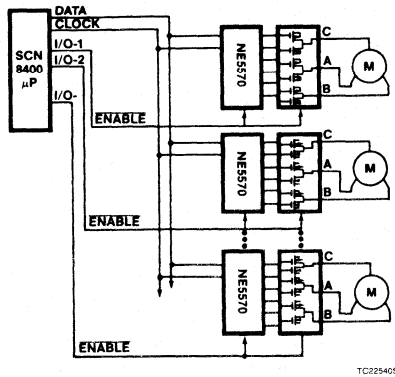


Figure 11. Multiple Controllers on Serial Bus

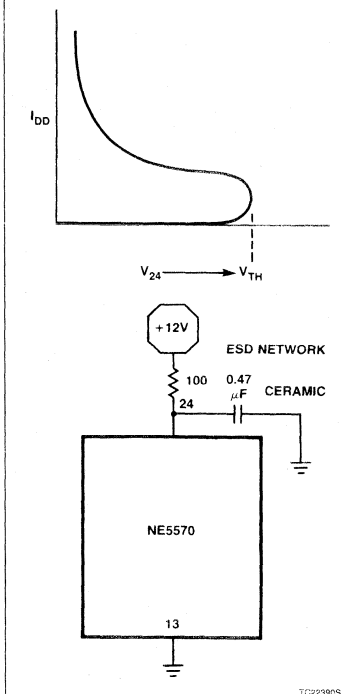


Figure 12. Recommended Protection Circuit for NE5570

port signal line for each motor control module. To select a particular motor, the I/O port sends the CE signal which enables the respective NE5570 to receive the proper input data commands. This allows several motors within a radius of approximately 10 to 12 feet to be controlled by a single I^2C processor simultaneously. (See Figure 11.)

ESD Protection

The NE5570 must be protected from external power supply transients which exceed 16V — even for a few nanoseconds (see Figure 12). This is due to the presence of a snap-back clamp circuit connected from the supply pin (Pin 24) to ground. This device forms a negative resistance switch (NPN) which, if not current-limited after turn-on, can short the supply to ground. The resulting current obviously will destroy the device.

Power-Up Sequence

In order to insure that the outputs of the NE5570 are in defined states at power-up, some timing delays must be added externally. It is essential that the V_{REF} supply (Pin 5) come up before the 12V supply. Minimum delay of the 12V supply with respect to V_{REF} is 1μs. Second, reset must be programmed Low (active) for a period lasting until both the V_{DD} supply (Pin 24) and V_{REF} (Pin 5) are active.

By adding a PNP transistor, as shown in Figure 13, with an RC delay circuit connected from V_{REF} (+5V) to the base of the transistor, initial power-up starts with the condition that the base is at 0V and the transistor is in conduction shorting Pin 4 to Ground. As the base-emitter voltage approaches 0V, Q1 turns off, setting the internal logic in the proper states. Pin 4 is now accessible to external reset signals for normal programming.

A SERIAL BUS MICROPROCESSOR

Interface for the NE5570

Figure 14 shows a completed design example of a brushless motor controller which utilizes an SCN8400 microprocessor with a piggy-back 2732 PROM as an automatic function generator. Command selection is via a small keypad attached to the PC board. The procedure calls for entry of the DAC commands in three-digit format with a range from 0 to 255. The complete controller is mounted on a single PC board as shown in Figure 15. Lock, Brake, and Disable commands, in addition to Reverse, are entered on separate keys from the DAC commands.

Clock and Data from the microprocessor (SCN8400) are all that comprise a normal I^2C bus using the standard Philips I^2C peripherals; however, the NE5570 requires a Chip Enable and this must be provided from a separate I/O port (Pin 27).

A Microprocessor-Controlled Servo with Torque or Velocity Feedback (Figure 14)

Input data loading of the command word is illustrated in Figure 14. After lowering the chip enable input (Pin 3), an 11-bit word is loaded in sequence. Data bits are latched during rising edges of the clock. After 11 clock pulses, the chip enable is deactivated by raising Pin 3 High.

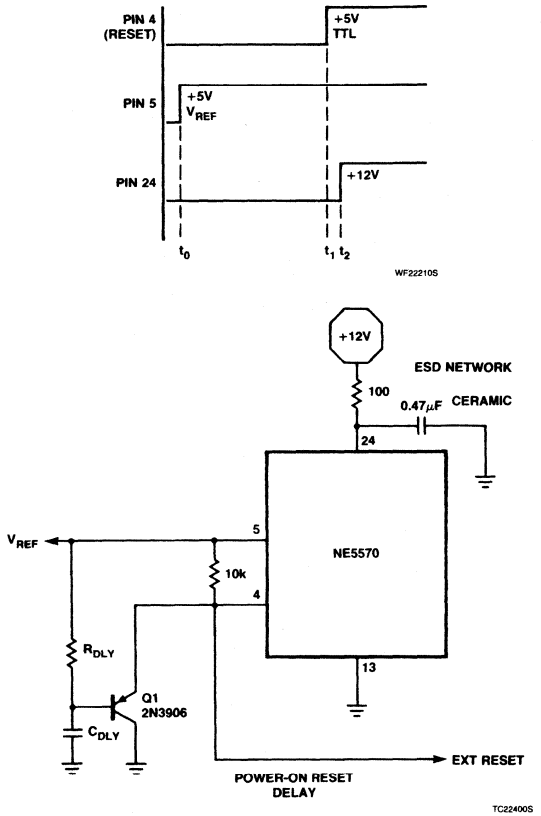


Figure 13. Supply and Reference Start Sequence

The 11-bit data word is organized into two fields: a rotation field and a speed field. From Figure 15, Bits 1, 2, and 3 determine the direction of rotation; a 101 indicates clockwise, a 100 indicates counter-clockwise. Data Bits 4 – 11 are decoded as one of 256 possible speeds, from 11 to 255.

Commands are as follow:

Lock — On this command the motor magnets oppose each other and result in the motor coming to an immediate halt in a fixed position with detent torque.

Brake — During motor operation, issuing the brake command causes the motor to come to an immediate halt, thus ending in a non-torqued or disabled state.

Disable — Issuing the disable command causes the driver FETs to immediately disengage and causes an immediate condition of zero torque. If issued during motor rotation, the motor will immediately cease to be driven and will slow to a stop from its own frictional losses.

Run — The run command tells the NE5570 to activate immediately using the command that is currently resident in the 11-bit shift register.

When coming out of a Lock, Brake, or Disabled state, the NE5570 must be given both a speed/rotation command plus an additional run command to start.

The special function commands are defined by the 11-bit words shown in Figure 17.

Interfacing to the NE5570 may be accomplished by almost any microcontroller or computer through the use of 3 I/O port lines. Emulation of the motor commands may easily be implemented via port commands. Multiple NE5570s may be implemented and controlled via a central processor by address decoding logic and the chip enable lines. As an example, Figure 14 illustrates the interfacing to an SCN8400 microcontroller via the I^2C bus. The Data input line is connected to the SDA (serial data) pin on the SCN8400 microcontroller (Pin 2). The Clock input line from the NE5570 is connected to the serial clock pin (Pin 3), and the Chip Enable input is connected to Port 2, Bit 2 (Pin 27 on the 8400). To emulate the commands via the I^2C port, a series of instructions are incorporated in a software routine called "motor" listed in Figure 18.

In this routine, the rotation control word is pre-loaded in the 3 MSBs of Register 1, and the remaining 8 bits defining speed are preloaded in Register r0. This routine accomplishes the following: disables any I^2C device that may also be on the bus by issuing the "disable address" (it is a good idea to disable any CLIPs peripherals on the bus when using the bus for any non-I^2C operations); second, toggles the chip enable High-Low-High once (an optional procedure to ensure that the shift register is initialized); third, programs the interface for a no-acknowledge mode (this tells the microcontroller to not generate an extra clock pulse for a peripheral acknowledgement; the NE5570 does not generate an acknowledgement). The routine then activates the NE5570 via port instructions, and transmits a series of 11 bits, the 3 MSBs from register f1, and all 8 bits from register r0 in high-bit to low-bit order. Assuming that these registers are properly loaded with a correct motor command, all motor control possibilities can be transmitted via this routine. To finish, the routine deactivates the chip enable line, "wakes up" the CLIPs peripherals that may be on the bus by issuing a STOP command, restores the normal I^2C mode of operation, and returns.

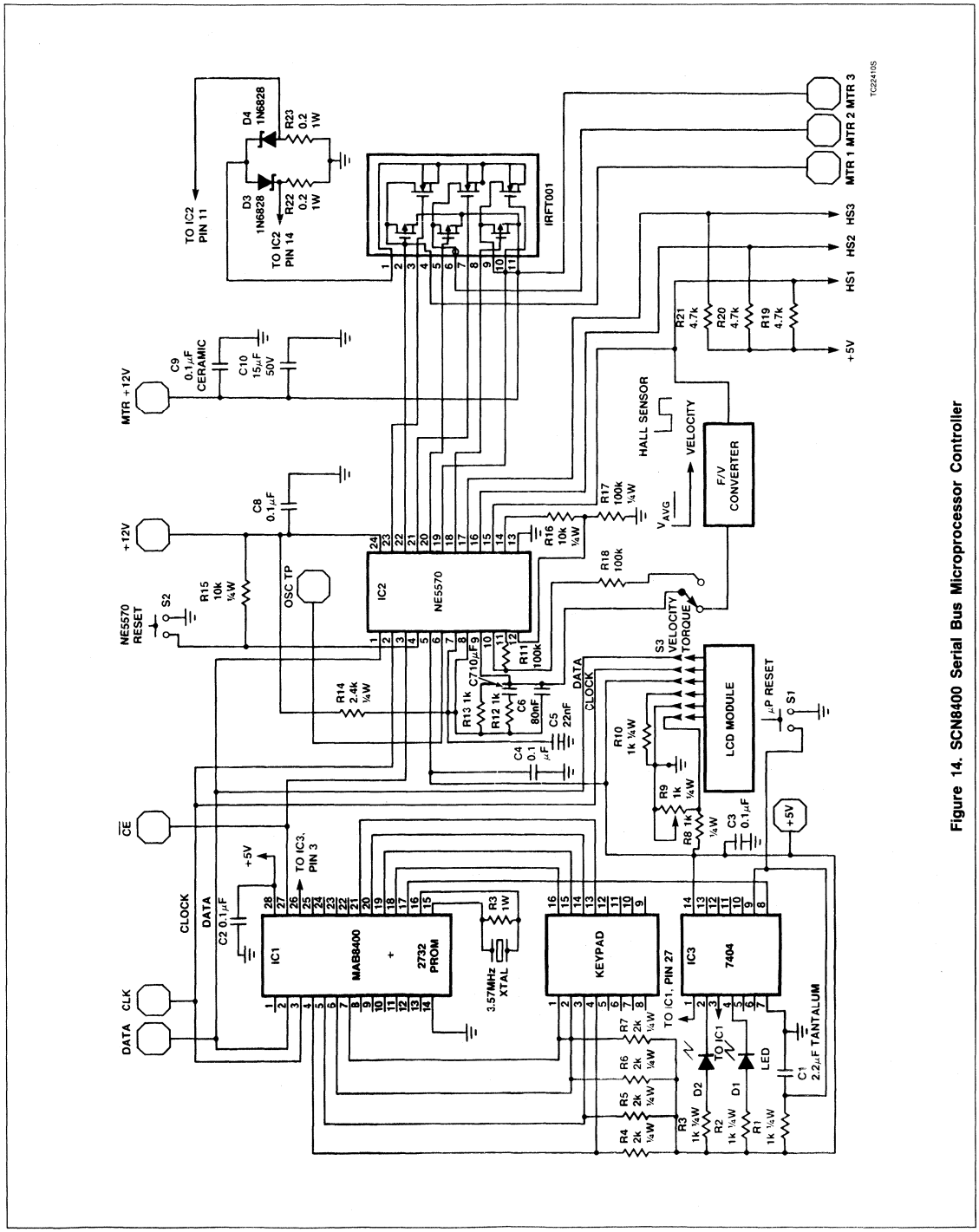


Figure 14. SCN8400 Serial Bus Microprocessor Controller

This configuration may be extended to control multiple NE5570s by simply utilizing different port lines connected directly or through a decoder to each chip enable line on the motor controller ICs. The same routine may be used; just activate the appropriate chip enables. For additional serially-loading peripherals, refer to application notes AN163 and AN1681 "TEA1017: Using the C-Bus Devices on the I^2C Bus".

NOTES:

1. Fenger, Carl, "AN163: Small Area Networks Using Serial Data Transfer," *Signetics Linear Data and Applications Manual,* Volume II, Sunnyvale, CA, 1985.
2. Fenger, Carl, "AN1681: TEA1017: Using the C-Bus Devices on the I^2C Bus, "Linear Division, Signetics Corporation, 1986.
3. Holt, Charles A., *Introduction to Electromagnetic Fields and Waves;* John Wiley and Sons, 1963.
4. Rutkowski, George B., *Handbook of Integrated Circuit Operational Amplifiers;* Prentice Hall, Inc., 1975.
5. Airpax Brushless Motors – Model K85901; Pub. Catalog CMO-834, 1983, Airpax Corporation, Cheshire, CN.
6. MotorCon '85, Official Proceedings of the 7th International Conference, Chicago, IL, Intertec Communications, Inc., Oxnard, CA.
7. PCI '82, Volume 4, Conference Proceedings, San Francisco, CA, Intertec Communications, Inc., Oxnard, CA.

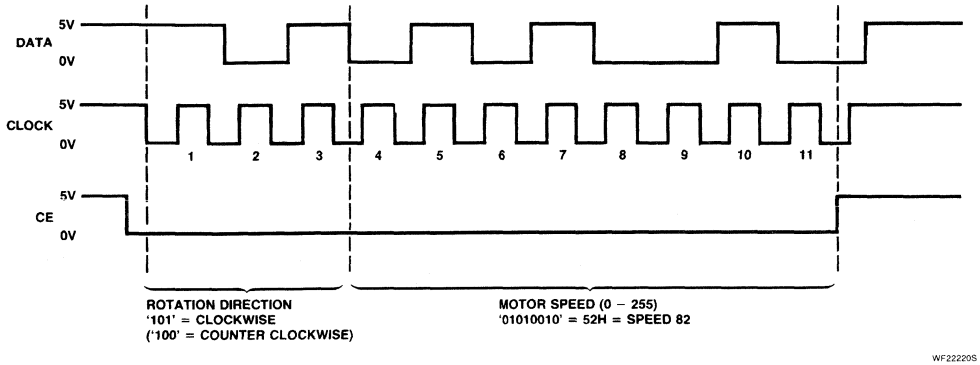


Figure 16. A Typical Command for the NE5570 Motor Controller

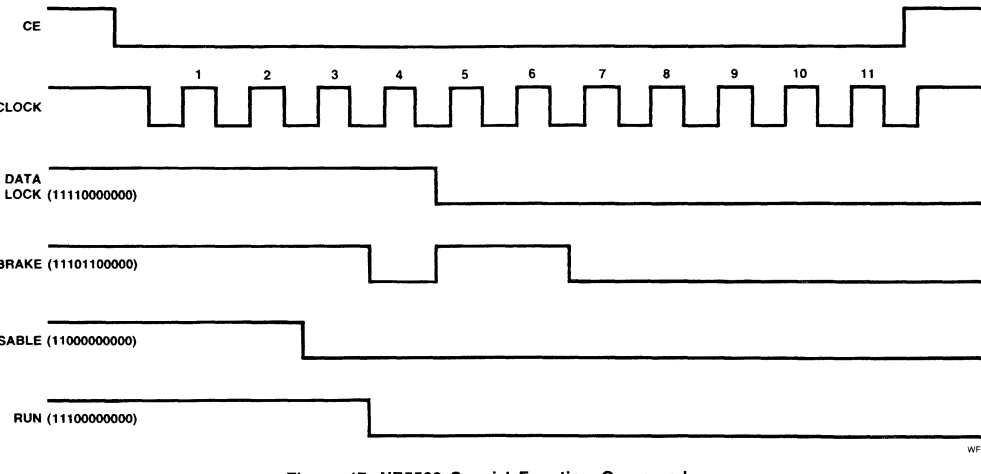


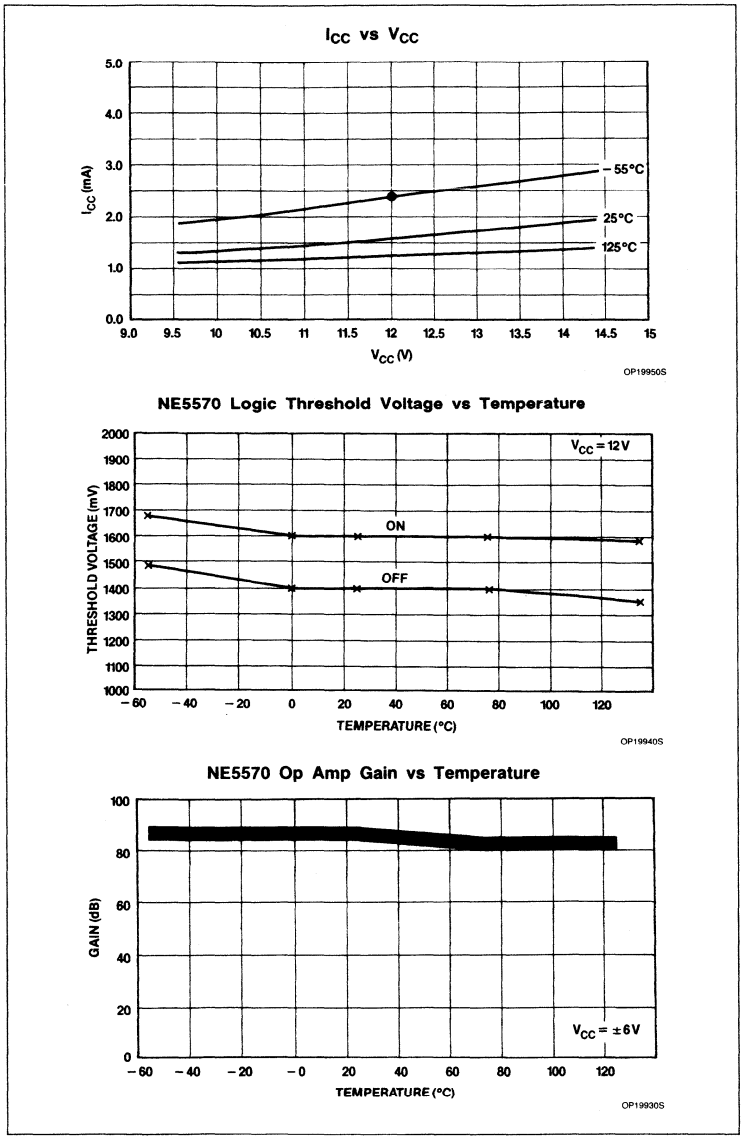
Figure 17. NE5560 Special Function Commands

```
Motor       mov s1, #H'18'          ;Reset S10 status.
            mov s0, #H'02'          ;Load iic disable.
            mov s1, #H'0F8'         ;Start condition.
            call pinwt              ;
            orL p2, #H'02'          ;
            nop                     ;
            anL p2, #H'0FD'         ;Clear motor controller.
            nop                     :
            orL p2, #H'02'          ;
        *
        *   mov s1, #H'18'          ;Initial bus status register to a know
                                    ;state.
            mov s2, #H'07'          ;Leave acknowledge mode
        *                           ;and program bus clock frequency
                                    (45kHz).
            anL p2, #H'0Fd'         ;Activate for data reception.

            mov s1, #H'0EB'         ;Prepare for a 3-bit transmission.
            mov a, rl               ;send rotation command.
            mov s0, a               ;Transmit first 3-bits.
            call pinwt              ;Wait for transmission complete.
            mov a, r0               ;Get speed command.
            mov s0, a               ;Transmit.
            call pinwt              ;Wait for transmission complete.
            orL p2, #H'02'          ;Deactivate.
            mov s1, #H'0D8'         ;Stop condition
            mov s1, #H'18'          ;reset sio
            mov s2, #H'41'          ;restore ack mode.
            ret
        *
        *
pinwt       mov a, s1               ;Wait for end of serial transmission
            jb4 pinwt               ;via polling of PIN bi in reg s1.
            ret                     ;
```

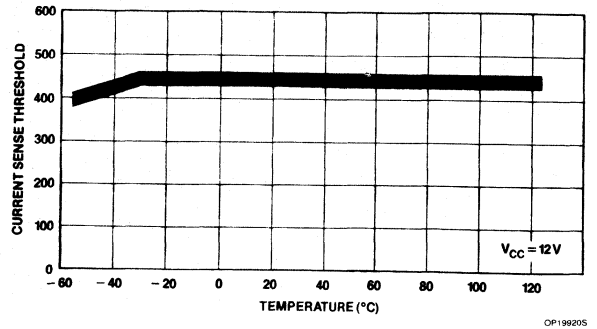
Figure 18. Motor-Controller Routine for Use on the I^2C Bus

TYPICAL PERFORMANCE CHARACTERISTICS

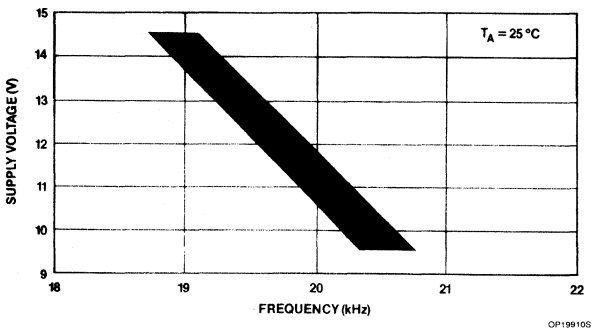


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

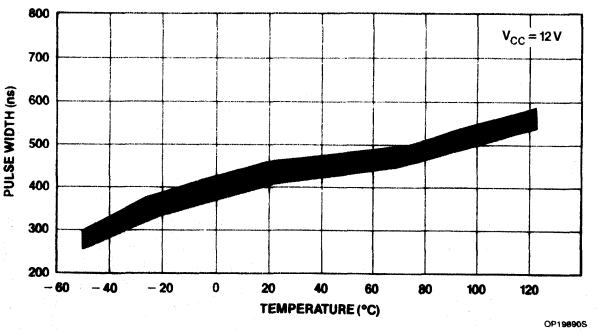
NE5570 Current Sense Comparator Threshold vs Temperature



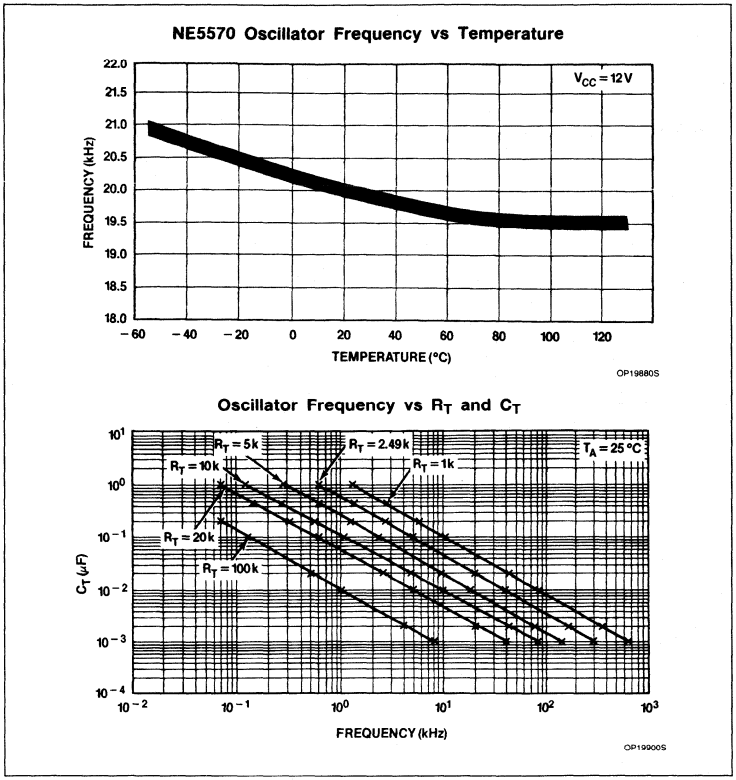
NE5570 Oscillator Frequency vs Supply Voltage



NE5570 Oscillator Output Pulse Width



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



AN1311
Low Cost A/D Conversion Using the NE5044

Application Note

Figure 1 shows an application for a multiplex A/D conversion using the pulse position encoder NE5044. In addition to its low cost per channel, the NE5044 has the following advantages:

- By grounding unused channel inputs between 3 and 7, high impedance analog inputs are available.
- Because of the serial output, only one microprocessor input is required.
- The 25mA output permits direct connection of optical couplers for optical isolation.
- The encoder in the 16-pin dual in-line package operates between 5 and 16V, but only uses 13mA.
- The non-linearity of the dual ramp conversion is between 0.1 and 0.3%.
- A voltage regulator with 20mA capability is on-chip.
- The seven analog inputs operate between approximately 1.5 and 3V with input current of 200nA.
- Open or short conditions, or connection to 5V are detected.
- The pulse which is to be measured is connected to the input T1 of the SCN8048. The instruction associated with this input, JUMP on NOT T1(JNT 1) and JUMP on T1 are used to start the 8-bit timer by using instruction start T. The instruction MOVE A, T transfers the result.

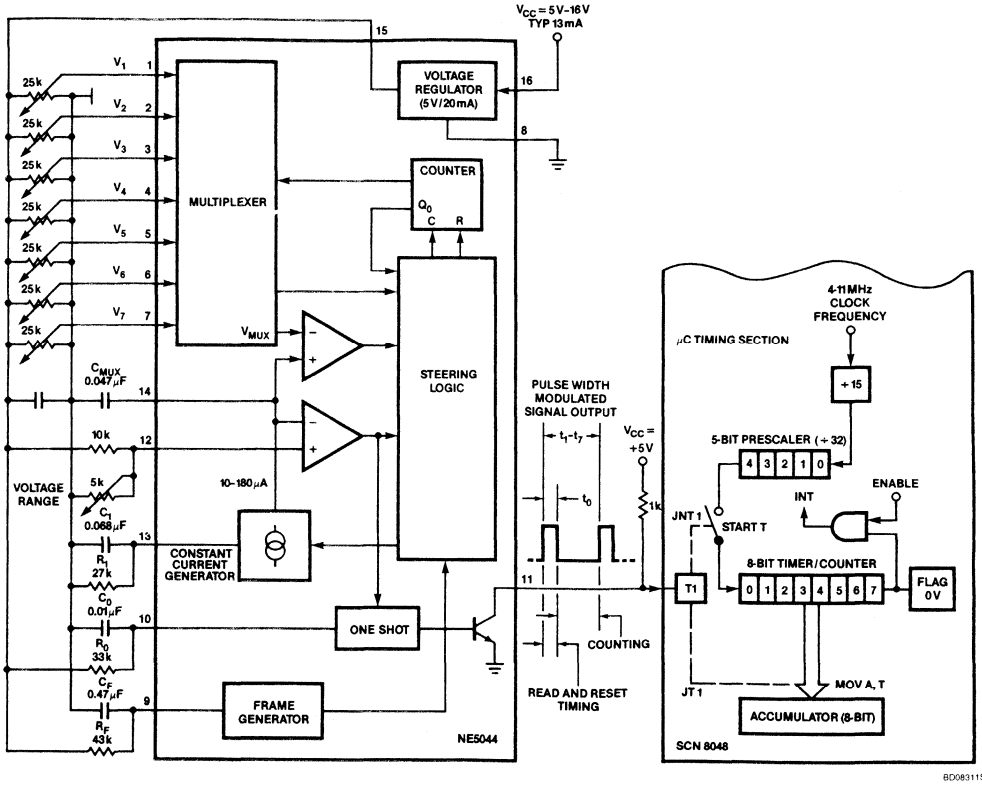


Figure 1. The 7-Channel RC Encoder NE5044 has Various Advantages. The Serial Output of 7 Analog Values is Achieved by Pulse Position Modulation Within a Frame of Typically 20ms. The Pulse Widths Permit Processing Even With Slow Microcontrollers

Low Cost A/D Conversion Using the NE5044

AN1311

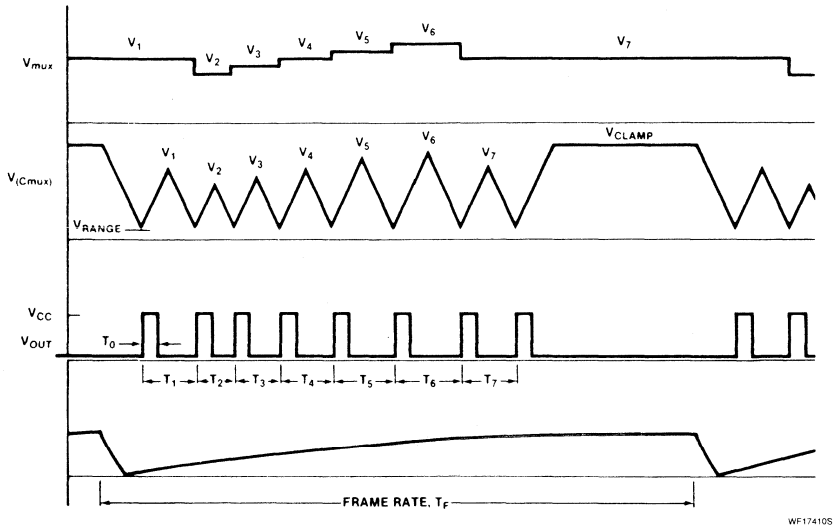


Figure 2. The NE5044 Timing Diagram

Originally published as "A/D — Umsetzer für Mikrocontroller," Klaus Petersen, Elektronik, April 19, 1985, Munich, Germany.

AN1341
Control System for Home Computer and Robotics Applications

Application Note

INTRODUCTION

With the rapid expansion of microprocessors and home computers into virtually all areas of modern life, there is an increasing need for methods of communication between computers and remote devices. Communication is usually accomplished by parallel digital data transfer and digital/analog conversion. This method is used in the case of most stationary computer peripheral devices. For movable peripheral equipment, or when communication has to cover larger distances, various forms of serial data concepts are used. The choice of a particular serial data bus system depends on cost/performance tradeoffs and possible requirements for coding and protocol standardization. In a digital system, a serial message unit typically consists of a byte of serial digital data plus additional bits for addressing, synchronization, and for other required system management functions.

In consumer applications, where low cost is an important factor, mixed digital and analog encoding methods can offer significant advantages over other serial encoding methods. The digital proportional system described here uses pulse-position modulation for serial data transfer. In contrast to pure digital encoding, where one message block (or frame) contains one byte of data, the digital proportional system packs several bytes of data into one frame. This is possible because the information is encoded in the form of pulse position.

This application note will first make a brief comparison of data transfer methods to show where the PPM transmission concept is advantageous. Then it will describe the control system that was implemented with recently developed integrated circuits. Next, it will explain the computer interface hardware and software, and, finally, it will use a robotics application as an example to point out the various features and the flexibility of the system.

Table 1. Comparison of Data Transfer Methods

TYPE	ENCODING	TYPICAL PERFORMANCE		APPLICATION
		Accuracy	Speed	
Digital bus	Parallel data	8-/16-bit	1Mbaud	Computer peripherals
Asynchronous or synchronous bus	Serial data	8-bit	300 – 1200 baud	Data communication Computer peripherals Robotics Serial ports (RS-232) Telephone modems
Computer network	Serial data	8-/16-bit	1Mbaud	Computer Communications
Digital proportional bus	Serial PPM	8-bit	3500baud	Consumer Home control Robotics

OVERVIEW OF THE CONTROL SYSTEM DATA BUSES

A comparison of various data transfer methods is shown in Table 1. The first three methods are purely digital and are mostly used for commercial data bus systems and for computer networks. The most common type of communication with a computer, besides the keyboard, is the standard parallel bus used to connect to peripheral equipment. It usually has 8 or 16 bits and typical megabaud transfer rates. For serial data transfer, asynchronous or synchronous data communication is used. Most common formats use 8 bits with modems operating at 300 to 1200baud. This is the standard method of serial communication used for peripherals, robotics, instrumentation ports, and telephone modems. The third method uses more sophisticated serial data computer networks. These networks, which are presently widely discussed in the industry, are high-performance buses with megabaud rates. They are intended for commercial computer communication, but not for low cost consumer applications.

The digital proportional bus uses pulse-position modulation for serial data transfer. It typically has 8-bit accuracy, with a speed of up to 3500baud. The serial bus is intended for low cost and medium-performance consumer applications such as home control, robotics, hobby, and educational uses. It is also used in consumer telemetry applications such as radio control. In contrast to the other buses in this table, the proportional bus uses mixed analog and digital encoding methods, which result in simple and compact hardware. The pulse positions are proportional to analog input voltages. The concept also lends itself to either amplitude or frequency modulation for remote control.

Other consumer-oriented serial buses belonging to this category are the D^2B and I^2C small area network serial buses developed by Philips[4]. These buses are digital encoding methods.

DIGITAL PROPORTIONAL ENCODING

A comparison between digital proportional and pure digital encoding methods is shown in Figure 1. Here one frame of digital data and digital proportional data are compared. The serial digital frame shown in the left part of the figure consists of one data byte plus additional bits for frame management. This format may vary when different standards are used. In contrast to this, a frame in a digital proportional system contains several bytes of data. This is because, with pulse-position coding, the data is represented by the time interval between pulses. In this case, a frame has 8 pulses and 7 bytes of data. In digitized form, each byte is 8-bit accurate. Notice that both systems have the amplitude noise immunity offered by digital encoding. One additional advantage of pulse-position coding is the fact that the analog voltage can be retrieved relatively easily anywhere in the system.

The pulse-position encoding process, which results in the pulse train shown in the figure, can be achieved using mixed digital and analog methods. Combined with a multiplex-

Control System for Home Computer and Robotics Applications AN1341

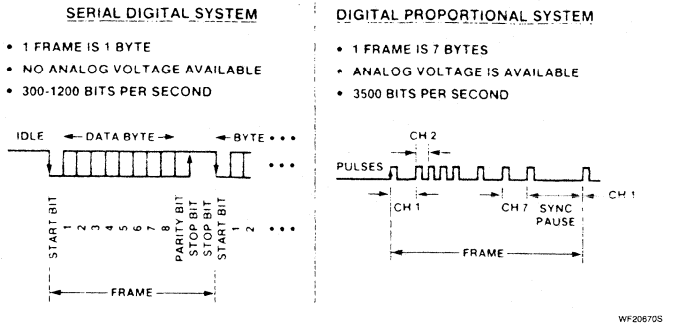


Figure 1. Comparison of Serial Digital Transmission and Digital Proportional Transmission

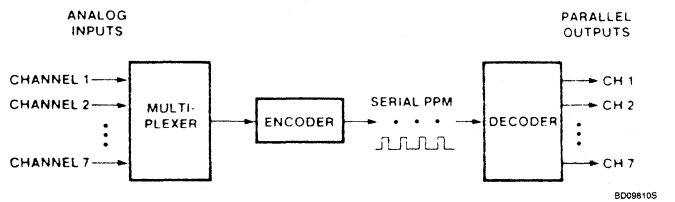


Figure 2. Standard Multiplexed Analog Proportional System

er, the standard serial data system is shown in Figure 2. Here seven parallel analog inputs are multiplexed and thus serialized. The pulse-position encoded pulses are transmitted to a decoder. The decoder converts the serial pulses into parallel pulse-width modulated outputs.

COMPUTER-CONTROLLED DIGITAL PROPORTIONAL CONTROL SYSTEM

If this bus is combined with a home computer or microprocessor, a complete serial data system is obtained as shown in Figure 3. First, digital information from the home computer is encoded in pulse position. The encoded information is transmitted over an RF link in this case. Other transmission methods such as wire, carrier current, fiber optics, or infrared can also be used. The signal is then detected, demultiplexed, and used for motion control functions, typically with a servomotor as shown. A return path for sense channel data, shown in the lower portion of the figure, uses the same encoding method but a different RF frequency. On the receiving end, pulse information is converted directly to the 8-bit digital form and fed back to the computer. The sensor data can then be processed to make control decisions. This means, with the system as shown here, all the elements of a computer remote-controlled system are present. The following section describes the building blocks required to implement this system.

IC BUILDING BLOCKS

Encoder (NE5044)

Encoder Circuit Operation

The digital-to-pulse encoder block diagram is shown in Figure 4. The encoder uses an 8-bit D/A converter and an analog-to-pulse-position converter. The encoder is a parallel input-serial output IC containing all the active circuitry necessary to generate a precise pulse-position modulated signal with seven channels. A multiplexed dual linear ramp technique is used to provide excellent linearity, minimal crosstalk, and low temperature drift. An on-chip 5V regulator, V_{REF}, eliminates power supply sensitivities and has up to 20mA current capability for driving external loads such as the RF transmitter. The encoder can be used in the fixed-frame mode, or, with the addition of one external NPN transistor, in the variable-frame mode.

The encoder inputs are either digital (i.e., inputs from the D_0, D_1, . . . , D_7 computer I/O data lines), or multiplexed analog (i.e., inputs from the CH1, CH2, . . . , CH7 manual controls). The 8-bit parallel data from the computer I/O bus is converted into analog voltage, V_A, by the D/A converter. The manual inputs are usually joysticks. Each joystick presents an analog voltage to one of the multiplexer inputs. The analog multiplexer output voltage is V_A. Each channel has an input selector switch. The two input choices are either the computer mode (i.e., input from the D/A converter), or the manual mode (i.e., input from the analog multiplexed joysticks).

The multiplexer functions as a strobed voltage follower. Each multiplexer input, when active, is high impedance, and transfers the selected input voltage to the multiplexer output. The high-impedance multiplexer inputs eliminate the loading of the control inputs. This simplifies the mixing circuits where several control voltages may be mixed into one input.

The variable analog voltage, V_A, resulting either from the D/A conversion or from the analog multiplexer, is used to set the threshold of a comparator. V_A minimum = 2V corresponds to 0, i.e., all lines = 0 on the 8-bit data bus, and V_A maximum = 3V corresponds to 256 – 1 = 255, i.e., all lines = 1 on the 8-bit data bus. The joystick range is also 2V to 3V.

Pulse-position timing is generated by alternately charging and discharging the C_{MUX} capacitor between two thresholds. The bottom threshold voltage is fixed at V_{RANGE} = 1V. The peak threshold voltage, V_A, defines each channel timing. The constant current generator, I_C, is a bidirectional current source whose current is set by an external resistor, R_I, where:

$$I_C = \pm \frac{V_{REF}}{2R_I}$$

An internal feedback loop maintains a constant current and very high output impedance. This yields a typical voltage-to-PPM encoder linearity error of less than 0.1%. An external capacitor, C_I, is required to ensure stability of the feedback loop. Independent control of I_C and V_{RANGE} allows the encoder to be tailored to virtually any combination of input voltage change and output pulse width change.

Two high-gain comparators, C1 and C2, compare the voltage across C_{MUX} with the multiplexer or the D/A output voltage, V_A, and with the range input voltage, V_{RANGE}. The input bias currents and offset voltages of these comparators are sufficiently low so as not to influence the overall accuracy of the encoder. The comparators feed the counter control logic, which counts the channels and controls the current source. The logic also controls two monostables that generate the frame timing and the output pulse timing. The logic operates as a loop: when I_C is positive (sourced from the current generator into

Control System for Home Computer and Robotics Applications AN1341

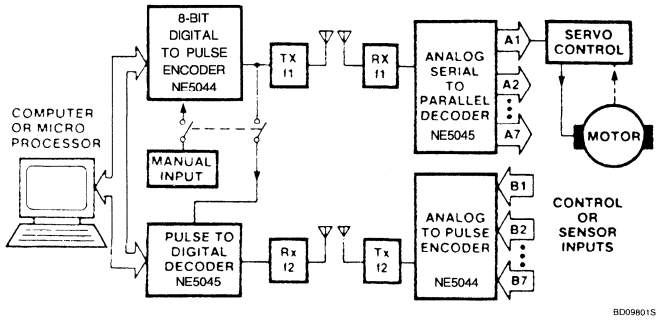


Figure 3. Block Diagram of the Analog/Digital Proportional Control System for Home Computer Applications

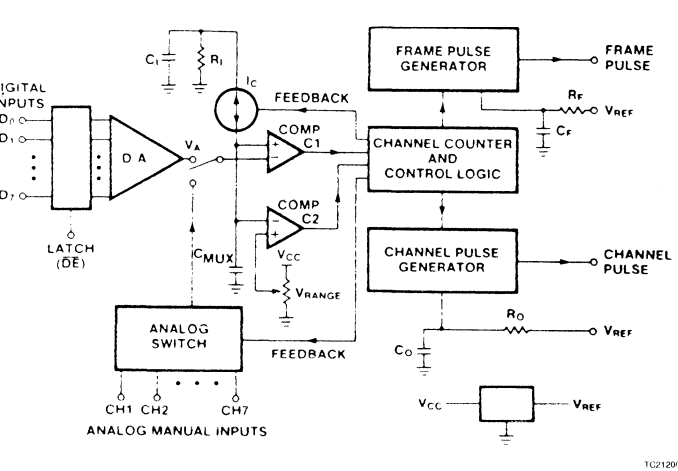


Figure 4. Block Diagram of the Analog/Digital-to-Pulse Position Encoder

C_{MUX}), the capacitor linearly charges up until it reaches a peak voltage, V_A. V_A is equal to the multiplexed output voltage for CH1, or the D/A output voltage for the first data byte. Assume this to be the voltage for channel 1, V_1. At this time the C1 comparator output goes High, which reverses the direction of I_C. I_C is then negative, sinking current into the generator from C_{MUX}. C_{MUX} then linearly discharges until it reaches the bottom threshold voltage set by V_{RANGE}. At that time the C2 comparator output goes High. This again reverses the polarity of I_C, clocks the counter, and triggers once the channel pulse generator. C_{MUX} again charges up, but then the C1 comparator output goes High when C_{MUX} reaches V_2, with the voltage on CH2. The resulting voltage waveform on C_{MUX} is a triangle wave whose positive peaks correspond to the V_A voltages on CH1 through CH7 (or to the 7 byte D/A input sequence), and whose negative peaks are constant and equal to V_{RANGE}. This waveform is shown in Figure 5.

Internal voltage clamping is used to prevent encoder malfunction if any input is shorted to supply, is grounded, or is open-circuited. This feature eliminates catastrophic failures due to opens or shorts in the control joystick potentiometers.

The frame pulse generator can operate as an astable or monostable multivibrator whose period is $0.66R_F C_F$. The encoder will generate a synchronizing pulse at the end of each frame. When V_{CMUX} reaches the seventh positive peak, it reverses and discharges to V_{RANGE}. When $V_{CMUX} = V_{RANGE}$, the counter is clocked to the state where C_{MUX} again charges up, but the output of the C1 comparator is ignored and C_{MUX} charges up to V_{CLAMP} and remains there, as shown in Figure 5. The encoder will remain in this state until a positive pulse from the frame generator is received. If R_F and C_F are connected as shown in Figure 4, the frame generator operates in the astable-multivibrator mode. It produces a narrow positive pulse output. This pulse allows C_{MUX} to start discharging again. When V_{CMUX} reaches V_{RANGE}, the counter is clocked to the state where the entire process starts over from channel 1. The frame period in this astable mode is referred to as the fixed-frame mode and as T_{FRAME} in Figure 5. The variable-frame mode, or the monostable-multivibrator mode, is discussed later.

The output of the channel pulse generator is a positive pulse width equal to $0.85R_O C_O$. The output stage is an open-collector NPN transistor capable of sinking 25mA. This configuration allows the encoder to drive a wide variety of RF stages and provides current pulses in 2-wire communication applications.

Encoder Design Equations

The triangular waveform on C_{MUX} has a fixed voltage slope (constant-current charging) and variable positive peak voltages. The time between the negative peaks of V_{CMUX}, equal to the output period for that channel, is given by:

$$t_N = \frac{2(V_N - V_{RANGE})C_{MUX}}{I_C}$$

V_N, the voltage on channel N, is either the wiper voltage on a joystick potentiometer connected between V_{REF} and ground, or the D/A output voltage, V_A. Thus $V_N = X_N V_{REF}$.

V_{RANGE} is also derived from V_{REF} so that $V_{RANGE} = Y V_{REF}$. The resulting channel time period is:

$$t_N = \frac{2(X_N - Y)V_{REF}C_{MUX}}{(V_{REF}/2R_I)}$$

$$t_N = 4R_I(X_N - Y)C_{MUX}$$

Thus, each channel pulse width, t_N, is independent of supply voltage and depends only on external passive components.

The conversion rate, CR, for each channel is the change in output period, dt_N, divided by the change in input voltage for that channel, dV_N.

$$CR = dt_N/dV_N$$

$$= (1/V_{REF})\ (dt_N/dX_N)$$

$$= 4R_I\ C_{MUX}/V_{REF}$$

In most applications, the input variable X_N will have a neutral, or center, value about which it will vary, thus:

$$X_N = X_O + X_N$$

and

$CR = (1/V_{REF})\ (dt_N/dx_N) = 4R_I\ C_{MUX}/V_{REF}$

where X_O is the neutral value for X and is assumed to be the same for all N. Now:

$$t_N = 4(X_O - Y + X_N)R_I\ C_{MUX}$$

If we let:

$$t_{NEUTRAL} = 4(X_O - Y)R_I\ C_{MUX}$$

be the neutral value for t_N, then:

$$t_N = t_{NEUTRAL} + 4X_N\ R_I\ C_{MUX}$$

It should be noted that the temperature stability of all the encoded times depends on the temperature coefficients of the respective external RC time constants. The typical temperature sensitivity of t_N using wire-wound resistors and polycarbonate capacitors is less than 100ppm/°C in the −20°C to +70°C temperature range. For the above example, this corresponds to a change in t_N of ±7.5μs for a change in temperature of ±50°C.

Interfacing the encoder to the modulator of an RF transmitter can be done in several ways depending on the desired output power, frequency stability, and oscillator leakage. The simplest method is to use the PPM output to modulate directly the bias current of a crystal-controlled oscillator. In a high-performance system, separate oscillator, modulator, and RF output stages may be required. In some systems, it may be required to provide additional filtering between the PPM encoder and the RF modulator to comply with FCC regulations. Additional filtering may also be required in computer-controlled systems, where RF transmission can cause interference between channel pulses and frame pulses.

Encoder Applications

The encoder inputs have been designed to accept a wide variety of signal sources. This can range from simple systems using as an input the wiper of a control pot, which is connected between V_{REF} and ground, to complex systems incorporating mixing, exponential processing, and/or control polarity reversing. In all cases it must be remembered that the control inputs to the encoder look like voltage-followers; that is, they draw only very small currents (less than 200nA). The voltage range for these inputs is +1.5V to +5V; however, internal clamps limit the linear control to approximately +1.5V to +3.5V. Channels 4, 5, 6, and 7 analog inputs may be used to select the desired number of output pulses by grounding one of these inputs. That is, by grounding CH4 input, only the first three inputs of the encoder will be used and a three-channel encoder results. Grounding CH5 input results in a four-channel encoder and so on. Thus, any number of channels between 3 and 7 may be selected. The selected channels will continue to be PPM encoded.

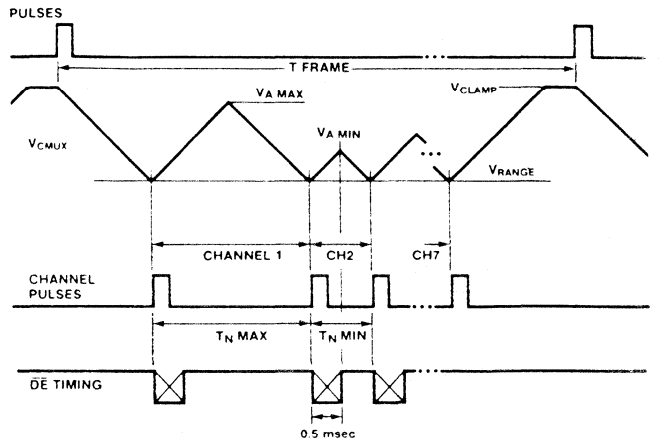


Figure 5. Encoding System Timing Diagram

In the fixed-frame mode, the frame generator functions as an astable multivibrator. In this mode, the total seven-channel time width is included in t_{FRAME} and the synchronization pause is the time difference between the seven-channel time width and t_{FRAME}. In some applications, it may be desirable to allow the synchronization pause, which follows the last channel, to have constant duration. The variable-frame mode simplifies the synchronization pulse detector in the receiver, since the total seven-channel time width is before t_{FRAME}, and the frame pulse generator operates as a monostable multivibrator. Here the synchronization pause is equal to T_{FRAME}. However, the variable-frame mode may complicate the design of the pulse stretchers in the servos. The encoder can be operated as a variable-frame encoder by discharging the C_F capacitor each time the channel pulse output goes High. After the last channel-end output pulse, C_F is allowed to charge fully and the frame generator resets the encoder to channel one.

Decoder (NE5045)

Decoder Block Diagram

Figure 6 shows the block diagram of the decoder. To decode the PPM signal, a serial-to-parallel conversion is required. The decoder separates up to seven channels of serial information into pulse-width modulated outputs. An on-chip voltage regulator, V_R, provides power supply rejection for the decoder as well as a regulated output for a radio receiver if used.

The serial PPM train, after RF detection, is fed into the decoder logic. The channel counter, the gates G1, G2, G3, and the flip-flop, make up the serial-to-parallel decoder. The channel counter is a 3-stage Johnson counter. The pulse-generator monostable provides noise immunity by blanking the input for a fixed time period. The synchronization pause-detector is required to separate successive frames and to initiate the channel count sequence. If a channel is lost due to interference, the system will synchronize again with the next frame without interruption of data. The output from the decoder is a parallel set of pulses. The width of these pulses represents the information for the control channels.

Decoder Circuit Operation

The high-gain input amplifier, A_V = 60dB, allows either positive or negative pulses to be used and has input bias currents less than 10nA. Signals as low as $20mV_{P-P}$ can be demodulated. The current generator, I_F, can be used to provide positive feedback, thereby creating hysteresis in the input switching levels. Hysteresis prevents false triggering due to noise or distortion. If positive input pulses are used, the signal is connected to the amplifier non-inverting input. In this case, the input threshold is set by the voltage difference between the amplifier input pins, established externally with a resistive divider network. Negative input signals are coupled to the amplifier inverting input. Each positive edge at the amplifier non-inverting input exceeding the voltage at the amplifier inverting input produces an output signal.

The amplifier output signal, gated by G1, sets the flip-flop. Assume, for the time, that G2 is

Low. The flip-flop setting and the pulse generator monostable produce a minimum pulse that clocks the counter. The width of this pulse is $t_M = 0.66R_M C_M$. With this arrangement, the system will not respond to any next pulse after the present pulse rising edge and before the end of t_M. In effect, the input is turned off for a period equal to t_M following the leading edge of each input pulse. The noise immunity of the decoder is thus enhanced by the ratio of t_M to the period between input pulses, t_N.

The channel counter is clocked each time the flip-flop is set, and the sync pause detector monostable is reset (capacitor C_S is discharged). The sync pause is the time between the last channel pulse in a frame and the first channel pulse of the following frame. When the flip-flop is reset, C_S begins to charge up through R_S. The time constant $t_S = 0.66R_S C_S$ is normally much larger than the time between input pulses, so the output of the pause detector remains Low until the last pulse of a given frame is received.

Q_0 will go Low and G2 will go High in a synchronized-frame system after the last channel-end pulse in a frame. Gate G1 disables the decoder input until the pause detector monostable times out; at that time G2 will go Low. This serves two purposes;

1. Establishes synchronization in no more than one frame.
2. Prevents the channel counter from overflowing due to extra noise pulses in a given frame.

Thus, any noise pulses in a frame will only affect the consecutive channels after the present channel, and only in the present frame. If fewer than 7 input channels are used, Q_0 goes High after the last channel-end pulse and the channel counter is reset when the pause detector monostable goes High. Each channel has a totem-pole output stage capable of sourcing 2mA and sinking 1mA.

Decoder Design Equations

The minimum pulse generator and the synchronization pause detector each have time periods given by:

$$t_M = 0.66R_M\ C_M$$
$$t_S = 0.66R_S\ C_S$$

respectively. The constraints on these time periods are:

t_M smaller than the minimum time width between consecutive leading edges of the serial PPM input; t_{NMIN} = 1ms in the present robotics application.

t_S greater than the maximum input pulse width; t_{NMAX} = 2ms in the robotics application.

t_S smaller than the sync pause.

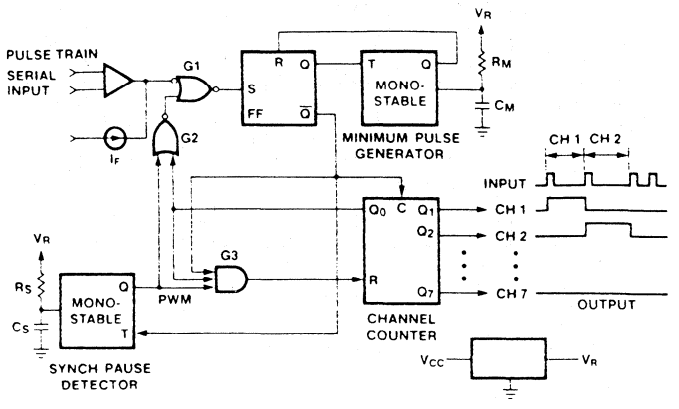


Figure 6. Block Diagram of the Pulse Position Decoder (NE5045)

Servo Amplifier (NE544)

Servo Amplifier Block Diagram and Circuit Operation

The control servo could be considered the workhorse of the remote-control system, since its function is to translate the pulse information into a usable mechanical form. A block diagram of the servo control IC is shown in Figure 7. This IC is used to convert the pulse-width information into the position of a control surface.

The input pulse width is nominally 15ms for the zero position. It is amplified and directed to a pulse comparator. The leading edge of the input pulse is used to trigger an internal feedback pulse whose length is proportional to the position of the servo control arm.

The width of the input pulse is compared to the width of the internal pulse in the pulse comparator circuit, and the difference, called the error pulse, is fed to a pulse-stretcher and Schmitt-trigger circuit. At the same time, the polarity information resulting from the pulse comparison is stored in a directional flip-flop. This polarity information is then gated by the Schmitt-trigger output for a length of time which is proportional to the error pulse. The gate output actuates a bidirectional motor drive circuit so that the servo motor can be driven in either direction with an amount of drive proportional to the error in the servo position. The position is sensed with a feedback potentiometer wiper that is mechanically coupled to the control surface.

The dynamic behavior of the servo can be adjusted by externally setting the pulse-stretcher gain and the deadband. The circuit, shown in Figure 7, converts pulse width to position.

A similar circuit can be used to convert pulse width to analog voltage. This is shown in Figure 8. In that case, the output pulse is simply integrated and its DC value is fed back to control the timing of the monostable multivibrator. The feedback is negative, and the output voltage adjusts to a value proportional to the input pulse. This circuit can be used, for example, if analog information such as voltage or current is used or displayed directly without digital processing.

Servo Amplifier Timing

For the servo amplifier in Figure 7, a monostable multivibrator was developed that can be used in the linear or in the exponential charge mode. The leading edge of the input pulse starts the process.

In the linear mode, a constant-current source, I_T, charges up the C_T capacitor. The charging is linear and the C_T voltage versus time is a ramp. When the ramp voltage reaches the comparator threshold voltage, V_{TH}, the timing cycle stops. The threshold voltage, V_{TH}, is the negative feedback voltage. The length of the timing cycle for an ideal circuit is given in the following equation:

$$t = V_{TH}\ C_T / I_T$$

The sources of timing error are: the offset voltage and the bias current of the comparator, the saturation resistance of the internal transistor that resets C_T, and the errors in the charging current, I_T. These errors can be kept to less than 0.4% by proper component design, proper process design, and matched component layout. The I_T current source can be programmed by the R_T resistor, from Pin 2 to ground. This adds flexibility since the same time constant can be obtained with a range of different capacitance and current values.

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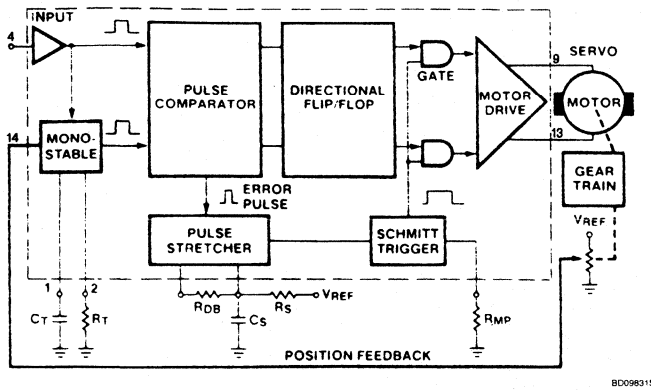


Figure 7. Servo Amplifier (NE544) Block Diagram and Pulse Width-to-Position Conversion

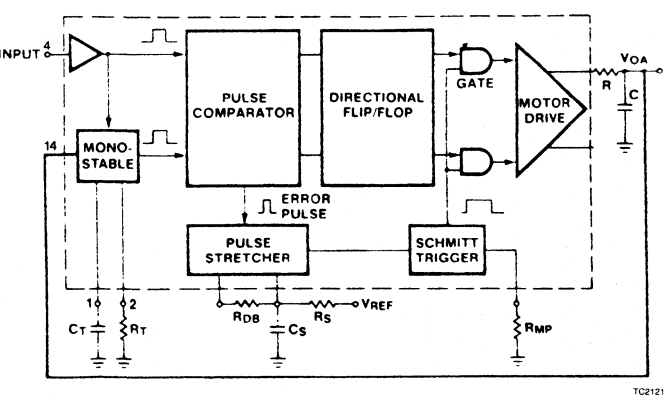


Figure 8. Servo Amplifier (NE544) and Pulse Width-to-Analog Voltage Conversion

This flexibility also permits the use of the circuit in the exponential charge mode — which might be desirable for low-cost applications. In the exponential charge mode, the R_T resistor is connected from V_{REF} to Pin 1 (see Figure 7). The R_T resistor is charging up the C_T capacitor at Pin 1. The exponential timing response is given by the following equation:

$$t = R_T C_T \ln \frac{V_{REF}}{V_{REF} - V_{TH}}$$

Otherwise, the circuit function is similar to that of the linear mode.

The remaining resistors and capacitors, shown externally to the servo amplifier IC in Figure 7, determine the relationship between the error pulse and the output pulse. This permiting adjustment of the system's dynamic performance for a variety of servo motors and mechanical components.

HOME COMPUTER INTERFACE

Interface Requirements and Hardware

This section examines how the encoder system interfaces to the computer. The encoder interfaces directly with the internal data bus of a home computer by using the peripheral I/O port as shown in Figure 9. Besides the 8-bit bidirectional data lines, D_0 and D_7, four other control lines are required to communicate with the computer. These are: two address lines, A_0 and A_1, a $\overline{\text{Device Select}}$ line, and a Phase Zero Clock line. A_0, A_1, and $\overline{\text{Device Select}}$ are 3-state lines[8]. The hardware interface to the encoder requires only two flip-flops and two OR gates (see Figure 9).

The interface peripheral card plugs into the I/O connector on the computer board. It connects the computer to the joystick console via a 14-wire, 2ft. flat cable. The plug-in card can be modified for different hardware additions, and thus can be used to accommodate various home computer interface requirements.

The hardware implementation of the computer/robot interface contains an 8-bit D/A, an analog-to-PPM converter, flip-flops, gates, one 8-bit latch, seven switches, seven joystick controls, resistors, and capacitors. The D/A output range is 2V to 3V. The 2V corresponds to the digital input word 0, and 3V corresponds to the digital word 255. For manual joystick control, there are seven analog input lines, which access the multiplexer inputs. These input lines can be individually switched between computer control and joystick control.

Interface Signals and Timing

The data flow will be explained with reference to Figures 9 and 10. The P and F flip-flops serve as storage buffers. Synchronous with the computer Phase Zero Clock, they transfer the channel and the frame data from the P and F data lines to the computer. The ribbon cable lines, P and F, tell the computer that an encoder-console pulse is present. A complete frame contains eight channel pulses and starts and ends with a frame pulse. The P line carries the pulse-position data. The P line also serves as the system clock to tell the computer when to write data. Combining these functions simplifies the hardware when compared to a standard data acquisition system where these functions are separate. The QP flip-flop is set by the encoder channel pulses. The QF flip-flop is set by the encoder frame pulses. Both QP and QF flip-flops are reset by the computer write signal, $\overline{DE} = 0$. The $\overline{AE}$ and DTR lines are the read-enable and the data-ready controls for the pulse-to-digital converter.

Figure 11 illustrates the timing sequence of the computer-encoder dialogue. The rising edge of the channel pulse causes the P signal to go High (see arrow 1). To read P, the computer reads the D_4 data line. This line is read when the P flip-flop output is enabled and strobed. For this to occur, both A_1 and $\overline{\text{DEV.SEL.}}$ must be zero. The computer senses P = 1 and starts to prepare data on the D_0 and D_7 lines (see arrow 2). After the new data is on the bus, the computer sends the write signal, $\overline{DE} = 0$, to the encoder (see arrow 3). The new data is latched into the D/A input latch. $\overline{DE} = 0$ resets the QP and QF flip-flops (see arrow 4). QP or QF go Low before the channel or frame pulse disappears. To activate $\overline{DE}$, both A_0 and $\overline{\text{DEV.SEL.}}$ are zero. The D/A input data is designated as the "$D_0 - D_7$ Latch Output" signal in the figure. The idle data latched at the QF reset is erased by the first QP reset, when data for the first channel is latched.

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Two consecutive channel pulses (within the same frame) are spaced from a minimum of 1ms to a maximum of 2ms. The frame pulses and F = 1 settings have a rate of about 50Hz. To read line F, line D_5 is selected. The D_5 line is read when the F flip-flop output is enabled by pulling both A1 and $\overline{DEV.SEL}$. Low.

CONTROL SYSTEM APPLICATIONS

General Uses

Figure 12 illustrates the available transmission media for the serial data bus. In the present application, RF transmission was chosen. The figure also represents the consumer's viewpoint. It illustrates that a reduced number of components are needed between the encoder-decoder IC chip set and the home computer, thus keeping the system price low.

Some of the applications of the control concept are listed in Figure 13. A natural use is robotics. The control system concept can be used for home control, alarm and security systems, remote-controlled video games, and remote sensing of variables such as temperature, pressure, position, or motion. Analog data can be transferred and can be used for computer-controlled models. Examples of this last application would be a "smart" mouse that can learn to negotiate a maze and Radio Control models programmed by computer.

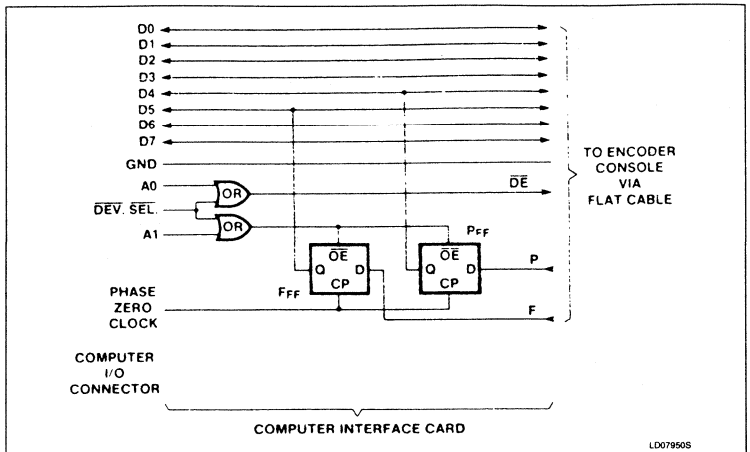


Figure 9. Computer-Encoder Interface

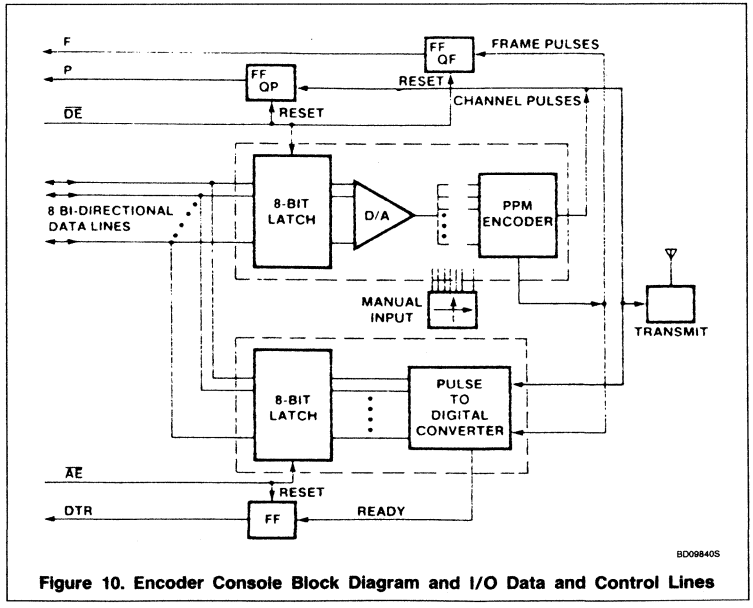


Figure 10. Encoder Console Block Diagram and I/O Data and Control Lines

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Computer-Controlled Robot

The digital proportional system is well-suited to robotics applications because of the multi-channel positioning capability and the possibility for computer remote control. Figure 14 shows the features which were incorporated in the computer-controlled robot application. The objective was to use existing home computers to remotely control a robot. The robot, which has a built-in receiver and decoder, has seven motion capabilities. These are:

1. Forward and backward drive
2. Steering
3. Head rotation
4. Shoulder movement
5. Elbow movement
6. Wrist rotation
7. Hand opening and closing

These motions can be executed in the "play" mode by either keyboard or manual joystick control. In either case, the motion can be recorded and then replayed. In the "record" mode, individual channels can be edited by simultaneously recording these channels while playing back the other channels.

The playback and the recording speed can vary. The max./min. speed ratio is 256/2 = 128. This permits recording in slow motion and playback at normal speed for precise control, or allows special effects such as slow or fast playback. Except for the drive channel, all other channels are closed-loop and can function at variable speed, with the servo motors and the servo amplifiers providing local feedback. The drive channel is open-loop and, when playing back with the drive active, the speed should be the same as the recording drive speed.

A discrete component radio control was used for the wireless robot control. The transmitter frequency and its range are based on standard radio control techniques.

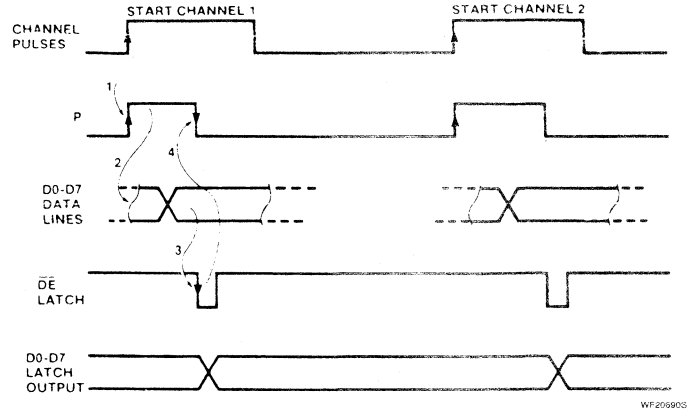


Figure 11. Computer-Encoder Interface Timing Diagram

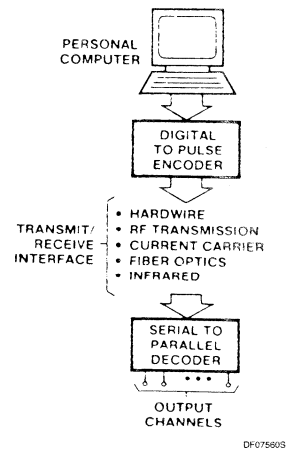


Figure 12. Available Transmission Media for the Serial Data Bus

COMPUTER PROGRAM

Computer-Robot Software Interface

To execute the different operating modes, an efficient software program is essential. The program has to be flexible and fast enough to interact in real-time with the robot. Machine language was used for the speed required to process the data. There are several operation options:

- Keyboard control over any channel combination with positive and negative steps in geometrical progression
- Joystick control over any channel combination
- Parallel recording of any channel combination from joysticks or keyboard. In the "record" mode the PPM-to-digital conversion is done by the software program
- Combined recording and playback, for individual channel editing
- Combined recording and playback, for any channel combination
- Graphic display of the pulse width of all seven channels
- Graphic display of the amount of motion-recording memory used for storage

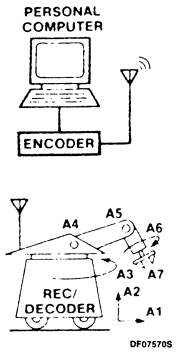
To determine how much time the "record" or the "play" modes would last in a real-time application with a home computer, two things should be defined: the available memory and the speed at which the channel data is stored-in or read-out from this memory. Approximately 19kB of memory is available for recording. One frame has 7 channels and one channel has 8 bits. The total number of frames that may be recorded in memory is: 19,000/7 = 2,714. Data is stored in memory per frame. Because one frame lasts about 20ms, the memory data is addressed at 20ms intervals.

The choice of the recording speed is available. Any speed can be specified by an integer from 1 to 255. This number, Nf,

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- ROBOTICS
- HOME CONTROL
- ALARM AND SECURITY SYSTEMS
- VIDEO GAMES (REMOTE CONTROL)
- REMOTE SENSING
  - TEMPERATURE
  - PRESSURE
  - POSITION, LIGHT, ETC.
- ANALOG DATA TRANSFER (VOLTAGE/CURRENT)
- COMPUTER CONTROLLED MODELS

Figure 13. General Control Applications of the Serial Data Bus



- PLAY MODE
  - COMPUTER (KEYBOARD) CONTROL
  - MANUAL JOYSTICK CONTROL
- RECORD MODE
  - EDITING
  - VARIABLE RECORDING SPEED

REMOTE MOTION CAPABILITIES
A1 - FORWARD/BACKWARD MOTION
A2 - STEERING (90°C)
A3 - HEAD ROTATION (360°C)
A4 - SHOULDER (ARM) MOVEMENT (110°C UP/DOWN)
A5 - ELBOW MOVEMENT (110°C UP/DOWN)
A6 - WRIST ROTATION (360°C)
A7 - HAND (CLAW) - OPEN/CLOSE

Figure 14. Features of the Computer-Controlled Robot Application

represents the number of frames to be skipped between memory updates in terms of 20ms increment per frame. The computer will record one out of every Nf + 1 frames, or play the same channel data Nf + 1 times before incrementing to the next set of channel data in memory.

For example, at speed = 1, the memory usage is fast, every 2nd frame or 2 × 20ms = 40ms. The memory capacity is used up after 2,714 × 2 = 5,428 frames or in 5,428 × 20ms = 108s of real-time. At speed 255, the memory usage is slow, every 256th frame or 256 × 20ms = 5.12s. The memory capacity is used up after 2,714 × 256 = 694,784 frames or in 694,784 × 20ms = 3h:51min of real-time. For a 90° mechanical arm rotation, a 1s minimum time was observed. One frame update per second means a speed of 1s/20ms = 50. At this speed, the memory capacity will be used up in 2,714s = 45min real-time.

Real-Time PPM-to-Digital Software Conversion

Pulse-position modulation can be converted directly to binary form by counting the time between channel pulses. The software program divides the 1ms-2ms time interval between two channel pulses into about 190 bits, through a numerical algorithm. The peak counting error is ±2 bits. Clock pulses are counted and the total is adjusted to fit a 0 - 255 scale.

Floppy disk operations, to save or load data records, are done under a disk-operating software program already written for the particular home computer used. At this time the computer is instructed to perform disk/memory data transfers and not to control the robot. In the present program, configuration disk/memory data transfers and robot control cannot be done at the same time.

System Control Program

The overall program uses both BASIC and machine language. The use of BASIC is confined to the program portion, which takes user inputs for defining the various operating modes. The program sections that control data flow to the robot are written in machine language. This is necessary because, with the PPM-to-digital conversion, less than 50μs are available to present data to the bus after a channel pulse is received. If executed in BASIC, the instruction cycle of the channel play loop would take in excess of 1.5ms which is much too long. Machine language becomes even more essential if a full-duplex system is used, because such a system requires processing of sensor information simultaneously with the execution of a motion program.

The BASIC Program

The BASIC program section takes user inputs to set up the system configuration. Initial options include: playing the channel data program stored in memory, loading an old channel data program from disk into memory, saving the memory program on disk, or recording a new program in memory. If the "record" option is chosen, then the computer asks for the channel numbers to be recorded. Individual play/record channel control allows the user to record one or more channels and play the rest from memory. This feature permits re-recording of individual channels so that an entire seven-channel program doesn't have to be redone because of an error in one channel. Channel data for recording can be entered by joystick or from the keyboard.

The Assembly Program

Figure 15 shows a flow diagram of the machine language section of the program, and Figure 16 shows the data management sequence. In addition to the main memory locations for channel data storage ($4000 – $9000), two memory buffers are used for input and editing. The keyboard buffer ($300 – $306) holds data entered from the keyboard during a recording sequence, and the scratchpad buffer ($19 – $1F) is used for channel data storage during each frame.

The program sequence begins with a memory pointer set to $4000. When the computer senses a positive-going frame edge, the DE line is pulled Low to reset the QF flip-flop and, when an internal frame counter equals Nf + 1, seven bytes of data are moved from memory (pointer to pointer +6) to the scratchpad buffer. The program uses the time before the first channel pulse arrival to update the screen graphics and scan for keyboard input. The screen display shows a bar graph of the control surface relative position (from –1 to +1 for each channel), and of the storage memory usage. Valid keyboard inputs include channel number, increment or decrement, steps from 0.5% to 10% of the whole 1ms range, and "return". If a "return" is sensed, then the accumulator is loaded with the scratchpad byte for the last keyboard-specified channel number. The last specified increment/decrement amount is implemented and the new data is stored in the appropriate scratchpad location.

The program sets a channel counter equal to zero and waits for the first positive-going pulse edge. Upon sensing the positive-going pulse edge, the computer increments the channel counter and checks whether the first channel has been selected for "play" or "record". If channel one has been specified as "play", the data in the first scratchpad location is loaded onto the data bus and the $\overline{DE}$ line is pulled Low, latching the data as encoder input. The PPM-encoded data is sent to the robot. If "record" has been specified for channel one, then the counter checks if keyboard or joystick has been specified as an input option. For keyboard recording, the first byte in the keyboard buffer is copied to the first position in the scratchpad buffer. The byte is also put on the data bus and sent to the robot by pulling the $\overline{DE}$ line Low.

For joystick recording, the computer software must do a PPM-to-digital conversion (A/D). This is initiated by zeroing an internal counter and pulling the $\overline{DE}$ line Low to reset the QP flip-flop. A small loop alternates between incrementing the counter and scanning for the next positive-going pulse edge. When the positive-going edge is sensed, the loop is broken and the count will be proportioned to the time between pulses. The joystick record sequence is then completed by incrementing the channel counter. The same sequence is followed for each channel. When the channel counter specifies that the eighth pulse has arrived, the seven bytes from the scratchpad buffer memory are copied back into the storage memory (pointer to pointer +6), and the pointer is incremented by seven. The computer waits for the next Nf + 1 positive-going frame edge, after which the entire sequence is repeated. The programming/play sequence ends when either the keyboard scan senses a press on the space bar, or the storage memory capacity has been reached (approximately one and one-half minutes at full speed), or an end marker is read into the first position in the scratch pad buffer. Upon manual termination (space bar press), a zero is stored after the last valid channel as an end marker.

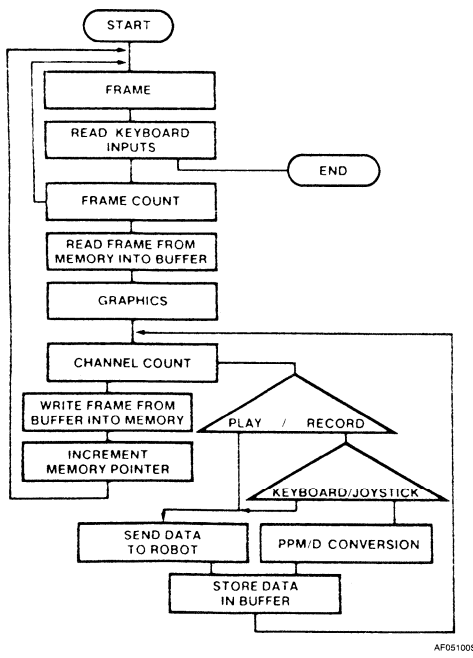


Figure 15. Flow Chart of the Robot Control Computer Program

	FRAME 1	FRAME 2	FRAME 3
STORAGE MEMORY ($HEX)	4000 - - -	4007 - - -	400E - - -

SCRATCHPAD BUFFER ($HEX)	19	1A	1B	1C	1D	1E	1F
CHANNEL NUMBER	1	2	3	4	5	6	7
KEYBOARD BUFFER ($HEX)	300	301	302	303	305	306	

DATA MANAGEMENT SEQUENCE

1. Move data from storage ($4000-4006) to scratchpad ($19-1F).
2. Operate on scratchpad data
   a. Record joystick: PPM-to-digital count = $18,X. X=channel no.
   c. Playback: $18,X-PPM serial to robot.
3. Move scratchpad data back to storage memory pointer: $4000-$4007
4. Increment storage memory pointer
5. Goto 1.

Figure 16. Software Data Management Sequency and Memory Allocation

Switched-mode power supply circuits

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SG2524C	SMPS controller	999
SG3524	SMPS controller	1006
SG3524C	SMPS controller	999
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AN120
An Overview of Switched-Mode Power Supplies

Application Note

Conceptually, three basic approaches exist for obtaining regulated DC voltage from an AC power source. These are:

- Shunt regulation
- Series linear regulation
- Series switched-mode regulation

All require AC power line rectification.

The series switched-mode regulators will be referred to as switched-mode power supplies or SMPS during the course of this article.

Briefly stated, if all three types of regulation can perform the same function, the following are some of the key parameters to be addressed:

- From an economical point of view, cost of the system is paramount.
- From an operations point of view, weight of the system is critical.
- From a design criteria, system efficiency is the first order of business.

The series and shunt regulators operate on the same principle of sensing the DC output voltage, comparing to an internal reference level and varying a resistor (active device) to maintain the output levels within prespecified limits.

Switched-mode power supplies (SMPS) are basically DC-to-DC converters, operating at frequencies in the 20kHz and higher region. Basically, the SMPS is a power source which utilizes the energy stored during one portion of its operating cycle to supply power during the remaining segment of its operating cycle.

Linear regulators, both shunt and series, suffer when required to supply large currents with resultant high dissipation across the regulating device. Efficiency suffers tremendously. (Efficiencies less than 40% are typical.)

Switched-mode power supplies operate at much higher levels of efficiency (generally in the order of 75% to 80%), thereby reducing significantly the energy wasted in the regulated supply. The SMPS does, however, suffer significantly in the ripple regulation it is able to maintain, as opposed to a much higher degree of regulation available in series (or shunt) linear regulators.

The linear regulators obtain improved regulation by virtue of the series pass elements always conducting, as opposed to SMPS devices having their active devices operative only during a portion of the overall operating period.

Some definitions and comparisons between linear regulators and switched-mode power supplies follow for reference.

REGULATION

Line Regulation — (Sometimes referred to as static regulation) refers to the changes in the output (as a percent of nominal or actual value) as the input AC is varied slowly from its rated minimum value to its rated maximum value (eg. from $105VAC_{RMS}$ to $125VAC_{RMS}$).

Load Regulation — (Sometimes referred to as dynamic regulation) refers to changes in output (as a percent of nominal or actual value) when the load conditions are suddenly changed (eg. minimum load to full load.)

NOTES:
The combination of static and dynamic regulation are cumulative; care should be taken when referring to the regulation characteristics of a power supply.

Thermal Regulation — Referred to as changes due to ambient variations or thermal drift.

TRANSIENT RESPONSE

The ability of the regulator to respond to rapid changes in either line variations, load variations, or intermittent transient input conditions. (This parameter is often referred to as "recovery time.")

AC PARAMETERS

Voltage Limiting — The regulator's ability to "shut down" in the event that the internal control elements fail to function properly.

Current Limiting — Often referred to as "fold-back", where the amplifier segment of the regulator folds back the output current of the device when safe operating limits are exceeded.

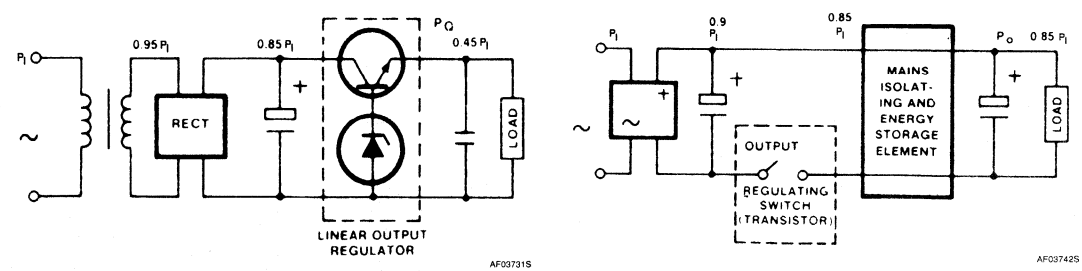
Thermal Shutdown — The regulator's ability to shut itself down when the maximum die temperature is exceeded.

GENERAL PARAMETERS

Power Dissipation — The maximum power the regulator can tolerate and still maintain operation within the safe operating area of its active devices.

Efficiency — The ratio (in percent) of the usable versus total power being dissipated in a regulated supply. (The losses can be AC as well as DC losses.)

EMI/RFI — Generation of ElectroMagnetic/Radio Frequency Interference signals and magnetic field disturbance in SMPS devices. (Transformer and choke design are available which reduce both RFI & EMI to safe acceptance regions.)



a. Conventional Supply — 45% Efficiency **b. Switched-Mode Supply — 80%Efficiency**

Figure 1. Losses in Regulated Power Supplies

An Overview of Switched-Mode Power Supplies

AN120

The balance of this section will be dedicated to the discussion of the general operation of Switched-Mode Power Supplies (SMPS) with emphasis on the Signetics NE5560 Control and Protection Module.

Switched-mode power supplies (SMPS) have gained much popularity in recent years because of the benefits they offer. They are now used on a large scale in desk calculators, computers, instrumentation, etc., and it is confidently expected that the market for this type of supply will grow.

The advantages of SMPS are low weight and small size, high efficiency, wide AC input voltage range, and low cost.

- Low weight and small size are possible because operation occurs at a frequency beyond the audible range; the inductive elements are small.
- High efficiency because, for output regulation, the power transistor is switched rapidly between saturation and cut-off and therefore has little dissipation. This eases heatsink requirements, which contributes to weight and volume reduction. Conventional linear regulator supplies may have efficiencies as low as 50%, or less, but efficiencies of 80% are readily achievable with SMPS (see Figure 1).
- Wide AC input voltage range because the flexibility of varying the switching frequency in addition to the change in transistor duty cycle makes voltage adaptation unnecessary.
- Low overall cost, due to the reduced volume and power dissipation, means that less material is required and smaller semiconductor devices suffice.

Switched-mode power supplies also have slight disadvantages in comparison to linear regulators, namely, somewhat greater circuit complexity, tendency to RFI radiation, slower response to rapid load changes, and less ability to remove output ripple.

HOW SWITCHED-MODE POWER SUPPLIES OPERATE

The switched-mode power supply is a modern version of its forerunner, the electromechanical vibrator, used in the past to supply car radios. But the new concept is much more reliable because of the far greater lifetime of the transistor switch. Figure 2 shows the principle of the AC fed SMPS. In this system, the AC voltage is rectified, smoothed, and supplied to the electronic chopper, which operates at a frequency above the audible range to prevent noise. The chopped DC voltage is applied to the primary of a transformer, and the secondary voltage is rectified and smoothed to give the required DC output. The transformer is necessary to isolate the output from the input. Output voltage is sensed by a control circuit, which adjusts the duty cycle of the switching transistor, via the drive circuit, to keep the output voltage constant irrespective of load and line voltage changes. Without the input rectifier, this system can be operated from a battery or other DC source.

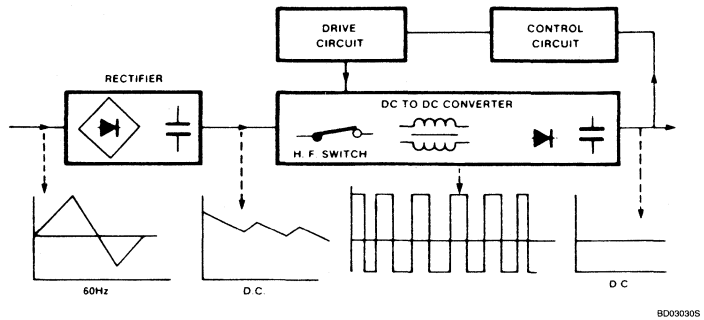


Figure 2. Block Diagram of Switched-Mode Power Supply

Depending on the requirements of the application, the DC-to-DC converter can be one of the three basic types: flyback converter, forward converter, or push-pull (balanced) converter.

The Flyback Converter

Figure 3 shows the flyback converter circuit, and the waveforms of transistor voltage, V_{CE}, and choke current, I_L, reflected to the primary (choke double-wound for line isolation). Cycle time and transistor duty cycle are denoted T and δ, respectively. While Q1 conducts, energy is accumulated in the choke magnetic field (I_L rising and D_1 reverse-biased), and it is discharged into the output capacitor and the load during the flyback period, that is, while Q1 is off (I_L falling and D_1 forward-biased). During Q1 conduction, C_O continues delivering energy to the load, so providing smoothing action. It will be noted that only one inductive element is needed, in distinction to the converter types discussed below, which require two. As the V_{CE} waveform shows, the peak collector voltage is twice the input voltage, V_I, for δ equal to 0.5.

The Forward Converter

A major advantage of the forward converter, particularly for low output voltage applications, is that the high frequency output ripple is limited by the choke in series with the output. Figure 4 illustrates the circuit. During the transistor-on (or forward) period, energy is simultaneously stored in the choke L_O and passed via D_1 to the load. While Q1 is off, part of the energy accumulated in L_O is transferred to the load through free-wheeling diode D_2. Output capacitor C_O smoothes the ripple due to transistor switching. After transistor turn-off, the magnetic energy built up in the transformer core is returned to the DC input via the demagnetizing winding (closely coupled with the primary) and D_3, so limiting the peak collector voltage to twice the input voltage, V_I.

The Push-Pull Converter

This converter type, given in Figure 5, consists of two forward converters operating in push-pull. Diodes D_1 and D_2 rectify the rectangular secondary voltage generated by Q1 and Q2 being turned on during alternate half cycles. Push-pull operation doubles the frequency of the ripple current in output filter L_OC_O and so reduces the output ripple voltage. The peak transistor voltage is $2V_I$.

MAKING THE BEST CONVERTER CHOICE

There exist several versions of the three fundamental circuits described earlier.

These are shown in Figure 6. Circuits IA, IIA and IIIA are the basic types. In the two transistor circuits IB and IIB, transistors Q1 and Q2 conduct simultaneously and diodes D_4 and D_5 limit the peak collector voltage to the level of DC input voltage, V_I. Similarly, in the push-pull circuits IIIB and IIIC, the collector voltage does not exceed V_I; in circuit IIIB, Q1 and Q2 are turned on during alternate half cycles, in circuit IIIC, Q1 and Q4 are turned on in one half cycle and Q2 and Q3 in the next.

Converter choice depends on application and performance requirements. The flyback converter is the simplest and least expensive; it is recommended for multi-output supplies because each output requires only one diode and one capacitor. However, smoothing may

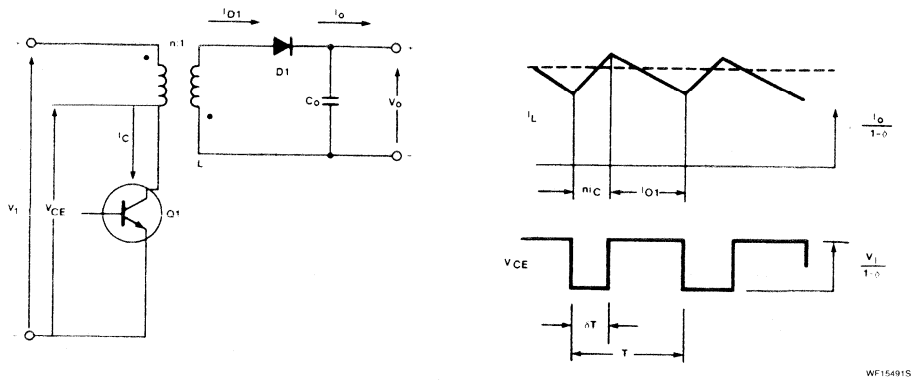


Figure 3. Flyback Converter Circuit Diagram and Waveforms

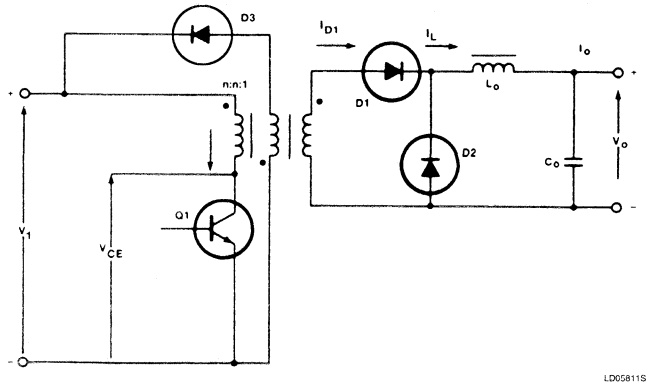


Figure 4. Forward Converter Circuit Diagram

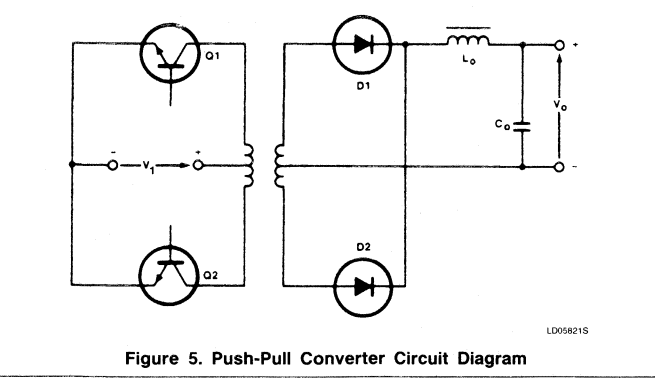


Figure 5. Push-Pull Converter Circuit Diagram

be a problem where ripple requirements are severe. The push-pull type has the most complex base drive circuit but it produces the lowest output ripple with given values of L_O and C_O.

Figure 7 is a general guide for the choice of converter type, based on output voltage and power. In the case of the flyback converter, it becomes more and more difficult to keep the percentage output ripple below an acceptable level as the output power increases and the output voltage decreases. For reasons of circuit economy, however, the flyback converter is the best proposition if the output power does not exceed about 10W. For output powers higher than about 1kW, the push-pull converter is preferable.

THE CONTROL AND PROTECTION MODULE

In addition to providing adequate output voltage stabilization against line voltage and load changes, the control module must give fast protection against overload, equipment malfunction, and the effects of switch-on immediately following switch-off. In addition the following features are desirable:

- Soft-Start: a gradual increase of the transistor duty cycle after switch-on causing a slow rise of the output voltage, which prevents an excessive inrush current due to a capacitive load or charging of the output capacitor.
- Synchronization: to prevent interference due to the difference in free-running frequencies (for example, in a system in which a low-power SMPS supplies the base drive circuit of the output switching transistor in a high-power SMPS).

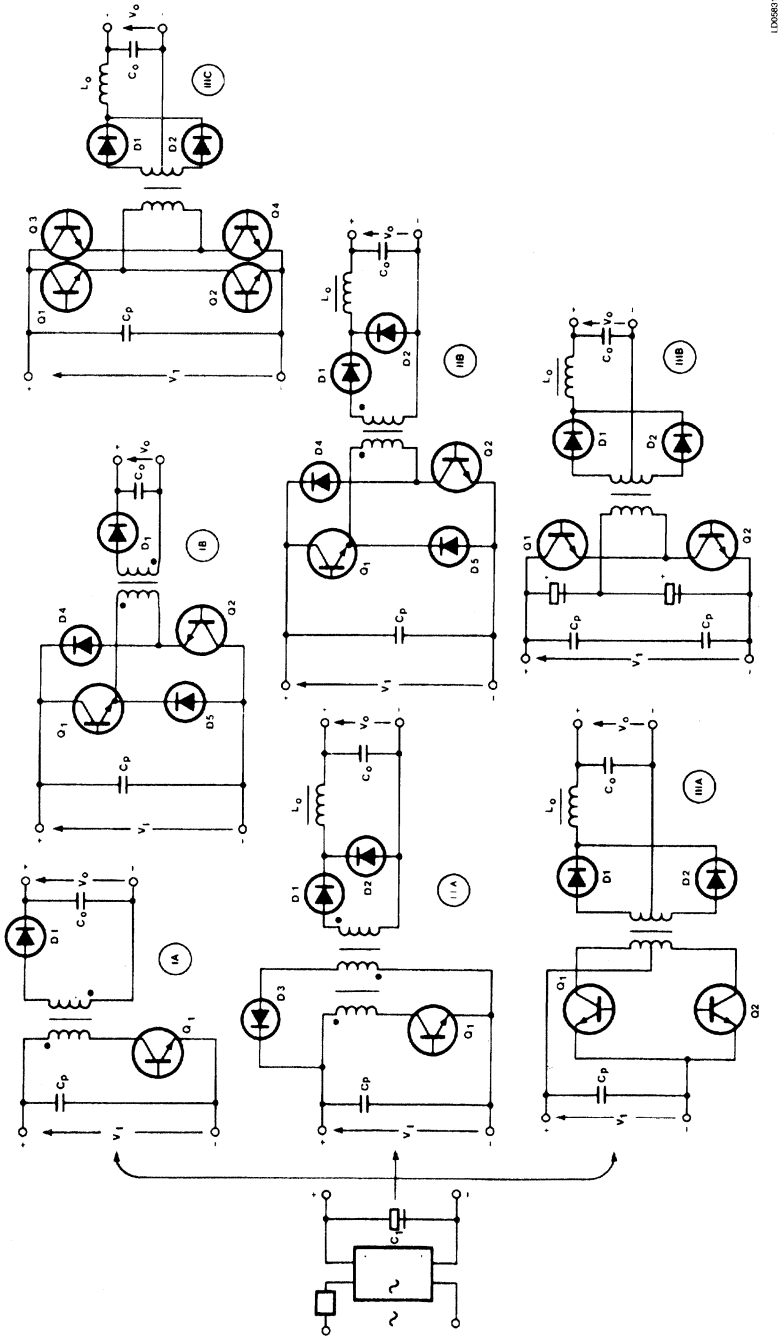
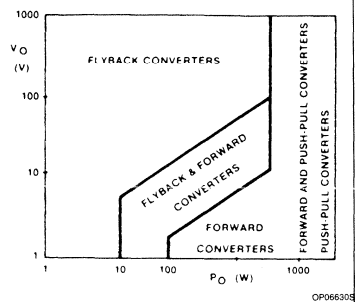


Figure 6. Various DC-to-DC Converter Types with Their Rectifier Supply

NOTES:
Flyback converter family with 1A single-transistor type and 1B two-transistor type.
Forward converter family with 2A single-transistor type and 2B two-transistor type.
Push-pull converter family with 3A conventional type, 3B single-ended type, and 3C bridge type.
Capacitor C_P is a high-frequency bypass (20Hz switching frequency).



NOTE:
Converter choice as a function of SMPS output voltage, V_O and output power, P_O.

Figure 7. Converter Type

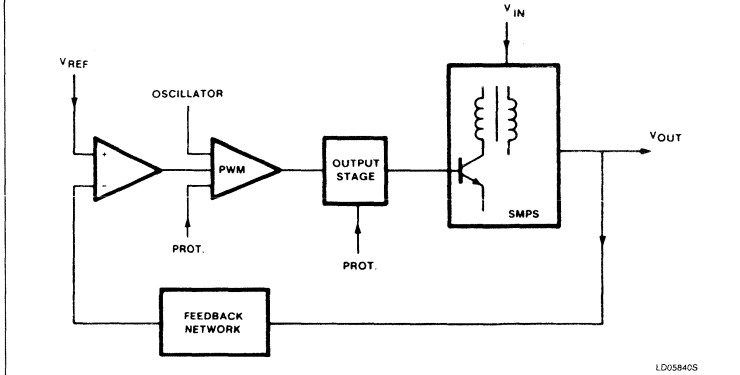


Figure 8. SMPS Control Loop

- Remote switch-on and switch-off: essential for sequential switching of supply units in, for instance, a computer supply system.

The control and protection circuitry of a switched-mode power supply (SMPS) is a crucial and complicated part of the whole supply. Integration of this circuitry on a chip will therefore ease the design of an SMPS considerably.

SMPS CONTROL LOOP

Figure 8 shows the principal control loop of a regulated SMPS. The output voltage V_O is sensed and, via a feedback network, fed to the input of an error amplifier where it is compared with a reference voltage.

The output of this amplifier is connected to an input of the pulse-width modulator, PWM.

The other input of this modulator is used for an oscillator signal, which can be a sawtooth or a triangle.

As a result, a rectangular waveform with the frequency of the oscillator is emerging at the output of the PWM.

The width of this pulse is dictated by the output voltage of the error amplifier.

After passing through an output stage, the pulse can be used to drive the power transistor of the SMPS.

When the width of the pulse is varied, the on-time of this transistor will also vary and consequently the amount of energy taken from the input voltage, V_I.

So, by controlling the duty cycle δ of the power transistor, one can stabilize the output of the SMPS against line and load variations. The duty cycle δ is defined as t_{ON}/T for the power transistor. Protections for overvoltage, overcurrent, etc., can be realized with additional inputs on the PWM or the output stage.

INITIAL TURN-ON

It may be helpful to operate an SMPS open loop with reduced error amplifier gain. This provides an easy way to verify correct operation of control loop elements.

NE/SE5560
Switched-Mode Power Supply Control Circuit

Product Specification

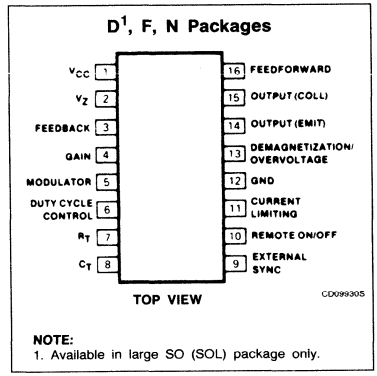
DESCRIPTION

The NE/SE5560 is a control circuit for use in switched-mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched-mode power supplies, including an internal temperature-compensated reference source, internal Zener references, sawtooth generator, pulse-width modulator, output stage and various protection circuits.

FEATURES

- **Stabilized power supply**
- **Temperature-compensated reference source**
- **Sawtooth generator**
- **Pulse-width modulator**
- **Remote on/off switching**
- **Current limiting**
- **Low supply voltage protection**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Maximum duty cycle clamp**
- **Feed-forward control**
- **External synchronization**

PIN CONFIGURATION



NOTE:
1. Available in large SO (SOL) package only.

ORDERING INFORMATION

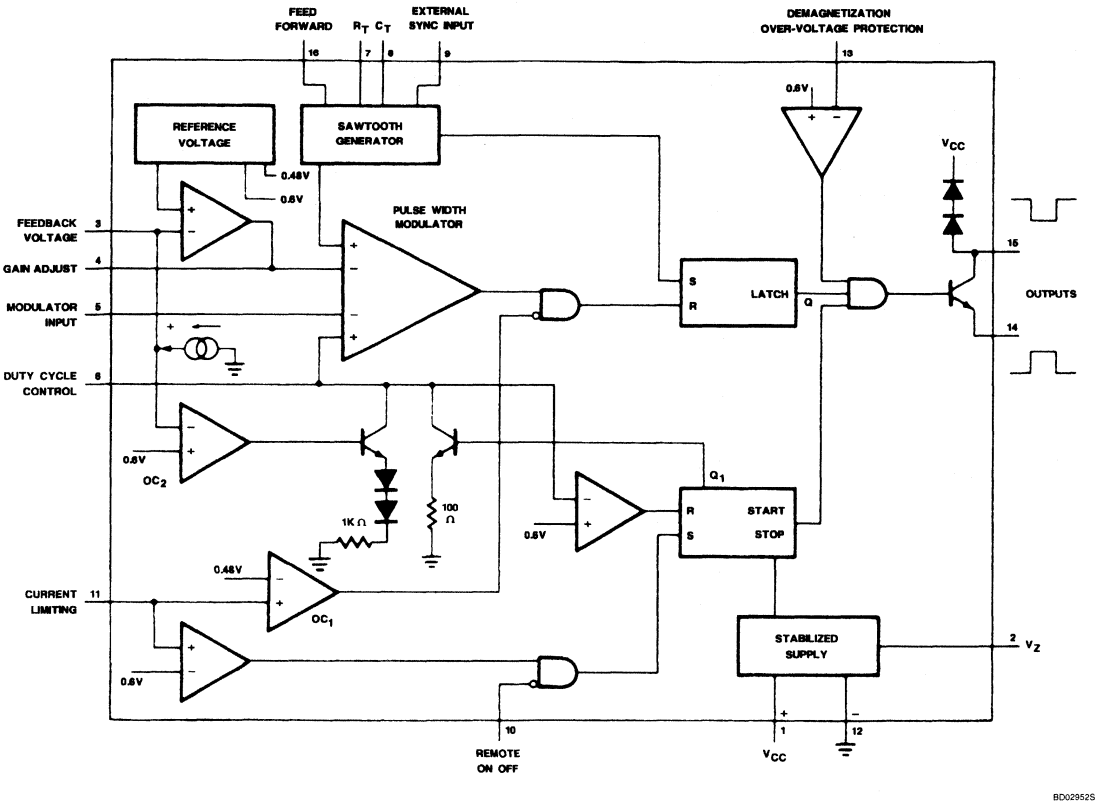
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to 70°C	NE5560N
16-Pin Plastic Dip	−55°C to 125°C	SE5560N
16-Pin Cerdip	0 to 70°C	NE5560F
16-Pin Cerdip	−55°C to 125°C	SE5560F
16-Pin SOL	0 to 70°C	NE5560D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC} I_{CC}	Supply[1] Voltage-forced mode Current-fed mode	 +18 30	 V mA
I_{OUT}	Output transistor (at 20 − 30V max) Output current Collector voltage (Pin 15) Max. emitter voltage (Pin 14)	 40 V_{CC} + 1.4V +5	 mA V V
T_A	Operating ambient temperature range SE5560 NE5560	 −55 to +125 0 to 70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:
1. Does not include current for timing resistors or capacitors.

BLOCK DIAGRAM



NOTE:
1. See Voltage/Current fed supply characteristic curve.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
			Min	Typ	Max	Min	Typ	Max	
Reference sections									
V_{REF}	Internal reference voltage	25°C Over temperature	3.69 3.65	3.72	3.81 3.85	3.57 3.53	3.72	3.95 4.00	V V
	Temperature coefficient of V_{REF}			−100			−100		ppm/°C
V_Z	Internal Zener reference Temperature coefficient of V_Z	$I_L = -7mA$	7.8	8.4 200	8.8	7.8	8.4 200	8.8	V ppm/°C
Oscillator section									
	Frequency range	Over temperature	50		100k	50		100k	Hz
	Initial accuracy oscillator	R = 5kΩ		5			5		%
	Duty cycle range	$f_O = 20kHz$	0		98	0		98	%
Modulator									
	Modulation input current	Voltage at Pin 5 = 2V Over temperature		0.2	20		0.2	20	μA
Housekeeping function									
I_{IN}	Pin 6, input current	At 2V Over temperature		0.2	20		0.2	20	μA
	Pin 6, duty cycle limit control	For 50% max duty cycle 15kHz to 50kHz/41% of V_Z	40	50	60	40	50	60	% of duty cycle
	Pin 1, low supply voltage protection thresholds		8	9.0	10.5	8	9.0	10.5	V
	Pin 3, feedback loop protection trip threshold		400	600	720	400	600	720	mV
I_{IN}	Pin 3, pull-up current	At 2V	−7	−15	−35	−7	−15	−35	μA
	Pin 13, demagnetization/over-voltage protection trip on threshold	Over temperature	470	600	720	470	600	720	mV
	Pin 13, input current	At 0.25V 25°C Over temperature		−0.6	−10 −20		−0.6	−10 −20	μA
	Pin 16, feed-forward duty cycle control	Voltage at Pin 16 = $2V_Z$	30	40	50	30	40	50	% original duty cycle
	*Pin 16, feed-forward input current	At 16V, $V_{CC} = 18V$ 25°C		0.2	5		0.2	5	μA
		Over temperature			10			10	μA

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$, $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
			Min	Typ	Max	Min	Typ	Max	
External synchronization									
	Pin 9 Off		0		0.8	0		0.8	V
	On		2		V_Z	2		V_Z	V
	Sink current	Voltage at Pin 9 = 0V, 25°C		−65	−100		−65	−125	μA
		Over temperature			−125			−125	μA
Remote									
	Pin 10 Off		0		0.8	0		0.8	V
	On		2		V_Z	2		V_Z	V
	Sink current	At 0V 25°C		−85	−100		−85	−125	μA
		Over temperature			−125			−125	μA
Current limiting									
I_{IN}	Pin 11 Input current	Voltage at Pin 11 = 250mV 25°C		−2	−20		−2	−20	μA
		Over temperature			−40			−40	μA
	Single pulse inhibit delay	Inhibit delay time for 20% overdrive at 40mA I_{OUT}		0.7	0.8		0.7	0.8	μs
OC_1	Trip Levels: Shut down, slow start, low level		0.500	0.600	0.700	0.500	0.600	0.700	V
OC_2	Current limit, high level		0.400	0.480	0.560	0.400	0.560	0.500	V
ΔOC	Low Level in terms of high level, OC_1		0.750	0.800	0.850	0.750	0.800	0.850	V
Error amplifier									
V_{OH}	Output voltage swing		6.2		9.5	6.2		9.5	V
V_{OL}	Output voltage swing				0.7			0.7	V
	Open-loop gain		54	60		54	60		dB
R_F	Feedback resistor		10k			10k			Ω
BW	Small-signal bandwidth			3			3		MHz
Output stage									
	V_{CE}(SAT) I_C = 40mA				0.5			0.5	V
	Output current (Pin 15)		40			40			mA
	Max. emitter voltage (Pin 14)		5	6		5	6		V
Supply voltage/current[1]									
I_{CC}	Supply current	I_Z = 0, voltage-forced, V_{CC} = 12V, 25°C			10			10	mA
		Over temp.			15			15	mA
V_{CC}	Supply voltage	I_{CC} = 10mA current-fed	20		23	19		24	V
V_{CC}	Supply voltage	I_{CC} = 30mA current-fed	20		30	20		30	V

NOTE:
1. Does not include current for timing resistors or capacitors.

MAXIMUM PIN VOLTAGES

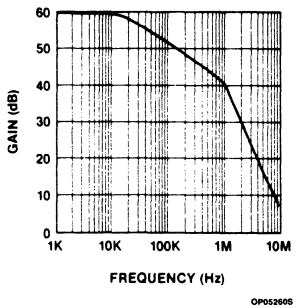
NE5560		
Pin No	**Function**	**Maximum Voltage**
1	V_{CC}	See Note 1
2	V_Z	Do not force (8.4V)
3	Feedback	V_Z
4	Gain	
5	Modulator	V_Z
6	Duty Cycle Control	V_Z
7	R_T	Current force mode
8	C_T	
9	External Sync	V_Z
10	Remote On/Off	V_Z
11	Current Limiting	V_{CC}
12	GND	GND
13	Demagnetization/Overvoltage	V_{CC}
14	Output (Emit)	V_Z
15	Output (Collector)	$V_{CC} + 2V_{BE}$
16	Feed-forward	V_{CC}

NOTE:

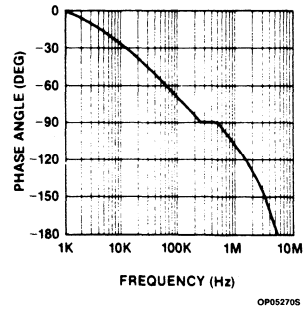
1. When voltage-forced, maximum is 18V; when current-fed, maximum is 30mA. See voltage-/current-fed supply characteristic curve.

TYPICAL PERFORMANCE CHARACTERISTICS

Error Amplifier Open-Loop Gain

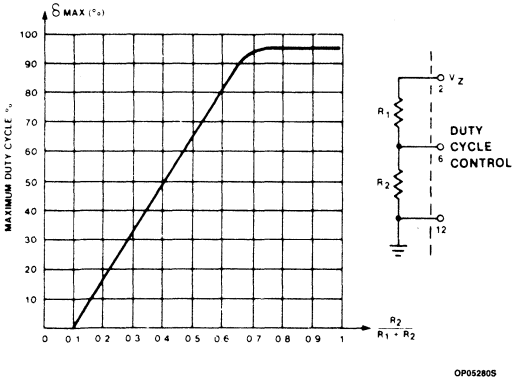


Error Amplifier Open-Loop Phase



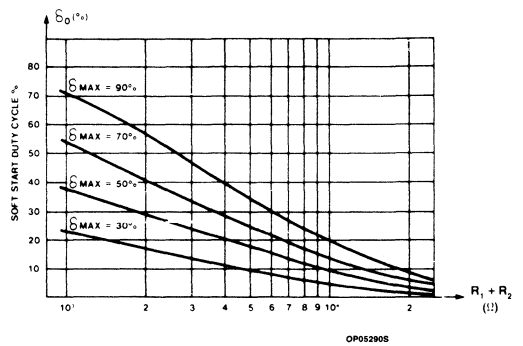
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Graph for Determining δ_{MAX}



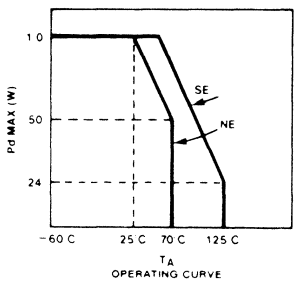
OP05280S

Soft-Start Min. Duty Cycle vs $R_1 + R_2$



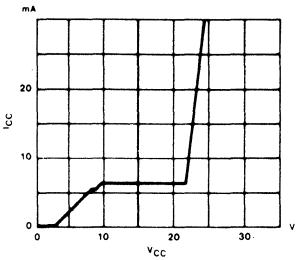
OP05290S

Power Derating Curve



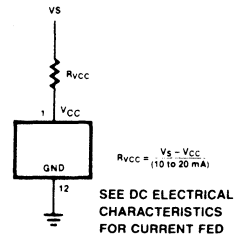
OP05300S

NE5560 Voltage-/Current-Fed Supply Characteristics



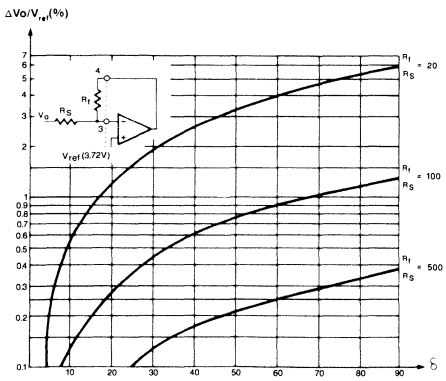
OP05310S

Current-Fed Dropping Resistor



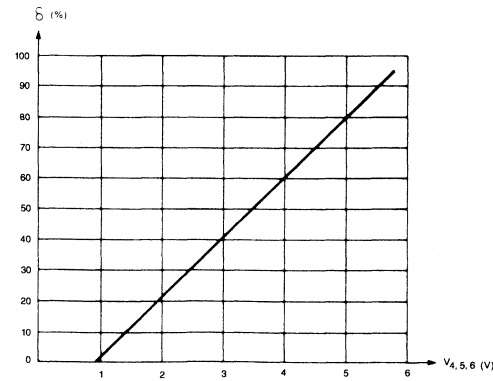
TC08780S

Regulation vs Error Amp Closed-Loop Gain



OP05320S

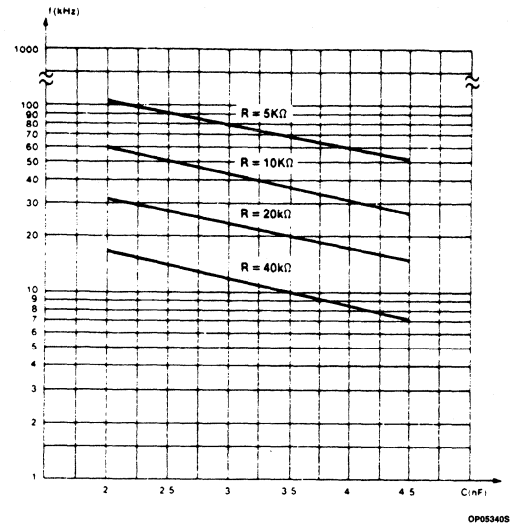
Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage



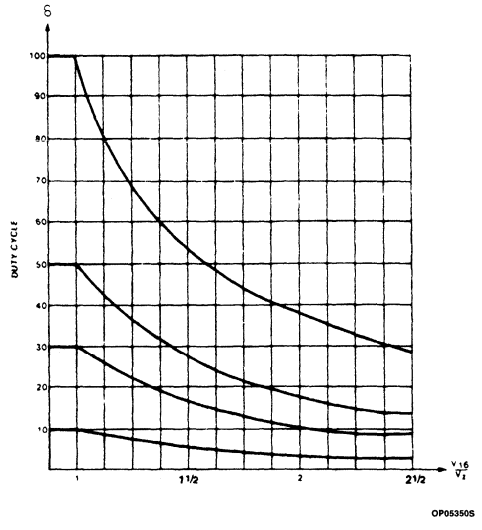
OP05330S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Typical Frequency Plot vs R_T and C_T



Duty Cycle Sensitivity to Feed-Forward Voltage (Pin 16)



THEORY OF OPERATION

The following functions are incorporated:

- A temperature-compensated reference source.
- An error amplifier with Pin 3 as input. The output is connected to Pin 4 so that the gain is adjustable with external resistors.
- A sawtooth generator with a TTL-compatible synchronization input (Pins 7, 8, 9).
- A pulse-width modulator with a duty cycle range from 0 to 95%.

The PWM has two additional inputs:

Pin 6 can be used for a precise setting of δ_{MAX}

Pin 5 gives a direct access to the modulator, allowing for real constant-current operation:

- A gate at the output of the PWM provides a simple dynamic current limit.
- A latch that is set by the flyback of the sawtooth and reset by the output pulse of the above mentioned gate prohibits double pulsing.
- Another latch functions as a start-stop circuit; it provides a fast switch-off and a slow start.
- A current protection circuit that operates via the start-stop circuit. This is a combined function with the current limit circuit, therefore Pin 11 has two trip-on levels; the lower one for cycle-by-cycle current limiting, the upper one for current protection by means of switch-off and slow-start.
- A TTL-compatible remote on/off input at Pin 10, also operating via the start-stop circuit.
- An inhibit input at Pin 13. The output pulse can be inhibited immediately.
- An output gate that is commanded by the latches and the inhibit circuit.
- An output transistor of which both the collector (Pin 15) and the emitter (Pin 14) are externally available. This allows for normal or inverse output pulses.
- A power supply that can be either voltage- or current-driven (Pins 1 and 12). The internally-generated stabilized output voltage V_Z is connected to Pin 2.
- A special function is the so-called feed-forward at Pin 16. The amplitude of the sawtooth generator is modulated in such a way that the duty cycle becomes inversely proportional to the voltage on this pin: $\delta \sim 1/V16$.
- Loop fault protection circuits assure that the duty cycle is reduced to zero or a low value for open- or short-circuited feedback loops.

Stabilized Power Supply (Pins 1, 2, 12)

The power supply of the NE5560 is of the well known series regulation type and provides a stabilized output voltage of typically 8.5V.

This voltage V_Z is also present at Pin 2 and can be used for precise setting of δ_{MAX} and to supply external circuitry. Its max. current capability is 5mA.

The circuit can be fed directly from a DC voltage source between 10.5V and 18V or can be current-driven via a limiting resistor. In the latter case, internal pinch-off resistors will limit the maximum supply voltage: typical 23V for 10mA and max. 30V for 30mA.

The low supply voltage protection is active when $V_{(1-12)}$ is below 10.5V and inhibits the output pulse (no hysteresis).

When the supply voltage surpasses the 10.5V level, the IC starts delivering output pulses via the slow-start function.

The current consumption at 12V is less than 10mA, provided that no current is drawn from V_Z and $R_{(7-12)} \geqslant 20k\Omega$.

The Sawtooth Generator

Figure 2 shows the principal circuitry of the oscillator. A resistor between Pin 7 and Pin 12 (GND) determines the constant current that charges the timing capacitor $C_{(8-12)}$.

This causes a linear increasing voltage on Pin 8 until the upper level of 5.6V is reached. Comparator H sets the RS flip-flop and Q1 discharges $C_{(8-12)}$ down to 1.1V, where comparator L resets the flip-flop. During this flyback time, Q2 inhibits the output.

Synchronization at a frequency lower than the free-running frequency is accomplished via the TTL gate on Pin 9. By activating this gate ($V^9 < 2V$), the setting of the sawtooth is prevented. This is indicated in Figure 3.

Figure 4 shows a typical plot of the oscillator frequency against the timing capacitor. The frequency range of the NE5560 goes from < 50Hz up to > 100kHz.

Reference Voltage Source

The internal reference voltage source is based on the bandgap voltage of silicon. Good design practice assures a temperature dependency typically ± 100ppm/°C. The reference voltage is connected to the positive input of the error amplifier and has a typical value of 3.72V.

Error Amplifier Compensation

For closed-loop gains less than 40dB, it is necessary to add a simple compensation capacitor as shown in Figures 4 and 5.

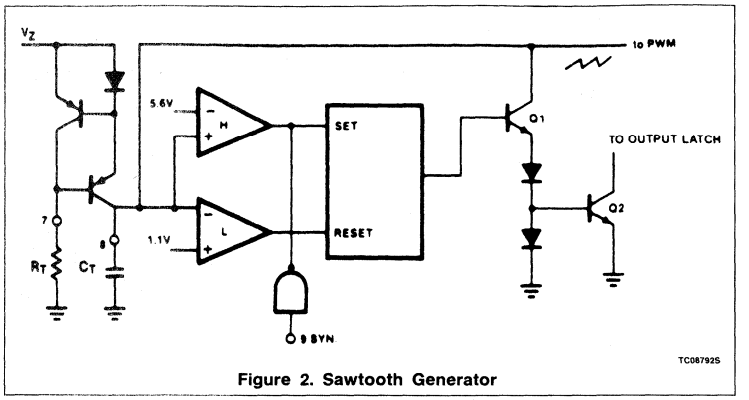


Figure 2. Sawtooth Generator

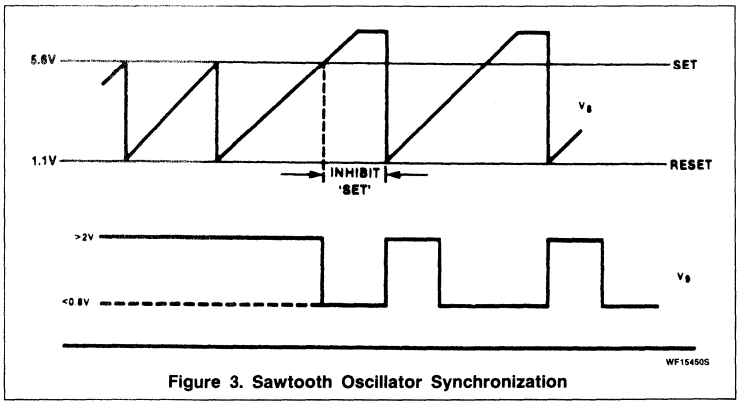


Figure 3. Sawtooth Oscillator Synchronization

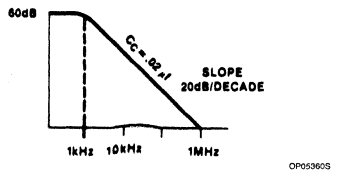


Figure 4. Error Amplifier Compensation Open-Loop Gain

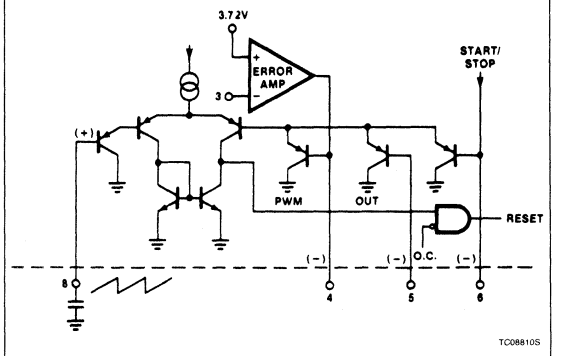


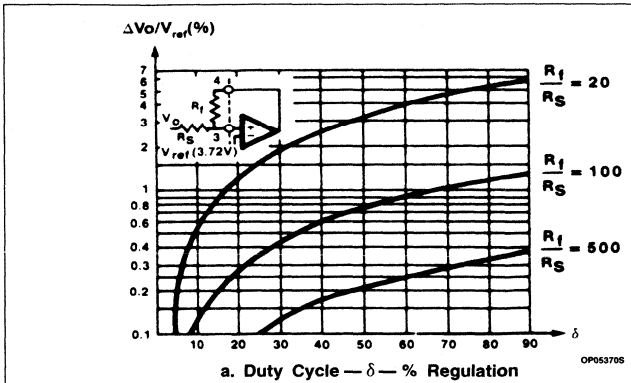
Figure 5. Error Amplifier

Error Amplifier with Loop-Fault Protection Circuits

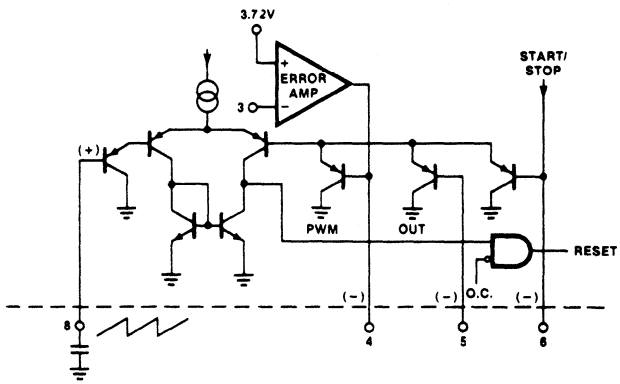
This operational amplifier is of a generally used concept and has an open-loop gain of typically 60dB. As can be seen in Figure 5, the inverting input is connected to Pin 3 for a feedback information proportional to V_O.

The output goes to the PWM circuit, but is also connected to Pin 4, so that the required gain can be set with R_S and $R_{(3-4)}$. This is indicated in Figure 5, showing the relative change of the feedback voltage as a function of the duty cycle. Additionally, Pin 4 can be used for phase shift networks that improve the loop stability.

When the SMPS feedback loop is interrupted, the error amplifier would settle in the middle of its active region because of the feedback via $R_{(3-4)}$. This would result in a large duty cycle. A current source on Pin 3 prevents this by pushing the input voltage high via the voltage drop over $R_{(3-4)}$. As a result, the duty cycle will become zero, provided that $R_{(3-4)} > 100k$. When the feedback loop is short-circuited, the duty cycle would jump to the adjusted maximum duty cycle. Therefore, an additional comparator is active for feedback voltages at Pin 3 below 0.6V. Now an internal resistor of typically 1k is shunted to the impedance on the δ_{MAX} setting Pin 6. Depending on this impedance, δ will be reduced to a value δ_0. This will be discussed further.



a. Duty Cycle — δ — % Regulation



b. Pulse-Width Modulation

Figure 6

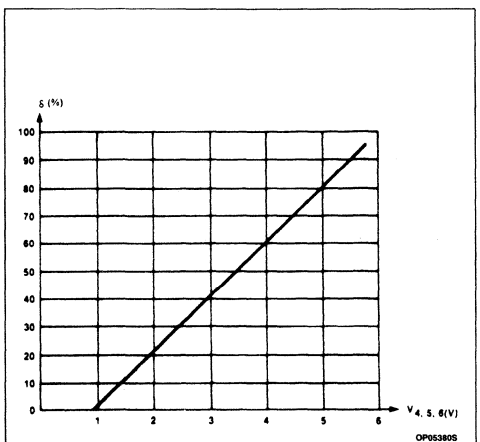


Figure 7. Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage

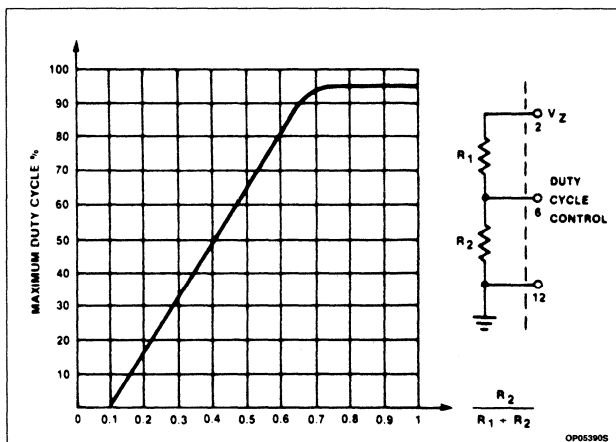


Figure 8. Graph for Determining δ_{MAX}

The Pulse-Width Modulator

The function of the PWM circuit is to translate a feedback voltage into a periodical pulse of which the duty cycle depends on that feedback voltage. As can be seen in Fig ıre 6, the PWM circuit in the NE5560 is a long-tailed pair in which the sawtooth on Pin 8 is compared with the LOWEST voltage on either Pin 4 (error amplifier), Pin 5, or Pin 6 (δ_{MAX} and slow-start). The transfer graph is given in Figure 7. The output of the PWM causes the resetting of the output bistable.

Limitation of the Maximum Duty Cycle

With Pins 5 and 6 not connected and with a rather low feedback voltage on Pin 3, the NE5560 will deliver output pulses with a duty cycle of ≈ 95%. In many SMPS applications, however, this high δ will cause problems. Especially in forward converters, where the transformer will saturate when δ exceeds 50%, a limitation of the maximum duty cycle is a must.

A DC voltage applied to Pin 6 (PWM input) will set δ_{MAX} at a value in accordance with Figure 7. For low tolerances of δ_{MAX}, this voltage on Pin 6 should be set with a resistor divider from V_Z (Pin 2). The upper and lower sawtooth levels are also set by means of an internal resistor divider from V_Z, so forming a bridge configuration with the δ_{MAX} setting is low because tolerances in V_Z are compensated and the sawtooth levels are determined by internal resistor matching rather than by absolute resistor tolerance. Figure 8 can be used for determining the tap on the bleeder for a certain δ_{MAX} setting.

As already mentioned, Figure 9 gives a graphical representation of this. The value δo is limited to the lower and the higher side;

- It must be large enough to ensure that at maximum load and minimum input voltage the resulting feedback voltage on Pin 3 exceeds 0.6V.
- It must be small enough to limit the amount of energy in the SMPS when a loop fault occurs. In practice, a value of 10 – 15% will be a good compromise.

Extra PWM Input (Pin 5)

The PWM has an additional inverting input: Pin 5. It allows for attacking the duty cycle via the PWM circuit, independently from the feedback and the δ_{MAX} information. This is necessary when the SMPS must have a real constant-current behavior, possibly with a fold-back characteristic. However, the realization of this feature must be done with additional external components. When not used, Pin 5 should be tied to Pin 6.

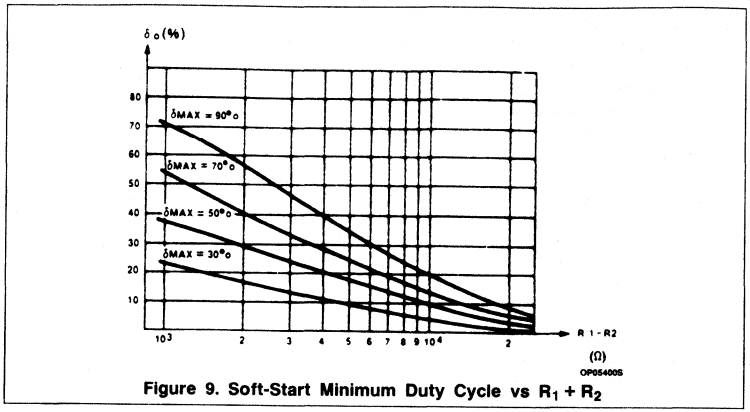


Figure 9. Soft-Start Minimum Duty Cycle vs $R_1 + R_2$

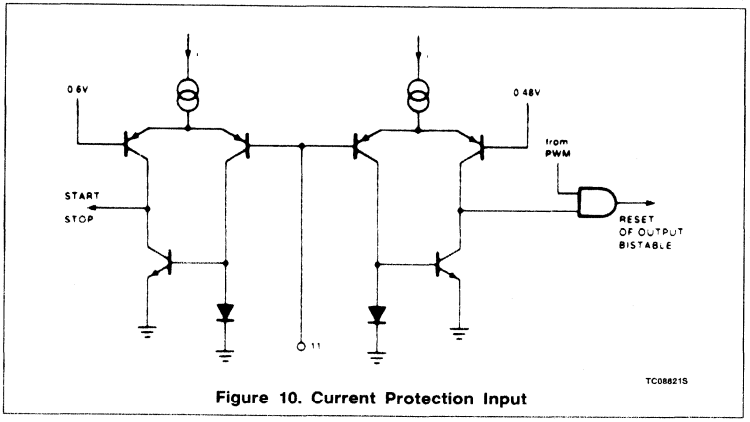


Figure 10. Current Protection Input

Dynamic Current Limit and Current Protection (Pin 11)

In many applications, it is not necessary to have a real constant-current output of the SMPS.

Protection of the power transistor will be the prime goal. This can be realized with the NE5560 in an economical way. A resistor (or a current transformer) in the emitter of the power transistor gives a replica of the collector current. This signal must be connected to Pin 11. As can be seen in Figure 10, this input has two comparators with different reference levels. The output of the comparator with the lower 0.48V reference is connected to the same gate as the output of the PWM.

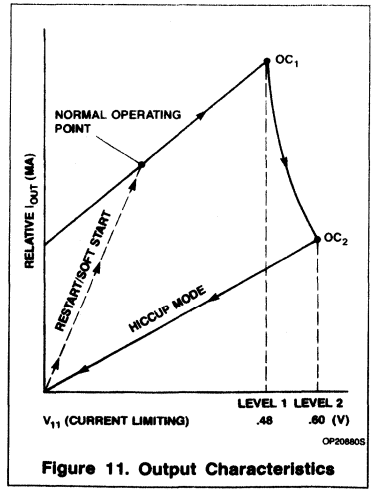


Figure 11. Output Characteristics

When activated, it will immediately reset the output flip-flop, so reducing the duty cycle. The effectiveness of this cycle-by-cycle current limit diminishes at low duty cycle values. When δ becomes very small, the storage time of the power transistor becomes dominant. The current will now increase again, until it surpasses the reference of the second comparator. The output of this comparator activates the start-stop circuit and causes an immediate inhibit of the output pulses. After a certain deadtime, the circuit starts again with very narrow output pulses. The effect of this two-level current protection circuit is visualized in Figure 11.

The Start-Stop Circuit

The function of this protection circuit is to stop the output pulses as soon as a fault occurs and to keep the output stopped for several periods. After this dead-time, the output starts with a very small, gradually increasing duty cycle. When the fault is persistent, this will cause a cyclic switch-off/switch-on condition. This "hiccup" mode effectively limits the energy during fault conditions. The realization and the working of the circuit are indicated in Figures 12 and 13. The dead time and the soft-start are determined by an external capacitor that is connected to Pin 6 (δ_{MAX} setting).

An RS flip-flop can be set by three different functions:

1. Remote on/off on Pin 10.
2. Overcurrent protection on Pin 11.
3. Low supply voltage protection (internal).

As soon as one of these functions cause a setting of the flip-flop, the output pulses are blocked via the output gate. In the same time transistor Q1 is forward-biased, resulting in a discharge of the capacitor on Pin 6.

The discharging current is limited by an internal 150Ω resistor in the emitter of Q1. The voltage at Pin 6 decreases to below the lower level of the sawtooth. When V6 has dropped to 0.6V, this will activate a comparator and the flip-flop is reset. The output stage is no longer blocked and Q1 is cut off. Now V_Z will charge the capacitor via R1 to the normal δ_{MAX} voltage. The output starts delivering very narrow pulses as soon as V6 exceeds the lower sawtooth level. The duty cycle of the output pulse now gradually increases to a value determined by the feedback on Pin 3, or by the static δ_{MAX} setting on Pin 6.

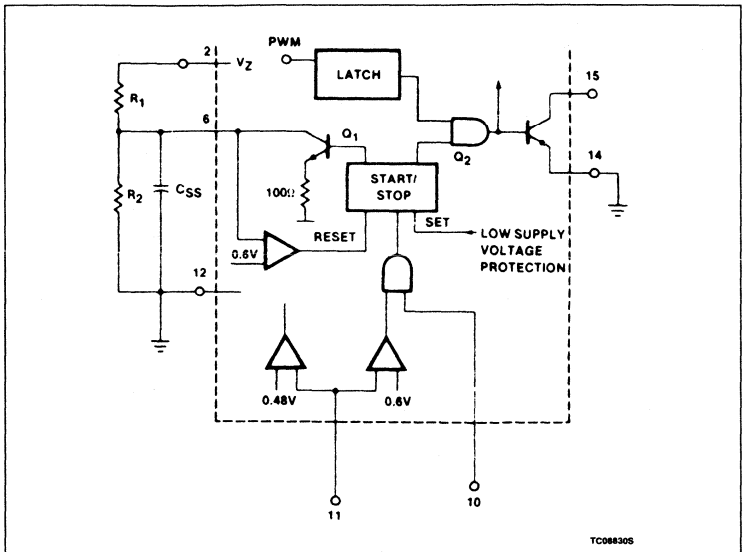


Figure 12. Start-Stop Circuit

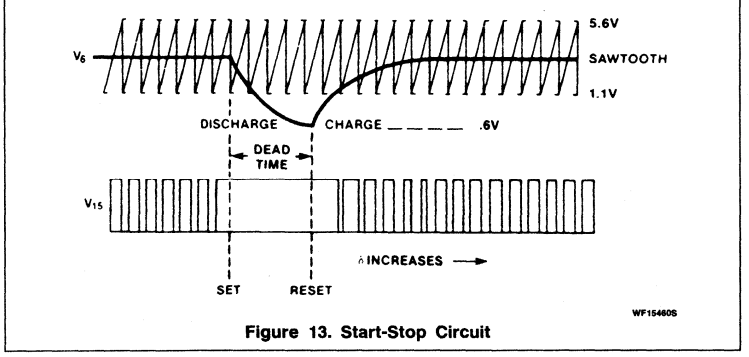


Figure 13. Start-Stop Circuit

Remote On/Off Circuit (Pin 10)

In systems where two or more power supplies are used, it is often necessary to switch these supplies on and off in a sequential way. Furthermore, there are many applii ations in which a supply must be switched by a logical signal. This can be done via the TTL-compatible remote on/off input on Pin 10. The output pulse is inhibited for levels below 0.8V. The output of the IC is no longer blocked when the remote on/off input is left floating or when a voltage > 2V is applied. Start-up occurs via the slow-start circuit.

The Output Stage

The output stage of the NE5560 contains a flip-flop, a push-pull driven output transistor, and a gate, as indicated in Figure 14. The flip-flop is set by the flyback of the sawtooth. Resetting occurs by a signal either from the PWM or the current limit circuit. With this configuration, it is assured that the output is switched only once per period, thus prohibiting double pulsing. The collector and emitter of the output transistor are connected to respectively Pin 15 and Pin 14, allowing for normal or inverted output pulses. An internally-grounded emitter would cause untolerable voltage spikes over the bonding wire, especially at high output currents.

This current capability of the output transistor is 40mA peak for $V_{CE} \cong 0.4V$. An internal clamping diode to the supply voltage protects the collector against overvoltages. The max. voltage at the emitter (Pin 14) must not exceed +5V. A gate, activated by one of the set or reset pulses, or by a command from the start-stop circuit will immediately switch-off the output transistor by short-circuiting its base. The external inhibitor (Pin 13) operates also via this base.

Demagnetization Sense

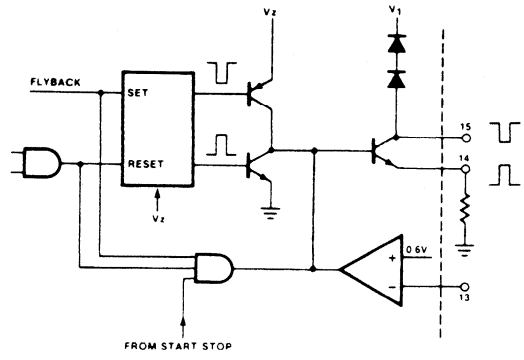
As indicated in Figure 14, the output of this NPN comparator will block the output pulse, when a voltage above 0.6V is applied to Pin 13. A specific application for this function is to prevent saturation of forward-converter transformers. This is indicated in Figure 15.

Feed-Forward (Pin 16)

The basic formula for a forward converter is

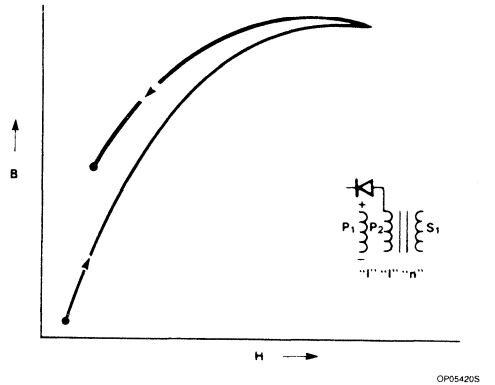
$$V_{OUT} = \frac{dV_{IN}}{n}$$ (n = transformer ratio)

This means that in order to keep V_{OUT} at a constant value, the duty cycle δ must be made inversely proportional to the input voltage. A preregulation (feed-forward) with the function $\delta \sim 1/V_{IN}$ can ease the feedback-loop design.



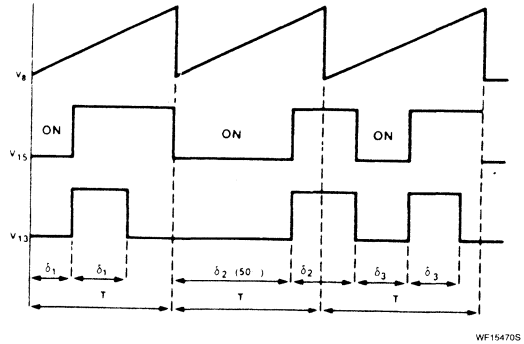
TC08841S

NOTE:
The signal V_{13} can be derived from the demagnetizing winding in a forward converter as shown below.



OP05420S

Figure 14. Output Stage



WF15470S

Figure 15. Output Stage Inhibit

This loop now only has to regulate for laod variations which require only a low feedback gain in the normal operation area. The transformer of a forward converter must be designed in such a way that it does not saturate, even under transient conditions, where the max. inductance is determined by $\delta_{MAX} \times V_{IN}$ max. A regulation of $\delta_{MAX} \sim 1/V_{IN}$ will allow for a considerable reduction or simplification of the transformer. The function of $\delta \sim 1/V_{IN}$ can be realized by using Pin 16 of the NE5560.

Figure 16 shows the electrical realization. When the voltage at Pin 16 exceeds the stabilized voltage V_Z (Pin 2), it will increase the charging current for the timing capacitor on Pin 8.

The operating frequency is not affected, because the upper trip level for sawtooth increases also. Note that the δ_{MAX} voltage on Pin 6 remains constant because it is set via V_Z. Figure 17 visualizes the effect on δ_{MAX} and the normal operating duty cycle δ. For $V_{16} = 2 \times V_Z$, these duty cycles have halved. The graph for $\delta = f(V_{16})$ is given in Figure 18.

NOTE:
V_{16} must be less than Pin 1 voltage.

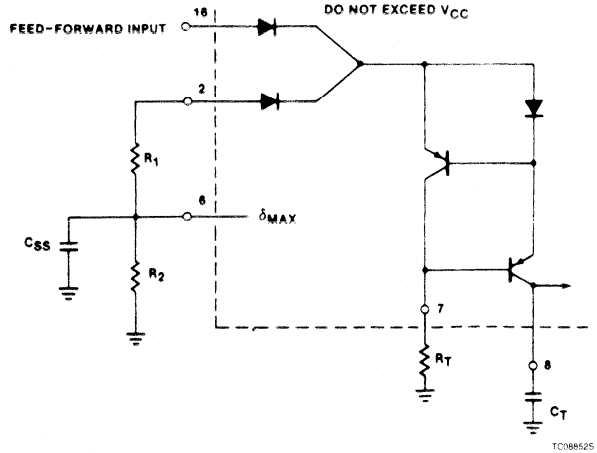


Figure 16. External δ Maximum Control

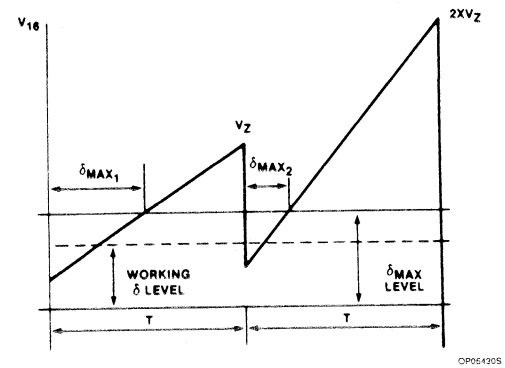


Figure 17. Feed-Forward Circuitry

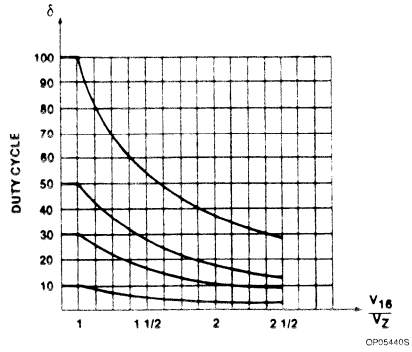


Figure 18. Feed-Forward Regulation

APPLICATIONS

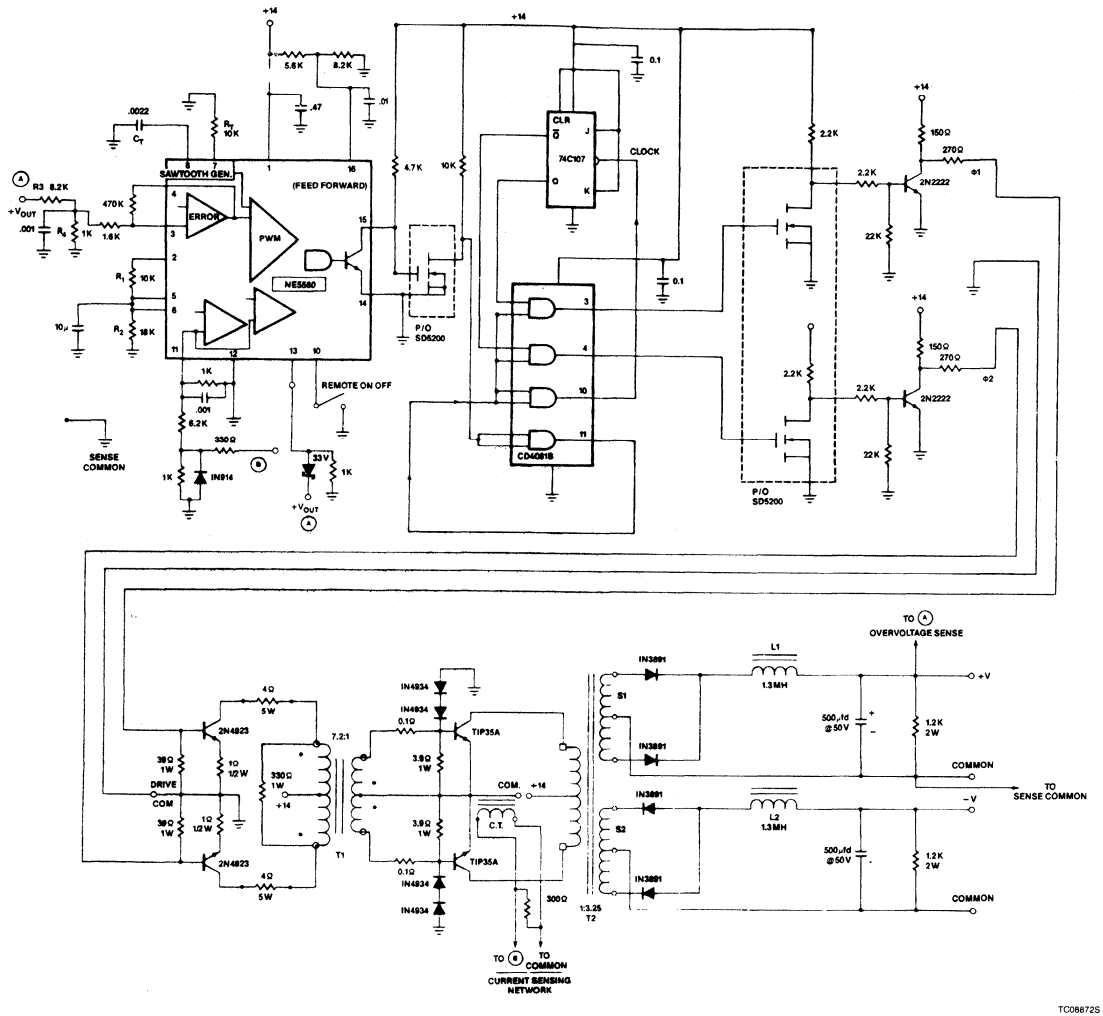
NE/SE5560 Push-Pull Regulator

This application describes the use of the Signetics NE/SE5560 adapted to function as a push-pull switched mode regulator, as shown in Figures 19 and 20.

Input voltage range is +12V to +18V for a nominal output of +30V and −30V at a maximum load current of 1A with an average efficiency of 81%.

Features include feed-forward input compensation, cycle-to-cycle drive current protection and other voltage sensing, line (to positive output) regulation < 1% for an input range of +13V to +18V and load regulation to positive output of < 3% for $\Delta I_L(+)$ of 0.1 to 1A.

The main pulse-width modulator operates to 48kHz with power switching at 24kHz.



NOTES:

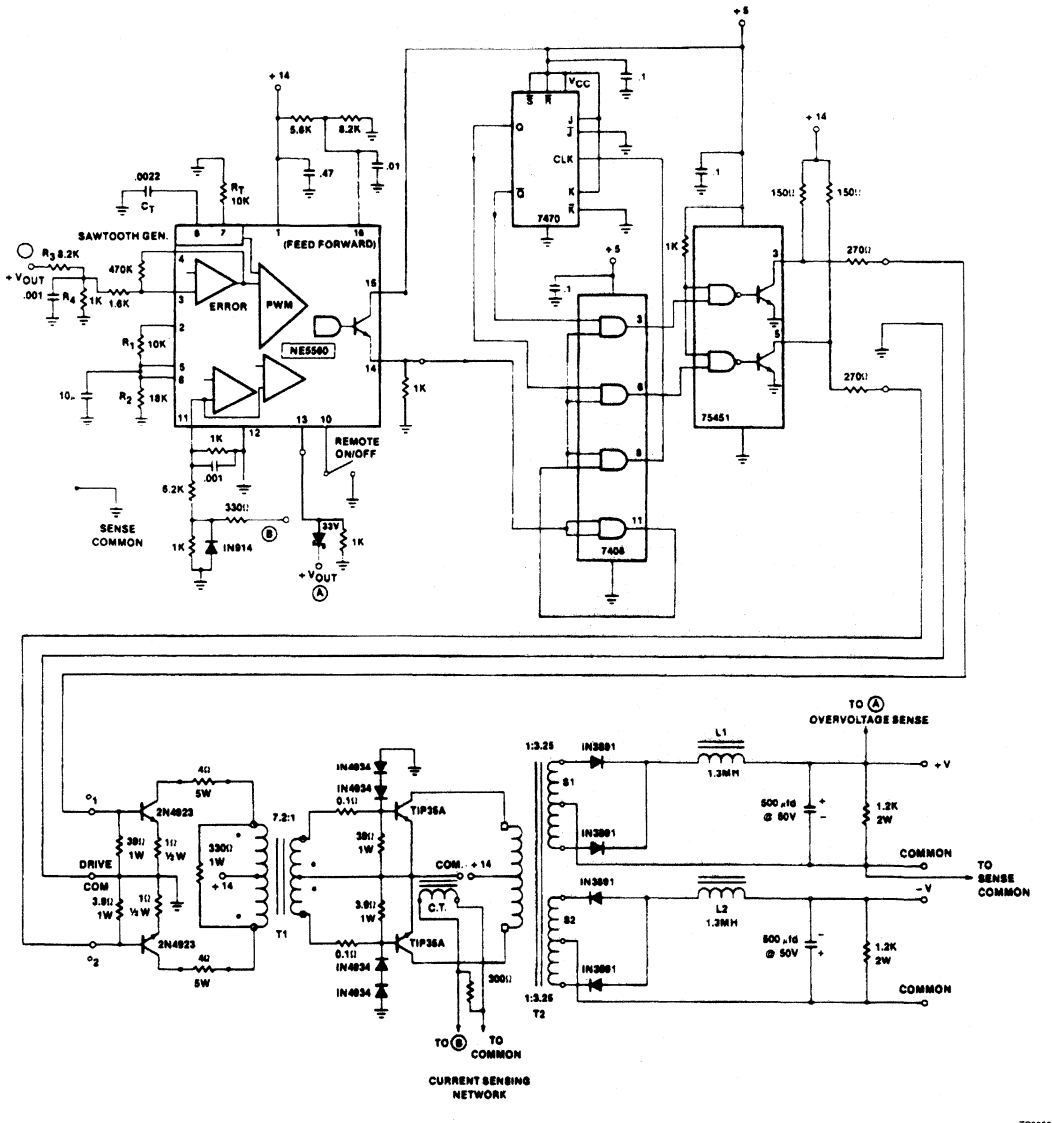
Power ground and signal ground must be kept separated

T_1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622 3C8 material
C.T. = 50T #26 on Ferroxcube 2616 core (3C8) F2D bobbin

T2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22,
Core = Ferroxcube 4229 3C8 material

L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material.

Figure 19. NE/SE5560 Push-Pull Switched-Mode Regulated Supply With CMOS Drive Conversion Logic



TC08861S

NOTES:
Power ground and signal ground must be kept separated
T_1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622 3C8 material
C.T. = 50T #26 on Ferroxcube 2616 core (3C8) F2D bobbin
T2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22,
Core = Ferroxcube 4229 3C8 material
L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material.

Figure 20. NE/SE5560 Push-Pull Switched-Mode Regulated Supply With TTL Drive Conversion Logic

NE/SE5561
Switched-Mode Power Supply Control Circuit

Product Specification

DESCRIPTION

The NE5561/SE5561 is a control circuit for use in switched-mode power supplies. It contains an internal temperature-compensated supply, PWM, sawtooth oscillator, overcurrent sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required.

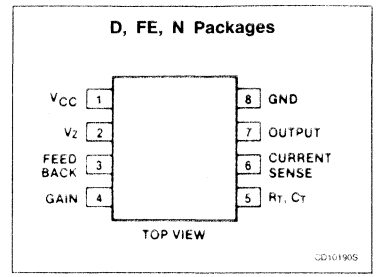
FEATURES

- **Micro-miniature (D) package**
- **Pulse-width modulator**
- **Current limiting (cycle-by-cycle)**
- **Sawtooth generator**
- **Stabilized power supply**
- **Double pulse protection**
- **Internal temperature-compensated reference**

APPLICATIONS

- **Switched-mode power supplies**
- **DC motor controller inverter**
- **DC/DC converter**

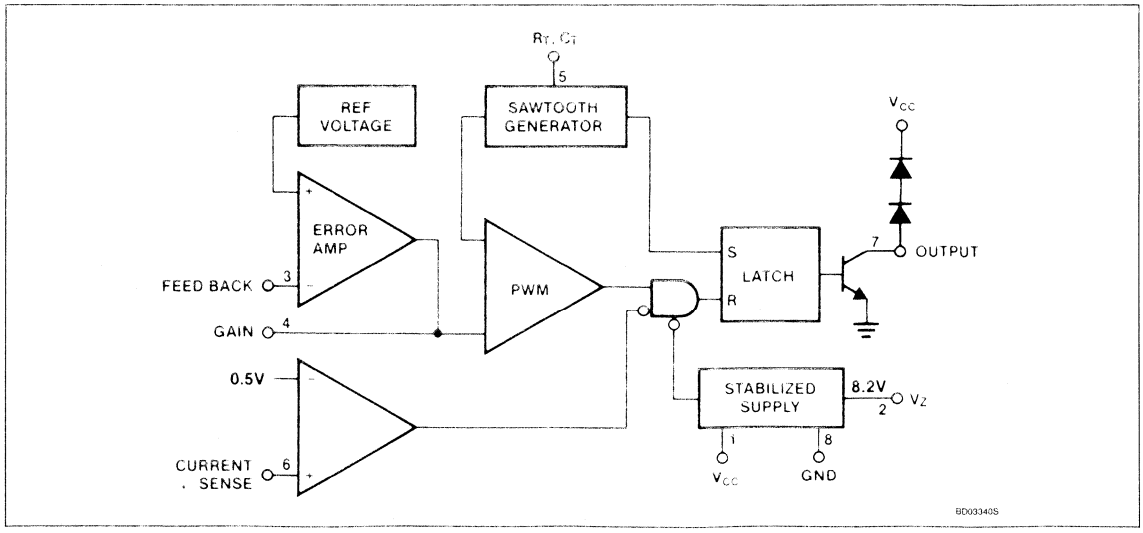
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5561N
8-Pin Plastic DIP	−55 to +125°C	SE5561N
8-Pin Cerdip	0 to +70°C	NE5561FE
8-Pin Cerdip	−55 to +125°C	SE5561FE
8-Pin SO	0 to +70°C	NE5561D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply[1]		
	Voltage-forced mode	+18	V
	Current-fed mode	30	mA
	Output transistor (at 20-30V max)		
I_{OUT}	Output current	40	mA
V_{OUT}	Output voltage	V_{CC} + 1.4V	V
	Output duty cycle	98	%
P_D	Maximum total power dissipation	0.75	W
T_A	Operating temperature range		
	SE5561	−55 to +125	°C
	NE5561	0 to 70	°C

NOTE:
1. See Voltage-Current-fed supply characteristic curve.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 12V, T_A = 25°C, unless otherwise specified.

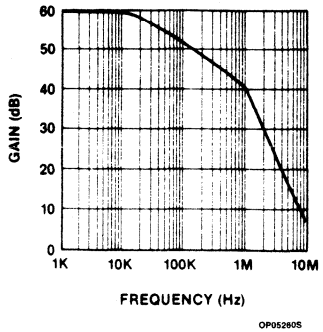
SYMBOL	PARAMETER	TEST CONDITIONS		SE5561			NE5561			UNIT
				Min	Typ	Max	Min	Typ	Max	
Reference section										
V_{REF}	Internal ref voltage	T_A = 25°C		3.69	3.75	3.84	3.57	3.75	3.96	V
		Over temperature		3.65		3.88	3.55		3.98	V
V_Z	Internal zener ref	*I_L = 7mA		7.8	8.2	8.8	7.8	8.2	8.8	V
	Temp. coefficient of V_{REF}				±100			±100		ppm°C
	Temp. coefficient of V_Z				±200			±200		ppm/°C
Oscillator section										
	Frequency range	Over temperature		50		100k	50		100k	Hz
	Initial accuracy	R_T and C_T constant			5			5		%
	Duty cycle range	f_O = 20kHz		0		98	0		98	%
Current limiting										
I_{IN}	Input current	Pin 6 = 250mV	T_A = 25°C		−2	−10		−2	−10	μA
			Over temp.			−20			−20	μA
	Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	I_{OUT} = 20mA		0.88	1.10		0.88	1.10	μs
			I_{OUT} = 40mA		0.7	0.8		0.7	0.8	μs
	Current limit trip level			.400	.500	.600	.400	.500	.600	V
Error amplifier										
	Open-loop gain				60			60		dB
	Feedback resistor			10k			10k			Ω
BW	Small-signal bandwidth				3			3		MHz
V_{OH}	Output voltage swing			6.2			6.2			V
V_{OL}	Output voltage swing					0.7			0.7	V
Output stage										
I_{OUT}	Output current	Over temperature		20			20			mA
V_{CE}	Sat	I_C = 20mA, Over temp.				0.4			0.4	V

DC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V, T_A = 25°C, unless otherwise specified.

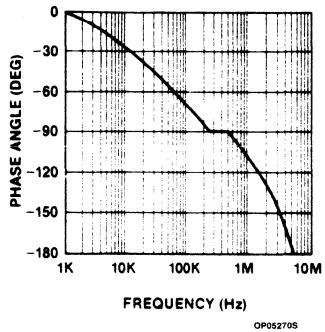
SYMBOL	PARAMETER	TEST CONDITIONS		SE5561			NE5561			UNIT
				Min	Typ	Max	Min	Typ	Max	
Supply voltage/current										
I_{CC}	Supply current	I_Z = 0, voltage-forced	T_A = 25°C			10.0			10.0	mA
			Over temp.			13.0			13.0	mA
V_{CC}	Supply voltage	I_{CC} = 10mA, current-fed		20.0	21.0	22.0	19.0	21.0	24.0	V
		I_{CC} = 30mA current		20.0		30.0	20.0		30.0	V
Low supply protection										
	Pin 1 threshold			8	9	10.5	8	9	10.5	V

TYPICAL PERFORMANCE CHARACTERISTICS

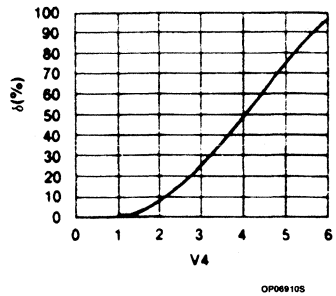
Error Amplifier Open-Loop Gain



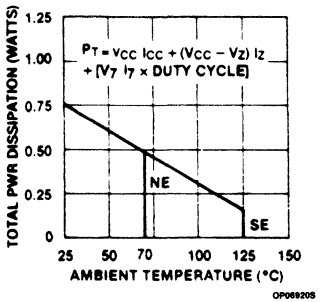
Error Amplifier Open-Loop Phase



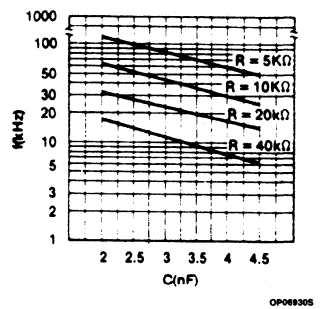
Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage

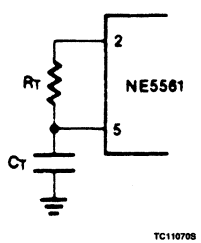


Power Derating Curve

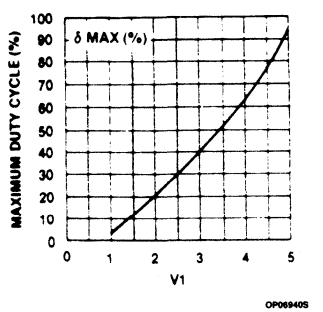


Typical Frequency Plot vs R_T and C_T

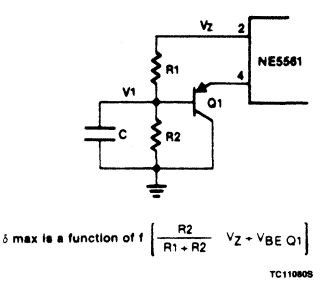




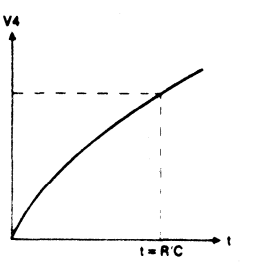
Maximum Duty Cycle vs Base Voltage on Q1



Start-Up Circuit

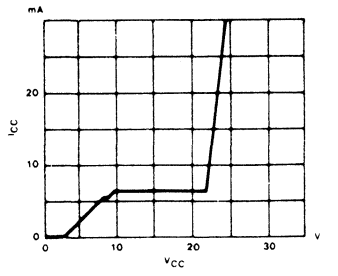


Slow-Start Voltage



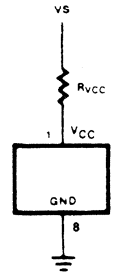
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

NE5561 Voltage-Current-Fed Supply Characteristics



OP06960S

Current-Fed Dropping Resistor



TC11090S

$$R_{VCC} = \frac{V_S - V_{CC}}{(10 \text{ to } 20mA)}$$

NOTE:
See DC Electrical Characteristics for Current Fed V_{CC} Range.

NE5561 Start-Up

The start-up, or initial turn-on, of this device requires some degree of external protective duty cycle limiting to prevent the duty cycle from initially going to the extreme maximum ($\delta > 90\%$). Either overcurrent limit or slow-start circuitry must be employed to limit duty cycle to a safe value during start-up. Both may be used, if desired.

To implement slow-start, the start-up circuit can be used. The divider R1 and R2 sets a voltage, buffered by Q1, such that the output of the error amplifier is clamped to a maximum output voltage, thereby limiting the maximum duty cycle. The addition of capacitor C will cause this voltage to ramp-up slowly when power is applied, causing the duty cycle to ramp-up simultaneously.

Overcurrent limit may be used also. To limit duty cycle in this mode, the switch current is monitored at Pin 6 and the output of the 5561 is disabled on a cycle-by-cycle basis when current reaches the programmed limit. With current limit control of slow-start, the duty cycle is limited to that value, just allowing maximum switch current to flow. (Approximately 0.50V measured at Pin 6.)

APPLICATIONS

5V, 0.5A Buck Regulator Operates from 15V

The converter design shows how simple it is to derive a TTL supply from a system supply of 15V (see Figure 1). The NE5561 drives a 2N4920 PNP transistor directly to provide switching current to the inductor.

Overall line regulation is excellent and covers a range of 12V to 18V with minimal change (< 10mV) in the output operating at full load.

As with all NE5561 circuits, the auxiliary slow start and δ_{MAX} circuit is required, as evidenced by Q1. The δ_{MAX} limit may be calculated by using the relationship:

$$\frac{R2}{R1 + R2}(8.2V) = V\delta_{MAX}$$

The maximum duty cycle is then determined from the pulse-width modulator transfer graph, with R1 and R2 being defined from the desired conditions.

NE/SE5562
Switched-Mode Power Supply Control Circuit

Product Specification

DESCRIPTION

The NE/SE5562 is a single-output control circuit for switched-mode power supplies. This single monolithic IC contains all control and protection features needed for full-featured switched-mode power supplies.

The 100mA source/sink output is designed to drive power FETs directly. The associated output logic is designed to prevent double pulsing or cross-conduction current spiking on the output.

All of the control and protect features work cycle-by-cycle up to the maximum operating frequency of 600kHz.

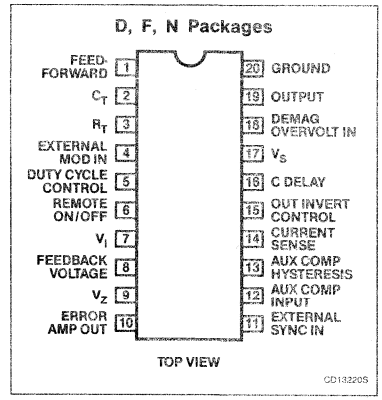
For ease of interface, all digital inputs are TTL or CMOS compatible.

The NE5562 is supplied in 20-pin glass/ceramic (Cerdip), plastic DIP, and plastic SO packages. The NE grade part is characterized and guaranteed over the commercial ambient temperature range of 0°C to +70°C and junction temperature range of 0°C to +85°C. The SE5562 is supplied in the glass/ceramic (Cerdip) package. The SE grade part is characterized and guaranteed over the ambient temperature range of −55 to +125°C and junction temperature range of −55 to +135°C.

FEATURES

- **Stabilized power supply**
- **Temperature-compensated reference source**
- **Sawtooth generator**
- **Pulse width modulator**
- **Remote on/off switching**
- **Current limiting (2 levels)**
- **Auxiliary comparator, with adjustable hysteresis**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Duty cycle adjust and clamp**
- **Feed-forward control**
- **External synchronization**
- **Total shutdown after adjustable number of overcurrent faults**
- **Soft-start**

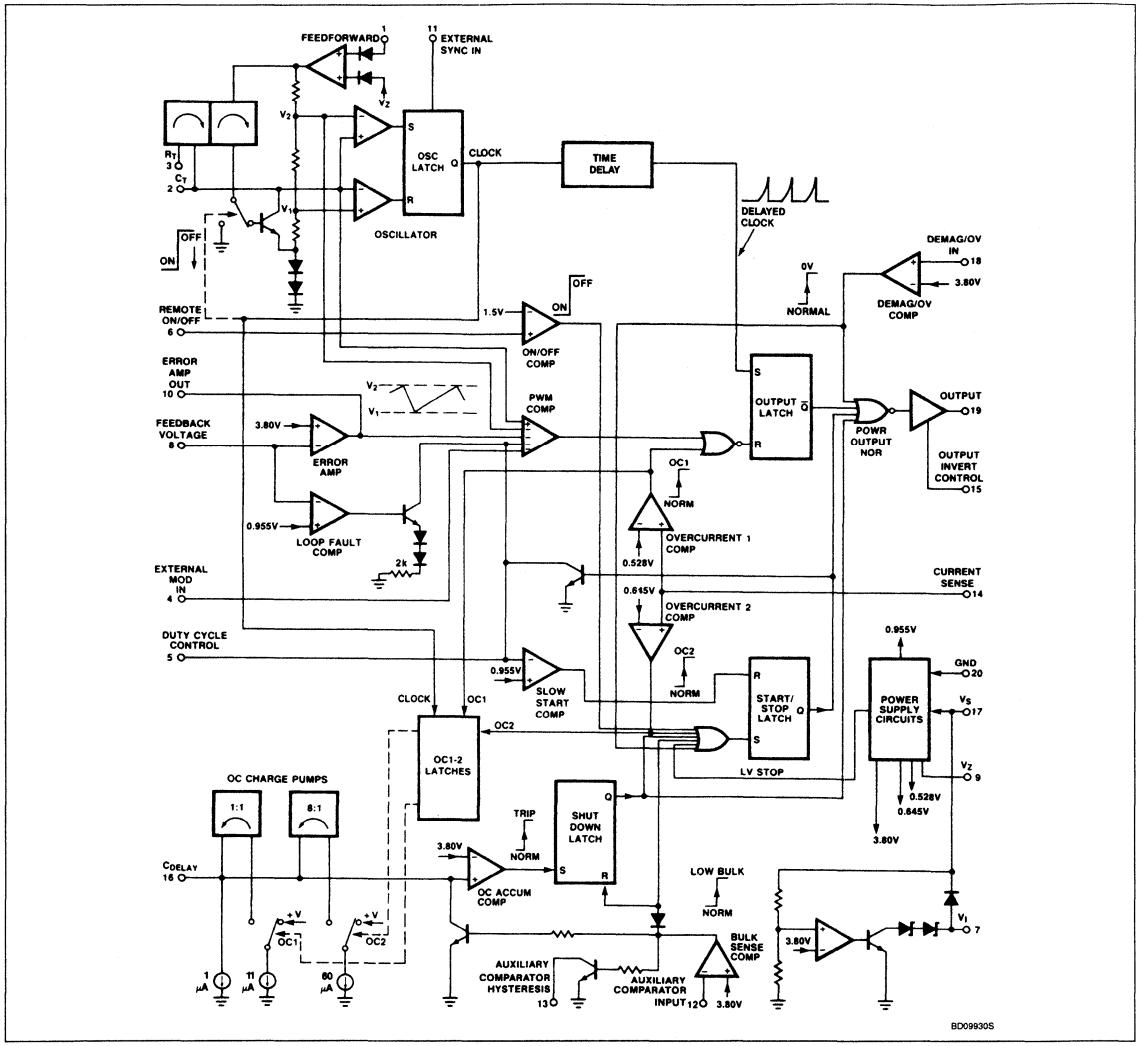
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SO	0 to +70°C	NE5562D
20-Pin Ceramic DIP	0 to +70°C	NE5562F
20-Pin Plastic DIP	0 to +70°C	NE5562N
20-Pin Ceramic DIP	−55°C to +125°C	SE5562F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S I_{CC}	Supply voltage-fed mode (Pin 17) current-fed mode (Pin 7)	 16 30	 V mA
	Output transistor output current	100	mA
	Sync (Pin 11)	V_S	V
	Duty cycle control (Pin 5)	V_Z	V
	Remote on/off (Pin 6)	V_S	V
	Output invert control (Pin 15)	V_S	V
	Feedback pin (Pin 8)	V_Z	V
	C_{DELAY} (Pin 16)	V_Z	V
	External mod in (Pin 4)	V_S	V
FF	Feed-forward (Pin 1)	V_S	V
	Demag/overvoltage in (Pin 18)	V_Z	V
	Current sense (Pin 14)	V_S	V
	Low supply sense and hysteresis (Pins 12, 13)	V_S	V
T_J	Operating junction temperature	135	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec)	300	°C

NOTES:
1. Ground Pin 20 must always be the most negative pin.
2. For power dissipation, see the application section which follows.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage-fed current-fed	 10 to 16 15	 V mA
T_A	Ambient temperature range NE grade SE grade	 0 to +70 −55 to +125	 °C °C
T_J	Junction temperature range NE grade SE grade	 0 to +85 −55 to +135	 °C °C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Internal reference										
V_{REF}	Reference voltage	Internal	T_A = 25°C	3.76	3.80	3.84	3.76	3.80	3.84	V
V_{REF}	Reference voltage	Internal	Over temp.	3.72	3.8	3.90	3.725	3.8	3.870	V
	Temperature stability	Internal			30			30		ppm/°C
	Long-term stability	Internal			0.5			0.5		μV/ 1000hrs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Reference										
V_Z	Zener voltage	9	I_L = 7mA, T_A = 25°C	7.35	7.60	7.75	7.35	7.6	7.75	V
V_Z	Zener voltage	9	I_L = 7mA, Over temp.	7.25		7.80	7.20		7.78	V
$\triangle V_Z/\triangle T$	Temperature stability	9	I_L < 1mA		50			50		ppm/°C
Low supply shutdown										
	Comparator threshold voltage	Internal	T_A = 25°C	8.30	8.45	8.75	8.30	8.45	8.75	V
	Comparator threshold voltage	Internal	Over temp.	8.00	8.45	8.90	8.00	8.45	8.90	V
	Hysteresis	Internal		25	50	8.00	25	50	800	mV
Oscillator										
f_{MIN}	Frequency range, minimum	1, 2, 3, 11	R_T = 42.7kΩ, C_T = 0.47μF		60	80		60	80	Hz
f_{MAX}	Frequency range, maximum	1, 2, 3, 11	R_T = 2.87kΩ, C_T = 380pF	600			600			kHz
	Initial accuracy	1, 2, 3, 11	f_O = 52kHz, R_T = 16kΩ and C_T = 0.0015μF, T_A = 25°C	48.6	54	59.4	48.6	54	59.4	kHz
	Voltage stability	1, 2, 3, 11, 17	10V < V_S < 18V		−215			−215		ppm/V
	Temperature stability	1, 2, 3, 11			300	500		300	500	ppm/°C
	Sawtooth peak voltage	2, 3	T_A = 25°C[1]	5.00	5.25	5.40	5.00	5.25	5.40	V
		2, 3	Over temp.	4.80	5.25	5.60	4.80	5.25	5.60	V
	Sawtooth valley voltage	2, 3	T_A = 25°C	1.25	1.70	2.00	1.25	1.70	2.00	V
		2, 3	Over temp.	1.0	1.7	2.1	1.25	1.7	2.0	V
	Sync. in high level	11		2.0		V_Z	2.0		V_Z	V
	Sync. in low level	11		0.0		0.8	0.0		0.8	V
	Sync. in bias current	11	(Sourced), V_{11} < 0.8V		0.50	10.0		0.50	10.0	μA
	Feed-forward ratio, maximum	1			2			2		
	Feed-forward duty cycle reduction	1	V_{FF} = 2V_Z, T_A = 25°C	11	13.5	19	11	13.5	19	%
		1	Over temp.	6	13.5	22	8		22	%
	Feed-forward reference voltage	9			V_Z	V_S		V_Z	V_S	V
	Feed-forward bias current	1			2.5	50.0		2.5	50.0	μA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Error amp										
I_{BIAS}	Input bias current	8			1.0	5.0		1.0	5.0	μA
A_{VOL}	DC open-loop gain	8, 10	R_L > 100kΩ	60	86		60	86		dB
V_{OH}	High output voltage	10	I_{SOURCE} = 1mA	5			5			V
V_{OL}	Low output voltage	10	I_{SINK} = 1mA			2.0			2.0	V
	PSRR from V_Z and V_S	Internal	f_O < 300kHz		−40			−40		dB
BW	Small-signal gain band-width product				8			8		MHz
	Feedback resistor range			1		240	1		240	kΩ
I_{SINK}	Output sink current		V8 = V10 = 5V			10			10	mA
I_{SOURCE}	Output source current		V8 = 3V, V10 = 1V			5			5	mA
	Sawtooth feedthrough		A_V = 100, 0% duty cycle		200			200		mV
PWM comparator and modulator										
	Minimum duty cycle	19	@V_{COMP} <, f = 300kHz	0			0			%
	Maximum duty cycle	19	@V_{COMP} >, f = 300kHz, V15 = 0V	95		98	95		98	%
A_{CC}	Duty cycle	10, 19	f = 15kHz to 200kHz, V_{IN} = 0.472 V_Z	41	49	55	41	49	55	%
t_{PD}	Propagation delay to output	2, 19	V_{15} = 0		400			400		ns
I_{BIAS}	Bias current, external modulator input	4	(Sourced)		0.20	20		0.20	20	μA
I_{BIAS}	Bias current, duty cycle control	5	(Sourced)		0.20	20		0.20	20	μA
	Soft-start trip voltage	5		.910	0.955	0.990	0.922	0.955	0.988	V
Remote on/off (shutdown)										
	Output enabled	6		0		0.80	0		0.80	V
	Output disabled	6		2		V_Z	2		V_Z	V
I_{BIAS}	Bias current	6			1	10		1	10	μA
V_{IN}	Maximum input voltage	6		V_Z			V_Z			V
	Delay to output(s)	6, 19			400			400		ns

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Current limit comparator(s)										
	Shutdown, OC2	14		.593	0.645	.697	0.593	0.645	0.697	V
	Minimum duty cycle, OC1	14		.486	0.528	.570	0.486	0.528	0.570	V
I_{BIAS}	Bias current	14	(Sourced)		0.5	50		0.5	50	μA
OC_1	C_{DELAY} charge current	16		−18.2	−13	−6.5	−18.2	−13	−7.8	μA
OC2	C_{DELAY} charge current	16		−770	−550	−250	−770	−550	−330	μA
C_{DELAY}	Discharge current	16	$V12 = V_Z$	0.4	1.4	4.0	0.8	1.4	2.0	μA
C_{DELAY}	Shut off trip level	16	T_A = 25°C	3.75	3.86	3.97	3.75	3.86	3.97	V
Auxiliary comparator with shutdown										
I_{BIAS}	Bias current	12	(Sourced)		1	10		1	10	μA
	Threshold voltage	12		3.69	3.80	3.91	3.69	3.80	3.91	V
C_{DELAY}	Discharge current	12	V_{IN} = 3V	5	10		5	10		mA
	Hysteresis	12, 13			10			10		mV
Demagnetization overvoltage comparator										
I_{BIAS}	Bias current	18			2	10		2	10	μA
	Threshold voltage	18		3.62	3.80	3.91	3.69	3.80	3.91	V
	Hysteresis	18			10			10		mV
Output stage										
V_{OH}	High output voltage	19	I_{SOURCE} = 100mA	V_S − 2.5	V_S − 1.9		V_S − 2.5	V_S − 1.9		V
V_{OL}	Low output voltage	19	I_{SINK} = 2mA		0.16	0.4		0.16	0.4	V
V_{OL}		19	I_{SINK} = 100mA, T_A = 25°C		1.4	2.0		1.4	2.0	V
		19	I_{SINK} = 100mA, over temp.			2.25			2.25	V
	I_{SINK} max	19		100			100			mA
	I_{SOURCE} max	19		100			100			mA
t_R	Rise time	19	C_L = 2000pF		160			160		ns
t_F	Fall time	19	C_L = 2000pF		80			80		ns
Supply current/voltage										
I_{CC}	Supply current	17	10V < V_S < 16V (Voltage-fed mode), $V_I < V_S$		9	15		9	15	mA
V_S	Input voltage	7, 17	I_I = 15mA, (Current-fed mode) V_S = meter	14.2	15.3	16.7	14.2	15.3	16.7	V
Operating frequency range for all functions but feed-forward working cycle-by-cycle										
f_{MIN}	Minimum frequency	All	R_T = 42.7kΩ, C_T = 0.47μF		60	80		60	80	Hz
f_{MAX}	Maximum frequency	All	R_T = 2.87kΩ, C_T = 380pF	600	1000		600	1000		kHz

NOTE:
1. Sawtooth peak and valley voltages were designed to be temperature-dependent to provide the frequency independence of temperature.

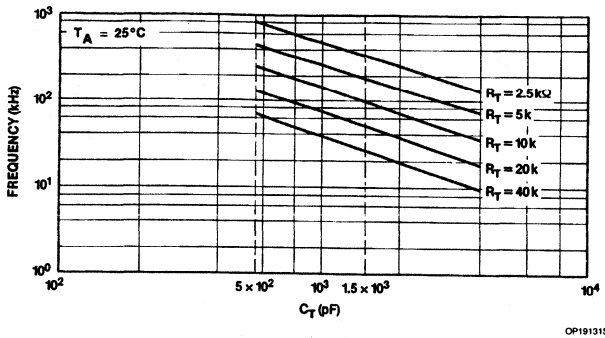


Figure 1. Frequency vs R_T, C_T NE/SE5562

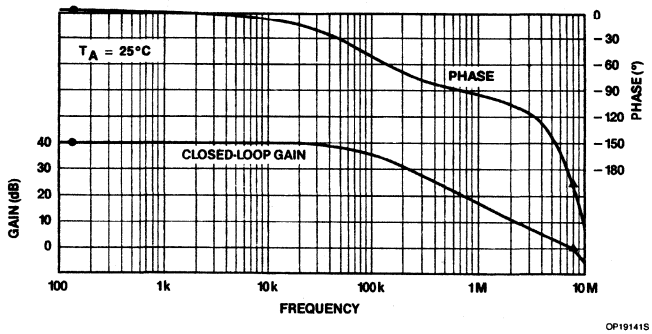


Figure 2. Error Amplifier Closed-Loop Response

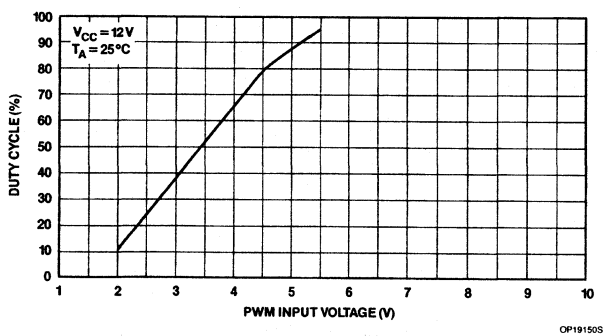


Figure 3. Duty Cycle vs PWM Input Voltage

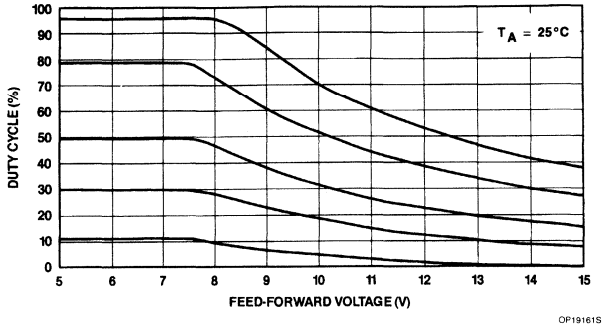


Figure 4. Duty Cycle vs Feed-forward Voltage

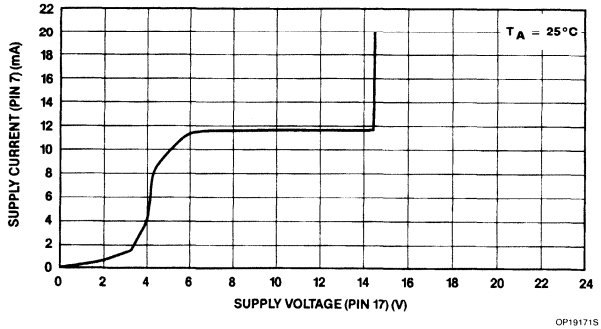


Figure 5. Current-Feed Characteristics

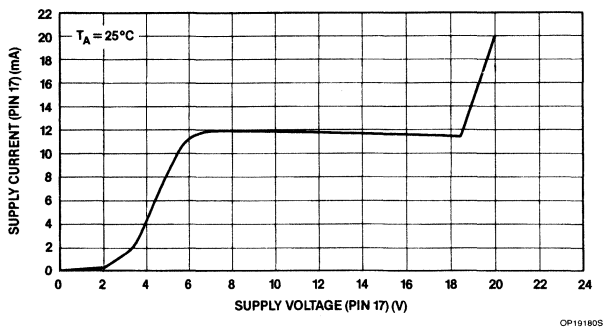


Figure 6. Voltage-Feed Characteristics

THE NE/SE5562 THEORY OF OPERATION

INTRODUCTION

Switched-mode power conversion relies on the principle of pulsed energy storage in an inductive or capacitive element. Capacitive switched converters are typically used with low power systems for which only tens of milliamperes are required. Medium and high power converters tend to use inductive storage elements as shown in Figures 7 – 9 with which a single switch may be moved around to create step-up (flyback) positive or negative polarity and step-down (forward or buck) conversion from a fixed-voltage source. The relationship between input and output voltage in each case is controlled by the switching on-to-off ratios, which is termed duty cycle. Duty cycle modulation is the common factor in this basic type of power control mechanism. By adding a high-gain operational amplifier, having one input tied to a stable DC reference voltage, configured in a negative feedback loop to maintain a constant output voltage as shown in Figure 10, the switched-mode controller becomes a dynamic voltage regulator. It is this single-switch topology that is most readily adapted to the NE/SE5562 SMPS Control IC.

The ability to switch inductor currents at rates up to 600kHz with state-of-the-art power FETs makes the design of small, efficient switching power converters an attainable reality. Protective features such as programmable slow-start and cycle-by-cycle current limiting allow safe, maintenance-free power supplies to be mass-produced at reduced cost to the manufacturer. Integrated technology makes long-term reliability a predictably achievable goal.

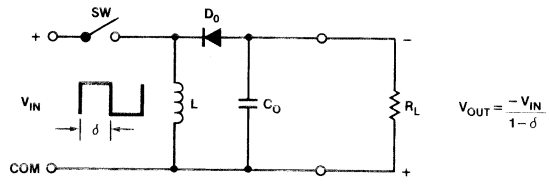


Figure 7. Negative Output Flyback Converter

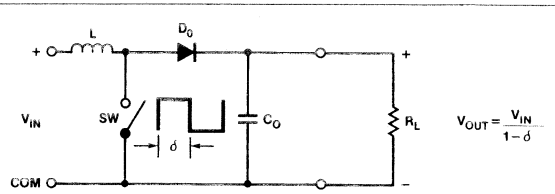


Figure 8. Positive Output Flyback Converter

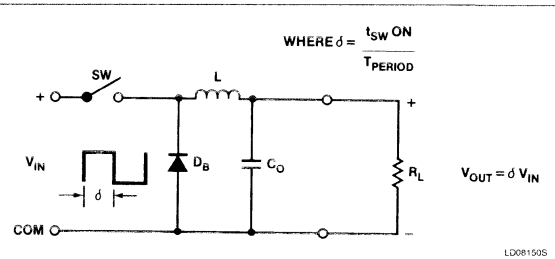


Figure 9. Forward Converter (Single Inductor) Step Down

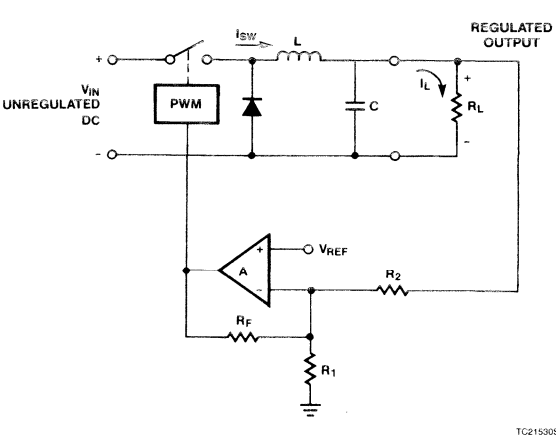


Figure 10. The Forward (Buck) Converter ($V_{OUT} = V_{IN}(\delta)$)

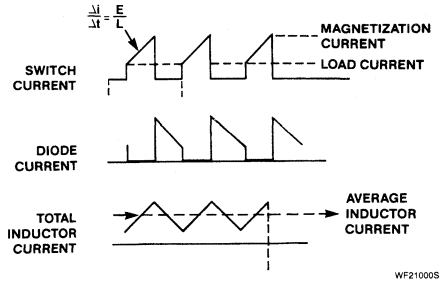


Figure 11. PWM Switching Waveforms

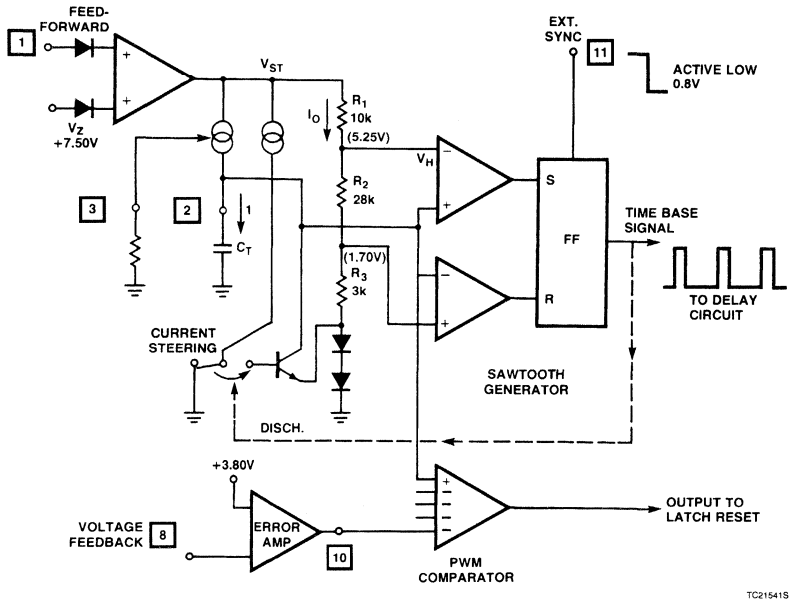


Figure 12

THE NE/SE5562 THEORY OPERATION

The Sawtooth Oscillator

The sawtooth oscillator consists of a gated charge-discharge capacitor circuit with threshold comparators setting the peak and valley voltages of the ramp. The resistor divider R1 – 3 is supplied with a source voltage derived from either V_Z (7.50V) minus two diode drops, or, when feed-forward is in control, a voltage greater than V_Z and proportional to the main supply voltage. The nominal upper threshold voltage is 5.25V and the lower threshold 1.70V. These then determine the sawtooth peak and valley voltages, respectively.

Operation

Beginning with the charge cycle, ramp voltage builds up on the timing capacitor due to a constant current supplied to the node at Pin 2. When capacitor voltage reaches the upper threshold, comparator A switches, setting the latching flip-flop. The output of the latch goes high, generating a clock pulse. The discharge transistor is simultaneously turned on, reducing charge on the timing capacitor to the point at which the lower threshold voltage, 1.70V, is reached. The lower comparator is then activated, resetting the latch and terminating the clock pulse. Note that the discharge transistor is referenced to the same return diodes as the threshold resistor divider and the discharge current is made to track with the charge current. This charge and discharge tracking results in a true sawtooth waveform even at extended frequencies. Figure 15 shows a family of curves which explains the relationship between R_T, C_T, and the frequency of the sawtooth generator. The data sheet shows the initial accuracy of the oscillator at 60Hz and 600kHz.

THE PULSE WIDTH MODULATOR AND ERROR AMPLIFIER

The PWM consists of a multi-input voltage comparator (Figure 13) having its positive input tied to the sawtooth ramp voltage and the various negative inputs referenced to ORed control signal nodes. The primary control signal is the error amplifier output voltage node which sets the active duty cycle termination point of the PWM output waveform. As the error amplifier input signal derived from the power supply load voltage varies, for instance in a negative direction, the amplifier output moves upward, raising the PWM comparator toward longer duty cycles at the output on Pin 19. The start-up sequence begins with zero voltage at the input to the error amplifier. Since this could signal an open feedback loop, the loop fault comparator on Pin 8 clamps the PWM duty cycle until the feedback voltage exceeds 0.955V. A second comparator monitors the duty cycle control, Pin 5, with the same threshold level, inhibiting the output via the start-stop latch (Figure 14).

The charging of the slow-start capacitor provides a controlled ramp-up of the output duty cycle and a resultant gradual increase in energy fed to the output magnetics.

The dynamic response of the PWM comparator is shown in the simulated waveform drawing of Figure 15. The error amplifier output voltage is depicted as sloping positive (increasing) with time as referenced to the sawtooth waveform. This causes the duty cycle to increase with time. This is an indication of an increasing load on the power supply as output voltage is decreasing. The Pin 5 (δ_{MAX}) control voltage is also superimposed midway on the sawtooth, indicating the limits of duty cycle increase as the output waveform no longer increases in duty cycle after the δ_{MAX} threshold is crossed. A hypothetical overcurrent pulse (Pin 14) is shown to illustrate cycle termination immediately at the output (Pin 19).

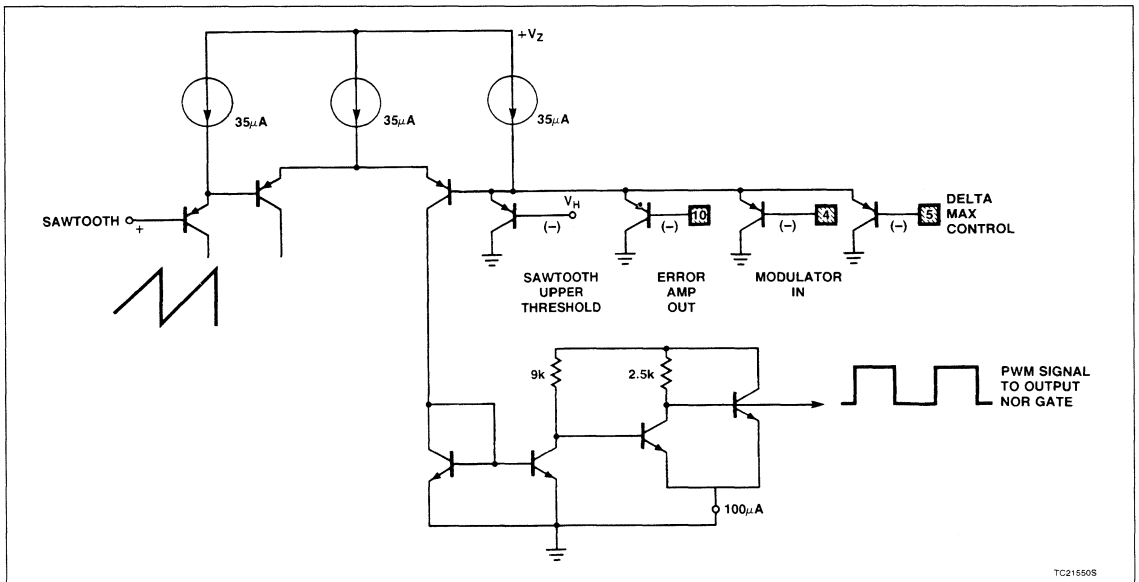


Figure 13. PWM Comparator

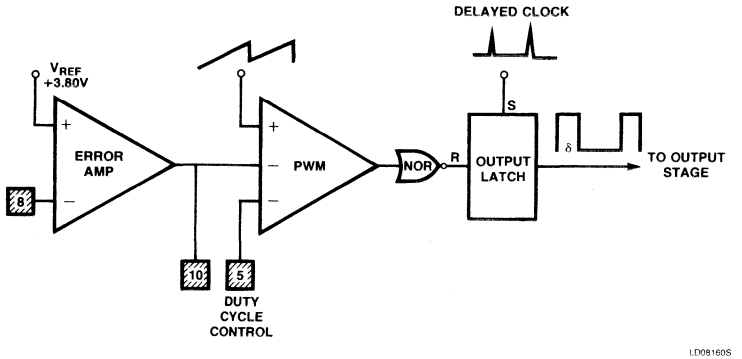


Figure 14. The Duty Cycle Control Circuit, Pulse Width Modulator, and Error Amplifier, Reference, and Output Latch

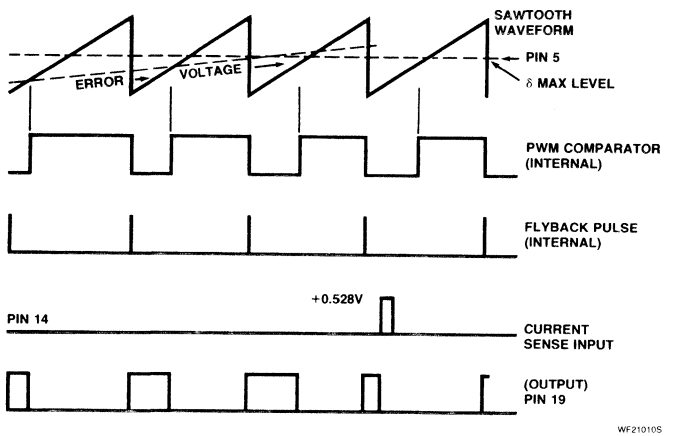


Figure 15. Duty Cycle vs Feedback Error and Overcurrent Sense

The error amplifier's non-inverting input is tied to a bandgap reference of 3.80V, accurate to ± 2% at 25°C. The temperature stability of the voltage reference is 30ppm/°C.

The error amplifier is designed for an open-loop gain of 86dB having a small-signal unity gain bandwidth of 3MHz. Closed-loop gain is stable to 10dB, as shown in Figure 17. The DC output excursion of the amplifier is capable of controlling the full PWM range of 0 to 95%. The amplifier can sink 10mA and source 5mA. The nominal DC output for 50% duty cycle is 3.55V. Feedback control resistor value may range from 1kΩ to 240kΩ without overload or instability. However, low closed-loop gains must be compensated by lag lead network techniques for optimum stability. Loop compensation networks may intersect the open-loop gain curve with a slope 2 closure and must then be compensated to maintain overall phase and gain margin (Figure 16).

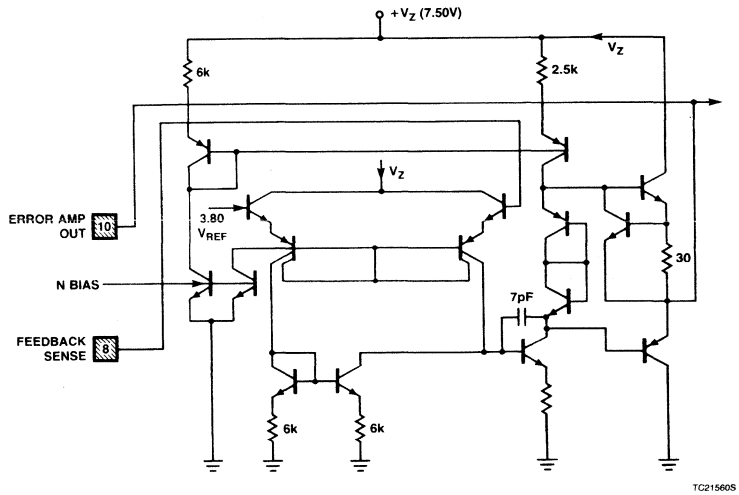


Figure 16. Error Amplifier

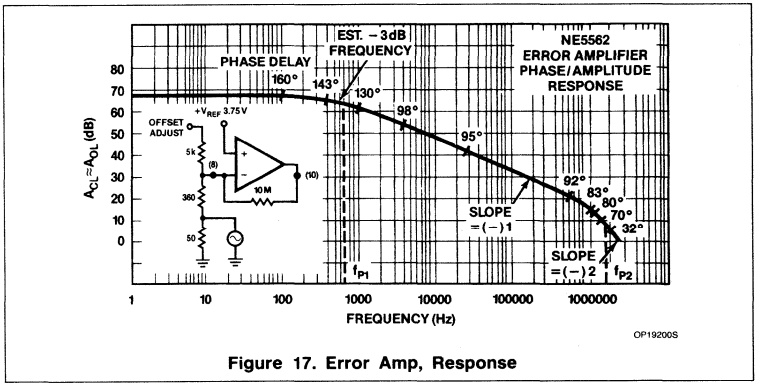


Figure 17. Error Amp, Response

Feed-Forward Compensation (Pin 1)

To provide a means of automatically improving line-to-load voltage regulation, a technique called feed-forward regulation is made a part of the NE/SE5562 active mechanism. Referring back to the diagram for the sawtooth oscillator, note that Pin 1 is capable of changing the internal supply voltage to the charging circuit for the timing capacitor, C_t. With a nominal duty cycle of 30%, for instance, increasing Pin 1 voltage by 1V from 10.3 to 11.3 will reduce the output duty cycle by approximately 5%. Thus, a primary has caused a decrease in volt-seconds (duty cycle X primary volts) of 5/30 or 16% (Figure 4). The result is a small over-compensation in the output energy, but an overall safe margin in transformer flux.

NOTE:
Figure 18 shows a delta V_1 of 7.5V.

The mechanism which produces inverse duty cycle modulation is shown in Figure 18. Increasing Pin 1 voltage beyond the value of V_z (7.50V) increases the charge rate on C_T, causing the duty cycle to be terminated earlier for each cycle that input voltage is increased. The threshold voltages at the sawtooth limit comparator reference inputs are changed with Pin 1 also in order to offset any change in oscillator frequency.

The secondary benefit of using feed-forward is the attenuation of any low-frequency AC riding on the DC supply before it reaches the regulated output.

Note that a start delay circuit is added to the Pin 1 divider in order to prevent internal race conditions during initial power-up. Once the turn-on transient has decayed, normal operation of the feed-forward circuit is assured. Figure 19 shows an RC delay placed in a base clamping circuit to provide reliable starting.

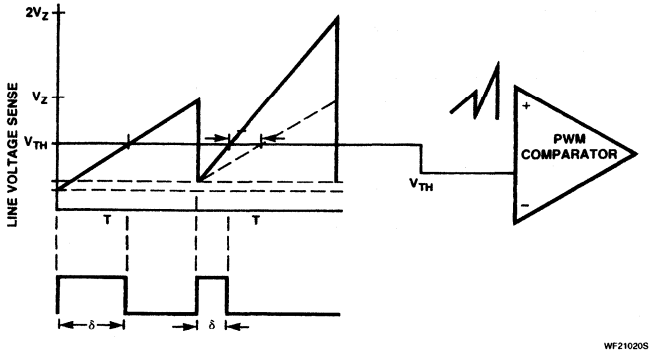


Figure 18. Feed-forward

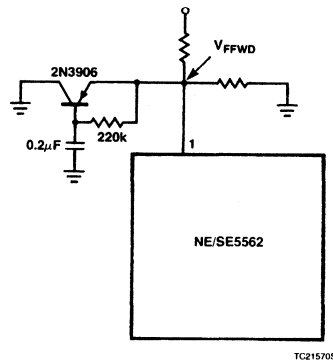


Figure 19. Feed-forward Turn-On Delay Circuit

SYNCHRONIZATION

The synchronization of the sawtooth oscillator to an external pulse of negative-going polarity is shown in Figure 20. When the sync input pulse crosses the 1.5V threshold, negative, the sawtooth oscillator is prevented from discharging the timing capacitor, causing the charge voltage on the capacitor to remain high (5.25V) until the sync pulse again goes above 1.5V, allowing reset. This action stretches the period of the oscillator and results in a lower frequency undersynchronization control than the free-running frequency.

NOTE:
See oscillator schematic, Figure 12, for sync circuit details.

The following relationship holds —

$$f_{free\text{-}run} > f_{sync}$$

$$f_{sync} = \frac{1}{t_0 + \tau}$$

A typical recommended starting point in calculating frequency for synchronous operation is to set the free-run frequency approximately 10% higher than the sync frequency. Then set the pulse width, τ, to 10% of t_0, the free-run period, with the desired new frequency determined by the sum as above.

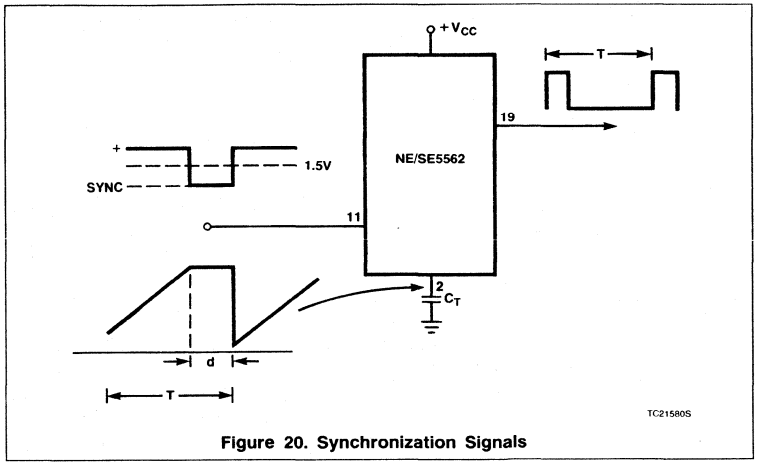


Figure 20. Synchronization Signals

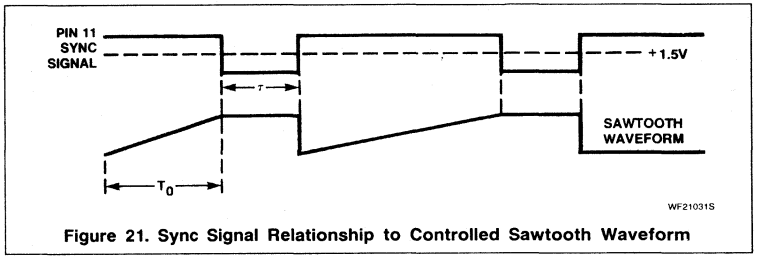


Figure 21. Sync Signal Relationship to Controlled Sawtooth Waveform

DUTY CYCLE LIMIT (PIN 5)

The forward or buck converter, and even the flyback converters, may require an automatic duty cycle limit to prevent transformer saturation or unstable behavior. A special input provides access to the PWM comparator for this purpose. As discussed previously in regard to the error amplifier, increasing load demand may drive the system current beyond safe limits. A simple solution is the placement of a duty cycle limit within the system dynamic response before this can occur. Figure 13 shows the PWM comparator with its multiple input ports. All are inverting in polarity and provide a lowest priority level sensing circuit. The lowest level on Pin 4, 5, or 10 gains control of the duty cycle limit. During normal operation, the δ_{MAX} circuit sends a continuous threshold signal tc the PWM comparator, setting a fixed limit on how much the error amplifier is allowed to increase the duty cycle in response to load demand. Figure 22 shows the circuit within the NE/SE5562 which actually controls duty cycle as listed below:

1. Duty cycle ramp-up (slow-start) during power-up. Time constant controlled by external R, C ramp voltage at Pin 5.
2. Slow-start if remote ON/OFF is actuated, if OC2 threshold trips, demagnetization/ overvoltage is sensed, or low supply voltage to the internal regulator is sensed ($V_S \leq 8.45V$).
3. Note that Pin 8 is monitored by the loop fault comparator. When the regulated supply feedback drops below this threshold level (0.955V), the duty cycle is clamped by two diodes in series with a 2kΩ load across Pin 5 to ground. This implies a minimum duty cycle condition as long as the low output level remains.

Referring to the graph in Figure 23, the designer may choose a divider ratio which, when referenced to V_Z, 7.5V, provides an easy duty cycle limit control. For example, a 50% limit results in a ratio of 0.48. Setting R_2 at a nominal value between 10 and 20kΩ and solving for R_1, the proper limit is obtained.

Example:

A duty cycle limit of 50% is required for a forward converter.

$R_2 = 10k\Omega$, find R_1

$$\frac{R_2}{R_1 + R_2} = 0.48$$

$$\therefore R_2 = 0.48\ (R_1 + R_2)$$

$$0.48R_1 = R_2 - 0.48R_2$$

$$\therefore R_1 = \frac{R_2(1 - 0.48)}{0.48}$$

$$= \frac{10k\Omega(0.52)}{0.48}$$

$$= 10.8k\Omega$$

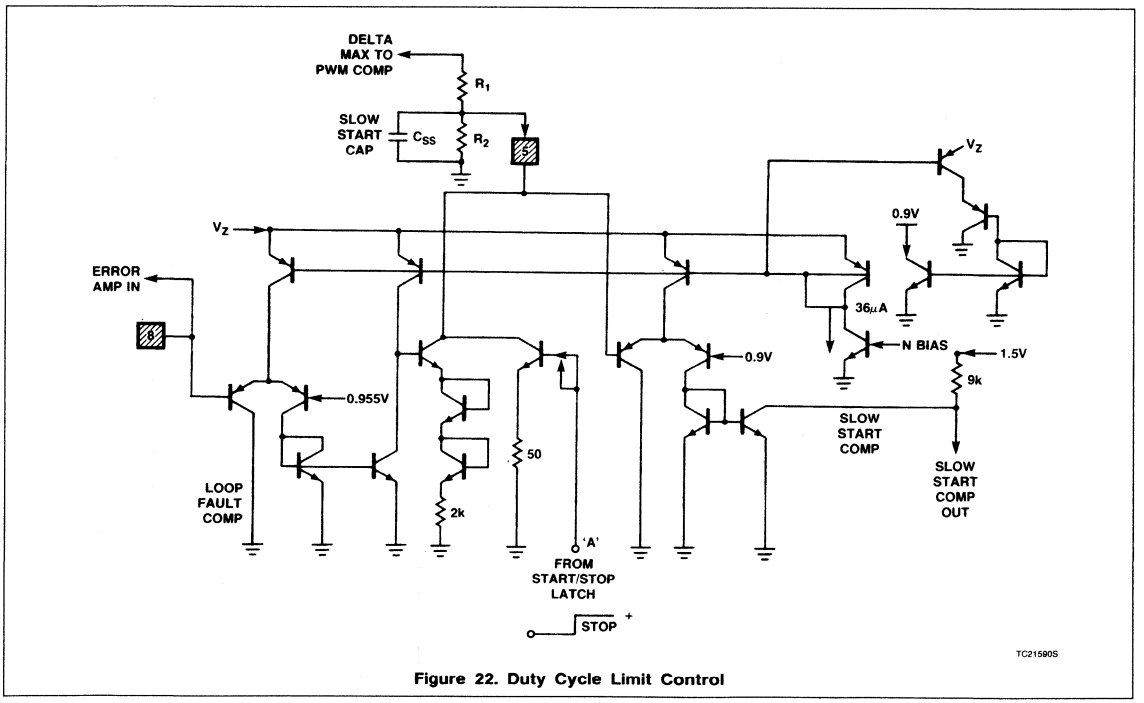


Figure 22. Duty Cycle Limit Control

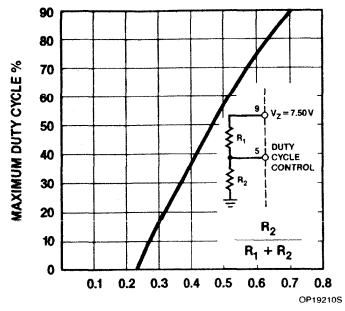


Figure 23. Maximum Duty Cycle

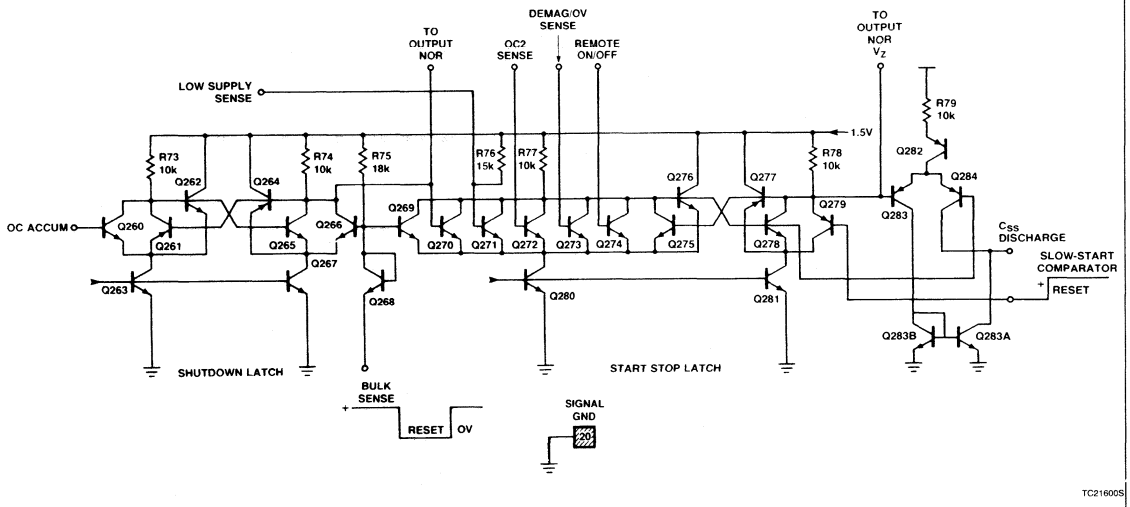


Figure 24. Start-Stop/Shutdown Latches

THE START-STOP CONTROL SEQUENCE

The start-up circuit involves a sequential set of conditions which progresses as follows: power-up after OFF condition or remote ON after OFF. Initially, 0V exist on the supply output, causing zero feedback volts on Pin 8. The slow-start capacitor is discharged, forcing Pin 5 to 0V, having been clamped by the internal discharge transistor. Internal supply regulator input exceeds 8.45V, releasing low voltage shutdown condition with Pin 5 below 0.955V. The slow-start comparator output goes high, resetting the start/stop latch, sending a low output signal to the output stage power NOR gate. The PWM signal is then enabled to feed the output drive circuits, starting energy flow through the magnetics. However, instantaneously the power supply output is still below 0.955V and the loop fault comparator forces the PWM to remain at a minimum duty cycle. The equivalent circuit at this instant in the start-up cycle which exists at Pin 5 is shown in Figure 26.

The actual minimum duty cycle is determined by the parallel source resistance of R_1 and R_2 combined with the shunt loading internal to Pin 5. High values of divider resistance, 20 – 30kΩ, will supply less shunt current to Pin 5 and create a lower modulator duty cycle, while lower values of R_1 and R_2 (5 – 10kΩ) will generate a higher modulator voltage and a greater resultant minimum duty cycle.

As the power conversion circuits become active and Pin 8 feedback voltage increases above 0.955V, the duty cycle network is unclamped; duty cycle increases, controlled by the RC time constant $R_1 \| R_2.C_{SS}$, and as output voltage brings the feedback voltage up to equal the reference voltage, 3.80V, the error amplifier takes control and the supply is in regulation.

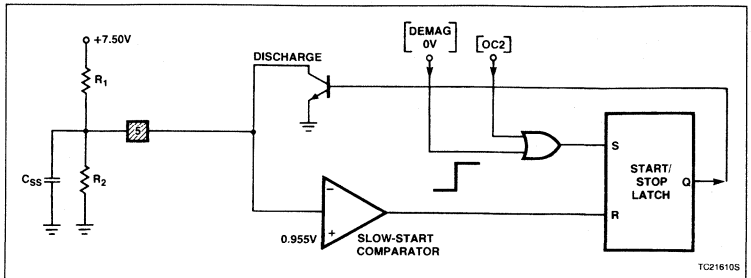


Figure 25. Slow-Start Comparator

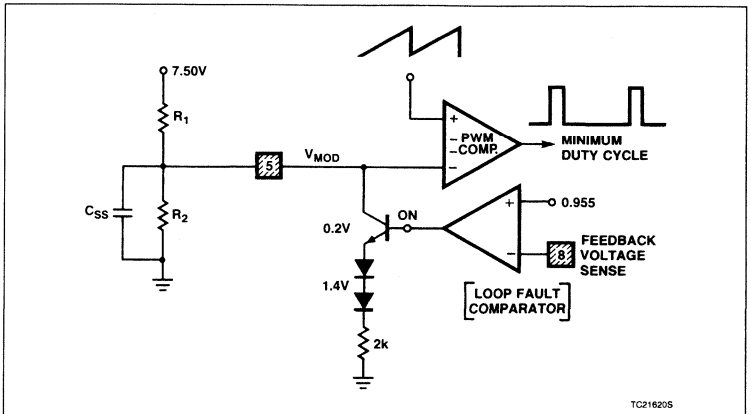


Figure 26. Loop Fault Comparator and Minimum Duty Cycle Clamp

The stop or shutdown sequence is initiated by any of the following conditions:

a. Supply voltage (bulk) sense below 3.80V at Pin 12.

b. Pin 17 below 8.45V or Pin 7 current below level (less than 9mA).

c. Remote ON/OFF voltage at Pin 6 greater than 2V.

d. Sustained OC2 causing C_{DLY} to charge above 3.80V (current sense on Pin 14 continuously above 0.645V peak).

DUAL-LEVEL OVERCURRENT COMPARATORS

The overcurrent sensing circuit (Figure 27) consists of a single PNP input buffer with emitter-follower tied to V_Z, 7.50V, feeding into the base of an NPN split-emitter transistor. This forms the input node to a set of dual-level voltage comparators with references of 0.528 and 0.645V, respectively. Current sources for the comparator are fixed biased NPNs.

The typical transition time delay for an overcurrent fault is 300ns. Bias current at the input averages 500nA.

If the overcurrent sense feature is not used, it is recommended that Pin 14 be tied to ground.

When used for sensing current-derived voltage impulses from the primary driver, a high-speed, low-impedance transient filter network is advised. An example is shown in Figure 28. Keep C_F close to the NE/SE5562.

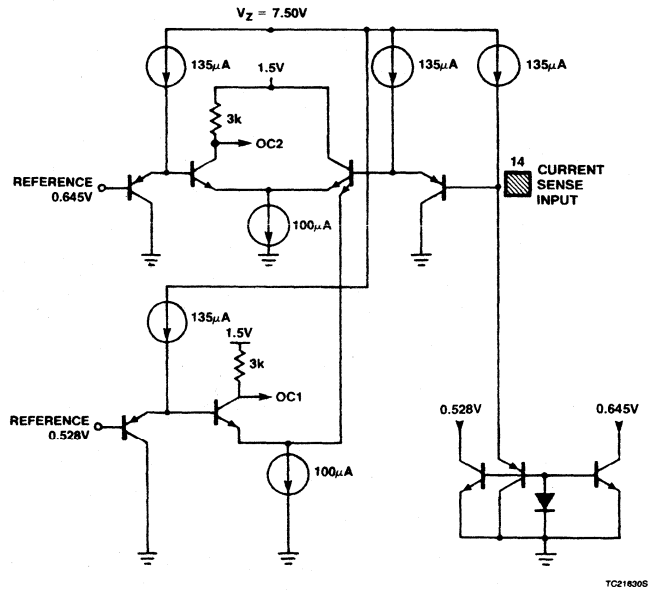


Figure 27. NE/SE5562 Overcurrent Comparator

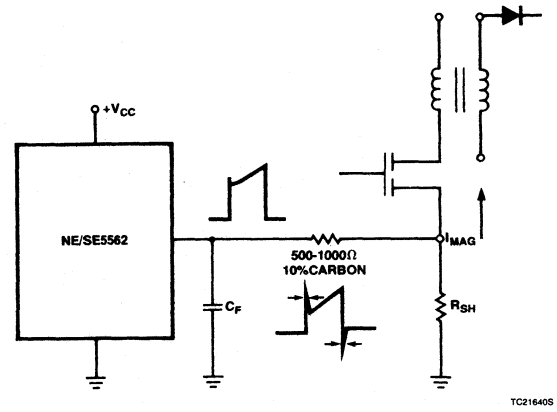


Figure 28. Transient Suppression

THEORY — OC1 AND OC2

Overcurrent Logic and Delay Capacitor Operations

The circuit takes a voltage input from Pin 14 and compares the level to a dual reference comparator with trips at 0.53 and 0.65V. The lower trip point actuates cycle-by-cycle shutdown of the output stage with an intrinsic delay of 400ns. The second level actuates the slow-start function. In addition, there exists a separate housekeeping circuit whose function is to terminate operation of the output stage if its threshold is exceeded. This involves a time delay circuit based on two separate switchable current sources, OC1 and OC2. The time delay capacitor allows the user to program shutdown of the system after a predetermined number of overcurrent cycles have occurred within the period set by the ramp-up of the delay capacitor. Once shutdown has occurred in this manner, external reset is required to restart the system. Referring to the logic block Figure 29, which controls the gating of the two charge pumps into the delay capacitor at Pin 16, the complete signal flow may be traced. Logic signals from the overcurrent 1 and 2 comparators are gated by the clock and delayed clock signals generated by the sawtooth oscillator. The complete sequence for an overcurrent fault may be understood by referring to Figure 30 for OC2. Here it is shown that an OC2 signal exists indicating that the 0.65V threshold has been exceeded by a signal at Pin 14.

Note that an overcurrent pulse within a particular clock frame turns on the respective OC2 charge ramp during the entire next clock frame. Consecutive overcurrent pulses of either OC1 or OC2 magnitude will activate the selected charge pump for the total duration that such overcurrent occurs. The charging cycle will continue until the delay capacitor reaches the 3.86V trip level.

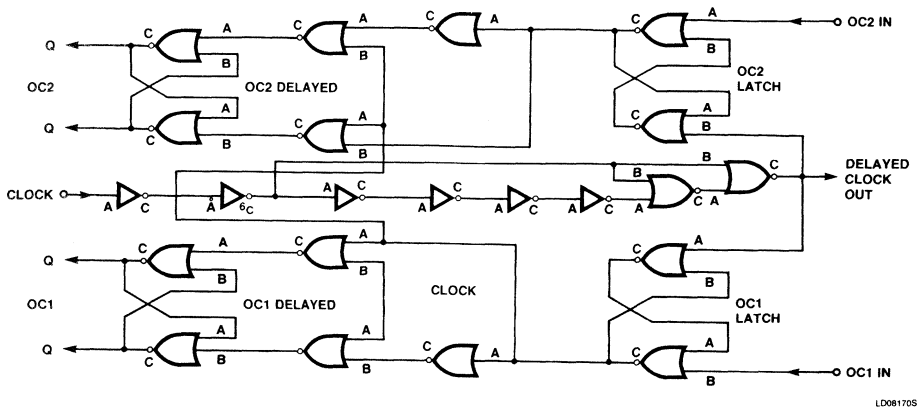


Figure 29. Overcurrent Logic

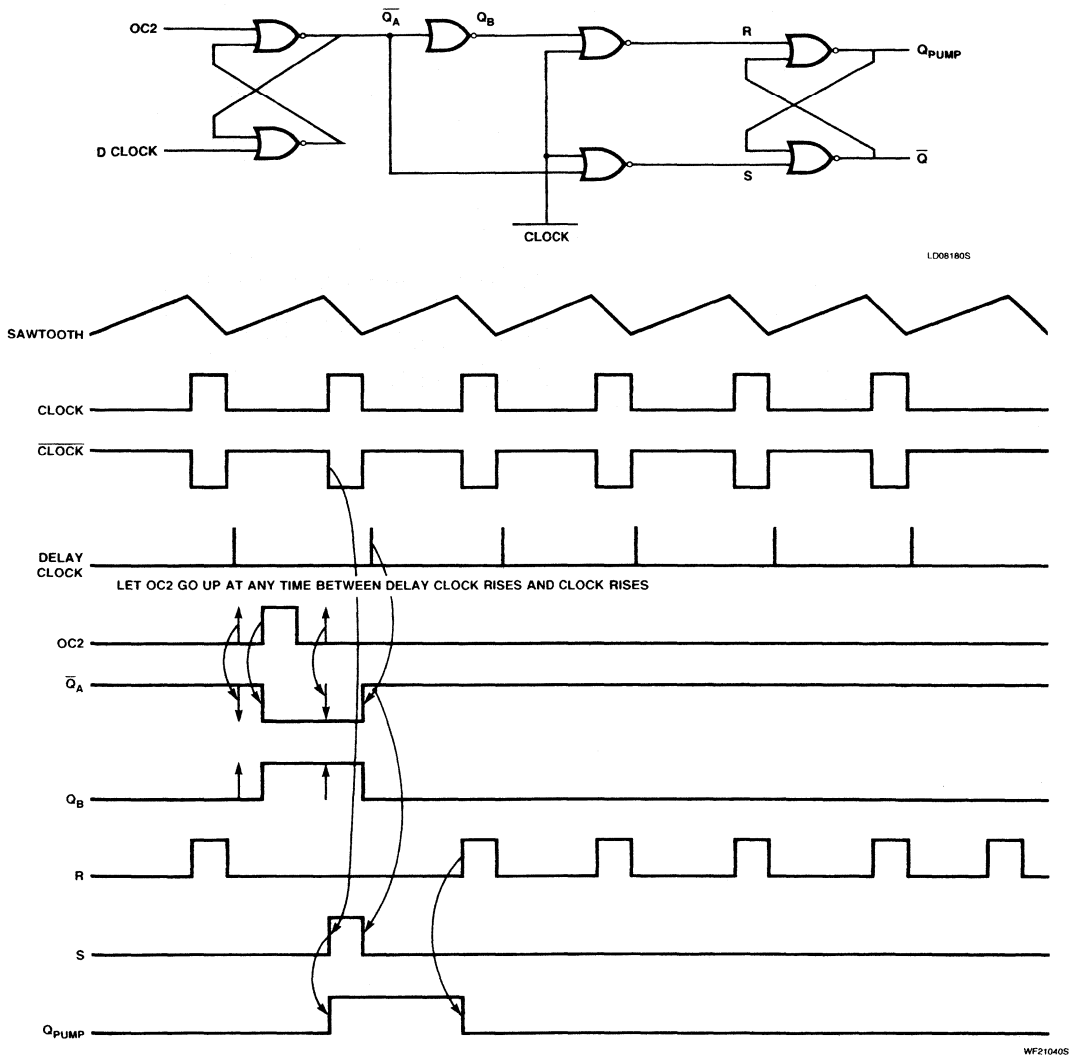
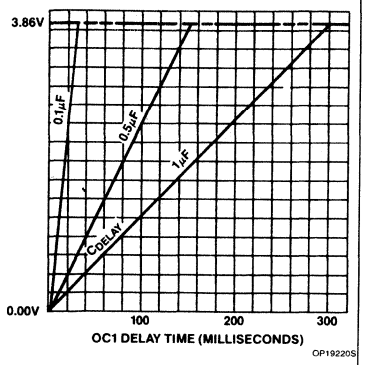


Figure 30. OC2 Fault Cycle



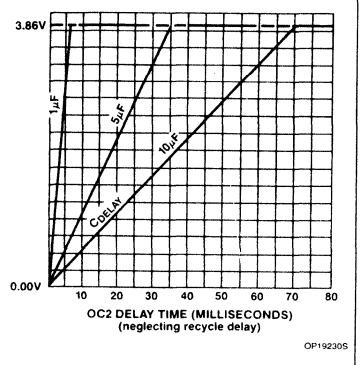


Figure 31. Overcurrent Shutdown Function

CALCULATING THE DELAY CAPACITOR

Actual delay time for a given capacitor value at Pin 16 may be estimated using the graphs in Figure 31 for OC1 and OC2. By first determining the allowable overcurrent time product for a particular power converter, a capacitor delay value may be calculated.

Note that the OC1 charge pump is typically 13μA while OC2 pumps 550μA into the capacitor. If the exact value is to be calculated for a particular delay requirement, use the following procedure:

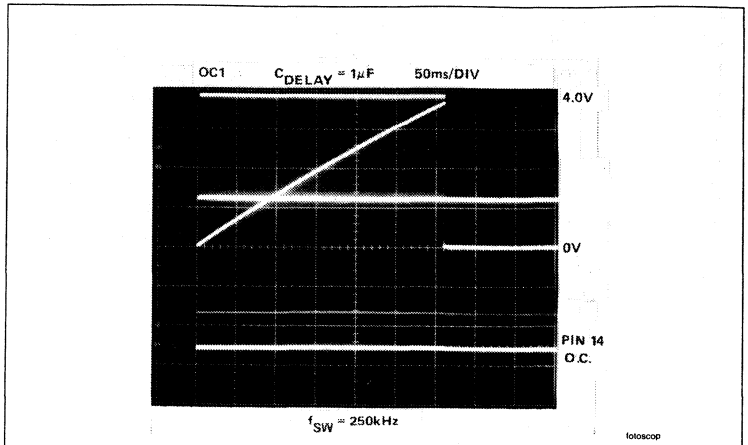


Figure 32. OC1 Ramp and Shutdown Delay

1. Determine the level of overcurrent — OC1 or OC2.
2. Find the maximum delay time which the supply may safely sustain for this continuous overcurrent condition. Note that OC1 may be activated on every cycle if OC2 is not reached, causing continuous charging of C-Delay. However, OC2 overcurrent detection causes the supply to go into slow-start shutdown (hiccup mode), on the first such pulse. OC2 delays are based on an interrupted charging cycle with total cycle time determined by the external slow-start delay capacitor duty cycle maximum divider — time constant.

For a continuous OC1 overcurrent:

$$C_{DLY} = \frac{(13 \times 10^{-6})(\text{Delay time — sec})}{3.86V} \quad (1)$$

For a continuous OC2 overcurrent:

$$C_{DLY} = \frac{(550 \times 10^{-6})(\text{Delay cycles} \times 1 / f_{SW})}{3.86V} \quad (2)$$

Some downward adjustment of the OC2 capacitor value may be necessary to compensate for the 1 – 2μA of discharge current at Pin 16 during the delay cycles.

Example: A maximum of 100 OC2 current fault cycles is allowed.

f_{SW} = 400kHz, find C_{DLY}

$$C_{DLY} = \frac{(550 \times 10^{-6})(100 \times 1/4 \times 105)}{3.86V}$$

$$= 0.036\mu F$$

Example: OC2/C_{DLY}

Find number of OC1 cycles before shutdown with 0.036μF C_{DLY}.

$$\text{Delay Time} = \frac{3.6 \times 10^{-8}F)(3.86V)}{13 \times 10^{-6}A}$$

$$= 10.7ms$$

$$\text{Total cycles to shutdown} = \frac{10.7 \times 10^{-3}}{2.5 \times 10^{-6}}$$

$$= 4280$$

Figure 33 shows an actual OC1 charging cycle for continuous fault current sensed at Pin 14 and a DLY = 1μF.

BULK-SENSE AUXILIARY COMPARATOR WITH SHUTDOWN

This circuit is intended to act as an automatic low-line detection mechanism. As shown in Figure 33, a voltage divider is connected from the main unregulated DC supply to Pin 12. The lower divider resistor may be a potentiometer of 5 – 10kΩ resistance with center-tap connected to Pin 13. The comparator which senses Pin 12 voltage is referenced to 3.80V and Pin 12 divider voltage must be greater than this voltage by a sufficient margin to operate within the prescribed low-line limits. For instance, if a line voltage drop of 25% is considered the shutdown threshold, then V_{12} should be calculated for a nominal operating voltage as shown in Figure 33.

When the line voltage drops more than 25%, the output stage is disabled. With the hysteresis connected as shown and the pot adjusted near midway, the line voltage will have to exceed $V_{NOMINAL}$ before the supply will restart. The hysteresis control may then be calibrated for the desired overexcursion before restart. This prevents unstable circuit chatter.

The reset switch provides a means for resetting the shutdown latch after overcurrent faults have charged C_{DLY} to its trip threshold. This also provides a discharge path for the delay capacitor. Figure 34 shows internal circuit.

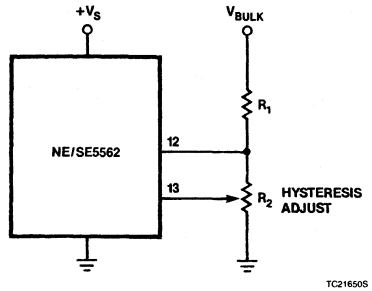


Figure 33. Bulk-Sense Comparator Divider

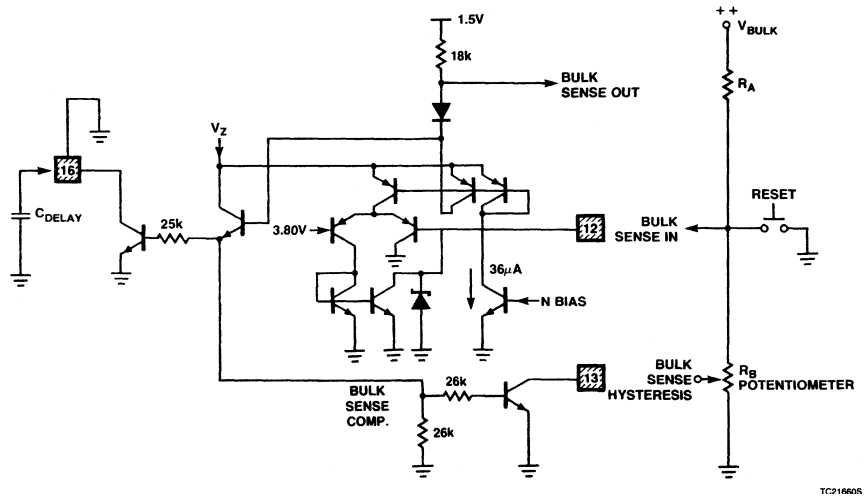


Figure 34. Bulk-Sense Comparator

THE OUTPUT DRIVE STAGE

The output stage contains the power NOR inhibit gate, invert logic function, and source-sink drivers. The driver stage is capable of sourcing and sinking 100mA at frequencies up to 600kHz. The output transistors are Schottky clamped to prevent saturation and the resultant switching delay due to stored charge. A 2.5Ω current sense resistor in the emitter of Q419 serves to drive active clamp Q427 when the output sources more than 200mA. This places a limit on the peak current available during instantaneous charging of a power MOS FET gate. This feature protects the output stage from inadvertent catastrophic overload.

When sinking current, the output is clamped to a maximum of 1.4V. Output swing for positive output is typically $V_S - 1.9V$ at 100mA sourcing. Rise time for a 2000pF load at Pin 19 is typically 160ns with a fall time of 80ns.

The power NOR gate provides a fast response inhibit function to shutdown the output in the event of a number of different fault conditions. All inputs are internal to the device and do not appear directly on the external pins as is shown on Figure 35.

The additional flexibility of an invert control allows the polarity at the output during duty cycle to be reversed. This provides a simple means of designing with P-channel power MOS FETs without adding external inverters. The invert logic is controlled by a simple logic signal at Pin 15. Grounding will cause the output to be a normal positive output and a high level gives inverted output.

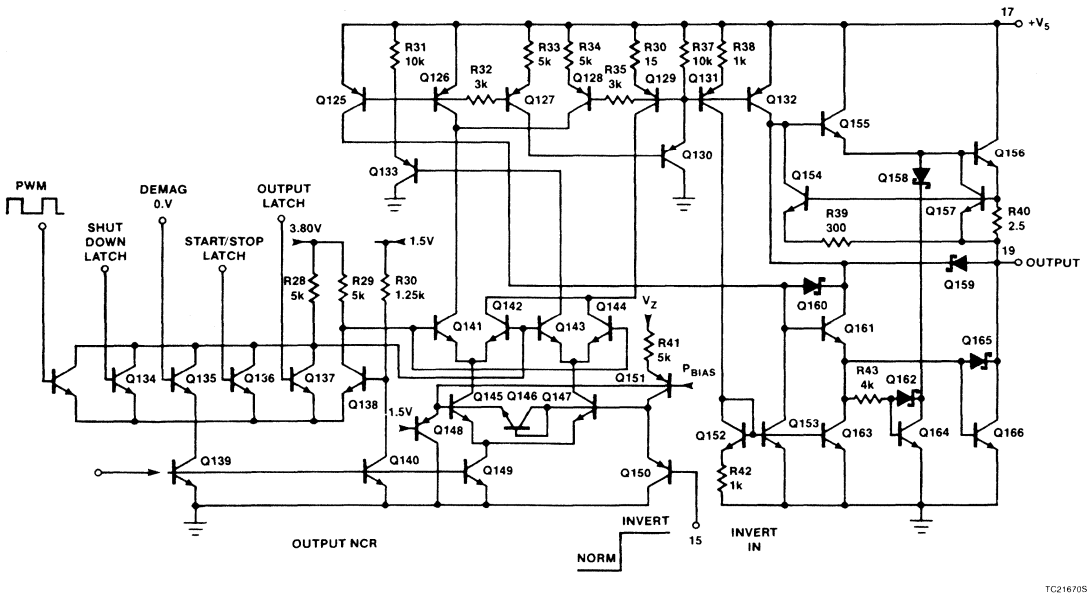


Figure 35. Output Driver Schematic

THE INTERNAL VOLTAGE REGULATOR

The internal regulator is configured to provide for external supply to the NE/SE5562 from either a voltage feed or a current feed.[1]

For the current-fed mode, a series-dropping resistor may be used to power the device from voltages greater than 18V with current supply of 15 to 25mA. Note that supply current stated in the data sheet is for the device only without load on the output or V_Z. Drive currents also are pulse-related and thus reflect frequency components onto the current-feed circuit. These must be filtered out at Pin 7 with adequately large capacitors in order to prevent motor-boating (see Figure 36 and Figure 37).

Input current to Pin 7 flows through Zeners Z_1 and Z_2, and short regulator transmitter QR. A differential amplifier with 3.80V reference provides feedback to regulate V_S to 15V.

In the voltage-fed mode using Pin 17, the Zeners prevent current flow through QR for input voltages less than 19V.

Power dissipation of the device must stay within the allowable package limits. These limits are derived from the thermal characteristics of the particular package chosen. The NE5562N plastic package is capable of operating within the temperature range (ambient) of 0 to +70°C. This rating applies to the surface-mount product NE5562D also. Obviously, the power dissipation of the "D" package is lower than the standard DIP. Thermal resistance for the various packages are:

20-Pin plastic — NE5562N/SE5562N: θ_{JA} 61°C/W

20-Pin glass/ceramic — NE5562F/SE5562F: θ_{JA} 90°C/W

20-Pin SO: −55 to +85°C/W (board-dependent)

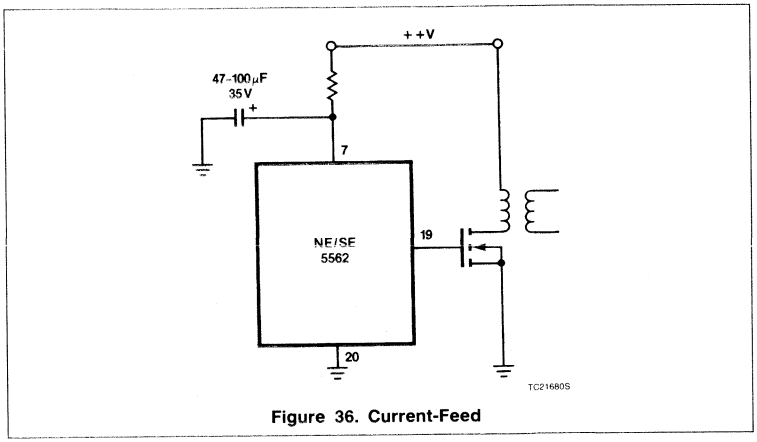


Figure 36. Current-Feed

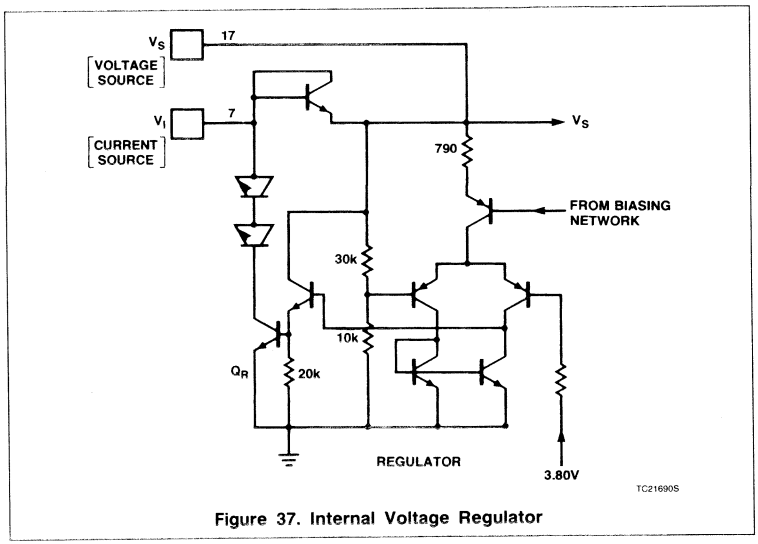


Figure 37. Internal Voltage Regulator

NOTE:
1. See Figures 5 and 6 for Internal Regulator Response Curves.

Design Example — An NE5562N is operated at 40°C ambient in the voltage-fed mode with V_S = 15V; assume I_S = 22mA average:

$$\therefore P_D = (22 \times 10^{-3})(15)$$
$$= 330mW$$

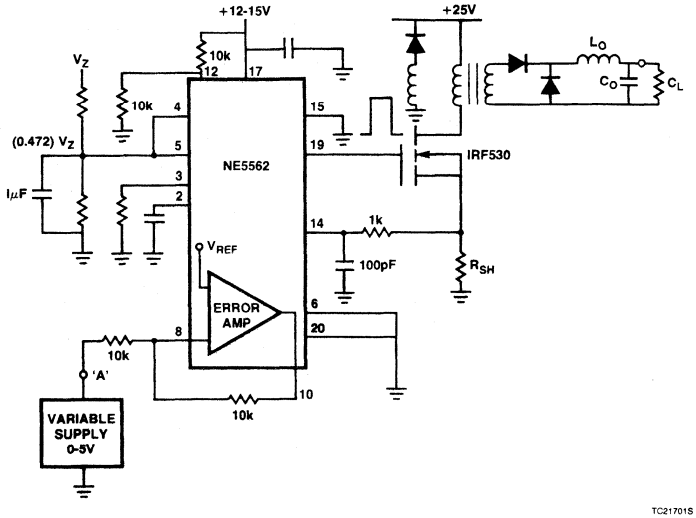
Solving for the temperature rise from ambient to the IC functions:

$$\text{Temperature rise} = 61°C/W \times 0.33W$$
$$= 20.1°C$$

Junction temperatures will be 20.1°C above average ambient temperatures which is 40°C.

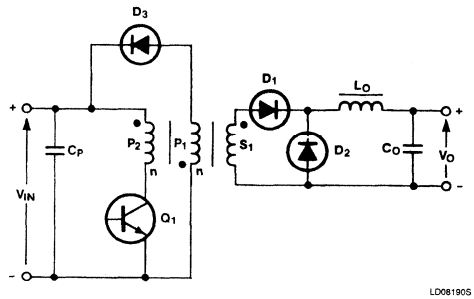
$$T_J = 40°C + 20.1°C = 60.1°C$$

The allowable maximum junction temperature is 150°C. 125°C is more conservative. The conditions of this example are safe.



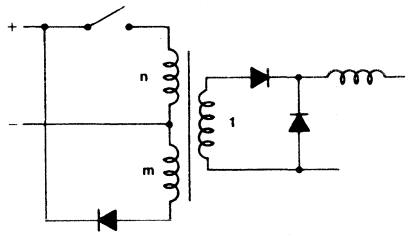
NOTES:
1. Supply will become active as point 'A' reaches the level of V_{REF}, 3.80V.
2. Monitor Pin 19 and Pin 2 on dual-trace scope with voltmeter connected to supply output.

Figure 38. Open-Loop Test Setup



NOTE:
The P_1 clamp winding prevents collector voltage from exceeding 2X V_{IN} during off time.

Figure 39. Forward Converter



To Prevent Core Saturation Due to Flux Staircasing

$$\delta_{max} < 1 - \frac{m}{m+n} \quad \text{if } m = n \; \delta_{max} < .5$$

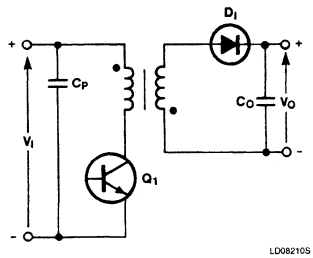
LD08200S

Demagnetization of Core

$$V_{CE\ max} = V_{i\ max} \times \frac{m+n}{m} \quad (V)$$

Maximum Voltage Across Transistor

Figure 40. Forward Converter Design Formulas



LD08210S

Figure 41. Isolated Secondary

Flyback Converter Design

Flyback Converter

Advantages:

- Simple circuit. Only one inductive component even with line isolation.
- Economic. Low component count, low cost.
- Work over large input voltage variations.
- Can accommodate multiple outputs.

Disadvantages:

- Large output ripple current due to discontinuous energy transfer.
- Large output capacitor; has to supply part of the load current.
- Low leakage inductance required to prevent high voltage spikes at the switching transistors.
- Relatively large core volume for the output power. Core driven in one direction only.

Design Parameters for Flyback Inductor

Input

- Minimum input voltage
- Maximum input voltage

Output

- Output voltage or voltages
- Output current or currents
- Output load

Frequency of Operation

Estimate of Overall Efficiency. (η)

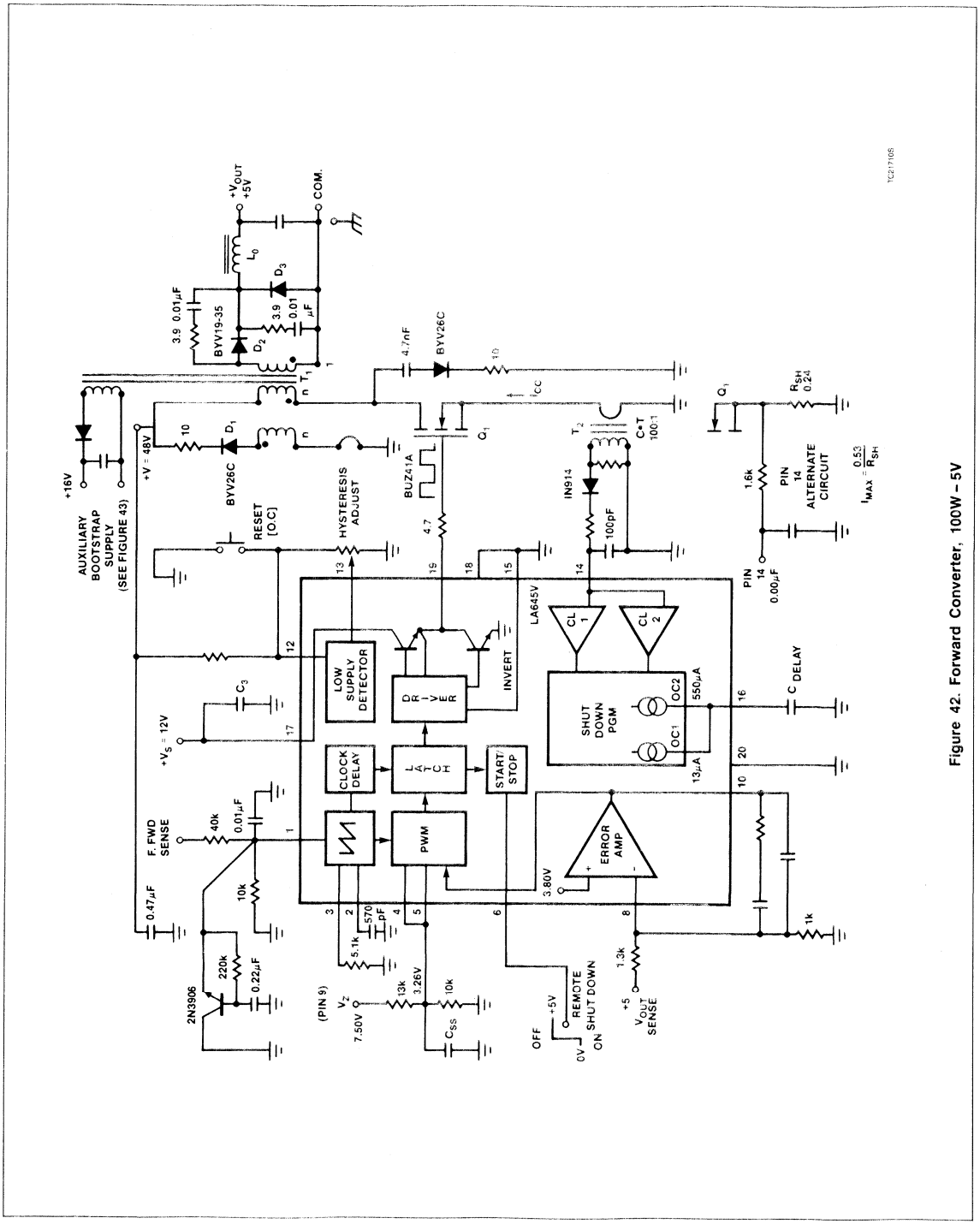


Figure 42. Forward Converter, 100W – 5V

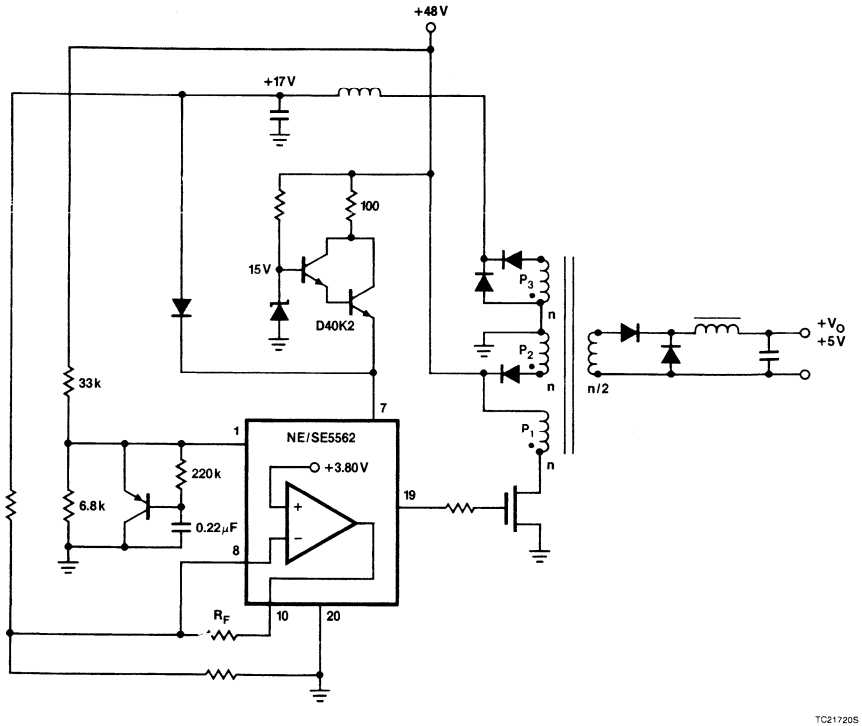
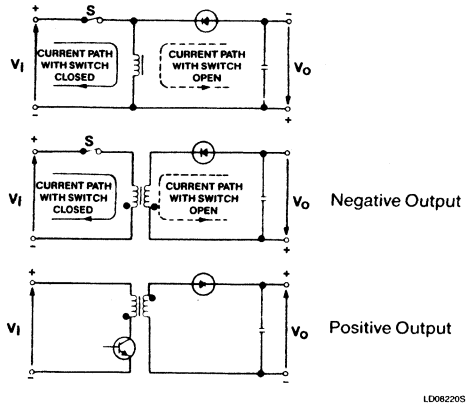
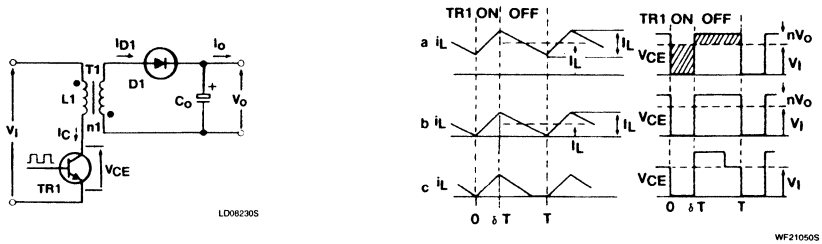


Figure 43. Shunt-Regulated Output With Bootstrap Supply



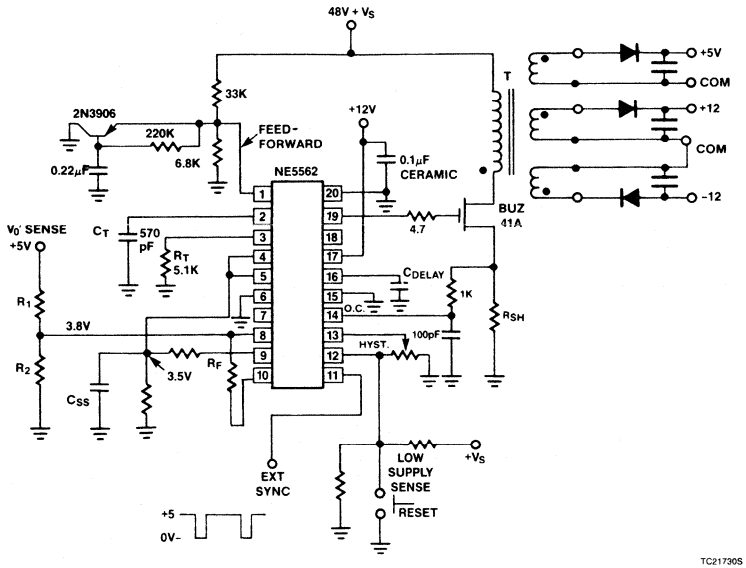
Development of Practical Flyback Converter Circuit



Flyback Converter and Current and Voltage Waveforms

NOTES:
a. Uninterrupted choke current
c. Interrupted choke current

Figure 44



NOTE:
400kHz operation with feed-forward line regulation and cycle-by-cycle current limiting.

Figure 45. NE5562 Flyback Converter

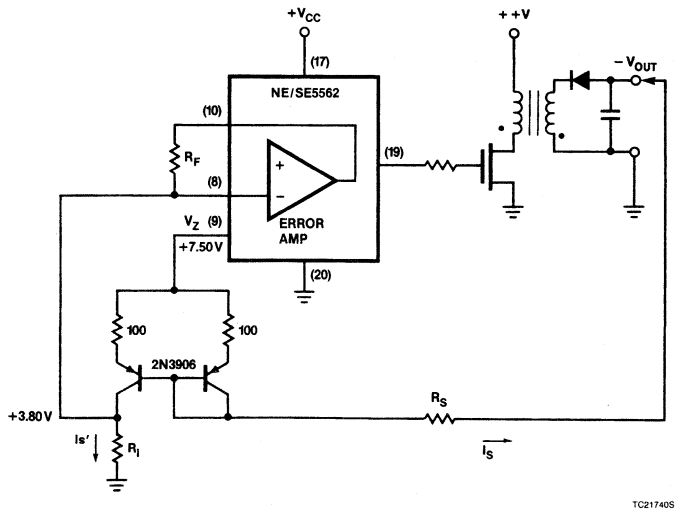


Figure 46. Negative Output Regulator Using Current Mirror

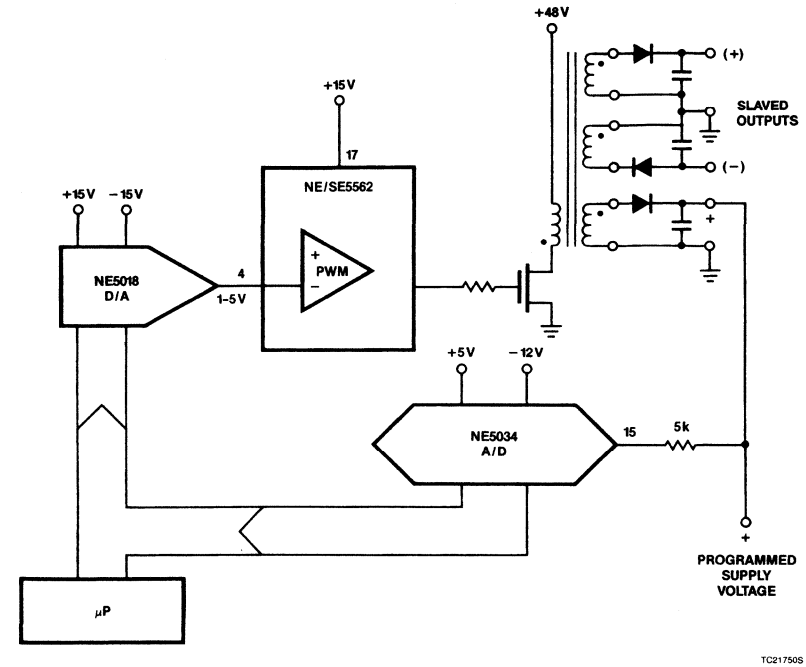


Figure 47. Microprocessor-Controlled SMPS

REFERENCES

1. R.D. Middlebrook and Slobadan Ćuk, *Advances in Switched Mode Power Conversion*, Volumes I and II, TESLA Co., Pasadena, CA, 1983.
2. Rudolf P. Stevens and Gordon E. Bloom, *Modern DC to DC Switchmode Power Convertor Circuits*, Van Nostrand Reinhold/Computer Science and Engineering Series, 1985.
3. H. Dean Venable, *Stability Analysis Made Simple,* Venable Industries, Inc., 1981.
4. J. Jongsma and L.P.M. Bracke, *High Frequency Ferrite Power Transformer and Choke Design*, N. V. Philips ELCOMA Publications, Eindhoven, the Netherlands, September 1982.
5. Edwin S. Oxner, *Power FETs and Their Applications*, Prentice-Hall, 1982.

NE5568
Switched-Mode Power Supply Controller

Product Specification

DESCRIPTION

The NE5568 is a control circuit for use in switched mode power supplies. It contains an internal temperature-compensated supply, PWM, sawtooth oscillator, over-current sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required. The NE5568 is a selected version of the NE5561.

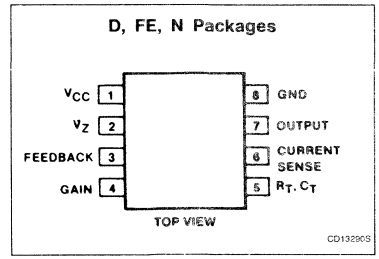
FEATURES

- **Micro-miniature (D) package**
- **Pulse width modulator**
- **Current limiting (cycle by cycle)**
- **Sawtooth generator**
- **Stabilized power supply**
- **Double-pulse protection**
- **Internal temperature-compensated reference**

APPLICATIONS

- **Switch mode power supplies**
- **DC motor controller inverter**
- **DC/DC converter**

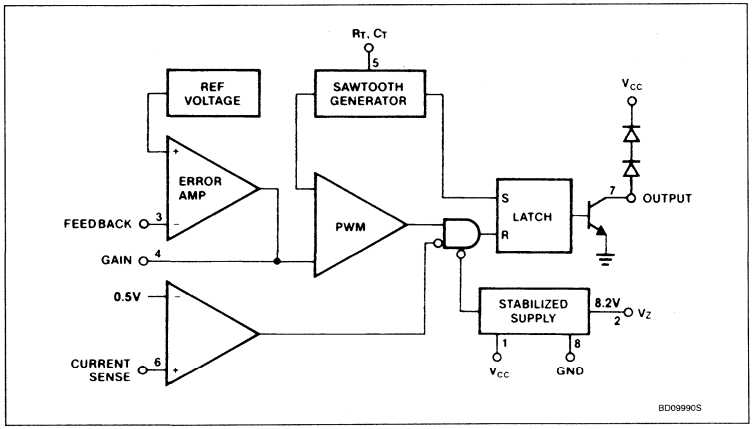
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5568N
8-Pin Cerdip	0 to +70°C	NE5568FE
8-Pin SO package	0 to +70°C	NE5568D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
I_{OUT}	Output current	40	mA
	Output duty cycle	98	%
P_D	Max total power dissipation	0.75	W
T_A	Operating temperature range	0 to 70	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		NE5568 Min	NE5568 Typ	NE5568 Max	UNIT
Reference section							
V_{REF}	Internal reference voltage	T_A = 25°C		3.69	3.75	3.84	V
		Over temperature		3.66		3.87	V
V_Z	Internal zener ref	I_L = 7mA		7.8	8.2	8.8	V
	Temperature coefficient of V_{REF}				± 100		ppm/°C
	Temperature coefficient of V_Z				± 200		ppm/°C
Oscillator section							
f	Frequency range	Over temperature		50		100k	Hz
	Initial accuracy	R_T and C_T Constant			5		%
	Duty cycle range	f_o = 20kHz		0		98	%
Current limiting							
I_{IN}	Input current	Pin 6 = 250mV	T_A = 25°C		−2	−10	μA
			Over temp.			−20	μA
	Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	I_{OUT} = 20mA		0.88	1.10	μs
			I_{OUT} = 40mA		0.7	0.8	μs
	Current limit trip level			0.400	0.500	0.600	V
Error amplifier							
	Open-loop gain				60		dB
	Feedback resistor			10k			Ω
BW	Small-signal bandwidth				3		MHz
V_{OH}	Output voltage swing			6.2			V
V_{OL}	Output voltage swing					0.7	V
Output stage							
I_{OUT}	Output current	Over temperature		20			mA
V_{CE}	Saturation	I_C = 20mA, over temperature				0.4	V
		I_C = 40mA, over temperature				0.5	V
Supply voltage/current							
I_{CC}	Supply current	I_Z = 0, voltage-fed	T_A = 25°C			10.0	mA
			Over temp.			13.0	mA
V_{CC}	Supply voltage	I_S=10mA, current-fed		19.0	21.0	24.0	V
		I_{CC} = 30mA, current-fed		20.0		30.0	V
Low supply protection							
	Pin 1 threshold			8.0	9.0	10.5	V

NOTE:
All curves and applications of NE5561 apply exactly.

μA723/723C/SA723C
Precision Voltage Regulator

Product Specification

DESCRIPTION

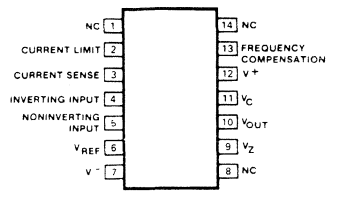
The μA723/SA723C is a monolithic precision voltage regulator capable of operation in positive or negative supplies as a series, shunt, switching, or floating regulator. The 723 contains a temperature-compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

FEATURES

- **Positive or negative supply operation**
- **Series, shunt, switching, or floating operation**
- **0.01% line and load regulation**
- **Output voltage adjustable from 2V to 37V**
- **Output current to 150mA without external pass transistor**
- **μA723 MIL-STD-883A, B, C available**

PIN CONFIGURATION

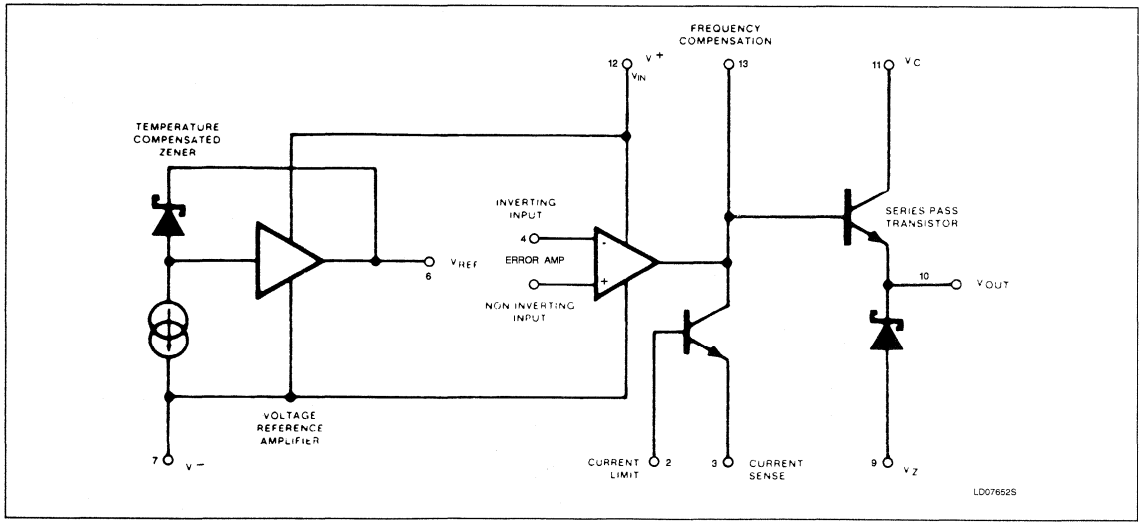
D, F, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Ceramic DIP	−55°C to +125°C	μA723F
14-Pin Plastic DIP	−55°C to +125°C	μA723N
14-Pin Plastic DIP	−40°C to +85°C	SA723CN
14-Pin Ceramic DIP	0 to 70°C	μA723CF
14-Pin Plastic DIP	0 to 70°C	μA723CN
14-Pin Plastic SO	0 to 70°C	μA723CD

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Pulse voltage from V+ to V– (50ms)	50	V
	Continuous voltage from V+ to V–	40	V
	Input-output voltage differential	40	V
V_{DIFF}	Error amplifier maximum input differential voltage	±5	V
V_{CM}	Error amplifier non-inverting input (Pin 5) to –V (Pin 7)	8	V
I_{OUT}	Maximum output current	150	mA
	Current from V_{REF}	15	mA
	Current from V_Z	25	mA
P_{MAX}	Maximum power dissipation $T_A = 25°C$ (still-air)[1] F package N package D package	 1190 1420 1040	 mW mW mW
T_A	Operating ambient temperature range μA723 μA723C SA723C	 –55 to +125 0 to 70 –40 to +85	 °C °C °C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. The following derating factors should be applied above 25°C:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, unless otherwise specified.[1]

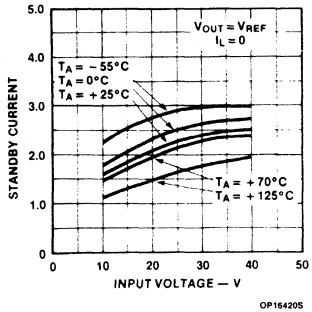
SYMBOL	PARAMETER	TEST CONDITIONS	μA723			μA723C/SA723C			UNIT
			Min	Typ	Max	Min	Typ	Max	
$V_{R\ LINE}$	Line regulation[2]	V_{IN} = 12V to V_{IN} = 15V V_{IN} = 12V to V_{IN} = 40V		0.01 0.02	0.1 0.2		0.01 0.1	0.1 0.5	%V_{OUT} %V_{OUT}
$V_{R\ LOAD}$	Load regulation[2]	I_L = 1mA to I_L = 50mA		0.03	0.15		0.03	0.2	%V_{OUT}
ΔVIN/Δ VO	Ripple Rejection	f = 50Hz to 10kHz, C_{REF} = 0		74			74		dB
		f = 50Hz to 10kHz, C_{REF} = 5μF		86			86		dB
I_{OS}	Short-circuit current	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
V_{REF}	Reference voltage	I_{REF} = 0.1mA	6.95	7.15	7.35	6.80	7.15	7.50	V
$V_{REF\ (LOAD)}$	Reference voltage change with load	I_{REF} = 0.1mA to 5mA			20			20	mV
V_{NOISE}	Output noise voltage	BW = 100Hz to 10kHz, C_{REF} = 0 BW = 100Hz to 10kHz, C_{REF} = 5μF		20 2.5			20 2.5		μV_{RMS} μV_{RMS}
S	Long-term stability	Tj = Tjmax. TA = 25°C for end point measurment		0.1			0.1		%1000 hrs.
I_{SCD}	Standby current drain	I_L = 0, V_{IN} = 30V		2.3	3.5		2.3	4.0	mA
V_{IN}	Input voltage range		9.5		40	9.5		40	V
V_{OUT}	Output voltage range		2.0		37	2.0		37	V
V_{DIFF}	Input-output voltage differential		3.0		38	3.0		38	V
The following specifications apply over the operating temperature ranges.									
$V_{R\ LINE}$	Line regulation	V_{IN} = 12V to V_{IN} = 15V			0.3			0.3	%V_{OUT}
$V_{R\ LOAD}$	Load regulation	I_L = 1mA to I_L = 50mA			0.6			0.6	%V_{OUT}
TC	Average temperature coefficient of output voltage			0.002	0.015		0.003	0.015	%/°C

NOTES:

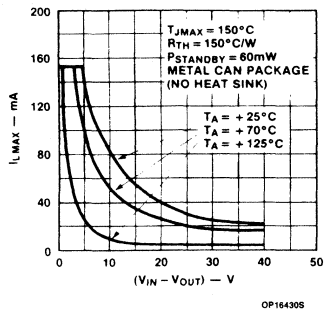
1. V_{IN} = V+ = V_C = 12V, V– = 0V, V_{OUT} = 5V, I_L = 1mA, R_{SC} = 0, C_1 = 100pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10kΩ.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

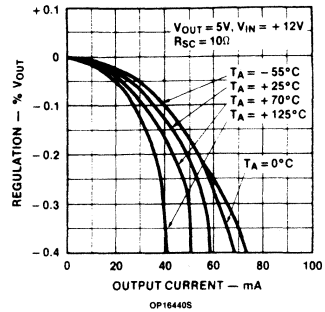
Standby Current Drain as a Function of Input Voltage



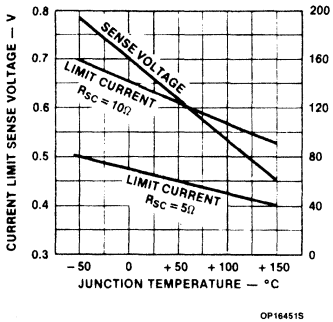
Maximum Load Current as a Function of Input-Output Voltage Differential



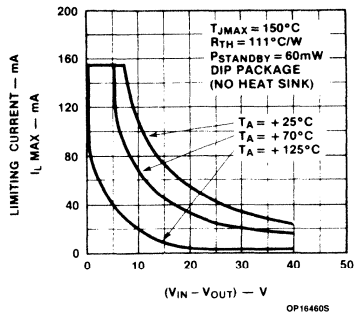
Load Regulation Characteristics with Current Limiting



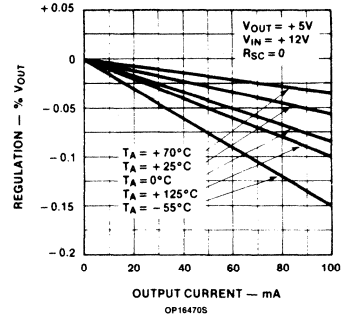
Current Limiting Characteristics as a Function of Junction Temperature



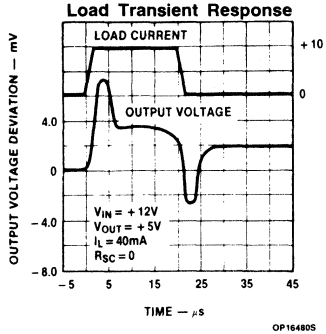
Maximum Load Current as a Function of Input-Output Voltage Differential



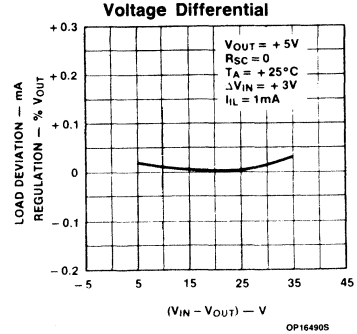
Load Regulation Characteristics Without Current Limiting



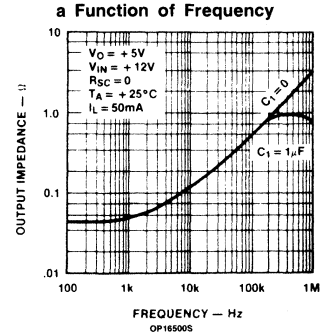
Load Transient Response



Line Regulation as a Function of Input-Output Voltage Differential

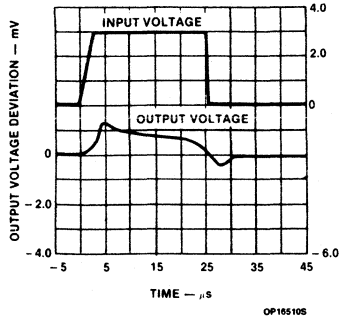


Output Impedance as a Function of Frequency

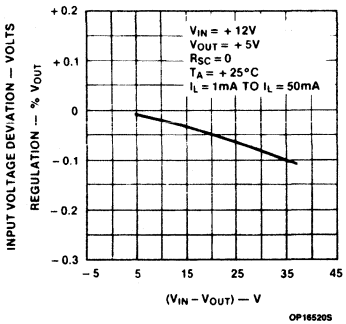


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

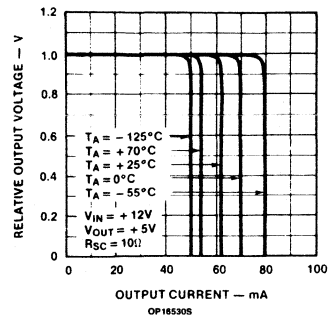
Line Transient Response



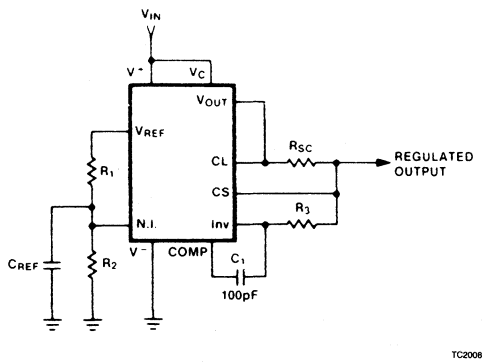
Load Regulation as a Function of Input-Output Voltage Differential



Current Limiting Characteristics



TYPICAL APPLICATIONS

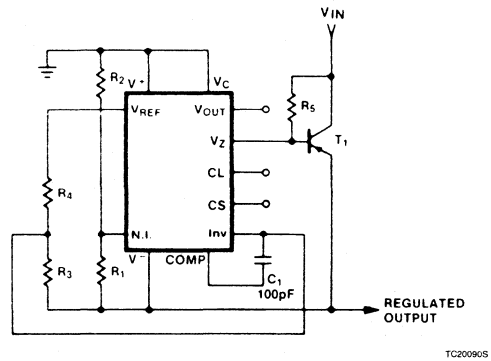


NOTES:

$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$

$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift

Low Voltage Regulator (V_{OUT} = 2 to 7V)

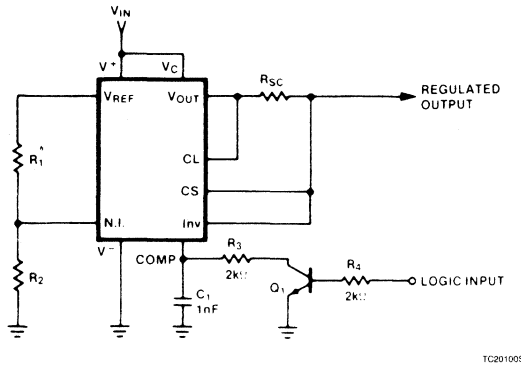


NOTE:

$V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}\right]$; $R_3 = R_4$

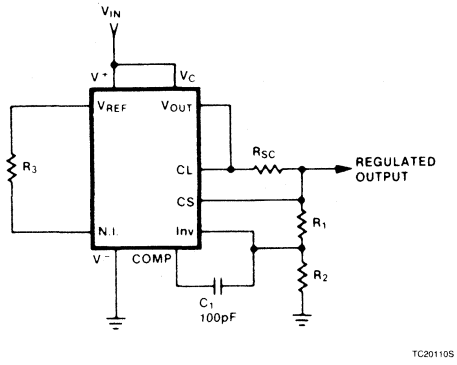
Negative Voltage Regulator

TYPICAL APPLICATIONS (Continued)



NOTE:

$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$



NOTES:

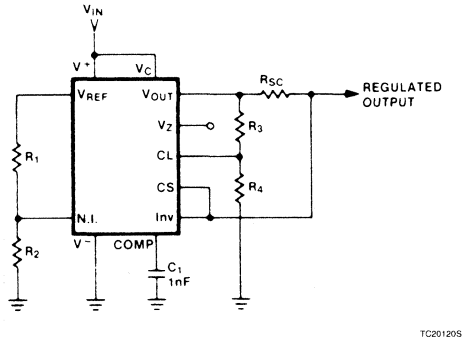
$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]; \; R_3 = R_4$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$ for minimum temperature drift

R_3 may be eliminated for minimum component count

Remote Shutdown Regulator With Current Limiting (V_{OUT} = 2 to 7V)

High Voltage Regulator (V_{OUT} = 7 to 37V)

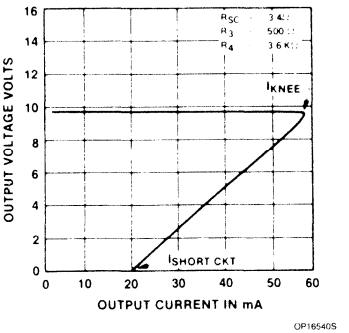


NOTES:

$$I_{KNEE} = \left[\frac{V_{OUT} R_3}{R_{SC}\, R_4} + \frac{V_{SENSE}\,(R_3 + R_4)}{R_{SC} R_4}\right]$$

$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

$$I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}\right]$$



NOTES:

$$\frac{R_4}{R_3} = \frac{V_{OUT}\; I_{SC}}{V_{SENSE}(I_{KNEE} - I_{SHORT\ CKT})} - 1$$

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}}\left[1 + \frac{R_3}{R_4}\right]$$

Foldback Current Limiting Regulator (V_{OUT} = 2 to 7V)

SG1524C/2524C/3524C
Switched-Mode Power Supply Control Circuits

Preliminary Specification

DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual in-line package is the voltage reference, error amplifier, oscillator, pulse-width modulator, pulse steering flip-flop, dual alternating output switches and current-limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer-coupled DC-to-DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications.

FEATURES

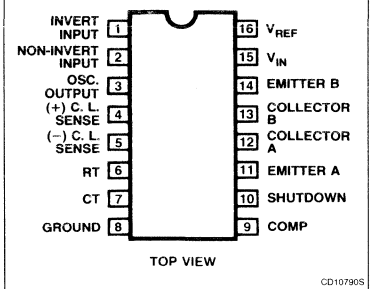
- **Fully interchangeable with standard SG1524 family**
- **Precision reference internally trimmed to within 1% and guaranteed**
- **High-speed current limit function**
- **Low supply protection with hysteresis**
- **200mA of output current**
- **60V output capability**
- **Wide common-mode input range for both error amp and current limit comparator**
- **Very good CMRR & PSRR for both error amp and current limit comparator**
- **Superior logic design using ECL circuits for glitch-free high-speed operation and fault protection**

APPLICATIONS

- **Switched-mode power supplies**
- **Motor control circuitry**

PIN CONFIGURATION

D[1], F, N Packages



TOP VIEW

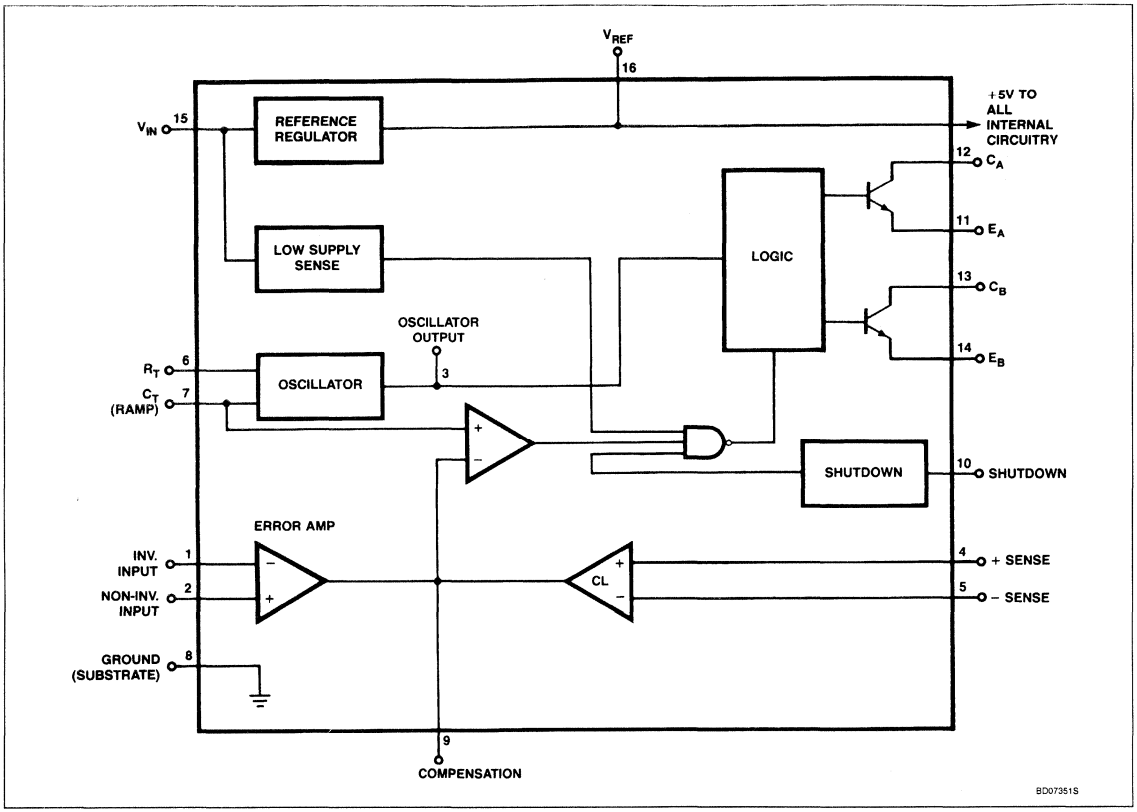
CD10790S

NOTE:
1. Available in large SO (SOL) package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	SG3524CN
16-Pin Ceramic DIP	0 to +70°C	SG3524CF
16-Pin Plastic SOL	0 to +70°C	SG3524CD
16-Pin Plastic DIP	−40°C to +85°C	SG2524CN
16-Pin Ceramic DIP	−40°C to +85°C	SG2524CF
16-Pin Plastic SOL	−40°C to +85°C	SG2524CD
16-Pin Plastic DIP	−55°C to +125°C	SG1524CN
16-Pin Ceramic DIP	−55°C to +125°C	SG1524CF

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{IN}	Supply voltage	40	V
V_C	Collector supply voltage	60	V
I_O	Output current (each output)	250	mA
I_{REF}	Reference output current[1]	50	mA
V_{REF}	Externally forced reference voltage	5.5	V
	Error amp inputs	$V_{IN}-3$	V
	Error amp max diff. voltage[2]	0.5	V
	Oscillator charging current	5	mA
	Current limit sense inputs	V_{IN}	V
	Current limit max. diff. voltage	40	V
	Shutdown inputs	5.5	V
P_D	Maximum power dissipation $T_A = 25°C$ (still-air)[3, 4] F package N package D package	 1190 1450 1090	 mW mW mW
T_J	Operating junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Short-circuit protected.
2. Inputs are clamped by two diodes. Resistors should be used to limit input current to less than 1mA maximum.
3. $P_D = I_{SB}V_{IN} + 2$ duty cycle (I_{OUT} $V_{CE\ ON}$) + I_{REF} ($V_{IN} - 5V$) + $2I_{CT}$ ($V_{IN} - 3.6$).
4. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.6mW/°C
   D package at 8.7mW/°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{IN}	Supply voltage	7 to 40	V
V_C	Collector supply voltage (with emitters grounded)	0 to 60	V
I_O	Output current (each output) ($V_{CE} < 2.5V$)	0 to 200	mA
I_{REF}	Reference load current	0 to 20	mA
V_{CM}	Error amp common-mode input	1.5 to ($V_{IN} - 4$)	V
V_{CM}	Current limit amp common-mode input	0 to ($V_{IN} - 4$)	V
	Oscillator charging current	0.02 to 2	mA
R_T	Oscillator timing resistor	2 to 150	kΩ
T_A	Operating ambient temperature range		
	SG1524C	−55 to 125	°C
	SG2524C	−40 to 85	°C
	SG3524C	0 to 70	°C
T_J	Operating junction temperature range		
	SG1524C	−55 to 150	°C
	SG2524C	−40 to 125	°C
	SG3524C	0 to 125	°C
C_T	Oscillator timing capacitor	0.47 to 100	nF
f_{OSC}	Oscillator frequency	0.1 to 400	kHz

DC AND AC ELECTRICAL CHARACTERISTICS Minimum and maximum limits apply over recommended operating junction temperature range, typical data applies at $T_J = 25°C$, and $V_{IN} = V_C = 20V$, $R_T = 2.7k\Omega$, $C_T = 0.01\mu F$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SG1524C/2524C			SG3524C			UNIT
			Min	Typ	Max	Min	Typ	Max	
Turn-on characteristics									
V_{IN}	Input minimum voltage	After turn-on	7		40	7		40	V
	Turn-on input voltage		4.9	6	6.5	4.9	6	6.5	V
	Input voltage hysteresis		100	240	360	100	240	360	mV
V_{REF}	Turn-on reference voltage		4.3	4.60	4.8	4.3	4.60	4.8	V
	Reference voltage hysteresis		100	240	360	100	240	360	mV
Reference section[1]									
V_{OUT}	Output voltage	Over temperature	4.9		5.1	4.9		5.1	V
V_{OUT}	Output voltage	$T_J = 25°C$	4.95	5.00	5.05	4.915	5.00	5.105	V
	Temperature stability			15	50		15	50	mV
	Line regulation	$V_{IN} = 7$ to 40V		1.0	15		1.0	15	mV
	Load regulation	$I_L = 0$ to 20mA		10	20		10	20	mV
	Total output variation	$7V < V_{IN} < 40V$, $0mA < I_L < 20mA$	4.90	5.0	5.10	4.90	5.0	5.10	V
I_{OUT}	Maximum output current	$V_{REF} = 0V$	−120	−60	−25	−120	−60	−25	mA
	Output noise voltage	$10Hz < f < 10kHz$, $T_A = 25°C$		170			170		μV_{RMS}
	Long-term stability	$T_A = 25°C$, 1khrs		20			20		mV
RR	Ripple rejection	$T_A = 25°C$, f = 2400Hz		60			60		dB
Oscillator section									
	Initial frequency		38	41	44	38	41	44	kHz
	Frequency temp. stability				2			2	%
	Voltage stability	$V_{IN} = 7$ to 40V		0.5	1.0		0.5	1.0	%
	Sawtooth peak voltage	$V_{IN} = 40V$	3.2	3.5	3.8	3.2	3.5	3.8	V
	Sawtooth valley voltage	$V_{IN} = 7V$	0.5	.75	1.0	0.5	.75	1.0	V
	Clock amplitude		2.85	3.4		2.85	3.4		V
	Clock pulse width	Measured level = 2.0V	.25	0.5	.75	.25	0.5	.75	μs
f_{MIN}	Minimum frequency	$R_T = 150k\Omega$, $C_T = 0.1\mu F$		100			100		Hz
f_{MAX}	Maximum frequency	$R_T = 2k\Omega$, $C_T = 470pF$, $T_J = 25°C$		550			550		kHz
f_{MAX}	Maximum frequency	$R_T = 2k\Omega$, $C_T = 470pF$	400			400			kHz
f_{MAX}	Maximum frequency	$R_T = 2k\Omega$, $C_T = 1nF$	290			290			kHz
	Current mirror	$I_{RT} = -2mA$[4]	−2.0	−1.86	−1.7	−2.0	−1.86	−1.7	mA
	Saturation voltage	$I_{CT} = 5mA$, $V_P3 = 5V$	.55	0.72	1.0	.55	0.72	1.0	V

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) Minimum and maximum limits apply over recommended operating junction temperature range, typical data applies at $T_J = 25°C$, and $V_{IN} = V_C = 20V$, $R_T = 2.7k\Omega$, $C_T = 0.01\mu F$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SG1524C/2524C			SG3524C			UNIT
			Min	Typ	Max	Min	Typ	Max	
Error amplifier section[2]									
V_{OS}	Input offset voltage	$R_S = 2k\Omega$		1.0	5.0		1.0	10	mV
I_{BIAS}	Input bias current	$R_S = 1k\Omega$		1.0	5.0		1.0	10	μA
I_{OS}	Input offset current	$R_S = 1k\Omega$		0.04	1.0		0.04	1.0	μA
CMRR	Common-mode rejection ratio	$V_{CM} = 1.5$ to 12.5V	75	85		75	85		dB
PSRR	Supply voltage rejection ratio	$V_{IN} = 7$ to 40V	80	93		80	93		dB
	DC open-loop gain	$C_L = 0.01\mu F$ $V_9 = 1$ to 4V	60	79		60	79		dB
	Gain bandwidth product	$T_A = 25°C$, $A_V = 0B$	2	5		2	5		MHz
	Output low level	$I_{SINK} = 100\mu A$, $V_{CC1}1 - V_{CC2} > 0.15V$		0.3	0.5		0.3	0.5	V
	Output high level	$I_{SOURCE} = 100\mu A$, $V_2 - V_1 > 0.15V$	5.0	5.6	6.0	5.0	5.6	6.0	V
	Output sink current	$V_1 - V_2 > 0.15V$, $V_9 = 2.5V$	100	136	170	100	136	170	μA
	Output source current	$V_2 - V_1 > 0.15V$, $V_9 = 2.5V$	−170	−140	−100	−170	−140	−100	μA
PWM comparator section									
	Minimum duty cycle	$V_2 = 0.5V$, $V_9 = V_1$			0			0	%
	Maximum duty cycle	$V_2 = 3.9V$, $V_9 = V_1$	45	48.7	50	45	48.7	50	%
	Duty cycle for max. freq.	$V_2 - V_1 > 0.15V$, Rt = 2kΩ, $C_T = 470pF$	32		42	32		42	%
I_{BIAS}	Input bias current	$I_{RT} = 0mA$, $V_2 = 2.5V$, $V_9 = V_1$	−5.0		0	−5.0		0	μA
	Propagation delay to output			0.5			0.5		μs
Current-limiting section[2]									
	Sense voltage		180		220	170		230	mV
I_{BIAS}	Input bias current	$R_S = 10k\Omega$, $V_2 - V_1 > 0.15V$	−5		0	−5		0	μA
CMRR	Common-mode rejection ratio	$V_{CM} = 0$ to 12.5V	50	90		50	90		dB
PSRR	Power supply rejection ratio	$V_{IN} = 7$ to 40V	50	90		50	90		dB
V_{OL}	Output low voltage	$V_2 - V_1 > 0.15V$, $V_4 - V_5 > 0.3V$	0	0.28	0.2	0	0.28	0.2	V
t_{PD}	Propagation delay to output			0.7			0.7		μs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

Minimum and maximum limits apply over recommended operating junction temperature range, typical data applies at T_J = 25°C, and V_{IN} = V_C = 20V, R_T = 2.7kΩ, C_T = 0.01μF, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SG1524C/2524C			SG3524C			UNIT
			Min	Typ	Max	Min	Typ	Max	
Shutdown input									
I_{BIAS}	Input bias current	T_J = 25°C, V_{10} = 1V	10		200	10		200	μA
	Shutdown threshold voltage	T_J = 25°C	0.6	0.8	1.0	0.6	0.8	1.0	V
	Shutdown threshold voltage		0.4		1.3	0.4		1.3	V
t_{PD}	Propagation delay to outputs			0.5			0.5		μs
Output section (each output)									
V_{CE}	Collector emitter voltage	I_C = 100μA	60	75		50	75		V
	Collector leakage current	V_{CE} = 60V, V_{10} = 1.5V		0.1	20		0.1	20	μA
	Collector saturation voltage	I_C = 20mA		0.2	0.4		0.2	0.4	V
	Collector saturation voltage	I_C = 200mA		1.2	2.0		1.2	2.0	V
	Emitter output voltage	I_E = 20mA	17.5	18		17.5	18		V
	Emitter output voltage	I_E = 200mA	16.5	17.5		16.5	17.5		V
t_R	Collector rise time Emitter rise time	T_A = 25°C, I_C = I_E = 10mA, C_L = 15pF		0.5 0.1	0.6 0.2		0.5 0.1	0.6 0.2	μs μs
t_F	Collector fall time Emitter fall time	T_A = 25°C, I_C = I_E = 10mA, C_L = 15pF		0.1 0.1	0.2 0.2		0.1 0.1	0.2 0.2	μs μs
Total supply current[3]									
I_{SB}	Standby supply current	V_{IN} = 40V, I_{RT} = 0mA, V_{10} = 1.5V		9.0	11.0		9.0	11.0	mA
I_{CC}	Operating supply current	V_{IN} = 40V, I_C = I_E = 10mA		11	15		11	15	mA

NOTES:
1. Unless otherwise specified, I_L = 0mA.
2. Unless otherwise specified, V_{CM} = 2.5V.
3. Unless otherwise specified, I_{REF} = 0mA.
4. I_{RT} is the current into Pin 6.

SG3524
SMPS Control Circuit

Product Specification

DESCRIPTION

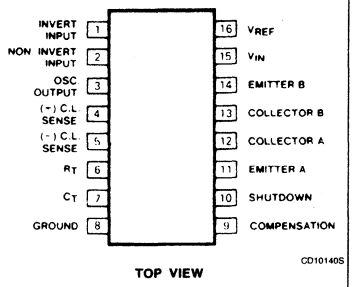
This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse-width modulator, pulse steering flip-flop, dual alternating output switches and current-limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer-coupled DC-to-DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG3524 is designed for commercial applications of 0°C to +70°C.

FEATURES

- **Complete PWM power control circuitry**
- **Single ended or push-pull outputs**
- **Line and load regulation of 0.2%**
- **1% maximum temperature variation**
- **Total supply current is less than 10mA**
- **Operation beyond 100kHz**

PIN CONFIGURATION

D, F, N Packages

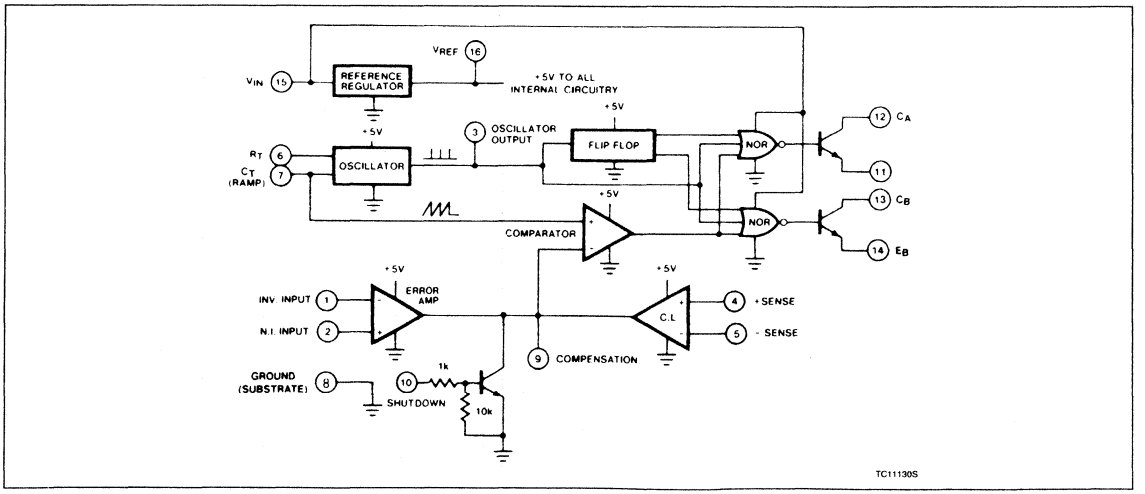


TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	SG3524N
16-Pin Cerdip	0 to +70°C	SG3524F
16-Pin SO	0 to +70°C	SG3524D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{IN}	Input voltage	40	V
I_{OUT}	Output current (each output)	100	mA
I_{REF}	Reference output current	50	mA
	Oscillator charging current	5	mA
P_D	Power dissipation Package limitation Derate above 25°C	 1000 8	 mW mW/°C
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{IN} = 20V, and f = 20kHz, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Reference section						
V_{OUT}	Output voltage		4.6	5.0	5.4	V
	Line regulation	V_{IN} = 8 to 40V		10	30	mV
	Load regulation	I_L = 0 to 20mA		20	50	mV
	Ripple rejection	f = 120Hz, T_A = 25°C		66		dB
I_{SC}	Short circuit current limit	V_{REF} = 0, T_A = 25°C		100		mA
	Temperature stability	Over operating temperature range		0.3	1	%
	Long-term stability	T_A = 25°C		20		mV/kHz
Oscillator section						
f_{MAX}	Maximum frequency	C_T = 0.001 mF, R_T = 2kΩ		300		kHz
	Initial accuracy	R_T and C_T constant		5		%
	Voltage stability	V_{IN} = 8 to 40V, T_A = 25°C			1	%
	Temperature stability	Over operating temperature range			2	%
	Output amplitude	Pin 3, T_A = 25°C		3.5		V_P
	Output pulse width	C_T = 0.01 mF, T_A = 25°C		0.5		μs
Error amplifier section						
V_{OS}	Input offset voltage	V_{CM} = 2.5V		2	10	mV
I_{BIAS}	Input bias current	V_{CM} = 2.5V		2	10	μA
	Open-loop voltage gain		68	80		dB
V_{CM}	Common-mode voltage	T_A = 25°C	1.8		3.4	V
CMRR	Common-mode rejection ratio	T_A = 25°C		70		dB
BW	Small-signal bandwidth	A_V = 0dB, T_A = 25°C		3		MHz
V_{OUT}	Output voltage	T_A = 25°C	0.5		3.8	V
Comparator section						
	Duty cycle	% each output "ON"	0		45	%
	Input threshold	Zero duty cycle		1		V
	Input threshold	Maximum duty cycle		3.5		V
I_{BIAS}	Input bias current			1		μA

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 0°C$ to $+70°C$, $V_{IN} = 20V$, and $f = 20kHz$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Current limiting section						
	Sense voltage	Pin 9 = 2V with error amplifier set for maximum out, $T_A = 25°C$	180	200	220	mV
	Sense voltage T.C.			0.2		mV/°C
V_{CM}	Common-mode voltage		−1		+1	V
Output section (each output)						
	Collector-emitter voltage (breakdown)		40			V
	Collector-leakage current	$V_{CE} = 40V$		0.1	50	μA
	Saturation voltage	$I_C = 50mA$		1	2	V
	Emitter output voltage	$V_{IN} = 20V$	17	18		V
t_R	Rise time	$R_C = 2k\Omega$, $T_A = 25°C$		0.2		μs
t_F	Fall time	$R_C = 2k\Omega$, $T_A = 25°C$		0.1		μs
Total standby current						
	(excluding oscillator charging current, error and current limit dividers, and with outputs open)	$V_{IN} = 40V$		8	10	mA

THEORY OF OPERATION

Voltage Reference

An internal series regulator provides a nominal 5V output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5V supply by connecting Pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0V.

This reference regulator may be used as a 5V source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 1.

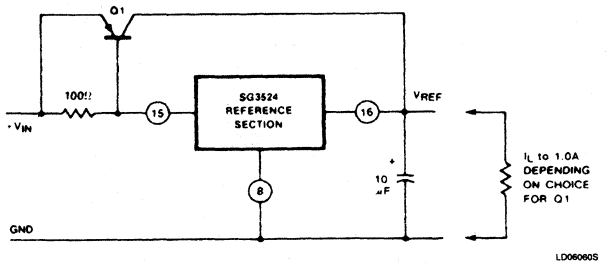
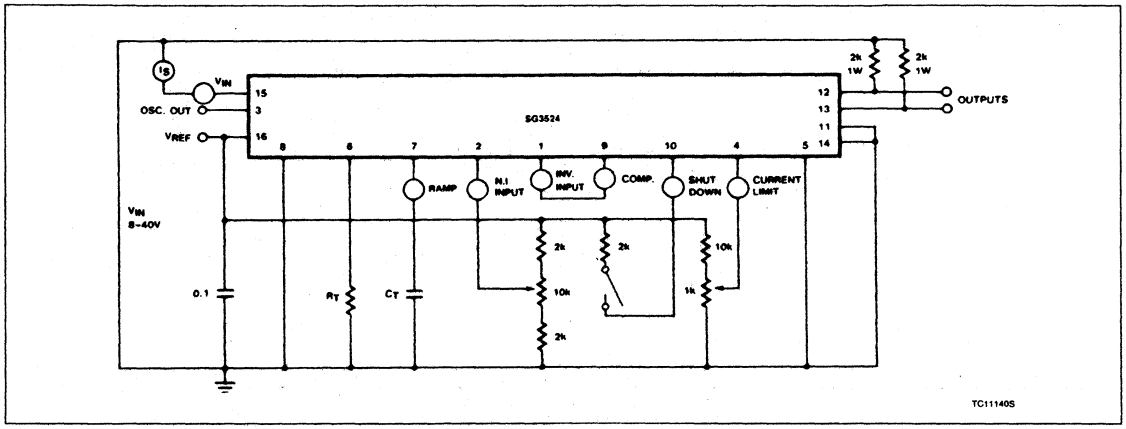


Figure 1. Expanded Reference Current Capability

TEST CIRCUIT



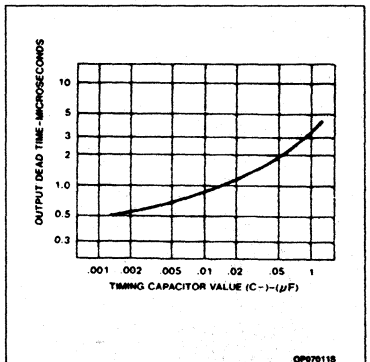


Figure 2. Output Stage Dead Time as a Function of the Timing Capacitor Value

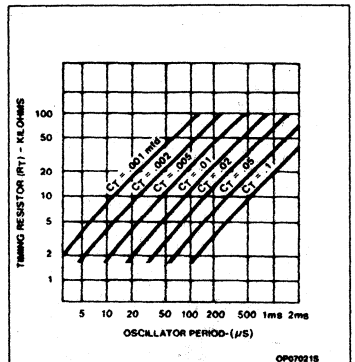


Figure 3. Oscillator Period as a Function of R_T and C_T

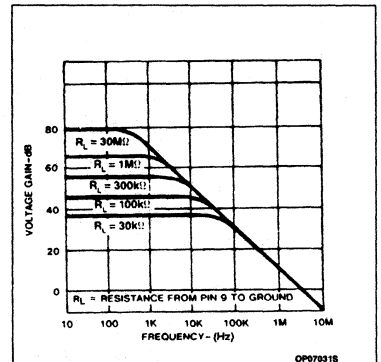


Figure 4. Amplifiers Open-Loop Gain as a Function of Frequency and Loading on Pin 9

Oscillator

The oscillator in the SG3524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series-connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to $3.6V \div R_T$ and should be kept within the approximate range of 30μA to 2mA; i.e., $1.8k < R_T < 100k$.

The range of values for C_T also has limits as the discharge time of C_T determines the

pulse-width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 2. A pulse width below approximately 0.5μs may allow false triggering of one output by removing the blanking pulse prior to the flip-flop's reaching a stable state. If small values of C_T must be used, the pulse-width may still be expanded by adding a shunt capacitance (≈100pF) to ground at the oscillator output. [(Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse-width slightly.)] Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between 0.001 and 0.1 μF.

The oscillator period is approximately $t = R_T C_T$ where t is in microseconds when $R_T = \Omega$ and $C_T = \mu F$. The use of Figure 3 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0 – 90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each output's duty cycle is 0 – 45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the SG3524 to an external clock, a pulse of ≈ + 3V may be applied to the oscillator output terminal with $R_T C_T$ set slightly greater than the clock period. The same considerations of pulse-width apply. The impedance to ground at this point is approximately 2kΩ.

If two or more SG3524s must be synchronized together, one must be designated as master with its $R_T C_T$ set for the correct period. The slaves should each have an $R_T C_T$ set for approximately 10% longer period than the master with the added requirement that C_T(slave) = one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse — which occurs first and has a wider pulse width — will reset the slave units.

Error Amplifier

This circuit is a simple differential input transconductance amplifier. The output is the compensation terminal, Pin 9, which is a high-impedance node ($R_L \approx 5M\Omega$). The gain is

$$A_V = g_M R_L = \frac{8\, I_C\, R_L}{2kT} \cong 0.002\, R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from Pin 9 to ground, as shown in Figure 4.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 4 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain crossover at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series RC combination between Pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus 0.001μF.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground, thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5V reference voltage must be divided down as shown in Figure 5. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open-loop test circuit.

Current Limiting

The current limiting circuitry of the SG3524 is shown in Figure 6.

By matching the base-emitter voltages of Q1 and Q2, and assuming a negligible voltage drop across R_1:

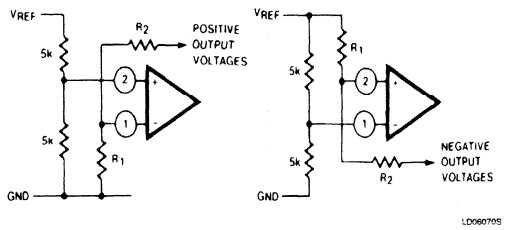
$$\text{Threshold} = V_{BE}(Q1) + I_1 R_2 - V_{BE}(Q2)$$

$$= I_1 R_2 \cong 200\text{mV}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ± 1V common-mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by $R_1 C_1$ and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage required to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, Pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and to shorten an output pulse, should transformer saturation occur. Another application is to ground Pin 5 and use Pin 4 as an additional shutdown terminal: i.e., the output will be off with Pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 7. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).



NOTE:
Note change in input connections for opposite polarity outputs.

Figure 5. Error Amplifier Biasing Circuits

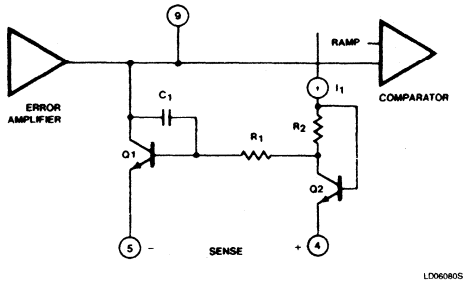
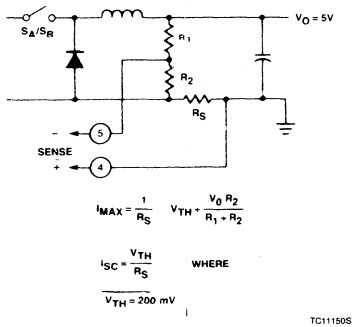


Figure 6. Current Limiting Circuitry of the SG3524



NOTE:
Foldback current limiting can be used to reduce power dissipation under shorted output conditions.

Figure 7. Foldback Current Limiting

SG3526

Switched-Mode Power Supply Control Circuit

Product Specification

DESCRIPTION

Specifically designed for use in fixed-frequency switching regulators and other power control applications, this Switched-Mode Power Supply Control Circuit can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer-coupled.

Included in this monolithic integrated circuit is a temperature-compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two 200mA source/sink power drivers. Also included are housekeeping functions such as soft-start and low supply voltage lockout, digital current limiting, double-pulse inhibit, a data latch for single-pulse metering, adjustable dead time, and provision for symmetry correction inputs.

The output cirtcuit has been redesigned to eliminate the current spiking problem associated with source/sink drivers. The output stage has been designed so that in the transition from source-to-sink, or sink-to-source, the conducting device is shut off one transistor delay before the other device is turned on. This output correction allows the designer to utilize the speed of the other features of this controller at system frequencies up to 400kHz.

For ease of interface, all digital inputs are TTL and CMOS compatible. Active LOW logic allows wired-OR connections for maximum flexibility.

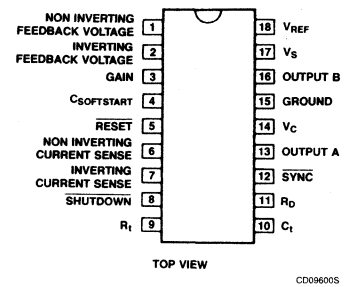
The low-cost SG3526 is rated for continuous operation over the junction temperature range of 0°C to +125°C. It is furnished in either the Cerdip package or a dual in-line plastic package with copper alloy lead frame for improved heat dissipation.

FEATURES

- **7.4 to 35V operation**
- **Dual 200mA source/sink outputs**
- **Cycle-by-cycle operation of all features up to 400kHz**
- **No current spikes on V_C line at source-to-sink or sink-to-source transitions**
- **Stabilized power supply**
- **Current limiting**
- **Temperature-compensated reference source**
- **Sawtooth generator**
- **Low supply voltage protection**
- **External synchronization**
- **Double-pulse suppression**
- **Programmable dead time**
- **Programmable soft start**
- **18-pin dual in-line plastic package, 18-pin Cerdip hermetic package, or 20-pin plastic SO**

PIN CONFIGURATIONS

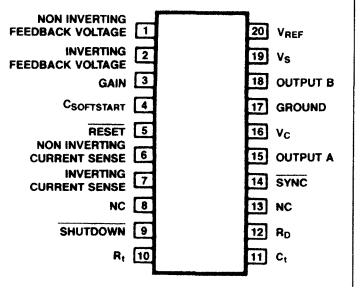
F, N Packages



TOP VIEW

CD09600S

D Package[1]



TOP VIEW

CD09590S

NOTE:
1. SOL and non-standard pinout.

ORDERING CODE

DESCRIPTION	AMBIENT TEMPERATURE	ORDER CODE
20-pin Plastic SOL DIP	0 to +70°C	SG3526D
18-pin Cerdip	0 to +70°C	SG3526F
18-pin Plastic DIP	0 to +70°C	SG3526N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	40	V
V_C	Collector supply voltage	40	V
V_{IN}	Logic input voltage range, Pins 5, 8, 12	−0.3 to +5.5	V
V_{IN}	Analog input voltage range, Pins 1, 2, 6, 7	−0.3V to V_S	V
I_O	Output current	± 250	mA
I_{REF}	Reference load current	50	mA
I_{IN}	Logic sink current	15	mA
P_D	Package power dissipation (Plastic DIP)[2] (SO), (Cerdip)[2]	1.9 1.4	W[1] W[1]
T_S	Storage temperature range	−65 to +150	°C

NOTES:
1. Maximum junction temperature, T_{JMAX} = 150°C. Rating is for T_A = 25°C.
2. Plastic θ_{JA} = 66°C/W; Cerdip θ_{JA} = 88°C/W; SO θ_{JA} = 85°C/W.

BLOCK DIAGRAM

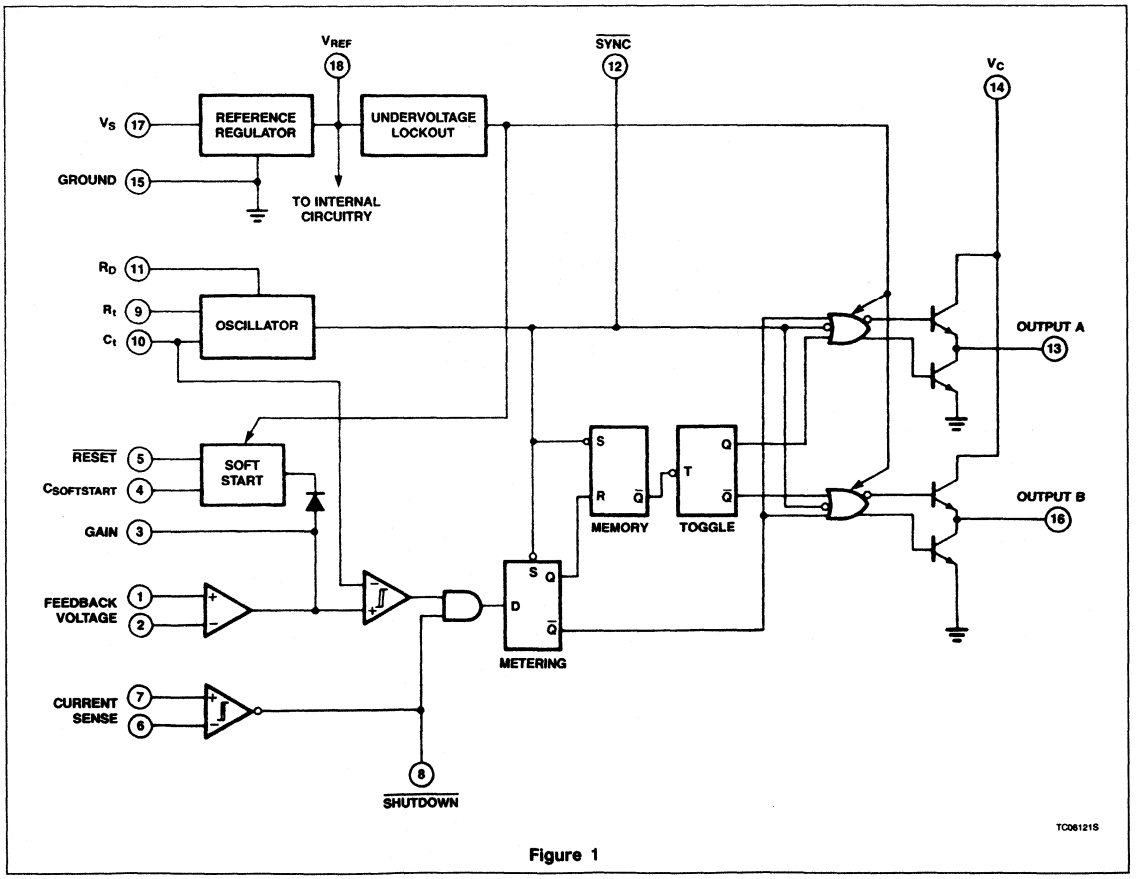


Figure 1

DC ELECTRICAL CHARACTERISTICS All specs over operating junction temperature range, V_S = 15V, unless otherwise noted.

SYMBOL	CHARACTERISTICS	TEST PINS	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Reference, Pin 18							
V_{REF}	Reference voltage	18	T_J = +25°C		5.00		V
	Temperature stability	18			0.2	0.4	mV/°C
	Total output variation	18	7.4V < V_S < 35V, 0 < I_L < 10mA	4.85	5.00	5.15	V
	Line regulation	18	7.4V < V_S < 35V, I_L = 0mA		0.6	2	mV/V
	Load regulation	18	0mA < I_L < 10mA		0.4	2.5	mV/mA
	Short circuit current	18	V_{REF} = 0V	-25	-75	-125	mA
	Output noise voltage	18	10Hz ≤ f ≤ 80kHz		100		μV_{RMS}
Low supply shutdown, Internal and Pin 5							
	Comparator threshold voltage			3.8	4.2	4.8	V
	Hysteresis				0.2		V
	Reset voltage out	5	When shutdown for LOW V_S		0.2	0.4	V
	Reset voltage out	5	When not shutdown	2.4	4.8		V
	Reset sink current	5	When shutdown, V_{IL} = 0.4V		-190	-360	μA
	Reset source current	5	When not shutdown, V_{IH} = 2.4V		-110	-200	μA
Oscillator, Pins 9, 10, 11 and SYNC, Pin 12[1]							
	Minimum frequency range	9, 10, 11 & 12	R_T = 150k, C_T = 20μF, R_D = 0Ω			1.0	Hz
	Maximum frequency range		R_T = 2k, C_T = 300pF, R_D = 0Ω, T_J = 125°C	400			kHz
	Initial accuracy	9, 10	R_T = 4.12k, C_T = 0.01μF, R_D = 0Ω, T_J = 25°C	36.8	40	43.2	kHz
V_{COSC}	Voltage stability[2]	9, 10	7.4V < V_S < 35V		0.02	0.04	%/V
T_{COSC}	Temperature stability[2]	9, 10			0.04	0.06	%/°C
	Sawtooth peak voltage	10	V_S = 35V	2.0	3.0	3.5	V
	Sawtooth valley voltage	10	V_S = 7.4V	0.5	1.0	1.5	V
	Sync. in HIGH level	12	I_{SOURCE} = 40μA	2.4	4.0		V
	Sync. in LOW level	12	I_{SINK} = 3.6mA		0.2	0.4	V
	Sync. in bias current, HIGH	12	V_{IH} = 2.4V		-105	-200	μA
	Sync. in bias current, LOW	12	V_{IL} = 0.4V		-180	-360	μA
	Min sync. in pulse width to trigger	12		200	150		ns

DC ELECTRICAL CHARACTERISTICS (Continued) All specs over operating junction temperature range, V_S = 15V, unless otherwise noted.

SYMBOL	CHARACTERISTICS	TEST PINS	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Error amp, Pins 1, 2 and 3[3]							
V_{OS}	Input offset voltage	1, 2			2.0	10	mV
I_B	Input bias current	1, 2			210	1000	nA
I_{OS}	Input offset current	1, 2			5	200	nA
A_{VOL}	DC open-loop gain	1, 2, 3		60	68		dB
V_{OH}	High output voltage	3	I_{SOURCE} = 100μA	3.6	4.2		V
V_{OL}	Low output voltage	3	I_{SINK} = 100μA		0.11	0.4	V
CMRR	Common-mode rejection ratio	1, 2, 3	R_S = 2k	70	110		dB
PSRR	Power supply rejection ratio	1, 2, 3	V_S = 10V to 20 V	90	110		dB
	Small-signal bandwidth	1, 2, 3			1.0		MHz
	Feedback resistor range	2, 3		50		1000	kΩ
	Output sink current	3		70	100		μA
	Output source current	3		70	100		μA
PWM comparator, Internal and Pin 3[1]							
	Minimum duty cycle		V_{COMP} = 0.4V			0	%
	Maximum duty cycle		V_{COMP} = 3.6V	45	49		%
	Dead time accuracy		R_T = 4.12k, C_T = 0.01μF, R_D = 0Ω		1.5		μs
	Prop. delay, PWM comp to output				250		ns
	Bias current, duty cycle control	3			1		μA
Soft-start, Pins 4 and 5							
	Soft-start trip voltage	4	V_{RESET} = 0.4V		22	50	mV
	Soft-start charge current	4	V_{RESET} = 2.4V	−180	−120	−85	μA
V_{LOW}	Reset voltage, OFF	5	I_{SINK} = 3.6mA		0.2	0.4	V
V_{HIGH}	Reset voltage, ON	5	I_{SOURCE} = 40μA	2.4	4.0		V
	Reset bias current, HIGH	5	V_{IN} = 2.4V		−110	−200	μA
	Reset bias current, LOW	5	V_{IN} = 0.4V		−200	−360	μA
Remote ON/OFF (shutdown), Pin 8							
	Off (LOW)	8	I_{SINK} = 3.6mA		0.2	0.4	V
	On (HIGH)	8	I_{SOURCE} = 40μA	2.4	4.0		V
	Input current, shutdown HIGH	8	V_{IN} = 2.4V		−100	−200	μA
	Input current, shutdown LOW	8	V_{IN} = 0.4V		−190	−360	μA
	Delay to output(s)	8			400		ns
Current limit comparator, Pins 6 and 7							
	Common-mode range	6, 7	V_S = 18V	0		15	V
	Sense voltage for Min duty cycle	6, 7		70	100	140	mV
	Input bias current	6, 7	V_{CM} = 0V to 15V		−3	−20	μA
	Voltage gain	6, 7			68		dB
	Delay to outputs	6, 7	100mV overdrive		700		ns

DC ELECTRICAL CHARACTERISTICS (Continued) All specs over operating junction temperature range, V_S = 15V, unless otherwise noted.

SYMBOL	CHARACTEPISTICS	TEST PINS	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Output stage, Pins 13, 14 and 16							
V_{OH}	High output voltage	13, 14, 16	I_{SOURCE} = 20mA, V_C = 15V	12.8	13.5		V
			I_{SOURCE} = 100mA, V_C = 15V	12.5	13.3		V
			I_{SOURCE} = 200mA, V_C = 15V	12.0	13.2		V
V_{OL}	Low output voltage	13, 14, 16	I_{SINK} = 20mA, V_C = 15V		0.15	0.3	V
			I_{SINK} = 100mA, V_C = 15V		1.25	1.8	V
			I_{SINK} = 200mA, V_C = 15V		2.20	3.00	V
	Output leakage	13, 14, 16	V_C = 40V		45	100	μA
	I_{SINK} Max	13, 14, 16	V_C = 15V	200	250		mA
	I_{SOURCE} Max	13, 14, 16	V_C = 15V	200	250		mA
t_R	Rise time	13, 14, 16	C_L = 1000pF, V_C = 15V		300		ns
			C_L = 0pF, V_C = 15V		50		ns
t_F	Fall time	13, 14, 16	C_L = 1000pF, V_C = 15V		200		ns
			C_L = 0pF, V_C = 15V		50		ns
Supply current[4]							
I_{CC}	Shutdown LOW	17	7.4V < V_S < 35V		24	30	mA
Operating frequency for cycle-by-cycle operation of all protect features							
	Maximum frequency			400	500		kHz

NOTES:
1. f_{OSC} = 40kHz (R_T = 4.12k, C_T = 0.01μF, R_D = 0Ω) unless otherwise noted.
2. Guaranteed by design.
3. V_{CM} = 0V to 5.2V.
4. R_T = 4.12kΩ.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_S	Logic supply voltage	7.4	35	V
V_C	Collector voltage	4.5	35	V
I_O	Output load current	0	±200	mA
I_L	Reference load current	0	10	mA
f_{OSC}	Oscillator frequency	1Hz	400	kHz
R_t	Oscillator timing resistance	2	150	kΩ
C_t	Oscillator timing capacitance	150pF	20	μF
DT	Programmed dead time	3	50	%
T_A	Ambient temperature range	0	+70	°C
T_J	Junction temperature range	0	+125	°C

THEORY OF OPERATION

Internal Reference

The internal reference is capable of maintaining 1% accuracy over the specified operating temperature range. The reference voltage is 5.00V at Pin 18. Short-circuit current is typically 50mA. The reference output remains stable within 30mV over an input range of 8 to 35V. Complete regulation characteristics versus line and load (see Figure 1) are listed in the Electrical Characteristics section of the data sheet. The maximum recommended load on the reference supply is 20mA.

THE RAMP OSCILLATOR

The ramp oscillitor is a self-sustained, fixed-frequency circuit with programmability provided by selecting the value of an external resistor and capacitor as shown in Figure 2. An internal current source is set by the resistor R_t to a certain value of charging current sufficient to generate a stable ramp over a range of 1Hz to 400kHz.

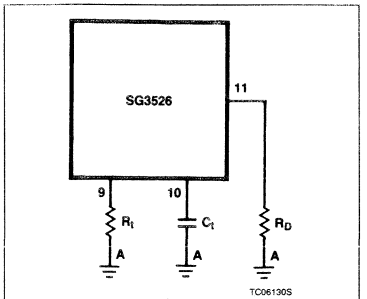
THE ERROR AMPLIFIER

The error amplifier is a transconductance-type with open-loop unity gain bandwidth of 1MHz. Typical source/sink current is 100μA. Open-loop DC gain is 68dB with a single dominant pole at 500Hz. (See Figure 3 for detailed response.) Compensation is achieved by simple 'C' (100pF) or RC network for lag-lead compensation. This network is placed in shunt to ground from Pin 3 (refer to Figure 4). Common-mode voltage is 5V for a standard positive supply and ground for negative supply.

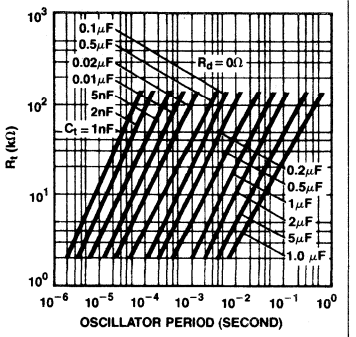
The Pulse Width Modulator

The pulse width modulator consists of a high-speed comparator with non-inverting input tied to the ramp generator and inverting input driven by the error amplifier output. (See Figure 5.) The resultant output forms a gated input to the metering flip-flop of which the '$\overline{Q}$' output feeds the 'R' input on the memory latch, and 'Q' output enables the main output gates (G2, G3). Alternate half-cycles are then enabled at the output (Pins 13 and 16) by the action of the toggle flip-flop. Initiation of the beginning of each half of the duty cycle is triggered by the start of the ramp, and termination occurs at the point in time where error output meets ramp voltage. It is with this sequence of control events that glitch-free output is guaranteed.

Pulse delay times in the PWM loop are specified in the data sheet. Maximum operating frequency must take such delay times into account in order to guarantee reliable functioning of the controller under a closed-loop condition. The Signetics SG3526 is rated at a typical maximum frequency of 500kHz.



a. Ramp Oscillator Frequency Determining Components and Dead Time Programming



b. Oscillator Period vs R_+ and C_+

Figure 2

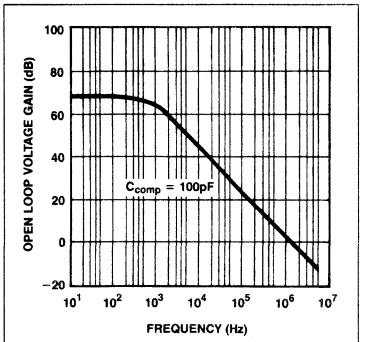


Figure 3. Error Amplifier Open-Loop Gain vs Frequency

PWM GAIN

The DC gain of the pulse width modulator is determined by the ratio of input voltage to the primary power switching circuit to the active ramp voltage differential. This is given as 3.6V and 0.4V with a differential of 3.2V.

Example:
The DC supply voltage to the power converter is 48V.

$$\text{Therefore, PWM Gain} = \frac{48}{3.2} = 15$$

(For further information on loop response calculations, please refer to references 1, 2.)

THE OUTPUT DRIVER STAGE

The output driver circuit has been carefully designed to prevent cross-conduction current spikes by eliminating any overlap conduction within the totem-pole structure. The source and sink capacity is rated at 200mA. In addition, supply voltage on the driver transistors is rated at 35V with no risk of destroying the IC due to excessive power dissipation. Note the output waveform in Figure 6 shows a full 10V drive level at the rated 200mA load current. This capability means that a Power MOS gate capacity of 4000pF can be driven with a voltage rise time of 0.2μs for a 10V output.

PROTECTIVE FUNCTIONS

Dead Time Control

The dead time control circuit, incorporated as an integral part of the ramp oscillator, is provided to allow the designer the ability to control the minimum off time between alternate half-cycles. (See Figures 7 and 8.) The value of R_D, as shown in the graph, allows the programming of this delay time from a minimum (Pin 11 grounded) of 1.5μs to a maximum of 9.7μs for a resistance of 22Ω tied from Pin 11 to ground (Figure 8b). Obviously, dead time in the oscillator must conform to the limitations imposed by the operating frequency.

Overcurrent Limit

The overcurrent limit function is an integral part of the PWM circuit and, as such, inputs on Pins 6 and 7 will control the cycle-by-cycle operation of the output stage on both halves of the duty cycle. The overcurrent comparator is specifically designed to propagate a high-speed shutdown signal to turn off the output metering flip-flop in the event of an overcurrent of predetermined magnitude. The overcurrent sense inputs must be treated with care in respect to lead length and shunt capacity in order to obtain the maximum speed of response. Some typical circuit configurations are shown in Figure 9a. Note that either Pin 6 or 7 may be used as threshold reference voltage anywhere within the common-mode voltage range of the comparator. As shown, a simple technique is to ground Pin 6 and to program Pin 7 high ($\geq$ 100mV) for shutdown. Very little noise immunity is allow-

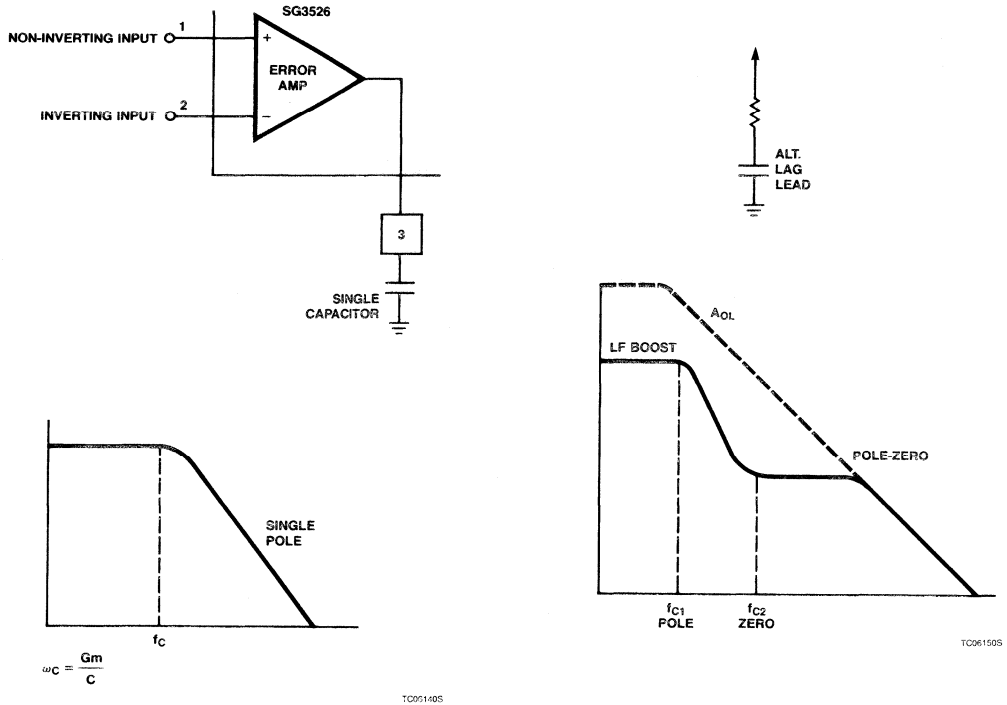


Figure 4. Loop Compensation

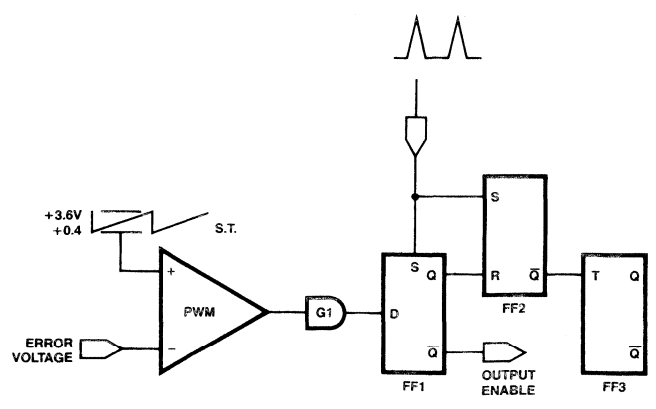


Figure 5. PWM

ed in this case. An improved method is to set Pin 6 at some positive voltage level (such as +2.5V) and thus provide an average noise threshold of 2.5V +100mV as shown in Figure 9b. This particular circuit provides a considerable improvement in noise immunity. Note that care must be taken in providing a low impedance reference at Pin 6. The over-current sense comparator provides a typical hysteresis of 20mV with a threshold of 100mV (Figure 9c). The typical delay time to deactivate the output drive is 700ns at T_J = 25°C rising to 1200ns at T_J = 125°C.

Soft-Start

This circuit provides a programmed ramp-up of the duty cycle at power-on, after remote shutdown (reset Pin 5) or low supply sense. A capacitor from Pin 4 to ground is charged towards the turn-on threshold by a 100μA source. Time constants for various values of capacitance are plotted for the designer's convenience as shown in Figure 10. The soft-start function is inititated by holding the reset below 0.2V which causes C to discharge. The Reset function, when low, also holds the error amplifier output low, initiating a minimum duty cycle at the output drivers. Low voltage shut-down occurs when V_S (Pin 17) drops below 4.0V.

External Synchronization

An external sync pulse may be injected into Pin 12 in order to provide synchronous operation of a switched-mode controller as shown in Figure 11. The required voltage level is active LOW with a threshold of 0.4V typical and a minimum pulse width of 150ns. A periodic signal at a rate approximately 10% higher than the free-running frequency of the ramp oscillator is required.

THERMAL CONSIDERATIONS

The power dissipation of the SG3526 must be considered in the design procedure in order to insure operation within the allowable device limits, particularly when maximum operating frequency is desired. The graph provided in Figure 12 will serve as a guide to staying within the device thermal limits in any design. Device dissipation is determined by summing all of the various current-voltage products, both pulsed and DC, noting the package type and the ambient operating temperature, then plotting this total device power on the respective derating graph.

UNDERVOLTAGE LOCKOUT

Should supply voltage in Pin 17 drop low enough to affect the internal reference regulator, an output inhibit circuit is activated. In addition, the voltage on Pin 5 (Reset) will be brought to a low state in order to signal remote sensing indicators. This characteristic is shown graphically in Figures 13a and b.

SYMMETRY CORRECTION

Should an external symmetry monitoring and correction circuit be required where drive unbalance may be critical, Pin 8, the shut-down function, is available to program either half of the output cycle off. This is accomplished by applying a TTL low signal with a pulse synchronized to the clock frequency. Keep in mind that the typical delay from Pin 8 is either output before shutdown is 400ns.

DOUBLE PULSE PROTECTION

The memory flip-flop must be reset by the PWM signal. This set-reset sequence provides insurance that alternate sync pulses initiate alternate A-B output cycle, preventing double pulses at the output.

CAUTION: Supply Decoupling —
Pin 17, the supply input to the internal regulator, should be decoupled from Pin 14 in order to prevent pulsed switching currents from interacting with outputs.

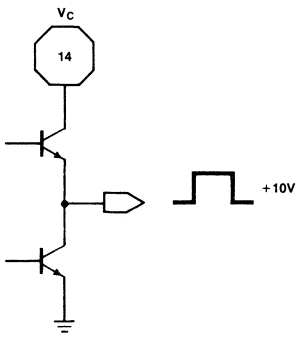


Figure 6. Output Stage

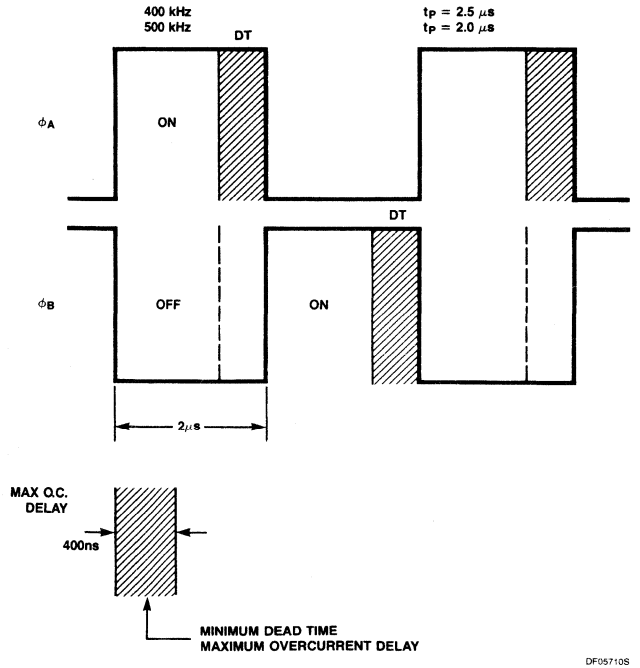
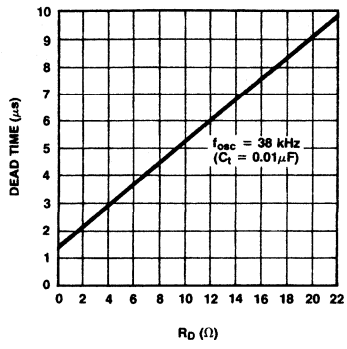
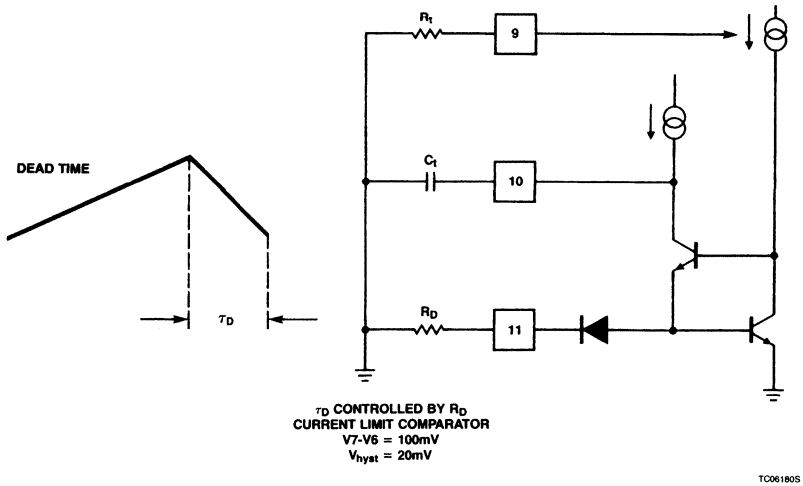


Figure 7

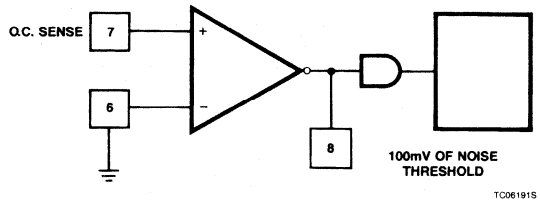


a. Output Driver Dead Time vs R_D Value

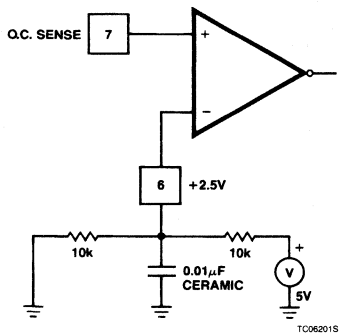


b. Dead Time

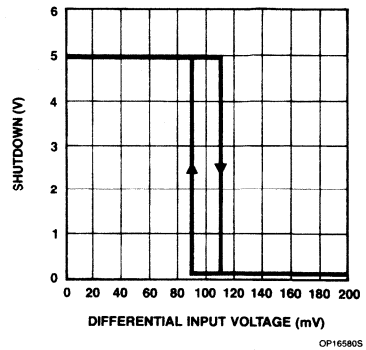
Figure 8



a. OC Threshold



b. OC Threshold



c. Current Limit Transfer Function

Figure 9

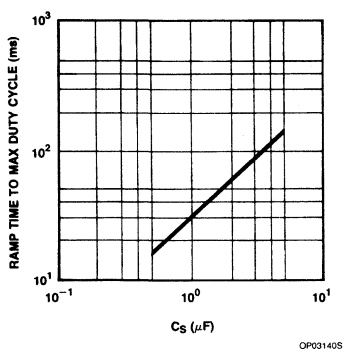


Figure 10. Soft-Start Time Constant vs C_S

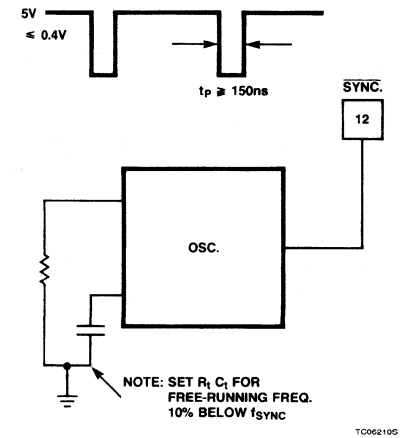


Figure 11

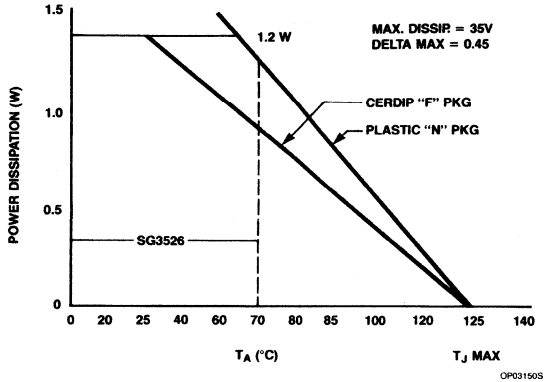
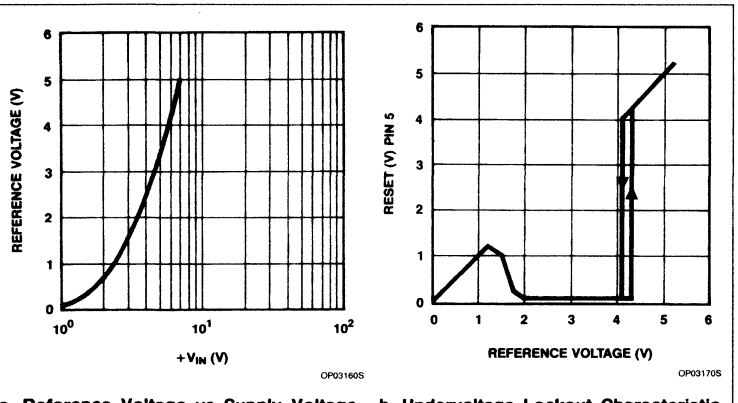


Figure 12. Power Dissipation vs Ambient Temperature



a. Reference Voltage vs Supply Voltage b. Undervoltage Lockout Characteristic

Figure 13

REFERENCES:

1. *Advances in Switched-Mode Power Conversion*, Volumes I and II, R.D.Middlebrook and Slobodan Cuk; Telsa Co., Pasadena, CA, 1983.

2. *Stability Analysis Made Simple*, H. Dean Venable; Venable Industries, Rancho Palos Verdes, CA, 1981.

CONTROL CIRCUIT FOR SMPS

GENERAL DESCRIPTION

The TDA1060 is a bipolar integrated circuit intended for the control of a switched-mode power supply. It incorporates all the control functions likely to be required in switched-mode power supplies for professional equipment.

Features

- Suitability for a wide range of supply voltages
- Built-in stabilized power supply for external circuitry
- Built-in temperature-compensated voltage reference
- Adjustable frequency
- Adjustable control loop sensitivity
- Adjustable pulse width
- Adjustable maximum duty factor
- Adjustable overcurrent protection limit
- Low supply voltage protection with hysteresis
- Loop fault protection
- Slow-start facility
- Feed-forward facility
- Core saturation protection facility
- Overvoltage protection facility
- Remote ON/OFF switching facility

QUICK REFERENCE DATA

Supply voltage (voltage source)	V_{CC}	max.	18 V
Supply current (current source)	I_{CC}	max.	30 mA
Output current	$-I_{14}; I_{15}$	max.	40 mA
Stabilized voltage	V_Z	typ.	8,4 V
Reference voltage	V_{ref}	typ.	3,72 V
Output pulse repetition frequency range	f_o	50 Hz to 100	kHz
Operating ambient temperature range			
TDA1060; T	T_{amb}	−25 to + 125	°C
TDA1060A	T_{amb}	0 to + 70	°C
TDA1060B	T_{amb}	−55 to + 150	°C

PACKAGE OUTLINES

TDA1060, TDA1060A: 16-lead DIL; plastic (SOT38).
TDA1060B: 16-lead DIL ceramic (cerdip) (SOT74).
TDA1060T: 16-lead mini-pack; plastic (SO16; SOT109A).

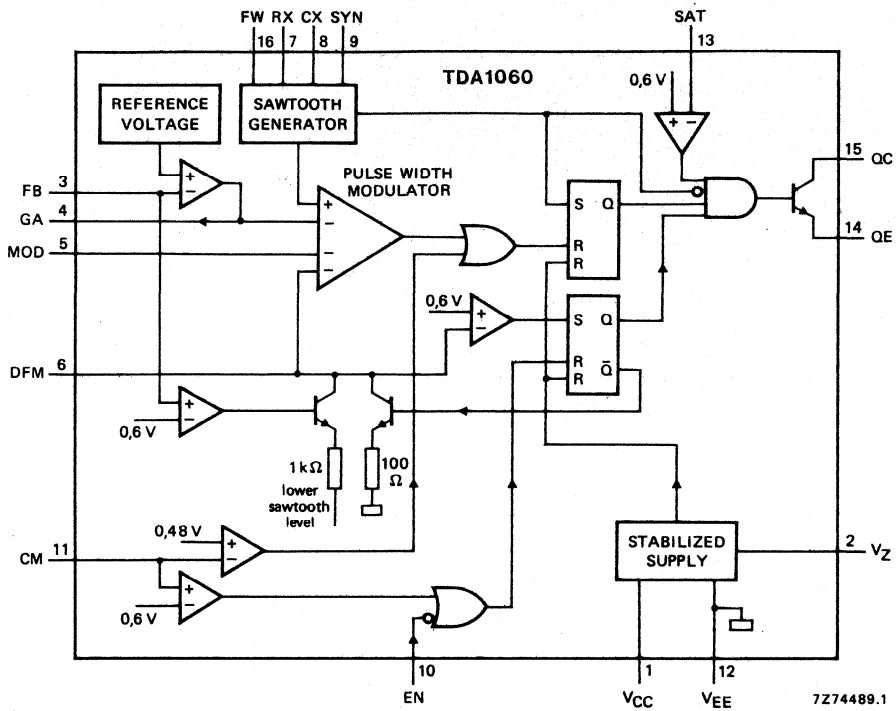


Fig. 1 Block diagram.

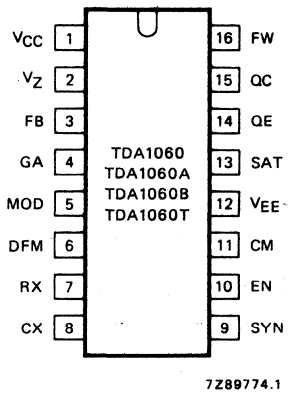


Fig. 2 Pinning diagram.

PINNING

1	V_{CC}	positive supply connection
2	V_Z	stabilized voltage output
3	FB	feedback input
4	GA	gain adjustment output
5	MOD	modulation input
6	DFM	maximum duty factor input
7	RX	external resistor connection
8	CX	external capacitor connection
9	SYN	synchronization input
10	EN	ENABLE input
11	CM	overcurrent protection input
12	V_{EE}	common
13	SAT	core saturation and overvoltage protection input
14	QE	emitter output
15	Q_C	collector output
16	FW	feed-forward input

FUNCTIONAL DESCRIPTION

The TDA1060 contains the control loop for a fixed-frequency pulse-duration regulated SMPS. The device works as follows. The output voltage V_O of the SMPS is sensed via a feedback network and compared with an internal reference voltage V_{ref}. Any difference between V_O and V_{ref} is amplified and fed to a pulse-width modulator (PWM), where it is compared with the instantaneous level of a ramp waveform (sawtooth) from an oscillator. The output from the PWM is a rectangular waveform synchronized with the oscillator waveform; its duty factor depends on the difference between V_O and V_{ref}. This signal drives the base of the SMPS power switching transistor so that its conduction period and hence the amount of energy transferred from the input to the output of the SMPS is controlled, resulting in a constant output voltage.

Stabilized power supply: V_{CC} and V_Z (pins 1 and 2)

The circuit contains a voltage/current regulator and may be supplied either by a current source (e.g. a series resistor connected to the high voltage input of the SMPS), or a voltage source (e.g. a 12 V battery).

The stabilized voltage, typically 8,4 V, is also available at V_Z, pin 2 for supplying external circuitry, e.g. a potentiometer to adjust the maximum duty factor. This supply output is protected against short-circuits. The current drawn from this output increases the total IC supply current by the same amount.

When the supply voltage V_{CC} becomes too low, i.e. $V_{CC} < V_Z + 0{,}2$ V, the circuit is automatically switched off. As soon as the supply voltage exceeds this threshold value by more than 0,2 V the circuit starts the SMPS via the slow start procedure.

Operating frequency: RX and CX (pins 7 and 8)

The frequency of the sawtooth generator, and hence of the output pulses, is set by an external resistor R7 at RX, pin 7, and an external capacitor C8 at CX, pin 8 (see Fig. 7). The frequency may be set between 50 Hz and 100 kHz and is virtually independent of the supply voltage.

Maximum duty factor and slow start: DFM (pin 6)

The maximum duty factor is set by the voltage on the duty factor input DFM (see Fig. 4). This voltage usually is derived from the stabilized power supply V_Z, pin 2, by an external voltage divider, see Fig. 8. As the upper and lower levels of the sawtooth waveform are set by an internal voltage divider, the accuracy of the maximum duty factor setting is determined by resistor ratios rather than by absolute values.

In case of a short-circuited feedback loop ($V_{3\text{-}12}$ less than typ. 600 mV) the duty factor input is internally biased to the lower level of the sawtooth waveform via a resistor of typ. 1 kΩ. The maximum duty factor permitted in that case sets a maximum limit to the impedance level of the external voltage divider at pin 6.

During the flyback of the sawtooth the output pulse is inhibited. For a 1 nF capacitor C8 at pin 8 this flyback time is 1 μs. This sets a natural limit to the duty factor.

The time constant for the slow start is determined by an external capacitor connected between the maximum duty factor input DFM and V_{EE}, pin 12, together with the impedance of the voltage divider at pin 6. This capacitor also determines the dead time before the slow start procedure for remote ON/OFF or when the current sensing voltage has exceeded 600 mV, see below.

If the DFM input is note used it should be connected to V_Z via a resistor of 5 kΩ.

FUNCTIONAL DESCRIPTION (continued)

Control loop sensitivity, stability, and feedback loop fault protection, FB and GA (pins 3 and 4)

The device contains a control loop error amplifier, i.e. a differential amplifier that compares the voltage on the feedback input FB, pin 3, with the internal reference voltage. This reference voltage is a temperature-compensated voltage source based on the band-gap energy of silicon.

The control loop sensitivity is determined by the closed-loop gain A_f of the error amplifier. Normally the output from the SMPS is connected to the feedback input FB via a voltage divider and a series resistor. The closed-loop gain of the error amplifier is set by applying feedback from the gain adjustment output GA, pin 4, to the feedback input FB by a resistor R3-4, see Fig. 8.

To avoid instability a capacitor should be connected between the gain output GA and V_{EE}, pin 12. A 22 nF capacitor will cause the frequency response to fall off above 600 Hz.

The feedback input FB is internally biased to the HIGH level, this gives a protection against a feedback loop fault: an open feedback loop will make the duty factor zero.

A shorted feedback loop (feedback voltage less than typ. 600 mV) causes the maximum duty factor input DFM to be internally biased to the lower level of the sawtooth waveform via a resistor of typ. 1 kΩ, thus substantially reducing the maximum duty factor. This duty factor will then be determined by the impedance of the external voltage divider at DFM, pin 6, and the internal biasing resistor.

Overcurrent protection input CM (pin 11)

There are two current limits, corresponding with voltages on the overcurrent protection input CM of typ. 480 mV and 600 mV. As soon as the voltage on this input exceeds 480 mV, the running output pulse is immediately terminated; the next pulse starts normally at the next period. If the voltage exceeds 600 mV, the output pulses are inhibited for a certain dead time, during which the slow start capacitor at pin 6 is unloaded. After this the circuit starts again with the slow start procedure.

If the overcurrent protection input CM is not used, it should be connected to V_{EE}, pin 12.

Feed-forward input FW (pin 16)

The feed-forward input FW can be connected to an external voltage divider from the input voltage of the SMPS, see Fig. 8. It has the effect of varying the supply voltage of the sawtooth generator with respect to the stabilized voltage. When the voltage on the feed-forward input increases, the upper level of the sawtooth is also increased. Since neither the voltage level that sets the maximum duty factor nor the feedback voltage are influenced by the feed-forward, the duty factor reduces (see Fig. 6). This can therefore compensate for mains voltage variations.

If feed-forward is not required the feed-forward input FW should be connected to V_{EE}, pin 12.

Synchronization input SYN (pin 9)

The frequency of the sawtooth waveform, and hence of the output pulses, can be synchronized via the TTL compatible synchronization input SYN. The synchronizing frequency must be lower than the oscillator free-running frequency. When the synchronization input is LOW the sawtooth generator is stopped; it starts again when the input goes HIGH. Synchronization pulses do not influence the slope of the sawtooth, and hence not the width of the output pulses, they only change their separation in time.

For free-running operation it is advisable to connect the synchronization input SYN to V_Z, pin 2.

Core saturation and overvoltage protection input SAT (pin 13)

To obtain a protection against core saturation, especially during transient conditions, the output transformer of the SMPS has to be fitted with a winding serving as a current sensor. Its output voltage is rectified and fed to the SAT input.

This core saturation protection may be combined with an overvoltage protection. To this end a portion of the SMPS output voltage is also fed to the SAT input either via a voltage divider or via a suitable regulator diode (zener diode). The output pulses are inhibited as long as the voltage on this input exceeds the threshold voltage, typ. 600 mV.

The voltage at the SAT input does not influence the frequency of the sawtooth generator and hence not of the output pulses.

If none of these protection facilities are used, the SAT input should be connected to V_{EE}, pin 12.

Remote ON/OFF switching: ENABLE input EN (pin 10)

The output pulses can be switched on and off by applying logic levels to the TTL compatible ENABLE input. A LOW level causes immediate inhibition of the output pulses, a subsequent HIGH level switches the circuit on with the slow-start procedure.

If this facility is not required, EN should be connected to V_Z, pin 2.

Modulation input MOD (pin 5)

The duty factor of the output pulses may be reduced below the value resulting from the voltages on the maximum duty factor input DFM and the gain adjust output GA by applying a lower voltage to the modulation input MOD. This input may be used with an external control loop, e.g. for constant-current control, or to obtain a fold-back characteristic.

If the modulation input is not used, it should be connected to V_Z, pin 2.

Output QC and QE (pins 13 and 14)

To avoid double pulses that might occur at an excessively low mains voltage or an excessively high output current the output is preceded by a latch. The two outputs offer a choice of output current polarity, QC giving a positive current, i.e. a current flowing into the output, and QE giving a negative current, a current flowing out of the output. The two connections have the additional advantage that the relatively large output currents do not flow through the V_{CC} and V_{EE} connections, where they could induce noise.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (voltage source)	V_{CC}	−0,5 to + 18	V
Supply current (current source)	I_{CC}	max. 30	mA
Feed-forward input voltage range			
$V_{CC} < 24$ V	$V_{16\text{-}12}$	0 to V_{CC}	V
$V_{CC} > 24$ V	$V_{16\text{-}12}$	0 to 24	V
Input voltage range (all other inputs)	V_I	0 to V_Z	V
Emitter output voltage range	$V_{14\text{-}12}$	0 to 5	V
Collector output voltage range	$V_{15\text{-}12}$	0 to V_{CC}	V
Output current			
d.c. (see Figs 3a, c and e)	$-I_{14}$; I_{15}	max. 40	mA
peak; t = max. 1 μs; duty factor d < 10%	$-I_{14}$; I_{15}	max. 200	mA
Storage temperature range			
TDA1060; T	T_{stg}	−55 to + 150	°C
TDA1060A	T_{stg}	−55 to + 150	°C
TDA1060B	T_{stg}	−55 to + 150	°C
Operating ambient temperature range			
TDA1060; T	T_{amb}	−25 to + 125	°C
TDA1060A	T_{amb}	0 to + 70	°C
TDA1060B	T_{amb}	−55 to + 150	°C
Power dissipation (see Figs 3b, d and f)	P_{tot}	max. 1	W

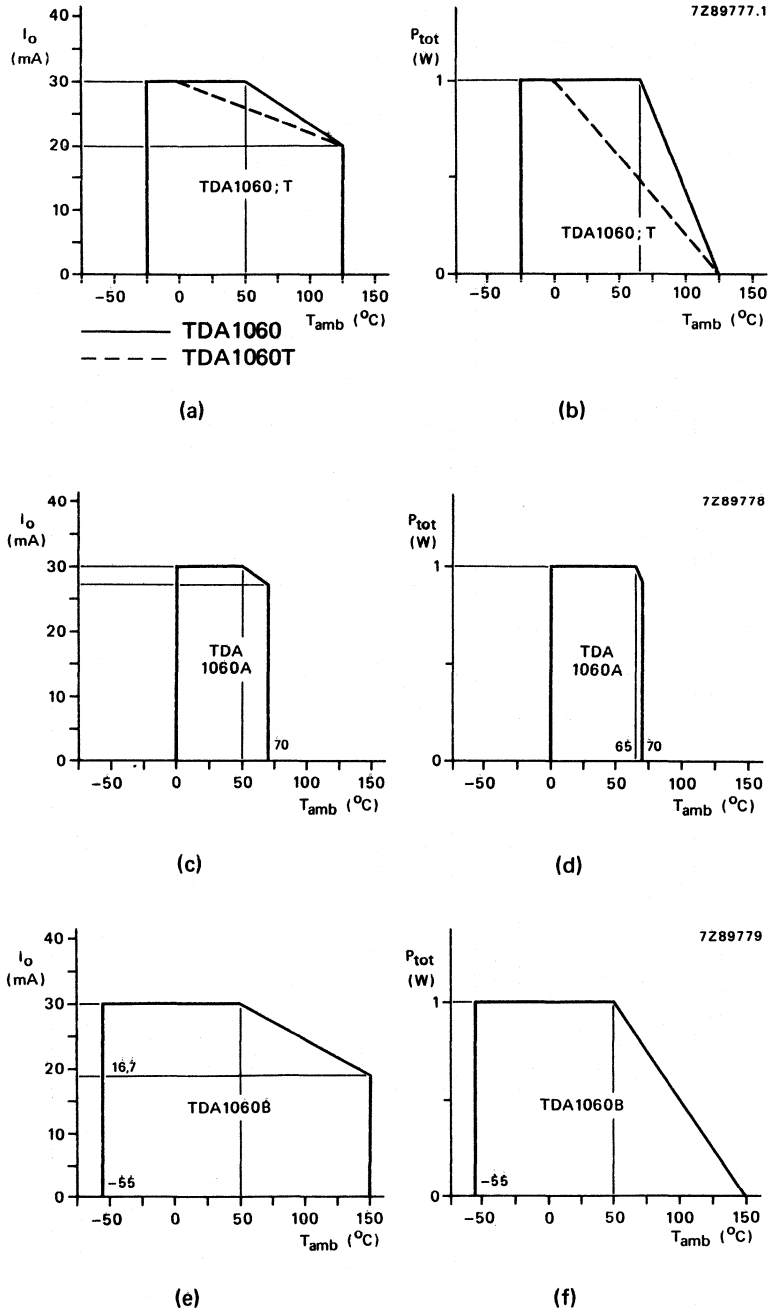


Fig. 3 Output current and power dissipation derating curves.

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = operating ambient temperature range, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Operating ambient temperature range					
TDA1060; T	T_{amb}	−25	–	125	°C
TDA1060A	T_{amb}	0	–	70	°C
TDA1060B	T_{amb}	−55	–	150	°C
Supply V_{CC} (pin 1)					
Supply voltage at I_{CC} = 15 mA					
TDA1060; T	V_{CC}	18,5	23	27	V
TDA1060A	V_{CC}	18,5	23	27	V
TDA1060B	V_{CC}	18	23	27,5	V
at I_{CC} = 30 mA					
TDA1060; T	V_{CC}	19,5	24	29	V
TDA1060A	V_{CC}	19,5	24	29	V
TDA1060B	V_{CC}	19	24	29,5	V
Supply current; R7 = 25 kΩ; duty factor δ = 50%; I_Z = 0; at T_{amb} = 25 °C	I_{CC}	2,5	–	10	mA
over ambient temperature range	I_{CC}	2,5	–	15	mA
Threshold voltage of low supply voltage protection at T_{amb} = 25 °C	V_{CC}	8,85	–	10,8	V
Variation with temperature	$-\Delta V_{CC}/\Delta T$	–	7,5	–	mV/K
Hysteresis of low supply voltage protection	ΔV_{CC}	–	500	–	mV
Stabilized supply output V_Z (pin 2)					
Output voltage at T_{amb} = 25 °C	V_Z	7,5	8,4	9	V
Variation with temperature	$\Delta V_Z/\Delta T$	−1,5	–	+ 1,5	mV/K
Output current	$-I_Z$	–	–	5	mA
Feedback input FB (pin 3)					
Input voltage, feedback operation	$V_{3\text{-}12}$	2	–	V_Z-1	V
Input current at $V_{3\text{-}12}$ = 2 V	$-I_3$	1,5	12	35	μA
Internal reference voltage, measured at pin 3; pins 3 and 4 interconnected and grounded via a 100 nF capacitor; T_{amb} = 25 °C	V_{ref}	3,42	3,72	4,03	V
Variation with temperature	$\frac{\Delta V_{ref}/V_{ref}}{\Delta T}$	–	0,01	–	%/K
Variation with supply voltage	$\frac{\Delta V_{ref}}{\Delta V_{CC}}$	–	0,8	–	mV/V

parameter	symbol	min.	typ.	max.	unit
Long-term variation with time	$\pm \Delta V_{ref}/\Delta t$	–	2	–	μV/h
Threshold voltage of feedback loop short-circuit protection at $T_{amb} = 25\,^{o}C$	$V_{3\text{-}12}$	470	600	720	mV
Variation with temperature	$\frac{\Delta V_{3\text{-}12}/V_{3\text{-}12}}{\Delta T}$	–	0,01	–	%/K
Gain adjustment output GA (pin 4)					
Open-loop gain, pin 3 to pin 4	A_o	–	60	–	dB
External feedback resistance	$R_{3\text{-}4}$	10	–	–	kΩ
Modulator input MOD (pin 5)					
Input current at $V_{5\text{-}12} = 2$ V; $V_{4;\,6\text{-}12} > 2$ V	$-I_5$	–	–	5	μA
Maximum duty factor input DFM (pin 6)					
Input voltage for limiting the duty factor to 50%; f_o = 20 to 50 kHz; $V_{16\text{-}12} = 0$ V	$V_{6\text{-}12}$	–	$0{,}42V_Z$	–	V
Input current at $V_{6\text{-}12} = 2$ V	$-I_6$	–	–	6	μA
Capacitor discharge current during fault condition	I_6	2,5	–	–	mA
Minimum output OFF time at C7 = 1,8 nF	t_{off}	–	1	–	μs
Variation of max. duty factor with temperature at f_o = 20 kHz and δ_{max} = 50%	$\Delta\delta_{max}/\Delta T$	–	0,02	–	%/K
Internal biasing resistor to V_{EE} at $V_{3\text{-}12} = 0$ V	$R_{6\text{-}12}$	0,75	1	1,25	kΩ
Synchronization input SYN (pin 9)					
Input voltage, sawtooth ON	V_{IH}	2	–	V_Z	V
sawtooth OFF: TDA1060; TDA1060A; TDA1060T	V_{IL}	0	–	0,8	V
TDA1060B	V_{IL}	0	–	0,6	V
Input current at $V_{9\text{-}12} = 0$ V	$-I_{IL}$	20	–	120	μA
External resistor connection RX (pin 7)					
External frequency adjustment resistor	R7	5	–	40	kΩ
External capacitor connection CX (pin 8)					
Sawtooth, upper level at $V_{16\text{-}12} = 0$ V	$V_{8\text{-}12}$	–	5,7	–	V
lower level	$V_{8\text{-}12}$	–	1,3	–	V
Oscillator frequency R7 = 6,4 kΩ, C8 = 6,4 nF	f_{osc}	–	30,5	–	kHz
Output pulse repetition frequency range	f_o	0,05	–	100	kHz
Variation with temperature	$\frac{\Delta f_o/f_o}{\Delta T}$	–	0,03	–	%/K

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Feed-forward input FW (pin 16)					
Input voltage					
for $V_{CC} < 24$ V	$V_{16\text{-}12}$	0	–	V_{CC}	V
for $V_{CC} > 24$ V	$V_{16\text{-}12}$	0	–	24	V
Input current at $V_{16\text{-}12} = 16$ V; $V_{CC} = 18$ V; $T_{amb} = 25\ ^{o}C$	I_{16}	–	–	5	μA
Frequency variation with input voltage at $V_{16\text{-}12} > 8$ V	$\frac{\Delta f_o/f_o}{\Delta V_{16\text{-}12}}$	–	1	–	%/V
Overcurrent protection input CM (pin 11)					
Input voltage	$V_{11\text{-}12}$	0	–	V_Z	V
Input threshold voltage for single pulse inhibit (current limit mode); $T_{amb} = 25\ ^{o}C$	V_{T1}	400	–	500	mV
Ratio of threshold voltages for shot down/ slow start and for single pulse inhibit	V_{T2}/V_{T1}	–	1,25	–	
Threshold variation with temperature	$\Delta V/\Delta T$	–	125	–	μV/K
Input current at $V_{11\text{-}12} = 250$ mV	$-I_{11}$	–	–	10	μA
Turn-off delay, $I_{15} = 40$ mA; $V_{11\text{-}12} = 1{,}2 \times V_{T1}$	t_d	–	–	1,0	μs
Core saturation and overvoltage protection input SAT (pin 13)					
Input voltage	$V_{13\text{-}12}$	0	–	V_Z	V
Input threshold voltage at $T_{amb} = 25\ ^{o}C$	$V_{13\text{-}12}$	470	600	720	mV
Threshold variation with temperature	$\Delta V/\Delta T$	–	125	–	μV/K
Input current at $V_{13\text{-}12} = 250$ mV	$-I_{13}$	–	–	7	μA
ENABLE input EN (pin 10)					
Input voltage					
ON	V_{IN}	2	–	V_Z	V
OFF: TDA1060; TDA1060A; TDA1060T	V_{IL}	0	–	0,8	V
TDA1060B	V_{IL}	0	–	0,6	V
Input current at $V_{10\text{-}12} = 0$ V	$-I_{IL}$	20	–	120	μA
Outputs QC and QE (pins 14 and 15)					
Output current	$-I_{14}; I_{15}$	40	–	–	mA
Emitter output voltage	$V_{14\text{-}12}$	–	–	5	V
Collector output voltage at $V_{14\text{-}12} = 0$ V; $I_{15} = 40$ mA	$V_{15\text{-}14}$	–	–	500	mV

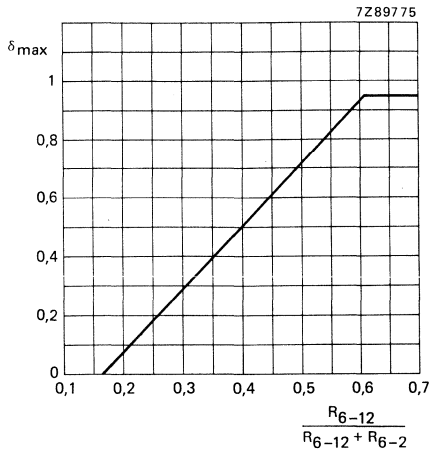


Fig. 4 Maximum duty factor δ_{max} as a function of the voltage divider ratio at the duty factor input DFM.

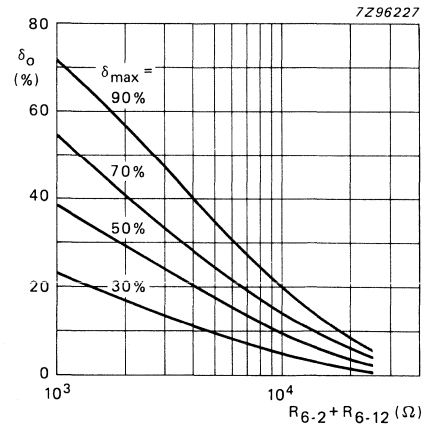


Fig. 5 Soft-start minimum duty factor (δ_o) as a function of R_{6-2} and R_{6-12}.

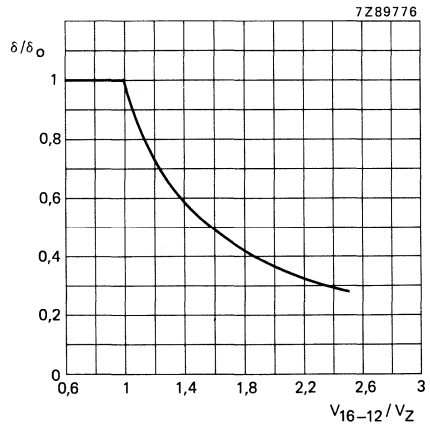


Fig. 6 Feed-forward regulation characteristic. Duty factor δ as a function of the voltage V_{16-12} on the feed-forward input FW. δ_o is the duty factor for $V_{16-12} \leqslant V_Z$.

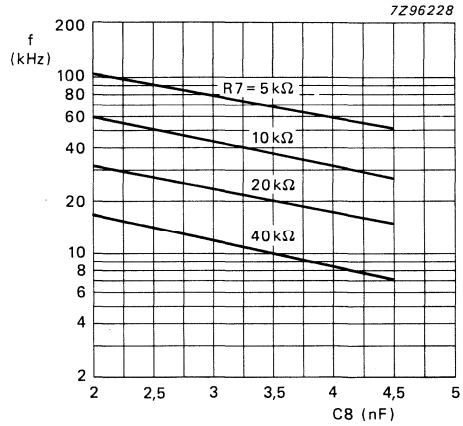


Fig. 7 Typical frequency as a function of C8 (R7 as parameter).

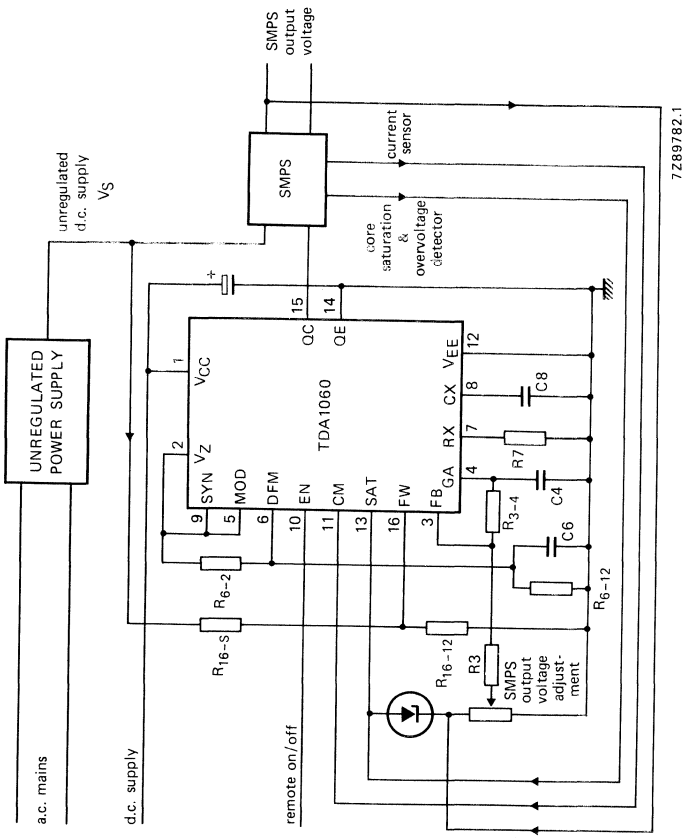


Fig. 8 Connections to the TDA1060 in a switched-mode power supply.

APPLICATION INFORMATION

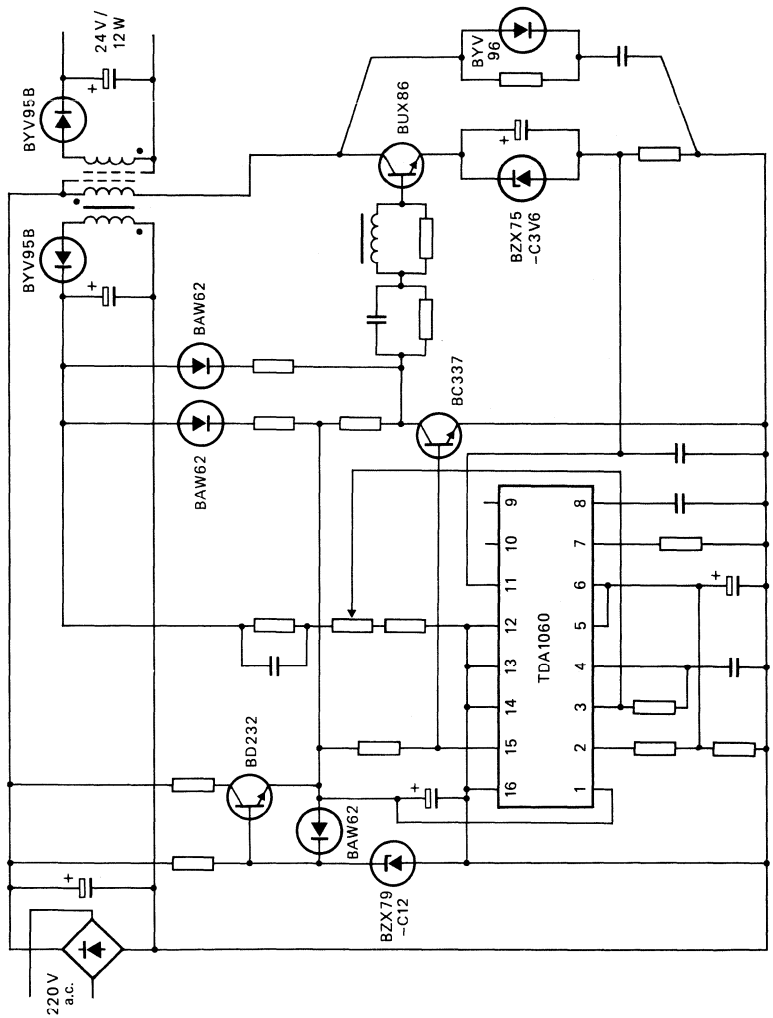


Fig. 9 Application of the TDA1060 in a 24 V, 12 W SMPS with flyback converter.

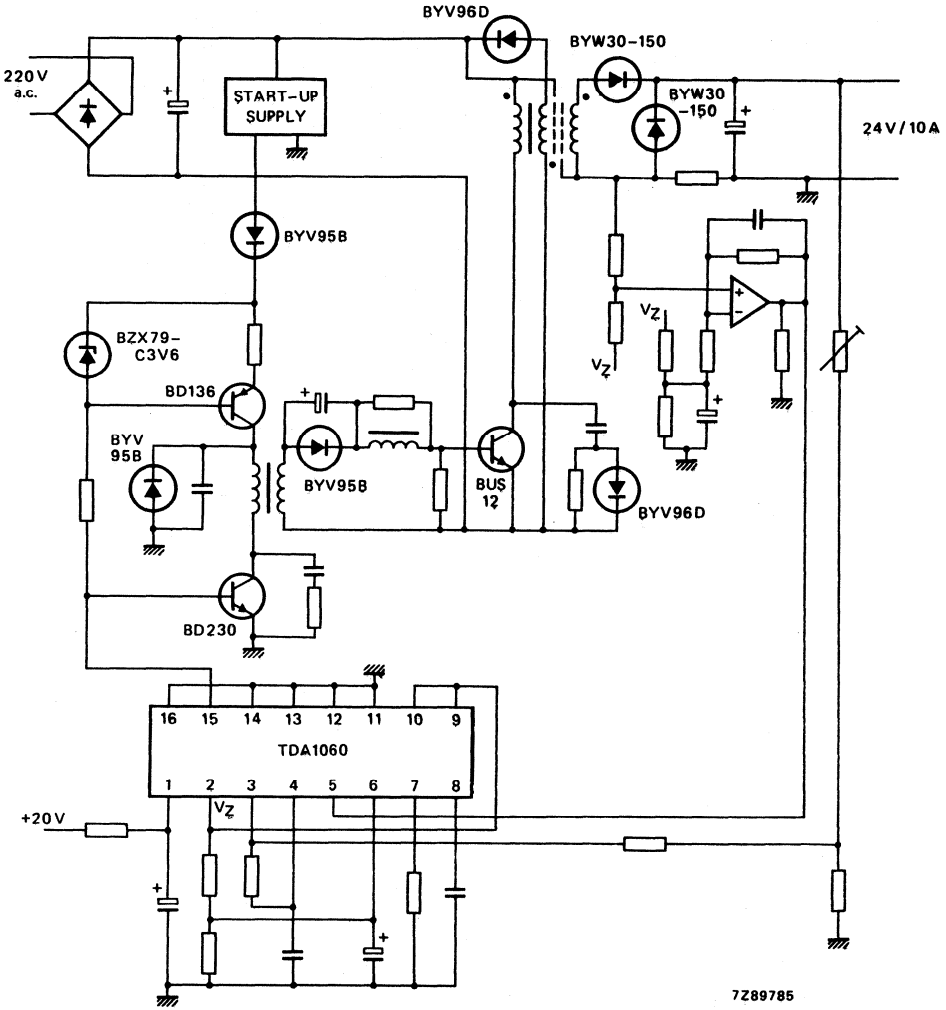


Fig. 10 Application of the TDA1060 in a 24 V, 240 W SMPS with forward converter.

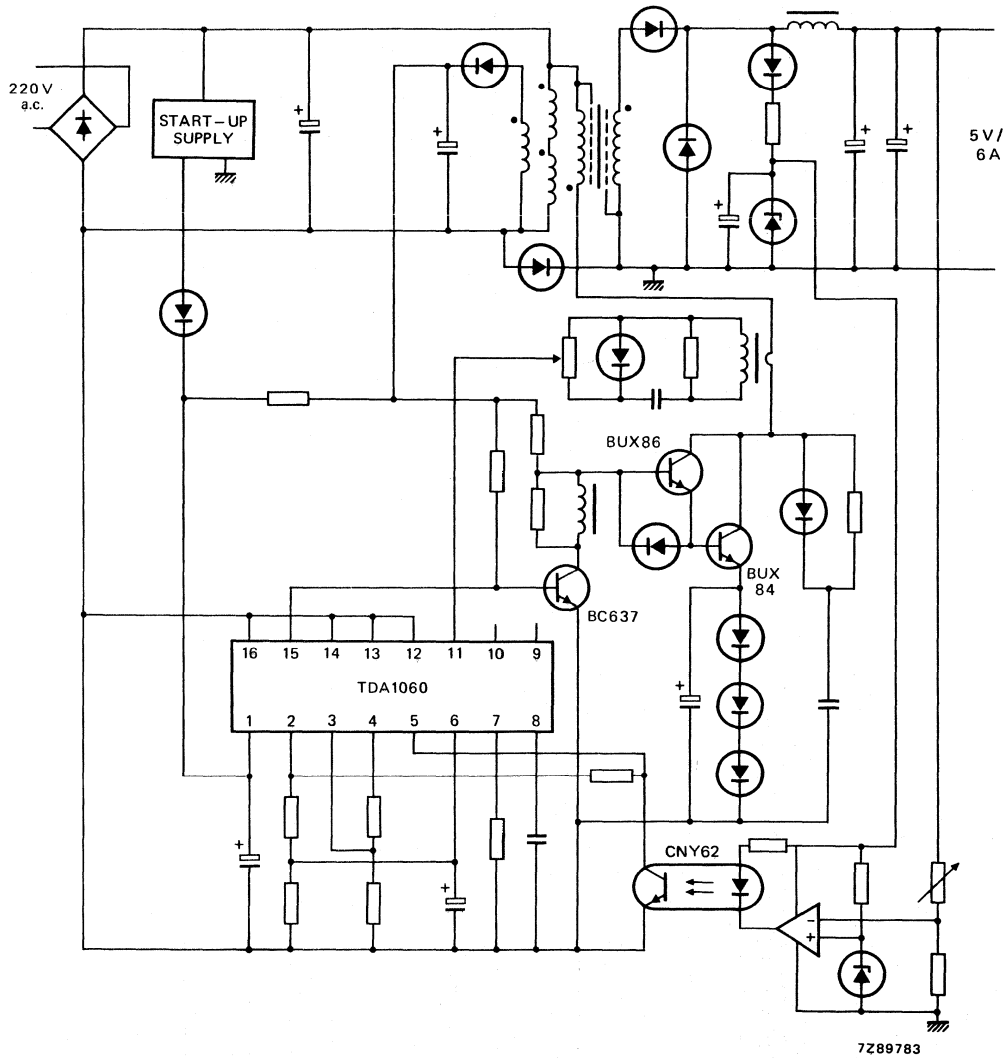


Fig. 11 Application of the TDA1060 in a 5 V, 30 W SMPS with forward converter and with an optocoupler CNY62 for voltage separation.

APPLICATION INFORMATION SUPPLIED UPON REQUEST.

CONTROL CIRCUIT FOR SMPS

GENERAL DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g. a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

Features

- Suited for frequency and duty factor regulation.
- Suited for flyback converters and forward converters.
- Wide frequency range.
- Adjustable input sensitivity.
- Adjustable minimum frequency or maximum duty factor limit.
- Adjustable overcurrent protection limit.
- Supply voltage out-of-range protection.
- Slow-start facility.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	14 V
Supply current	I_{CC}	max.	13 mA
Output pulse repetition frequency range	f_o	1 Hz to	100 kHz
Output current LOW	I_{OL}	max.	1 A
Operating ambient temperature range	T_{amb}	−25 to +	125 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

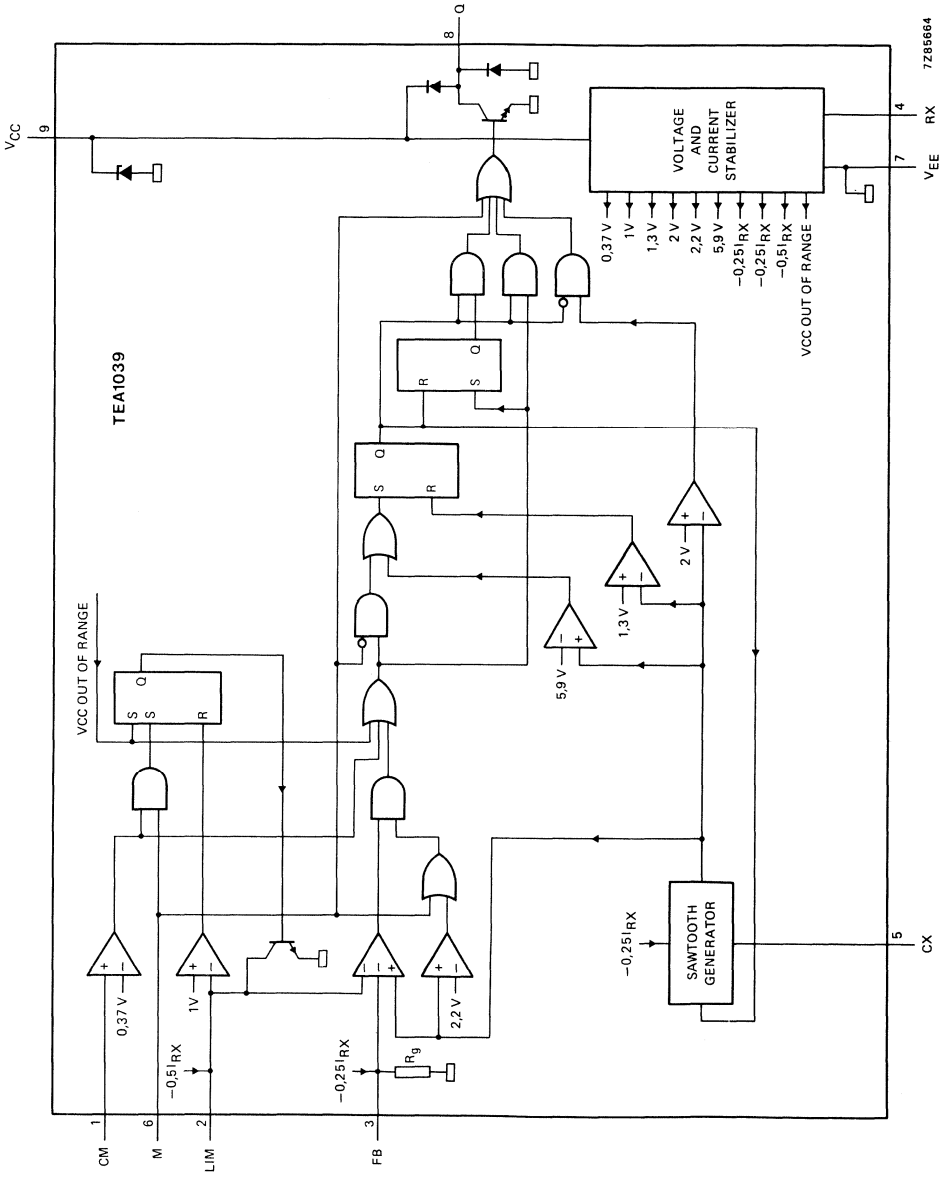


Fig. 1 Block diagram.

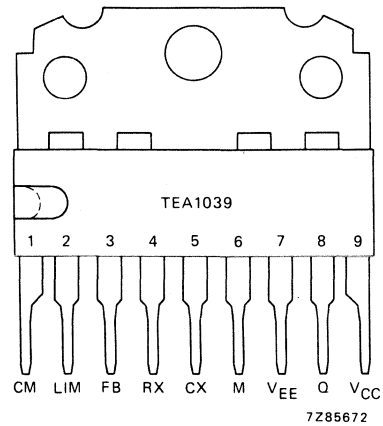


Fig. 2 Pinning diagram.

PINNING

1	CM	overcurrent protection input
2	LIM	limit setting input
3	FB	feedback input
4	RX	external resistor connection
5	CX	external capacitor connection
6	M	mode input
7	V_{EE}	common
8	Q	output
9	V_{CC}	positive supply connection

FUNCTIONAL DESCRIPTION

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e. when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

Supply V_{CC} (pin 9)

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary d.c. voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal V_{CC} out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

Mode input M (pin 6)

The circuit works in the frequency regulation mode when the mode input M is connected to ground (V_{EE}, pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

FUNCTIONAL DESCRIPTION (continued)

Oscillator resistor and capacitor connections RX and CX (pins 4 and 5)

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (pin 5) and ground (V_{EE}, pin 7), and an external resistor R_4 connected between the RX connection (pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Fig. 4). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2 V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2,2 V. As soon as the capacitor voltage reaches 5,9 V the capacitor is discharged rapidly to 1,3 V and a new cycle is initiated (see Figs 5 and 6).

For voltages on the FB and LIM inputs lower than 2,2 V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1,3 V to 5,9 V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figs 7 and 8). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

Feedback input FB (pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

Limit setting input LIM (pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from f_{max} to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

Overcurrent protection input CM (pin 1)

A voltage on the CM input exceeding 0,37 V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

Output Q (pin 8)

The output is an open-collector n-p-n transistor, only capable of sinking current. It requires an external resistor to drive an n-p-n transistor in the SMPS (see Figs 9 and 10).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Fig. 3).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, voltage source	V_{CC}	−0,3 to +20	V
Supply current range, current source	I_{CC}	−30 to +30	mA
Input voltage range, all inputs	V_I	−0,3 to +6	V
Input current range, all inputs	I_I	−5 to +5	mA
Output voltage range	V_{8-7}	−0,3 to +20	V
Output current range			
output transistor ON	I_8	0 to 1	A
output transistor OFF	I_8	−100 to + 50	mA
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range (see Fig. 3)	T_{amb}	−25 to +125	°C
Power dissipation (see Fig. 3)	P_{tot}	max. 2	W

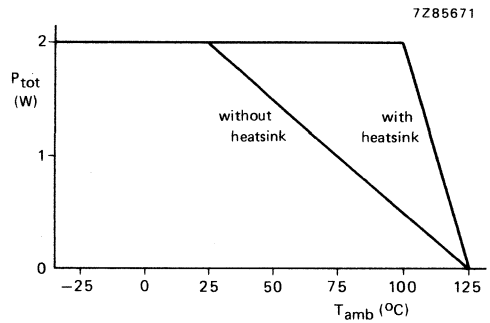


Fig. 3 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 9)					
Supply voltage, operating	V_{CC}	11	14	20	V
Supply current					
at V_{CC} = 11 V	I_{CC}	–	7,5	11	mA
at V_{CC} = 20 V	I_{CC}	–	9	12	mA
variation with temperature	$\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	–	–0,3	–	%/K
Supply voltage, internally limited					
at I_{CC} = 30 mA	V_{CC}	23,5	–	28,5	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	18	–	mV/K
Low supply threshold voltage	V_{CCmin}	9	10	11	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	–5	–	mV/K
High supply threshold voltage	V_{CCmax}	21	23	24,6	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	10	–	mV/K
Feedback input FB (pin 3)					
Input voltage for duty factor = 0; M input open	V_{3-7}	0	–	0,3	V
Internal reference current	$-I_{FB}$	–	0,5 I_{RX}	–	mA
Internal resistor R_g	R_g	–	130	–	kΩ
Limit setting input LIM (pin 2)					
Threshold voltage	V_{2-7}	–	1	–	V
Internal reference current	$-I_{LIM}$	–	0,25 I_{RX}	–	mA
Overcurrent protection input CM (pin 1)					
Threshold voltage	V_{1-7}	300	370	420	mV
variation with temperature	$\Delta V_{1-7}/\Delta T$	–	0,2	–	mV/K
Propagation delay, CM input to output	t_{PHL}	–	500	–	ns

	symbol	min.	typ.	max.	unit
Oscillator connections RX and CX (pins 4 and 5)					
Voltage at RX connection at $-I_4$ = 0,15 to 1 mA	V_{4-7}	6,2	7,2	8,1	V
variation with temperature	$\Delta V_{4-7}/\Delta T$	–	2,1	–	mV/K
Lower sawtooth level	V_{LS}	–	1,3	–	V
Threshold voltage for output H to L transition in F mode	V_{FT}	–	2	–	V
Threshold voltage for maximum frequency in F mode	V_{FM}	–	2,2	–	V
Higher sawtooth level	V_{HS}	–	5,9	–	V
Internal capacitor charging current, CX connection	$-I_{CX}$	–	0,25 I_{RX}	–	mA
Oscillator frequency (output pulse repetition frequency)	f_o	1	–	10^5	Hz
Minimum frequency in F mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Maximum frequency in F mode, initial deviation	$\Delta f/f$	−20	–	+20	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	−0,16	–	%/K
Output LOW time in F mode, initial deviation	$\Delta t/t$	−25	–	+25	%
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Pulse repetition frequency in D mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Minimum output LOW time in D mode at C_5 = 3,6 nF	t_{OLmin}	–	1	–	µs
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Output Q (pin 8)					
Output voltage LOW at I_8 = 100 mA	V_{8-7}	–	0,8	1,2	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	1,5	–	mV/K
Output voltage LOW at I_8 = 1 A	V_{8-7}	–	1,7	2,1	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	−1,4	–	mV/K

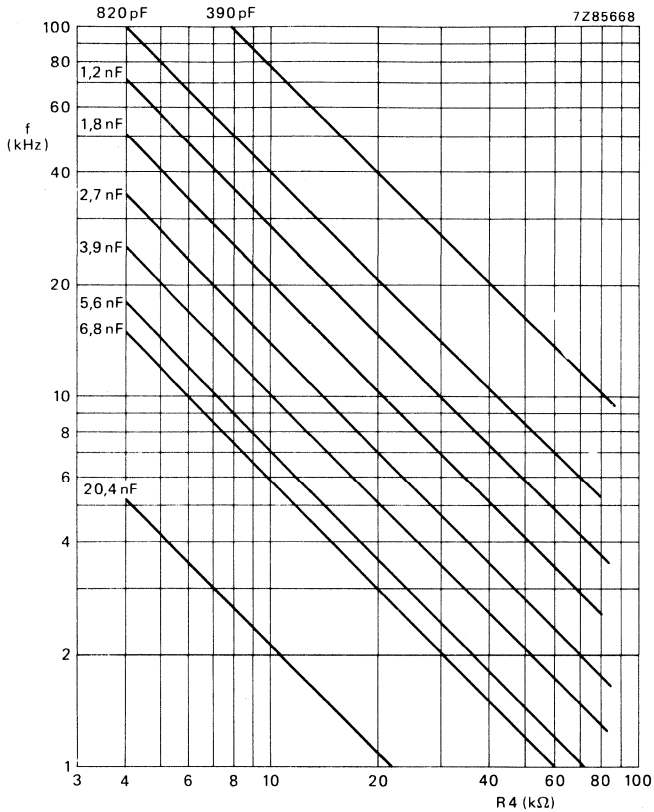


Fig. 4 Minimum pulse repetition frequency in the frequency regulation mode, and working pulse repetition frequency in the duty factor regulation mode, as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

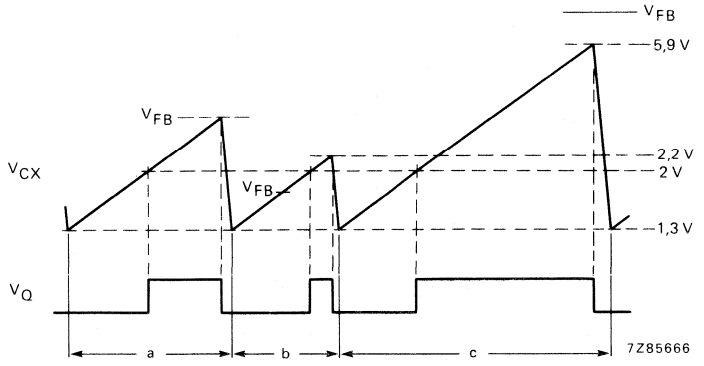


Fig. 5 Timing diagram for the frequency regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for three combinations of input signals. *a:* The voltages on inputs FB or LIM are between 2,2 V and 5,9 V. The circuit is in its normal regulation mode. *b:* The voltage on input FB or input LIM is lower than 2,2 V. The circuit works at its maximum frequency. *c:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit works at its minimum frequency.

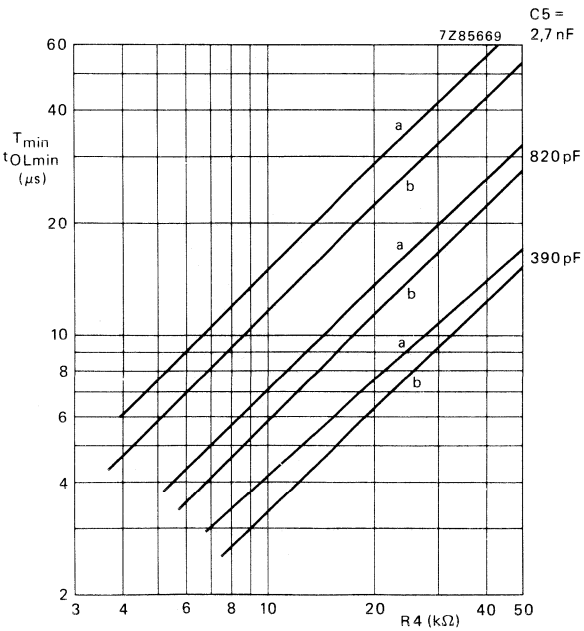


Fig. 6 Minimum output pulse repetition time T_{min} (curves a) and minimum output LOW time t_{OLmin} (curves b) in the frequency regulation mode as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

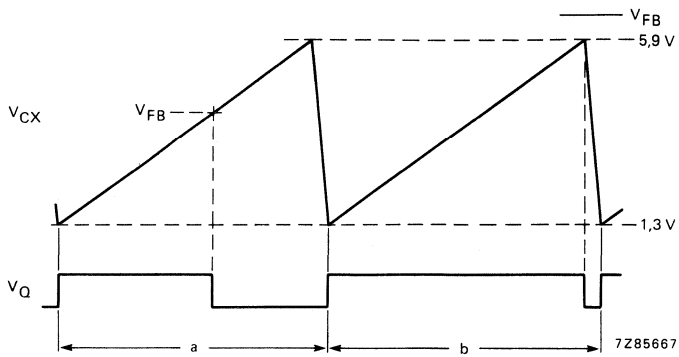


Fig. 7 Timing diagram for the duty factor regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for two combinations of input signals. *a:* The voltages on inputs FB or LIM are below 5,9 V. The circuit is in its normal regulation range. *b:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

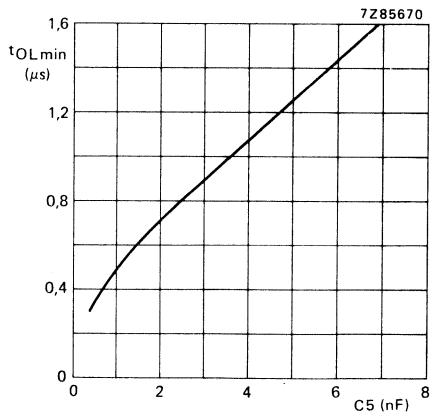


Fig. 8 Minimum output LOW time t_{OLmin} in the duty factor regulation mode as a function of external capacitor C5 connected between CX and ground. In this mode the minimum output LOW time is independent of R4 for values of R4 between 4 kΩ and 80 kΩ.

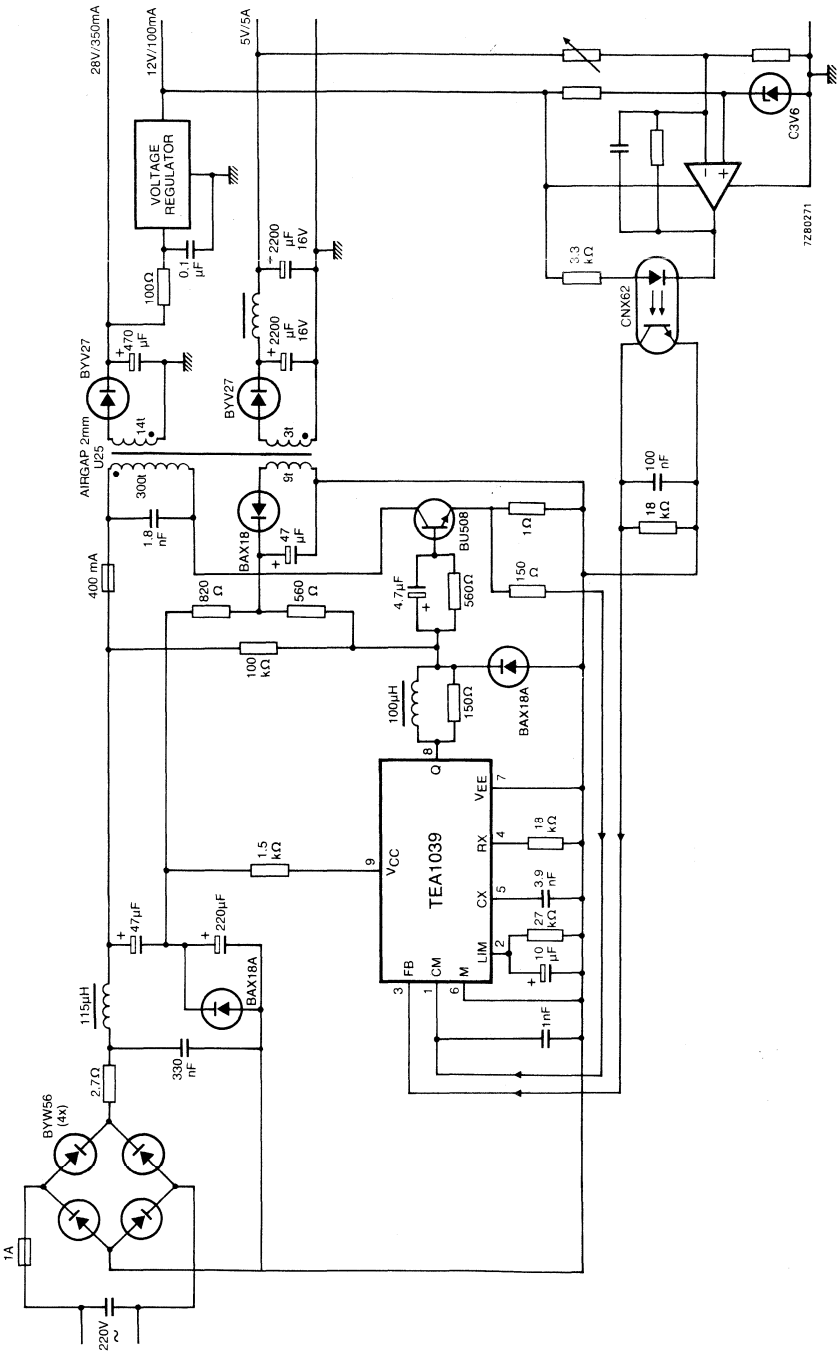


Fig. 9 Typical application of the TEA1039 in a variable-frequency flyback converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

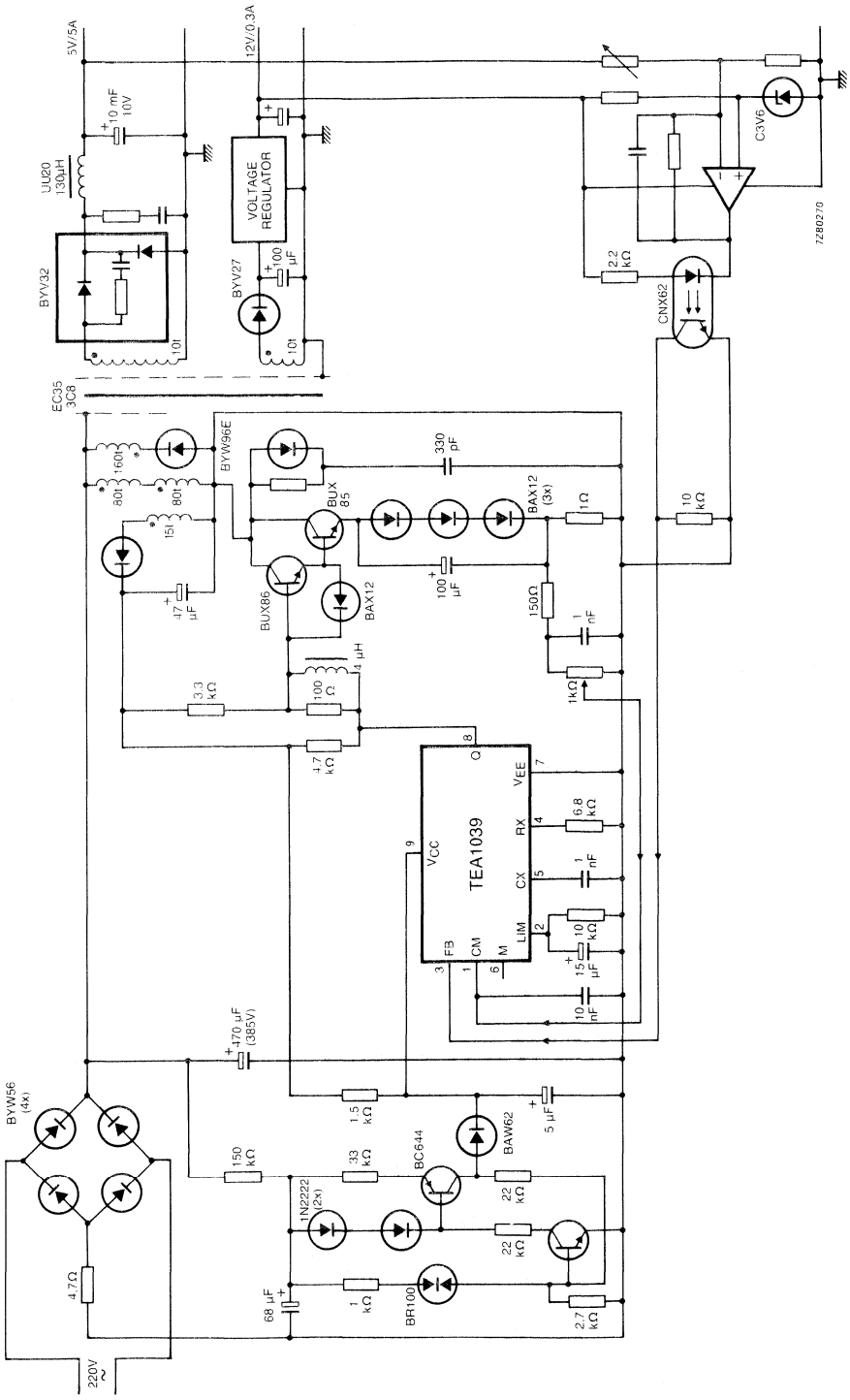


Fig. 10 Typical application of the TEA1039 in a fixed-frequency, variable duty factor forward converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

UC1842
UC2842
UC3842
Current-Mode PWM Controller

Product Specification

DESCRIPTION

The UC1842 family of control ICs provides in an 8-Pin mini-DIP the necessary features to implement off-line, fixed-frequency current-mode control schemes with a minimal external parts count. This technique results in improved line regulation, enhanced load response characteristics, and a simpler, easier to design control loop. Topological advantages include inherent pulse-by-pulse current limiting.

Protection circuitry includes built-in undervoltage lock-out and current limiting. Other features include fully-latched operation, a 1% trimmed bandgap reference, and start-up current less than 1mA.

These devices feature a totem-pole output designed to source and sink high peak current from a capacitive load, such as the gate of a power MOSFET. Consistent with N-channel power devices, the output is low in the OFF-state.

FEATURES

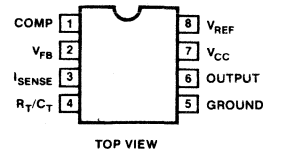
- **Low start-up current (⩽ 1mA)**
- **Automatic feed-forward compensation**
- **Pulse-by-pulse current limiting**
- **Enhanced load response characteristics**
- **Undervoltage lock-out with hysteresis**
- **Double pulse suppression**
- **High current totem-pole output**
- **Internally-trimmed bandgap reference**
- **400kHz operation, guaranteed min**

APPLICATIONS

- **Off-line switched mode power supplies**
- **DC-to-DC converters**

PIN CONFIGURATIONS

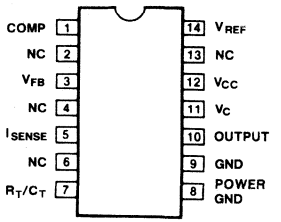
N Package



TOP VIEW

CD-3473S

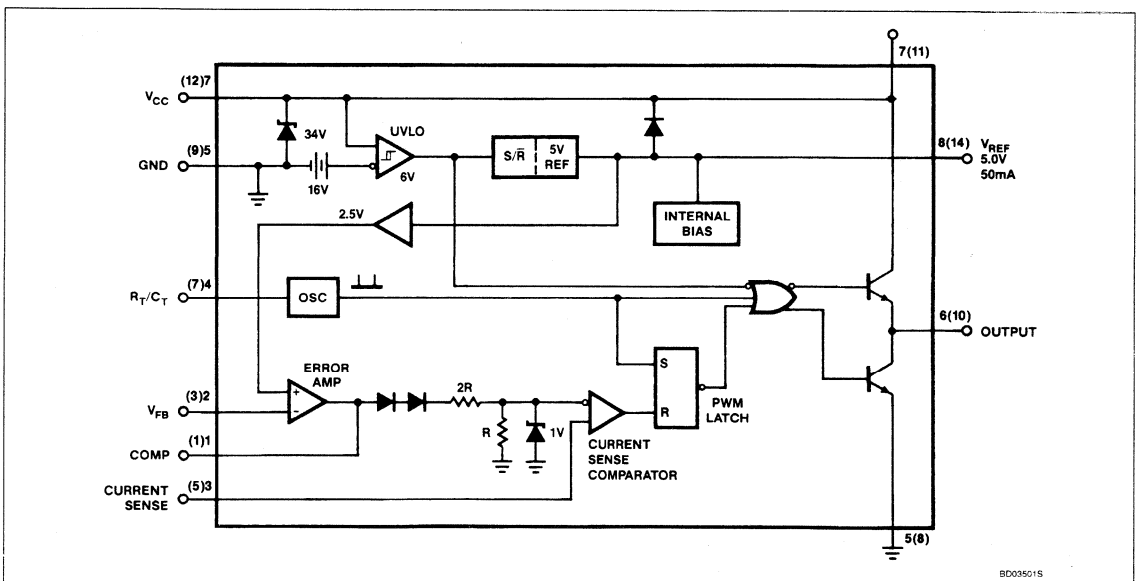
D Package



TOP VIEW

CD15140S

BLOCK DIAGRAM



NOTE:
Pin numbers in parentheses refer to the D package.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	UC3842N
14-Pin Plastic SO	0 to +70°C	UC3842D
8-Pin Plastic DIP	-40 to +85°C	UC2842N
14-Pin Plastic SO	-40 to +85°C	UC2842D
8-Pin Plastic DIP	-55 to +125°C	UC1842N

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (I_{CC} < 30mA)		Self-Limiting
V_{CC}	Supply voltage (low impedance source)	30	V
I_{OUT}	Output current[2, 3]	±1	A
	Output energy (capacitive load)	5	μJ
	Analog inputs (Pin 2, Pin 3)	-0.3 to 6.3	V
	Error amp output sink current	10	mA
P_D	Power dissipation at $T_A \leq 70°C$ (derate 12.5mW/°C for $T_A > 70°C$)[2]	1	W
T_{STG}	Storage temperature range	-65°C to +150	°C
T_{SOLD}	Lead temperature (soldering, 10sec max)	300	°C

NOTES:
1. All voltages are with respect to Pin 5; all currents are positive into the specified terminal.
2. See section in application note on "Power Dissipation Calculation".
3. This parameter is guaranteed, but not 100% tested in production.

DC AND AC ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $-55 \leq T_J \leq 125°C$ for UC1842/43; $-25 \leq T_J \leq 85°C$ for UC2842/43; $0 \leq T_J \leq 70°C$ for UC3842/43; $V_{CC} = 15$[4]; $R_T = 10k\Omega$; $C_T = 3.3nF$.)

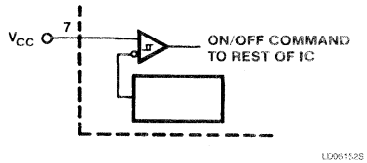
SYMBOL	PARAMETER	TEST CONDITIONS	UC1842 UC2842			UC3842			UNIT
			Min	Typ	Max	Min	Typ	Max	
Reference section									
V_{OUT}	Output voltage	$T_J = 25°C$, $I_O = 1mA$	4.95	5.00	5.05	4.90	5.00	5.10	V
	Line regulation	$12 \leq V_{IN} \leq 25V$		6	20		6	20	mV
	Load regulation	$1 \leq I_O \leq 20mA$		6	25		6	25	mV
	Temp. stability[1]			0.2	0.4		0.2	0.4	mV/°C
	Total output variation[1]	Line, load, temp.	4.90		5.10	4.82		5.18	V
V_{NOISE}	Output noise voltage[1]	$10Hz \leq f \leq 10kHz$, $T_J = 25°C$		50			50		μV
	Long-term stability[1]	$T_J = 125°C$, 1000 Hrs.		5	25		5	25	mV
	Output short-circuit	$T_J = 25°C$	−30	−100	−130	−30	−100	−130	mA
	Output short-circuit	$-55 < T_J \leq 0°C$	−30	−100	−180	−30	−100	−180	mA
Oscillator section									
	Initial accuracy	$T_J = 25°C$	47	52	57	47	52	57	kHz
	Voltage stability	$12 \leq V_{CC} \leq 25V$		0.2	1		0.2	1	%
	Temp. stability[1]	$T_{MIN} \leq T_J \leq T_{MAX}$		5			5		%
	Amplitude	$V_{PIN\ 4}$ peak-to-peak		1.7			1.7		V
Error amp section									
	Input voltage	V Pin 1 = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
I_{BIAS}	Input bias current			−0.3	−1		−0.3	−2	μA
A_{VOL}		$2 \leq V_O \leq 4V$	65	90		65	90		dB
	Unity gain bandwidth[1]	$T_J = 25°C$	0.7	1		0.7	1		MHz
	Unity gain bandwidth	$T_{MIN} < T_J < T_{MAX}$	0.5			0.5			MHz
PSRR	Power supply rejection ratio	$12 \leq V_{CC} \leq 25V$	60	70		60	70		dB
I_{SINK}	Output sink current	$V_{PIN\ 2} = 2.7V$, $V_{PIN\ 1} = 1.1V$	2	6		2	6		mA
I_{SOURCE}	Output source current	$V_{PIN\ 2} = 2.3V$, $V_{PIN\ 1} = 5V$	−0.5	−0.8		−0.5	−0.8		mA
	V_{OUT} High	$V_{PIN\ 2} = 2.3V$, $R_L = 15k$ to ground	5	6		5	6		V
	V_{OUT} Low	$V_{PIN\ 2} = 2.7V$, $R_L = 15k$ to Pin 8		0.7	1.1		0.7	1.1	V
Current sense section									
	Gain[2, 3]		2.85	3	3.15	2.85	3	3.15	V/V
	Maximum input signal[2]	$V_{PIN\ 1} = 5V$	0.9	1	1.1	0.9	1	1.1	V
PSRR	Power supply rejection ratio[2]	$12 \leq V_{CC} \leq 25V$		70			70		dB
I_{BIAS}	Input bias current			−2	−10		−2	−10	μA
	Delay to output[1]			150	300		150	300	ns

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) (Unless otherwise stated, these specifications apply for $-55 \leqslant T_J \leqslant 125°C$ for UC1842/43; $-25 \leqslant T_J \leqslant 85°C$ for UC2842/43; $0 \leqslant T_J \leqslant 70°C$ for UC3842/43; $V_{CC} = 15V$[4]; $R_T = 10k\Omega$; $C_T = 3.3nF$.)

SYMBOL	PARAMETER	TEST CONDITIONS	UC1842/43 UC2842/43			UC3842/43			UNIT
			Min	Typ	Max	Min	Typ	Max	
Output section									
I_{OL}	Output Low-Level	$I_{SINK} = 20mA$		0.1	0.4		0.1	0.4	V
		$I_{SINK} = 200mA$		1.5	2.2		1.5	2.2	V
I_{OH}	Output High-Level	$I_{SOURCE} = 20mA$	13	13.5		13	13.5		V
		$I_{SOURCE} = 200mA$	12	13.5		12	13.5		V
t_R	Rise time	$C_L = 1nF$		50	150		50	150	ns
t_F	Fall time	$C_L = 1nF$		50	150		50	150	ns
Undervoltage lockout section									
	Start threshold	X842	15	16	17	14.5	16	17.5	V
		X843	7.8	8.4	9.0	7.8	8.4	9.0	V
	Min. operating voltage after turn on	X842	9	10	11	8.5	10	11.5	V
		X843	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM section									
	Maximum duty cycle	X842/43	93	97	100	93	97	100	%
	Minimum duty cycle				0			0	%
Total standby current									
	Start-up current			0.5	1		0.5	1	mA
I_{CC}	Operating supply current	$V_{PIN\ 2} = V_{PIN\ 3} = 0V$		11	17		11	17	mA
	V_{CC} zener voltage	$I_{CC} = 25mA$		34			34		V
Maximum operating frequency section									
	Maximum operating frequency for all functions operating cycle-by-cycle		400			400			kHz

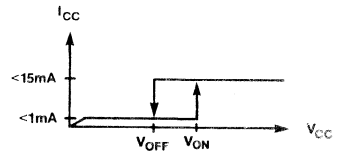
NOTES:
1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch with $V_{PIN\ 2} = 0$.
3. Gain defined as: $A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}$; $0 \leqslant V_{PIN\ 3} \leqslant 0.8V$.

UNDERVOLTAGE LOCKOUT



LD06152S

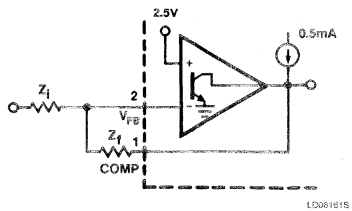
	UC1842
V_{ON}	16V
V_{OFF}	10V



LD06153S

NOTE:
During Undervoltage Lock-Out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with output leakage current.

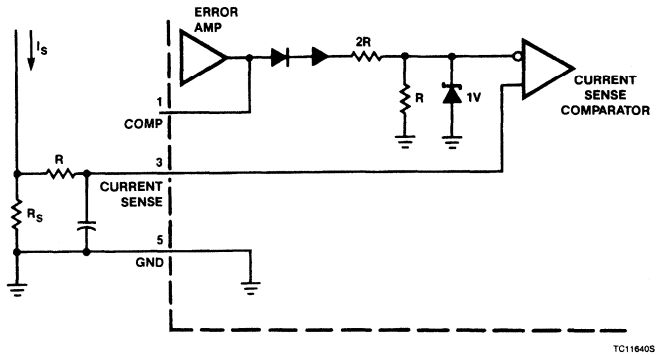
ERROR AMP CONFIGURATION



LD06161S

NOTE:
Error AMP can source or sink up to 0.5mA.

CURRENT SENSE CIRCUIT



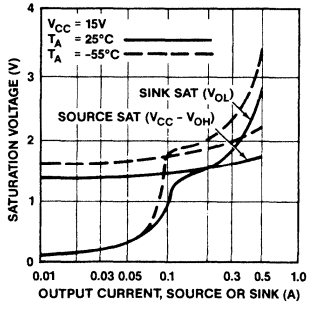
NOTE:
Peak current (I_S) is determined by the formula:

$$I_{S\ MAX} \approx \frac{1.0V}{R_S}$$

A small RC filter may be reqiured to suppress switch transients.

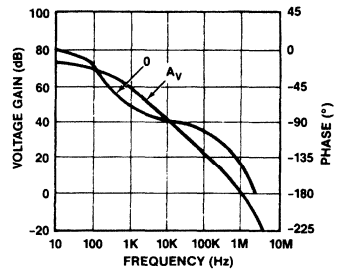
TYPICAL PERFORMANCE CHARACTERISTICS

Output Saturation Characteristics



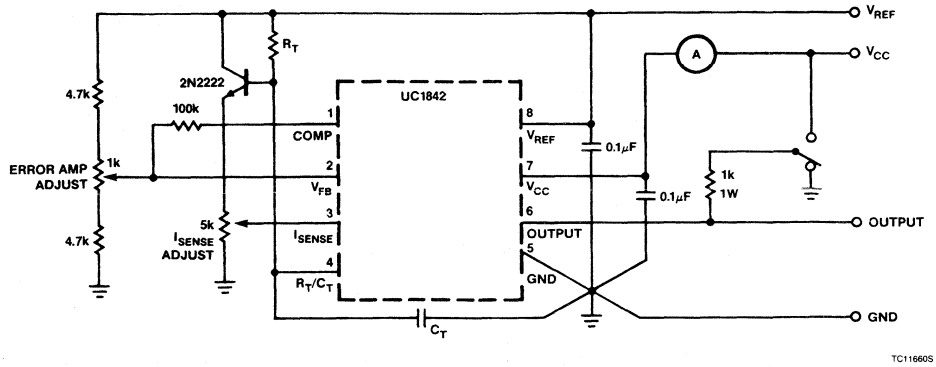
OP07790S

Error Amplifier Open-Loop Frequency Response



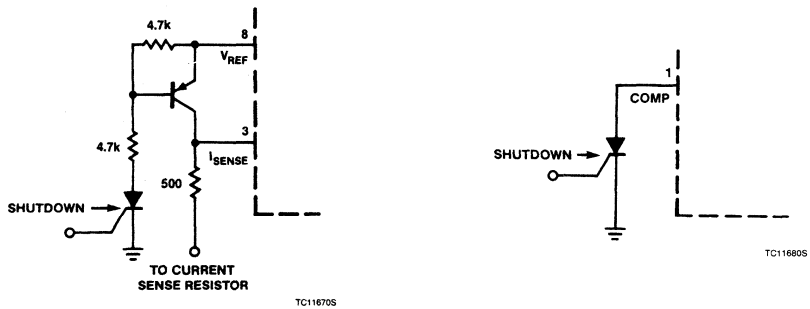
OP07800S

OPEN-LOOP LABORATORY TEST FIXTURE



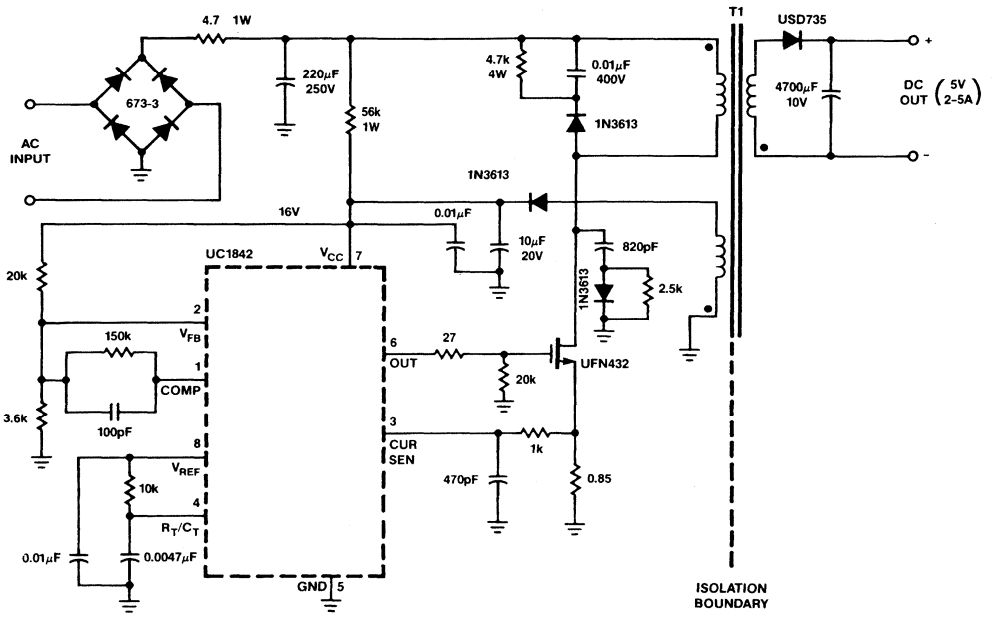
NOTE:
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Pin 3.

SHUTDOWN TECHNIQUES



NOTE:
Shutdown of the UC1842 can be accomplished by two methods; either raise Pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to Block Diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at Pins 1 and/or 3 is removed. In the examples shown, an externally-latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold (10V). At this point all internal bias is removed, allowing the SCR to reset.

OFF-LINE FLYBACK REGULATOR



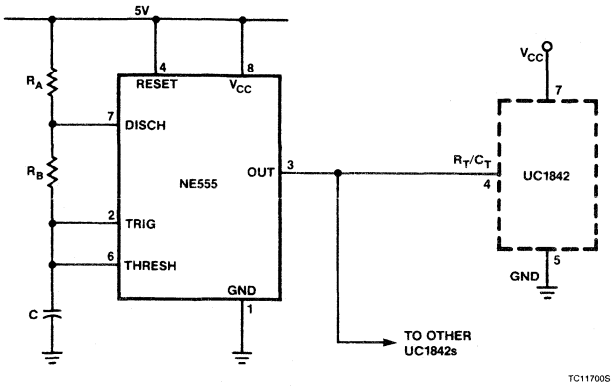
NOTES:
T1: Coilcraft E-4140-B
Primary - 97 turns
single AWG 24
Secondary - 4 turns
4 parallel AWG 22
Control - 9 turns
3 parallel AWG 28

SPECIFICATIONS

Input line voltage:	$90V_{AC}$ to $130V_{AC}$
Input frequency:	50 or 60Hz
Switching frequency:	40kHz± 10%
Output power:	25W maximum
Output voltage:	5V± 5%
Output current:	2 to 5A
Line regulation:	0.01%/V
Load regulation:	8%/A*
Efficiency @ 25 W,	
$V_{IN} = 90V_{AC}$:	70%
$V_{IN} = 130V_{AC}$:	65%
Output short-circuit current:	2.5A average

NOTE:
*This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the UC1842 error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings, and on transformer leakage inductance. For applications requiring better load regulation, a UC1901 Isolated Feedback Generator can be used to directly sense the output voltage.

SYNCHRONIZATION AND MAXIMUM DUTY CYCLE CLAMP



NOTES:

$$f = \frac{1.44}{(R_A + 2R_B)C}$$

$$D_{MAX} = \frac{R_B}{R_A + 2R_B}$$

AN122
NE5560 Push-Pull Regulator Application

Application Note

INTRODUCTION

NE/SE5560 Push-Pull Regulator

This application describes the use of the Signetics NE/SE5560 adapted to function as a push-pull switched-mode regulator, as shown in Figures 1 and 2.

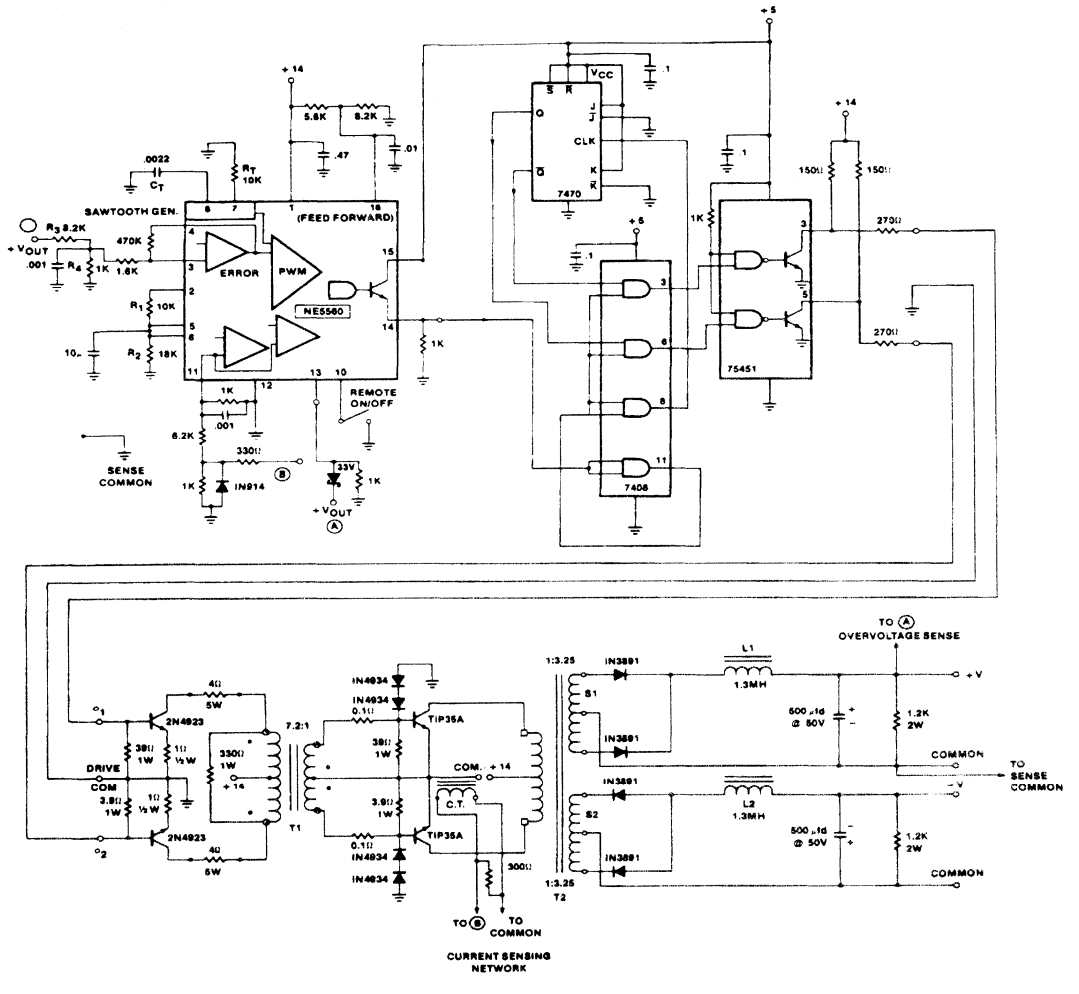
Input voltage range is +12 to +18V for a nominal output of +30 and −30V at a maximum load current of 1A with an average efficiency of 81%.

Features include feed-forward input compensation, cycle-by-cycle drive current protection and overvoltage sensing, line regulation (to positive output) < 1% for an input range of +13 to +18V and load regulation to positive output of < 3% for $\Delta I_L(+)$ of 0.1 to 1 Amp.

The main pulse-width modulator operates to 48kHz with power switching at 24kHz.

NE5560 Push-Pull Regulator Application

AN122



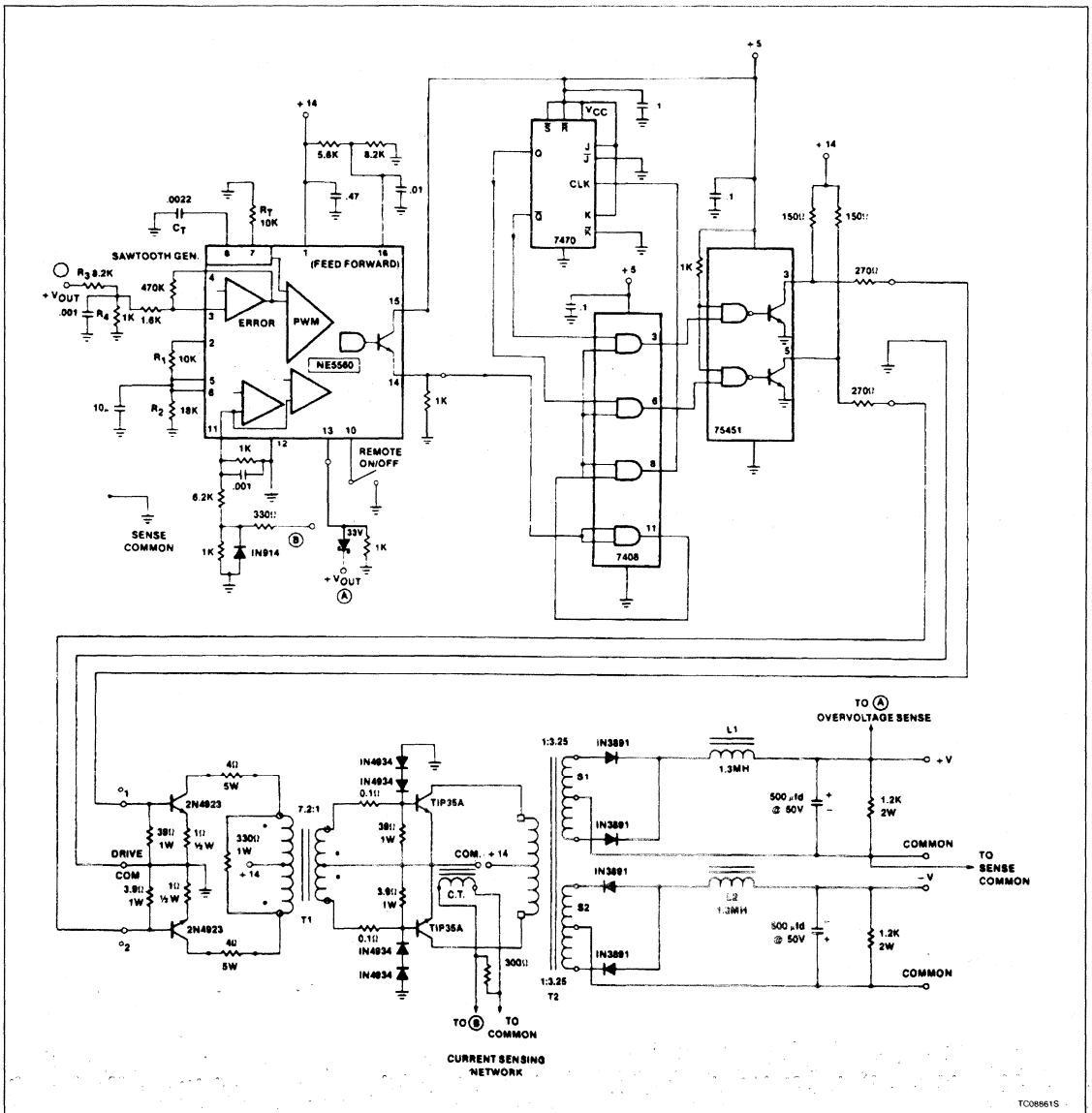
NOTE:
Power ground and signal ground must be kept separated.

T_1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622 3C8 material
C.T. = 50T #26 on Ferroxcube 2616 core (3C8) F2D bobbin
T_2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22
Core = Ferroxcube 4229 3C8 material
L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material

Figure 1. NE/SE5560 Push-Pull Switched-Mode Regulated Supply with CMOS Drive Conversion Logic

NE5560 Push-Pull Regulator Application

AN122



NOTE:
Power ground and signal ground must be kept separated.

T_1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622 3C8 material
C.T. = 50T #26 on Ferroxcube 2616 core (3C8) F2D bobbin
T_2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22
Core = Ferroxcube 4229 3C8 material
L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material

Figure 2. NE/SE5560 Push-Pull Switched-Mode Regulated Supply with TTL Drive Conversion Logic

AN123
NE5561 Applications

Application Note

INTRODUCTION

5V, 0.5A Buck Regulator Operates From 15V

The converter design shows how simple it is to derive a TTL supply from a system supply of 15V (see Figure 1). The NE5561 drives a 2N4920 PNP transistor directly to provide switching current to the inductor. Overall line regulation is excellent and covers a range of 12V to 18V with minimal change (< 10mV) in the output operating at full load.

As with all NE5561 circuits, the auxiliary slow start and δ_{MAX} circuit is required, as evidenced by Q1. The δ_{MAX} limit may be calculated by using the relationship.

$$\frac{R2}{R1 + R2}(8.2V) = V\delta_{MAX}$$

The maximum duty cycle is then determined from the pulse-width modulator transfer graph, and R1, R2 are defined from the desired conditions. (See Figure 2.)

NE5561 Boost Converter With Output Variable (18V to 30V, 0.2A)

The circuit shown uses the NE5561 SMPS controller in a non-isolated boost converter operating from a 15V line. The addition of three transistors and one diode is necessary to complete the design (see Figure 3).

Operation is as follows. Q1 is a combination slow start and max duty cycle limit transistor. When power is first applied to the circuit, C7 in a discharged state begins to charge toward the divider voltage, V_δ. This $V_\delta + V_{BE}$ controls the voltage on Pin 4, the error amp output, causing the duty cycle to be limited initially to δ_0, then to gradually approach its normal operating range, δ. The base divider is fed from V_Z, which is nominally 8.2V.

Output regulation starts at the error amplifier, with gain set by R2 (adj) and R5 combination. The error amp is stable for closed loop gain in excess of 40dB (×100), for which the regulation will be approximately 1%. C4 is added to the output to insure stability at gain below 40dB. C4 creates a dominant pole at approximately 1kHz, descending at 6dB per octave to unity near 1MHz. Input to the error amplifier is referenced to 3.75V and must reach this reference level for the output of the NE5561 to be active. Output voltage is then the quantity 3.75V times the divider ratio from V_{OUT} to Pin 3 as set by R2.

If the ratio is, for instance, 10:1, the output will be ≃ 37V. If the ratio is 5:1, the output will be ≃ 18.5V, etc.

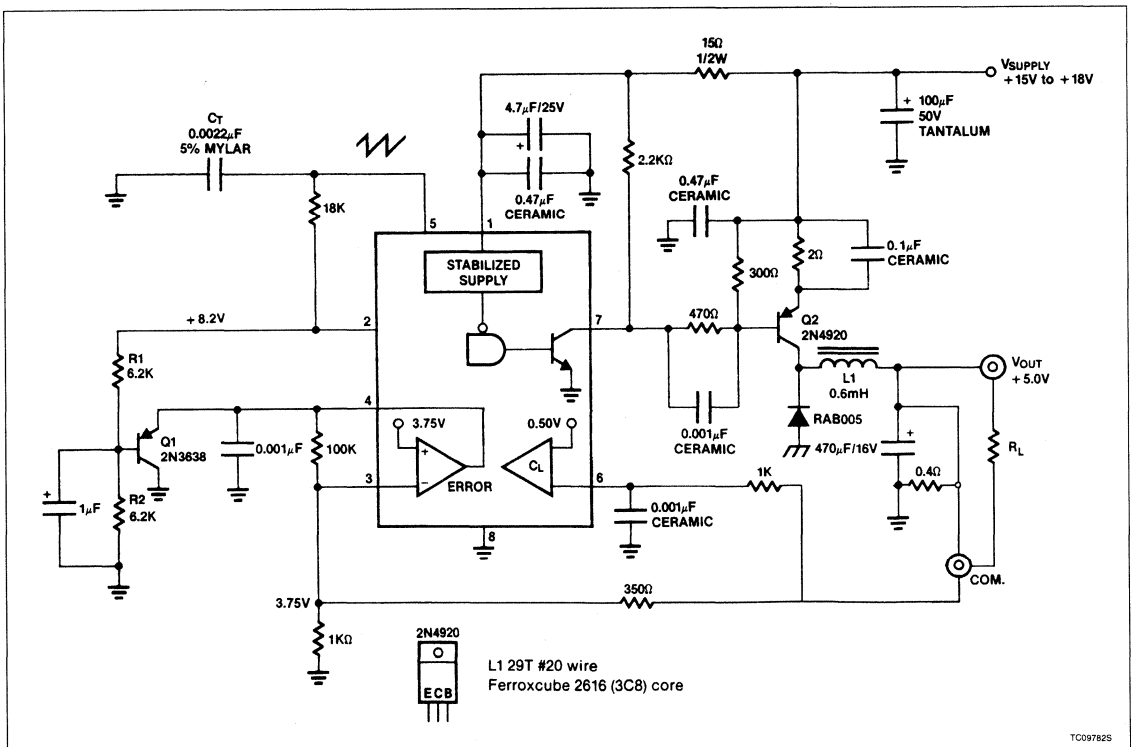


Figure 1. NE5561 5V/0.5A Buck Converter

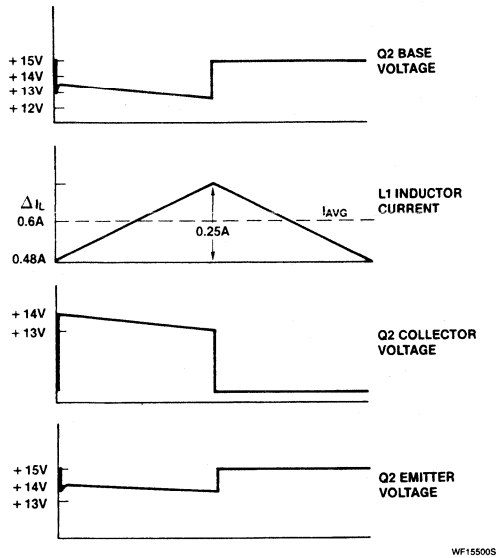
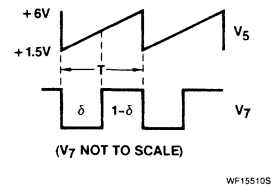
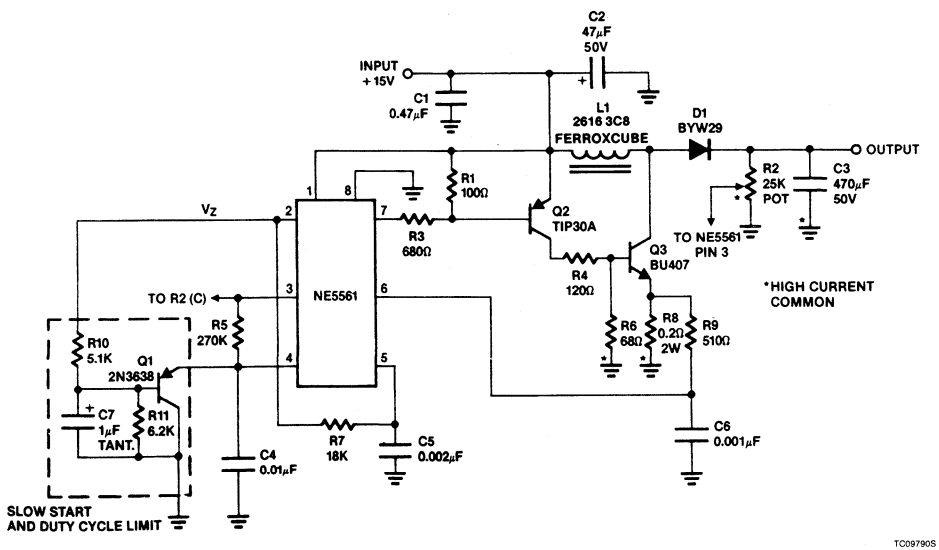


Figure 2. Typical Buck Converter Waveforms

Output to Q2 base is a square wave of variable duty cycle as determined by load demand. The internal transistor is open-collector and must have a pull-up resistance; in this application the base circuit of Q2. The duty cycle δ is a fraction between 0 and 1. The actual on time is proportional then to $\delta \times T$, where T is the period of the free-running frequency of the sawtooth generator internal to the NE5561. Frequency is set by the RC combination, R7 $\times$ C5 with charging current supplied from V_Z (8.2V). The stabilizing effect of the internal zener supply gives a constant frequency. The sawtooth waveform is related to duty cycle as shown below.





NOTES:
C5 is the timing capacitor
L1 is Ferroxcube 2616
3C8 with 14 turns of #18 enameled wire (0.14 mH)

$$\delta f_{MAX} \text{ is a function of } f\left[\frac{R11}{R10+R11}(V_Z)+V_{BE}\right]$$

Figure 3. DC-to-DC SMPS Using NE5561 Variable 18V to 30V Out at 0.2A

Q3 is switched on during the saturated portion of the output waveform from Pin 7 of the NE5561, termed δ, and is switched off during the remainder of the cycle $(1 - \delta)$.

The sawtooth frequency is set at approximately 22kHz in this example. The NE5561 is capable of operation to 100kHz, however.

Pin 6 of the NE5561 operates an overcurrent protective feature which resets the output on Pin 7 if the instantaneous Pin 6 voltage exceeds 0.50V. In this case, R8 determines the peak current of Q3 emitter circuit prior to shutdown. The operation of the overcurrent circuit is on a pulse-to-pulse basis, returning to normal as soon as the Pin 6 voltage falls below 0.50V. As is noted, a small degree of filtering is needed to eliminate short switching transient, allowing only the primary current wave form to be sensed.

Switching circuit operation proceeds as follows. Q3 turns on, causing magnetization current to begin increasing in L1, the switching indicator. After initial start-up, C3 is charged to the output, thus with Q3 on, Diode D1 is reverse-biased and does not conduct during the duty cycle, δ. C3, the output capacitor, sustains the full load current during this part of the cycle. When Q3 turns off, the magnetic field energy previously stored in L1 is discharged through D1, which is now forward-biased. The output capacitor is incrementally charged, restoring its depleted voltage. The ripple voltage is a function of the size of C3 and its internal resistance. For minimum ripple, a low ESR (Equivalent Series Resistance) capacitor must be used, since previously-mentioned peak load current flows in C3.

Single Transistor 100V, 250mA Buck Converter (Off-Line)

With a single 15V zener diode to limit package dissipation, the NE5561 controller may be operated directly from the rectified AC line. The following example shows the simplicity of such a converter which is capable of a nominal 100V output (see Figure 5). A base drive transformer is used to gain high voltage isolation between the NE5561 and the switching transistor, and to provide adequate base drive. A low power PNP transistor is used in an auxiliary slow-start and duty cycle limiting circuit to prevent over-excitation (Q1).

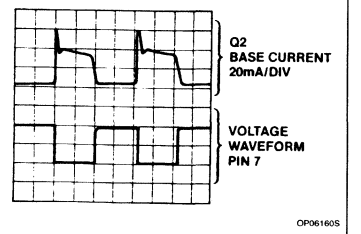


Figure 4. Switching Waveforms

Operation is as follows. Drive from the NE5561 output is fed to the primary of T1, base drive transformer, with a pulse-width modulated signal causing Q2 (BU407) to switch current to inductor, L1. As the current

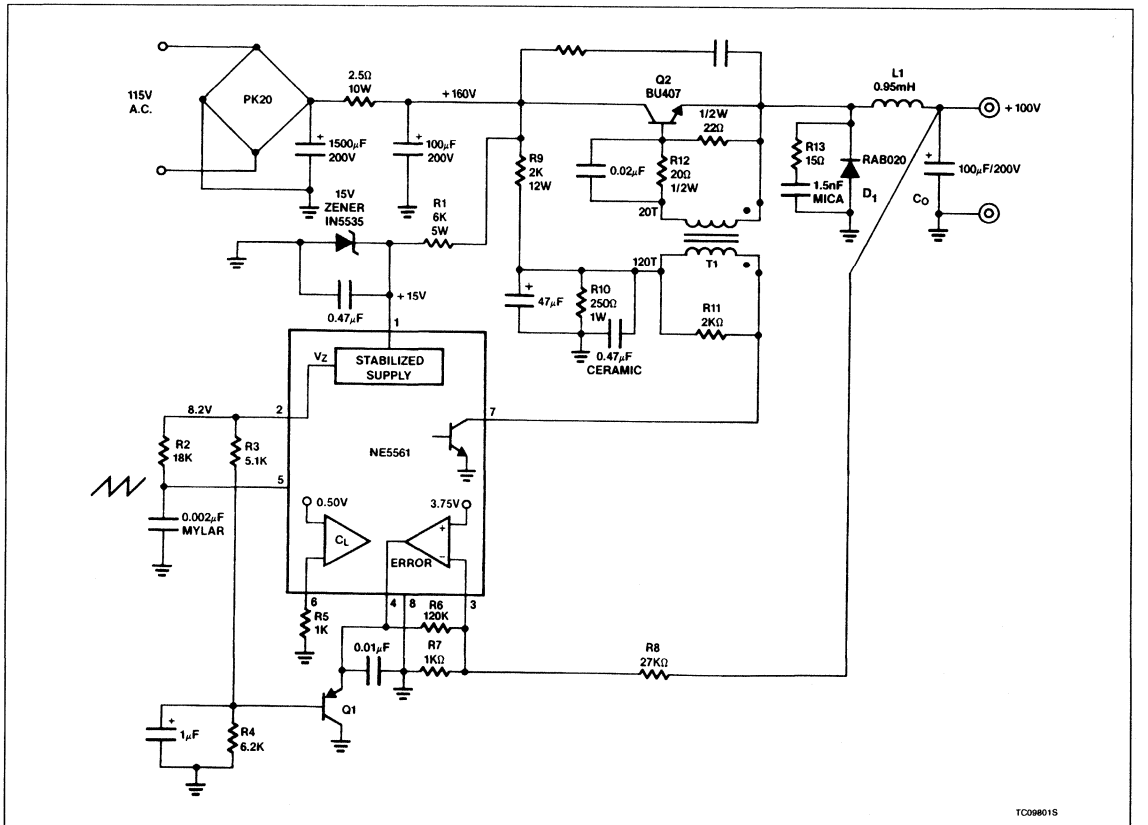


Figure 5. NE5561 100V/0.25A Switched-Mode Converter

builds up, energy is stored in L1, coincident with the saturation period (δ) of the NE5561 output stage. During this period, current also flows through L1 to C_O and the load. When Q2 cuts off, the choke field collapses and D1 conducts as the load is sustained by the inductor-stored energy.

V_{OUT} is sampled by the divider R7 and R8, rising until the junction of the divider is forced to 3.75V. Load variations are thus translated to duty cycle variations to maintain constant voltage at the output. The measured efficiency at 0.5A load is in excess of 72%. Line regulation is good from approximately 93V to 120V.

The base current waveform driving Q2 is shown in Figure 4. This indicates that the BU407 base current rises initially to 60mA to obtain fast turn-on, then settles to about 40mA for the remainder of the duty cycle, δ. Reverse-biasing of the emitter-base junction occurs to enhance turn-off.

Snubber networks are necessary, as shown across Q2 and commutation diode D1, to prevent component failure during fast switching. It is critical that these networks be placed physically adjacent to the respective components they protect, and that low inductance capacitors and resistors be used as snubbers (ceramic or dura mica caps and carbon resistors).

The base drive transformer is constructed using a Ferroxcube 2616-3C8 core, with primary of 120 turns of #26 wire, and 20 turns of #26 on secondary. The primary is wound in a simple solenoidal manner, first on the bobbin, followed by a layer of mylar tape to provide voltage isolation. Next, the secondary winding is added. Primary inductance measures 45mH with a leakage inductance of 120μH. It is important to have sufficient primary inductance to prevent excessive droop in base drive current. Also, leakage reactance must be kept reasonably low to minimize ringing.

DC Motor Drive with Fixed Speed Control

The circuit shown in Figure 7 incorporates a simple switched-mode approach to DC motor control, which is efficient and free of the dissipation problems inherent in linear drives. The NE5561 provides pulse-proportional drive and speed control based on DC tachometer feedback. A simple switching circuit consisting of one transistor (2N4920 PNP) and a commutation diode is used to deliver programmed pulse energy to the motor.

A frequency of approximately 20kHz is used to eliminate audio noise present in some switching drives. The DC tach in this example delivers 2.7V/1000 RPM. Its output is such that negative feedback occurs when this voltage is applied to the error amplifier of the NE5561, Pin 3, through a suitable divider. Note that the voltage to Pin 3 must be 3.75V in order to obtain servo lock. Thus, the divider from the tach output must be appropriate to maintain the proper ratio for speed control to occur.

As shown in the waveform pattern (Figure 6), duty cycle varies directly with load torque demand. No load current is $\simeq$ 0.3A and full load is 0.6A. Current and voltage waveforms at 0.6A are shown in Figure 6. If desired, torque limiting may be set by feeding a derivative of motor return current back to Pin 6 of the NE5561.

Operating range is 12V to 18V input for a tach output nominal variation of less than 20mV, and approximately 4.35V for the divider values shown. The motor is a Globe 100A 565 rated at $12V_{DC}$.

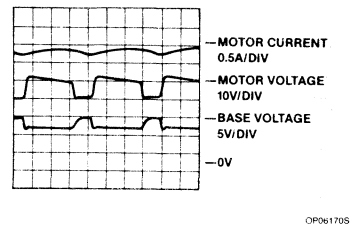


Figure 6. Switching Waveforms

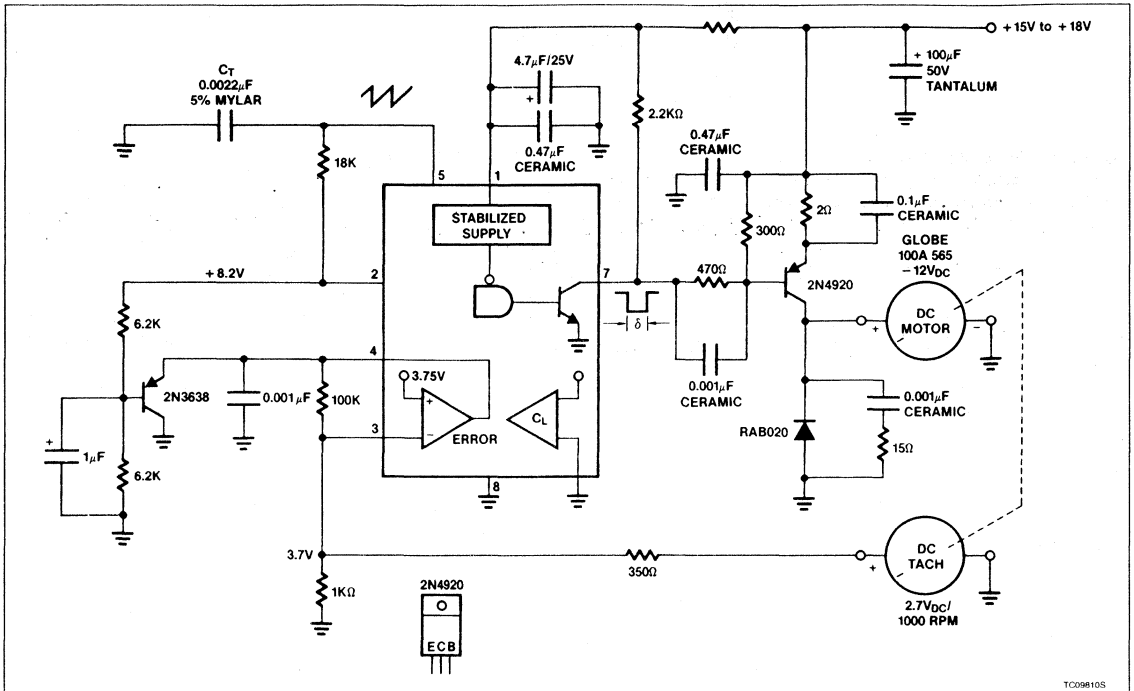
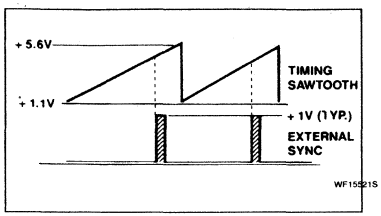


Figure 7. NE5561 Pulse-Width Modulated Motor Drive (Constant Speed)

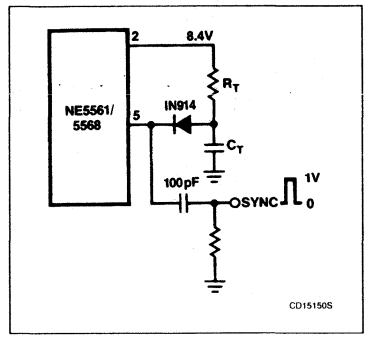
AN124
External Synchronization for the NE5561/5568

Application Note

Synchronization of the 5561 can be accomplished by forcing the timing pin (Pin 5) above the 5.6V sawtooth limit comparator for a short time.



This can be accomplished with a simple diode-coupled narrow pulse source with fairly low source impedance:



A drawback to this approach is that when the 5.6V threshold is reached, a discharge transistor is turned on to quickly pull the timing capacitor to ground and will also attempt to pull the pulse generator to ground. This condition can be avoided by keeping the pulse width very narrow (0.1μs) or by placing a differentiator network between the pulse generator and the diode.

The differentiator will now produce a positive-going spike with the positive edge of the sync pulse, resetting the sawtooth without passing too much current through the discharge transistor. The negative spike produced by the falling edge of the clock will be blocked by the diode and will have no effect on the sawtooth ramp. A narrow sync pulse is no longer necessary while a sharp-*edged* pulse is. The value of C_D should be sufficient to ensure that a 10V pulse will drive the capacitor, C_T, high enough to trip the 5.6V comparator according to:

$$C_T \Delta V_{CT} = C_D(\Delta V_{CT} - V_D)$$

This relates the magnitude of the spike to the size of the pulse. Also assume $R_D C_D < 1\mu s$.

The free-running frequency of the slaved 5561 should be slightly lower than the sync frequency for proper operation.

AN125
Progress in SMPS Magnetic Component Optimization

Application Note

The last ten years have seen considerable progress in the development of the switched-mode power supply. Both design methods and associated hardware have been refined by experience and intensive development. These improvements, especially in the understanding of the influence of magnetic material and winding-conductor properties on SMPS operation, are reflected in the more straightforward and complete design routines now available. The better understanding that made for the improved design routines has also resulted in improved core designs: the ETD range of ferrite cores. Furthermore, lessons learned from experience in wound-component production have been applied to the design of the associated hardware, especially the coil former. The improved core and coil former, together with specially-developed assembly hardware, form the ETD system.

IMPROVED DESIGN ROUTINES

AN1261 presents complete design routines for the magnetic components of all common versions of SMPS. Part 1 covers most aspects of SMPS design, with emphasis on the interaction between the electronic and magnetic aspects. The basic electrical relationships are given for forward, push-pull and flyback converters. Practical formulae are given for inductance and effective-current values. Auxiliary outputs and other special features are included in the coverage, as are related control aspects. All treatments are related to the magnetic design.

The data derived from Part 1 are used in Part 2 to select a suitable ferrite core for the transformer. Here, the magnetic and thermal properties of ferrite cores are considered as they affect their suitability for a given application. Initial selection of a suitable core is by means of charts showing the limits of performance to be expected at various frequencies. The optimum working conditions for cores in various transformer types are discussed, and a further chart enables this optimum to be determined. Wound transformer thermal characteristics are discussed, and formulae given for the losses in the core itself.

SELECTING THE CORRECT CORE

Most SMPS requirements can be satisfied by the range of cores currently available. The preferred grade of material for such high-frequency power applications is Ferroxcube 3C8.

Core Selection Charts

Due to the wide variation in application conditions, the selection charts have been designed to indicate the range of operation of the cores. This is done by using areas of throughput power as a function of frequency as shown in Figure 1. These are effectively areas of good design, since both boundaries represent the performance of a well-designed transformer.

The upper boundary of each area corresponds to a transformer design operating at optimum flux density sweep, with maximum use of the winding window, and Litz-wire windings, for minimum AC resistance. The lower boundary corresponds to a transformer design that also operates at optimum flux density, but has optimized solid-wire windings incorporating 8mm creepage distance for IEC 435 mains isolation, and with a demagnetising winding occupying one-third of the winding space.

Selection charts are given for push-pull, forward and flyback converter SMPS. However, the flyback converter charts are mainly intended as a cross-check on the design obtained by the method given in Reference 4 for chokes.

Operating Conditions

Converter type has the largest influence on throughput power obtainable, but other factors also influence performance, principally

- flux-density sweep
- winding configuration (simple or split, for example) and
- the presence of sensor or demagnetizing windings
- the type of conductor used in the windings
- the number of output windings required
- mains insulation requirements.

Generally, the selection charts assume worst-case conditions. Operation at ambient temperatures lower than the 60°C assumed, the use of feed-forward to ease the restriction on peak flux-density ($^1/_{1.72}$ of saturation to allow for transient conditions), or heatsinking or potting to reduce thermal resistance, will all increase transformer power capacity.

Flyback Transformers and Chokes

Flyback converter transformers and output chokes are magnetically much the same: the main design requirement is stored energy, $^1/_2I^2L$. This is the basis of a separate design routine that includes winding design. This routine, using specially-developed design

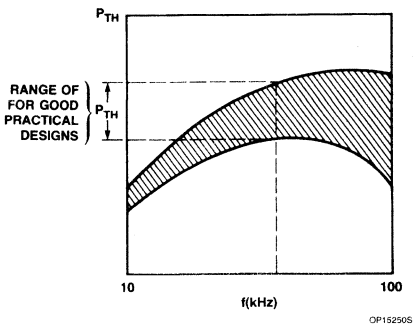


Figure 1. In the Core Selection Charts Given in AN1261, the Power-Handling Capabilities of Each Core are Plotted as a Shaded Area Extending From 10kHz to 100kHz. The Vertical Boundaries of This Area are the Upper and Lower Limits of Throughput Power Capacity Achievable by Good Design but Depending on Conductor Type and Insulation Requirements.

charts, leads directly to spacer thickness and number of turns.

OPERATING FLUX DENSITY

For chokes and flyback-converter transformers (which operate as chokes), stored energy is the basis of the design (subject to the core not being driven into saturation). With forward and push-pull converter transformers, the operating flux-density (both AC and DC components) is set at the beginning of the design process.

Forward and Push-Pull Converters

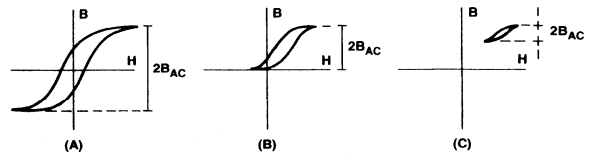
The operating flux density in forward and push-pull converter transformers strongly influences the overall volume of the transformer. Thus, it is set at the beginning of the design process to as high a level as is practical. For forward converter transformers, this level is determined by transient protection requirements or permissible core loss only. With push-pull converters, however, considerations of symmetry may dominate the choice.

Both forward and push-pull converter transformers must be designed to accommodate rapid changes of load. This is done by introducing a transient factor, usual symbol a, related to the range of input voltage for which the power supply is designed. A common value of a is 1.72. This is suitable for mains-fed supplies (215V to 370V or 200V to 340V), telephone supplies (40V to 70V), and mobile supplies (9V to 15.5V).

Considerations of symmetry usually result in the value of a being multiplied by a further factor ϵ for push-pull converter transformers. Asymmetry leads to core saturation, which in turn results in destruction of power switches. Principal causes of asymmetry are unbalanced flux linkage in windings and unequal conduction times in switches. Where care has been taken to achieve balanced transformer windings, and protection circuitry is incorporated to ensure equal conduction times, the value of ϵ may be 1.15; that is, a is increased from 1.72 to 2 for a typical core. Where unbalance is accepted, however, the value of ϵ should be 2. (A list of the symbols used in this article, together with their definitions, is given as Table 1.)

The use of feed-forward can considerably reduce the value of a required but at the expense of reduced transient response.

In forward-converter transformers, core remanence should also be taken into consideration. (Remanence is the induction remaining in a magnetized substance when the magnetizing force has become zero.) However, the introduction of a small air gap in the core, and the use of a slow-rise capacitor allow the whole first quadrant of the core hysteresis loop to be used.



a. Push-Pull

b. Forward Converter Transformers (With Slow-Rise Capacitor) or Ringing Choke

c. Flyback Converter Chokes

Figure 2. Flux-Density Excursions and Corresponding Flux-Density Sweeps

Figure 2 shows the maximum transformer flux-density sweeps for various converter types, and Table 2 gives the value of transient factors a and ϵ under various conditions.

Optimum Flux-Density Sweeps

Manipulation of the expression for the throughput power of an SMPS transformer shows that power reaches a maximum at a combination of operating frequency and flux density such that core loss is 44% of total loss. That is, when

$$0.44\frac{\Delta T}{R_{th}} = 16.7\ f^{1.3}\ B_{ac\ em}^{2.5}\ V_e$$

Here, the right-hand part of the expression is the typical hysteresis loss of Ferroxcube 3C8 ferrite. Since eddy current loss is neglected, this expression applies only up to about 100kHz.

Using this expression, curves of $B_{ac\ em}$, the peak flux-density sweep, have been derived for all Philips' SMPS transformer cores (See Figure 3).

THERMAL RESISTANCE AND TEMPERATURE RISE

The maximum permissible dissipation of a transformer or choke is set by its maximum operating temperature; ambient temperature and thermal resistance depend on core size, mounting method and attitude, the type of conductor in the winding and the amount of insulation incorporated. Due to the insulating effect of the interleaving where 8mm creepage distance is allowed for in the windings, two values are quoted for thermal resistance in AN1261 with and without creepage allowance.

Results confirm that transformer temperature rise can be accurately calculated from the product of total transformer dissipation and thermal resistance for any ratio of core to winding loss.

THE EFFECT OF OPERATING FREQUENCY

Winding Properties

Depending on frequency, the windings of an SMPS transformer fall into one of three categories. At low frequencies, the available winding-window height will be insufficient to accommodate minimum-loss (ideal) windings. At some higher frequency, f_L, the height of minimum-loss windings becomes less than that of the winding window. Finally, at some higher frequency, f_1, the number of turns required for the lowest-voltage winding becomes unity.

Where the winding height is insufficient for minimum-loss windings, winding loss is inversely proportional to the squares of both flux-density sweep and operating frequency. At frequencies above f_L winding loss becomes inversely proportional to operating frequency.

Flux-Density Sweep

From the considerations given earlier, it is apparent that at lower frequencies, operating flux density is limited by core saturation rather than loss. Above some frequency f_T, the optimum operating flux-density (for maximum power) becomes less than the saturation-related maximum, and the flux-density sweep is limited by the requirement that (for Ferroxcube 3C8) core loss $P_C = 0.44\ P_{TOT}$, where P_{TOT} is the total permissible dissipation.

Throughput Power

These various effects of operating frequency are combined to explain the observed variation of SMPS transformer throughput power with operating frequency for Ferroxcube 3C8 cores. Figure 4a shows the division between core and winding loss for an SMPS transformer as a function of operating frequency. Frequencies f_L, f_T and f_1, are marked. (Note

Table 1. List of Symbols

SYMBOL	DEFINITION	UNIT
B_{ac}	Flux-density sweep; half the peak-to-peak flux density excursion	T
B_{CF}	Coil former breadth	mm
f	Operating frequency	Hz
f_1	The frequency at which the number of turns on the lowest-voltage transformer winding becomes unity	Hz
f_L	The lowest frequency at which the coil former height is sufficient to accommodate ideal (minimum-loss) windings	Hz
f_T	The frequency above which no useful increase in the throughputpower capacity of a transformer can be obtained	Hz
H_{CF}	Coil former height	mm
L	Choke inductance	H
φ_{av}	Average turn length	mm
P_c	Total transformer core loss	W
θ_C	Transformer or choke thermal resistance with winding creepage distance incorporated	°C/W
θ_N	Transformer or choke thermal resistance for a winding without creepage distance	°C/W
V_e	Effective volume of a core	m^3
a	Ratio of core saturation flux to working flux allowed: for transient response without saturation	–
ΔT	Temperature rise above ambient	°C
ϵ	Unbalance factor	–

NOTES:
subscripts
e Effective value
cp Pertains to center pole

Table 2. Maximum Values of Flux-Density Sweep for Various Converter Types and Control Circuits

BOUNDARY CONDITIONS	FLUX-DENSITY SWEEP $B_{ac\ cp}$ (T)	
	Forward	Push-Pull
Maximum sweep for FXC 3C8 (100°C)	0.16	0.32
At transient factor a	$\frac{0.32}{2a}$	$\frac{0.32}{a}$
With unbalance factor ϵ*	–	$\frac{0.32}{\epsilon a}$
With x% feed-forward	$\frac{0.32}{2\ (1 + x/100)}$	$\frac{0.32}{(1 + x/100)}$
With unbalance factor ϵ and x% feed-forward	–	$\frac{0.32}{\epsilon\ (1 + x/100)}$

NOTE:
* ϵ is the ratio of peak flux-density in a balanced converter to the peak flux-density in an unbalanced converter.

that f_L may, in fact, be higher than f_T for some cores. This does not alter the main argument.) In Region I, operating flux-density is limited by saturation considerations only, so that throughput power is roughly proportional to frequency. Operation remains saturation limited into Region II, but here power increases roughly as the root of the frequency. (This relationship is complicated by the fact that average turn length decreases as ideal winding height decreases.) Region III begins at f_T, where core operating flux-density becomes limited by core loss to the optimum value for that frequency. The shape of the throughput power curve in the region depends on core material characteristics: the Steinmetz coefficient and its associated flux-density and frequency exponents. For Ferroxcube 3C8, flux-density is inversely proportional to the root of frequency. Then, winding resistance decreases slightly with frequency so that, since winding loss is constant, throughput power is also about constant.

Region IV begins where frequency increases to the point where the number of turns required on the lowest voltage winding falls to unity. (Contours of number of turns N as a function of frequency for various voltages are indicated in Figure 4a). When this happens, flux-density must then decrease with frequency. The rate of this decrease is greater than that required for optimum core loss, so that throughput power decreases. The effect is accentuated by the increasing contribution of eddy current losses at high frequencies.

In practice, other factors, such as eddy currents, parasitic capacitance and rounding of numbers of turns, cause the transitions from one region to another to become blurred so that, as Figure 4c shows, the throughput power characteristic is more rounded. Calculated values for real cores, Figure 5, shows that the general characteristics remain; however, there is always a frequency, close to the core transition frequency, above which no useful increase in throughput power can be obtained.

EFFECT OF CORE DESIGN

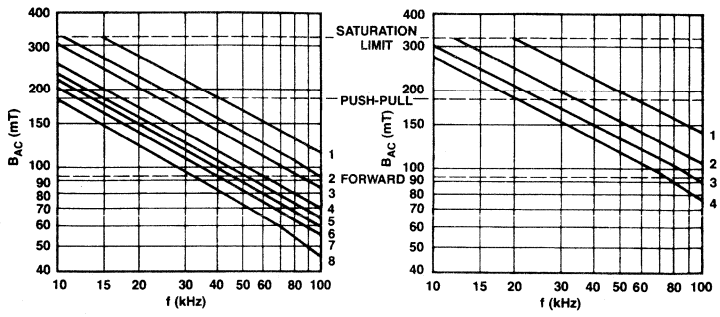
The more complete understanding of the factors that influence throughput power obtainable has made it possible to examine established core designs with a view to improving the designs available. Electrical, magnetic and mechanical considerations can now be combined so that the core can be made as effective as possible.

Existing Core Designs

Analysis of existing core designs shows that performance agrees well with values of f_T. The performance of the smaller cores is found to be relatively poor at 50kHz due to lack of sufficient winding window height for ideal windings.

The effectiveness of the use of core materials is another important consideration, since it directly affects the weight of an SMPS. Constant cross-section E cores generally have the best power-to-weight ratios.

Mechanical design is of great importance since this influences manufacturing cost and transformer production cost. The core should



1. EC35 2. EC41.EC52 3. EC70 4. EE42/42/15
5. EE42/42/20 EE42/54/20 EE42/66/20 6. EE55/55/21
7. EE55/55/25 UU64/79/20 8. EE65/66/27

(A)

1. UU15/22/6 EE20/20/5
2. UU20/32/7 EE25/25/7 EE30/30/7
3. UU25/40/13 4. UU30/50/16

(B)

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NOTE:
Horizontal lines indicate the limits for various converter types ($\alpha = 1.72$). The curves were calculated for a peak temperature rise of 40k.

Figure 3. Optimum, Peak, Center-Pole Flux-Density Sweeps $B_{AC\ CP}$ for a Variety of Cores for SMPS Applications

be cheap to manufacture. Enclosed cores, such as pot cores and their variants (RM, PQ, PM cores) are more expensive to make than E cores for a given power capacity. However, round center legs make for easier winding, with less leakage inductance — especially for strip. For all but the smallest transformers, E cores result in more compact design than U cores. Finally, due to their symmetry, E cores require some 20% less core material for a given power capacity than U cores, with a consequent reduction in eddy current losses. This last point is of special importance at higher operating frequencies.

Core Design Requirements

The requirements for a new core design are clear. The range of cores should be optimized for frequencies appropriate to their power handling capacity: 50kHz for 300W, 100kHz for 100W, for example. This requires proper choice of f_L and f_T. Optimization should be aimed at forward converter applications (the cores will then also be suitable for unbalanced push-pull converters).

The design of the associated coil formers is also critically important. They should be suitable for automatic handling. A large number of pins is required, both for flexibility of layout and to accommodate multiple secondaries.

The core and wound coil former should be quick and easy to assemble. The combination should be designed for horizontal mounting on PC boards to minimize height and make termination of strip windings easier.

THE ETD SYSTEM

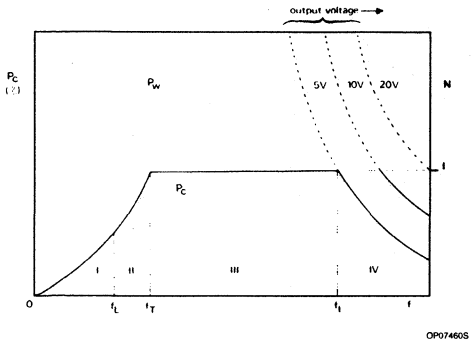
The Cores

These criteria have been adopted in the design of the ETD cores. They are constant cross-section E cores in Ferroxcube 3C8 ferrite with round center legs, photo and Figure 6, and are designed for

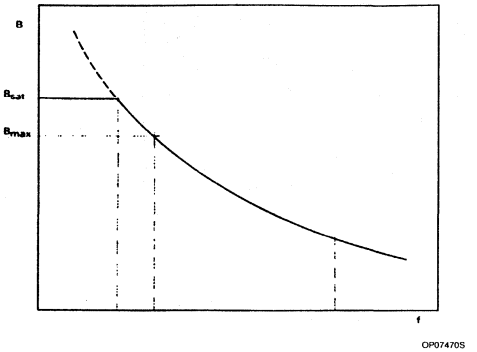
- Minimum throughput powers in the range 100W to 300W
- Economical manufacture
- Minimum weight of ferrite
- Operating frequencies in the range 50kHz to 150kHz
- High throughput power density
- Mains isolation
- Minimum transformer volume and PC board areas.

Magnetic properties are given in Table 3.

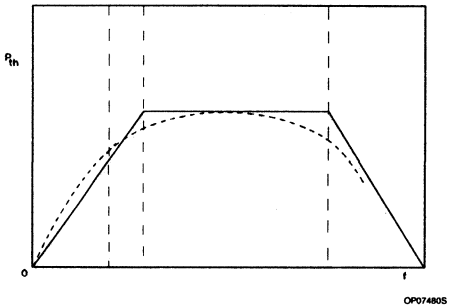
The ETD cores are compared with existing core designs for power per unit weight in Figure 7. Throughput power areas as a function of frequency for ETD cores are given in Figure 8, and the optimum flux-density sweep in Figure 9.



a. Division of Transformer Loss Between Core Loss and Winding Loss as a Function of Frequency Showing the Various Boundary Frequencies

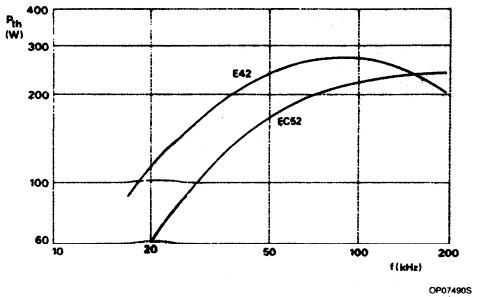


b. Relation Between Flux Density and Frequency for Maximum Throughput Power



c. The Corresponding Throughput Power Characteristic

Figure 4



NOTE:
There is a frequency (from Figure 3) above which no useful increase in throughput power can be obtained. For the EC52 core this is 100kHz, for the E42 core it is 52kHz.

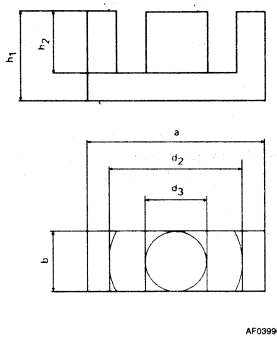
Figure 5. Calculated Throughput Powers (5V Forward Converters) With Frequency for EC52 and E42/21/20 Core Show the Same General Characteristics

The Coil Former and Assembly Hardware

Simple, rapid winding and assembly of ETD system-based transformers and chokes is made possible by the coil former of Figure 10, together with the associated snap-on stainless-steel assembly clips.

Table 3. Magnetic Dimensions of ETD System Cores

CORE TYPE	$A_{CP\ min}$ (mm^2)	A_e (mm^2)	V_e (mm^3)	φ_e (mm)
ETD 34	87	97.1	7640	78.6
ETD 39	117	125	11500	92.2
ETD 44	167	173	17800	103
ETD 49	204	211	24000	114



CORE TYPE	MID-LIMIT DIMENSIONS (mm)						MASS (g)
	a	d_2	d_3	h_1	h_2	b	(CORE HALF)
ETD 34	34.2	26.3	10.8	17.3	12.1	10.8	20
ETD 39	39.1	30.1	12.5	19.8	14.6	12.5	30
ETD 44	44.0	33.3	14.9	22.3	16.5	14.9	47
ETD 49	48.7	37.0	16.4	24.7	18.1	16.4	62

Figure 6. Outline Drawing and Dimensions of the New ETD Core Range

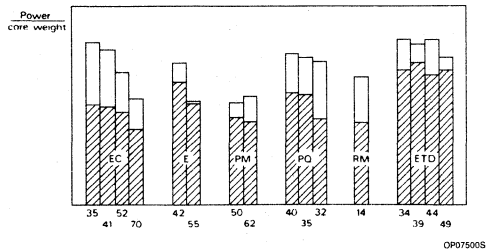


Figure 7. The Thoughput Power per Unit Weight of Core Material for ETD Cores Compared With That of Other Popular Core Types at two Operating Frequencies: 50kHz (Shaded Areas) and 100kHz (Open Areas). Forward-Converter Operation is Assumed

Principal features of the design are indicated in Figure 10:

- The length and number of slots gives a wide choice of lead-out position
- There is at least 8mm creepage distance from the pins to the ferrite core
- The pegs between the slots allow wire to be run from any one slot or pin to any other
- The four support legs provide 8mm creepage distance between the windings and the PC board
- The hood over the pins provides 8mm creepage distance between leadouts and assembly clips
- A separate grounding clip for the core is to be available.

The coil former itself is moulded in polybutylene terephthalate, a high-grade, flame retardant (UL94-VO), thermoplastic. Windings dimensions are given in Table 4.

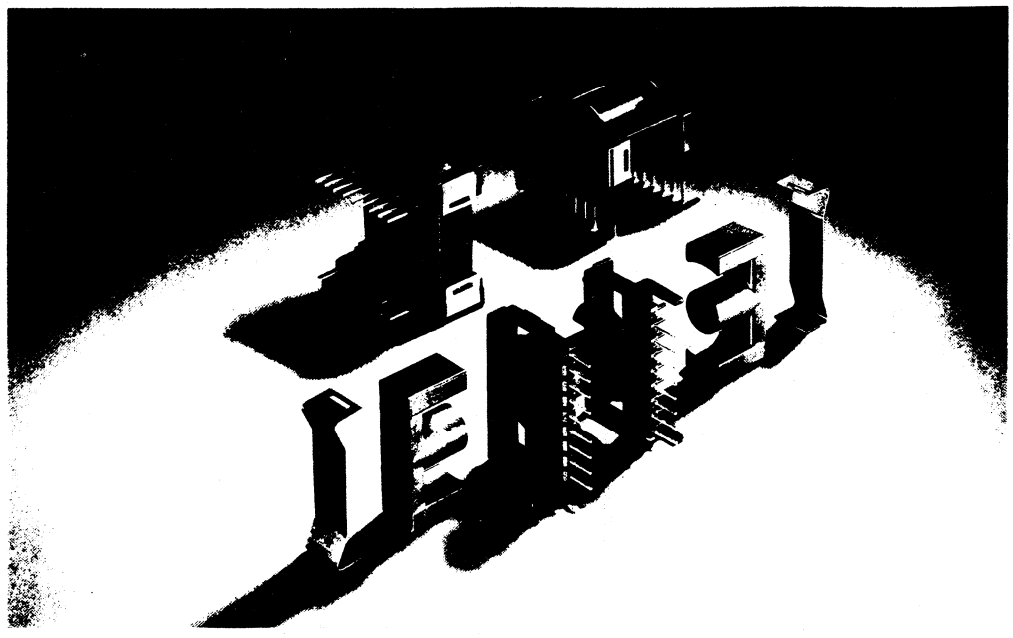
ETD system components provide OEMs with the most efficient electrical, magnetic and mechanical route to full, economical, automated production of SMPS transformers.

SWITCHED-MODE POWER SUPPLIES

The essential difference between switched-mode and conventional (mains) power supplies is operating frequency. Whereas conventional power supplies operate at mains frequencies, 50Hz or 60Hz, switched-mode power supplies (SMPS) operate at frequencies on the order of 50kHz. The complications associated with operation at these high frequencies are more than compensated for by the savings in weight and volume, especially of transformers and smoothing components.

Voltage conversion and control in SMPS is achieved by chopping the incoming supply voltage with a high-speed switch such as a transistor. The chopped voltage is applied to a transformer which performs voltage conversion and provides isolation. This transformer is generally wound on a ferrite core, and is much smaller and lighter than a 50Hz unit of comparable power capacity. Fine control of output voltage is obtained by varying the duty cycle of the switch.

Most SMPS converters require a DC input and provide a DC output. For operation from the mains, therefore, a rectifier and smoothing circuit generally precedes the converter itself (Figure 11).



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These ETD System Components Provide OEMs With the Most Efficient and Economical Route to SMPS Transformers

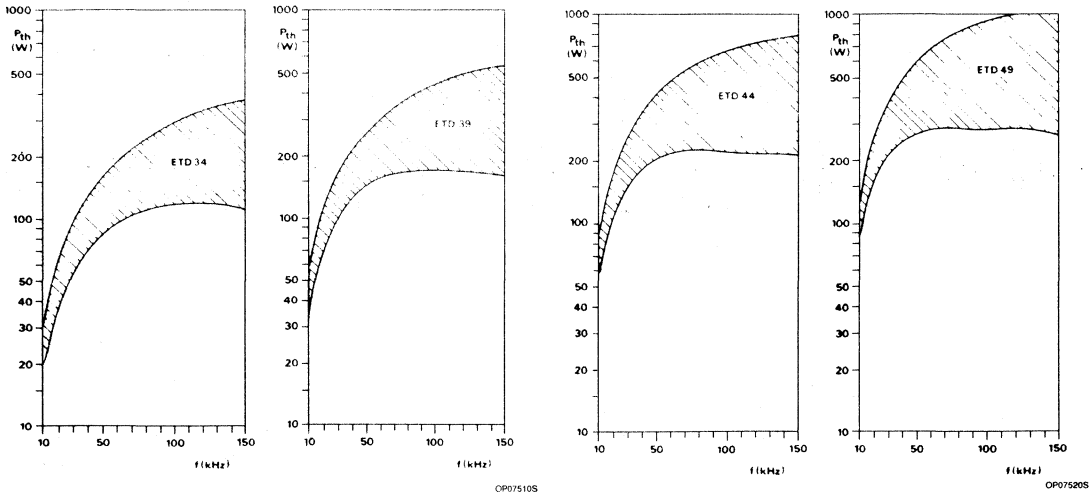


Figure 8. Throughput Power as a Function of Frequency for ETD Cores in Forward-Converter Transformers

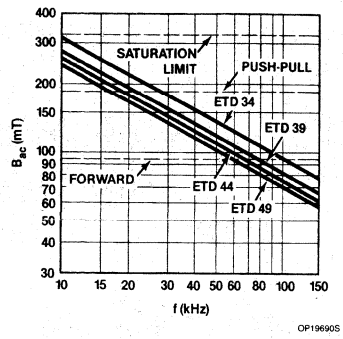


Figure 9. Optimum Flux-Density Sweeps for ETD Cores

Table 4. Winding Dimensions of ETD System Coil Formers

TYPE	B_{CF} (mm)	H_{CF} (mm)	φ_{av} (mm)
ETD 34	20.9	5.9	61
ETD 39	25.7	6.9	69
ETD 44	29.5	7.3	78
ETD 49	32.7	8.4	86

SMPS Converters

There are three basic SMPS converter arrangements; they and their variants are discussed in detail in AN1261.

In the forward converter, Figure 12, power is transferred directly to the load while the switch is closed; the energy stored in the inductor is transferred to the load while the switch is open. The switch may be transformer-coupled to the inductor for input/output isolation.

In the flyback converter, Figure 13, power is stored in the inductor while the switch is closed and transferred to the load while the switch is open. The functions of transformer and inductor may be combined where voltage transformation is required.

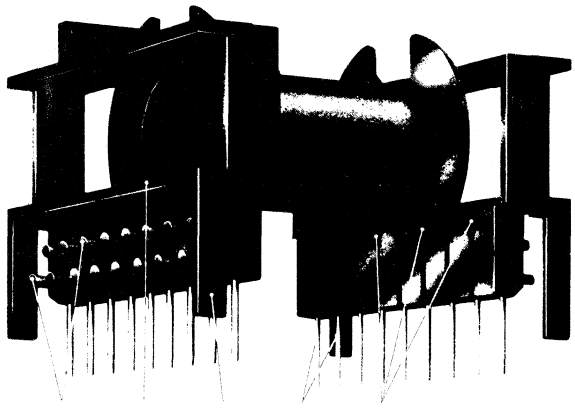
The push-pull converter is, effectively, a forward converter in which the output choke is driven by any push-pull arrangement of power transistors, including a full bridge (see Figure 14). Operation after the transformer is similar to that of a forward converter, but with twice the effective switching frequency.

Transformer and Choke Requirements

There are two main boundary conditions for the power transformer: it must not saturate (otherwise the power transistors will be damaged) and it must not overheat. In addition to these boundary conditions, the output choke should be capable of storing sufficient energy to deliver one output cycle so that ripple will be low and regulation good.

Saturation is prevented by designing for worst probable combinations of load change and input voltage fluctuation. In forward converters, provision must be made for removing energy stored in the transformer at the end of the ON period of the switch. In push-pull converters, the degree of symmetry achievable in both power switches and transformer windings determines the unbalance allowance.

Overheating of the transformer and choke is prevented by calculation of total power dissipation: core hysteresis and eddy current losses, and winding losses.



NOTES:
Pegs allow wires to be taken from most appropriate slot to chosen pin.
These plates give 8mm creepage distance between wires and assembly clips.
Legs give 8mm creepage distance from windings and PC board.
8mm creepage from pins to core.
Multiple slots for maximum freedom of lead-out position.

Figure 10. Coil Former Design for the ETD System, Intended for Automatic Winding

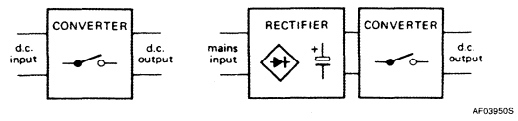


Figure 11. SMPS Converter

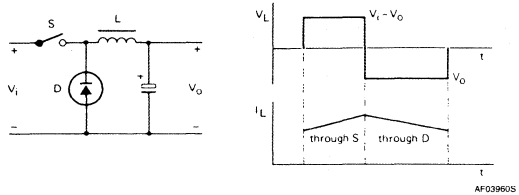


Figure 12. Forward Converter

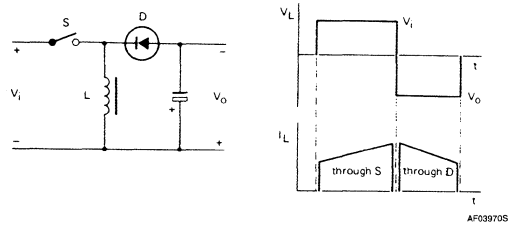


Figure 13. Flyback Converter

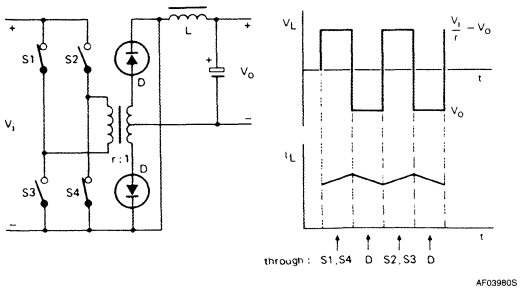


Figure 14. Push-Pull Converter

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AN126
Applications Using the SG3524

Application Note

APPLICATIONS

The capacitor-diode output circuit is used in Figure 1 as a polarity converter to generate a −5V supply from +15V. This circuit is useful for an output current of up to 20mA with no additional boost transistors required. Since the output transistors are current-limited, no additional protection is necessary. Also, the lack of an inductor allows the circuit to be stabilized with only the output capacitor.

Another low current supply is the flyback converter used in Figure 2 to generate ± 15V at 20mA from a +5V regulated line. The reference generator in the SG3524 is unused with the input voltage providing the reference. Current limiting in a flyback converter is difficult and is accomplished here by sensing current in the primary line and resetting a soft start circuit.

In the conventional single-ended regulator circuit shown in Figure 3, the two outputs of the SG3524 are connected in parallel for effective 0.0 − 90% duty cycle modulation. The use of an output inductor requires an RC phase compensation network for loop stability.

Push-pull outputs are used in this transformer-coupled DC − DC regulating converter shown in Figure 4. Note that the oscillator must be set at twice the desired output frequency, as the SG3524's internal flip-flop divides the frequency by 2 as it switches the PWM signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

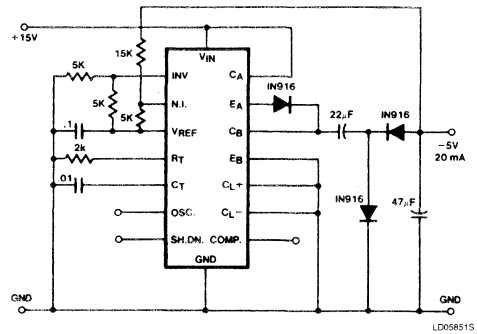


Figure 1

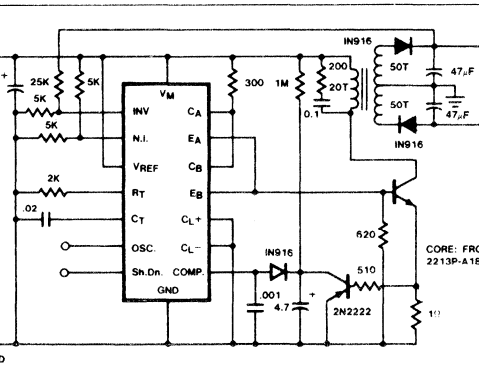


Figure 2

SG3524 PUSH-PULL ± 50V, 100W Converter (Off-Line)

A simple solution to off-line converter design for power audio amplifier circuits is shown in Figure 5. The SG3524 emitter outputs are used to drive directly a pair of BUZ41A Power FETs in the primary side of the step-down transformer at a 50kHz rate. (The main oscillator operates at 100kHz.) The transformer consists of 120T of #24 wire centertapped at 60T. This is sandwiched between two 50-turn center-tapped secondary windings of #20 wire. Diodes are fast recovery BYW30s; the output chokes, 500μH wound on EC35 (3C8) pair Ferroxcube cores, provide adequate filtering in conjunction with the 1000μF and 0.01μF ceramic capacitors across the output.

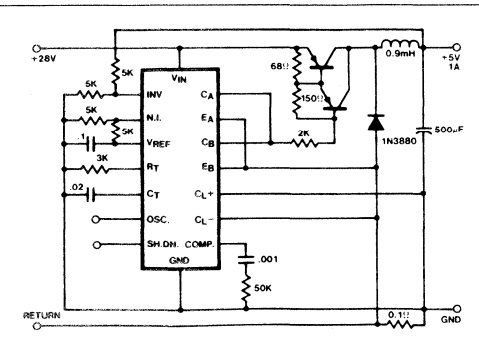


Figure 3

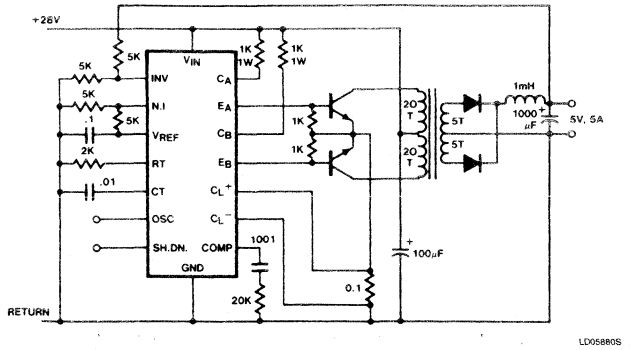


Figure 4

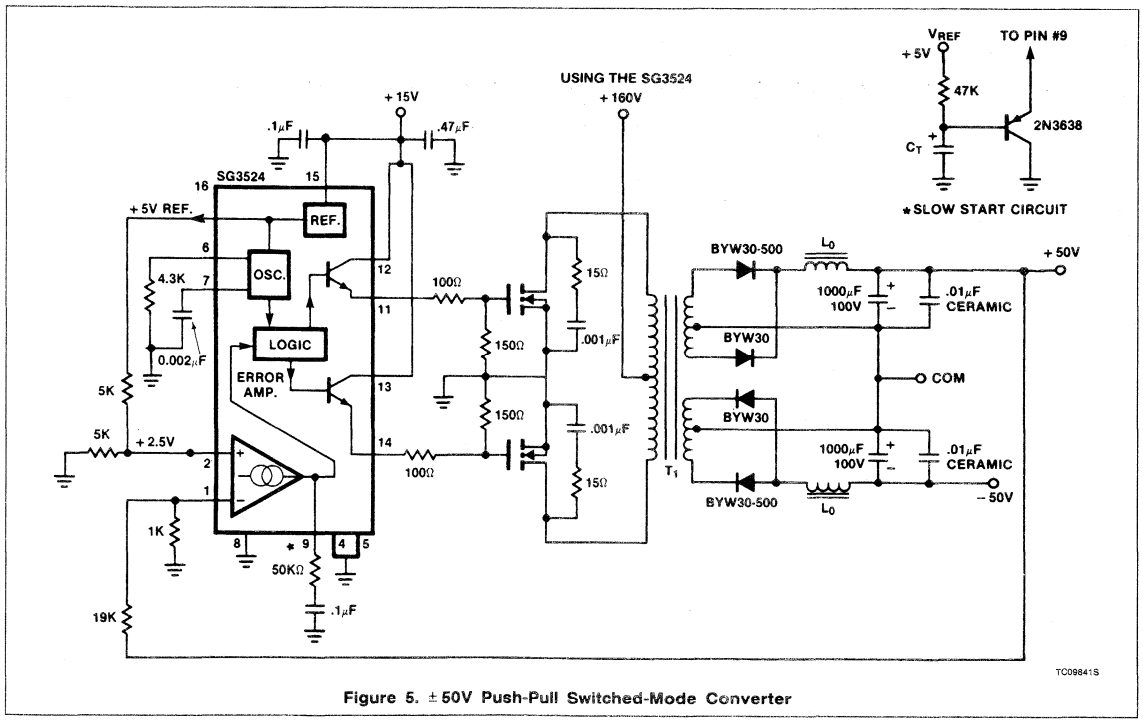


Figure 5. ±50V Push-Pull Switched-Mode Converter

AN128
Introduction to the Series-Resonant Power Supply

Application Note

There has long been a need for a smaller and more efficient alternative to the transformer/rectifier/series stabilizer circuit for deriving a constant, easily-isolated DC supply from the mains. The development of high voltage switching transistors has allowed the construction of SMPS circuits which go a long way toward meeting this need but are still far from providing the ideal answer to the problem. The main drawbacks of the SMPS, when it is supplied from the AC line, is limited efficiency due to switching losses and dissipation in dV/dt limiting RC networks, RFI due to the generation of near-rectangular current waveforms, difficult transformer design, and the need for a complex control circuit to ensure continued operation with an open-circuit or short-circuit load. A circuit that overcomes these drawbacks is the series-resonant power supply (SRPS) which incorporates an inverter in which a semiconductor switch maintains sinusoidal oscillation in a series-resonant LC network. Although the high-frequency sinusoidal currents generated in an SRPS allow it to be made compact and efficient, with far less RFI than the SMPS, its use has so far been restricted to low voltage power supplies due to the lack of a suitable low-loss, high voltage semiconductor switch.

Recently introduced GTOs (gate turn-off Thyristors described in References 1, 2 and 3) with their high VA ratings, fast switching and simple, transistor-like drive, now allow the construction of SRPS circuits which can operate from a rectified AC input and will undoubtedly replace the SMPS for controlled mains power conversion in applications such as television sets, industrial drives, fluorescent lighting systems, microwave and inductive cookers. The SRPS is also suitable for controlling the speed of DC series-wound motors in domestic appliances, and for reducing harmonic distortion in the AC supply by acting as a buffer between the AC line and a DC power supply. The main advantages of the SRPS are:

- It is a more than 90% efficient power converter.
- It causes minimal EMI/RFI because the AC input current can be made sinusoidally in phase with the AC line voltage.
- It can be built with a single, easily-designed, inductive element (transformer) which also provides line isolation.
- It continues to operate with the output short-circuit. It also continues to supply a well-stabilized output when it is not connected to a load.
- It can be made self-starting and, therefore, does not need a small transformer to supply the control circuit for the GTO.

Survey of GTOs for SRPS

TYPE NUMBER	V_{DRM} (V)	I_{TCRM} (A)	$I_{T(AV)}$ (A)	CASE
BT157	1500	10	2.2	TO-220
	1300	10	2.2	TO-220
BTW58	1500	25	6.5	TO-220
	1300	25	6.5	TO-220
	1000	25	6.5	TO-220
BTW59*	1500	50	12	TO-238
	1300	50	12	TO-238

NOTE:
* With isolated base.

Introduction to the Series-Resonant Power Supply

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PRINCIPLES OF SRPS OPERATION

Figure 1 is the basic circuit of an SRPS, the operating principle of which depends on sinusoidal alternating current generation in the $L_1C_1C_O$ circuit. For guaranteed self-oscillation, there are two conditions regarding the values of the components. The inductance of L_S must be at least ten times that of L_1, and the value of C_O must be at least twice that of C_1. The operation of the circuit will first be described without a load connected to V_O and with a very brief conduction period for the GTO. This will be followed by a description of the circuit operation under similar conditions but with a longer conduction period for the GTO. Since the behavior of the SRPS is complex (it sometimes functions as a fourth-order network), a complete analysis of the circuit is only possible with the aid of a computer. These theoretical descriptions are therefore only intended to give a basic understanding of the circuit operation and are followed by plots of the current and voltage waveforms derived by computer analysis of the basic circuit. The application note concludes with a description of ten methods of connecting a load to the SRPS.

Unloaded Circuit With Brief GTO Conduction Period

The waveforms for this mode of operation are given in Figure 2. Since $L_S \gg L_1$, and I_O is very small, the influence of L_S and I_O on the circuit behavior can be disregarded for this simplified description.

In the steady state, with the GTO turned off, C_1 is charged to V_S. Assume that the GTO is turned on for the very short time necessary to just discharge C_1. Further assume that current I_1 is negligible during this brief on-time of the GTO. When the GTO is switched off, current I_1 oscillates sinusoidally about zero at the resonant frequency of the circuit, comprising L_1 together with C_O and C_1 in series:

$$\omega = \frac{1}{\sqrt{(L_1\ C_{TOT})}}$$

where

$$C_{TOT} = \frac{C_1 C_O}{C_1 + C_O}$$

The peak oscillatory current is the supply voltage divided by the impedance of the resonant circuit (Z_1),

$$\hat{I}_1 = \frac{V_S}{Z_1} = V_S \sqrt{\frac{C_{TOT}}{L_1}} \qquad (1)$$

which has an instantaneous value

$$I_1 = \frac{V_S}{Z_1} \sin \omega t$$

For stable self-oscillation of the circuit, the minimum level of V_1 must just reach zero during each cycle. The instantaneous value of V_1 is therefore given by

$$V_1 = V_S(1 - \cos \omega t)$$

$$\hat{V}_1 = 2V_S \qquad (2)$$

the AC component of which is

$$\hat{V}_{1\ AC} = V_1 - V_S = V_S$$

This voltage therefore oscillates sinusoidally between 0V and $2V_S$ and has an average value equal to the supply voltage (V_S). Since the average value of the oscillatory current I_1 must therefore be zero, it is apparent that, as is to be expected, power is not drawn from the supply when the output from the circuit is unloaded.

The ratio V_O/V_1 is determined by the ratio of the values of C_1 and C_O. The peak value of V_O is

$$\hat{V}_O = V_S + \frac{\hat{V}_1 C_1}{2C_O} = V_S \frac{C_1 + C_O}{C_O}$$

the AC component of which is

$$\hat{V}_{O\ AC} = \hat{V}_O - V_S = V_S \frac{C_1}{C_O} \qquad (3)$$

Unloaded Circuit With Longer GTO Conduction Period

The waveforms for this mode of operation are given in Figure 3. If the conduction period of the GTO is made longer than that necessary to just discharge C_1, considerable current due

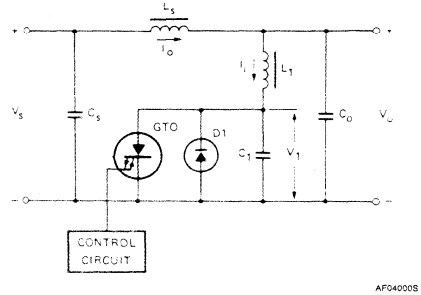


Figure 1. Basic SRPS Circuit

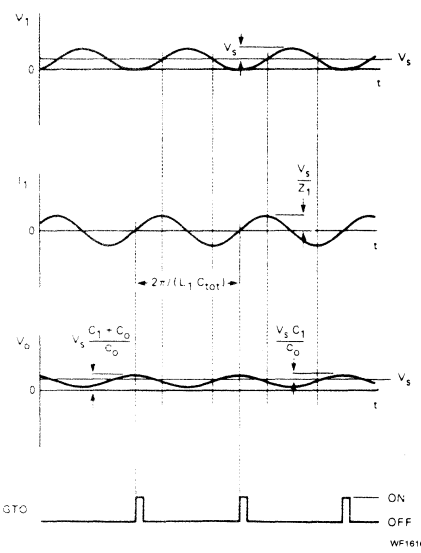


Figure 2. Waveforms of the Basic SRPS for the Shortest Possible Conduction Time for the GTO

to I_O and the discharge of C_O is flowing in L_1 at the turn-off instant. This value of I_1 will be denoted I_{OFF}. The peak oscillatory current V_S/Z_1 from equation (1) will now increase, in proportion to the ratio I_{OFF} to V_S/Z_1, by a factor

$$M = \sqrt{\left[\left(\frac{I_{OFF}Z_1}{V_S}\right)^2 + 1\right]}$$

The peak current through L_1 will therefore be

$$\hat{I}_1 = \frac{MV_S}{Z_1} \quad (4)$$

The peak voltage across C_1 in Equation 2 was V_S above its average value V_S. The rise of V_1 above V_S will now increase by the multiplying factor M, which gives

$$\hat{V}_1 = V_S + MV_S = V_S(M + 1) \quad (5)$$

the AC component of which is

$$\hat{V}_{1\ AC} = MV_S$$

Solving Equation 5 for the maximum multiplying factor in terms of the supply voltage and the maximum allowable peak voltage across the GTO gives

$$M_{MAX} = \frac{\hat{V}_1}{V_S} - 1 \quad (6)$$

The AC component of the output voltage is $\hat{V}_{1\ AC}$ multiplied by the ratio C_1/C_O, which gives

$$\hat{V}_{O\ AC} = \frac{\hat{V}_{1\ AC}\ C_1}{C_O} = \frac{MV_S\ C_1}{C_O} \quad (7)$$

Voltage Control Range of the Basic SRPS

Assuming that V_S is the rectified line voltage (300V) and that the maximum peak voltage permitted across the GTO (V_1) is 1200V, then from Equation 6 the maximum multiplying factor is 3 and, from Equation 4, the maximum peak current through L_1 is

$$\hat{I}_1 = \frac{3V_S}{Z_1} \quad (8)$$

Comparing Equations 1 and 8 shows that the peak current through L_1 increases threefold when the conduction period of the GTO is increased to the maximum allowed by the permitted peak voltage across the GTO (V_1). Comparing Equations 2 and 5 shows that, with M = 3, the peak voltage across the GTO increases from $2V_S = 600V$ to $4V_S = 1200V$ when the conduction period of the GTO is changed from minimum to maximum. Comparing Equations 3 and 7 shows that, with $C_1/C_O = 0.5$, the control range for the AC component of V_O is

$$V_{O\ AC}\ min = 0.5\ V_S = 150\ V$$

$$V_{O\ AC}\ max = 1.5\ V_S = 450\ V$$

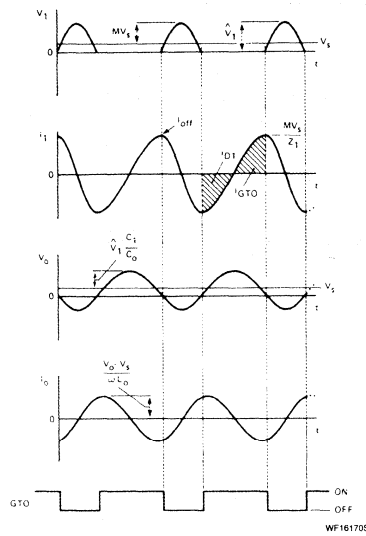


Figure 3. Waveforms for the Longest Possible Conduction Time for the GTO and V_1 = 1200V max, V_S = 300V, C_1 = 10nF, C_O = 22nF, L_O = 10mH, L_1 = 1mH, M = 3

The circuit can therefore be used as a power converter with its output voltage controllable over a 3:1 range by varying the conduction period of the GTO.

Alternatively, for a lower supply voltage such as V_S = 100V, and the same maximum peak voltage V_1 = 1200V, the maximum multiplying factor from Equation 6 is 11. Solving Equation 2 and 5 for V_S shows that the variation of supply voltage (V_S) that can be compensated by variation of the conduction period of the GTO is:

$$V_{S\ min} = \frac{\hat{V}_1}{M + 1} = 100V$$

$$V_{S\ max} = \frac{\hat{V}_1}{2} = 600V$$

The SRPS output voltage can therefore be stabilized against a 6:1 DC supply voltage variation by varying the conduction period of the GTO.

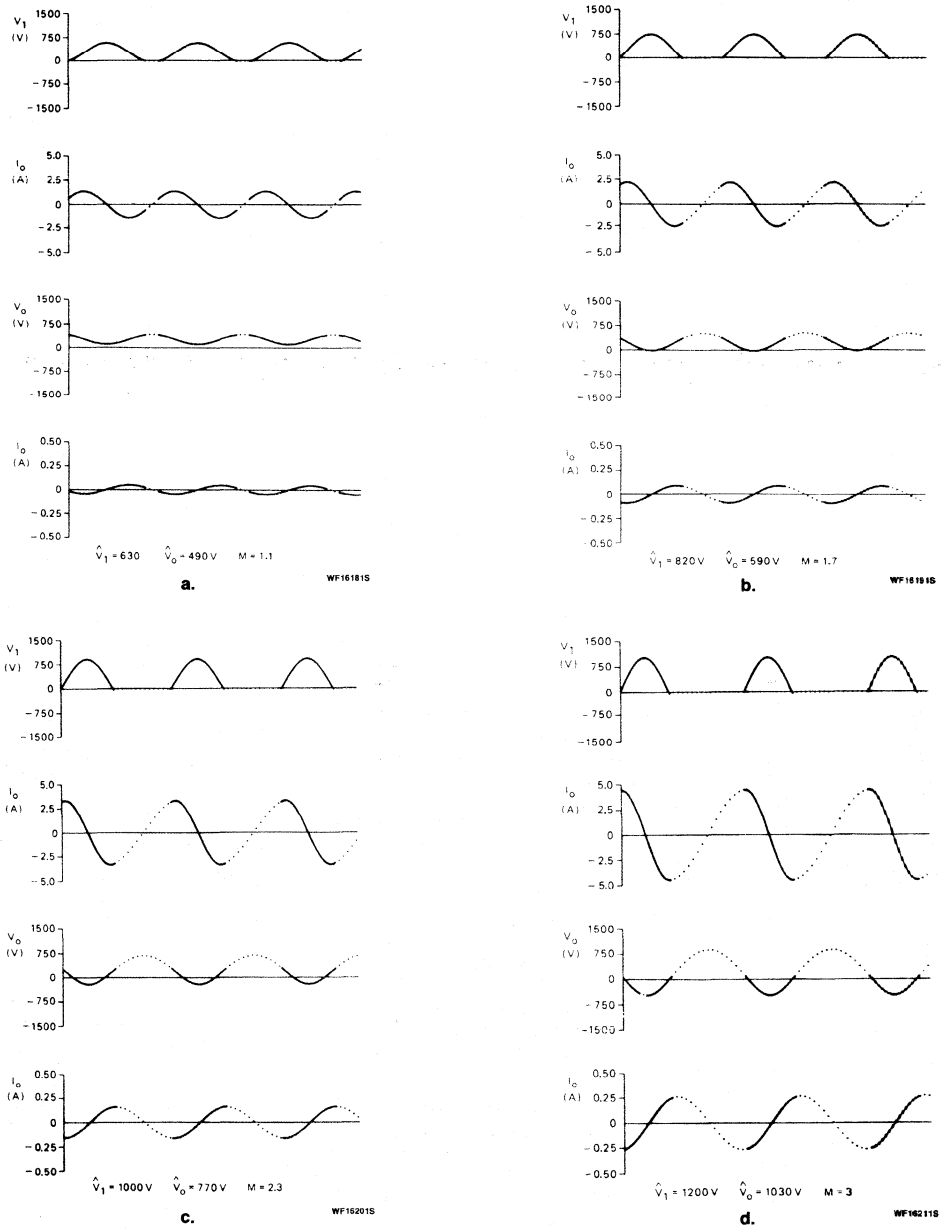
Computer Plot of the SRPS Voltage and Currents

As shown in Figure 4, a computer program has been used to plot the exact time functions for I_O, I_1, V_O and V_1 with $V_S = 300V_{DC}$ and components values L_S = 10mH, L_1 = 1mH, C_O = 20nF and C_1 = 10nF. The computer plots have been made for peak values of V_O of 490V, 590V, 770V and 1030V. Subtracting V_S = 300V from these figures gives the AC component of V_O, which is about 190V, 290V, 470V and 720V, respectively. This shows that the available output voltage control range for V_S = 300V and V_1 max. = 1200V is at least 3.8:1 instead of 3:1 as calculated in Equations 3 and 7. This is due to the fact that the voltages across the capacitors in the oscillatory circuit are almost 180° out of phase so that the voltage division between them is not directly proportional to their values. The plots also indicate that the operating frequency decreases as the conducting time of the GTO is increased.

Extracting Power From the SRPS

There are three basic methods of extracting power from the SRPS. They are:

1. From capacitor C_O, via a diode, to an output electrolytic capacitor. Since the output voltage $V_{O\ AC}$ is superimposed on the input DC level V_S, the voltage across the electrolytic capacitor will always exceed V_S. The circuit is therefore an up-converter and its main use is as a buffer between the AC line and a DC power supply unit.
2. From capacitor C_O via a capacitor which blocks the DC component of V_O so that pure AC is available at the output. This circuit is suitable for driving resistive loads and fluorescent lighting tubes. If the output from the blocking capacitor is rectified in a voltage doubler circuit, this type of SRPS is suitable for controlling the speed of a series-wound DC motor.



NOTE:
The dotted sections are the conduction period of the GTO, which is the maximum allowed by the V_1 specification.

Figure 4. Computer Plots of the Waveforms in the Circuit of Figure 1 With $V_S = 300V_{DC}$, $L_O = 10mH$, $L_1 = 1mH$, $C_O = 20nF$, $C_1 = 10nF$

3. By replacing inductor L_S with a transformer. This arrangement gives the best performance because it gives very good line isolation and the load can be correctly matched to the SRPS by adjustment of the turns ratio of the transformer. This type of circuit can drive resistive or rectifier loads and can also be used as a supply for fluorescent tubes. For rectifier loads, however, the leakage inductance of the transformer must be made very low; for example, by using sandwiched windings. The final part of this application note shows how inductor L_1 can be integrated with the transformer to overcome this problem and create an SRPS with a single inductive component.

PRACTICAL SRPS CIRCUITS WITHOUT POWER LINE ISOLATION

Direct-Coupled SRPS Up-Converter

The circuit of this type of SRPS is given in Figure 5. Diode D_O half-wave rectifies V_O and feeds the resultant half-sinewaves to output electrolytic C_O. Since the average value of V_O is V_S, the rectified half-sinewaves at the output are superimposed on the DC input voltage and the DC output voltage must necessarily exceed this level. The circuit is therefore an up-converter. The percentage of the total output power which has to be converted by the series-resonant circuit is $(V_O-V_S)/V_O$. For V_S = 200V (average voltage of full-wave rectified 220V mains) and $V_{O\,AC}$ = 500V, this amounts to only 60% of the total output power. This, together with the inherent high efficiency of the SRPS (about 95% at $V_S = 200V_{DC}$), allows the circuit to feed some current to the load, even when the input voltage is as low as 10% of the output voltage. For $V_{O\,AC}$ = 500V to 600V, the full-wave rectified AC input need not therefore be smoothed and can be obtained directly from a bridge rectifier followed by a low value decoupling capacitor (a few μF). This arrangement results in an SRPS up-converter with a well-stabilized DC output with a low level of superimposed 100Hz ripple. Since the AC current flowing via the bridge rectifier without a high value smoothing capacitor is sinusoidal, the circuit can convert unlimited power without exceeding the limits of power line harmonic generation specified for domestic equipment in CENELEC specification EN 50 006.

The foregoing considerations indicate that the main use for this type of SRPS is for reducing power line distortion by acting as a buffer between the AC supply and a 500V to 600V DC power supply of more than 500W.

Capacitively-Coupled SRPS Circuits

In capacitively-coupled SRPS circuits, the DC component of voltage V_O is blocked by a capacitor between C_O and the output rectifier. The circuit is given in Figure 6 which shows three methods of rectifying the AC component V_O.

Circuit 1. In Circuit 1 of Figure 6, the AC component of V_O is rectified in a voltage doubler circuit that applies a positive DC voltage to the load. Like the previously described up-converter, this circuit works best with a DC output of more than 500V, but has the added advantage of being immune to output short-circuits. The main use of Circuit 1 is speed control of a series DC motor connected as shown in Figure 7. Since inductor L_S has now been replaced by the series-connected armature and field windings of the motor, the SRPS has an effective input voltage of V_S minus the back EMF. Since the back EMF is proportional to the current through the motor at a given speed, it is not necessary to use a high value capacitor to smooth the rectified mains input. The current flowing in the 50Hz mains can therefore be made sinusoidal so that mains pollution is minimal. The range of back EMF must not exceed about 75% of supply voltage V_S so that the SRPS can still supply a reasonable amount of current when the motor is running at full speed.

Circuit 2. Circuit 2 of Figure 6 is similar to Circuit 1 except that the output rectifier/voltage doubler is connected to provide a negative DC output voltage. The possible uses for this circuit are few.

Circuit 3. Circuit 3 of Figure 6 is again similar to Circuits 1 and 2 except that the output is bridge-rectified. Since the bridge rectifier provides half the average output voltage of a voltage doubler rectifier, the minimum peak value for the DC output can be reduced to about 250V. A disadvantage of the circuit, however, is that the output is floating with respect to the return line of the input voltage.

SRPS CIRCUITS WITH POWER LINE ISOLATION

Since capacitor C_{IN} has a much higher value than C_O, C_O is effectively in parallel with L_S so that V_O appears across this inductor. If line isolation is required, L_S can therefore be replaced by a transformer with output rectifier connected to the secondary winding (Figure 8). The manner in which the rectifier and transformer are connected then determines the mode of operation; i.e., power transferred to the load

- when the current in the primary winding of the transformer is positive (forward mode, Circuit 1)
- when the current in the primary is negative (flyback mode, Circuit 2)
- when the current in the primary is positive and when it is negative (forward flyback mode, Circuit 3).

In Circuit 3, a bridge rectifier can also be used with an untapped secondary winding.

In addition to driving rectifier loads via a transformer with low leakage inductance, these circuits with transformer-coupled output are also suitable for driving a resistive load or a load that behaves like a voltage source, for example, a fluorescent lamp or a magnetron in a microwave cooker. The best performance is obtained with a DC output of about 300V.

SRPS With a Single Inductive Component (Transformer)

In the circuits shown in Figure 8, inductor L_1 is rather bulky because, at operating frequencies of about 50kHz, the flux swing in the core is quite large. It is therefore necessary to use a large core to prevent saturation and consequent overheating due to hysteresis losses. The core heating problem can be completely overcome by constructing the output transformer in such a manner that L_S is formed by

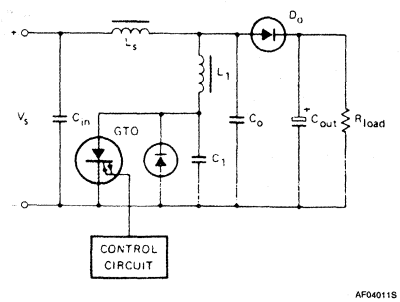


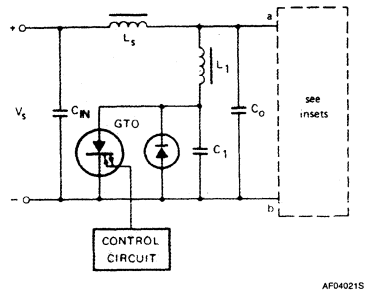
Figure 5. SRPS Up-Converter

the primary self-inductance and magnetizing inductance of the transformer, and L_1 is formed by the primary and secondary leakage inductances. The flux swing of the transformer core is then quite small and the hysteresis losses are low.

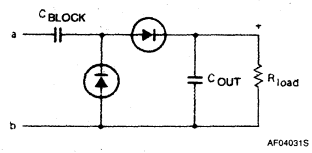
Figure 9 shows how inductor L_1 can be integrated with the output transformer. First, since C_{IN} is a much higher value than C_O, C_O is effectively in parallel with the primary winding of the transformer and can therefore be connected in this position. Second, if the value of C_O is multiplied by the square of the turns-ratio of the transformer, it can be connected in parallel with the secondary winding. Finally, since there is now no connection to the junction of L_S and L_1, L_1 can be integrated with the output transformer. This final step is clarified by the equivalent T-circuit of the transformer given in Figure 10. Since a requirement for guaranteed self-oscillation of the SRPS is that the value of L_S is at least ten times that of L_1, the minimum coefficient of coupling for the transformer is $\geqslant 0.8$. A transformer with sufficient leakage inductance can easily be constructed on a pair of ferroxcube U-cores with the primary wound round one pole and the secondary wound round the other. If the external magnetic field with this type of construction is too great (for example, in a television receiver), the primary and secondary windings can be stacked on the gapped center pole of a pair of E-cores. Experiments have shown that when this type of transformer is installed in a working SRPS and positioned within 4cm of the deflection coils of a 26-inch CTV set with a 30AX deflection system, there is no perceptible distortion of the raster. If the transformer is positioned within 4cm of the most sensitive part of the tube (cathode, grid 1 and 2 area), the maximum distortion of the raster is 1mm.

An important advantage of the SRPS with a single inductive element is that it is inherently immune to a short-circuited output. It is therefore self-starting, even with 0V across the output capacitor, so it is not necessary to use a separate transformer to provide a supply for the GTO control circuit.

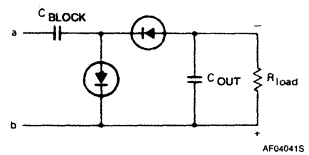
The single-transformer SRPS can be used in any of the modes of operation illustrated in Figure 8 and can provide controlled power for all the previously mentioned types of load. Because the design of SRPS circuits is complex, we have calculated the time functions for the variables V_O, V_I, I_O and I_I and used them in a closed-loop computer program to calculate the steady-state conditions for any set of input conditions. The computer program has also been used to construct a set of five universally-applicable graphs as a design aid for SRPS circuits.



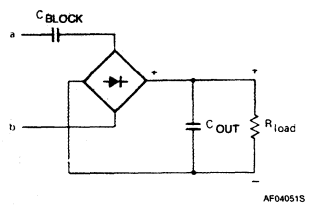
a. General Circuit



b. Circuit 1



c. Circuit 2



d. Circuit 3

Figure 6. SRPS Circuits With Capacitively-Coupled Output

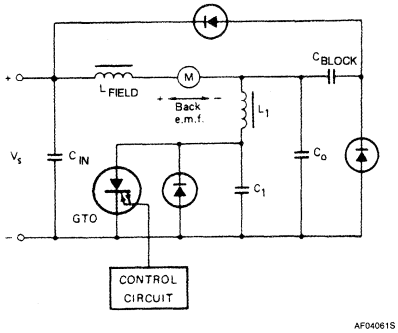
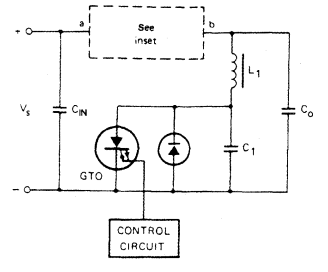
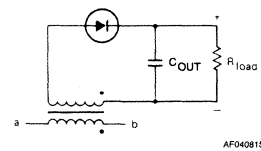


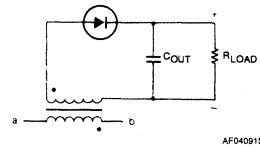
Figure 7. SRPS With Capacitively-Coupled Output Controlling the Speed of a DC Series-Wound Motor



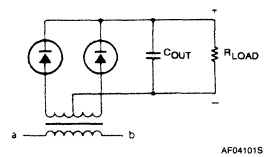
a. General Circuit



b. Circuit 1 — Forward

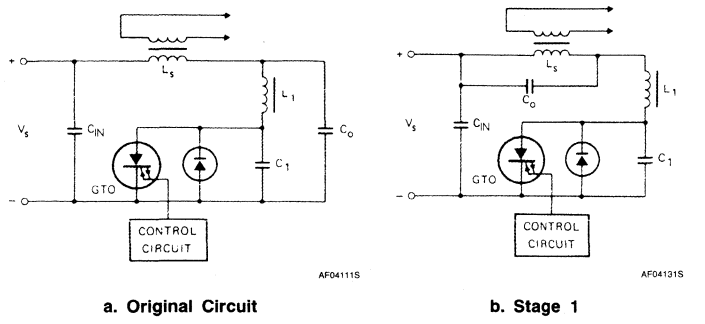


c. Circuit 2 — I^2 Flyback



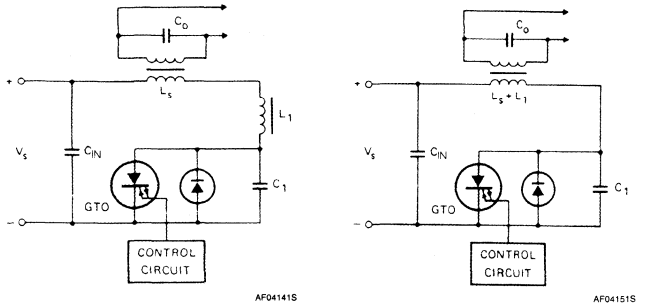
d. Circuit 3 — Forward/Flyback

Figure 8. SRPS Circuits With Transformer-Coupled Output



a. Original Circuit

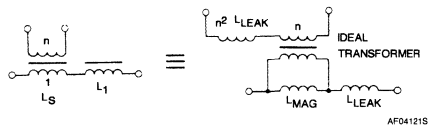
b. Stage 1



c. Stage 2

d. Stage 3

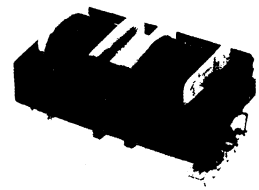
Figure 9. The Three Stages of Integrating Inductor L_1 With the Output Transformer of an SRPS



NOTES:
Approximate Relations in the Equivalent Circuit ($L_S \geqslant 10L_1$)
$L_1 = 2L_{leak}$
$L_S = L_{mag}$

Figure 10. Transformer Equivalent T-Circuit With Ideal Transformation

Power Line Isolated SRPS Output Transformer



NOTES:
Typical construction in which the leakage inductance is used for L_S. This transformer is for a 150W to 200W power supply operating at a frequency of 30–40kHz

REFERENCES

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2. Woodworth, A., *"Understanding GTO data as an aid to circuit design," Electronic Components and Applications*, Vol. 3, No. 3, May 1981.
3. Burgum, F. J., *"Basic GTO drive circuits," Electronic Components and Applications*, Vol. 3, No. 4, August 1981.

AN1211
A Microprocessor Controlled Switched-Mode Power Supply

Application Note

INTRODUCTION

With the proper interfacing, a microprocessor can be programmed to form a closed loop feedback controller for a switched-mode power supply. This application note describes the use of the Signetics switched-mode power controller, the NE5560, in conjunction with the 8048/8748 microprocessor to achieve a selectable regulated DC output voltage with value set by keyboard entry or software. The circuit described operates on a nominal +15 volts with output variable from 17 to 70 volts DC. Additional circuits describe the use of programmable buck and negative output boost supplies but having a closed analog loop.

OPERATION: THE SMPS SECTION

The switched-mode power supply consists of an NE5560 pulse width modulated control IC and suitable output switching devices to drive a boost converter. The converter switching frequency is fixed at 20kHz by the timing components, a 20kΩ resistor (Pin 7, 5560) and a .003μF capacitor (Pin 8). This fixes the internal sawtooth generator frequency. (See NE5560 Block Diagram Figure 1.)

Input voltage to the pulse width modulator Pin 5 provides duty cycle control, "δ", from 0 to 98% by programming the excursion of 1V to 6V. The corresponding output duty cycle change is shown in Figure 2a (PWM Transfer Function). A change in duty cycle converts directly to a change in output voltage from the power supply.

The boost or flyback converter principle states that output versus input voltage varies as the ratio $V_{IN}/1-\delta$ where 'δ' is percent duty cycle (on-time of the switching transistor). This causes output voltage to increase as duty cycle increases – very rapidly as δ approaches 98%. In this application, a limit of $\delta = 0.8$ is more practical resulting in an output equal to five times the input voltage at maximum duty cycle. The δ – max limit is fixed by the ratio of the resistor divider tied to Pin 6 as outlined graphically in Figure 2b.

A/D AND D/A INTERFACING TO THE MICROPROCESSOR

In order to control the PWM on a continuous basis from the microprocessor and accurately sense changes in output voltage, both digital-to-analog and analog-to-digital interface devices are required. The system accuracy is determined mainly by the number of data bits actively controlling an output or retrieving an analog signal. In this system both the A/D and D/A converter are 8-bit devices and therefore are capable of differentiating 256 discrete data levels in or out of the μP control unit. Figure 3 shows a block diagram of the μP-controlled SMPS.

Supply output is monitored on a continuous basis via the 8-bit NE5034 A/D converter. The NE5034 has an internal structure as shown in the block diagram in Figure 4.

A/D SENSES SUPPLY OUTPUT

The input voltage at the A/D input (supply output) is changed to an input current via the input resistor feeding Pin 15. This current is compared internally through a D/A converter with NE5034. The internal conversion process involving a successive approximation register operating in conjunction with the internal D/A is initiated when a start pulse is received from the microprocessor. At this point, the internal clock is reset and synchronized with the start pulse Diode D_1, from Pin 10 to 11, which stops the free running clock (f_{CLK} = 500kHz) on receipt of the start signal, allowing it to restart on cue. The complete analog-to-digital signal conversion will be completed 8 clock pulses later at which time the "data ready" line of the NE5034 goes low (Pin 18). (See Figure 5 "Timing".)

The data from the A/D digital lines is actually sent through a common tri-state bus, to the 8048/8748 microprocessor on receipt of the "data ready" (DR) signal from the NE5034 and a corresponding output enable (OE) from the processor part. An adjustment to activate the proper bits at +70 volts is achieved by the full scale adjust pot feeding Pin 15 of the NE5034. Full scale operation is adjusted such that a maximum of 2mA flows into Pin 15 of the NE5034. With a 5kΩ input resistor as shown in Figure 6, 10V will appear at the wiper of the full scale pot for a +70V output level.

D/A CONVERTER INSTRUCTS PWM

The tri-state bus also sends 8-bit commands to the D/A converter (NE5018) on a continual basis preceded by a latch enable (LE) from the 8048/8748 in order to update the PWM and change the output voltage of the supply.

Total cycle time is in the order of 20μs for the A/D and 2μs for the D/A. The 8048/8748 is operating at 6MHz and can initiate changes in stimulus in a few microseconds. Output voltage is continually being compared to the last value entered on the keyboard and held at this value. The SMPS will be an order of magnitude slower in response time since its switching frequency (20kHz) and the time constant of the output loop filter enter in to determine total delay.

THE WORKING SYSTEM

Figure 6 shows the schematic of the microprocessor controlled SMPS. The μP may be a mask programmed 8048 or a U-V erasable 8748 which allows greater flexibility. Note that this particular type of circuit requires the dedicated attention of the μP: that is the continuous on-line monitoring of supply output via the A/D converter with corresponding updating of the duty cycle through the D/A converter.

Output current is limited by the peak current capability of the lone output switching transistor Q_1. $I_{average}$ is typically set to half the peak inductor current (3A). This allows an input power of 22W maximum. Assuming an overall efficiency of 70%, output power is limited to 15W.

ALTERNATE CIRCUITS

μP Programmable Output Supply with Analog Feedback Loop

Figure 7 shows a block diagram of a programmable buck regulator operated from rectified AC line input ($160V_{DC}$). In this configuration, the microprocessor puts out a digital 8-bit code which selects a given reference voltage which, in turn, is summed with the converter DC output using a single op amp. The output of the op amp then drives the PWM to provide closed loop duty cycle control. Output voltage is now adjustable over a range of ≅ +16V to

A Microprocessor Controlled Switched-Mode Power Supply AN1211

+125V for a duty cycle variation of 10 to 75%.

Finally, a programmable negative output boost converter using the same general feedback arrangement is shown in Figure 8. In this case, however, a current output (NE5118) D/A converter is used. The microprocessor output now selects a negative current in the range zero to minus 2mA from the NE5118 which is converted to a positive voltage output from the NE535 op amp. Negative feedback is used as before to provide a regulated negative output voltage from the supply which again is proportional to the negative reciprocal of $(1-\delta)$ multiplied times the input voltage.

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NE5034 8-Bit A/D Data Sheet, Signetics Corporation

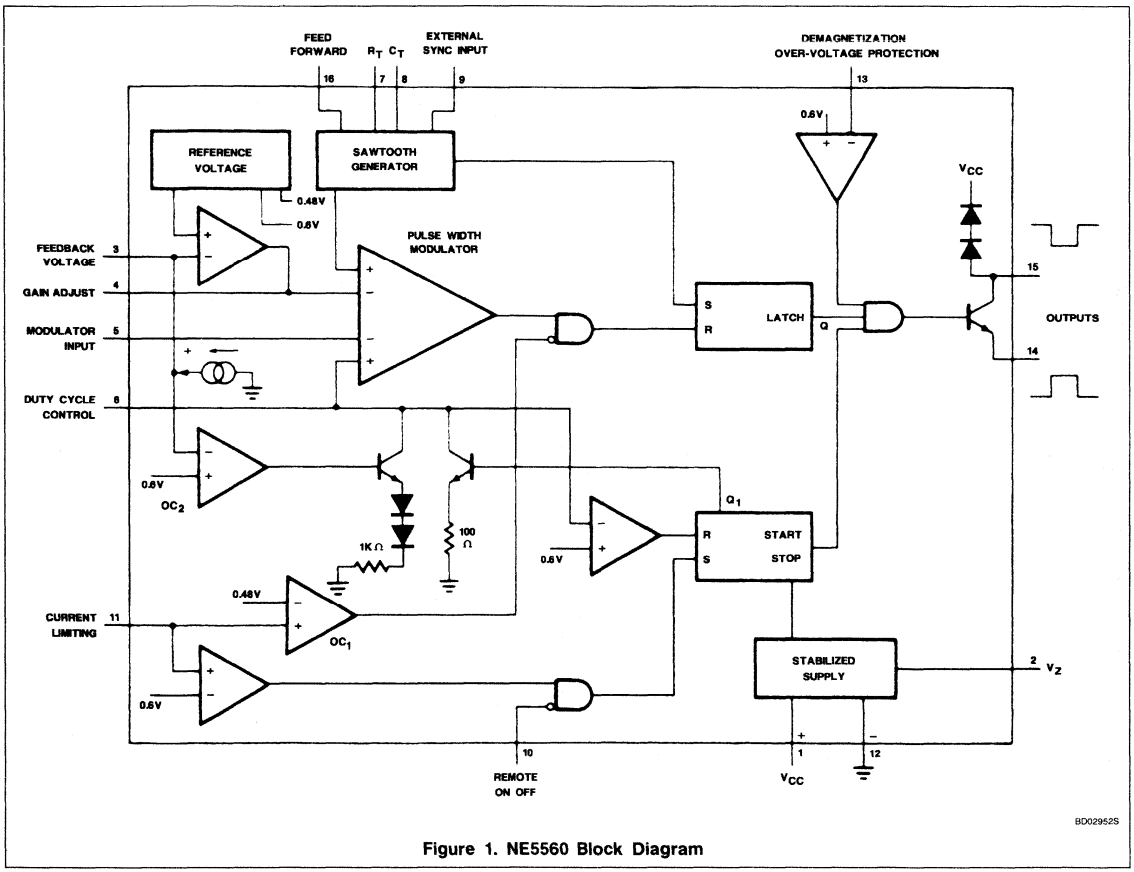
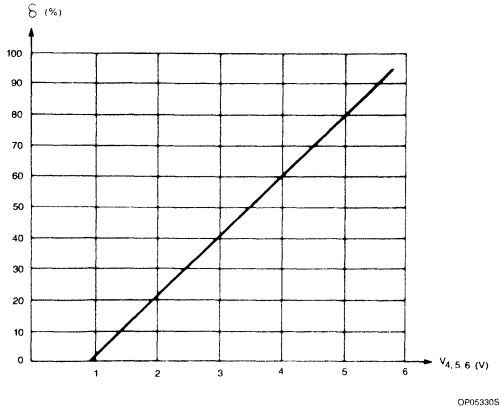


Figure 1. NE5560 Block Diagram

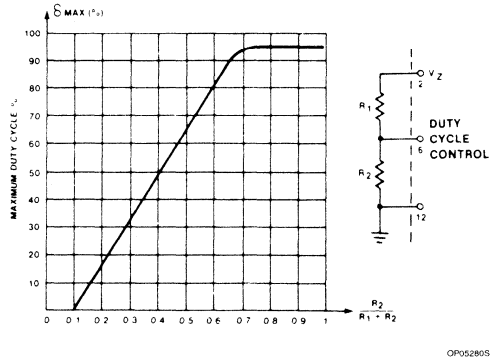
A Microprocessor Controlled Switched-Mode Power Supply AN1211

Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage



a.

Graph for Determining δ_{MAX}



b.

Figure 2

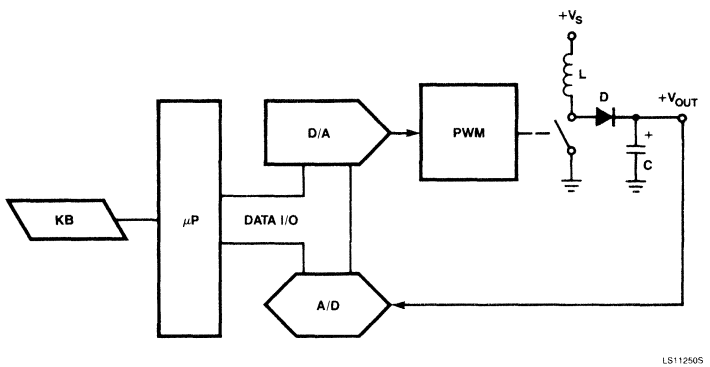


Figure 3. μP Programmable Boost Converter Block Diagram

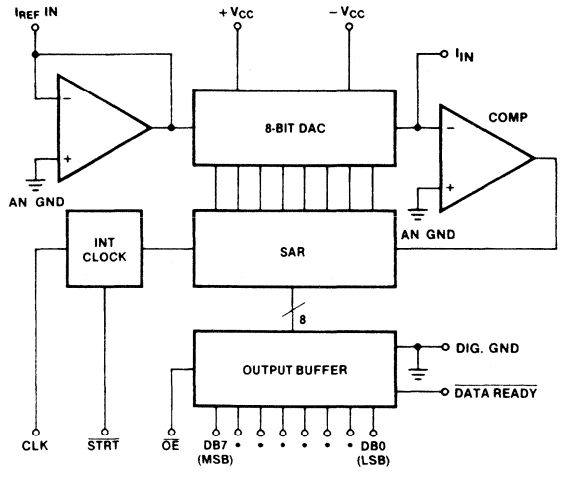


Figure 4. NE5034 A/D Converter

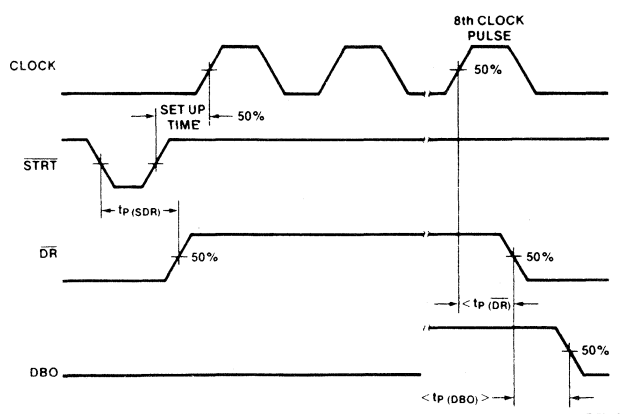


Figure 5. NE5034 A/D Timing

A Microprocessor Controlled Switched-Mode Power Supply AN1211

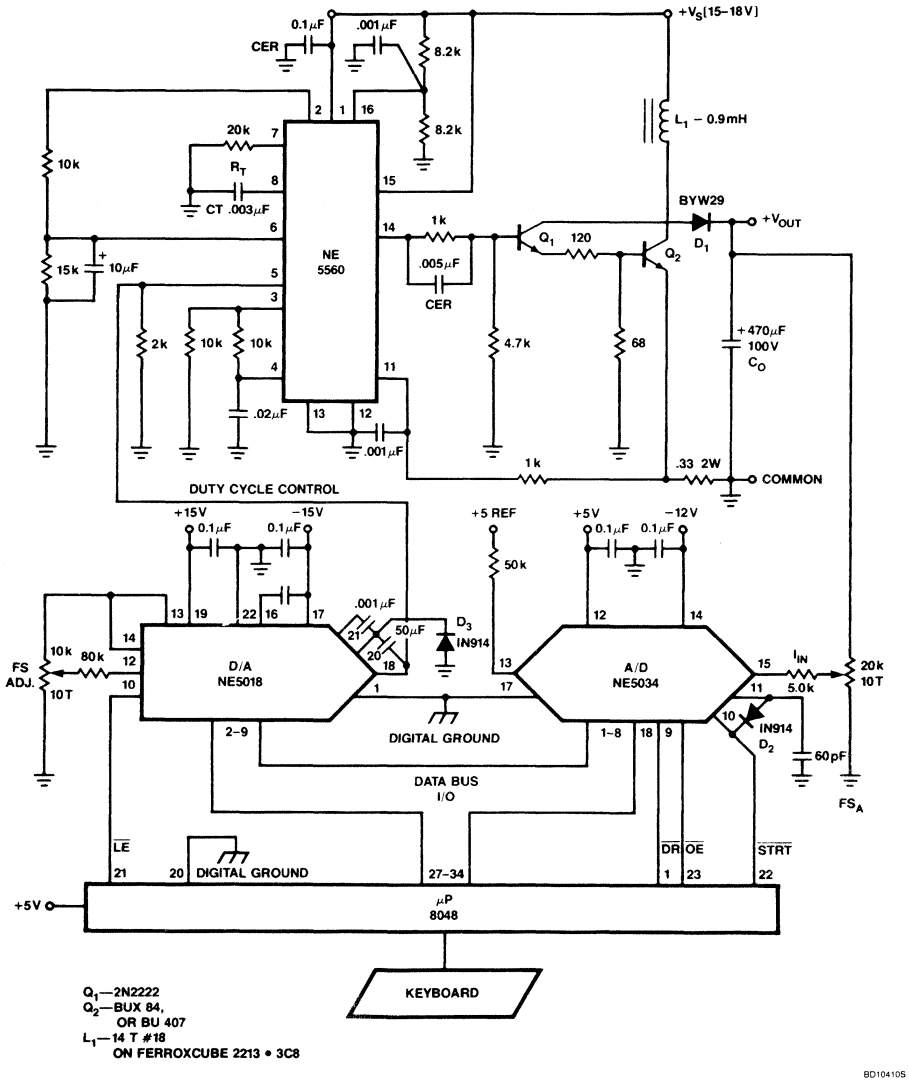


Figure 6. Programmable 17 – 20V Boost Converter Schematic

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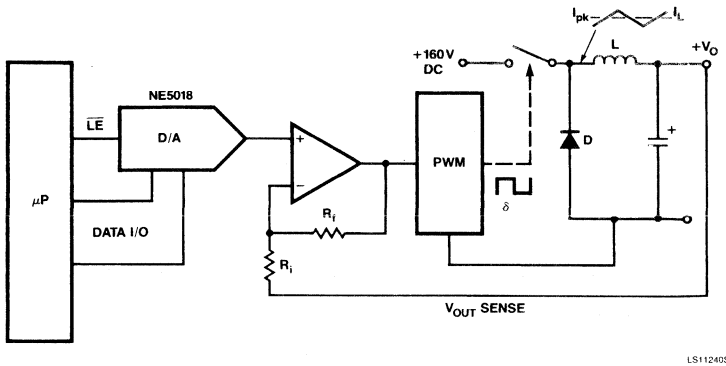


Figure 7. Programmable Reference Buck Converter

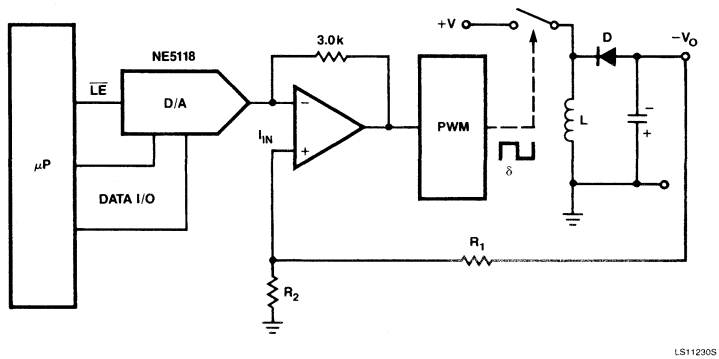


Figure 8. Programmable Negative Boost Converter

AN1221
Switched-Mode Drives for DC Motors

Application Note

ABSTRACT

The purpose of this paper is to demonstrate the use of integrated switched-mode controllers, generally used for DC power conversion, as the primary control and excitation element in practical PWM drives for DC motors. Basic principles, related to motor specifications and drive frequency, are discussed.

Finally, a series of circuit configurations are shown to illustrate velocity and position servo applications in addition to ideas on constant speed and constant torque using the NE5560 switched-mode controller integrated circuit.

PRINCIPLES OF THE PWM MOTOR DRIVE

THE MOTOR

Pulse-width-modulated drives may be used with a number of DC motor types; however, our discussion will be limited to permanent magnet field motors. This does not impose a severe restriction since PM motors are available today in a large variety of sizes, shapes, and power ratings from fractional to integral HP ranges. The PM motor, however, does have definite advantages for PWM drive as will be made evident in our discussion.

To begin with, let us look at some of the characteristics of DC motors in general, and see how these affect the design of a pulse-width motor drive.

The permanent magnet field motor may be represented in terms of a simplified equivalent circuit as shown in Figure 1.

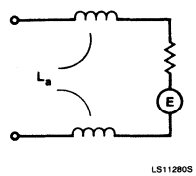


Figure 1. Typical Motor Circuit

L_A represents the total armature inductance, R is the equivalent series resistance, and E the back emf which represents that portion of the total input energy which has been converted to mechanical output. When the armature is not rotating, E = 0 and the motor is limited simply to the series armature R and L components.

Inductance, which may vary from tens of μH to mH, will have a significant effect on PWM drive designs. This is due to the fact that average motor current is a function of the electrical time constant of the motor, τ_E. Specifically, pulse current will depend upon the ratio of the pulse-width, δ*T, to the motor electrical time constant, τ_E. A motor which has high armature inductance will require a lower PWM drive frequency in order to develop the necessary torque in most instances.

As we examine the motor current waveform (shown in Figure 2) for fixed period excitation and two different motor electrical time constants, the effects are obvious. A low inductance motor allows the use of higher switching drive frequency which results in faster response.

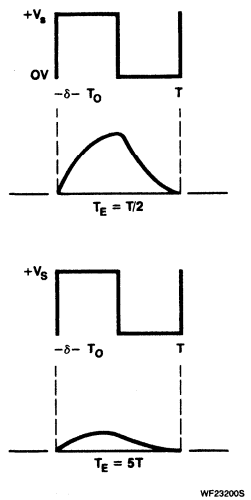


Figure 2. Instantaneous Motor Circuit

In general, then, to achieve optimum efficiency in a PWM motor drive at the highest practical frequency, the motor should have an electrical time constant, τ_E, close to the duration of the applied waveform, T. (τ_E = kT for k small.)

The printed circuit motor is probably the lowest inductance motor available since the armature is etched from a flat disc-like material much like the standard double-sided printed circuit board. These motors also exhibit very fast response and high torque. Electrical time constants in the order of 100μs allow these motors to be used with switching rates as high as 100kHz, with typical drive circuits being operated at 10kHz.

MOTOR TORQUE

Now that we have discussed the role played by PWM frequency in gaining a high enough average motor current, the control of motor torque output as it relates to motor current is required. How is torque controlled in a PWM system? The answer is by controlling the duty cycle. Frequency is held constant so pulse-width relays torque control information to the motor. Torque is dependent on average motor current which, in turn, is controlled by duty cycle (I_{ave} $\alpha\delta$). The on-time of the voltage waveform to the motor is represented by the symbol "δ". Obviously, mechanical transient response depends on an input current.

To illustrate the general theory, a typical starting sequence will be simulated using the block diagram as reference with a manually adjusted DC level controlling the duty cycle. (Figure 3)

PWM MOTOR CONTROL

At initial start-up, the duty cycle is adjusted to be long enough to give sufficient starting torque. At zero rotational velocity (ω = 0), the back emf ϵ = 0V which causes full step voltage across the motor terminal to appear across the inductor series impedance. The initial motor current determined according to the equation:

EQ1

$$Ldi/dt + Ri = V_S[u(t)-u(t-t)],$$

where the drive signal is a variable duty cycle rectangular voltage wave with peak amplitude V_S and on-time δ (%). Motor current prior to armature rotation is shown by Equation 2.

EQ2

$$Im(t) = V_S/R[1-e^{-t/\tau}E]$$
(for $t = \delta$*T),

where τ_E equals L_m/R_t, the motor electrical time constant. Current now rises in the motor windings exponentially at a rate governed mainly by average supply voltage and motor inductance. If the pulse width is close to the τ_E of the motor as shown previously, motor current at the termination of the first pulse will

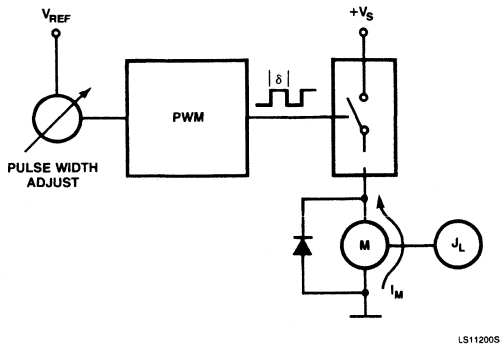


Figure 3. Simplified PWM Motor Control

reach nearly 60% of $I_{max} = V_s/R_t$. For the remainder of the PWM cycle, switch S1 is off and motor current will decay through the diode at a different rate, depending upon the external circuit constants and internal motor leakage currents, according to the equation:

EQ3

$$I(t)/decay = -I_O e^{-(t-t_O)/\tau E'}$$

The simultaneous solution of Equations 1 – 3 over many cycles will result in a figure for the average motor current, I_{ave}. This magnitude is much higher prior to armature rotation.

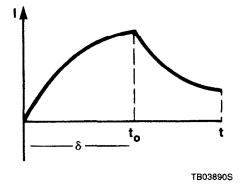


Figure 4. Motor Current Waveform

Note that motor current at the end of the cycle time, T, remains at a level, I_1, which is the starting current of the next cycle. As this sequence repeats, adequate current soon flows to cause armature rotation. As soon as rotation begins, back emf is generated which subtracts from the supply voltage. The general motor equation then becomes:

EQ4

$$L_A di/dt + R_T i = V_S(t) - \epsilon$$

For a given PWM duty cycle, δ, the motor reaches a quiescent speed, ω – rpm, governed by the negative load torque and damping friction. With the end of the starting ramp, duty cycle is reduced because less current is required than was necessary for accelerating the motor and load inertias. The torque available from the motor is now lower due to the reduced I_{ave} level and a constant rpm is reached governed by average friction and loading. Torque is related by:

EQ5

$$Torque = I_{ave} K_T,$$

where K_T = Motor Torque Constant

For a low inductance motor where the electrical time constant is much less than the duty cycle, δ, average current will be nearly equal to:

EQ6

$$I_{ave} \cong (V_S - \epsilon) \bullet \delta / R_T$$

For a motor time constant, τ_E, close to the switching period, the current will be proportionately lower as determined by the exponential current equations, (Equations 2 and 3 where,

$$V_S = ((V_t) - \delta).)$$

In summary, the principle control variable in the PWM motor control system is 'duty cycle', δ; by changing δ, motor torque and velocity may be tightly controlled. Next we shall discuss the integrated controller.

THE SWITCHED MODE CONTROLLER

For the remaining portion of the paper, the NE5560 will be the principle integrated switched-mode controller referred to. Let us examine some of its features and then see how they fit into a number of motor drive designs. The device (see Figure 5) contains an internal voltage reference of 3.72V connected to the non-inverting input of the error amplifier. The feedback signal from the motor tach or other monitoring element must be scaled to center about this positive input level. The error amplifier output, in addition to being available for gain adjustment and op amp compensation, is connected internally to the pulse-width modulator.

Frequency may be fixed at any value from 50Hz to 100kHz and duty cycle adjusted at any point from 0 to 98%. Supply is either voltage fed 11 to 18V, or current fed from 10 to 30mA. Automatic shut-down of the output stage occurs at low supply threshold – 10.5V. The error amplifier has 60dB of open loop gain, is stable for closed loop gains above 40dB. It is compensated for unity gain by adding an external .02μF capacitor from Pin 4 to ground. The switching output is single ended from either emitter (+5V max) or collector output saturated during duty cycle on-time. The device has protective features such as high speed overcurrent sense on Pin 11, which works on a cycle-by-cycle basis to limit duty cycle, plus a second level of slow start shutdown. It is this input which can be adapted to act as a motor torque limit detector.

THE OPEN LOOP PWM CONTROLLER USING THE NE5560 FOR SWITCHED MODE MOTOR DRIVE (SMMD)

For a given motor characteristic the switched-mode controller frequency should be set to allow best dynamic response considering starting current and motor electrical time constant, as discussed previously. The drive transistors must be capable of carrying peak motor current and, particularly if voltage above 50V is to be switched to the motor, these devices must be protected by snubber networks and diode transient suppressors. The new power MOS FETs provide an excellent solution to many DC drive designs since very low drive current is needed and they are self-protected from reverse transients by an internal intrinsic diode. These devices may be paralleled for added power handling capability.

Figure 6 shows a simple unipolar drive capable of driving a low voltage motor controlled by an external DC voltage to the PWM.

CONSTANT VELOCITY SERVO

Figure 8 shows in block form the general circuit used to obtain a constant speed SMMD servo. Figure 8a shows a unipolar drive using DC tachometer feedback to the PWM error amplifier. Starting torque is limited by the slow start circuit which limits duty cycle at power on. Average motor current is deter-

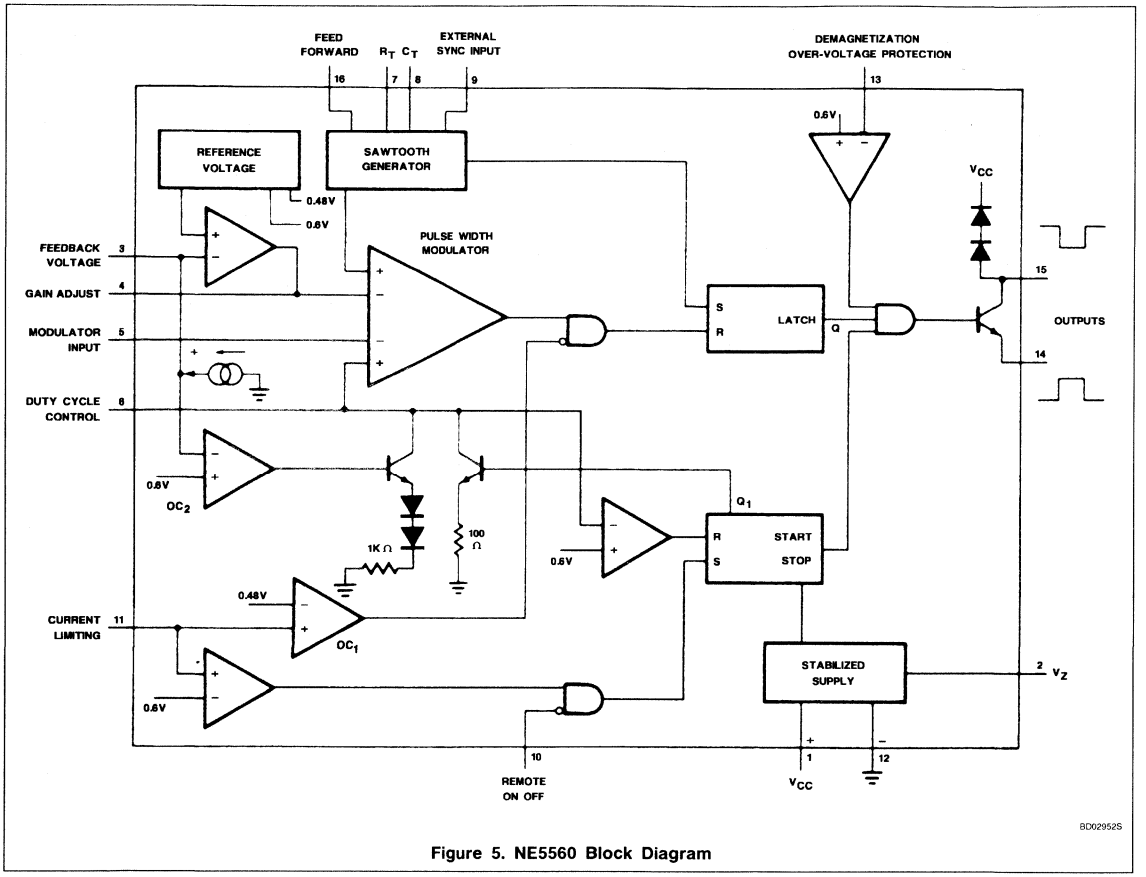


Figure 5. NE5560 Block Diagram

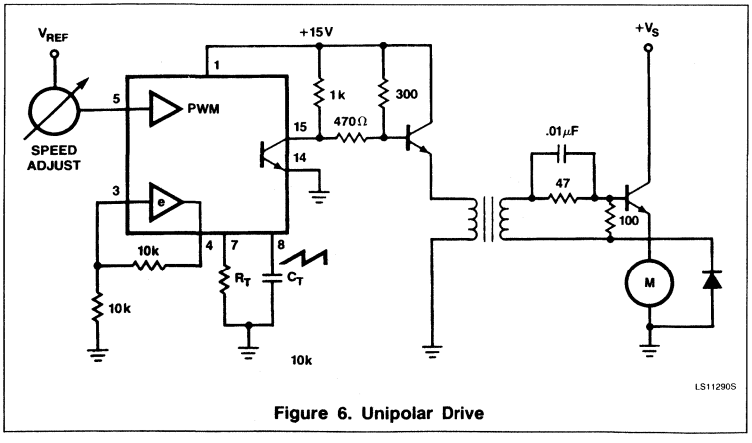


Figure 6. Unipolar Drive

mined by the duty cycle which, in turn, is governed by the speed torque characteristic of the motor as was shown in Figures 7a – 7c.

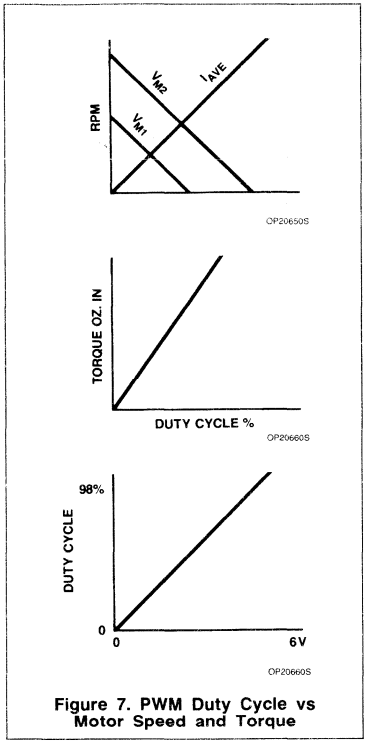
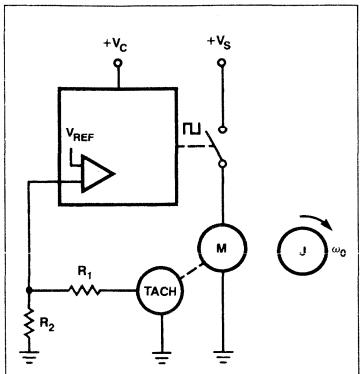
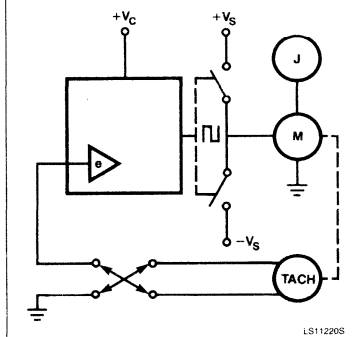


Figure 7. PWM Duty Cycle vs Motor Speed and Torque

Figure 8b shows a bi-directional drive in a half-bridge configuration. In this case the duty cycle controls the direction of motor rotation. If the average duty cycle favors the CW switch, the motor turns CW, and vice-versa for the CCW switch. This circuit form can actually be used for both velocity and position servo-designs. The reversing switch allows tach output to match the polarity of the PWM reference which is always positive.



a. Unipolar Drive with Velocity Feedback



b. Bidirectional Drive with Velocity Feedback

Figure 8

FIXED SPEED SERVO

The unipolar drive circuit in Figure 9 uses the NE5560 to develop a switched-mode motor drive (SMMD) with constant speed control suitable for small 20V motor operation. The switching drive is developed by a single IRF130 power Hex FET capable of 12 amps continuous current with a voltage rating of 100V drain to source. The PWM drive from the NE5560 is applied to the gate at a nominal 10kHz, although much higher frequencies are possible. Peak gate to source (V_{GS}) is 10 to 15V to provide minimum R_{on}. A shunt return resistor is placed in the source lead to monitor motor drive current on a cycle-by-cycle basis with resistance value set to develop +0.48V at the desired maximum current. The NE5560 then automatically limits the duty cycle, should this threshold be exceeded. This may be used as an auto torque limit feature in addition to protecting the switching device.

The network from Pin 2 (V_Z) to Pins 5 and 6 provides a simple slow start by gradually ramping up the duty cycle at power on.

DYNAMIC VARIABLE DUTY CYCLE BRAKING

R_3, R_4 sets fixed braking duty cycle control by forcing Pin 3 to remain at $\cong$ +3V, thereby causing a relatively long duty cycle for braking communication. The higher V_B is set, the shorter is the duty cycle, which results in slower braking rate. Over-current circuit is still active.

POSITION SERVO USING SMMD WITH μP CONTROL

By coupling the switched motor drive in a bi-directional drive as shown in Figure 10, and then sensing linear position with a potentiometer or LVDT connected to a lead screw, for instance, the loop can be closed on a position servo. The input to control position of the mechanical stage may be fed as a DC offset to a summing amplifier whose output is fed to Pin 5 of the NE5560, as shown. Forward lead-lag compensation may be combined with the summing amplifier function to achieve a stable response. A velocity loop may be closed through the error amplifier at Pin 3.

Note that Pin 5 may easily be interfaced to a microprocessor by means of a unipolar D/A converter working in the 1 to 6V output range.

CONCLUSION

The switched-mode motor drive, SMMD, using small, easily available, monolithic integrated control devices designed for switched-mode power, SMPS, applications may easily be adapted to perform a number of useful and efficient torque, velocity and position operations. The ready availability of good quality switching power devices in both bi-polar and power FET technology makes such designs even more effective and easily attainable by the controls systems designer.

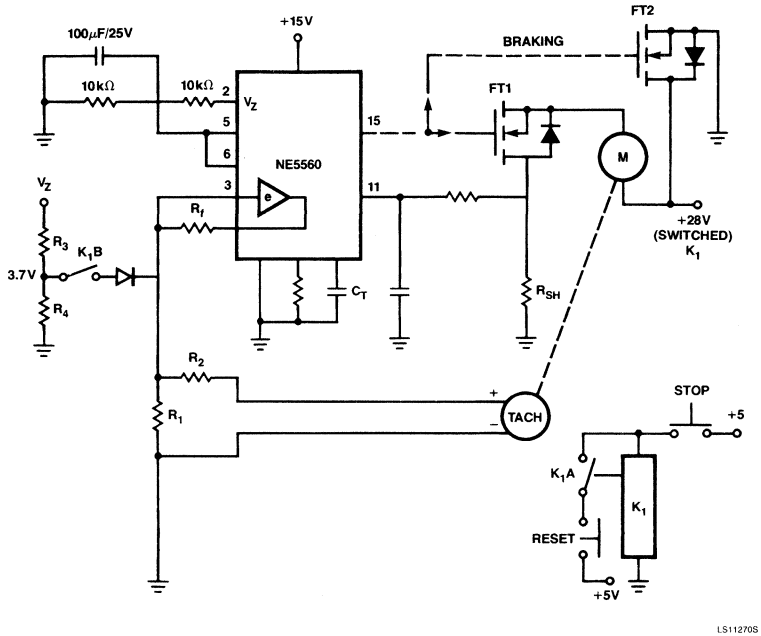


Figure 9. Basic Unidirectional Drive with Dynamic Braking

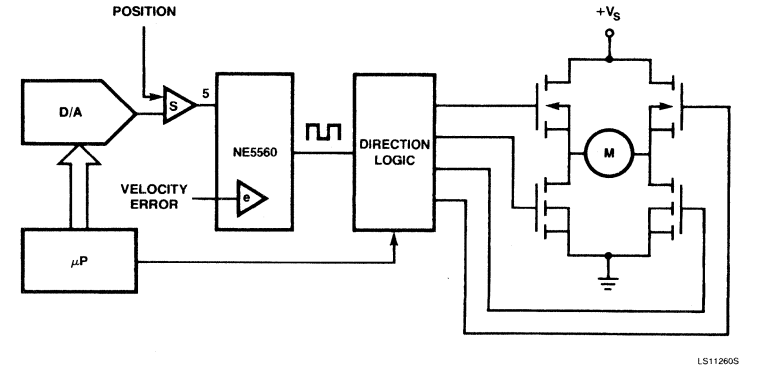


Figure 10. Microprocessor Control of PWM Drive with Four Quadrant Output

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AN1261
High-Frequency Ferrite Power Transformer and Choke Design

Application Note

PART 1: SWITCHED-MODE POWER SUPPLY MAGNETIC COMPONENT REQUIREMENTS

In switching power supplies, problems often arise with the design of the magnetic components, the ferrite-cored transformers, and chokes. The interaction between electronic and magnetic design deserves particular attention. Firstly, in switched-mode power supplies (SMPS), the power transformer and choke, and the electronic circuitry, are so interdependent that design is hardly possible without the magnetic aspects being constantly taken into account. Secondly, by combining magnetic and electronic design, a far better insight is gained into the operation of the circuit, with a consequent improvement in the design itself.

This application note covers most aspects of switching power supply design, with emphasis on the magnetic aspects. Here, the basic electrical relationships for SMPS are given for forward, push-pull, and flyback converters. Practical formulas are given for inductance and effective-current values; auxiliary outputs and other special features are also covered. Some aspects of control are treated. All treatments are related to the magnetic design.

THE FORWARD CONVERTER

Non-isolated

Principle of Operation

Figure 1 shows the outline circuit of a forward converter. The basic operation of an ideal converter is described by

$$V_O = \delta V_I \qquad (1)$$

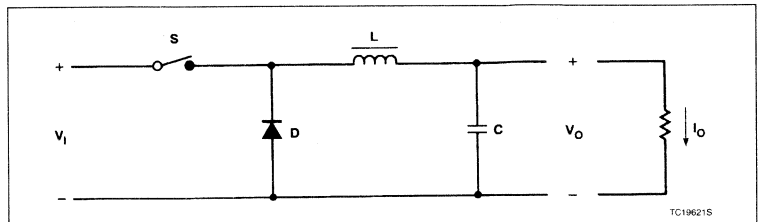


Figure 1. Outline Circuit of a Forward-Converter Switched-Mode Power Supply

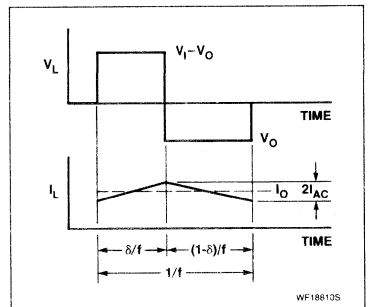


Figure 2. Voltage Waveform Across the Power Choke in a Forward-Converter SMPS, and the Associated Current Waveform

Figure 2 shows the voltage waveform across the inductance and the associated current waveforms.

NOTE:
All symbols for quantities used here are listed in the Table.

Minimum Choke Inductance

For continuous-mode operation (uninterrupted current flow through the choke) — otherwise, regulation deteriorates — output current I_O must always be greater than half the choke ripple current $2I_{AC}$. This is ensured by using a minimum value for the choke inductance

$$L_{MIN} = \frac{1}{2f}\,\frac{V_O}{I_{O\ MIN}}\left(1 - \delta_{MAX}\,\frac{V_{I\ MIN}}{V_{I\ MAX}}\right) \qquad (2)$$

An increase in δ as a result of a sudden load increase will cause a temporary increase in choke ripple current. As long as the ripple component is much smaller than the DC component, which is usually the case, this does not affect the design of the choke.

Choke Design

Output choke L carries a direct current equal to the DC current in the load. Thus, to avoid saturation, an airgap is required in the core. The design steps are:

- Determine $I_M = \sigma I_{O\ MAX} + I_{AC}$
- Calculate $I^2_M L_{MIN}$
- Proceed to Part 4 of this series.

For core loss, see Part 2.

Deriving Auxiliary Power from the Choke

During the flywheel period $(1 - \delta)/f$, that is, while the power switch is not conducting, the voltage across the choke is stabilized. By adding secondary windings to the choke, auxiliary stabilized low voltages can be obtained as shown in Figure 3.

High-Frequency Ferrite Power Transformer and Choke Design

LIST OF SYMBOLS

SYMBOL	UNIT*	DEFINITION
A_{CP}	m^2	Core center-pole cross-sectional area
$A_{CP\ MIN}$	m^2	Minimum core center-pole cross-sectional area
A_e	m^2	Effective core cross-sectional area
B_{AC}	T	Flux-density sweep; half the peak-to-peak flux density excursion
$B_{AC\ OPT}$	T	Optimum center pole peak flux density sweep for maximum throughput power
B_{CF}	mm	Coil former (or winding window) breadth
dV/dt	V/s	Maximum permissible rate of voltage increase
f	Hz	Operating frequency
f_R	Hz	Resonant frequency of transformer primary and slow-rise capacitor combination
H_{CF}	mm	Height of coil former or winding window
I_{AC}	A	Half peak-to-peak current ripple
I_E	A	RMS current at full load
I_M	A	Peak choke current
I_{magM}	A	Maximum (peak) transformer magnetizing current
I_{maxM}	A	Maximum peak inductor current
I_O	A	Power supply output (load) current
$I_{O\ MIN}$	A	Minimum required output (load) current
$I_{O\ MAX}$	A	Maximum required output (load) current
$I_{I\ M}$	A	Peak primary current
k	–	$P_{AUX}/P_{AUX\ MAX}$
ℓ_{AV}	m	Average turn length
ℓ_e	m	Effective magnetic path length in a core
L	H	Choke inductance
L_{AUX}	H	Inductance of choke with auxiliary winding
L_{MIN}	H	Minimum required value of L
L_s	H	Stray inductance of power supply output circuit
m	–	Ratio of demagnetizing (energy-recovery) winding turns to secondary winding turns
n	–	Number of turns
N	–	Number of turns in a winding portion
N_D	–	Number of turns in main choke winding
N_{PRIM}	–	Integral, rounded number of primary turns
P	W	Power
P_C	W	Total transformer core loss
P_E	W	Eddy-current loss in a core
P_H	W	Hysteresis loss in a core
P_{IN}	W	Converter input power
P_L	W	Power absorbed in a choke
$P_{O\ MAX}$	W	Maximum output power used for choke design
$P_{O\ MIN}$	W	Minimum output power used for choke design
P_{TH}	W	Transformer throughput power
P_W	W	Dissipation in transformer windings
r	–	Transformer turns ratio
θ_{JC}	°C/W	Transformer or choke thermal resistance with winding creepage distance incorporated
θ_{JN}	°C/W	Transformer or choke thermal resistance for a winding without creepage distance
t_C	s	Commutation time
t_F	s	Turn-off (fall) time of power switch
V_{AUX}	V	Voltage on auxiliary winding
V_{CEM}	V	Maximum voltage across power switch
V_{CESM}	V	Maximum collector-emitter voltage for a power-switching transistor with the base-to-emitter voltage $V_{BE} \leqslant 0$
V_e	m^3	Effective volume of a core
V_F	V	Voltage drop across output choke and leads
V_I	V	Steady state (DC) input voltage to a converter
$V_{I\ BO}$	V	'Brown-out' converter input voltage
$V_{I\ MAX}$	V	Maximum (peak) converter input voltage
$V_{I\ MIN}$	V	Minimum (trough) converter input voltage (including drop-out)
V_{IR}	V	Peak-to-peak converter input-voltage ripple
V_O	V	Output (load) voltage
$V_{O\ MAX}$	V	Maximum output voltage
V_R	V	Voltage drop of output rectifier
V_R	V	Overshoot (ringing) voltage allowance
x	%	Feedforward factor. The maximum % increase in duty factor allowed by the control in response to a sudden load change
z	–	Proportionality factor
α	–	Ratio of core saturation flux to working flux allowed: for transient response without saturation
β	–	Voltage-limiting factor
δ	–	Duty factor of power switch
δ_{MAX}	–	Maximum permitted duty factor
δ_{MIN}	–	Minimum duty factor
$\delta_{O\ MAX}$	–	Maximum duty factor under steady-state conditions
δ_{TR}	–	Transient duty factor
ΔI_O	A	Step change in load current
ΔT	°C	Temperature rise above ambient
ϵ	–	Unbalance factor
μ_a	–	Amplitude permeability at a stated mean flux density and for a stated variation
μ_e	–	Effective relative permeability
μ_0	H/m	Permeability of free space: $4\pi \times 10^{-}$ H/m
σ	–	Ratio of setting of overcurrent trip to rated output current

SUBSCRIPTS

1	Pertains to a transformer primary or (in winding design) primary winding portion
2	Pertains to a transformer secondary or (in winding design) secondary winding portion
AUX	Pertains to an auxiliary winding
CP	Pertains to center pole of an E or EC core, or to the wound leg of a U core
e	Effective value
L	Pertains to choke

SUPERSCRIPT

′	(as in r′) a preliminary (not rounded) value

* unless otherwise stated.

High-Frequency Ferrite Power Transformer and Choke Design

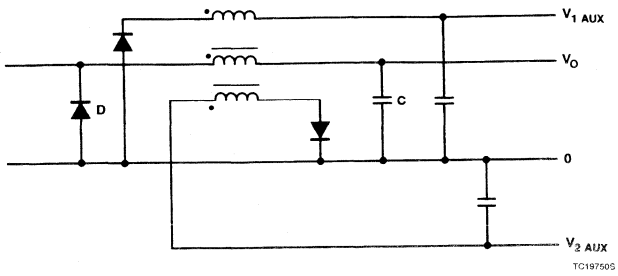


Figure 3. Auxiliary Low-Voltage Outputs can be Obtained by Adding Windings to the Choke of a Forward Converter

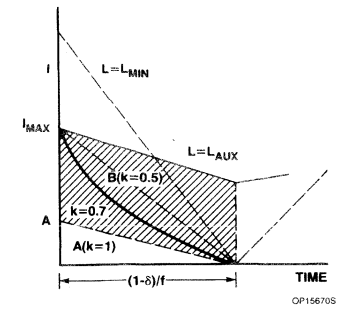


Figure 4. Current Through a Forward-Converter Choke With Auxiliary Windings

These auxiliary voltages are rectified by diodes that conduct during the flywheel period. Since auxiliary loads decrease the amount of energy recovered by flywheel diode D, the amount of auxiliary power that can be derived is limited to 20 – 30% of the total output power.

In order to store sufficient energy in the choke to supply an auxiliary load, inductance L_{MIN} calculated from Equation 2 must be increased to L_{AUX}. This might lead to the use of a larger core: see Part 4.

The relationship between L_{MIN} and L_{AUX} is

$$L_{AUX} > L_{MIN}/\left\{1 - \left((0.3 \text{ to } 0.4)\ \frac{1}{1-\delta_{MAX}} \right)\right\} \quad (4)$$

The factor (0.3 to 0.4) corresponds to an auxiliary load being 20 – 30% of the total. If output ripple is not important, a higher proportion of auxiliary load can be drawn.
The turns ratio

$$r \approx V_O/V_{AUX} = N_D/N_{AUX} \quad (5)$$

During forward conversion, during the period δ/f, the input power

$$P_{IN} = \delta V_I I_O$$

Similarly, the throughput power

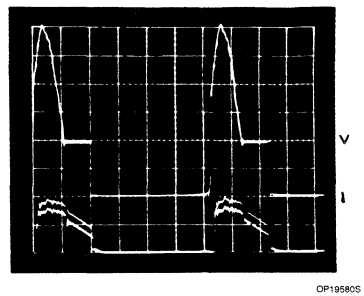
$$P = \delta V_O I_O$$

The difference is the power stored in and then removed from the choke:

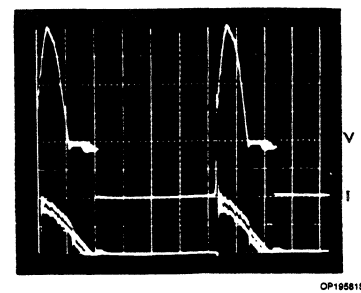
$$P_L = P_{IN} - P = \delta I_O\ (V_I - V_O)$$

From Equation 1,

$$P_L = \delta I_O\ (V_I - \delta V_I)$$
$$= \delta V_I I_O\ (1 - \delta)$$
$$= P_{IN}\ (1 - \delta)$$



a. $L > L_{AUX}$



b. $L < L_{AUX}$

NOTE:
These oscillograms were taken from a TV power supply, hence the voltage peaks.

Figure 5. Oscillogram of Choke Waveforms

High-Frequency Ferrite Power Transformer and Choke Design

If, during flywheel period $(1-\delta)/f$, the choke current is divided between output and flywheel diodes as indicated in Figure 4 by line A, P_{AUX} is maximum ($P_{AUX\ MAX}$). The current below A is that through the flywheel diode of the primary output. Figure 5 shows some waveforms.

Due to leakage induction, flywheel diode current does not begin at A, but at I_{MAX}, as the auxiliary output currents are then zero. This decreases the value of $P_{AUX\ MAX}$. If the current is shared according to line B in Figure 4, $P_{AUX} = kP_{AUX\ MAX}$, where $k = 0.5$. In practice, k will be somewhat higher: a value of $k = 0.7$ is reasonable.

If $L = L_{MIN}$, no auxiliary power can be drawn. From these considerations it follows that the auxiliary power that can be obtained is limited and depends on k, δ, and L, such that

$$P_{AUX} \leqslant k(1-\delta)\ (1 - L_{AUX}/L_{MIN})\ P_{IN}$$

The required value of L_{AUX} is obtained from

$$L_{AUX} > L_{MIN}/\{1 - \frac{P_{AUX}}{kP_{TOT}(1-\delta_{MAX})}\}$$

Substituting $k = 0.7$ and $P_{AUX}/P_{TOT} = (0.2$ to $0.3)$ yields Equation 4.

$$(P_{TOT} = P_{TH} - I_O(V_F + V_R + V_O))$$

Single Forward-Converter With Isolating Transformer

Principle of Operation

The outline circuit of a forward-converter with power line isolation is given in Figure 6.

The magnetic energy stored in the transformer while S is ON must be removed while S is OFF, otherwise the energy stored and removed during a complete switching cycle would not be zero and the transformer core would rapidly saturate. A solution involving minimum power loss is to add a winding, closely coupled to the primary, and a diode D_3 such that a flow of magnetizing current is ensured while S is OFF.

The operation of the transformer-isolated forward-converter is described by the same basic expression, Equation 1, as was used for the non-isolated version. The transformer also adds an extra degree of freedom of choice of output voltage for practical values of δ. This output voltage becomes

$$V_O = \frac{\delta V_I}{r} \qquad (6)$$

Voltage and current waveforms for a transformer-isolated forward-converter are given in Figure 7.

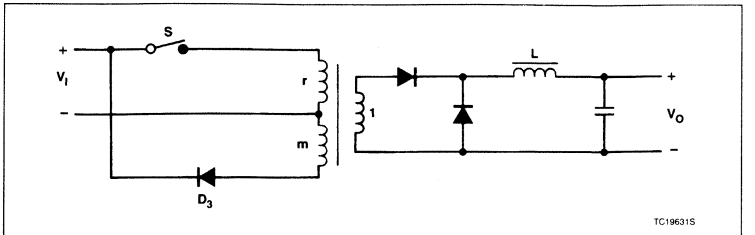


Figure 6. Outline Circuit of a Power Line-Isolated Forward-Converter SMPS

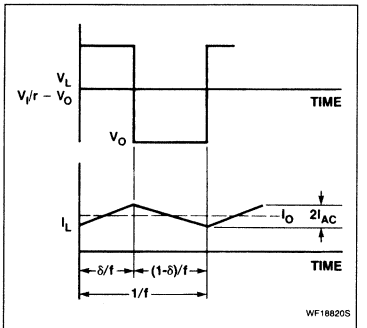


Figure 7. Output Circuit Waveforms for the Power Line-Isolated Forward-Converter

Duty Factor

The maximum allowable duty factor at which the core will not saturate due to flux staircasing depends on r and m:

$$\delta_{MAX} < 1 - \frac{m}{m+r} \qquad (7)$$

The maximum voltage across the power switch (here, a transistor) is then

$$V_{CEM} = V_{I\ MAX}\frac{m+r}{m} \qquad (8)$$

When using a transistor with $V_{CESM} = 850V$ in a forward-converter with a maximum (rectified) input voltage of 375V, it is usually adequate to limit V_{CE} to $2 \times 375 = 750V$. Thus, with $m = r$, there is 100V to spare for ringing and integrated supply voltage surges.

The effective duty factor depends on frequency, turns ratio, r, rated load current, the leakage inductance of the transformer and the inductance of the leads to the output diodes.

As a guide for power line operated SMPS, decrease the conduction time so that

$$\delta_e/f = \delta/f - rI_O \times 1.2 \times 10^{-9} \qquad (9)$$

The inductance of the leads to the output diodes is reflected into the primary as the square of the turns ratio. With large turns ratios, combined with high switching currents, the loss due to communication delay becomes substantial. The effect is as if the available duty factor is decreased.

In Figure 8a,

$$t_C \approx I_O r L_S/V_I$$

Now, L_S is about 1 nH/mm of leads and, for a 220V power line supply, $V_{I\ MIN} \approx 200V$. With the shortest possible leads to the output diodes, experiment shows that the commutation delay is

$$t_C \approx 1.2 I_O r \times 10^{-9}$$

This is an important reason for not operating low-voltage high-current SMPS at high frequencies, but, rather, to use a frequency just above the audible range.

Preliminary Turns Ratio and Core Selection

The preliminary turns ratio

$$r' = \frac{\delta_{E\ MAX}\ V_{I\ MIN}}{V_{O\ MAX} + V_F + V_R} \qquad (10)$$

For transformer core selection, see Part 2.

Multiple-Output Transformers

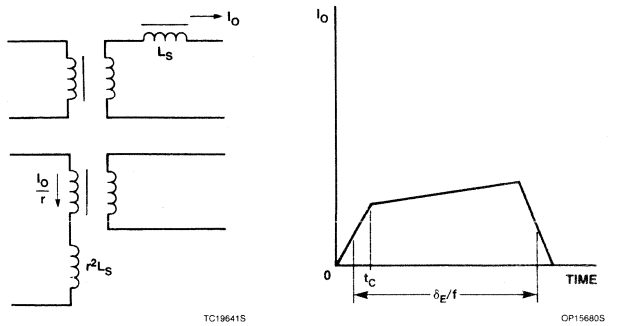
Additional outputs at any DC level can be obtained simply by adding further secondaries of the appropriate number of turns to the output transformer. The regulation of the additional outputs will be better than with a flyback converter. However, each output needs two diodes and a power choke, against the single diode needed with a flyback converter.

Warning: the flywheel diode *must* always conduct when the forward diode does not. Otherwise, peak forward-conversion rectification occurs and the output voltage could rise to the peak value of the forward-conversion voltage, which might be much higher than the nominal voltage, with disastrous results. So, ensure that the appropriate minimum load is always present at each output.

With several different outputs, it is necessary to find that value of volts-per-turn for the transformer that allows each output voltage to be obtained within the permitted tolerance

High-Frequency Ferrite Power Transformer and Choke Design

AN1261 Part 1



a. Inductance in the Secondary is Reflected Back into the Primary as the Square of the Turns Ratio

b. There is a Delay, t_C, During Which Neither Output Diode Conducts

Figure 8. Effect of Stray Inductances in the Output Circuit of an Isolated Forward-Converter

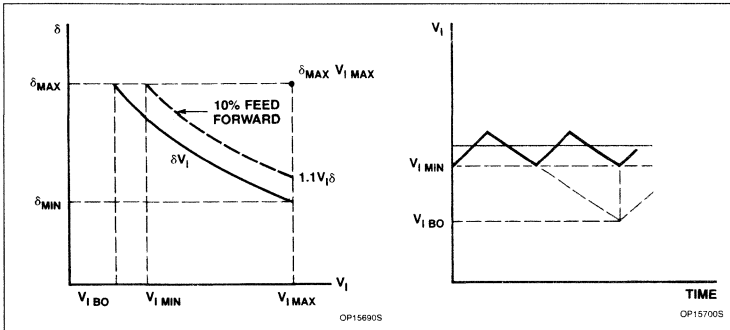


Figure 9. Input Voltage and Duty Factor Combinations Under Transient Load Conditions for Feedback and Feed-forward Control

with an integral number of turns. The procedure for this is described in Part 3.

Control Method

The function of the control circuit is to stabilize the output against variations in input voltage and load by adjusting the duty factor of the switching device. However, the effect of step load changes cannot be corrected immediately because some time is needed for the current through the choke to assume the new value of the load current.

A momentary change in output voltage is thus inevitable. The time required for resumption of the desired level of output voltage after the sudden load change depends greatly on the properties of the control system. Two basic control characteristics can be distinguished (See Figure 9).

Feedback — A step increase in load current causes the power switch duty factor to increase instantly to its maximum value δ_{MAX}, regardless of the level of input voltage. It is thus possible for $(\delta V_I)_{MAX} = \delta_{MAX} V_{I\ MAX}$.

Feed-forward — A step rise in load current causes the power switch duty factor to increase to a value x% higher than its steady-state value for a constant load.

The $(\delta V_I)_{MAX}$ product in response to a step load increase will be higher with feedback control. This results in a shorter delay in adjusting to the new load because the choke current is forced to increase at a maximum rate. However, the output transformer must be so designed that it is able to cope with the product $\delta_{MAX} V_{I\ MAX}$ without saturating.

With feed-forward control,

$$(\delta V_I)_{MAX} = (1 + \frac{x}{100})\delta_{MIN} V_{I\ MAX}$$

The corresponding value of α for the transformer design is

$$\alpha = 1 + \frac{x}{100}$$

Difficulties may be encountered with converter starting at full load with minimum power line voltage (15% below nominal). If the duty factor is close to maximum, all the output current will flow into the load and little or no current will be available to charge the output capacitor. Starting will be improved if the steady-state value of the duty factor is 10% below its maximum allowable value.

One disadvantage of feedback control is that a larger transformer core is generally required to avoid saturation.

Primary Inductance and De-Saturation

The primary inductance is given by

$$L_1 = \mu_0 \mu_a n_1^2 A_e / \ell_e \qquad (11)$$

where the value of μ_a is obtained from the core data.

The maximum, peak, primary magnetizing current is

$$I_{magM} = \frac{(\delta V_I)_{MAX}}{L_1 f} \qquad (12)$$

The peak primary current is

$$I_{1M} = \frac{1}{r}(I_O + \frac{I_{O\ MIN}}{2}) + I_{magM} \qquad (13)$$

Primary inductance L_1 together with slow-rise dV/dt capacitor C (Figure 10) across the switch forms a resonant circuit with a natural frequency

$$f_r = 1/\{2\pi\sqrt{(L_1 C)}\} \qquad (14)$$

The value of C used should satisfy the relationship

$$\frac{I_{1M} t_F}{2V_{CESM}} = C > I_{1M}/(dV/dt)$$

It is recommended that $f_r > f$. At a lower value of f_r, the core might fail to desaturate and flux staircasing could occur, with disastrous results. A higher f_r offers sufficient safety margin under all conditions; a ratio $mf_r/(rf)$ of about 1.2 is a good compromise. An electronic solution to the problem can be found in some control ICs (e.g., TDA1060) where there is a facility for reducing the duty factor when core saturation is possible.

High-Frequency Ferrite Power Transformer and Choke Design

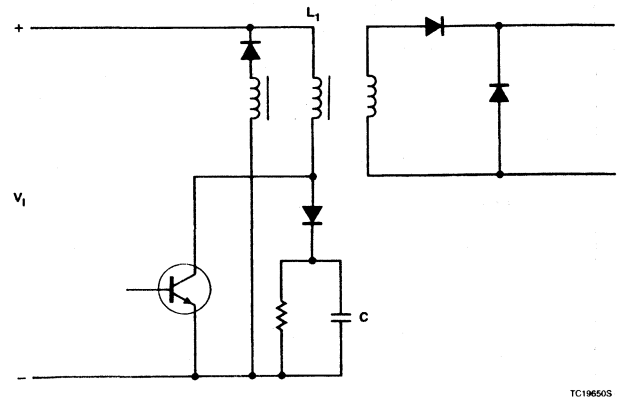


Figure 10. Forward-Converter Transformer With Magnetizing (Energy Recovery) Winding, and a Slow-Rise Capacitor in the Primary Circuit

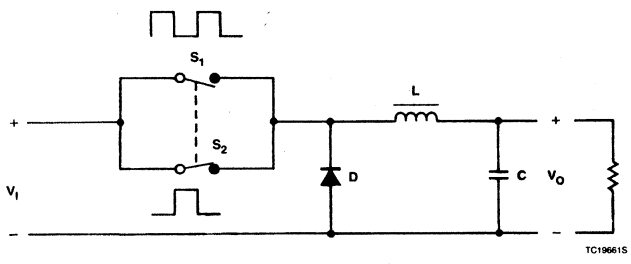


Figure 11. Outline Circuit of a Double-Forward SMPS Converter. Switches S_1 and S_2 Operate Alternately

The value and spread of L_1 may be reduced by introducing an airgap in the core; the penalty is higher magnetizing current. The spacer thickness required is generally smaller than the range for which the l^2L curves discussed in Part 4 apply. For these small values of spacer thickness S (total airgap 2S), the value of μ_e (and, thus, L_1) can be obtained for cores of *constant cross-sectional area* from

$$s = \frac{l_e}{2}\left(\frac{1}{\mu_e} - \frac{1}{\mu_a}\right) \qquad (16)$$

If it is not possible to decrease L_1 sufficiently to make $f_r > f$, the addition of a sensor winding on the transformer to generate a signal to prevent premature switch-on should be considered.

Transformer Currents

The ripple in the output choke is, in general, only a few percent of the DC load current. For this reason, the transformer current can be regarded as a square wave for the purposes of winding loss calculation.

The maximum RMS current values are given, approximately, for the primary and secondary by

$$I_{e1} = \frac{I_O}{r}\sqrt{\delta_{OMAX}} = \frac{I_{e2}}{r} \qquad (17)$$

where

$$\delta_{O\ MAX} = \delta_{MAX}\frac{V_I}{V_{I\ AV\ MIN}} \qquad (18)$$

Duty factor $\delta_{O\ MAX}$ is used in these calculations for the following reason.

For 220V power line, the minimum line voltage is roughly $185V_{RMS}$. Using an input filter capacitor of about $2\mu F/W$ (to cope with a mains drop-out of 10ms), the peak-to-peak ripple at 185V power line input is about 20V. Under these conditions the minimum average (steady-state) input voltage

$$V_{I\ AV\ MIN} = \sqrt{2}V_{I\ MIN} - \tfrac{1}{2}V_{IR} \qquad (19)$$
$$= 252V.$$

However, δ_{MAX} is set so that the converter can handle a 10ms drop-out. But mains drop-out is not a steady-state condition, so that $\delta_{O\ MAX}$ should be used to calculate I_e and, thus, the loss and consequent temperature rise of the transformer.

Choke Design

To determine the minimum required choke inductance and for the choke design, see the Principle of Operation.

Transient Response Time

The transient response time required for a forward-converter to adjust to a step in the load current of ΔI_O is

$$t_R = (\Delta I_O L)/\{(V_O + V_F + V_R)\left(\frac{\delta_{tr}}{\delta} - 1\right)\} \qquad (20)$$

The Double Forward Converter

Principle of Operation

The equivalent circuit diagram of a double forward converter is shown in Figure 11. It comprises two forward converters in parallel, with flywheel diode D and filter LC common to both. Switches S_1 and S_2 operate alternately, which doubles the ripple frequency of the choke current. Since energy is pumped twice per converter period, the output voltage is

$$V_O = 2\delta V_I \qquad (21)$$

High-Frequency Ferrite Power Transformer and Choke Design

Choke Inductance
The minimum choke inductance is calculated in a similar way to that for the single forward converter. However, since there are now two charges and two discharges per converter period,

$$L > \frac{V_O}{4fI_{O\ MIN}}\left(1 - \frac{2\delta_{MAX}V_{IMIN}}{V_{I\ MAX}}\right) \quad (22)$$

Further choke design proceeds as in section on Single Forward-Converter.

Preliminary Transformer Turns Ratio
The transformer is designed in a similar way to that for the single forward converter, except that now the turns ratio is twice as great. The preliminary turns ratio of a double forward converter transformer is

$$r' = 2\frac{\delta_{E\ MAX}V_{I\ MIN}}{V_{O\ MAX} + V_F + V_R} \quad (23)$$

Transient Response Time
The transient response time required for a double forward converter to adapt to a step in the load current of ΔI_O is

$$t_R = (\Delta I_O L)/2\{(V_{O\ MAX} + V_F + V_R)\left(\frac{\delta_{TR}}{\delta} - 1\right)\} \quad (24)$$

THE FLYBACK CONVERTER

Non-Isolated Inverting Converter

The outline circuit of an inverting flyback converter is given in Figure 12. The basic operation of an ideal inverting flyback converter is described by

$$V_O = \frac{\delta}{1-\delta}V_I \quad (25)$$

The voltage waveform across inductance L and the associated current waveforms under steady-state conditions are given in Figure 13.

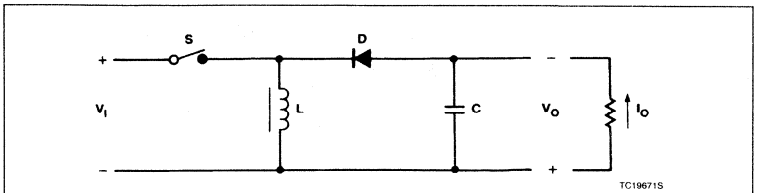


Figure 12. Outline Circuit of a Non-Isolated, Inverting Flyback Converter

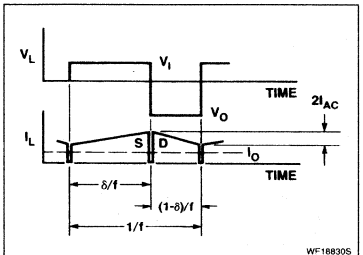


Figure 13. Voltage and Current Waveforms for the Choke of a Non-Isolated, Inverting Flyback Converter

Power Inductor
The minimum inductance required to ensure continuous-mode operation at minimum load $P_{O\ MIN}$ is

$$L > \frac{(\delta_{MIN}V_{I\ MAX})^2}{2fP_{O\ MIN}} \quad (26)$$

NOTE: use of P_O allows output diode loss to be neglected.

The maximum peak current through the inductor is $I_M = I_{DC\ MAX} + 2I_{AC}$, and

$$I_M = \frac{\sigma P_{O\ MAX}}{\delta_{MAX}V_{I\ MIN}} + \frac{\delta_{MAX}V_{I\ MIN}}{2fL} \quad (27)$$

For inductor design, see Part 4.

It is evident that the value of the inductor is inversely proportional to the minimum load. On the other hand, the choke must not saturate at maximum load if the supply voltage is minimum. Thus, continuous choke current with large output power variations is not always practical. The alternatives are:

- Pre-load the supply to decrease the ratio $P_{O\ MAX}/P_{O\ MIN}$.
- Change the operating frequency.
- Accept a discontinuous choke current at the expense of higher peak current through switch and output capacitor.

In the last case, the choke current waveform will be triangular rather than trapezoidal. For a triangular current waveform, Equations (26) and (27) become

$$L > \frac{(\delta_{MIN}V_{I\ MAX})^2}{2fP_{O\ MIN}} \quad (28)$$

and

$$I_M = 2\frac{\sigma P_{O\ MAX}}{\delta_{MAX}V_{I\ MIN}} \quad (29)$$

Proceed now with Part 4.

Non-Inverting Boost Converter

Principle of Operation
The outline circuit of a boost converter is shown in Figure 14. Its operation is described by

$$V_O = \frac{V_I}{1-\delta}$$

The voltage waveform across inductor L and the associated current waveforms under steady-state conditions are shown in Figure 15.

Power Inductor
The minimum inductance required to ensure continuous-mode operation of the choke at load $P_{O\ MIN}$ is

$$L > \frac{2}{27}\frac{V_O^2}{fP_{O\ MIN}} \quad (30)$$

The maximum peak inductor current is

$$I_{MAX\ M} = \frac{\sigma P_{O\ MAX}}{V_{IMIN}} + \frac{\delta_{MAX}V_{I\ MIN}}{2fL} \quad (31)$$

Proceed now with Part 4.

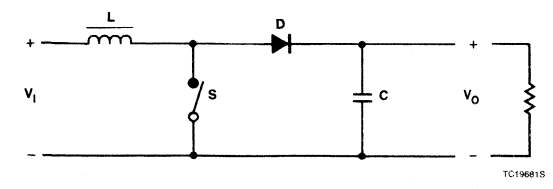


Figure 14. Outline Circuit of a Boost Flyback Converter

High-Frequency Ferrite Power Transformer and Choke Design

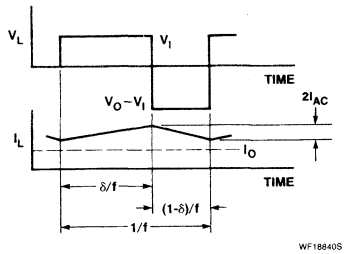


Figure 15. Voltage and Current Waveforms for the Choke of a Boost Flyback Converter

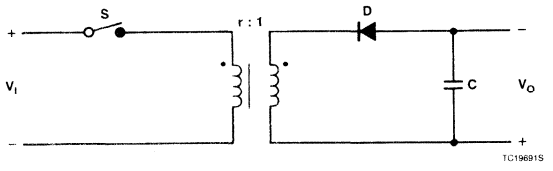


Figure 16. Outline Circuit Diagram of a Transformer-Isolated Flyback Converter

Transformer-Isolated Flyback Converter

Principle of Operation

For high-voltage low-current supplies, a useful variant of the inverting flyback converter is obtained by adding secondary windings to the choke to form a transformer, Figure 16. A further benefit of this arrangement is power line isolation.

Turns Ratio

In order to protect the switching devices, the turns ratio

$$r < \frac{V_{CESM} - (V_{IMAX} + V_f)}{V_O + V_F + V_R} \qquad (32)$$

At high voltages, such as rectified power line, a good compromise between inductor size, switching-transistor peak current, and diode peak current can usually be obtained by one of the following procedures. At moderate input voltage range,

$$\frac{V_{I\ MAX}}{V_{I\ MIN}} < 2$$

take $\delta_{MIN} = 0.3$. This yields

$$\delta_{MAX} = 1/\{1 + \frac{7}{3}(V_{I\ MIN}/V_{I\ MAX})\} \qquad (33)$$

so that

$$r' = \frac{3}{7}\{V_{I\ MAX}/(V_O + V_F + V_R)\} \qquad (34)$$

At large input voltage range, that is,

$$\frac{V_{I\ MAX}}{V_{I\ MIN}} > 2$$

take

$$r' = \frac{1}{V_O + V_F + V_R}\sqrt{(V_{I\ MAX}V_{I\ MIN})} \qquad (35)$$

This yields

$$\delta_{MIN} = 1/\{1 + \frac{V_{I\ MAX}}{r'(V_O + V_F + V_R)}\} \qquad (36)$$

NOTE: If $\delta_{MIN} > 0.3$, take $\delta_{MIN} = 0.3$ and proceed as for a small input voltage range, otherwise

$$\frac{1}{\delta_{MAX}} = 1 + (1 - \delta_{MIN})V_{I\ MIN}/\delta_{MIN}V_{I\ MAX}$$

A *voltage limiting winding* with turns ratio between primary and limiting winding r/m limits switching device voltage to $\beta V_{I\ MAX}$. The maximum duty factor must then be such that

$$\delta_{MAX} < 1 - \frac{1}{\beta}. \qquad (37)$$

where

$$\delta_{MIN} = 1/\{1 + \frac{(1 - \delta_{MAX})V_{I\ MAX}}{\delta_{MAX}V_{I\ MIN}}\} \qquad (38)$$

and

$$r' = \frac{\delta_{MIN}V_{I\ MAX}}{(1 - \delta_{MIN})(V_O + V_F + V_R)} \qquad (39)$$

with

$$m = \frac{r}{(\beta - 1)} \qquad (40)$$

Power Inductor

To ensure continuous-mode operation, design the choke primary for minimum load.

$$L < \frac{(\delta_{MIN}V_{I\ MAX})^2}{2fP_{O\ MIN}} \qquad (41)$$

The maximum peak current through the primary

$$I_{MAX\ M} = \frac{\sigma P_{O\ MAX}}{\delta_{MAX}V_{I\ MIN}} + \frac{\delta_{MAX}V_{I\ MIN}}{2fL}$$

Proceed with Part 4. The number of turns on the choke secondary, together with r, are found in Part 3.

Multiple Output

Additional output voltages at any DC level can be obtained by simply adding additional secondaries of the appropriate numbers of turns. Note that, if the range of DC output voltages is large, leakage inductance will increase and regulation deteriorate.

The design procedure is covered in the following section.

Effective Currents

The maximum value of the RMS current through the primary winding is

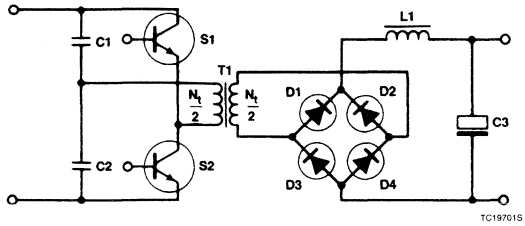
$$I_{e1} = \frac{P_{O\ MAX}\sqrt{\delta_{O\ MAX}}}{\delta_{O\ MAX}V_{I\ MIN}}\sqrt{\{1 + \frac{1}{3}\left(\frac{P_{O\ MIN}}{P_{O\ MAX}}\right)^2\}} \qquad (42)$$

and through secondary x,

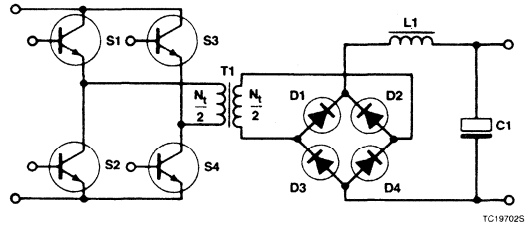
$$I_{ex} = \frac{r_x P_{OX\ MAX}\sqrt{(1 - \delta_{O\ MAX})}}{\delta_{O\ MAX}V_{I\ MIN}} \times \sqrt{\{1 + \frac{1}{3}\left(\frac{P_{O\ MIN}}{P_{O\ MAX}}\right)^2\}} \qquad (43)$$

where

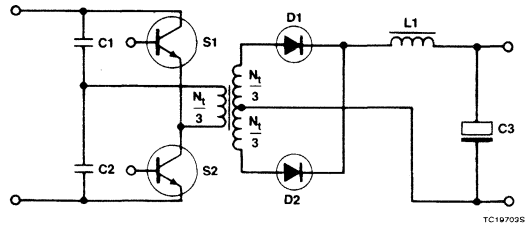
$$\delta_{O\ MAX} = 1/\left\{1 + \frac{V_{I\ AV\ MIN}}{r(V_O + V_F + V_R)}\right\}$$



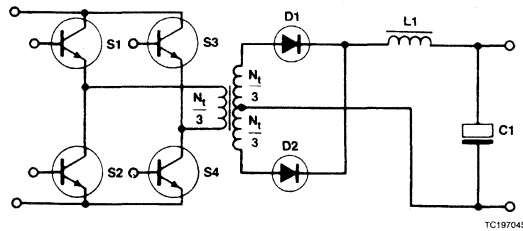
a. Two-Winding (1 + 1) Transformer in a Single-Ended Push-Pull Converter With a Bridge-Rectified Output



b. Two-Winding (1 + 1) Transformer in a Bridge Converter With a Bridge-Rectified Output

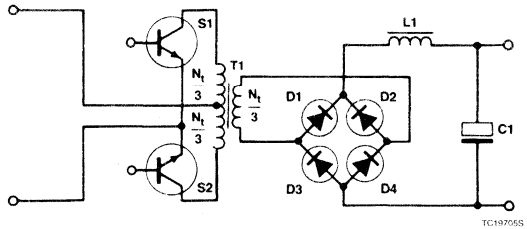


c. Three-Winding (1 + 2) Transformer in a Single-Ended Push-Pull Converter With a Bi-Phase Output

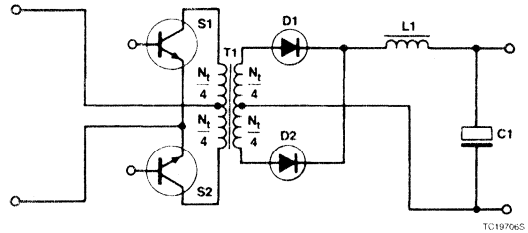


d. Three-Winding (1 + 2) Transformer in a Bridge Converter With a Bi-Phase Output

Figure 17. The Basic Configurations of Push-Pull Converters



e. Three-Winding (1 + 2) Transformer in a Push-Pull Converter With a Bridge-Rectified Output



f. Four-Winding (2 + 2) Transformer in a Push-Pull Converter With a Bi-Phase Output

Figure 17. The Basic Configurations of Push-Pull Converters (Continued)

High-Frequency Ferrite Power Transformer and Choke Design

THE PUSH-PULL CONVERTER

Principle of Operation

Outline circuits of the various basic configurations of push-pull converters are shown in Figure 17.

Since energy is pumped twice per converter period, the basic operation of a push-pull converter is described by

$$V_O = \frac{z\,\delta\,V_I}{2} \qquad (44)$$

For full bridge and conventional push-pull converters, $z = 4$; for half bridge push-pull converters $z = 2$.

The voltage waveform across the choke and the associated current waveforms are shown in Figure 18.

Duty Factor

With the equal conduction times per converter cycle, the maximum allowable duty factor is 0.5, but a more practical value is 0.45. In practice, wiring and transformer stray inductances result in a finite commutation time between output diodes. As a result, the interval during which energy is supplied to the output is shorter, and the effective duty factor smaller. This effective duty factor depends on operating frequency, transformer ratio, load current, and the stray inductance of the leads to the rectifier diodes.

To compensate for the increased commutation time, the energy transfer period δ/f should be decreased to about

$$\delta_e f = \delta/f - 1.2 r I_O \times 10^{-9} \qquad (45)$$

Transformer Turns Ratio

The preliminary turns ratio is

$$r' = \frac{2\delta_{E\ MAX} V_{I\ MIN}}{V_O + V_F + V_R} \qquad (46)$$

Power Choke Inductance

The minimum choke inductance that ensures continuous choke current, and, thus, continuous-mode operation is

$$L > \frac{V_O}{4 f I_{AC}}\left(1 - 2\delta_{MAX}\frac{V_{I\ MAX}}{V_{I\ MIN}}\right) \qquad (47)$$

Here,

$$I_{AC} = I_{O\ MIN} - I_{MAG\ M} \qquad (48)$$

and

$$I_{MAGM} = \frac{r\delta_{MAX} V_{I\ MIN} \ell_e}{2 n_1^2 \mu_O \mu_e A_e f} \qquad (49)$$

During transistor conduction, Figure 19, the magnetizing current changes from $+I_{MAG\ M}$ to $-I_{MAG\ M}$. While both transistors are off, during the interval ($\frac{1}{2}f - \delta f$) the transformer primary is open circuit. This forces the magnetizing current to flow through the output diodes in series. Thus, the load and magnetizing currents converge in one diode and cancel in the other.

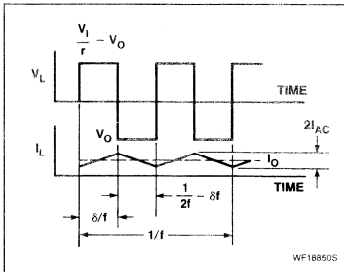


Figure 18. Voltage Waveform Across the Choke of a Push-Pull Converter Together with the Associated Current Waveforms

If, at low output current, one diode ceases to conduct, there is no path for the magnetizing current, which is then diverted through the conducting diode and the output choke to the output capacitor. This causes the output voltage to rise. From this, it follows that the minimum load current that can be drawn from the converter without one diode ceasing to conduct in this way is

$$I_{O\ MIN} = I_{MAGM} + I_{AC}$$

The magnetizing current flowing through the output diodes is

$$I_{MAGM} = \frac{\delta_{MAX} V_{I\ MIN} r}{2 L_1 f}$$

where

$$L_1 = n_1^2 \mu_0 \mu_e \ell_e / A_e$$

These two expressions together yield equation 49.

From Figure 19, the peak current through the power choke is

$$I_M = \sigma(I_{O\ MAX} + I_{O\ MIN} + I_{MAGM}) \qquad (50)$$

Further choke design proceeds with Part 4.

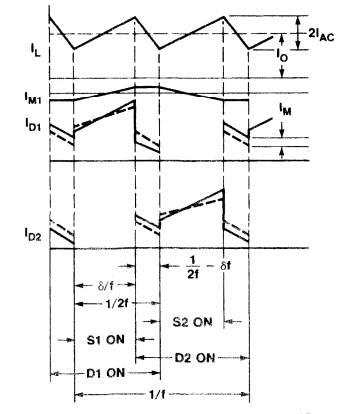


Figure 19. Waveform for Calculating the Peak Choke Current of a Push-Pull Converter

Transformer Currents

In a push-pull transformer, only one half of the double winding conducts at a time. The peak current through each half of the double winding is

$$I_{1M} = 1_M / r$$

The effective primary current in each winding half is

$$I_{e1} \approx \frac{I_O}{r}\sqrt{\delta_{O\ MAX}} \qquad (52)$$

and, in the secondary,

$$I_{e2} \approx I_O\sqrt{\delta_{O\ MAX}} \qquad (53)$$

where

$$\delta_{O\ MAX} = \frac{\delta_{MAX} V_{I\ MIN}}{V_{I\ AV\ MIN}}$$

Transient Response Time

The transient response time required for a push-pull converter to adjust to a step in the load current of ΔI_O is

$$t_r = (\Delta I_O L)/2\ (V_O + V_F + V_R)\ \left(\frac{\delta_{tr}}{\delta} - 1\right) \qquad (54)$$

High-Frequency Ferrite Power Transformer and Choke Design

AN1261 Part 2

PART 2: SWITCHED-MODE POWER SUPPLY MAGNETIC CONSIDERATIONS AND CORE SELECTION

CORE SELECTION

Available ferrite core types cater for a wide range of SMPS application requirements. The preferred grade of ferrite for high-frequency power applications is Ferroxcube 3C8: a range of cores in this material is listed in Table 1, together with the principal data required by a designer. All symbols for quantities used are listed in the Table below.

If the proper core for a given application is to be selected, a number of factors should be taken into account. The type of converter circuit used, for example, determines to a large extent the throughput power capacity of a transformer wound on a given core type.

The discussion here assumes that no pre-magnetization — magnetic bias by a permanent magnet — is applied to the core.

The selection charts given here are mainly intended for cores for push-pull and forward converter transformers. The design procedure for flyback converter transformers differs considerably, and the selection charts given here are mainly intended as a check on the core selected in Part 4.

Core Selection for Forward and Push-Pull Transformers

Selection charts 1, 2 and 3 show the throughput power as a function of frequency for a number of ferrite cores in the frequency range 10kHz to 100kHz. Note that the transformer throughput power must exceed the output power by an amount set by the efficiency of the output circuit, as discussed in Part 1.

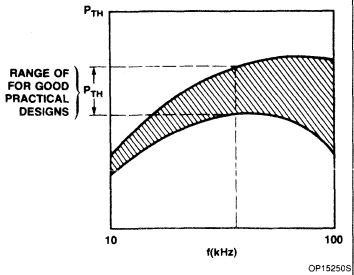
Table 1. Principal Data for Cores for High-Frequency Power Applications

CATALOG NUMBER[1]	CORE TYPE	$A_{CP\ MIN}$ (mm^2)	A_e (mm^2)	V_e ($mm^3 \times 10^3$)	l_e (mm)	B_{CF} (mm)	H_{CF} (mm)	l_{AV} (mm)	θ_{JN} (°C/W)	θ_{JC}[2] (°C/W)
4322 020 52500	EC35/17/10	66.5	84.3	6.53	77.4	21.4	4.6	53	17.4	20.0
4322 020 52510	EC41/19/12	100	121	10.8	89.3	24.4	5.5	62	15.5	17.0
4322 020 52520	EC52/24/14	134	180	18.8	105	28.2	7.5	70	10.3	11.9
4322 020 52530	EC70/34/17	201	279	40.1	144	41.3	11.5	96	7.1	7.8
4312 020 34070	EE20/20/5	23.5	31.2	1.34	42.8	10.5	3.0	38	35.4	
4312 020 34020	EE25/25/7	52.0	55.0	3.16	57.5				30.0	
4312 020 34550	EE30/30/7	46.0	59.7	4.00	66.9	16.3	4.8	56	23.4	
4312 020 34110	EE42/42/15	172	182	17.6	97.0	26.2	6.8	93	10.4	12.2
4312 020 34120	EE42/42/20	227	236	23.1	98.0	26.2	6.8	103	10.0	11.5
4312 020 34170	EE42/54/20	227	236	28.8	122	35.3	6.8	103	8.3	9.8
4312 020 34190	EE42/66/20	227	236	34.5	146	50.0	6.8	103	7.3	8.1
4312 020 34100	EE55/55/21	341	354	43.7	123	32.5	7.7	116	6.7	7.4
3122 134 90210	EE55/55/25	407	420	52.0	123	32.5	7.7	124	6.2	6.8
4312 020 34380	EE65/66/27	517	532	78.2	147	38.6	10.2	150	5.3	6.1
3122 134 90690	UU15/22/6	30.0	30.0	1.44	48.0	10.0	4.0	45	33.3	
3122 134 90300	UU20/32/7	52.2	56.0	3.80	68.0	14.5	5.5	57	24.2	
3122 134 90460	UU25/40/13	100	100	8.60	86.0	19.0	7.0	75	15.7	
3122 134 90760	UU30/50/16	157	157	17.4	111	26.0	9.0	104	10.2	
3122 134 91390	UU64/79/20	289	290	61.0	210			110/98[3]	5.4	6.2

NOTES:
1. Core material 3C8.
2. For IEC class 2 insulation.
3. Wound on both legs.

High-Frequency Ferrite Power Transformer and Choke Design

Each core is represented as a shaded area, as shown in Figure 1.



NOTE:
In the core selection charts, the power-handling capability of each core is plotted as a shaded area extending from 10kHz to 100kHz. The vertical boundaries of this area represent the upper and lower limits of throughput power capacity achievable by good design, but depending on conductor type and power line insulation requirements.

Figure 1. Power Handling Capability

The actual throughput power obtainable with a given core depends to a large extent on the following characteristics:

- The flux density sweep
- The winding configuration (simple or split/sandwiched windings, sensor or demagnetization windings, see Part 3)
- Conductor type (solid, strip, Litz, see Part 3)
- Single or multiple output
- Power line insulation requirements

The upper limit of the shaded area for each core refers to a transformer design with optimized flux-density sweep, maximum use of the winding window, and Litz wire for minimum AC resistance. The lower limit refers to a design with 8mm creepage distance for IEC 435 power line insulation, optimized flux-density sweep, a (1 + 2) winding configuration (Part 1), and optimized but solid-wire windings. In addition, the following general conditions were assumed in the calculation of both boundaries:

- The hot-spot (peak) temperature of the core is 100°C; the temperature rise is 40°C
- The maximum flux-density sweep is limited to 1/1.72 of the maximum permissible flux density for the core material (0.32T for FXC 3C8) to cope with transient conditions
- The thermal behavior of wound cores, but without potting or additional heatsinking, was assumed
- Core flux densities are calculated assuming minimum cross-sectional areas.

Thus, the selection charts are based on worst-case conditions. Where the ambient temperature is lower than 60°C, when feed-forward (Part 1) is used to ease the restriction on maximum flux density, or when heatsinking or potting are employed to improve heat transfer, throughput power capacity will be increased.

It may happen that, at a given power level, more than one type of core may be used. The following criteria may be used to make a choice:

- copper foil secondary windings are preferable for low-voltage, high-current supplies; thus, for ease of winding, a core with a round center pole should be chosen
- coil formers and mounting hardware are not available as standard for all core types
- production logistics may be improved if one core type is used for both transformer and choke.

Where these considerations do not apply, the choice of core should be guided by the discussion of Section 2.

Core Selection for Flyback Converters and Chokes

The magnetic design of flyback transformers and output chokes for forward and push-pull converters is essentially the same: the main design parameter is the energy to be stored. Core selection, therefore, is made on the basis of energy stored, $\frac{1}{2}LI_M^2$. A selection procedure based on energy to be stored is given in Part 4. This leads directly to spacer thickness and number of turns. Once a core has been chosen from Part 4, use charts 4 and 5 to check that the core chosen satisfies the throughput power requirements. If not, choose a larger core size for the design procedure in Part 4.

OPERATING FLUX DENSITY

When determining operating flux density, a distinction must be made between transformers and chokes. For chokes, and flyback-converter transformers (which also function as chokes), the most important parameter is the maximum peak flux density. The flux density sweep follows from the inductance value required.

For push-pull and forward-converter transformers, both AC and DC components of flux density must be taken into account from the start of the design process.

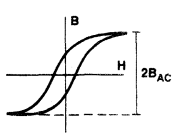
Flux-Density Levels for Forward and Push-Pull Transformers

The operating flux density of a transformer can seldom approach the maximum permissible flux density in practice since an allowance must be made for transient conditions, such as sudden load increases.

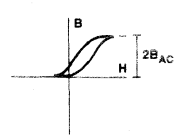
Unless special electronic measures (Part 1) are taken, a transient factor is required to cope with sudden load changes. This factor is related to the ability of the power supply to accept a range of input voltages. The input voltage range of power line operated power supplies may be 215V to 370V, or 200V to 340V; for telephone supplies, 40V to 70V; and for mobile supplies, 9V to 15.5V. The usual transient factor is 1.72.

For symmetrical excitation of the core (push-pull), the maximum possible flux-density sweep (Figure 2) is, in principle, twice that for asymmetrical excitation. In practice, however, allowance has to be made for unbalance when determining the operating flux density.

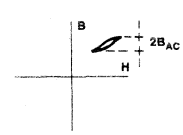
The maximum operating flux density depends on the protection circuitry. One source of unbalance is unequal flux linkage between two halves of a center-tapped winding. For this reason, bifilar windings are to be preferred. However, this is not possible in power line operated supplies since the voltage across the winding might be greater than the maximum voltage between adjacent turns.



a. Push-Pull Converter Transformers



b. Forward-Converter Transformer (With Slow-Rise Capacitor) or Ringing-Choke Flyback Converter



c. Flyback Converter Choke

Figure 2. Flux-Density Excursions and the Corresponding Flux-Density Sweeps

Table 2. Maximum Values of Flux-Density Sweep for Various Converter Types and Control Circuits

BOUNDARY CONDITIONS	FLUX-DENSITY SWEEP $B_{AC\ CP}$ (T)	
	Forward	Push-pull
Maximum sweep for FXC 3C8 (100°C)	0.16	0.32
At transient factor α	$\frac{0.32}{2^{\alpha}}$	$\frac{0.32}{\alpha}$
With unbalance factor ϵ		$\frac{0.32}{\epsilon^{\alpha}}$
With x% feed-forward	$\frac{0.32}{2(1 + x/100)}$	
With unbalance factor ϵ and x% feed-forward		$\frac{0.32}{\epsilon(1 + x/100)}$

The major reason for asymmetry is unequal conduction times or saturation voltages of the power switches in a push-pull converter. Storage effects can result in different switch-off delays. Core saturation occurring due to a delay decreases the primary inductance so that the magnetizing current rises steeply. This may lead to the destruction of the power switches. As a further safeguard, the maximum operating flux density should be decreased by an additional factor that depends on the efficiency of the protection circuit. A practical guide is a 15% allowance for a fully protected converter (unbalance factor $\epsilon = 1.15$), but a 100% allowance for an unbalanced push-pull converter ($\epsilon = 2$).

In forward converters, remanence should, in theory, also be allowed for. However, to obtain the correct primary inductance, some airgap is often useful. This airgap, together with the slow-rise capacitor (Part 1), results in the whole first quadrant of the BH loop being useful in practice, as is shown in Figure 2.

Where feedforward control is used, the transient factor can be reduced considerably and a higher flux-density sweep can often be applied.

The actual transient factor is determined by the feed-forward percentage used. Note, however, that application of feed-forward reduces the transient response of the power supply.

Practical flux-density and sweep limits are summarized for various converter types in Table 2. The curves of Figure 3, show the optimum flux-density sweep, where throughput power is maximum, for a range of cores in the frequency range 10kHz to 100kHz. Horizontal lines indicate the maximum allowable sweep for various converter types. Further lines can be added for other boundary conditions with the aid of Table 2. The given curves are calculated for a transformer temperature rise of 40°C.

The converter operating frequency is set by the required output voltage and current, and by the type of switch to be used. Once this frequency is known, the optimum flux-density sweep can be found for any core type.

Where the frequency is more or less fixed, and two core types could be used (Section 1), preference should be given to that core type for which the intersection of the optimum sweep curve with the set frequency is closest to the maximum flux density sweep.

Where frequency can be chosen freely, the frequency corresponding to the intersection of the optimum sweep curve with the line for the maximum flux-density sweep represents the optimum use of the core material.

Operation at the optimum sweeps represented by the curves of Figure 3 means that core loss and permissible winding loss are in optimum proportion. Deviation from the optimum proportion of core and winding loss, results in a lower throughput power. When the design is limited by saturation flux density, deviation is inevitable. The effect of deviation from the optimum flux density is plotted in Figure 4. This plot, which applies to any frequency, gives a rough indication of the reduction in throughput power from the optimum value. Once the optimum flux density sweep has been determined for the core and converter combination, the number of turns can be calculated as shown in the next section.

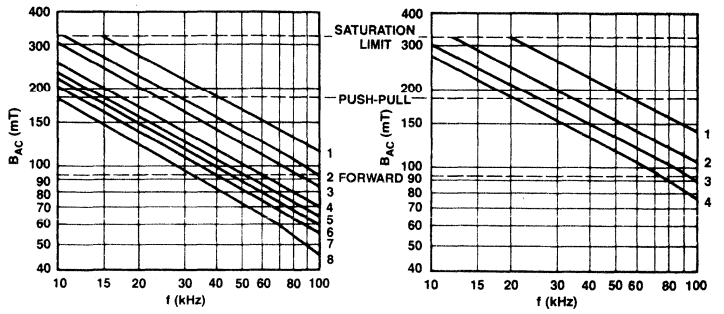
Flux Densities for Chokes and Flyback Transformers

The maximum flux density is taken into account in the design procedures given in Parts 1 and 4. The design centres around the maximum stored energy $\frac{1}{2}LI_M^2$ in the choke, which, in turn, is related to the inductance value from which follows the number of turns.

The flux-density sweep in chokes is generally relatively low, and so, in consequence, is the core loss. It may happen, however, especially in ringing choke flyback converters, that the flux-density sweep is comparable to that in forward converters. Core loss is not then negligible and should be calculated as shown in the section on core loss.

Once core type, spacer thickness, and number of turns have been established, the peak flux-density sweep can be calculated:

$$B_{AC\ CP} = \frac{LI_{AC}}{N_{PRIM}\, A_{CP}}$$



NOTE:
Horizontal lines indicate the limits for various converter types, with $\alpha = 1.72$. The curves are calculated for a transformer temperature rise of 40°C.

Figure 3. Optimum Peak Center-Pole Flux Density Sweeps $B_{AC\ OPT}$ for a Variety of Cores for SMPS Applications

where I_{AC} is found during the design process (Part 1). In the case of a flyback transformer, all quantities refer to the primary.

If I_{AC} is relatively high, core loss will be significant.

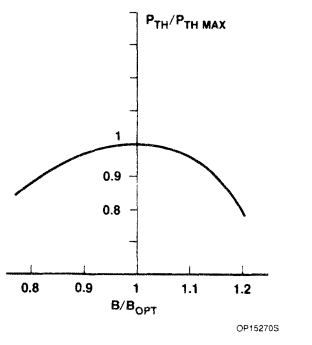


Figure 4. The Effect on Throughput Power Capacity of a Deviation in B_{AC} from the Optimum Value Indicated in Figure 3

NUMBER OF TURNS

Once the flux-density sweep is known, the number of turns can be determined.

Forward and Push-Pull Converter Transformers

The *minimum* number of turns in the secondary

$$n_{2\,MIN} = \frac{\delta V_I}{r' A_{CP\ MIN} B_{AC\ CP} f z}$$

z = 2 for forward and half-bridge push-pull converters;

z = 4 for full-bridge push-pull converters.

The values of δ and V_I are obtained from $\delta V_I = \delta_{MAX} V_{I\ MIN} = \delta_{MIN} V_{I\ MAX}$ (this and r' are found in Part 1).

$n_{2\ MIN}$ will generally not be an integer and must be rounded. If the value of $n_{2\ MIN}$ is small, rounding will change the flux density sweep significantly. To prevent saturation, rounding should be to the next higher integer. The effect of rounding can be counteracted by changing the operating frequency.

Where operating frequency is not fixed, iteration will result in a satisfactory design. When the actual flux-density sweep is within 10% of the optimum, throughput power will be within 5% of its maximum.

Use the flux-density sweep obtained after rounding to determine core loss.

Flyback Converters and Chokes

Flyback converters and output chokes: the number of turns is derived and rounded in the choke design procedure given in Part 4.

Flyback transformers: the rounded number of primary turns is found in the choke design procedure of Part 4. The value of r' is calculated in Part 1.

CORE LOSS

At frequencies approaching 100kHz, core loss has two main components: hysteresis loss and eddy-current loss. The hysteresis loss in Ferroxcube 3C8 at 100°C is

$$P_H \approx 16.7\ f^{1.3} B^{2.5}_{AC\ EM} V_e$$

This expression applies between 10kHz and 100kHz for both symmetrical and asymmetrical excitation, and for both sine and square wave fields.

The eddy-current loss for Ferroxcube 3C8, under the same conditions, is

$$P_E \approx 0.8 f^2 B^2_{AC\ EM} A_e V_e$$

The contribution of eddy-current loss in the core is greatly dependent on core size, frequency and flux density sweep. Below 100kHz, eddy-current loss may be neglected for small cores. However, for the larger cores, such as the E65 and EC70, eddy-current loss becomes important at much lower frequencies.
For very large cores, with center-pole diameters exceeding 35mm, the expressions for both P_H and P_E do not hold, even below 100kHz.

In the above expressions, $B_{AC\ EM}$ is the peak effective flux density sweep. It is related to $B_{AC\ CP}$ by

$$B_{AC\ CP} A_{CP} = B_{AC\ EM} A_e$$

For cores of constant cross sectional area, such as most E and U cores, $B_{AC\ CP}$ and $B_{AC\ EM}$ are similar in value, but they differ significantly for EC cores.

High-Frequency Ferrite Power Transformer and Choke Design

THERMAL RESISTANCE

In order to determine the maximum permissible dissipation of a transformer or choke, its thermal behavior must be known. This depends on core size, conductor form, and insulation requirements. Table 1 gives two values for thermal resistance: with and without creepage distance allowance at the ends of the winding.

These thermal resistances were measured with the transformer mounted on a printed circuit board with no local heat sources. They are referred to the hot-spot temperature in the middle of the center leg of the core (as deduced from the measured value on the ferrite surface).

For hot-spot temperatures up to 100°C, the maximum permissible winding dissipation may be obtained from:

$$P_W = \frac{\Delta T}{\theta_J} - P_C$$

This expression may be used for any ratio of core to winding dissipation.

In a choke with a large DC component of current, where core loss is negligible, $P_W = \Delta T/\theta_J$.

The temperature rise should be checked again once the winding design is complete. Winding design is treated in Part 3 for transformers and Part 4 for chokes. If the actual temperature rise is too high, the estimated throughput capacity was optimistic and a larger core should be used.

DATA NECESSARY FOR WINDING DESIGN

Before it is possible to move to the design of the windings, the following data should be available.

Forward and push-pull converters

- Core type(s)
- Coil former dimensions
- Power line insulation requirements
- Preliminary turns ratio (Part 1)
- Rounded number of secondary turns
- Operating frequency
- Secondary current and waveform
- Winding dissipation permitted
- Other windings — auxiliary outputs or sensor windings.

Flyback Transformers

- Core types (Part 4)
- Coil former dimensions
- Number of primary turns (Part 4)
- Preliminary turns ratio (Part 1)
- Operating frequency (Part 3)
- Primary and secondary currents and waveforms
- Other windings — sensor or auxiliary outputs
- Winding dissipation permitted
- Core loss
- Power line insulation requirements

Output and Flyback Chokes

- Core loss

Proceed to Part 4 for remaining design.

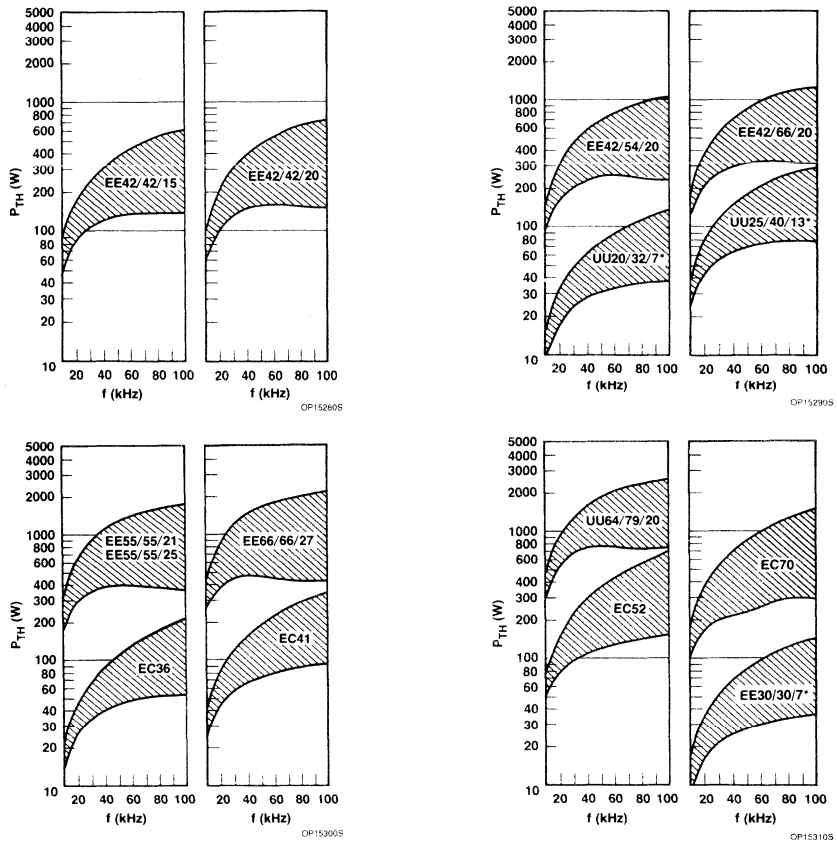
CORE SELECTION CHARTS

These charts allow an initial selection to be made of the appropriate ferrite core for a particular SMPS application. The upper limit of the shaded areas represents the performance of the core under ideal conditions: Litz wire windings and the whole of the winding window devoted to power transfer windings. Thus, there are no auxiliary windings, such as energy-recovery (demagnetizing) windings, and no allowance for creepage distance. The lower limit of the shaded area corresponds to the minimum performance to be expected from a basic, practical design. Thus, allowance is made for creepage distance, 30% of the remaining window is assumed to be occupied by auxiliary windings (non-power transfer windings), and the winding design is assumed to be optimized as shown in Part 3 of this series, but of simple construction. For both boundaries, optimum flux-density sweep is assumed.

NOTE:
*Cores marked with an asterisk have insufficient winding breadth for creepage distance for IEC 435 power line isolation.

THROUGHPUT POWER CORE SELECTION CHART 1

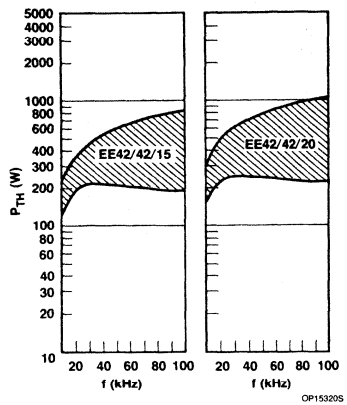
Forward Converter

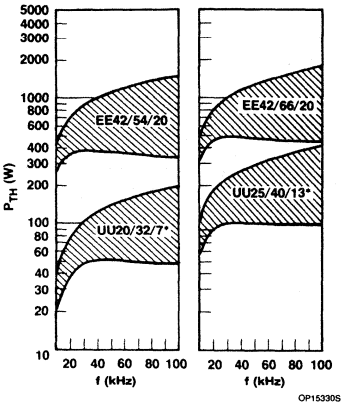


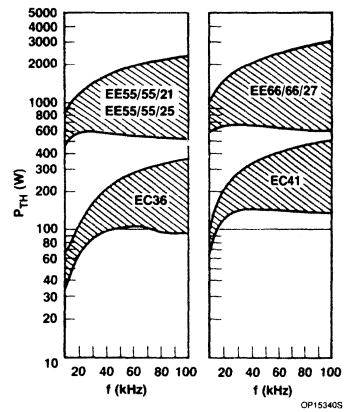
NOTE:
*Without creepage allowance.

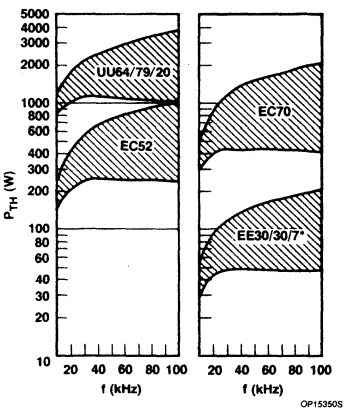
THROUGHPUT POWER CORE SELECTION CHART 2

Balanced Push-Pull Converter





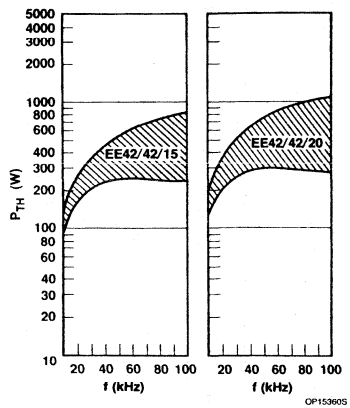


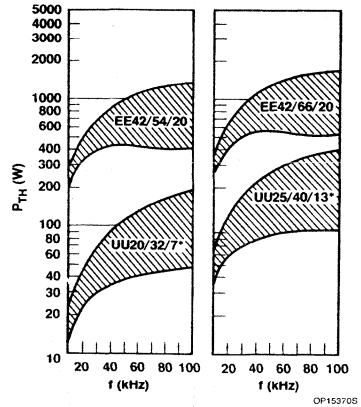


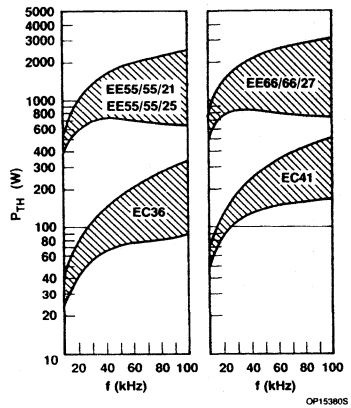
NOTES:
In order to obtain the performance indicated here, great care in both converter design and transformer winding layout is required to ensure that core excitation remains symmetrical. Any asymmetry could result in saturation of the core and destruction of the power switches in the converter.
*Without creepage allowance.

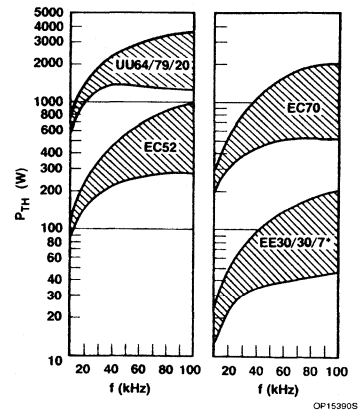
THROUGHPUT POWER CORE SELECTION CHART 3

Unbalanced Push-Pull Converter





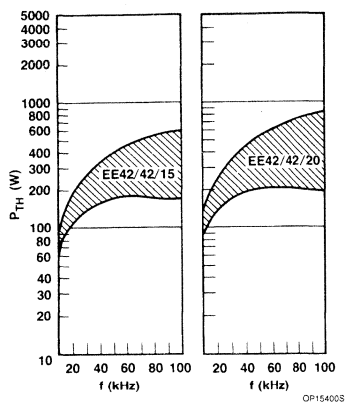


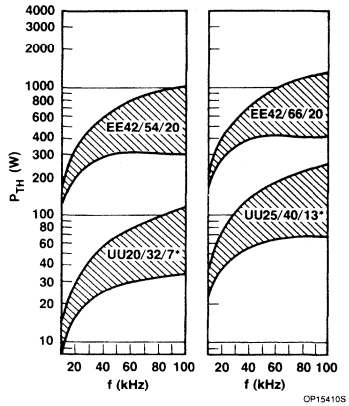


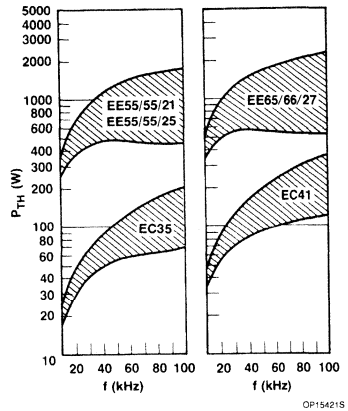
NOTE:
*Without creepage allowance.

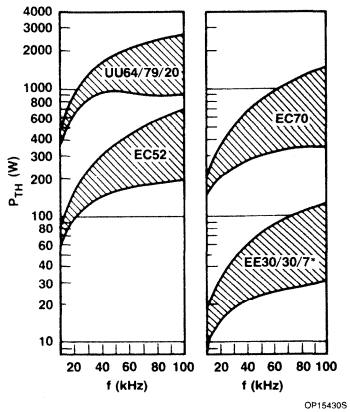
THROUGHPUT POWER CORE SELECTION CHART 4

Flyback $\gamma = 1^{+}$





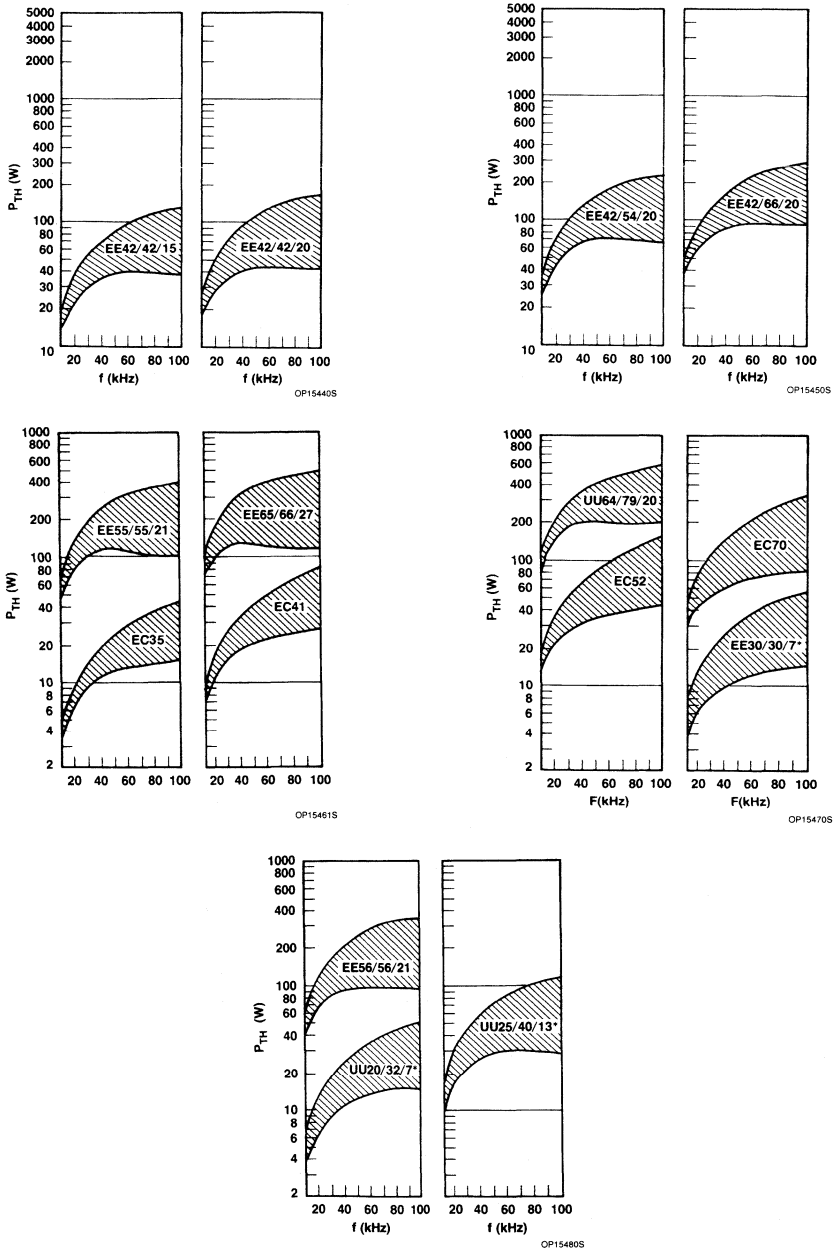




NOTES:
These charts are intended as a guide only: the choke selection procedure in Part 4, based on stored energy, should be used to make the choice of core. These charts can be used to check that choice.
$^{+}$ γ is the ratio of minimum to maximum load current for good regulation at constant duty factor.
*Without creepage allowance.

THROUGHPUT POWER CORE SELECTION CHART 5

Flyback $\gamma = 0.25$ +



NOTES:
+ γ is the ratio of minimum to maximum load current for good regulation at constant duty factor.
*Without creepage allowance.

High-Frequency Ferrite Power Transformer and Choke Design

PART 3: TRANSFORMER WINDING DESIGN

INTRODUCTION

At ultrasonic frequencies, the simple design rules used for low frequency transformer winding design are no longer valid.

Winding resistance and thus winding loss are increased through eddy-current effects — the proximity effect. At power line frequencies these effects can be ignored.

The design methods and aids presented here aim at finding the optimum winding design: that is, the winding geometry that yields lowest loss.

In drafting these design aids, the number of decisions made for the designer has been restricted to a minimum. He thus obtains a maximum of freedom of choice.

The essential background information will be given after presenting practical design procedures.

A certain amount of background information is required to use that freedom properly.

DEFINITION OF THE PROBLEM: BOUNDARY CONDITIONS

Given Boundary Conditions

The following boundary conditions are set once a core is selected:

- Frequency
- Primary and secondary RMS currents
- Primary and secondary turns numbers
- Winding breadth
- Available winding height
- Permissible winding loss

Coil former and winding dimensions are defined in Figure 1 and the List of Symbols which is on the following page.

These parameters can only marginally — if at all — be varied in winding design, therefore, they are termed given boundary conditions.

Winding breadth b_W follows from coil former breadth B_{CF} and the required creepage allowance c as set by the insulation standard. Available winding height is the height of the winding window H_{CF} in the coil former less the height occupied by the screens with the insulation, and the auxiliary windings (control windings not taking part in power transfer.) This available height should accommodate the power-transfer windings. It is not possible to determine beforehand the maximum height of individual windings.

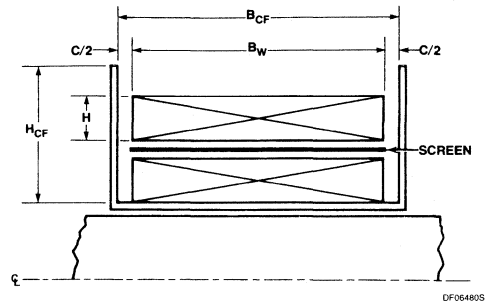


Figure 1. Definitions of Coil Former and Winding Dimensions

Chosen Boundary Conditions

In the winding design process the designer can make his own choice of

- Winding configuration
- Conductor form (wire, strip, bunched wire, etc.)

At the moment of choice, it is not always clear which choice is best. When an inexpensive design has an acceptable loss it may be preferable to a more costly design with even lower loss. it may therefore be desirable to work out more than one design by making preliminary choices for these boundary conditions.

The Design Problem

The actual winding design is now to determine the most suitable winding geometry.

Solving this problem requires (preferably convenient) means and methods to determine

— for strip windings (strip width equal to winding breadth)
  - strip thickness

— for wire windings
  - number of layers
  - wire size.

Having chosen the interleaving thicknesses, all further desired parameters can be calculated. Such means and methods are presented in this paper. For the prevailing set of (given and chosen) boundary conditions they are directed to finding the geometry giving minimum loss.

DESIGN PROCEDURES

The design process is organized in the following five phases.

I Collecting the boundary conditions.

II Determining the ideal power windings.

III Evaluating winding loss and required height. (According to the result, the design process then branches to Phase IV or Phase V, or a new start is required.)

IV Determining the optimum combination of non-ideal designs that will fit into the available height.

V Finalizing the design.

NOTE:
Here, the term "ideal" is used to describe windings designed for minimum loss regardless of the height of coil former required. Non-ideal windings have a height less than that required for ideal windings and the lowest possible loss that this height permits.

PHASE I. COLLECT THE BOUNDARY CONDITIONS

Given Boundary Conditions

Collect the given boundary conditions as set by circuit requirements and the core selected (Parts 1 and 2 of this series for forward and push-pull transformers, Parts 1 and 4 for flyback transformers).

1. Core Related:

- Operating frequency
- Maximum permissible winding loss $P_{W\ MAX}$
- Preliminary primary to secondary turns ratio r'.

For forward and push-pull transformers:

- Number of turns in secondary N_{SEC}
- Full-load RMS secondary current $I_{e\ 2}$.

For flyback transformers:

- Number of turns in primary N_1
- Full-load RMS primary current $I_{e\ 1}$
- Full-load RMS secondary current $I_{e\ 2}$.

2. Circuit Related:

- In the case of power line isolation, creepage distance c
- Data on windings other than power windings, such as demagnetizing and sensor windings
- Single or multiple secondaries.

LIST OF SYMBOLS

SYMBOL	UNIT*	DEFINITION
b	mm	Breadth of (rectangular) conductor
b_W	mm	Actual winding breadth
B	T	Leakage flux density
B_{CF}	mm	Coil former (or winding window) breadth
c	mm	Creepage distance required by the ruling insulation standard
C	–	Winding configuration factor: simple = 1; split/sandwiched = 2
C_N	–	Correction factor for N (strip windings)
C_p	–	Correction factor for p (wire windings)
d	mm	Wire diameter
d_O	mm	Overall wire diameter of enamelled wire
d_∞	mm	Optimum wire diameter for p > 1
f	Hz	Operating frequency
f_e	kHz	Effective frequency
F_g	–	Space (copper) factor in the layer breadth
F_R	–	Ratio of AC resistance to DC resistance (at a specified frequency)
h	mm	Conductor height: for solid, round wire $h = d\sqrt{(\pi/4)}$; for strip conductor, strip thickness
H	mm	Height of a winding (portion)
H_A	mm	Available height for power windings or winding portions
H_R	mm	Remaining free winding height: H_A less the combined heights of the power windings
i	mm	Thickness of interleaving
I_E	A	RMS current at full load
ℓ_{AV}	m	Average turn length
n	–	Preliminary number of turns
n_H	–	Winding-height factor for bunched wire
n_S	–	Number of strands in bunched wire
n_t	–	Winding pitch factor for bunched wire
N	–	Rounded number of turns in a winding portion

SYMBOL	UNIT*	DEFINITION
N_ℓ	–	Number of turns per layer
N_{PRIM}	–	Rounded number of primary turns
N_{SEC}	–	Rounded number of secondary turns
p	–	Number of layers
P_M	W	Winding loss margin: $P_{W\ MAX}$ minus total winding loss
P_W	W	Dissipation in transformer windings
$P_{W\ MAX}$	W	Maximum permissible winding dissipation
r	–	Transformer turns ratio
r_{AC}	Ω/m	AC resistance per unit length of conductor (under specified conditions)
r_{DC}	Ω/m	DC resistance per unit length of conductor
R_{AC}	Ω	AC resistance
R_{DC}	Ω	DC resistance
t	mm	Winding pitch
t_{MIN}	mm	Minimum winding pitch required for a given wire size
T	mm	b_W/N, winding breadth-to-turns ratio
z	–	Factor
Δ	mm	Skin thickness
θ	–	Ratio of minimum to maximum leakage flux density over the height of a winding
μ_0	H/m	Permeability of free space: $4\pi \times 10^{-}$ H/m
σ	Ωm	Resistivity
φ	–	Effective conductor height, expressed as a multiple of Δ

SUBSCRIPTS

1	Pertains to a transformer primary or primary winding portion
2	Pertains to a transformer secondary or secondary winding portion
e	An effective value
id	An ideal (optimum) value

SUPERSCRIPT

'	(as in r') a preliminary (not rounded) value.

* unless otherwise stated.

High-Frequency Ferrite Power Transformer and Choke Design

Chosen Boundary Conditions

1. *Winding configuration:* Choose between the simple configuration (where C = 1) or the split/sandwiched configuration (where C = 2). In the latter case, decide which winding will be split, and which sandwiched. (It is usual to split the winding with the larger number of turns.) Sketch the complete winding arrangement (not to scale), including any auxiliary or multiple-output windings, as in Figures 4, 18 and 20. Draw also the leakage-flux (or NI) diagram and determine for each of the power windings the value of ϑ, the ratio of minimum to maximum leakage flux density over the height of the winding. Normally $\vartheta = 0$, but in multiple output transformers it occurs that $\vartheta \neq 0$.

   In the case of a flyback transformer, draw the leakage-flux diagram for both the period of primary conduction and the period of secondary conduction.

2. *Conductor form:* Assume single round wire initially. The results thus obtained will guide the final choice of conductor.

Derived Boundary Conditions

1. *Effective frequency:* If the waveform of the current through the windings is known from previous designs, the effective frequency f_e can be obtained by analysis of the current waveform. If the waveform is unknown, assume that f_e is the switching frequency in kHz.

2. *Effective skin thickness* in copper at 100°C is

   $\Delta_e = (5.62/f_e)$ (mm)

   with f_e in kHz.

3. *Number of turns*

   a. Forward and push-pull transformers; secondary, $N_2 = N_{SEC}/C$
   primary, $n_1 = N_{SEC}r'$.
   Initially, round n_1 to the next even integer N_{PRIM}. It is essential that N_{PRIM} is even if the winding is to be split, and it avoids a further rounding if there are two layers in a simple winding. Then,

   $N_1 = N_{PRIM}/C$.

   b. Flyback transformers: A flyback transformer may use a split/sandwiched winding configuration to reduce leakage inductance, but this will not, however, reduce winding loss. The design procedures are always those for simple windings. But, of course, the number of turns of the split winding must be rounded to an even number.

   $N_2 = N_1/r'$

   rounded to an integer.

   c. Multiple-output windings

- Calculate (as described in Part 2 of this series) for the output with the lowest voltage, that is, with the smallest number of turns, and round up to the next integer.
- To obtain the number of turns for the other outputs divide the required output voltage by the volts-per-turn value for the lowest-voltage winding. Round the numbers of turns of all outputs to the nearest integer.
- Check whether the various output voltages are within the required limits with these numbers of turns.
- If not, increase the number of turns of the lowest-voltage winding by one, and repeat the calculations, starting with the volts per turn.
- When the numbers of turns for the correct output voltages have been established, correct the number of primary turns using the volts-per-turn value last found.

4. *Winding window*

   a. Winding breadth $b_W = B_{CF} - c$, see Figure 1.

   b. Available height: the height available for the *complete* power windings is H_{CF} less

- An allowance for imperfect contact between layers, interleavings and screens;
- The height of screens and their insulation (C times);
- The height of auxiliary windings handling little or no power, such as:
  - A sensor winding on the primary side of the screen that may also supply a little power for the control circuitry,
  - A demagnetizing winding.

Such windings are not designed for minimum loss. To save height, single layers are assumed of winding pitch

$t = b_W/(N + 1)$.

Choose a wire size such that $t_{MIN} \leq t$ and $d \leq \Delta_e$. Then with an interleaving of thickness i suitable for the winding pitch, the required height is

$H = d_O + i$.

The height that remains after all deductions divided by C is H_A, the height available for one primary and one secondary winding portion.

PHASE II: DETERMINE THE IDEAL POWER WINDINGS

Not yet knowing the value of p, multilayer windings are assumed initially. If, during the design procedure, this assumption proves incorrect, the design procedure switches to that for single-layer windings.

Follow the procedure below for all power windings.

Ideal Multilayer Windings of Solid, Round Wire

1. Calculate $d_\infty = \left(\frac{17.1 b_W}{N f_e}\right)^{1/3}$

2. If $\vartheta = 0$, read C_p from the table below. If p is not known, take p = 1.5 for a sandwiched winding or p = 2 in other cases.

p	1.5	2	2.5	3 to 4.5	> 4.5	if p > 3 check
C_p	1.06	1.03	1.02	1.01	1	for errors

   If $\vartheta \neq 0$, calculate

   $C_p = \sqrt{\frac{1 - \vartheta}{(1 - \vartheta^3)^{1/3}}}$

   Then calculate $d_{ID} = d_\infty C_P$.

3. Select the nearest standard wire size from a wire table and note d, d_O, t_{MIN} and r_{DC}.

4. *Number of layers:*

   a. $p_{ID} = \frac{N}{b_W/t_{MIN} - 1}$

   NOTE:
   This expression is valid only for t_{MIN} from Step 3.

   — If $p_{ID} \leq 1.5$ a strip or foil alternative may be preferable.

   — If $\vartheta = 0$ and $p_{ID} \leq 1$, the expression for d_∞ in Step 1 is not valid. Go to the single-layer winding procedure.

   b. Find p by rounding up p_{ID} to the next suitable value: to a multiple of 0.5 for a sandwiched winding, and to an integer in other cases.

   c. Calculate $N\ell = N/p$. If that value is not an integer, consider an adaptation of N to facilitate manufacture. Start again with the new value of N.

   d. If $\vartheta = 0$, check that the value of p used equals that assumed in Step 1. If not, repeat from Step 2 using the correct value of p.

5. Determine the winding pitch $t = b_W/(N\ell + 1) = pb_W/(N + p)$. $N\ell$ may not be the

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same in all layers (Step 3c); this will result in different values of t. Remember that all layers should occupy the full breadth b_W. Do not allow a difference greater than one turn in Nℓ.

6. Select a suitable interleaving, thickness i, for the winding pitch and calculate the required height $H_{ID} = p(d_O + i)$.
7. Resistance factor $F_R = 1 + \frac{1}{2}(d/d_{ID})^6$ when $d/d_{ID} < 1.25$. But when $p = 1.5$ this expression holds only for $d/d_{ID} < 1.15$.
8. AC resistance per meter length of wire $r_{AC} = F_R\, r_{DC}$.
9. Winding loss of a complete winding (of C portions) $P_W = CI_e^2 N\ell_{AV} r_{AC}$, taking for the average turn length ℓ_{AV} the value for a fully wound coil former in m.

Having found the ideal designs for all power windings using this procedure, proceed to Phase III.

Single- and Half-Layer Windings of Solid Round Wire

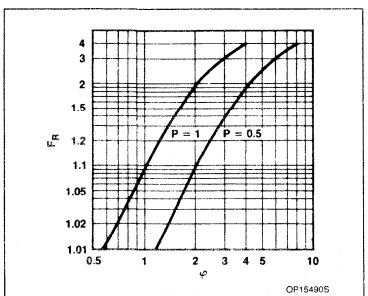
This procedure applies only when $\vartheta = 0$.

Arriving from Step 4a of the previous procedure, take $p = 1$.

1. Winding pitch $t = pb_W/(N + p)$.
2. Select from a wire table the thickest standard wire for which $t_{MIN} \leqslant t$ and note d, d_O and r_{DC}. Also choose a suitable interleaving, thickness i.
3. $H = p(d_O + i)$.
4. $\varphi = \sqrt{(0.124 f_e d^3/t)}$, ($f_e$ in kHz, d and t in mm).

NOTE:
If f_e differs from the switching frequency, use the lower value of frequency.

5. Read F_R from Figure 2. Beyond the chart, $F_R = p\varphi$.
6. $r_{AC} = F_R r_{DC}$.
7. $P_W = CI_e^2 N\ell_{AV} r_{AC}$, where ℓ_{AV} in m.



NOTE:
Above $F_R = 4$, take $F_R = p\varphi$.

Figure 2. F_R vs φ for Single- and Half-Layer Windings

In the case of a sandwiched winding, consider a strip or foil winding. If a wire winding is preferred, and if φ from Step 4 is about 4 or greater, a half-layer winding will probably have about equal r_{AC}, about half the wire size and about one quarter of the copper content; follow the above procedure using $p = 0.5$.

Having found the ideal designs for all power windings, go to Phase III.

Ideal Strip or Foil Windings

1. If $\vartheta = 0$, read C_N from the table below.

N	0.5	1	1.5	2	2.5	3 to 4.5	⩾5
C_N	1.69	1.19	1.06	1.03	1.02	1.01	1

If $\vartheta \neq 0$, calculate $C_N = \left\{\frac{(1-\vartheta)^3}{1-\vartheta^3}\right\}^{1/4}$

Then determine f_e (kHz).

$h_{ID} = C_N \sqrt{\frac{9.74}{Nf_e}}$ mm, using f_e in kHz.

2. Select the nearest available strip or foil thickness, h.
3. $F_R = 1 + (1/3)(h/h_{ID})^4$ when $h/h_{ID} < 1.4$.
4. $r_{AC} = F_R/(45 b_W h)\Omega/m$ (b_W and h in mm).
5. $P_W = CI_e^2 N\ell_{AV} r_{AC}$.
6. Select a suitable interleaving, thickness i, then $H_{ID} = N(h + i)$.

NOTE:
This procedure is for copper at 100°C, resistivity 1/45Ωmm²/m. It can be adapted to aluminium conductor (62% higher resistivity at 100°C). In the expression for h_{ID} (Step 1) replace 9.74 by 15.8; in Step 4, replace 45 by 28.

Compare P_W from Step 5 with that of the wire version of the winding, (Step 9 or Step 7) and choose the ideal solution for lowest r_{AC}. Having found the ideal designs for all power windings, go to Phase III.

PHASE III: EVALUATE THE DESIGN WITH RESPECT TO WINDING LOSS AND HEIGHT

The success of a design attempt is judged on the basis of winding-loss margin P_M and remaining free height H_R.

The winding-loss margin is calculated from $P_{W\,MAX}$ and the total loss of the power windings. The remaining free height is calculated from H_A and the heights of the power windings.

There are four possible results of the evaluation:

- *P_M and H_R both positive:* design attempt successful, proceed to Phase V.
- *P_M and H_R both negative:* boundary conditions do not permit a successful design. Make a fresh start with a higher operating frequency or a larger core, for example
- *P_M positive and H_R negative:* a frequent occurrence, especially at lower frequencies. Try non-ideal winding designs requiring less height as in Phase IV.
- P_M negative and H_R positive: reconsider the chosen boundary conditions and start again. Some basic considerations are:
  - Split/sandwiched designs offer lower loss than simple ones, especially at higher frequencies.
  - Strip or foil windings tend to have lower losses than (single-layer) wire windings.
  - If H_R is large, try replacing a single-wire winding by a multiple-wire or bunched-wire winding. Design procedures are given in the next section. A Litz-wire winding may also be possible if H_r is particularly large. Evaluate the result again.

If adoption of one of these measures results in both H_R and P_M being positive, the design is successful; if not, try a higher operating frequency or a larger core in a new design.

ALTERNATIVE DESIGNS: MULTIPLE, BUNCHED AND LITZ-WIRE WINDINGS

Ideal Multiple-Wire Windings

1. Choose the number of parallel strands n_S: usually 2 or 3.
2. Follow the design procedure for ideal multilayer windings of solid, round wire, as if the winding had $n_S N$ turns. If Step 4a results in $p_{ID} \leqslant 1$, follow the single-layer design procedure, again replacing N by $n_S N$.
3. Divide the value of r_{AC} by n_S to find the AC resistance of the n_S parallel strands.

Ideal Bunched-Wire Windings

Bunched wire consists of a few strands of insulated wire twisted together to form a bunch. The strand diameter is not so small that eddy-current loss is negligible.

The minimum winding pitch of a bunched wire of n_S strands is $n_T\, t_{MIN}$, and the layer height without interleaving is $n_H t_{MIN}$, where t_{min} is the minimum winding pitch given in the wire tables for a single strand. Values of n_t and n_h for crude experimental bunches are given for guidance in the table below.

n_S	4	5	6	7	8	9	10
n_T	2.45	2.94	2.98	3.11	3.61	3.89	4.34
n_H	2.31	2.69	2.93	2.93	3.16	3.16	3.26

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Multilayer Bunched-Wire Winding

1. Choose n_S. a bunch of 7 strands gives the best space (copper) factor.

2. If $\vartheta = 0$, read C_p from the table below. If p is not known, take p = 1.5 for a sandwiched winding, and p = 2 in other cases.

p	1.5	2	2.5	3 to 4.5	> 4.5	if p > 3 check 1 for errors
C_p	1.06	1.03	1.02	1.01		

If $\vartheta \neq 0$, calculate

$$C_p = \sqrt{\frac{1-\vartheta}{(1-\vartheta^3)^{1/3}}}$$

$$\text{Then } d_{ID} = C_p \left(\frac{17.1 b_w}{n_S N f_e} \right)^{1/3}$$

3. Select the nearest standard wire size from a wire table, and note d, d_O, t_{MIN} and r_{DC}.

4. Number of layers:

a. $$p_{ID} = \frac{N}{b_W/(n_T t_{MIN}) - 1}$$

NOTE:
The expression holds only for t_{MIN} from the previous steps. If $p_{ID} \leq 1$, the expression in Step 2 does not apply.

b. Find p by rounding p_{ID} up to the next suitable value. For sandwiched windings, round to multiples of 0.5; in other cases, round to integers.

c. Calculate $N\ell = N/p$. If this does not yield and integer, consider adapting N to facilitate manufacture. Start again using the new value of N.

d. If $\vartheta = 0$, check that the value of p found is that assumed in Step 2. If not, repeat from Step 2 using the correct value of p.

5. Winding pitch $t = b_W/(N\ell + 1) = pb_W/(N + p)$. $N\ell$ may not be the same in all layers. This will result in different values of t, since all layers should occupy the full winding breadth. Do not permit differences of more than one turn in $N\ell$.

6. Select a suitable interleaving, thickness i, for the winding pitch. The required height $H = p\ (n_H t_{MIN} + i)$ where n_H is given in the table in the section on Ideal Bunched-Wire Windings.

7. Resistance factor $F_R = 1 + \frac{1}{2}\ (d/d_{ID})^6$.

8. Resistance per meter length of bunch $r_{AC} = F_R r_{DC}/n_S$ where r_{DC} is the resistance per meter length of strand.

9. $P_W = CI_e^2 N\ell_{AV} r_{AC}$, where ℓ_{AV} in m.

Single-Layer and Half-Layer Bunched-Wire Windings

This procedure applies only if $\vartheta = 0$ and p = 1.

1. Winding pitch $t = pb_W/(N + p)$.

2. From a wire table, select the thickest strand for which $t_{MIN} \leq t/n_T$ and note d, t_{MIN} and r_{DC}. Also, choose a suitable interleaving, thickness i, for the winding pitch.

3. Required height $H = p\ (n_H t_{MIN} + i)$.

4. $\varphi = \sqrt{(0.124 n_S f_e d^3/t)}$.
NOTE:
If f_e differs from the switching frequency, use the lower of the two values (in kHz).

5. Read F_R from Figure 2. Beyond the range of Figure 2, $F_R = p\varphi$.

6. The AC resistance per meter length of bunch $r_{AC} = F_R r_{DC}/n_S$, where r_{DC} is the DC resistance of a meter length of *strand*.

7. Winding loss $P_W = CI_e^2 N\ell_{AV} r_{AC}$, where ℓ_{AV} is in m.

If φ in Step 4 is greater than or equal to about 4, a half-layer design might be preferable for a sandwiched winding.

Litz-Wire Windings

Litz-wire is here taken to be a kind of bunched wire in which the strands are so thin ($d \ll \Delta_e$) that eddy-current effects can be neglected. Its main drawback is its low space (copper) factor, often only 25% to 30%.

Litz-wire is standardized and commercially available. The standards specify numbers of strands, strand diameter, overall diameter and DC resistance.

Mechanical stress deforms the bunch so that the breadth in the layer and, thus, the minimum winding pitch are greater than the overall diameter of the bunch, but the height of the layer is smaller.

1. Knowing the winding current I_X, select a bunch of strand diameter d and number of strands n_S such that $\pi d^2 n_S \cong I_X$. The resulting current density will be about 4 A/mm^2.

2. Due to deformation, the winding pitch $t \cong 1, 2d_O$, where d_O is the overall diameter of the bunch.

3. Provisional number of layers $p' = Nt/(b_W - t)$.

4. If p' is within 10% of the next lower integer, the winding may be feasible with care with this lower value. Otherwise, take for p the next higher integer. Then calculate $n'_S = n_S(p/p')^2$.

5. Select a standard Litz-wire with the same strand diameter, and a number of strands as large as possible, but lower than n'_S.

6. The required height of the winding will be less than $H = p\ (d_O + i)$, where i is the thickness of the interleaving.

7. The DC resistance per meter length is usually given for 20°C, multiply that value by 1.3 to get the resistance at 100°C. Then calculate $P_W = CI_e^2 N\ell_{AV} r_{DC}$, using ℓ_{AV} in m.

NOTE:
If all windings in the transformer are of Litz-wire, the split/sandwiched winding configuration does not lead to lower losses.

If a suitable Litz-wire is not readily available, the above procedure can be adapted to use multiple Litz-wire using similar methods to those for multiple wire.

PHASE IV: DETERMINE THE OPTIMUM COMBINATION OF NON-IDEAL DESIGNS

When ideal designs overflow the winding space, non-ideal designs must be used. First, collect a few non-ideal versions of, if possible, primary and secondary. The accommodation procedure will then show which combinations fit into the available height. The one having the lowest loss can then be used as the final design.

Non-Ideal Design Versions in Solid Round Wire

Non-ideal design versions of wire windings are generated simply by successively reducing the number of layers to reduce winding height.

The procedure given in this Section is not valid when at the start p = 1. However, it remains valid if step 2 yields values of $p \leq 1$.

1. Note, for the coil former, b_W and ℓ_{AV} (is in m); and for the ideal design, d_{ID} (before rounding), N, l_e, p, t, d, H, r_{AC}, and P_W.

   A table such as that shown below will be found a convenient design route.

2. Reduce p by one step

   — of 0.5 for a sandwiched winding.

   — of 1 in other cases.

3. If $N\ell = N/p$ is not an integer, consider adapting N to obtain an integral number of turns per layer. If possible, let this adaptation cancel a previous one. Calculate the winding pitch.

   $t = pb_W/(N + p)$.

4. Select (from a wire table) the thickest standard wire for which $t_{MIN} \leq t$ and note d, d_O, and r_{DC}. Select a suitable interleaving, thickness i.

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5. Required height

   $H = p\ (d_O + i)$.

6. Resistance factor

   $F_R = 1 + \frac{1}{2}(d/d_{ID})^6$.

   If $p_{ID} > 1$, this expression holds for $p \leqslant 1$, but this is not the case if $p_{ID} \leqslant 1$.

7. Resistance per meter length of wire

   $r_{AC} = F_R r_{DC}$.

8. Winding loss

   $P_W = CI_e^2 N \ell_{AV} r_{AC}$.

For each design version, repeat this procedure from Step 2.

Example: In this table of design versions, the 3-layer version is the ideal design; the others are derived using the procedure above.

Primary: **Split, C = 2, b_W = 13.4mm, d_{ID} = 0.437mm, I_e = 0.565A, ℓ_{AV} = 0.053m.**			
p	3	2	1
N	57	58	57
t	0.670	0.447	0.231
d	0.450	0.355	0.180
d_O		0.414	0.222
r_{DC}		0.225	0.873
F_R		1.144	1.002
r_{AC}	0.223	0.257	0.875
P_W	0.430	0.505	1.688
i		0.06	0.06
H	1.728	0.948	0.282

Non-Ideal Design Versions of Strip or Foil Windings

Here, the required reduction in height is obtained by using thinner conductor.

1. Note, for the coil former, b_W and ℓ_{AV}, and for the ideal design, N, I_e, h_{ID} (before rounding), h, i, r_{AC}, H, and P_W. Set out a table in the form shown below.

2. For h, take the next available size below that used in the last design, and select a suitable interleaving, thickness i.

3. Resistance factor $F_R = 1 + (1/3)(h/h_{ID})^4$.

4. Resistance per meter length of conductor

   $r_{AC} = F_R/(45 b_W h)$.

5. Winding loss $P_W = CI_e^2 N \ell_{AV} r_{AC}$.

6. Required height $H = N(h + i)$.

For each successive version, repeat from Step 2 onward.

Example of a table of design versions of strip conductor:

Secondary: **Sandwiched, C = 2, N = 4, b_W = 13mm, h_{ID} = 0.222mm, I_e = 8.05A, ℓ_{AV} = 0.053m.**				
h	0.2	0.15	0.1	0.073
i	0.1	0.06	0.06	0.04
F_R		1.069	1.014	1.004
r_{AC}	0.0104	0.0122	0.0173	0.0235
P_W	0.286	0.335	0.475	0.646
H	1.20	0.84	0.64	0.452

Alternative Winding Designs With Reduced Height

It is difficult to predict the value of n_S, that is, the best starting point for the following procedure when the loss margin is positive.

— If $p_{ID} > 1$, use the procedure for Non-Ideal Design Versions, but divide t (Step 3) and r_{DC} (Step 4) by n_S.

— For a sandwiched winding, if $p_{ID} \leqslant 1$ and p = 1, use the procedure for single- and half-layer winding, again dividing t (Step 1) and r_{DC} (Step 2) by n_S.

Bunched wire: use the procedure for Ideal Multiple Wire Windings as follows:

— If $p_{ID} > 1$, commence with Step 4b and continue with values of $p > P_{ID}$.

— For a sandwiched winding, if $p_{ID} \leqslant 1$ and p = 1, use the procedure for Single-Layer and Half-Layer Bunched Wire Bindings with p = 0.5.

Litz-wire: use the appropriate procedure with lower values of p.

Having collected several versions of, preferably, all power windings, follow the procedure in the next section.

Accommodation Procedure

This procedure seeks combinations of design versions that fit into the available winding height, together with their total winding loss.

1. Calculate, for all versions of the primary, the maximum permissible secondary height, as shown in the table below.

   $H_{2MAX} = H_A - H_1$.

   Note, also, primary dissipation $P_{W\ 1}$ of all versions.

2. Select, for each primary version, the secondary that most nearly fills H_{2MAX} and note its dissipation P_{W2}.

3. Calculate the remaining free height

   $H_R = H_{2MAX} - H_2$
   and total winding loss
   $P_W = P_{W1} + P_{W2}$.

4. Select the combination having the lowest value of P_W.

Table 1 illustrates the accommodation procedure for a transformer with two power windings. The same principles apply for transformers with more power windings, even though the number of combinations is greater. Much labor might be saved if design versions with excessive loss per mm of winding height are not considered.

Since the maximum permissible winding loss is 1.23W, the 2-layer primary combined with the secondary using 0.1mm strip results in a satisfactory design. There is no need to consider the secondary using 0.15mm strip, although the excess height of 0.02mm (C = 2) could perhaps, be accommodated by careful manufacture.

NOTE:
The example is for a split/sandwiched winding configuration (C = 2), so that winding heights are for one portion of each winding.

PHASE V: FINALIZING THE DESIGN

In order to prepare the transformer design for production, four further steps are necessary.

1. Check that the design route followed was the correct one, and that no errors have crept in. Moreover, ensure that the correct value of winding-configuration factor C was used throughout.

2. Make a dimensioned sketch of a cross-section through the windings in the winding window. Calculate the conductor lengths required for each winding, using the actual average turn lengths. For wire windings, check that $N\ell$ turns of the wire selected will fit into the winding breadth, that is, that $b_W \geqslant (N\ell + 1)t_{MIN}$.

3. Prior to prototype evaluation, make a final estimate of the transformer temperature rise using winding losses recalculated from the actual winding lengths obtained in the previous step.

4. In preparation for manufacture, collect all required information about core and coil former, windings and interleavings, screens and their interleavings, interwinding insulation, and terminations. Specify winding pitches for wire windings: windings are generally not close-packed since all layers should be of equal breadth.

This concludes the practical design procedures. The following sections contain supplementary information only.

BACKGROUND

The essential difference between a designer and a computer is creative thinking. Thus, a true designer will find no lasting satisfaction in following design procedures that resemble

Table 1. Illustrating the Accommodation Procedure for H_A = 1.778mm and $P_{W\ MAX}$ = 1.23W

Primary versions (split, single wire)	p_1 $P_{W\ 1}$ (W) H_1(mm).	3 0.430 1.728	2 0.505 0.948		1 1.688 0.282
Height available for secondary	$H_{2\ MAX}$	0.050	0.830		1.496
Secondary versions (sandwiched, strip)	H_2 (mm) h (mm) $P_{W\ 2}$ (W)		0.84 0.15 0.335	0.64 0.1 0.475	1.20 0.20 0.286
Remaining height	H_R (mm)		−0.01	0.19	0.296
Total winding loss	P_W (W)		0.840	0.980	1.974

computer flow charts: he cannot help asking why the procedures are as they are, and how they can be extended to solve related problems. This section seeks to answer these and other questions with a view, too, to avoiding mistakes due to misinterpretation of the instructions. It is mainly qualitative in nature: mathematics have been reduced to a minimum, and higher-order effects, although included in the formulae behind the design aids, are generally not discussed.

EDDY-CURRENT EFFECTS IN WINDINGS

Transformer Magnetics

The main flux that couples primary and secondary windings is core-bound.

Since primary and secondary ampere turns oppose, the instantaneous value of the mutual flux is determined by the instantaneous difference between them. The magnetizing flux is proportional to the induced mmf per turn. In an ideal transformer (zero core reluctance and zero winding resistance) with a short-circuited secondary, the induced mmf and, thus, the magnetizing flux are both zero.

Flux also crosses the winding space. This flux is not common to all windings, and not even to all turns in the same winding, and is, therefore, known as leakage flux.

Figure 3a shows the leakage flux paths in a simple, ideal, short-circuited transformer (with no main flux). Within the winding space, primary and secondary leakage flux lie in the same direction. Since they mutually repel, they are in parallel with the interface between primary and secondary; that is, in parallel with the layers if the windings are on top of each other. Thus, in order not to jeopardize this parallelism, only complete layers of equal breadth will be considered.

The leakage flux-density is maximum at the interface between primary and secondary, Figure 3b. On both sides of this maximum, the flux-density falls roughly linearly to zero over the height of the winding.

Consider a flux path crossing the winding window at a distance x from the wall of the coil former. Figure 3a. Assuming that the current density over the height of the primary is constant.

$$\oint \frac{B}{\mu_O} ds = NI \frac{x}{H_1}$$

where B is the flux-density, s is the distance along the flux path, and NIx/H_1 is the number of ampere-turns enclosed. The field strength is negligible in the (high-permeability) core, and is assumed constant over the winding breadth, so that the leakage flux-density

$$B = \mu_O \times \frac{N}{b} \times I \times \frac{x}{H_1}$$

where b is the flux-path length outside core material. Figure 3b shows how B varies over the height of the wound area. There is a good case for arguing that, if b_W is smaller than the width of the winding window (perhaps due to creepage allowance), b should be taken equal to b_W. Note that leakage flux is not due to imperfect core material, but is an intrinsic property of a winding.

The leakage flux through the windings gives rise to eddy currents in the conductors.

In a transformer of normal construction, the leakage flux lies parallel to the layers of the winding and roughly normal to the turns.

Note that the leakage flux-density varies from layer to layer. In any given layer (e.g., at height x in Figure 3a) the leakage flux-density is proportional to the sum of the ampere-turns in that layer and the ampere-turns in the layers between that layer and the nearest point of zero flux-density.

The average leakage flux-density and, thus, the eddy-current losses, can be reduced by suitably mixing primary and secondary windings. One result of this process is the split/sandwiched configuration of Figure 4b.

Figure 4a again shows the leakage-flux distribution of a basic transformer winding arrangement. In Figure 4b, the primary winding is split into halves, with the secondary sandwiched between them. This halves the peak flux-density.

To make this construction possible, the split winding must have an even number of turns, and an even total number of layers. The sandwiched winding, although physically one unit, can also be regarded as consisting of two portions; its leakage flux distribution is shown in more detail so that it can be seen that it may have an odd number of layers.
Then, each portion contains a 'half' layer: a layer having half the *height* of a normal layer. Similarly, a portion of a sandwiched winding may contain a 'half' turn if the 'half' layer has an odd number of turns.

Due to the symmetry of the split/sandwiched configuration, only one portion of each winding need be considered in calculating the eddy-current effects.

The splitting-and-sandwiching process could, of course, be repeated to further reduce eddy-current loss. However, this quickly becomes unpractical: each interface between primary and secondary portions requires extra insulation, usually including screens to reduce radio frequency interference. Their presence reduces the space (copper) factor attainable in the winding window, eventually to such a degree that any improvement is either lost or not worth the extra complication.

A distinction can thus be made between

- simple windings, as in Figure 4a
- split windings, such as the primary in Figure 4b.
- sandwiched windings, such as the secondary in Figure 4b.

The design process described in this section deals exclusively with winding portions:

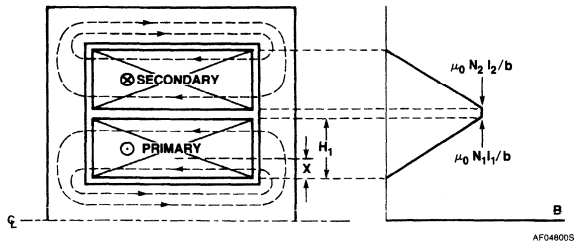
- a complete simple winding
- one half of a split winding
- one half of a sandwiched winding.

In the split/sandwiched winding configuration, the number of turns in a winding portion is half that in the complete primary or secondary.

Penetration of an Electromagnetic Wave Into a Conductor

Eddy currents are induced in a conductor exposed to an electromagnetic wave. They oppose the penetration of the wave and, in

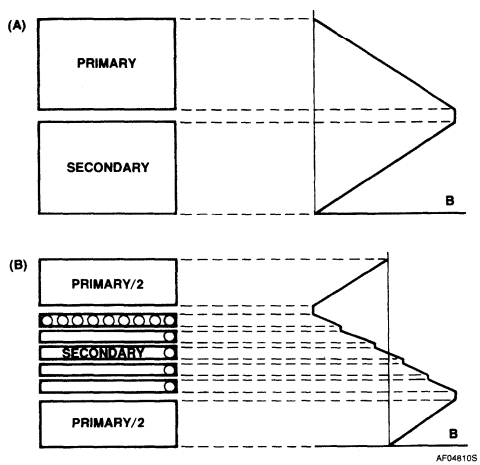
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a. Leakage Flux Paths in an Idealized, Short Circuited (to Main Flux) Transformer

b. Flux-Density Distribution

Figure 3



NOTE:
Either side of the secondary is to halve the peak leakage flux and, consequently, the eddy currents.

Figure 4. The Effect of Splitting a Transformer Primary Into Two Portions

resistive conductors, transform electromagnetic energy into heat.

Let plane x = 0 be the surface of a conductor of infinite depth. The electric and magnetic fields of a plane electromagnetic wave propagating in the nonconducting semi-space above the conductor, and incident perpendicularly upon it, are tangential to the surface and mutually perpendicular. If the positive x axis is into the conductor, the penetrating wave can be described by

$$A \exp\left\{-\frac{x}{\Delta} + j\left(\omega t - \frac{x}{\Delta} + \phi\right)\right\}$$

Constants A and ϕ (part of the incident energy is reflected from the surface) are not of interest here. The amplitude of the wave decays within the conductor as $e^{-x/\Delta}$, where Δ depends on the properties of the conductor and the frequency of the wave.

At a depth $x = \Delta$ the amplitude of the wave has decreased to 1/e of its value at the surface and the phase is delayed one radian. At a depth equal to a small multiple of Δ, there is no field in the bulk of the conductor and, consequently, no induced current.

At $x = 2\pi\Delta$, where the phase delay is just 2π radian, the field strengths decay to the negligible value $e^{-2\pi} = 0.0019$. This is at a depth of one wavelength of the penetrating wave.

Skin Effect

A straight, isolated, round wire carrying alternating current generates a concentric, circular magnetic field: both in the wire itself and in the surrounding space.

Isolated in this context means that there are neither other conductors nor magnetic fields in the vicinity of the wire. The low frequency field distribution under these circumstances is shown in Figure 5. The field is tangential to the surface of the wire.

This field induces eddy currents that oppose its penetration, enhancing the current flow near the surface and reducing it near the center of the wire as shown in Figure 6.

The net current flow remains the same, but the current density is nonuniform. This effect increases with wire diameter and frequency. The magnetic field within the wire is also redistributed.

As was the case with the penetrating electromagnetic wave, there is a tendency for current to flow only near to the surface of the wire: the skin effect.

Figure 7 shows the current distribution carrying the same alternating current at various frequencies. As frequency increases, Δ decreases and d/Δ increases.

This current redistribution results in the AC resistance of the wire being greater than its DC resistance.

The voltage is constant over any cross-section of the wire normal to its axis since there can be no radial current flow. In general, the voltage across a length of the wire is the sum of resistive and induced voltage drops. With a relatively thick wire ($c/\Delta \gg 1$), the voltage drop near the centre is mainly induced by the eddy currents, whereas, near the surface, where the current density is high, the voltage drop is mainly resistive.

If the wire is replaced by a tube of the same material and diameter, such that the tube has the same DC resistance as the wire of AC, its wall thickness will be equal to Δ, provided that the curvature of the surface is negligible ($d \gg \Delta$). For this reason, Δ is known as the (equivalent) skin thickness.

The term "penetration depth" is often used for Δ, but some authorities prefer this term for the wavelength ($2\pi\Delta$) of the penetrating wave discussed above. The (uniform) current density in the equivalent tube is equal to that at the surface of the wire it replaces. The ratio of AC resistance to DC resistance due to skin effect can be deduced from the relative cross-sectional areas of wire and tube:

$$F_R \cong \frac{d}{4\Delta}, \left(\frac{d}{\Delta} \gg 1, \text{ in practice}\right.$$

$$\left. F_R \cong \tfrac{1}{4}\left(\frac{d}{\Delta} + 1\right) \text{ if } \frac{d}{\Delta} \geqslant 5\right).$$

The AC resistance perimeter length of wire is proportional to d^{-1}, although the DC resistance is proportional to d^{-2}.

Skin thickness Δ depends on conductor material and frequency:

$$\Delta = \sqrt{\frac{\rho}{\pi \mu_O \mu_R f}}$$

The current redistribution establishes an equilibrium between inductive and resistive voltage drops. Increasing the frequency does not alter the flux-density at the surface because the current remains constant, but does cause an increase in the induced voltage which results in a smaller skin thickness and, thus, a higher current density. This, in turn results in a higher resistive voltage drop which opposes the concentration of current at the surface. A new equilibrium is achieved at a skin thickness proportional to $1/\sqrt{f}$. Similar reasoning can be established for the effect of μ_R and ρ.

The skin thickness itself is independent of the current carried by the wire. Because the wire is is immersed in its own field, there is a fixed relationship between average current density and magnetic flux-density.

Proximity Effect

A different class of eddy currents is found in wire exposed to an external alternating magnetic field normal to the axis of the wire. In that case, eddy-current flow in opposite sides of the wire is in opposite directions, figure 8.

Eddy-current flow is confined to a skin below the conductor surfaces that are tangential to the external field. No net current flow is assumed in the wire. To avoid the complications of a curved surface, a rectangular conductor is shown in Figure 8.

The situation resembles that of a turn in a winding exposed to leakage flux.

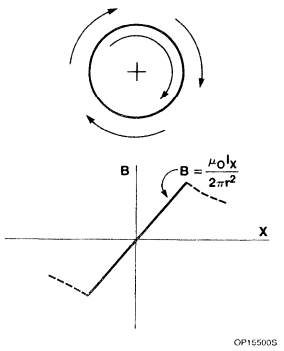
The essential difference is that the turn carries an alternating current, and that the leakage flux-density is proportional to this current. The relationship between current and leakage flux is not the same all over the winding, but depends on the position of the layer which contains the turn under consideration.

Because the leakage flux to which the turn is exposed originates from other turns in proximity to it, the eddy-current phenomenon is known as the proximity effect in this case.

Figure 9a represents a section through a few turns in a layer with the concentric magnetic flux paths associated with an isolated wire. Between the turns, however, individual flux lines, which are roughly perpendicular to the layer, oppose and so tend to cancel. The result is the flux pattern of Figure 9b. Such flux patterns from a number of layers result in the flux distribution of Figures 3 and 4. The difference between the two types of eddy-current effect is now evident.

Skin effect: tendency for the current to flow near the conductor surface, no current reversal and thus no increase in current flow. Proximity effect: there are two skin regions below the surfaces tangential to the magnetic field; besides the tendency for the main current to flow in the skin region where the magnetic field is highest, the skin regions carry opposite eddy currents that increase the effective current flow.

The leakage flux-density varies from layer to layer, but is constant over the breadth of each



NOTE:
X is the distance from the center of the conductor, and r is the conductor radius.

Figure 5. Low-Frequency Distribution of Flux Density B About a Round Current-Carrying Conductor

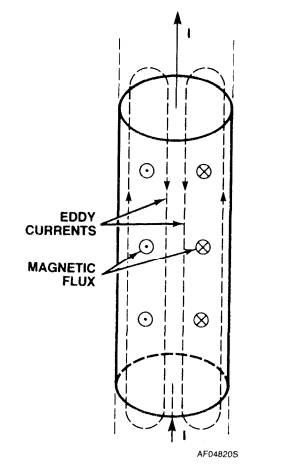


Figure 6. The Magnetic Field Generated by an AC Current in a Wire Induces Currents in the Wire that Oppose its Own Penetration

layer (Figures 3 and 4). The proximity effect is greatest in the layers at both sides of the interface between primary and secondary, where the leakage flux-density is greatest.

The simplest case is that of a strip or foil winding, where each layer has only one turn. The number of layers (and turns) is thus known at the start of the design process.

Figure 10, which is based on normalized conductor height, shows the relationship between proximity effect and leakage flux-density.

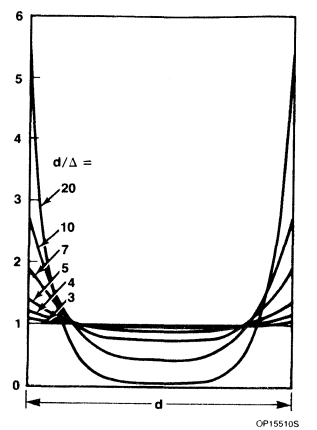


Figure 7. Current Distribution in a Wire Carrying Constant AC at Various Frequencies

The proximity effect in a wire winding depends not only on wire diameter, but also on the layer space (copper) factor.

The main geometrical parameters of a turn in a wire winding are wire diameter d and winding pitch t. Of course, $t \geq d_O$.

A useful simplification is to regard a round wire as a square wire of equal cross section and, thus, equal current density, Figure 11. Then, $h = d\sqrt{(\pi/4)} \cong 0.886d$. Extending this model allows a layer to be regarded as a strip of thickness h and layer space (copper) factor $F_\ell = h/t$ carrying a current N_ℓ times greater than that in the wire. The leakage flux is the same as that of the wire-wound layer, but the current density is $1/F_\ell$ times greater.

The equivalent conductor height $\varphi = h/\Delta$ for strip or foil windings, and $\varphi = (h/\Delta)\sqrt{F_\ell} = (d/\Delta)\sqrt{(F_\ell 4/\pi)} \cong 1.128\ (d/\Delta)\sqrt{F_\ell}$ for windings of solid round wire.

Comparison of h/Δ for strip with $(h/\Delta)\sqrt{F_\ell}$ for wire indicates that the skin depth in wire seems $1/\sqrt{F_\ell}$ times greater than in strip. This can be understood by remembering that Δ is proportional to $\sqrt{\rho}$ and that increasing ρ or increasing the current density has the same effect on the resistive voltage drop on which the equilibrium depends.

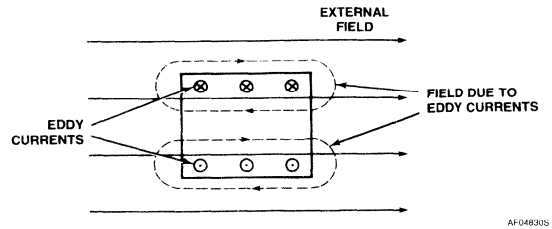
RESISTANCE

Resistance Factor F_R

The increase in conductor resistance due to proximity effects can be expressed in terms of resistance factor F_R: the ratio of AC resistance to DC resistance.

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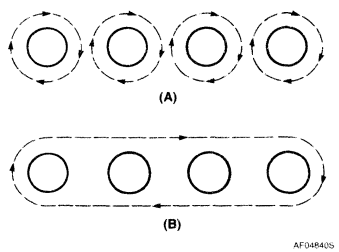
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NOTE:
A rectangular conductor is shown for clarity.

Figure 8. Eddy Currents Induced in a Conductor Exposed to an Alternating Magnetic Field Normal to its Length

The chart of Figure 12 gives F_R as a function of equivalent conductor height φ, with the number of layers p as a parameter. Inspection of these curves shows that there is a region where F_R is proportional to φ. In multi-layer windings, this region commences when φ is greater than about 3, but for single layer windings, when $\varphi \geqslant 1$. This is the region of skin conduction, where no current flows in the bulk of the conductor. The situation is similar to that for skin effect when $d/\Delta \gg 1$, where F_R is proportional to d. The curve for p = 1 (eddy-current loss negligible when $\varphi \lesssim 1$, skin conduction when $\varphi \geqslant 1$) also represents the behavior of the first layer of a multilayer winding. The curve for p = 0.5 shows similar behavior, but at double the values of φ. In all layers of a multilayer winding except the first, eddy-current loss (proportional to $F_R - 1$) increases as φ_4 up to $\varphi \cong 2$, and in proportion to φ above $\varphi \cong 3$. This is most clearly demonstrated by the curve for p = 10, but the effect is already evident in the curve for p = 1.5. Eddy-current losses in the higher layers evidently dominate the AC losses in the first layer, unless $\varphi \ll 1$.



NOTE:
The concentric flux due to the winding current (a) cancels between turns so that the resultant flux lines are parallel to the layer (b).

Figure 9. Four Turns From a Layer of a Winding

This explains the difference that will become apparent later between single and half-layer windings, and multi-layer windings.

It should be noted that eddy-current loss remains proportional to φ_4 in the lower bend of the curves, below $F_R \cong 2$. The bend is due to DC loss not being negligible compared to eddy-current loss in that region (see also Figure 2, mathematically a plot of $F_R - 1$, scale calibrated for F_R).

Figure 12 is most useful for determining the AC resistance of a winding of known geometry. However, it is not a convenient basis for optimizing winding geometry itself.

AC Resistance Per Meter Conductor Length r_{AC}

The AC resistance per meter conductor length is a useful quantity for comparing various versions of a given winding design.

Winding loss is proportional to winding resistance $R_{AC} = N\ell_{AV} r_{AC}$. In a given design problem, the number of turns and coil former dimensions are known. Conductor length $N\ell_{AV}$ is only slightly influenced by the number of layers or the conductor size. Thus, achievement of the design goal — the winding geometry for minimum loss — can be reduced to the achievement of minimum r_{AC}.

Windings of Strip or Foil Conductor

The geometry of windings of full-width strip or foil conductor is completely established once strip thickness h is known.

Strip breadth is b_W, and the number of layers is equal to the number of turns in the winding portion. These are all set by the boundary conditions, so that the only parameter remaining to be determined is thickness.

Since r_{AC} is proportional to F_R/φ, its value can be derived from Dowell's chart, Figure 12.

$$r_{AC} = r_{DC} F_R = \frac{\rho}{b_W h} F_R = \frac{\rho}{b_W \Delta} \cdot \frac{F_R}{\varphi} \quad (\text{since } \varphi = h/\Delta)$$

thus

$$r_{AC} \frac{b_W \Delta}{\rho} = \frac{F_R}{\varphi}$$

Therefore, it is sufficient to plot F_R/φ against φ as in Figure 13 There, the straight, dashed line labelled $F_R = 1$ represents r_{DC}. Since r_{DC} is proportional to φ^{-1}, its slope is – 1.

Each curve in Figure 13 has a minimum, marked by a dot. Each minimum occurs at the normalized, ideal* strip thickness h_{ID}/Δ and the lowest possible value of $r_{AC} b_W \Delta/\varphi$ from which the value of $r_{AC\ ID}$ can be calculated.

As, for given Δ, strip thickness increases beyond h_{ID}, eddy-current loss increases more quickly than DC loss decreases. Note that h_{ID} is independent of winding current because leakage flux-density is proportional to current density.

All minima in Figure 13 lie close to the straight line $F_R = 4/3$, although some deviation can be seen at low values of N.

In the practical design procedure, h_{ID} is found assuming this straight line, but a correction factor C_N has been added for the deviation that occurs when $N < 5$. Since, usually, $h \neq h_{ID}$, the approximation $F_R = 1 + (1/3)(h/h_{ID})^4$ is included in the design procedure to give the AC resistance.

Foil or strip conductor is only recommended for sandwiched windings, not for split or even simple windings.

There is no guarantee that current distribution is uniform over the breadth of a strip. In fact, there is a tendency for current density to be higher near the edges of a strip when $\Delta = \lessapprox \sqrt{(b_W h)}$, which is invariably the case. Non-uniform current density cannot occur when the leakage flux is truly parallel to the layers, so advantage should be taken of the repulsive forces between the leakage flux of primary and secondary. Sandwiching a strip winding between two portions of a wire winding, whose current density must be uniform over the layer breadth, ensures that there are strong repulsive forces on both sides of the strip winding, where leakage flux-density is maximum.

*The term "ideal" is used in preference to "optimum" since the former implies desirability but not neccesarily feasibility. A thickness other than h_{ID} may have to be used due either to conductor or space availability limitations.

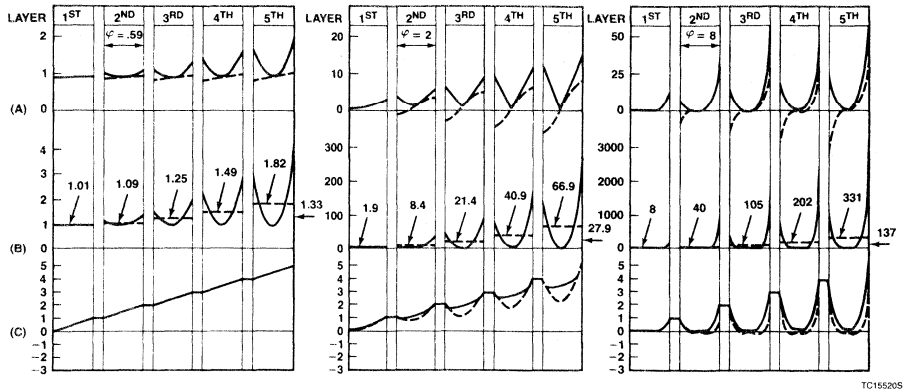


Figure 10. The Proximity Effect in a Winding of 5 Layers. Effective Conductor Heights are $\varphi = 0.59$ (Left), $\varphi = 2$ (Center) and $\varphi = 8$ (Right). Sections Through the Ends of the Layers of the Winding are Shown, Hatched. The Layers are of Strip Conductor, but Could Also be N_ℓ Turns of Rectangular Wire. The Current Density Distribution is Plotted in (a). The Full Line is the Amplitude, the Broken Line the Real Part, and the Dotted Line the Imaginary Part. The Losses are Plotted in (b). The Loss Distribution (Solid Line) is Proportional to the Square of the Current Density Amplitude. The Broken Line Shows the Average Loss in Each Layer, and the Dotted Line the Average Loss in the Complete Winding. Since the Scale Calibration is Multiples of the DC Loss, the Dotted Line Shows the Value of F_R. (c) is the Leakage Flux Diagram, Obtained by Integration of the Current Density. Scale Divisions are Layer Current; Line Types are as in (a)

Wire Windings: Winding Breadth-To-Turns Ratio T

The AC resistance per meter length of wire r_{AC} can be derived from a plot of F_R/φ_2 against φ, Figure 14.

For rectangular wire of breadth b (in the layer) and height h (normal to the layer)

$$\varphi = \frac{h}{\Delta}\sqrt{\frac{b}{t}}$$

and

$$F_R/\varphi^2 = \frac{r_{AC}\Delta^2 t}{r_{DC}h^2 b} = r_{AC}\frac{\Delta^2 t}{\rho h}$$

For round wire of diameter d

$$\varphi = \frac{h}{\Delta}\sqrt{\frac{h}{t}} = \left(\frac{\pi}{4}\right)^{3/4} \times \frac{d}{\Delta}\sqrt{\frac{d}{t}}$$

$$= \frac{1}{\Delta}\left(\frac{d}{t}\sqrt{\frac{\pi}{4}}\right)^{3/2}$$

so that, for a given ratio t/d,

$$F_R/\varphi^2 = r_{AC}\frac{\Delta^2 t}{\rho h} = r_{AC}\frac{\Delta^2 t}{\rho d}\sqrt{\frac{4}{\pi}}$$

is proportional to r_{AC}.

Here, $r_{DC} \propto \varphi^{-2}$ so that the line $F_R = 1$ has a slope of −2. Whereas Figure 13 gave the solution of the design of a strip winding, where the number of layers and conductor breadth were known, the plot of Figure 14 does not contain the solution for wire windings. The number of layers is still not known.

The winding breadth is introduced in the form of the winding breadth-to-turns ratio $T = b_W/N$.

Physically, T is the winding pitch in a single-layer winding containing all N turns. Note that at the interface between primary and secondary, the leakage flux-density $B = \mu_0 I/T$ and also that T is known at the start of the design process.

Since $t = pT$, for a rectangular wire

$$\varphi = \frac{h}{\Delta}\sqrt{\frac{b}{pT}}$$

and for round wire

$$\varphi = \left(\frac{\pi}{4}\right)^{3/4} \times \frac{d}{\Delta}\sqrt{\frac{d}{pT}}$$

Close-Packed Windings of Round Wire

For close-packed windings, $r_{AC}\Delta^2/\rho$ can be plotted against T/Δ, Figure 15; this gives better access to the design problem.

In close-packed wire windings $t = d_O$, so the layer space (copper) factor depends on the ratio d/d_O for the wire. This ratio is not constant: standard-wire tables show that d/d_O is smallest for fine wire, but the rate of change is rather low. If Figure 14 were replotted to give $r_{AC}\Delta_2/\rho$ against t, the calibration of the axes would, of course, change, but the shape of the curves would hardly be affected because the rate of change of d/t is so low. In order to replace t by T, the values for each of the curves must be divided by p, since $T = t/p$. This shifts every curve horizontally a distance — log p.

The introduction of T is an important step forward: knowing T/Δ, it is possible to read the lowest possible value of $r_{AC}\Delta^2/\rho$, the optimum number of layers, and, finally, from $d_O = t = pT$, the optimum wire size can be determined.

In order to plot Figure 15, values of d/d_O and its variation with wire size were estimated. So, although the plot of Figure 15 is adequate for illustrating the theory, its accuracy is not sufficient for practical design purposes.

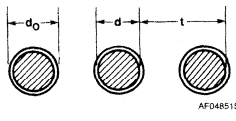
Spaced Windings of Round Wire

Windings are also possible with a pitch greater than the overall wire diameter: spaced windings. This introduces an additional degree of freedom that can be exploited to achieve a further reduction in AC resistance. This is illustrated by the plot of Figure 16.

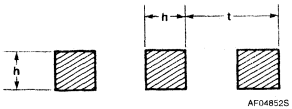
The solid curves in Figure 16 are for close-packed windings ($t = d_O$), as in Figure 15. The dash-dot curves are for windings of two layers, in which $t > d_O$. These show that there is a range of T/Δ where spacing results in lower values of r_{AC}. However, spacing should not be excessive: better performance is always possible if a smaller number of layers can be used.

The straight dashed lines in Figure 16 are a further addition: they show that spacing displaces the curves so that similar points lie on a line of slope $-\frac{2}{3}$. They also show that the curves for $p \leqslant 1$ are so steep that spacing brings no improvement.

In effect, spacing allows designs intermediate between close-packed versions.

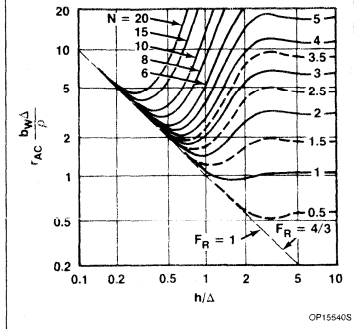


a. Principal Geometrical Parameters Describing a Turn in a Given Layer



b. Replacing a Round Wire With a Square One of Equal Cross Sectional Area Simplifies the Discussion Since Now a Layer Resembles a Turn of Strip Conductor

Figure 11



NOTE:
This virtually solves the design problem for strip windings. Given the number of turns N, the minimum in the appropriate curves gives the ideal (lowest loss) strip thickness as a multiple of the skin thickness. The resistance per meter length of strip can also be determined.

Figure 13. Plot of F_R/φ vs φ

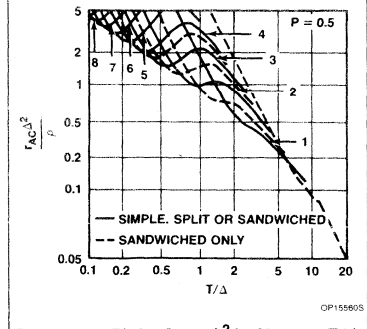


Figure 15. Plot of $r_{AC}\Delta^2/\rho$ Versus T/Δ With P as a Parameter for Close-Packed Wire Windings

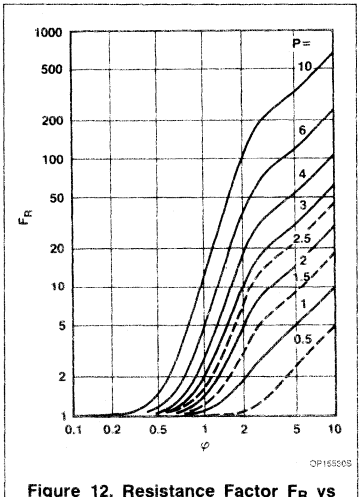


Figure 12. Resistance Factor F_R vs Equivalent Conductor Height φ, With Number of Layers p as a Parameter

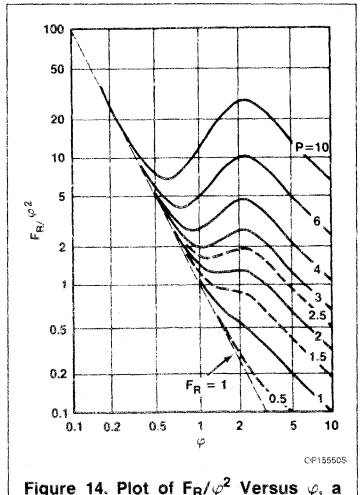


Figure 14. Plot of F_R/φ^2 Versus φ, a First Step Towards the Solution of the Design Problem for Wire Winding

The Basic Solution of the Design Problem

Sufficient information is now available to make a plot that effectively solves the design problem. This is given as Figure 17.

Figure 17a differs from Figure 14 in that spaced windings are included where they give lower loss. Furthermore, those parts of the curves for close-packed windings that are not useful for design purposes have been suppressed.

The full lines apply to optimum designs with an integral number of layers. The broken lines apply to optimum designs with a half layer (except in the plot of winding height, these often coincide with the full-line curves). The dotted lines are for non-optimum, close-packed windings.

There it can be seen that, if T/Δ is known, the optimum design is completely determined. Further inspection reveals that:

- for T/Δ greater than about 2, the optimum design is a single-layer winding but, in sandwiched designs, when T/Δ is greater than about 6, the optimum is a half-layer winding
- for T/Δ less than about 2, the optimum design has more than one layer.

Both the full and the broken lines for $p > 1$ show that the resistance minima occur generally for spaced windings so that it is important to include in the manufacturing instructions a specific statement that windings should not be close packed. The curves for $p \leq 1$ have a slope of about −1, indicating that $F_R \propto \varphi^{-1}$, so that they belong to the region of skin conduction. Moreover, they are, in principle, close-packed windings. It is clear that multilayer ($p > 1$) windings and those with $p \leq 1$ will require different design methods.

Multilayer Windings ($p > 1$)

The full lines in the chart for $r_{AC}\Delta^2/\rho$ and d/Δ, Figure 17, consist of several sections,

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each for a particular value of p. Together, for $p > 1$, they form nearly straight lines.

The ideal values of d and r_{AC} are, thus, generally independent of p. There is only a slight deviation for the lower values of p: it can be seen that the lines for $p = 1.5$ do not coincide with those for $p = 2$.

The resistance factor for optimum or ideal designs $F_{R\ ID} \cong 1.5$, which means that the eddy current loss is half the frequency-independent resistive loss, also called DC loss.

The slope of the straight lines indicates that $r_{AC\ ID} \propto (T/\Delta)^{-2/3}$ and $d_{ID} \propto (T/\Delta)^{1/3}$. Since $r_{DC} \propto d^{-2}$, $F_R = r_{AC}/r_{DC}$ must be constant.

If the actual wire diameter d deviates from the ideal diameter d_{ID}, the estimated resistance factor becomes

$$F_R = 1 + \tfrac{1}{2}\left(\frac{d}{d_{ID}}\right)^6$$

This approximation, derived from the first two terms of the series expansion of Dowell's expression, is sufficiently accurate for values of $F_R \leq 2$. In an ideal winding, where $d = d_{ID}$, $F_R = 1.5$. The expression is not valid in the region of skin conduction.

To find the ideal wire diameter for windings having a large number of layers, the expression $d_\infty/\Delta = 1.45\ (T/\Delta)^{1/3}$ can be used. In a more practical form this expression reads

$$d_\infty = \left(\frac{17.1bw}{Nf_e}\right)^{1/3} \quad \text{where } f_e \text{ is in kHz.}$$

The ideal wire diameter for a practical winding, d_{ID}, is then obtained using the correction factor C_p.

This factor corrects for the effect of the small steps between the line sections for practical numbers of layers.

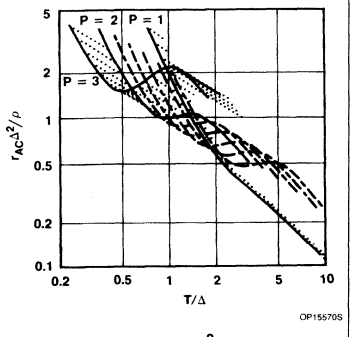
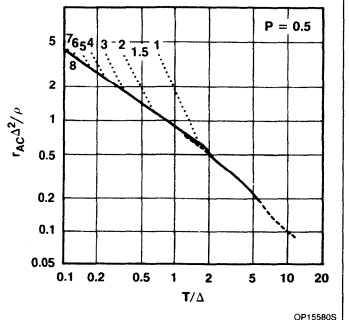
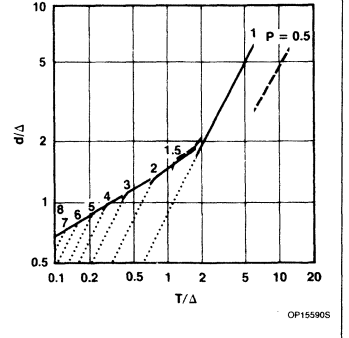


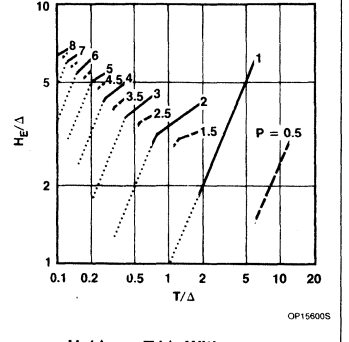
Figure 16. Plot of $r_{AC}\Delta^2/\rho$ vs T/Δ Extended for Spaced Windings



a. $r_{AC}\Delta_2/\rho$



b. d/Δ



c. H_e/Δ vs T/Δ With ρ as a Parameter

NOTE:
H_e is the required height excluding interleaving. Knowing T/Δ, the ideal winding geometry and the resistance per meter length of wire can be determined.

Figure 17. Basic Design Charts for Wire Windings

Using these expressions, ideal designs can be obtained by simple calculation.

Once knowing d_{ID} the winding geometry can be determined. After rounding d_{ID} to the nearest standard wire size, d_O is known. Following the design rules in the practical sections, the number of layers and the required height are easily found. Knowing r_{DC} of the selected wire, r_{AC} can be estimated after calculation of F_R.

Single-Layer and Half-Layer Windings

This is the region where the procedures of the previous section lead to a number of layers $p \leq 1$.

This definition is given because the criterion $T/\Delta > 2$ is only an indication.

First it is necessary to decide between strip and wire windings.

Strip or foil windings are often preferable.

For simple and split designs, it is known that $p = 1$. This is also the case in sandwiched designs if T/Δ is below about 6. Since windings should be close packed, geometry is fixed.

The end of the curve for $p = 1$ at $T/\Delta = 6$ is not a theoretical limit; the curve can be extended. But d may be so great that a different form of conductor will probably be chosen.

For sandwiched windings, a half-layer winding may be preferable, provided T/Δ is greater than about 6.

That saves winding height without a loss penalty. In case of doubt ($T/\Delta \cong 6$), a choice can be made after having worked out both alternatives.

The remaining problem is the estimation of r_{AC}. To solve that, calculate

$$\varphi = \left(\frac{\pi}{4}\right)^{3/4} \times \frac{d}{\Delta}\sqrt{\frac{d}{pT}}$$

or, alternatively,

$$\varphi = \sqrt{(0.124 f_e d^3/t)}$$

and read F_R from the plot of F_R versus φ, Figure 2.

Figure 2 gives the F_R plot in a more suitable form than Figure 12. Do not use the expression for F_R given in the previous section: it is not valid in the region of skin conduction.

High-Frequency Ferrite Power Transformer and Choke Design

Winding Height

Ideal Designs

In previous sections, methods were developed for designing minimum-loss windings of both strip and wire conductors. In developing these methods, possible height restrictions have so far been ignored.

By doing this, each winding could be treated separately, the design of a primary was not influenced by the secondary, and vice versa.

Such designs, not affected by a height restriction, are called ideal designs.

Similarly, terms such as ideal windings, ideal number of layers, ideal conductor size, etc., are also used.

It is, of course, necessary to check whether the situation is ideal: that the height of the winding window does not impose a height restriction on the windings.

The height of a winding (portion) is calculated from:
for strip windings, $H = N\ (h + i)$
for wire windings, $H = p\ (d_O + i)$.
For the available winding height (the height available for all power-transferring windings), see the section on "Given Boundary Conditions".

Non-Ideal Design Versions

In strip windings the only way to reduce winding height is to use thinner strip.

Various non-ideal design versions are found by repeatedly stepping to a smaller available strip thickness. The AC resistance is found from the expression for F_R.

In wire windings, a smaller winding height is obtained by reducing p. This leads to reduced pitch ($t = pT$) and thus, also, to reduced wire size ($d_O \leqslant t$), so that $d < d_{ID}$. To reduce the difference between d and d_{ID} as far as possible, a non-ideal wire winding should be close-packed using the thickest possible wire for the number of layers and winding breadth. The AC resistance can be estimated by means of the expression for F_R.

Several non-ideal design versions are found by repeatedly stepping to a lower number of layers.

Thus, non-ideal as well as ideal design versions can be found. Although these non-ideal design versions have smaller winding height than the ideal design, they also have higher loss.

IMPORTANT

There is no justification for using conductor sizes in excess of the ideal size (apart from rounding a calculated ideal size to the available size). Reduction of current density is a false motive. The extra conductor material has only an adverse effect.

Accommodation

Once a few design versions (the ideal design and one or more non-ideal versions) of the primary and secondary have been collected, selection of the most suitable combination is made by an accommodation procedure.

The accommodation procedure is given in detail and comprises the following basic steps:

- List the design versions obtained, the height they require and their losses
- Make combinations of primary and secondary designs having a total height not exceeding the available height, and note the winding loss of each
- Finally, select the lowest-loss combination.

Demagnetizing and control windings are usually designed for minimum height rather than minimum loss, since they do not take part in power transfer. Their height is taken into account in determining the height available for the power windings.

Design Evaluation

A design attempt is successful if the transformer does not run hot.

Final evaluation is, of course, experimental. Unnecessary experimentation can, however, be avoided if the estimated losses are first compared with the estimated permissible loss.

The permissible loss is estimated from the permissible temperature rise and the thermal resistance given in the data for the core selected*. Core loss was estimated in the process of core selection and determination of the number of primary and secondary turns.

Current densities much higher than are usual in low-frequency transformers may well be acceptable. As has been mentioned, conductors in excess of the ideal size make matters even worse.

If a design attempt fails, it is advisable to first review the chosen boundary conditions. This would not invalidate the results of the core selection procedure.

An improvement may be obtained by using split/sandwiched rather than simple windings. These tend to lower r_{AC}, thicker conductors and increased height. A different conductor form might also be considered.

A new start, including the core selection procedure, is required if the given boundary conditions have to be altered.

It may be possible to use same core size if switching frequency is increased. This leads to fewer turns, of thicker conductors and, thus, lower winding loss.

To avoid fruitless effort, the practical design process is so organized that an initial design evaluation is made as soon as suitable ideal designs and their losses have been determined.

Winding height can be reduced with the penalty of increased loss and vice versa (by using bunched wire, for example) but this will not help if the ideal design has neither loss nor height reserve.

Some Notes

Multiple-Output Transformers

Figure 18 shows a possible winding arrangement and leakage flux density distribution for a multiple output transformer.

In both primary and secondary 2, the flux-density varies from zero to a maximum, so these can be designed using the present methods. That is not possible for secondary 1 because its leakage flux distribution does not agree with the assumptions. The ratio of leakage flux-density to number of turns is much higher than has been assumed so far.

The ideal wire diameter for an infinite number of layers d_∞ in the winding exposed to the higher leakage flux is calculated as normal, but the layer correction factor becomes

$$C_p = \sqrt{\frac{1-\vartheta}{(1-\vartheta^3)^{1/3}}}$$

where ϑ is the ratio of minimum to maximum leakage field over the height of the winding.

In secondary 1 of Figure 18, $\vartheta = (N_{SEC\ 2}\ I_{SEC\ 2})/(N_{PRIM} I_{PRIM})$. The factor C_p is always less than unity and decreases with increasing ϑ. The higher leakage field is compensated for by using thinner wire. As is usual ($\vartheta = 0$) for wire windings, $F_{R\ ID} \cong 1.5$: the formula for F_R still applies.

Similarly, for strip conductor,

$$C_N = \left\{ \frac{(1-\vartheta^3)^{1/4}}{1-\vartheta^3} \right\}$$

As normal ($\vartheta = 0$) for strip windings, $F_{R\ ID} \cong 4/3$.

To obtain lowest total winding loss, the layout of the secondary windings (2 or more) in the winding window must be considered carefully.

*The thermal resistances in the published data can be reduced by potting the transformers. If this is to be done, it might be possible to eliminate the creepage distance, so increasing winding breadth. The loss in each winding can be estimated as $P_W = I^2 N l_{AV} r_{AC}$

High-Frequency Ferrite Power Transformer and Choke Design

AN1261 Part 3

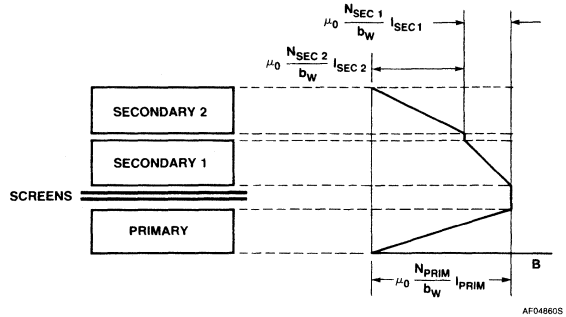


Figure 18. An Example of a Multiple-Output Transformer With Corresponding Leakage Flux Diagram

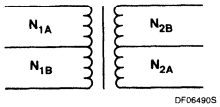


Figure 19. Push-Pull Transformer Windings Divided to Define Conduction Periods

- Secondaries of the same conductor type, either wire or strip: exposing the winding carrying the smallest current, that is, the one using the thinnest conductor, to the highest leakage field will result in lowest loss. Remember that the eddy current loss increases in proportion to φ^4.
- Secondaries of different conductor type (wire or strip): the optimum arrangement is not easy to predict. Work out the possible layouts and select for lowest total loss.

Push-Pull Transformers

In push-pull transformers, Figure 19, not all windings carry current at the same time.

The operation of a push-pull converter is explained in Part 1 of this series of publications. Here it is sufficient to split up one converter operating period into

- Interval a: N_{1A} and N_{2A} are conducting, other windings carry no current. During this interval the current waveforms in N_{1A} and N_{2A} are the same.
- Interval b: N_{1B} and N_{2B} are conducting.
- Interval c, occurring twice per period: N_{1A} and N_{1B} are nonconducting, N_{2A} and N_{2B} carry equal and opposite flywheel currents about half as great as the secondary currents during intervals a and b (magnetizing current neglected). The closer intervals a and b approach a half period (at full load) the shorter this interval will be. Whether or not the flywheel current pulses have an influence on winding design depends on the winding arrangement.

Bifilar windings are often used to achieve close coupling between winding halves.

Figure 20 shows a cross-section through the windings and the leakage flux diagrams during the three intervals.

If wire windings are used the flywheel currents during interval c cancel (higher order effects neglected). That is not quite so if 'bifilar' strip windings are used (two full-breadth strips and interleavings wound simultaneously). The peak flux-density is then about $1/(2N_2)$ times that during intervals a or b. Since the eddy-current loss is proportional to the square of frequency and flux-density, the eddy-current loss in interval c may be negligible if the half-secondaries have at least a few turns. It might not be possible to ignore the contribution of the flywheel currents to the DC loss unless interval c is very short.

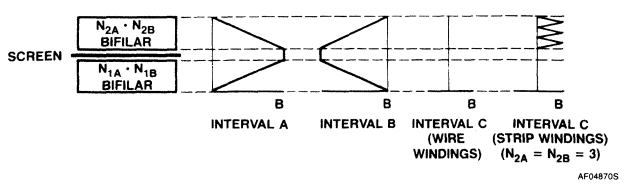


Figure 20. Cross-Section Through the Windings of a Bifilar-Wound Push-Pull Transformer Together With the Leakage Flux Diagrams for the Conduction Intervals Described in the Text

During intervals a and b, eddy currents are generated in both the conducting and the non-conducting windings.

Both windings of a pair are exposed to the same leakage flux and have about equal eddy-current loss. Only one of these has DC loss at a time.

For minimum loss (ideal designs), the ratio of eddy-current loss to DC loss remains one half for wire windings and one third for strip windings. That requires thinner conductors than in non-bifilar windings having equal numbers of turns, and winding pitch or strip breadth.

For multilayer wire windings, the reduction is $2^{-1/6} = 0.89$ (one step in the wire table), and for strip windings, $2^{-1/4} = 0.84$.

The reader can adapt the design procedures to cope with bifilar windings, as noted in the section "Phase II: Determine the Ideal Power Windings."

Multilayer wire windings:
- in step 1 multiply d_∞ by 0.89
- in step 4 use $2t_{MIN}$ in the expression for p_{ID}
- in step 9 calculate the loss in a winding pair.

Single-layer wire windings:
- in step 2, use $2t_{MIN}$ rather than t_{MIN}
- in step 6, calculate $r_{AC} = (2F_R - 1)r_{DC}$
- in step 7, estimate the loss of a winding pair.

Strip or foil windings:
- in step 1, multiply C_N by 0.84
- in step 5, estimate the loss of a winding pair.

Bifilar windings are not possible if the wire insulation cannot safely withstand at least twice the peak voltage across a winding half.

The transformer of Figure 21 differs from the previous one in that the primary winding halves do not share the same space.

The leakage flux diagrams show an asymmetry. During interval a winding N_{1B}, although not conducting, is subjected to a high leakage flux and has about three times the eddy current loss of the conducting winding N_{1A}, because the average of the RMS flux-density squared in N_{1A} is one third of that in N_{1B}. In interval b, however, N_{1A} has no eddy-current loss. The primary winding halves thus have different AC resistance due to a difference in eddy-current loss by a factor of four. Moreover, the leakage inductance is greater in N_{1A}. The energy stored in the leakage field can be expressed as $\frac{1}{2}LI^2$ or as $\frac{1}{2}VB^2/\mu_0$, where L is the leakage inductance and V the field volume (here proportional to the area of the flux diagram times the average turn length).

By arranging the windings as in Figure 22, only a minor asymmetry due to different turn lengths remains and eddy-current loss in the non-conducting primary is eliminated. In this arrangement the coupling between the primary winding halves will be less close and the stray capacitance across the secondaries, now situated between two screens, will be increased.

High-Frequency Ferrite Power Transformer and Choke Design

In Figure 23, the secondaries are also divided: non-conducting windings are not exposed to leakage flux. Now eddy-current loss during interval c occurs in the secondaries.

This indicates the effect of different current waveforms in primaries and secondaries, which means that their effective frequencies are different.

For split/sandwiched configurations, similar considerations apply as indicated above for simple configurations.

Here, also, leakage flux diagrams will be of great help in the analysis. The discussion in this Section clearly illustrates the general risk of overlooking important parameters in striving for an optimum in a particular respect.

Flyback Transformers

In a flyback transformer, current conduction in primary and secondary occurs alternately. When the primary conducts, there is no current in the secondary, and vice versa. Two different leakage flux-density diagrams are thus required, as in Figure 24.

The flux diagrams shown do not pretend to be accurate. In drawing the full-line portions, tight coupling to the core and a leakage flux parallel to the layers were assumed. However, since the repulsion between primary and secondary flux does not exist, the latter assumption is an idealization. The broken lines are speculative.
It is therefore recommended that the outer winding has the thinner wire.

The leakage flux generated by the current in the inner winding also induces eddy currents in the outer winding.

As a practical guide, it is recommended that the outer winding be wound with a wire one size smaller than that calculated using the procedures given in this article. The estimated winding loss will then probably prove slightly optimistic.

Although the present design methods are not as accurate for flyback transformers as they are for forward and push-pull types, their use is helpful in preventing excessive eddy-current loss.

Strip or foil windings: Since the leakage flux might not be truly parallel to the layers, we should not be surprised if the losses are higher than calculated. The current density near the edges of the conductor might be considerably higher than near the middle of the breadth. That effect is nearly independent of the conductor thickness. The use of multiple-wire, bunched or Litz-wire might be a better solution for low-voltage windings.

Screens

Eddy-current losses will also occur in the screens between primary and secondary.

Screens are always situated in positions of maximum flux-density.

Screens should not be thicker than necessary; there should be the minimum of overlap of the ends. Copper is not the most suitable material: a (non-magnetic) conductor of higher resistivity is preferable.

Eddy-current loss is directly proportional to conductivity, and proportional to the thickness cubed. Thus, screens should be as thin as possible (UL-1244 specifies a minimum of 0.15mm).

Although its low resistivity makes copper the natural choice for the winding conductor, it is not the first choice for screens. Phosphor bronze CuSn8 has a resistivity 10.9% of that of copper at 20°C and 13.8% at 100°C. The use of such a material reduces losses in proportion.

Additional loss can be caused by the capacitance of the overlap at the ends of the screen, which causes the screen to act as a shorted turn. This overlap should be as small as possible.

CHOSEN BOUNDARY CONDITIONS

Once the given boundary conditions have been established from the choice of core and numbers of primary and secondary turns, the designer can choose winding configuration and conductor type.

Winding Configuration

The designer can choose between:

- Simple windings
- Split/sandwiched windings

The lower losses of split/sandwiched windings arising from the halved peak leakage flux-density will be evaluated further, as will also the required winding height.

In the split/sandwiched configuration, a winding portion has half the number of turns of the complete primary or secondary winding. Hence the value of $T = b_W/N$ is doubled.

Strip or Foil Windings

The use of strip or foil windings is only recommended for sandwiched windings. The following discussion is given for completeness, because the route of a design process cannot always be predicted.

Analysis of the design formula shows that for moderate values of N (where $C_N \cong 1$), halving N increases h_{id} by a factor of about $\sqrt{2}$. Since the total number of turns in the complete winding remains the same, sandwiching increases the height of the ideal winding by 41%.

The influence of the interleaving is neglected. Besides the increase in required height, the extra winding interface with its insulation and screening reduces the available height.

In the extreme case, where N changes from 1 to 0.5, h_{ID} doubles because C_N also increases by a factor of $\sqrt{2}$.

$F_{R\ ID}$ was shown to be about constant for all values of N. So the ideal winding resistance tends to decrease as $1/\sqrt{2}$, a reduction of 29%.

For N = 0.5, $r_{AC\ ID}$ is half that for N = 1.

A smaller improvement can be obtained where the sandwiched version must be non-ideal.

Even if the simple version has to be non-ideal it may occur that its sandwiched counterpart has a lower AC resistance.

Wire Windings

If, for a simple wire winding having at least 2 layers, the ideal design is replaced by an, also ideal, split or sandwiched winding r_{AC} will be improved by about 37%. The penalty is a considerable increase in required height.

The actual increase in height is not readily predictable, since the number of layers may change (the effect of doubling T/Δ is shown in Figure 17). In many cases the split or sandwiched version will be non-ideal, so that the improvement in resistance is smaller than 37%. The improvement of a (non-ideal) split or sandwiched winding replacing a non-ideal simple winding also varies from case to case.

The replacement of an ideal, simple, single-layer winding by an ideal, split or sandwiched winding must be considered separately. Doubling T/Δ (Figure 17) results in halving $r_{AC\ ID}$. If the result is two single-layer portions, wire diameter will be doubled, and required height quadrupled. But, if the result is two half-layer portions, wire diameter and winding height remain the same.

This will not often occur in practice, because strip or foil windings are generally preferable to single-layer windings.

Conductor Form

The designer can choose between solid round wire, strip or foil conductor, multiple-wire, bunched-wire and Litz-wire.

Strip or Foil Versus Solid Round Wire

Strip or foil is only recommended for sandwiched windings. There will seldom be more than 10 turns in a winding portion.

Usually, the total winding may have up to 20 turns with as many interleavings in the (radial) heat-flow path. Depending on current density, internal overheating may occur if the number of turns and interleavings is unduly high.

Strip or foil windings can be considered if $T/\Delta \geqslant 2$, as an alternative for single-layer or half-layer wire windings, for example. If

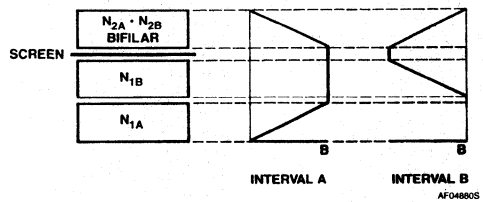


Figure 21. Cross-Section Through the Windings of a Push-Pull Transformer With a Bifilar Secondary, Together With the Leakage Flux Diagrams for Two Conduction Intervals. Note the Asymmetry

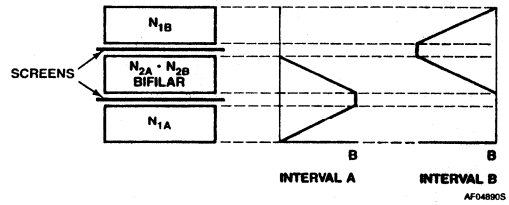


Figure 22. Rearrangement of the Windings of Figure 21 Showing the Reduced Asymmetry

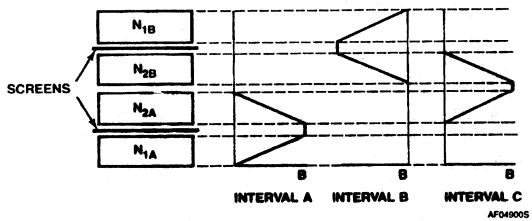


Figure 23. Cross-Section Through the Windings of a Push-Pull Transformer Showing That, With Divided Primary and Secondary Windings, the Non-Conducting Windings are not Exposed to Leakage Flux

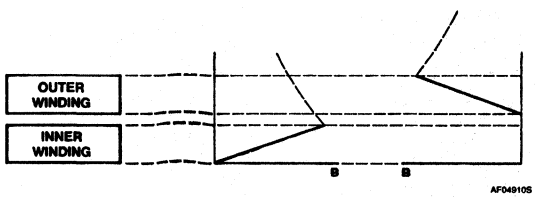


Figure 24. In a Flyback Converter Transformer, Primary and Secondary Conduct Alternately. Thus, Two Leakage Flux Diagrams are Required for Loss Analysis: One for the Inner Winding Conducting (Left) and One for the Outer Winding Conducting (Right)

the winding has only a few turns, they are a must.

In practical transformers, b_W/Δ may be assumed to be > 20. With $N \leqslant 10$, then $T/\Delta \geqslant 2$. The basic design chart for wire windings, Figure 17, shows that that is the region for single-layer or half-layer designs, for which $r_{AC\ ID}\ \Delta^2/\rho \cong 1.1(T/\Delta)^{-1}$

Choosing strip rather than wire reduces the winding resistance by a factor of about 0.9 $\sqrt{N}$ if ideal designs can be used.

If N > 1, the expression for the ideal strip thickness can be written as $h_{ID}/\Delta \cong 3^{1/4}N^{-1/2}$. Then, $r_{AC\ ID} = F_{R\ ID}\rho/(b_W h_{ID}) \cong (F_{R\ ID}/1.32)$ $\rho N^{1/2}(b_W\Delta)^{-1}$. Since $F_{R\ ID} \cong 1.33$, dividing this result by that for wire windings obtained above yields the factor $0.9/\sqrt{N}$.

With a non-ideal strip design, the improvement over an ideal solid-wire version is, of course, smaller, but the strip version remains preferable as long as the thickness of all turns in the portion together exceeds Δ.

For a non-ideal strip version in which $F_R \cong 1$ (that is, if $h \leqslant 0.5\ h_{ID}$), $r_{AC} \cong r_{DC} = \rho/(b_W h)$. To make this smaller than the $r_{AC\ ID}$ of the wire version, $Nh > \Delta/1.1$ or, as a rule of thumb, $Nh > \Delta$.

Multiple Wire

In a multiple-wire winding, each turn consists of n_S strands lying side-by-side in the layer, Figure 25.

Multiple-wire turns have the height of a single strand, but an area n_S times that of a strand, and a layer space (copper) factor the same as that in a layer wound conventionally with wire of the size of each strand.

The design procedure for solid round wire windings can easily be adapted for multiple-wire.

In the basic design chart of Figure 17, after dividing T/Δ by n_S, read d_{ID}/Δ, p_{ID} and $H_{E\ ID}/\Delta$ as usual. The value of $r_{AC\ ID}\Delta^2/\rho$ for the single strand must be divided by n_S to find the resistance of the multiple wire.

In effect, a single-wire winding is designed with a layer breadth b_W/n_S, or alternatively, the winding geometry is determined as if there were $n_S N$ turns. T/Δ and r_{AC} are thus $1/n_S$ times those for a normal wire winding.

Compared with normal, single-strand, multilayer windings (more than one layer per portion, $T/\Delta < 2$), $r_{AC\ ID}$ and d_{ID} decrease



NOTE:
The strands of one turn are indicated by black dots.

Figure 25. A Multiple-Wire Winding of 4 Turns, Each of 3 Strands

about as $n_S^{1/3}$ and H_e increase about as $n_S^{1/3}$.

With 2 parallel strands, Figure 26, the reduction in $r_{AC\ ID}$ and d_{ID} is about 20%: the height increase is roughly 25%. With 3 parallel strands, the reduction in $r_{AC\ ID}$ and d_{ID} is about 30%: the height increase is roughly 45%.

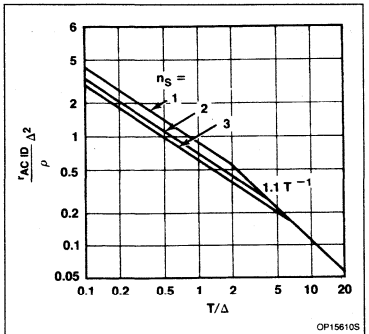
If the increased height does not permit the use of the ideal design of a multiple-wire version, the single-strand winding will often have a lower resistance. More than 3 parallel strands are not often used due to winding difficulty, or inadequate height.

In the region of $T/\Delta > 2$ it is usual to try to use strip or foil conductor. If that is not possible, multiple-wire may be considered.

Strip conductor, although promising lower resistance, cannot always be used because of uneven current distribution over the layer breadth, for example, or due to constructional problems.

If $T/\Delta > 2n_S$ lower resistance cannot be achieved, (Figure 26), but a multiple-wire winding design might be justified by reduced winding height, the use of thinner, more flexible wire, and saving in copper.

The curve for $p = 1$ in Figure 17 ends at $T/\Delta = 6$ only for practical reasons. There is no theoretical limit: the resistance remains inversely proportional to T/Δ. If $p = 1$ and $T/\Delta > 2n_S$, or if $p = 0.5$ and $T/\Delta > 6n_S$ the overall wire diameter and, thus, the winding height, will be found to reduce in inverse proportion to n_S. In order to understand how less copper can have equal resistance, it is necessary to realize that this is in the region of pure skin conduction ($\varphi \gg 1$). The breadth of a turn (either a single wire or n_S strands) and, thus the skin area remains the same. Stranding reduces the amount of useless conductor in the winding.



NOTE:
The improvement quickly vanishes between $T/\Delta = 2$ and $T/\Delta = 2n_S$. But if T/Δ exceeds $2n_s$, winding height and copper content are reduced by the use of thinner wire.

Figure 26. Design Chart for Multiple-Wire Windings Showing the Improvement in $r_{AC\ ID}$ Obtainable for n_s = 1, 2, and 3 Strands

Bunched-Wire

Bunched-wire comprises three or more enamelled wires, twisted around each other to form a bunch.

Here, a distinction is made between bunched-wire and Litz-wire, which latter is discussed in the next section. The difference is in the strand diameter: in bunched-wire it is of the order of magnitude of Δ, whereas in Litz-wire the strands are much finer. In the literature, the term bunched-wire is sometimes used for what is here called Litz-wire

In both bunched- and Litz-wire the strands undulate within the height of the layer. This ensures equal current sharing between the strands, because, on average, the position of each strand is in the middle of the layer height. Bunched-wire windings are designed in much the same way as single-wire windings having Nn_S turns, but adaptations of the procedures are required for the determination of winding pitch and layer height.

Litz-Wire

Litz-wire is a form of bunched-wire in which the strand diameter is small compared to Δ. Eddy-current effects are thus virtually eliminated, and the AC resistance is equal to the DC resistance.

Thus Litz-wire windings require no special design procedures: the design methods for low-frequency windings apply.

Litz-wire is standardized and commercially available.

For instance, IEC Publication 317-11 covers Litz-wire of 3 to 400 strands of 0.025mm to 0.071mm diameter. Standards and manufacturer's catalogs should be consulted for engineering data.

Litz-wire is generally only useful where ample winding space is available.

The main drawback of Litz-wire is its low space (copper) factor. Typically, only one quarter to one third of the winding space will be conductor.

NON-SINUSOIDAL CURRENT, EFFECTIVE FREQUENCY

So far, sinusoidal current waveform of frequency equal to the switching frequency has been assumed.

When considering proximity effect loss compared to DC (i.e., frequency-independent) loss, it was found that the total loss is minimum if the ratio of eddy-current loss to DC loss is 1:3 in strip or foil windings and 1:2 in multi-layer wire windings. In single-layer and half-layer windings there was no such optimum ratio.

The current waveforms associated with SMPS transformers are generally far from sinusoidal.

A non-sinusoidal repetitive waveform can be represented by a DC component, a component at the fundamental frequency (the switching frequency) and several components at harmonic frequencies. The DC component will not, of course, cause eddy-current loss: its current density is uniform over the conductor cross-section. The fundamental component has eddy-current loss as well as DC loss associated with it. This is also the case for the harmonic components, but the ratio of eddy-current to DC loss will be higher than for the fundamental.

Neglecting the non-sinusoidal character of the current waveform introduces an inaccuracy.

The sum of all eddy-current losses should be determined together with the total DC loss to ensure that they have the desired optimum ratio.

One problem is that, when designing the windings, it is not possible to make a reliable estimate of the current waveform.

Sometimes it is possible to make use of experience gained in previous designs.

Many designs have, in fact, been made as if the current were sinusoidal and the results have usually been satisfactory.

The errors due to calculation only at the switching frequency oppose. The component of loss occurring at DC is overestimated, whereas the components due to harmonics are underestimated.

The inaccuracy can be avoided by using an effective frequency in winding design.

The effective frequency is, of course, notional. It should be used only in connection with eddy-current effects.

In so far as eddy-current loss is proportional to φ^4 (that is to f^2), the effective frequency can be found from an analysis of the current waveform:

$$f_e = \frac{1}{2\pi}\frac{i}{I}$$

where I is the RMS winding current; i is the RMS value of dI/dt, the first derivative of the current waveform.

This expression does not apply in the region of skin conduction, where the eddy-current loss is proportional to φ or $\sqrt{f}$.

It is apparent that i contains no contribution from the DC component and a more pronounced contribution from the harmonics, since $d(\sin n\omega t)/dt = n\omega \cos n\omega t$. The rise and fall times of the current pulses have a considerable effect on the value of i. Moreover, some (if not all) of the higher harmonics lie in the region of skin conduction.

A simple method of determining f_e has not yet been found: f_e can be expected to be lower than the switching frequency f, but higher than $fI_{E\ AC}/I_E$, where $I_{e\ AC} = \sqrt{(I_e^2 - I_0^2)}$ is the RMS value of the AC component and I_0 is the DC component.

High-Frequency Ferrite Power Transformer and Choke Design

The use of this effective frequency, despite its not being valid in the region of skin conduction, will yield the optimum winding geometry.

Single-layer windings are chosen if $p_{ID} \leq 1$ and since f_e is valid for determining P_{id} the choice between multilayer and single-layer windings is clear. Both single and half-layer windings are close-packed, in principle, so their layer geometry is independent of frequency.

Since the effective frequency for the skin-conduction region is not known, winding loss cannot be accurately estimated, and, consequently, a reliable choice between a single-and a half-layer winding cannot always be made. In most practical cases, however, these problems do not occur because, in any case, strip windings are preferable in this region.

For use in choke design an expression for f_e has been derived and simplified, but due to the large variation in conditions it is impossible to give a typical example for transformer design.

For the waveform of Figure 27, provided that the rise and fall times are between 15% and 85% of the repetition period.

$$f_e \cong \frac{1.3f}{\sqrt{[1 + 3(I_0/I_{AC})^2]}}$$

and the effective current

$$I_e = \sqrt{(I_0^2 + I_{AC}^2/3)}.$$

For a sinusoidal rather than a triangular waveform superimposed on a DC current.

$$f_e = \frac{f}{\sqrt{[1 + 2(I_0/I_{AC})^2]}}$$

and

$$I_e = \sqrt{(I_0^2 + 1_{AC}^2/2)}.$$

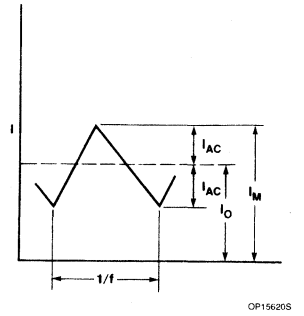


Figure 27. Current Waveform in a Smoothing Choke Idealized for the Calculation of Effective Frequency

APPENDIX: Example of Tables of Standard Wires Sizes

Enamelled Round Copper Winding Wire, IEC-grade 2

NOMINAL DIAMETER d (mm)	MAXIMUM OVERALL DIAMETER d_O (mm)	NOMINAL CROSS-SECT AREA (mm^2)	MINIMUM WINDING PITCH t_{MIN} (mm)	NOMINAL RESISTANCE AT 100°C r_{DC} (Ω/m)
0.040	0.054	0.00126	0.059	17.68
0.045	0.061	0.00159	0.066	13.97
0.050	0.068	0.00196	0.073	11.32
0.056	0.076	0.00246	0.082	9.022
0.063	0.085	0.00312	0.091	7.129
0.071	0.095	0.00396	0.102	5.613
0.080	0.105	0.00503	0.112	4.421
0.090	0.117	0.00636	0.125	3.493
0.100	0.129	0.00785	0.137	2.829
0.112	0.143	0.00985	0.152	2.256
0.125	0.159	0.0123	0.169	1.811
0.140	0.176	0.0154	0.187	1.444
0.160	0.199	0.0201	0.210	1.1052
0.180	0.222	0.0254	0.234	0.8733
0.200	0.245	0.0314	0.257	0.7074
0.224	0.272	0.0394	0.284	0.5639
0.250	0.301	0.0491	0.315	0.4527
0.280	0.334	0.0616	0.348	0.3609
0.315	0.371	0.0779	0.387	0.2852
0.355	0.414	0.0990	0.431	0.2245
0.400	0.462	0.126	0.481	0.1768
0.450	0.516	0.159	0.538	0.1397
0.500	0.569	0.196	0.593	0.11318
0.560	0.632	0.246	0.659	0.09022
0.630	0.706	0.312	0.736	0.07129
0.710	0.790	0.396	0.823	0.05613
0.800	0.885	0.503	0.922	0.04421
0.900	0.990	0.636	1.032	0.03493
1.000	1.093	0.785	1.139	0.02829
1.120	1.217	0.985	1.268	0.02256
1.250	1.351	1.227	1.408	0.01811
1.400	1.506	1.539	1.569	0.01444
1.600	1.711	2.011	1.783	0.011052
1.800	1.916	2.545	1.996	0.008733
2.000	2.120	3.142	2.209	0.007074
2.240	2.366	3.941	2.465	0.005639
2.500	2.631	4.909	2.742	0.004527

NOTE:
Values of t_{MIN} are based on recommendations for mass production of one particular manufacturer. Other manufacturers may use different values.

Medium Enamelled Copper Wires — AWG (B. & S.) (Diameters based on BS1844: 1952 — medium covering)

AWG (B. & S.)	NOMINAL COPPER DIAMETER d		MAXIMUM OVERALL DIAMETER d_O	NOMINAL CROSS-SECT. AREA	NOMINAL RESISTANCE AT 100°C r_{DC}	MINIMUM WINDING PITCH t_{MIN}
	Inch	mm	(mm)	(mm^2)	(Ω/m)	(mm)
44	0.00198	0.0503	0.06604	0.00199	11.190	0.071
43	0.00222	0.0564	0.07366	0.00250	8.899	0.079
42	0.00249	0.0633	0.08128	0.00314	7.073	0.087
41	0.00280	0.0711	0.09144	0.00397	5.594	0.098
40	0.00314	0.0798	0.1041	0.00500	4.448	0.111
39	0.00353	0.0897	0.1143	0.00631	3.519	0.122
38	0.00397	0.1008	0.1295	0.00799	2.783	0.138
37	0.00445	0.1130	0.1148	0.01003	2.215	0.154
36	0.00500	0.1270	0.1626	0.0127	1.754	0.172
35	0.0056	0.1422	0.1778	0.0159	1.398	0.188
34	0.0063	0.1600	0.1981	0.0201	1.105	0.209
33	0.0071	0.1803	0.2235	0.0255	0.8700	0.236
32	0.0080	0.2032	0.2489	0.0324	0.6853	0.261
31	0.0089	0.2261	0.2743	0.0401	0.5537	0.287
30	0.0100	0.2540	0.3048	0.0507	0.4386	0.319
29	0.0113	0.2870	0.3404	0.0647	0.3435	0.356
28	0.0126	0.3200	0.3759	0.0804	0.2762	0.393
27	0.0142	0.3607	0.4191	0.1022	0.2175	0.438
26	0.0159	0.4039	0.4699	0.128	0.1735	0.491
25	0.0179	0.4547	0.5232	0.162	0.1369	0.547
24	0.0201	0.5105	0.5817	0.205	0.10860	0.608
23	0.0226	0.5740	0.6502	0.259	0.08586	0.679
22	0.0253	0.6426	0.7214	0.324	0.06852	0.754
21	0.0285	0.7239	0.8052	0.412	0.05399	0.841
20	0.0320	0.8128	0.8966	0.519	0.04283	0.937
19	0.0359	0.9119	1.003	0.653	0.03403	1.048
18	0.0403	1.024	1.118	0.823	0.02700	1.168
17	0.0453	1.151	1.247	1.040	0.02137	1.303
16	0.0508	1.290	1.389	1.308	0.01699	1.452
15	0.0571	1.450	1.557	1.652	0.01345	1.627
14	0.0641	1.628	1.737	2.082	0.010670	1.815
13	0.0720	1.829	1.943	2.627	0.008460	2.030
12	0.0808	2.052	2.172	3.308	0.006717	2.270
11	0.0907	2.304	2.431	4.168	0.005331	2.540
10	0.1019	2.588	2.720	5.261	0.004224	2.842

NOTE:
Values of t_{MIN} are based on recommendations for mass production of one particular manufacturer. Other manufacturers may use different values.

High-Frequency Ferrite Power Transformer and Choke Design

PART 4: IMPROVED METHOD OF POWER CHOKE DESIGN

A power smoothing choke which is to carry a significant direct current component or to have a well-defined inductance is usually wound on a core whose magnetic circuit includes an air gap. The reluctance (magnetic resistance) of this air gap reduces the effective permeability of the core: either to increase the ampere-turns at which saturation occurs, or to reduce the effect of variations in the permeability of the core material on the inductance of the choke.

The traditional route to the design of a choke with a gapped core involves the use of Hanna curves, or some derivative of them. This design route has a number of disadvantages and limitations. Initial core selection is uncertain and designs may have to be made using a number of cores before the optimal solution is found. The design procedure involves considerable calculation and iteration, and the effects of changes in core operating conditions and mechanical tolerances, especially on the airgap, are not readily predicted.

To simplify the design of power chokes using Ferroxcube grade 3C8 cores, we have devised a method based on computer-generated charts. The first step in the design is the selection of a suitable core: this selection usually proves to be final. The published data for each core includes a further chart that replaces the Hanna curve and which is used for graphical design of the choke.

DESIGN METHOD

Ferroxcube 3C8 manganese-zinc ferrite is established as an excellent material for power transformer and choke cores operating at ultrasonic frequencies, especially those in switched-mode power supplies (SMPS). The new core selection and design charts greatly simplify the design of such chokes.

Starting with the peak current I_M that the choke is required to pass without saturating the core, and the minimum inductance required L_{MIN}, the designer obtains directly all the information necessary for the construction of the choke. Core size, spacer thickness, number of turns, and winding geometry are derived by straightforward procedures. Of special interest to those engineers to whom the subject is a black art: the magnetic properties of the core do not enter into the process at all.

The design method allows for ratios of alternating to direct current from small (smoothing chokes) to large (push-pull converter chokes). Parameter spreads due to manufacturing and temperature variations are taken into account in the construction of the design charts. The design procedures allow for spacer tolerances.

DEFINITION OF SYMBOLS

SYMBOL	UNIT	DEFINITION
A_L	H	Induction factor L/N^2
b_W	mm	Winding (layer) breadth
B_M	T	Peak flux density
d	mm	Nominal wire diameter
d_O	mm	Overall wire diameter
f	kHz	Frequency
f_e	kHz	Effective frequency (see text)
F_R	-	AC resistance factor R_{ac}/R_{dc}
h	mm	Thickness of foil conductor
H	mm	Winding height
H_A	mm	Available winding height
i	mm	Thickness of interleaving
I_e	A	RMS current at full load
I_0	A	DC component of current at full load
I_{AC}	A	AC component of current at full load
I_M	A	Peak value of current at full load
L	H	Inductance
N	–	Number of turns in a winding
p	–	Number of layers
P_W	W	Winding loss
R_{AC}	Ω	AC resistance
R_{DC}	Ω	DC resistance
s	mm	Spacer thickness

NOTE:
Subscript ID means "ideal" value.

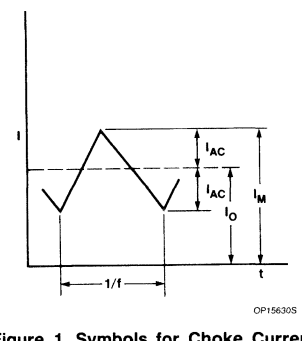


Figure 1. Symbols for Choke Current Used in the Text (See also the Table)

Core Operating Conditions

The selection and design charts are constructed for cores of Ferroxcube 3C8 operating at a hotspot temperature of 100°C. Operation at lower temperatures leads neither to core saturation nor to inductances lower than L_{MIN}. The design peak flux-density B_M is 0.32 T; however, the charts can be used for a lower value by designing for a peak current $0.32I_M/B_M$. (Symbols used in this article are listed and defined in the table; symbols for currents are illustrated by Figure 1. Note that in the equations the unit of frequency is kHz, *not* Hz; and the unit of length, mm. Some constants in the equations are based on these units.)

APPLICATIONS

For the purposes of the new design method, applications are divided into three classes:

I $I_{AC}/I_0 < 0.3$ as in smoothing chokes, and converter chokes for flyback-type SMPS, where the core flux-density remains above zero.

II $I_{AC}/I_0 \approx 1$ as in chokes where the operating flux-density returns periodically to zero. This is the case with flyback converters of the ringing-choke type.

III $I_{AC}/I_0 > 2$ as in converter chokes for push-pull-type SMPS, and fluorescent-lighting ballast chokes, where excitation is symmetrical.

In class III applications, the limiting factor in a design is core loss rather than core saturation. Operation at a permissible level of core loss usually entails reducing the peak flux density in the core; the amount of the reduction depends on operating frequency. The treatment given to class III designs here generally yields satisfactory results.

High-Frequency Ferrite Power Transformer and Choke Design

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CORE SELECTION

The design charts are supplemented by three core selection charts. Each chart covers a group of core types according to shape:

- UU and UI cores (Figure 2), comprising respectively two U cores of a U and an I core, generally give designs with the lowest ferrite cost. However, they are not available complete with coil formers.
- EE cores, a pair of E cores, may be preferable where other considerations dominate, such as the availability of coil formers.
- EC cores, although designed primarily for transformers, might perhaps be chosen because their use for both transformers and chokes in the same equipment simplifies parts stocking.

Figure 2 shows the core selection chart for UU and UI cores, examples of which are shown in Figure 3.

Selection Procedure

The selection curves are used to select a suitable core for the intended application. A full design can then be made using the design chart in the core data sheet with confidence that the result will be useful. The selection charts are used as follows:

- Knowing the value of peak choke current I_M and the minimum inductance required L_{MIN}, calculate the value of $I^2_M L_{MIN}$.
- Choose, at least provisionally, the shape of core (UU/UI, EE, or EC) based on the considerations in the previous paragraph. Draw on the appropriate selection chart a horizontal line $I^2_M L_{MIN}$. For class III designs use a value of $0.1fI^2_M L_{MIN}$, where f is the operating frequency in kHz.
- A core whose curve intersects this horizontal line can be used for the application. The spacer thickness corresponding to the intersection is, however, only an indication of the final value.

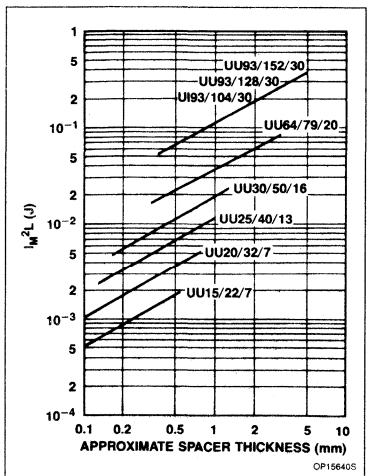


Figure 2. Selection Chart for U Cores



Figure 3. A Selection of Cores in Ferroxcube Grade 3C8 Ferrite

Effect of Core Size

Where, as is usual, more than one core could be used, the final choice may be governed by the consideration that operation near the right-hand end of the curves carries the risk of overheating. Moreover, selection of a larger core will generally result in a more conservative, efficient design than one based on a core that is only marginally large enough.

SPACER THICKNESS AND NUMBER OF TURNS

In the data sheet for the type of core selected, refer to the chart giving $(I^2_M L)_{MAX}$ and A_L as functions of spacer thickness. (Note: A_L for these power cores is the induction factor in Henrys.)

The charts contain a pair of curves of $(I^2_M L)_{MAX}$ and A_L for each of the three application classes. The design chart for the UU64/79/20 is given as Figure 4. In the design procedure, use the pair of curves of the appropriate class of application, as follows:

1. On the chart, draw again the horizontal line $I^2_M L_{MIN}$ (or $0.1fI^2_M L_{MIN}$ for class III applications) as in the selection procedure. The working point of the core must lie above this line and below the $(I^2_M L)_{MAX}$ curve for the core. In Figure 5, that is between lines SQ and SP.
2. Select a suitable spacer, of nominal thickness s. Draw vertical lines s_{MIN} and s_{MAX} on the chart, where $s_{MAX} - s_{MIN}$ is the tolerance field on the thickness of the spacer and the associated adhesive films. (Epoxy adhesive films vary in thickness from about 10μm to about 20μm.) Ensure that the horizontal distance between the intersection and s_{MIN} (a in Figure 5) is greater than the distance from s_{MIN} to s_{MAX} (b in Figure 5).
3. For s_{MIN}, read values of $(I^2_M L)_{MAX1}$ and A_{L1} from the chart. To avoid saturation the maximum number of turns allowed is

$$N_{MAX} = \sqrt{\frac{(I^2_M L)_{MAX1}}{I^2_M A_{L1}}} \qquad (1)$$

NOTE:
The upper left-hand corner of the shaded area in Figure 5 is the most critical point regarding number of turns and core saturation.

4. For s_{MAX}, read the value of A_{L2}. The minimum number of turns required to achieve L_{MIN} is then

$$N_{MIN} = \sqrt{\frac{L_{MIN}}{A_{L2}}} \qquad (2)$$

NOTE:
The lower right-hand corner of the shaded area is the most critical for number of turns and L_{MIN}.

5. Select an integral number of turns N between N_{MIN} and N_{MAX}.

NOTE:
If 'a' was taken to be only marginally greater than 'b' (Figure 5), the design attempt might fail since such an integer would not exist. Making $a < b$ makes $N_{MAX} < N_{MIN}$.

6. Establish the winding geometry using the winding design procedure in the next section.

WINDING DESIGN

The losses due to eddy currents in a winding carrying AC increase rapidly with conductor size (as d^4 for wire), but resistive losses in a conductor decrease with increasing size (as d^{-2} for wire). It follows, therefore, that there must be a frequency-dependent 'ideal' conductor size at which losses are minimum. This sets the upper limit to conductor size; there is no reason to increase losses by using a thicker conductor. The use of a thinner conductor is sometimes tolerable (low current density) or necessary (inadequate space).

The procedures that follow allow the ideal number of layers and wire size, or the thickness of strip, to be determined for chokes with an operating current waveform similar to that shown in Figure 1. They also indicate the course of action in the event of the available

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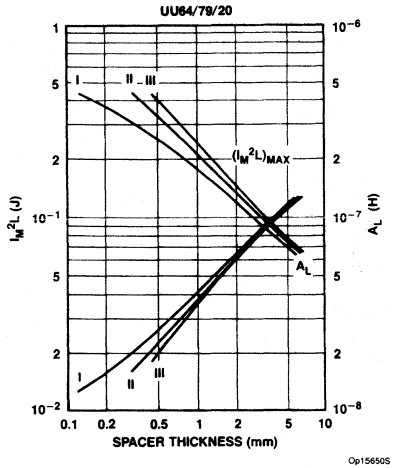


Figure 4. Design Chart for the UU64/79/20

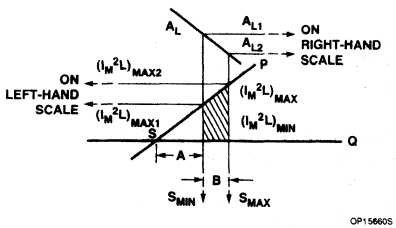


Figure 5. Construction for Graphical Design of Chokes Using the New Design Charts

winding window being insufficient to accommodate the ideal winding.

Copper conductors are assumed here and the operating temperature is taken to be 100°C, so that conductor resistivity is $1/45\Omega mm^2/m$ (30% higher than that at 20°C). Symbols used are defined in the Table and Figure 1.

Effective Frequency and Effective Current

To allow for the effect of waveform on eddy-current losses in the choke windings, it is necessary to convert actual frequencies and currents to effective values. For sinusoidal currents, the effective frequency f_e is equal to the actual frequency f. For small amounts of waveform distortion, and small DC components, f_e can still be taken as equal to f. For the waveform of Figure 1, and provided that the rise and fall times are between 15% and 85% of the repetition period,

$$f_e = \frac{1.3f}{\sqrt{1 + 3(I_0/I_{AC})^2}}$$

In designs for class I applications f_e may be only a few kiloHertz. Eddy-current effects are then negligible so that windings can be designed as if they are to carry DC only. Remember to use the correct value for DC resistivity.

For the waveform of Figure 1, the effective current I_e is given by:

$$I_e^2 = I_0^2 + I_{AC}^2/3$$

For sinusoidal currents with a significant DC component, however,

$$f_e = \frac{f}{\sqrt{1 + 2(I_0/I_{AC})^2}}$$

and

$$I_e^2 = I_0^2 + I_{AC}^2/2$$

where I_{AC} is the amplitude of the AC component.

Multi-Layer Wire Windings of Solid, Round Wire

In the following design procedure, it is assumed that all layers have the same breadth. However, where the number of turns in the winding cannot be divided into the ideal number of layers, a difference of one turn per layer is permissible.

1. The ideal wire diameter is

$$d_{ID} = 2.6\left(\frac{b_W}{Nf_e}\right)^{1/3}$$

2. Select the nearest standard wire size (for d and d_O) from a wire table such as that for IEC grade 1 winding wires.
3. The ideal number of layers is now

$$p_{ID} = \frac{N}{b_W/d_O - 1}$$

NOTE:
This expression is valid only for d_O from Step 2.

- If $p_{ID} \geqslant 1.5$ and the current density in wire d_{ID} is excessive, make a new design using a larger core.
- If $p_{ID} \leqslant 1.5$, also consider a foil or strip winding.
- If $p_{ID} \leqslant 1$, the expression for d_{ID} in step 1 is not valid: go to the single-layer winding procedure.

Find p by rerounding p_{ID} to the next highest integer. This rounding increases the spacing between turns.

4. The required winding height is
$H = p(d_o + i)$
5. If H exceeds the available height H_a, or if current density is low:
   - reduce p by one layer
   - select the thickest wire for which $d_O \leqslant pb_W/(N + p)$,
   - repeat from step 4, even if $p = 1$.
6. $F_R = 1 + \frac{1}{2}(d/d_{ID})^6$.
Check: if $F_R > 2$ an error has occurred.

NOTE:
$F_R = 1.5$ for $d = d_{ID}$; when $d < 0.7\ d_{ID}$, $F_R \approx 1$.

7. $P_W = I_e^2 R_{AC} = I_e^2 F_R R_{DC}$.*

NOTE:
*The DC resistance of copper wire is $0.0283/d^2\ \Omega/m$ at 100°C.

Single-Layer Windings of Solid, Round Wire

The design procedure is to be used only when p_{ID} calculated in step 3 of the previous section comes out as equal to or less than unity.

1. Select the thickest wire for which $d_O \leqslant b_W/(N + 1)$.

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2. $F_R = 0.33\, d\, f_e^{1/2} N/(N+1)$, only if $p_{ID} \leq 1$ in step 3 of the last section. F_R has no upper limit here.

3. $P_W = I_e^2 R_{AC} = I_e^2 F_R R_{DC}$.*

NOTE:
*The DC resistance of copper wire is $0.0283/d^2\ \Omega$/m at 100°C.

Bunched-(Litz-) Wire Windings

Eddy-current effects in bunched-conductor (or Litz-wire) windings are negligible and, thus, no special design procedure is required. Conductors of this type are not, however, necessarily the complete solution: their packing factor, and, consequently, winding thermal conductivity are both low. They might be an attractive alternative where the ideal solid-conductor winding fills less than half the available height. The resistance of bunched conductors, like that of solid conductors, is 30% higher at 100°C than at 20°C.

Foil or Strip Windings

Chokes for high current, low voltage SMPS often use windings of strip or foil conductor. The width b_W of the strip is equal to the available winding width.

1. $h_{ID} = \dfrac{3.1}{\sqrt{(Nf_e)}}$

2. $h_{MIN} = 0.8\, \dfrac{h_{ID}}{\sqrt{N}}$

3. $h_{MAX} = \dfrac{H_a}{N} - i$

Choose a value for i that suits a strip of thickness about H_a/N. If h_{MAX} h_{MIN}, try a wire winding.

4. Select a strip of thickness h such that $h_{MIN} \leq h < h_{MAX}$. Aim for $h = h_{ID}$.

5. $F_R = 1 + \dfrac{1}{3}\left(\dfrac{h}{h_{ID}}\right)^4$

Check that $F_R < 1.8$; if not, reduce h. When $h = h_{ID}$, $F_R = 1.33$; when $h < 0.6$ h_{ID}, $F_R \simeq 1$.

6. $P_W = I_e^2 R_{AC} = I_e^2 F_R R_{DC}$.

NOTE:
DC resistance of copper strip is $1/(45 b_w h)\Omega$/m at 100°C.

DESIGN EXAMPLE

A choke of 30mH minimum inductance is required for a peak current of 1A at 30kHz with a waveform as shown in Figure 1. $I_{AC}/I_0 = 0.1$, so this is a class I design.

Core Selection

Cost is important and quantities justify customized coil formers, so a UU core is selected.

The value of $I^2M L_{MIN} = 3 \times 10^{-2}$J. A horizontal line of this value drawn on the UU core selection chart intersects the curve for the UU 64/79/20 core at a spacer thickness of about 0.7mm.

Number of Turns and Spacer Thickness

Another horizontal line for $I_M{}^2 L_{MIN} = 3 \times 10^{-2}$ J drawn on the design chart for the UU64/79/20 core, Figure 4, intersects the $(I^2M L)_{MAX}$ curve for class I at a spacer thickness of 0.6mm. A resin-bonded paper sheet of 0.9mm thickness with a tolerance of −0.1mm is available. Adhesive thickness is between 0.01mm and 0.02mm, so the final spacer thickness could be 0.81 to 0.92mm. Vertical lines of these values are drawn on the design chart. The condition given with reference to Figure 5, that a > b, is satisfied.

From Figure 4, $(I^2M L)_{MAX1} = 0.036$J and $A_{L1} = 2 \times 10^{-7}$H.

Thus, from Equation 1,

$$N_{MAX} = \sqrt{\frac{0.036}{1 \times 2 \times 10^{-7}}} = 424.26 \text{ turns}$$

$A_{L2} = 1.9 \times 10^{-7}$H, so the minimum number of turns is, from Equation 2,

$$N_{MIN} = \sqrt{\frac{0.03}{1.9 \times 10^{-7}}} = 397.36$$

Since N_{MAX} is, as it should be, greater than N_{MIN}, the design is successful so far and a number of turns can be selected between these limits.

Winding Design

The effective operating frequency for the core is given by Equation 3,

$$f_e = \frac{1.3 \times 30}{\sqrt{1 + 3\ (0.1^{-2})}} \simeq 2.25\text{kHz}$$

At this effective frequency, eddy-current effects can be neglected, and the winding can be designed to fit the space available, allowing for the coil former wall thicknesses.

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Application Note

THEORY OF OPERATION

Internal Voltage Reference

The internal voltage reference provides a regulated source of +5V with an accuracy of 1% (2% over temperature) from an internal bandgap control circuit. The circuit is operational over the input range of 7 to 40V.

The reference regulator is capable of supplying a minimum of 25mA to an external load and may easily be expanded to handle higher currents by the addition of an external series pass PNP transistor as shown in Figure 2.

The internal biasing bandgap reference provides two voltage levels: a regulated 1.8V and an unregulated 3.4V. The 1.8V level is used to power the digital logic, set up low T_C bias currents, and set the switching thresholds of the Low Supply Protection circuit. The 3.4V level is generated by all of the 1.8V current passing through a 1kΩ resistor. It is used to set up the bias current for the output stage and to power two buffers in the logic and a PTAT current source (which powers the two bandgap references) and is part of the low T_C bias current generator. The 3.4V level is not regulated and doesn't need to be. It can vary ±200mV without affecting the operation of the part. The only concern should be that Pin 15 be at least 5V.

Low Supply Protection (See Figure 3)

This feature assures that sufficient input voltage exists to operate all internal sections of the part reliably. A reference voltage is fed to the low supply comparator preventing operation of the output stages with supply voltages below 6V on Pin 15.

The internal 1.8V bandgap reference becomes stable when V_{IN} = 5V with T_A = 25°C. This voltage is presented to the non-inverting input of a comparator. The inverting input of this comparator is connected to 0.383 times the 5V bandgap reference. Assume V_{IN} is increasing from 0V. At V_{IN} = 5V, the positive

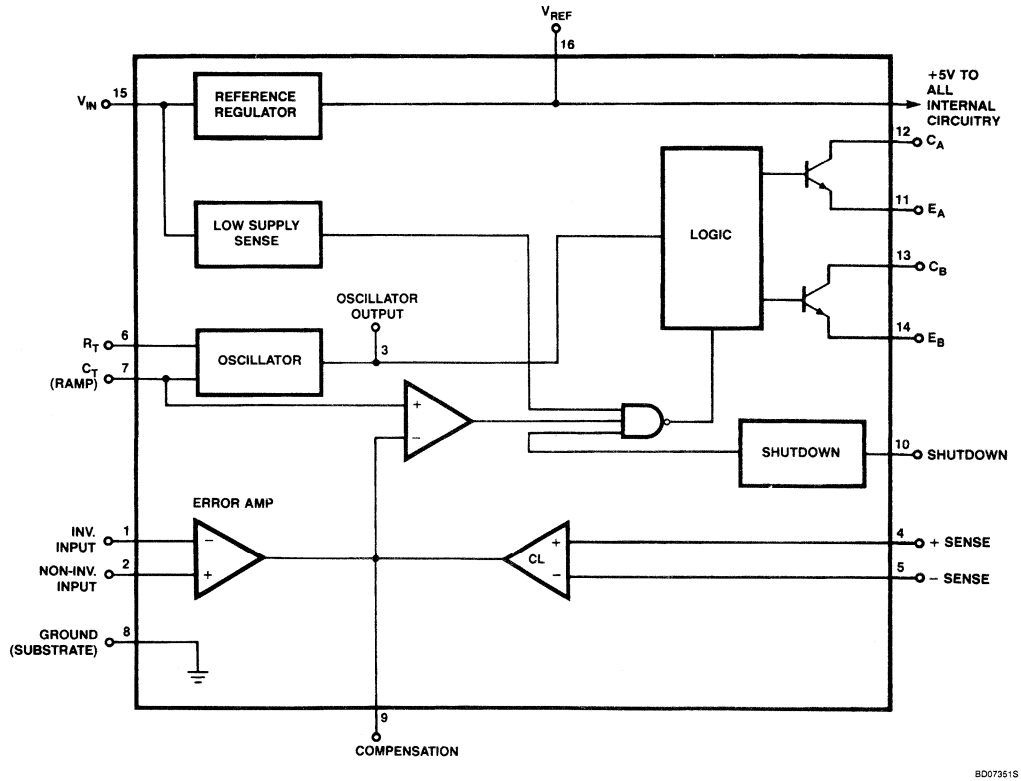


Figure 1. Expanded Block Diagram

Theory of Operation and Applications for SG1524C/2524C/3524C

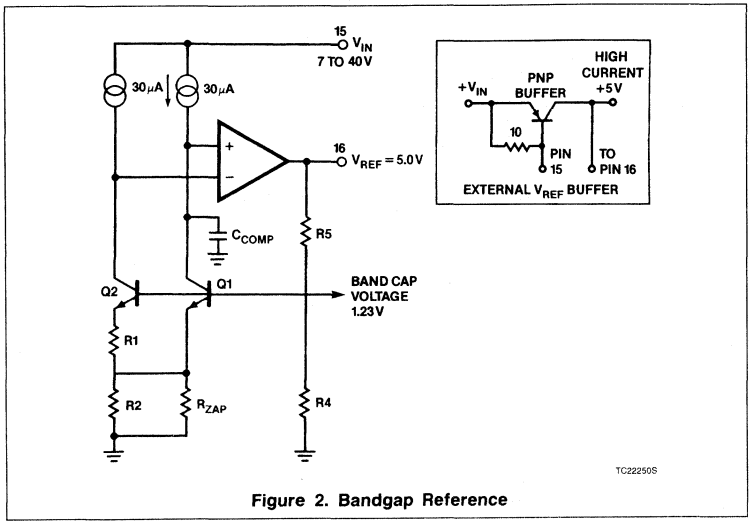


Figure 2. Bandgap Reference

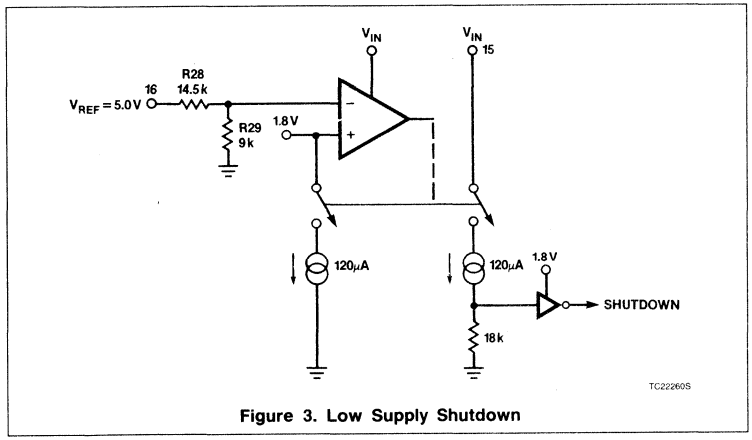


Figure 3. Low Supply Shutdown

input to the comparator sees a stable 1V while at the negative input to the comparator there is much less than 1.8V because when V_{IN} = 5V, 0.383V_{REF} is less than 1.8V. This will cause two current sources to be turned off: the first which turns the Shutdown input off, and the second which generates the hysteresis for the Low Supply Protection comparator. At this point the Shutdown Logic is active and places the output stage and logic in a disable mode.

NOTE:
Due to the low supply feature, tying Pins 15 and 16 together and operating at a supply voltage below 6.5V is not allowed as it was in the non-rev. version of this part.

When V_{IN} gets to about 6.2V, V_{REF} will be at 4.7V. The voltage divider of R28 and R29 will then present 1.8V to the comparator. 0.383V_{REF} = 0.383(4.7V) = 1.8V which will cause the comparator to switch. The new state of the comparator will turn on the two current sources mentioned before causing a shutdown condition in the logic and creating a new lower threshold (due to hysteresis) of 1.58V from a 4.13V_{REF}. When V_{IN} gets to 6.5V, V_{REF} will become stable at 5V and any further increase in V_{IN} will only cause a few millivolts of change.

Next assume V_{IN} is decreasing from some value above 6.5V (at T_A = 25°C). When V_{IN} drops low enough to force V_{REF} to 4.7V (i.e., V_{IN} = 6.2V), nothing will happen. Remember, the positive input to the comparator is now at 1.58V, not 1.8V. The switching point is actually at 1.68V because of an offset in this type of comparator. The negative input will be at 1.68V when V_{REF} is 4.4V. This is caused by V_{IN} falling to 5.9V (i.e., 1.68V = 0.383 (4.4V)). Under this condition the comparator will switch, turning off the two current sources and putting the part in the same disable state we started with at the start of this discussion, that is, the Output State is OFF. The result of all of this is 300mV of hysteresis seen at both V_{IN} and V_{REF} under all DC and AC switching conditions and over temperature. Even though it is the voltage condition on V_{REF} (Pin 16) that will turn on or off the Low Supply Protection circuit, the hysteresis will also appear at V_{IN} (Pin 15) which is where it is really needed. Also, the output of the Low Supply Protection circuit is connected to the shutdown port of the logic. This means that there are two types of protection against noise on the input supply line causing glitches on the outputs when the supply voltage is falling: 1) the hysteresis of the Low Supply Protection circuit and 2) the Double-Pulse Suppression ability of the logic.

The Pulse Width Modulator (PWM)

The pulse width modulator consists of a ramp oscillator, a high-speed comparator, and the error amplifier.

Ramp Oscillator — The ramp oscillator operates from the internal 5V reference supply. The principle of operation is that of a constant-current generator controlled by an external resistor at Pin 6 (R_T) which in turn sets the rate-of-charge on the external timing capacitor (C_T) at Pin 7. The charging current is designed to operate within the range of +0.02 to 2mA. This sets the range of values for R_T at 2k to 150kΩ. Note that frequency accuracy over temperature will be dependent on the characteristics of the timing resistor and capacitor. Carbon film or metal film resistors will be superior to carbon composition resistors. Ceramic capacitors are not recommended for timing circuit applications because of their high T_C and inaccuracies. It is better to select a mylar film, polystyrene or mica for this control element due to their inherently better dielectric qualities.

Values of C_T may vary from 0.47nF to 0.1μF and result in a operating range of 100Hz to 400kHz. The graph in Figure 5 of the data sheet shows the Frequency vs R_T/C_T values for easy selection.

Ramp Peak and Valley Voltage — The oscillator ramp voltage range sets the dynamic operating thresholds for the PWM comparator and thus controls the resulting conversion gain of the PWM modulator. The low threshold or "valley" voltage for the SG1524C is typically set at 0.75V and the high threshold or "peak" is 3.5V. Thus, the error amplifier voltage will control the active duty cycle by moving within these limits for each half cycle of the output, forcing the duty

Theory of Operation and Applications for SG1524C/2524C/3524C

cycle to range between 0 and 48.7%. (Refer to Figure 6.) Note that not only can the duty cycle be "fixed" by external shunt resistance to ground, but it can be dynamically controlled by modulating a voltage on Pin 9. Propagation delay through the PWM comparator to the output is typically 0.5μs. Maximum duty cycle limiting can be instituted by connecting an active voltage clamp to Pin 9. Leakage currents must be very low or this clamp will generate DC offset errors in the PWM response.

External Synchronization — Oscillator output, Pin 3, provides access to the PWM logic clock signal during normal operation. Alternately, it may be used to externally synchronize the Ramp Oscillator to a frequency higher than the natural period determined by R_T, C_T. Typically a pulse of 3 – 5.0V in magnitude having a 10% shorter period than the oscillator is applied to Pin 3, forcing the early reset of the ramp. Multiple units may likewise be interconnected to form a master-slave arrangement. The same differential time period conditions are set up between the master SG1524C and the slave units. Figure 7 shows a typical set of waveforms to attain synchronization.

Output Dead Time vs Timing Capacitor Value — The timing capacitor magnitude directly affects the length of the inhibit pulse sent to the PWM control logic (see Figure 8) to control the off time between alternate halves of the push-pull output drive signals. The larger the capacitance, the longer the reset time of the ramp oscillator, increasing the turn-on delay between each half cycle. This reset time, or turn-on delay, is the dead time.

Error Amplifier — This circuit is a simple differential input transconductance amplifier. The output is the compensation terminal, Pin 9, which is a high-impedance node ($R_L \approx 5M\Omega$).
The gain is:
$A_V = g_M R_L = 8I_C R_L \approx 0.002/2kT\ R_L$

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 10 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain crossover at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series R-C combination between Pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus 0.001μF.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground and thus shut off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal

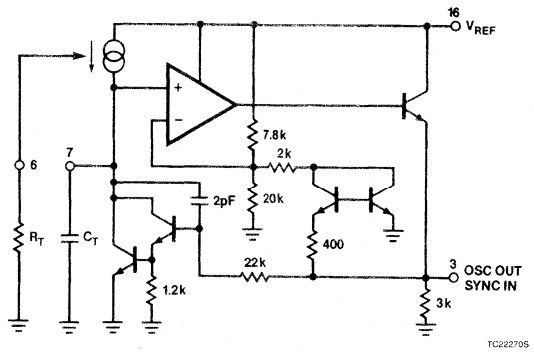


Figure 4. Oscillator

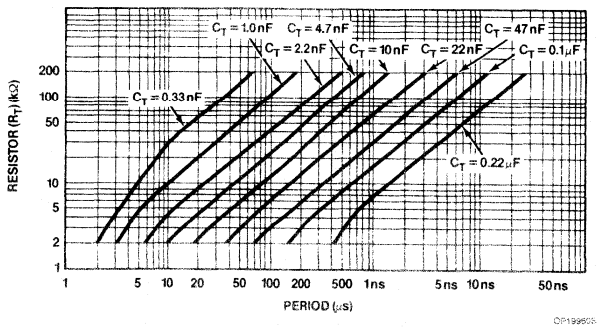


Figure 5. Oscillator Period as a Function of R_T and C_T

inversions may result. For conventional regulator applications, the 5V reference voltage must be divided down as shown in Figure 11. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open-loop test circuit.

Soft Start

Soft start can be implemented by connecting an external transistor to Pin 9 as shown in Figure 9. This will provide a controlled ramp-up of duty cycle.

Overcurrent Limit Cycle-by-Cycle

The overcurrent comparator in the SG1524C/3524C is capable of providing high-speed cycle-by-cycle shutdown of the output stage. Typical delay is 700ns from the overcurrent threshold trip to output drive inhibit. The typical threshold is 205mV. As can be seen in Figure 9, the output of the overcurrent comparator limits the PWM voltage to a typical value of 0.1V, immediately terminating the duty cycle.

Extra noise immunity may be obtained by simply raising the comparator reference pin to a suitable value of threshold voltage. One definite advantage to the SG1524C is that the common-mode voltage of the current limit comparator is −0.3V to 12.5V and the maximum differential voltage is 40V.

The proper connection to the current sense inputs for a positive waveform (V_{LIM}) is via Pin 4 (inverting input). This forces Pin 9 Low and terminates the duty cycle. (See Figure 12.)

The waveform photograph in Figure 13 shows a typical cycle-by-cycle shutdown sequence with actuation occuring on alternate phases.

Output Drivers

The NPN output transistors are greatly improved over the past SG3524 non-rev. parts and are rated at 200mA. Breakdown voltage at each collector is 60V. The collectors (Pins 12 and 13) are not diode-clamped to V_{CC}. Special isolation techniques are used in fabricating the SG1524C to allow the output collectors (V_C) to operate above the device supply voltage, (V_{IN}).

NOTE:
All other device pins must be operated below V_{IN}, Pin 15.

Rise and Fall Time

Collector rise time is 600ns maximum at 10mA with fall time at 200ns maximum. The emitters are faster with t_R equal to 200ns, maximum. Output speed becomes critical when operating near the maximum duty cycle.

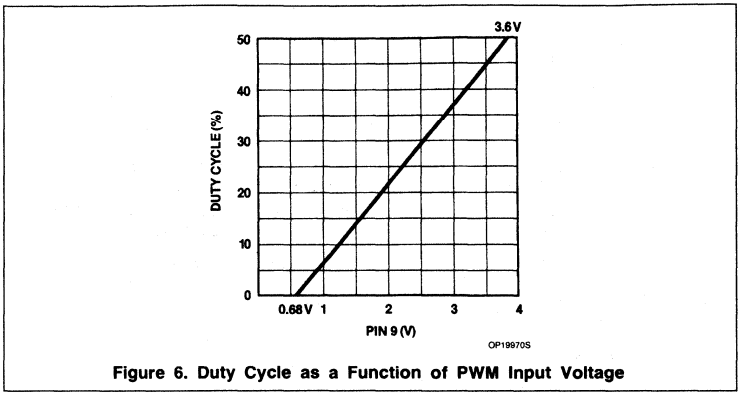


Figure 6. Duty Cycle as a Function of PWM Input Voltage

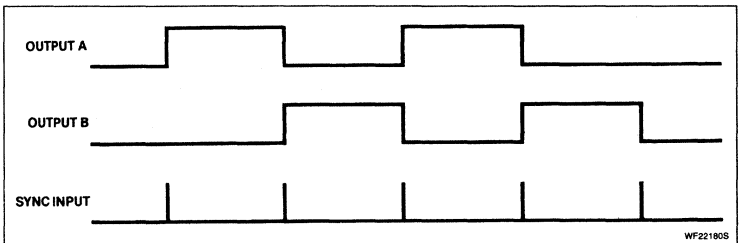


Figure 7. External Synchronization

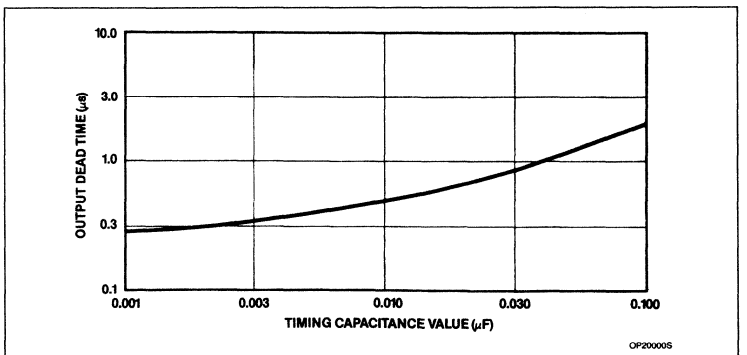


Figure 8. Output Stage Dead Time as a Function of the Timing Capacitance Value

External switching transistor turn-on and turn-off delays must be carefully considered.

Output Voltage Swing

Either inverting (collector) output or non-inverting (emitter) output may be used. Collector-emitter saturation voltages at 200mA are typically 1.2V, decreasing for lower sink currents. When operating at increased voltage levels with transformer coupling, reverse Schottky clamp diodes must be used on each collector to prevent pin voltages from going negative with respect to device ground (Pin 8). Also, high-speed overvoltage clamp diodes should be used to prevent inductive spikes exceeding the maximum voltage stand-off rating of 60V.

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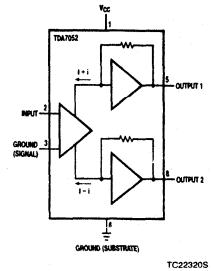


Figure 9. Soft Start Duty Cycle Limit

Power Dissipation

The device power dissipation limits must not be exceeded. This means that junction temperature under continuous operating conditions must remain below 150°C. T_J may be calculated as shown in Note 2 of the data sheet.

Example: SG1524CN

Collector Drive

$V_C = 45V$

$V_{IN} = 20V$

$I_C = 100mA$

$I = 10mA$

Duty Cycle = 0.35

$I_{REF} = -5mA$

$V_{CE} = 0.7$ on

$I_{OSC} = 5mA$

$P_D = (0.010*20) + 2\ (0.35)*(0.1)$

$*(0.7)(0.005)*(15) + 2$

$(0.005)*(16.4) = +0.488W$

Referring to the package thermal resistance listed in the package outlines section of the data book: $\theta_{JA} = 83°C/W$.

Assume an ambient temperature of 45°C. Therefore, the junction-to-ambient temperature differential is:

$T_{DIFF} = 0.455°C/W$

$J_A = 40.5°C$

$T_J = T_{DIFF} + T_A = 40.5°C + 45°C$
$= 85.5°C$

Example:

Emitter Drive
Same output current = 100mA

$P_D = (0.01*20) + 2(0.35)*$
$(0.1)*(20 - 18(0.005)*$
$(15) + 2(0.005)*(16.4)$
$= 0.579W$

$T_{JA} = (0.579)*(83°C/W)$
$= 48°C$

$T_J = 48°C + 45°C$

$T_J = 93°C$

A 100W multiple output push-pull converter is shown in Figure 4.

5V, 25W Converter

Push-pull outputs are used in this transformer-coupled DC-DC regulating converter shown in Figure 15. Note that the oscillator must be set at twice the desired output frequency since the SG1524C's internal flip-flop divides the frequency by 2 as it switches the PWM signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

SG3524C Push-Pull ±50V, 100W Converter

A simple solution to off-line converter design for power audio amplifier circuits is shown in Figure 16. The SG3524C emitter outputs are used to directly drive a pair of BUZ41A power FETs in the primary side of the step-down transformer at a 50kHz rate. (The main oscillator operates at 100kHz.) The transformer consists of 120T of #24 wire center-tapped at 60T. This is sandwiched between two 50-turn center-tapped secondary windings of #20 wire. Diodes are fast recovery BYW30s; the output chokes, 500μH wound on EC35 (3C8) pair Ferroxcube cores, provide adequate filtering in conjunction with the 1000μF and 0.01μF ceramic capacitors across the output.

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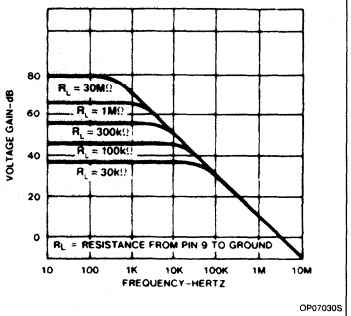
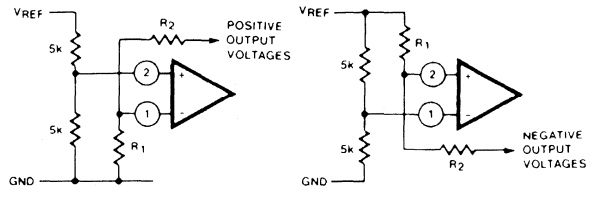


Figure 10. Amplifiers Open-Loop Gain as a Function of Frequency and Loading on Pin 9



$$V_O = \frac{2.5V\ (R = R_2)}{R1}$$

$$\frac{R_1 R_2}{R_2 = R_2} = 2.5k\Omega$$

NOTE:
Note change in input connections for opposite polarity outputs.

Figure 11. Error Amplifier Biasing Circuits

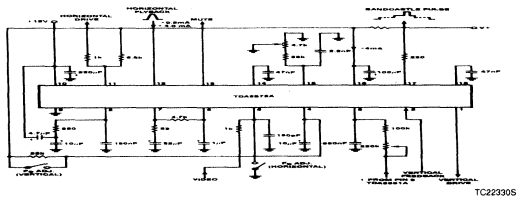


Figure 12. Current Limiting

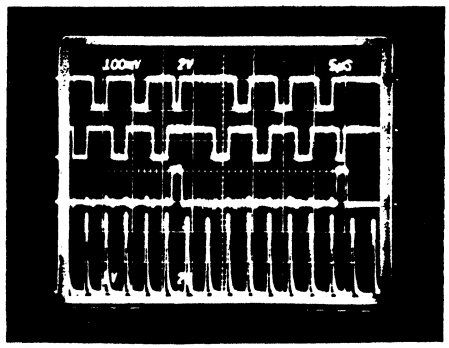


Figure 13. Cycle-by-Cycle Shutdown Sequence

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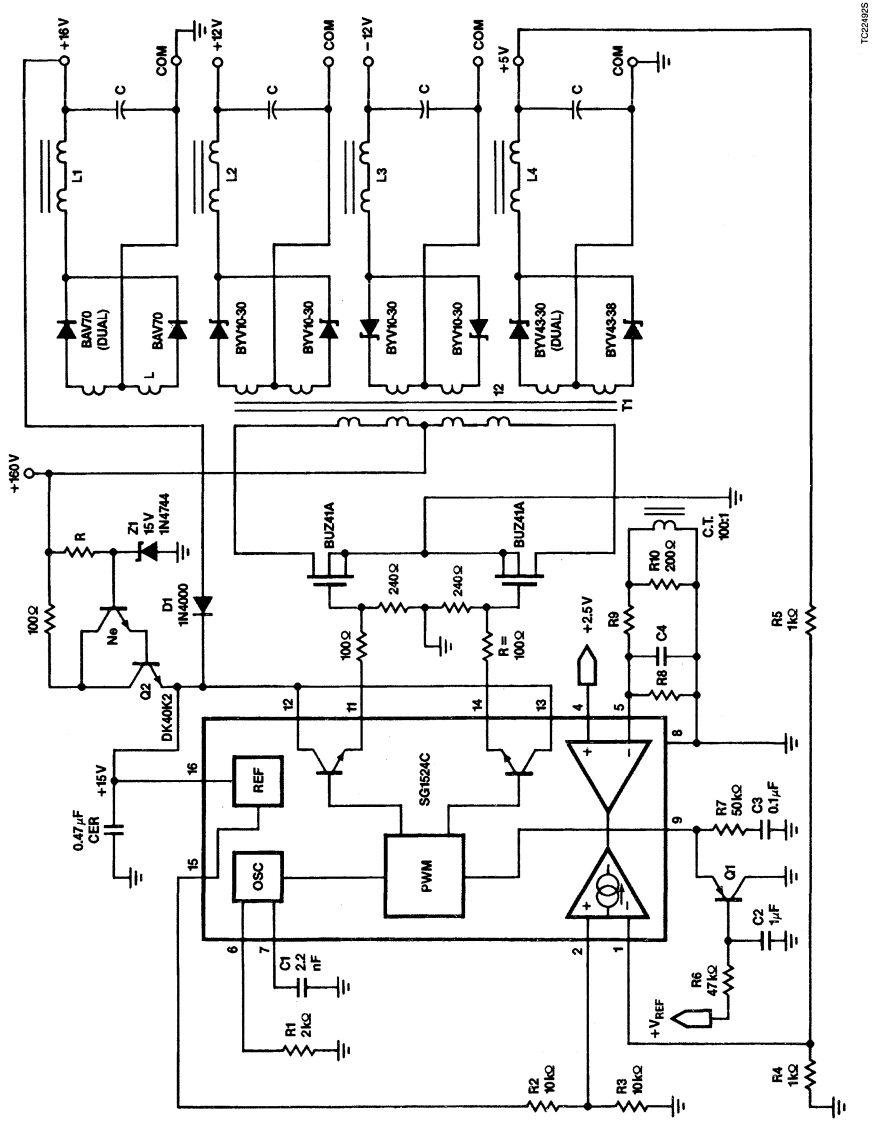


Figure 14. 100W Push-Pull Converter

NOTE:
Adjust R8, R9 for desired O.C. trip.

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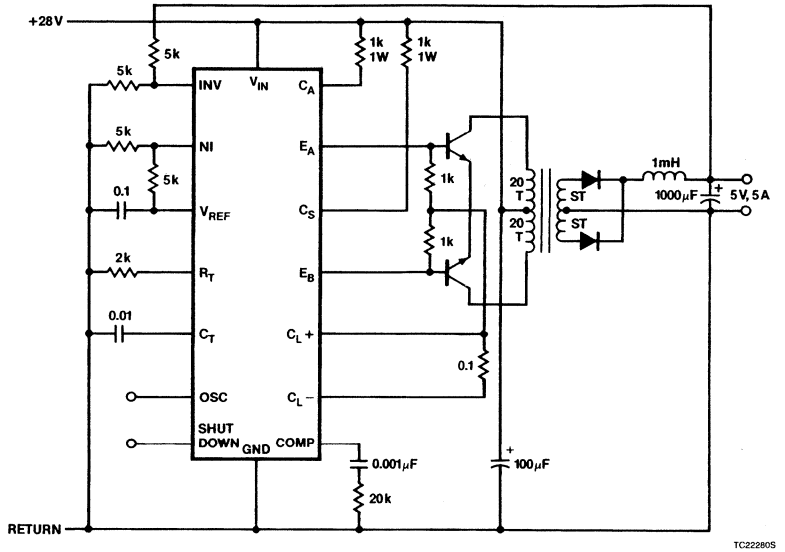


Figure 15. 5V, 25W Converter

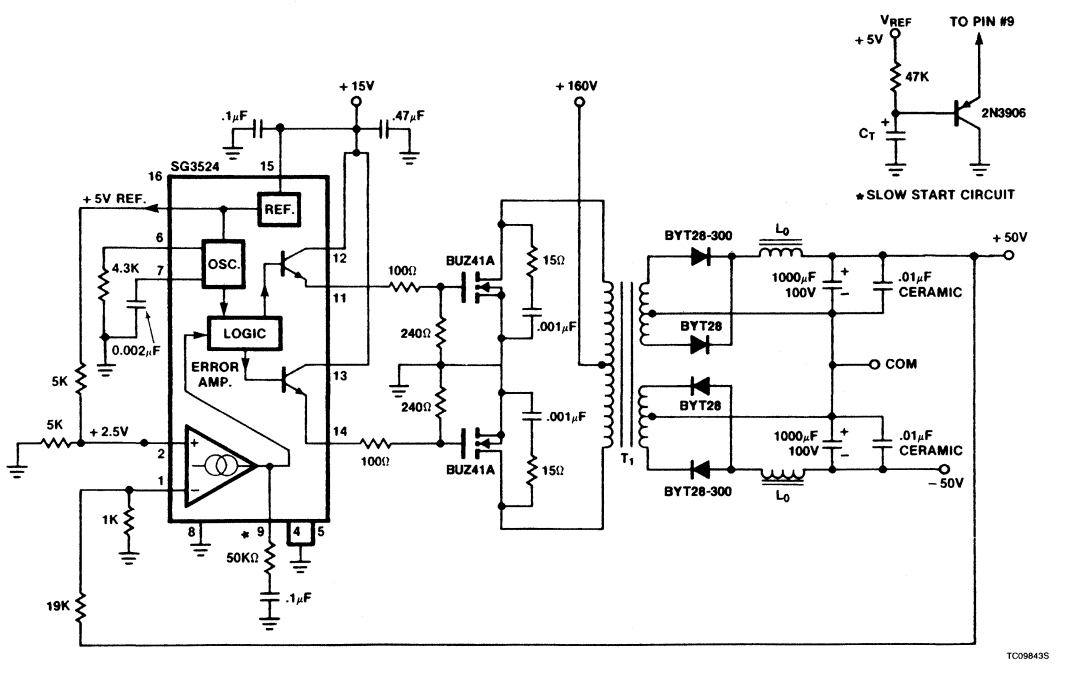


Figure 16. ±50V Push-Pull Switched-Mode Converter

SYSTEM CONTROL

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System control

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TEA5500	coded locking circuit for security systems	1159
TEA5500T	coded locking circuit for security systems	1159

CODED LOCKING CIRCUIT FOR SECURITY SYSTEMS

GENERAL DESCRIPTION

The TEA5500 is a coder/decoder circuit, for security systems. The system has the ability to transmit a complex code between a coding and decoding unit by infrared radiation. The device can operate as a coder or decoder depending on the external circuitry connected to the data input. The code is made by the 10 input pins E1 to E10 by connecting them either to ground (LOW) or to the positive supply (HIGH), or leaving them floating (∞). This allows $3^{10}-2$ combinations. Two combinations are prohibited; E1 to E10 = HIGH and E1 to E9 = HIGH, E10 = LOW.

Coding

In coding mode the data input is connected to V_P and both outputs (S1, S2) are connected to a pnp output transistor which drives an infrared radiation emitting diode.
After every start the coder completes three coding runs then stops automatically.

Decoding

In decoding mode an infrared sensitive diode is connected to the data input via an amplifier. If the input data is recognized, the data input of the decoder is temporarily closed (disregarding immediately following data) and one of the outputs is activated for a predetermined time after which the following start will activate the other output.
If the input data is not recognized, neither of the outputs are activated and after the third coding run is completed the data input of the decoder is temporarily closed.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 16)		V_P	3.0	4.5	6.5	V
Supply current (pin 16)	V_P = 4.5 V	I_P	1.8	2.5	3.2	mA
Operating ambient temperature range		T_{amb}	−40	–	+ 80	°C
Storage temperature range		T_{stg}	−50	–	+ 150	°C
Total power dissipation		P_{tot}	–	–	500	mW

PACKAGE OUTLINES

TEA5500: 16-lead DIL; plastic (SOT38).
TEA5500T: 16-lead mini-pack; plastic (SO16L; SOT162A).

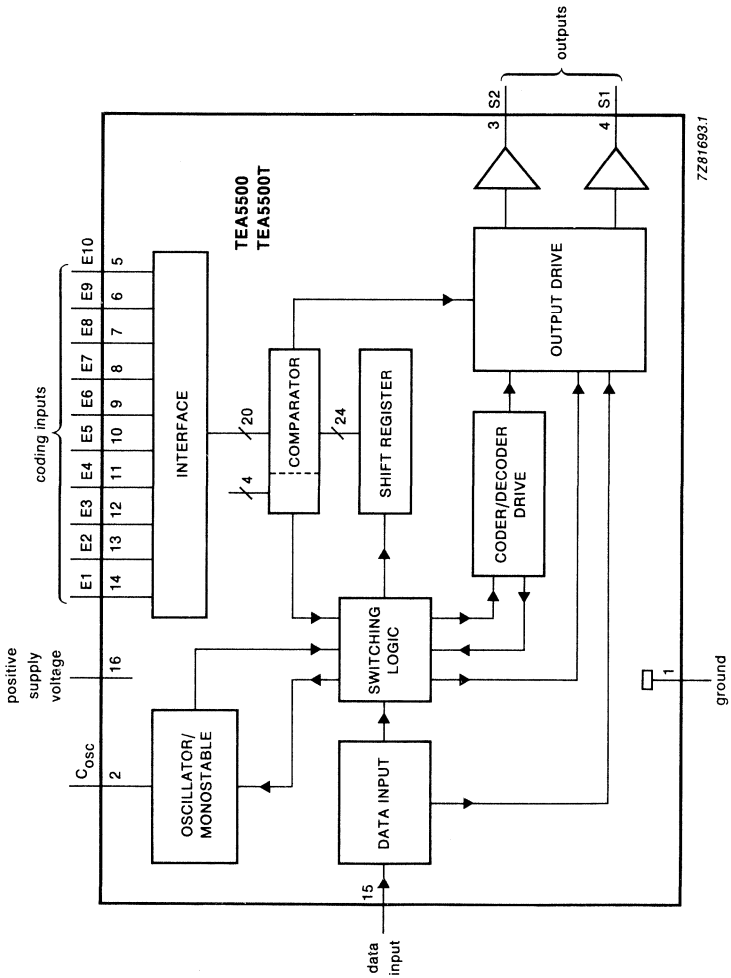


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

Pin functions

pin	mnemonic	description
1	GND	ground
2	C_{osc}	oscillator capacitor
3	S2	output 2
4	S1	output 1
5	E10	coding inputs
6	E9	
7	E8	
8	E7	
9	E6	
10	E5	
11	E4	
12	E3	
13	E2	
14	E1	
15	DATA	data input
16	V_P	positive supply voltage

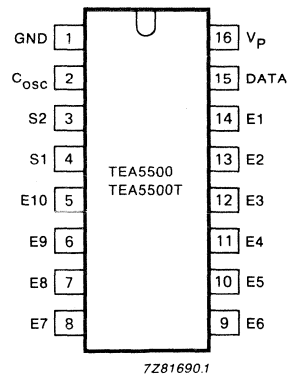


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 16)	V_P	–	7	V
Supply current (pin 16)	I_P	0	50	mA
Input voltage (pins 2 and 5 to 15)	V_I	−0.3	V_P + 0.3	V
Output voltage (pins 3 and 4)	V_O	−0.3	16	V
Total power dissipation	P_{tot}	–	500	mW
Storage temperature range	T_{stg}	−50	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 80	°C

THERMAL RESISTANCE

From junction to ambient

TEA5500: 16-lead DIL — $R_{th\ j\text{-}a}$ = 125 K/W
TEA5500T: 16-lead mini-pack — $R_{th\ j\text{-}a}$ = 160 K/W

CHARACTERISTICS

T_{amb} = 25 °C; voltages with respect to pin 1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 16)		V_P	3	4.5	6.5	V
Supply current	V_P = 4.5 V	I_P	1.8	2.5	3.2	mA
Output current (pins 3 and 4)	V_P = 4.5 V	I_O	25	–	–	mA
Inputs E1 to E10						
Input voltage HIGH		V_{IH}	V_P −0.3	–	–	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input voltage floating		V_{IFL}	1	–	V_P −1	V
Input current HIGH		I_{IH}	2	7	12	μA
Input current LOW		I_{IL}	−4	−9	−15	μA
Input current floating		I_{IFL}	–	–	2	μA
Data input						
Input voltage						
for decoding mode HIGH		V_{dH}	V_P −0.6	V_P	V_P + 0.3	V
for decoding mode LOW		V_{dL}	–	–	0.5	V
Input current						
in coding mode		I_{dc}	8	16	25	μA
in decoding mode HIGH	V_P = 4.5 V	I_{ddH}	–	–	2	μA
in decoding mode LOW	V_P = 4.5 V	I_{ddL}	−8	−16	−25	μA
Minimum pulse width of DATA input signal		τ_{dp}	2	–	–	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator characteristics	V_P = 4.5 V					
Switching voltage thresholds						
high level		V_{th}	3.10	3.32	3.50	V
low level		V_{tl}	0.65	0.71	0.90	V
Input current						
after switching high level		I_{th}	27	36	45	μA
after switching low level		I_{tl}	−6.7	−9	−11.3	μA
Ratio I_{th}/I_{tl}		ΔI_{osc}	3	4	5	
Duration of oscillator pulse						
in coding mode	note 1	τ_c	20	$0.4 \cdot C_{osc}$(pF)	–	μs
in decoding mode		τ_d	$3 \cdot \tau_c$	$0.4 \cdot C_{osc}$(pF)	$5 \cdot \tau_c$	μs
Oscillator capacitor						
in coding mode	notes 1 and 2	C_{osc}	56	–	–	pF
Duration of						
output active status		τ_o	–	$384 \cdot \tau_d$	–	
data input disabled status		τ_x	–	$576 \cdot \tau_d$	–	
Influence of temperature on duration of oscillator pulse		$\frac{\Delta\tau_c/\tau_c}{\Delta T}$	–	0.002	–	$^oC^{-1}$
Influence of supply voltage on duration of oscillator pulse		$\frac{\Delta\tau_c/\tau_c}{\Delta V_P}$	–	–	0.16	V^{-1}
Zener diode voltage across supply		V_z	6	–	8	V

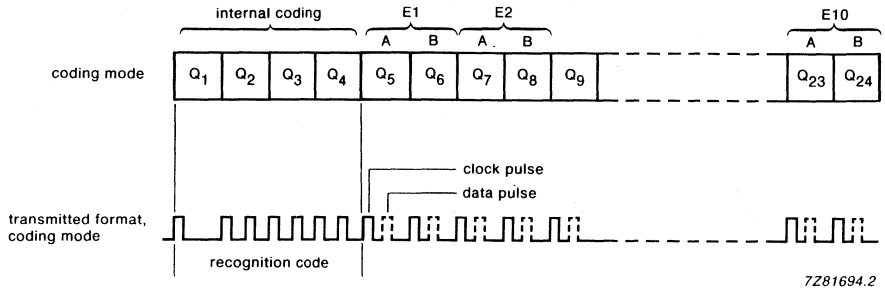
Notes to the oscillator characteristics

1. Minimum value coder – capacitor must provide minimum pulse width of DATA pulse τ_{dp} (= 1/5 τ_c).
2. Ratio coder/decoder capacitor 1:3.

DEVELOPMENT DATA

Code

The code consists of 24 bits. Each bit is represented by presence or absence of a data pulse following a clock pulse. The first 4 bits form the recognition code. The following 10 pairs of bits are determined by the connections of the input pins (E1 to E10). For the corresponding code in decoding mode the order of the input pins is reversed and connections "low" (L) and "floating" (∞) are interchanged.



coding	E1	E2	E3	-----	E8	E9	E10		∞	L	H
	↕	↕	↕		↕	↕	↕		↕	↕	↕
decoding	E10	E9	E8	-----	E3	E2	E1		L	∞	H

E	A	B	Q_A	Q_B
L	1	0	0	1
∞	0	1	1	0
H	1	1	0	0

example

coding	E1 = L	E2 = H	E3 = ∞	E4 = H	-----	E9 = L	E10 = ∞
decoding	E10 = ∞	E9 = H	E8 = L	E7 = H	-----	E2 = ∞	E1 = L

Fig. 3 Coding diagram.

TIMING

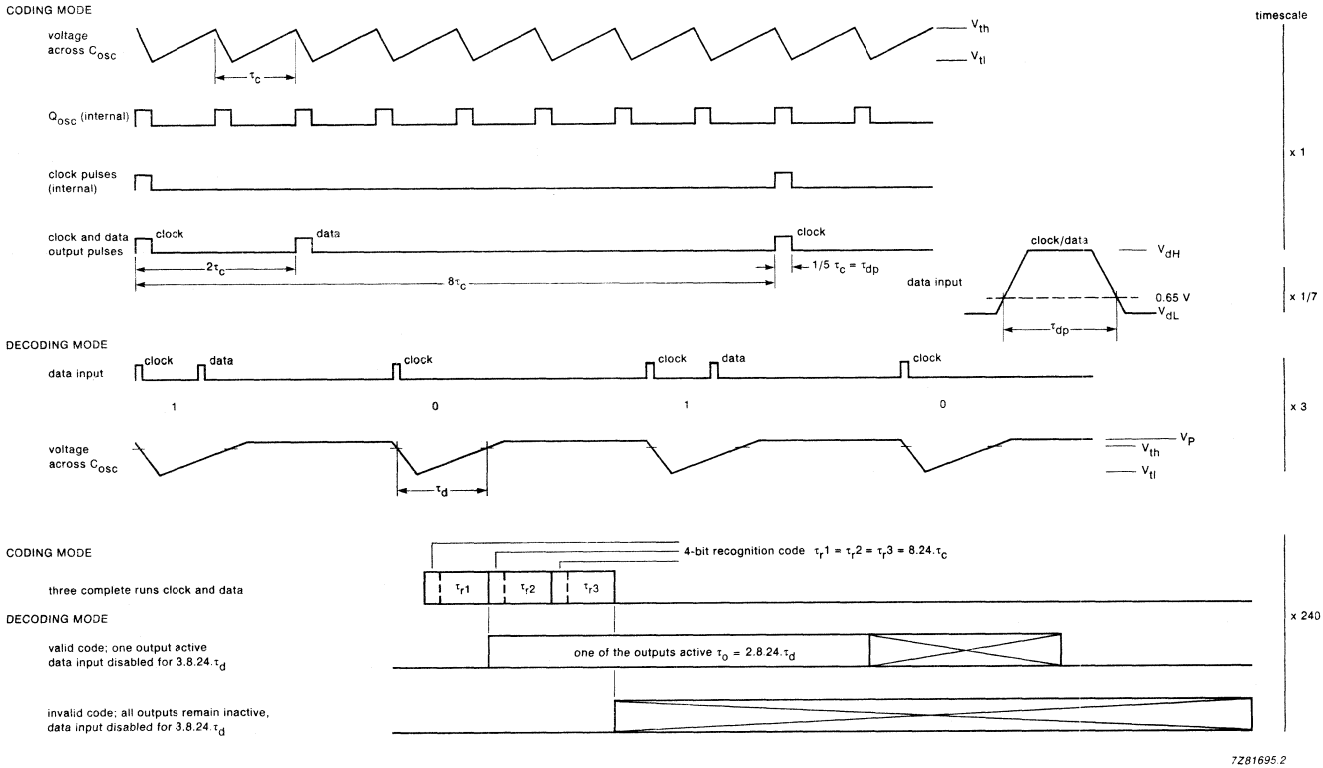
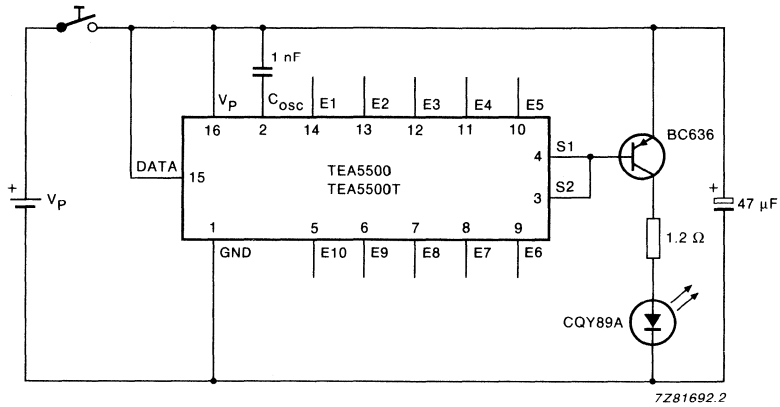


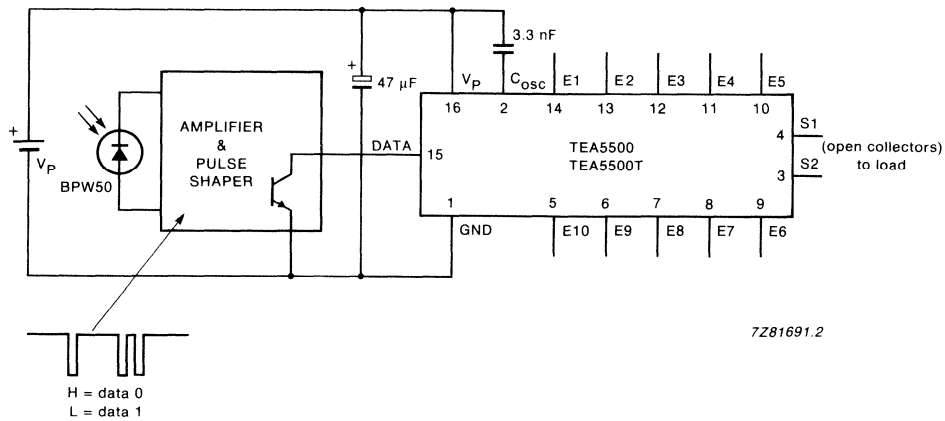
Fig. 4 Timing diagram of TEA5500.

APPLICATION INFORMATION



E1 – E10: code (H,L, ∞).

Fig. 5 Application diagram; coding mode.



E10 – E1: code (H, ∞, L).

Fig. 6 Application diagram; decoding mode.

RF COMMUNICATIONS

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Mixers/modulators/demodulators

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MC1496/MC1596
Balanced Modulator/ Demodulator

Product Specification

DESCRIPTION

The MC1496 is a monolithic double-balanced modulator/demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The MC1596 will operate over the full military temperature range of −55°C to +125°C. The MC1496 is intended for applications within the range of 0°C to +70°C.

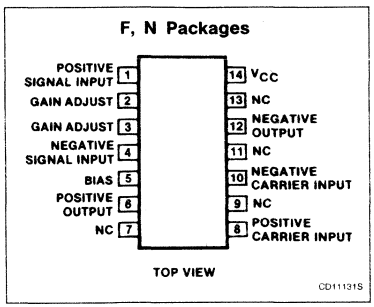
FEATURES

- **Excellent carrier suppression**
  65dB typ @ 0.5MHz
  50dB typ @ 10MHz
- **Adjustable gain and signal handling**
- **Balanced inputs and outputs**
- **High common-mode rejection — 85dB typ**

APPLICATIONS

- **Suppressed carrier and amplitude modulation**
- **Synchronous detection**
- **FM detection**
- **Phase detection**
- **Sampling**
- **Single sideband**
- **Frequency doubling**

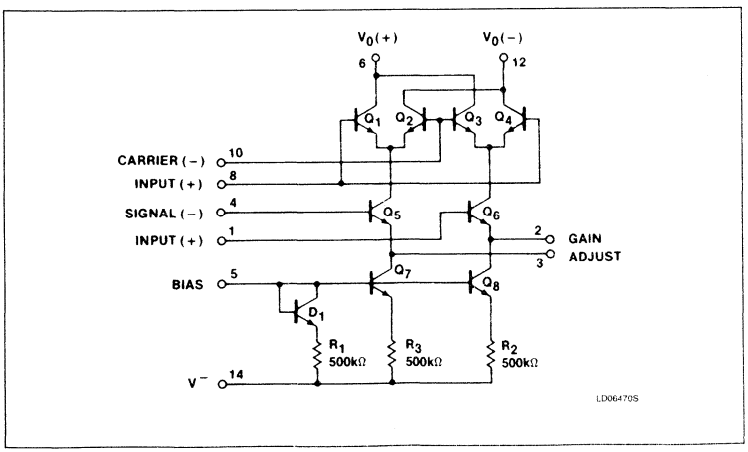
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Cerdip	0 to +70°C	MC1496F
14-Pin Plastic	0 to +70°C	MC1496N
14-Pin Cerdip	−55°C to +125°C	MC1596F
14-Pin Plastic	−55°C to +125°C	MC1596N

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Applied voltage	30	V
$V_8 - V_{10}$	Differential input signal	±5.0	V
$V_4 - V_1$	Differential input signal	$(5 \pm I_5\ R_e)$	V
$V_2 - V_1$, $V_3 - V_4$	Input signal	5.0	V
I_5	Bias current	10	mA
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package N package	 1190 1420	 mW mW
T_A	Operating temperature range MC1496 MC1596	 0 to +70 −55 to +125	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C.
   N package at 11.4mW/°C.

DC ELECTRICAL CHARACTERISTICS

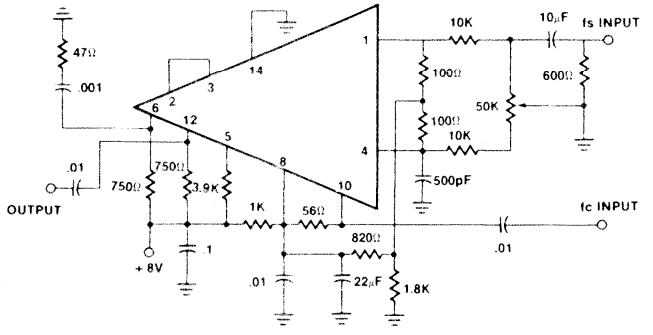
$V_{CC} = +12V_{DC}$; $V_{CC} = -8.0V_{DC}$; $I_5 = 1.0mA_{DC}$; $R_L = 3.9k\Omega$; $R_E = 1.0k\Omega$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Single-ended input impedance	Signal port, f = 5.0MHz							
R_{IP}	Parallel input resistance			200			200		kΩ
C_{IP}	Parallel input capacitance			2.0			2.0		pF
	Single-ended output impedance	f = 10MHz							
R_{OP}	Parallel output resistance			40			40		kΩ
C_{OP}	Parallel output capacitance			5.0			5.0		pF
	Input bias current								μA
I_{BS}	$I_{BS} = \frac{I_1 + I_4}{2}$			12	25		12	30	
I_{BC}	$I_{BC} = \frac{I_8 + I_{10}}{2}$			12	25		12	30	μA
	Input offset current								μA
I_{IOS}	$I_{IOS} = I_1 - I_4$			0.7	5.0		0.7	7.0	
I_{IOC}	$I_{IOC} = I_8 - I_{10}$			0.7	5.0		0.7	7.0	μA
TC_{IIO}	Average temperature coefficient of input offset current			2.0			2.0		nA/°C
I_{OO}	Output offset current $I_6 - I_{12}$			14	50		15	80	μA
TC_{IOO}	Average temperature coefficient of output offset current			90			90		nA/°C
V_O	Common-mode quiescent output voltage (Pin 6 or Pin 12)			8.0			8.0		V_{DC}
	Power supply current								mA_{DC}
I_{D+}	$I_6 + I_{12}$			2.0	3.0		2.0	4.0	
I_{D-}	I_{14}			3.0	4.0		3.0	5.0	
P_D	DC power dissipation			33			33		mW

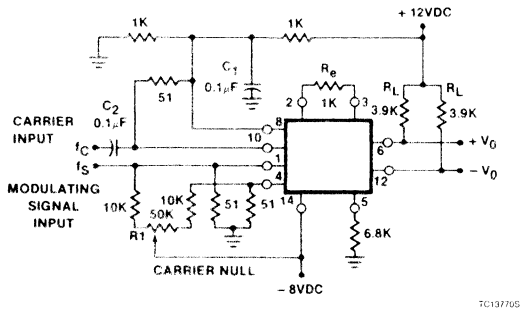
AC ELECTRICAL CHARACTERISTICS $V_{CC} = +12_{DC}$; $V_{CC} = -9.0V_{DC}$; $I_5 = 1.0mA_{DC}$; $R_L = 3.9k\Omega$; $R_E = 1.0k\Omega$; $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CFT}	Carrier feedthrough	$V_C = 60mV_{RMS}$ sinewave and offset adjusted to zero							
		$f_C = 1.0kHz$		40			40		μV_{RMS}
		$f_C = 10MHz$		140			140		
		$V_C = 300mV_{P-P}$ squarewave:							
		Offset adjusted to zero							
		$f_C = 1.0kHz$		0.04	0.2		0.04	0.4	mV_{RMS}
		Offset not adjusted $f_C = 1.0kHz$		20	100		20	200	
V_{CS}	Carrier suppressions	$f_S = 10kHz$, $300mV_{RMS}$ sinewave							
		$f_C = 500kHz$, $60mV_{RMS}$ sinewave	50	65		40	65		dB
		$f_C = 10MHz$, $60mV_{RMS}$ sinewave		50			50		
BW_{3dB}	Transadmittance bandwidth (Magnitude) ($R_L = 50\Omega$)	Carrier input port, $V_C = 60mV_{RMS}$ sinewave $f_S = 1.0kHz$, $300mV_{RMS}$ sinewave		300			300		MHz
		Signal input port, $V_S = 300mV_{RMS}$ sinewave $\lvert V_C \rvert = 0.5V_{DC}$		80			80		MHz
A_{VS}	Signal gain	$V_S = 100mV_{RMS}$; $f = 1.0kHz$ $\lvert V_C \rvert = 0.5V_{DC}$	2.5	3.5		2.5	3.5		V/V
CMV	Common-mode input swing	Signal port, $f_S = 1.0kHz$		5.0			5.0		V_{P-P}
A_{CM}	Common-mode gain	Signal port, $f_S = 1.0kHz$ $\lvert V_C \rvert = 0.5V_{DC}$		−85			−85		dB
DV_{OUT}	Differential output voltage swing capability			8.0			8.0		V_{P-P}

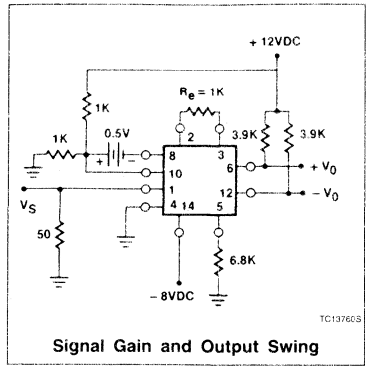
TEST CIRCUITS



Carrier Rejection and Suppression



Carrier Rejection and Suppression



Signal Gain and Output Swing

NE/SA602
Double-Balanced Mixer and Oscillator

Product Specification

DESCRIPTION

The SA/NE602 is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602 make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external L.O. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the SA/NE602 a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

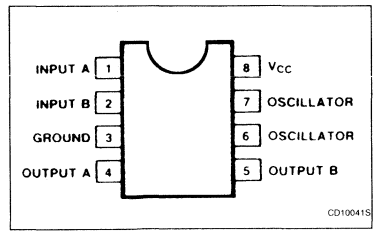
FEATURES

- **Low current consumption: 2.4mA typical**
- **Excellent noise figure: < 5.0dB typical at 45MHz**
- **High operating frequency**
- **Excellent gain, intercept and sensitivity**
- **Low external parts count; suitable for crystal/ceramic filters**
- **SA602 meets cellular radio specifications**

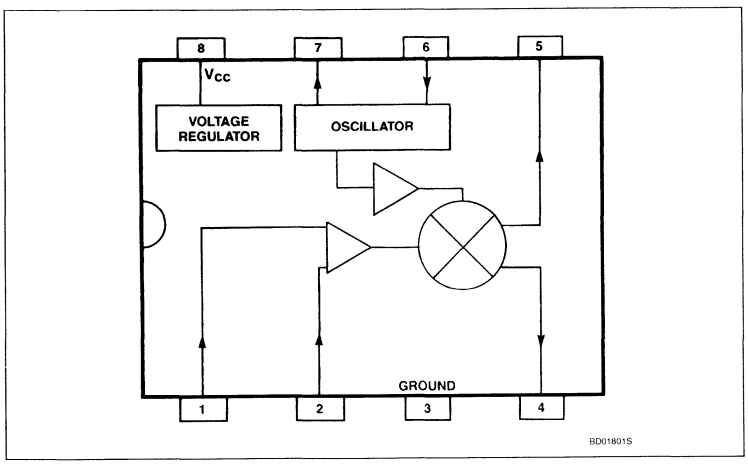
APPLICATIONS

- **Cellular radio mixer/oscillator**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **HF/VHF frequency conversion**
- **Instrumentation frequency conversion**
- **Broadband LANs**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE602N
8-Pin Plastic SO	0 to +70°C	NE602D
8-Pin Cerdip	0 to +70°C	NE602FE
8-Pin Plastic DIP	−40°C to +85°C	SA602N
8-Pin Plastic SO	−40°C to +85°C	SA602D
8-Pin Cerdip	−40°C to +85°C	SA602FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature range NE602 SA602	 0 to +70 −40 to +85	 °C °C

AC/DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 6V, Figure 1

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0	6.0	dB
	Third-order intercept point	RF_{IN} = −45dBm: f_1 = 45.0 f_2 = 45.06		−15	−17	dBm
	Conversion gain at 45MHz		14	18		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

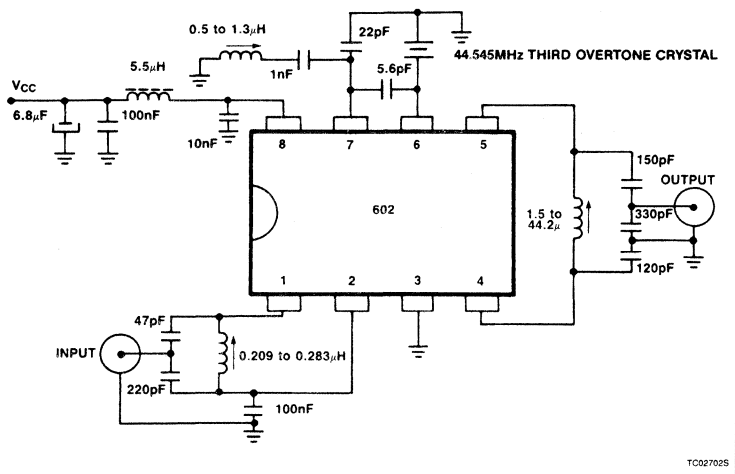


Figure 1. Test Configuration

DESCRIPTION OF OPERATION

The NE/SA602 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA602 is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio 2nd IF and demodulator, the SA602 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third-order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE602 should be appropriately scaled.

Double-Balanced Mixer and Oscillator

NE/SA602

Besides excellent low power performance well into VHF, the NE/SA602 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedence is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be at least $200mV_{P-P}$.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. 22kΩ will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

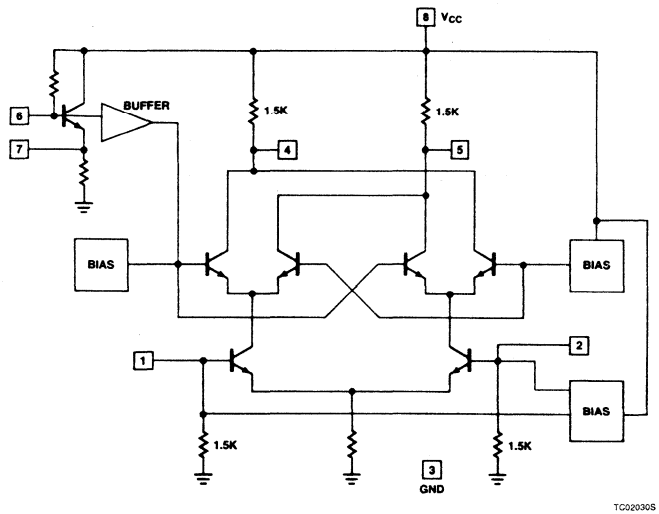
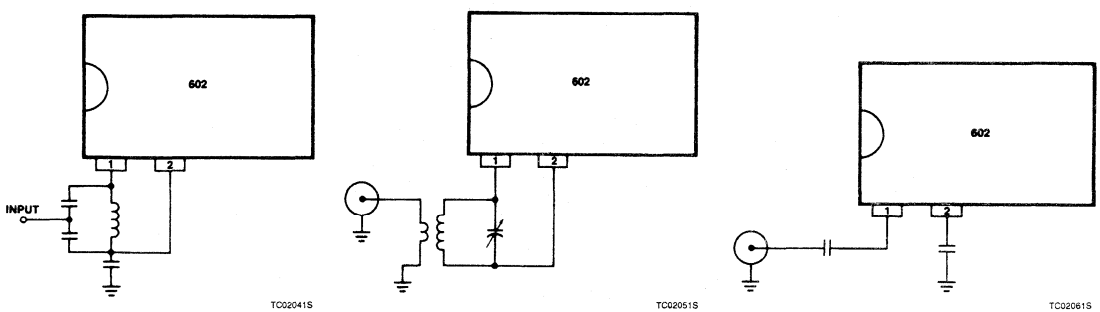


Figure 2. Equivalent Circuit

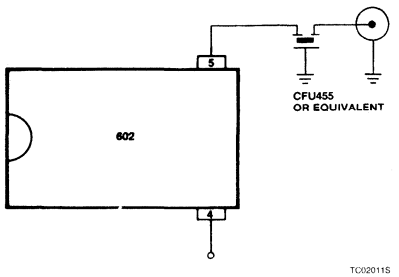


a. Single-Ended Tuned Input

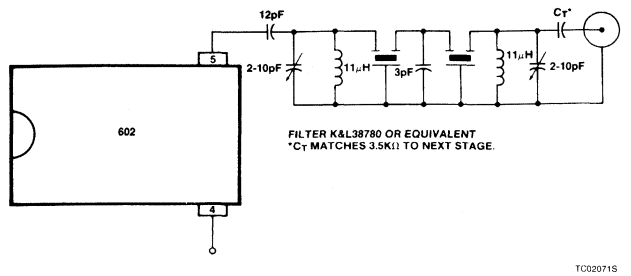
b. Balanced Input (For Attenuation of Second-Order Products)

c. Single-Ended Untuned Input

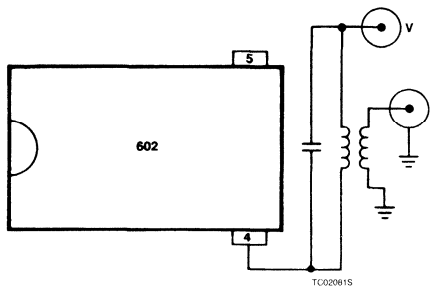
Figure 3. Input Configuration



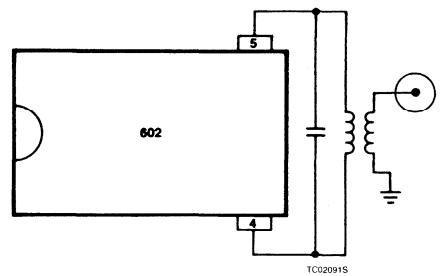
a. Single-Ended Ceramic Filter



b. Single-Ended Crystal Filter

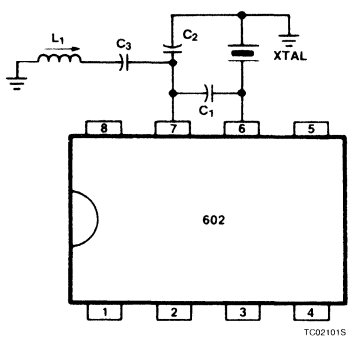


c. Single-Ended IFT

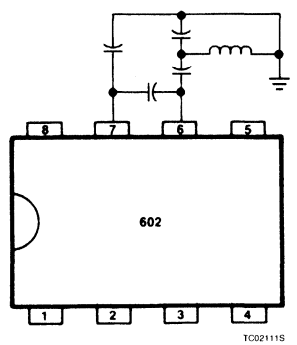


d. Balanced Output

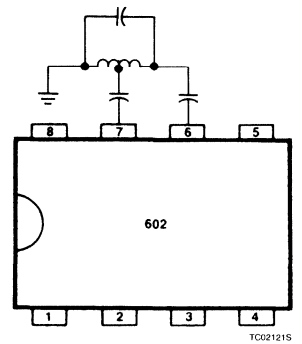
Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)



b. Colpitts L/C Tank Oscillator



c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

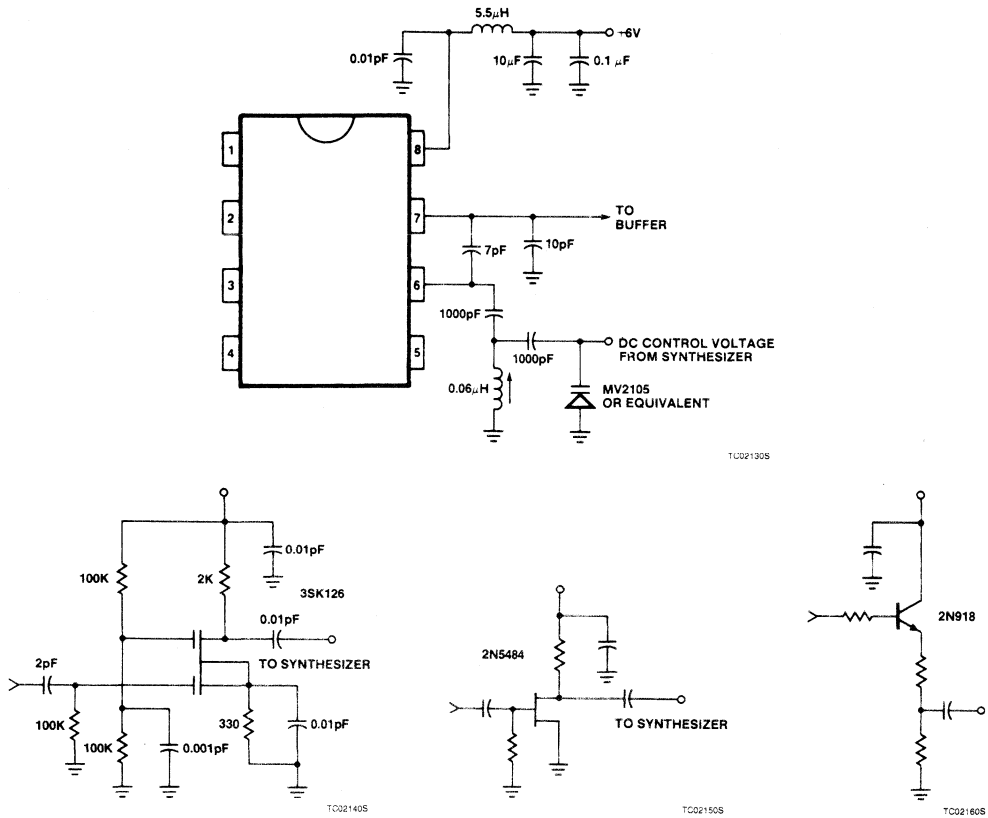


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

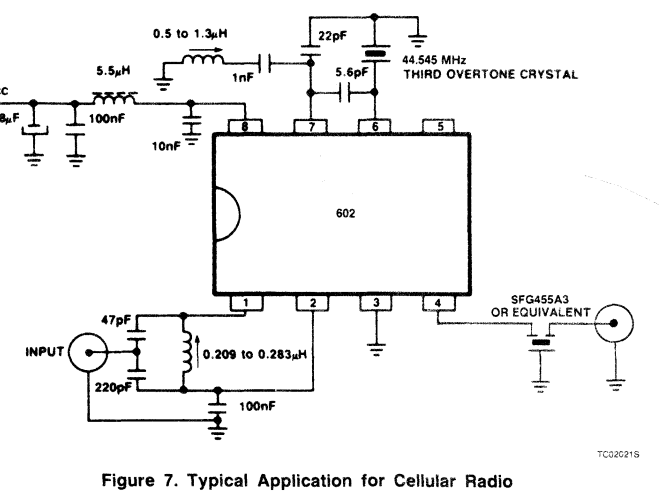


Figure 7. Typical Application for Cellular Radio

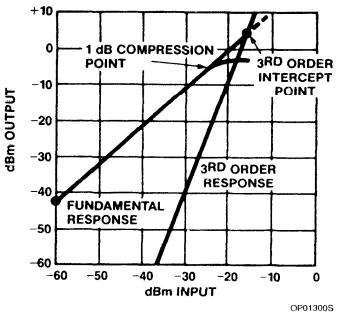


Figure 8. NE/SA602 Third-Order Intermod and 1dB Compression Point Performance

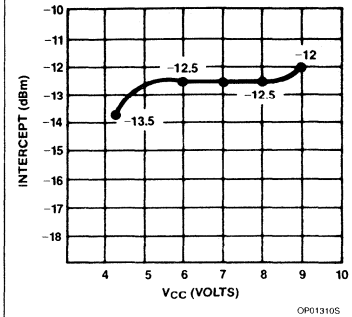


Figure 9. Input Third-Order Intercept Point vs V_{CC}

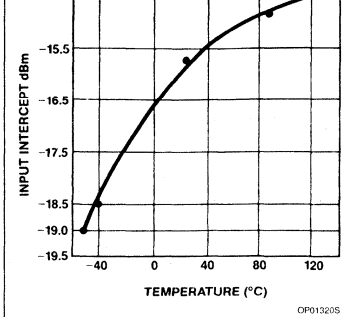


Figure 10. Third-Order Intercept Point vs Temperature

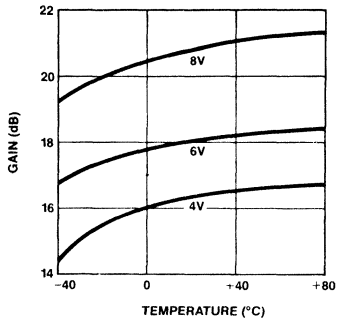


Figure 11

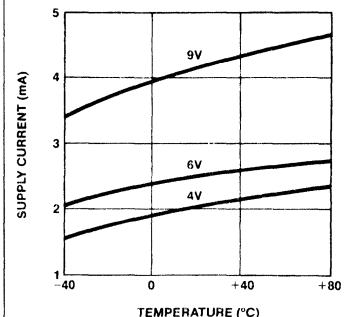


Figure 12

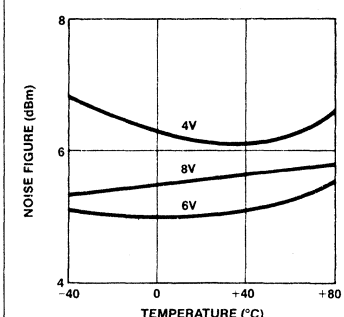


Figure 13

NE612
Double-Balanced Mixer and Oscillator

Product Specification

DESCRIPTION

The NE612 is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 49MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 49MHz is typically below 6dB and makes the device well suited for high performance cordless telephone. The low power consumption makes the NE612 excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE612 is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

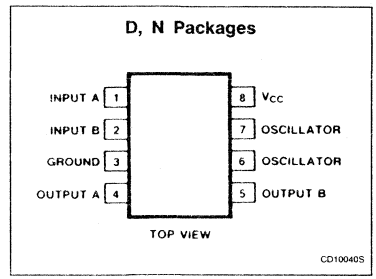
FEATURES

- **Low current consumption**
- **Low cost**
- **Operation to 500MHz**
- **Low radiated energy**
- **Low external parts count; suitable for crystal/ceramic filter**
- **Excellent sensitivity, gain, and noise figure**

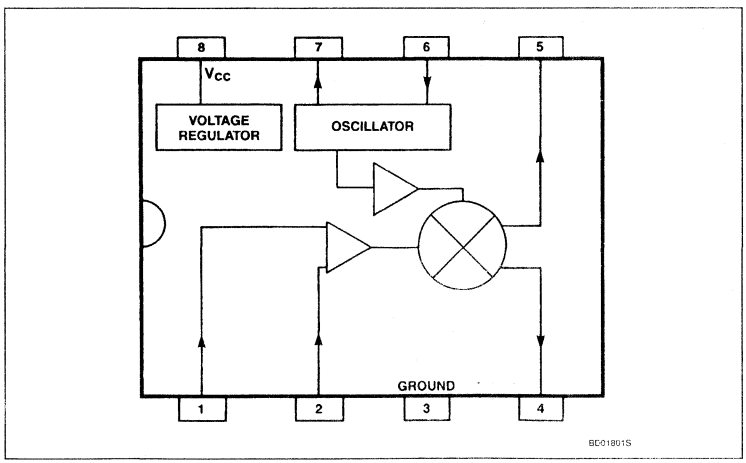
APPLICATIONS

- **Cordless telephone**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **Sonabuoys**
- **Communications receivers**
- **Broadband LANs**
- **HF and VHF frequency conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE612N
8-Pin Plastic SO	0 to +70°C	NE612D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

AC/DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 6V, Figure 1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	3.0	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 49MHz			5.0		dB
	Third-order intercept point at 49MHz	RF_{IN} = −45dBm		−15		dBm
	Conversion gain at 49MHz		14	18		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

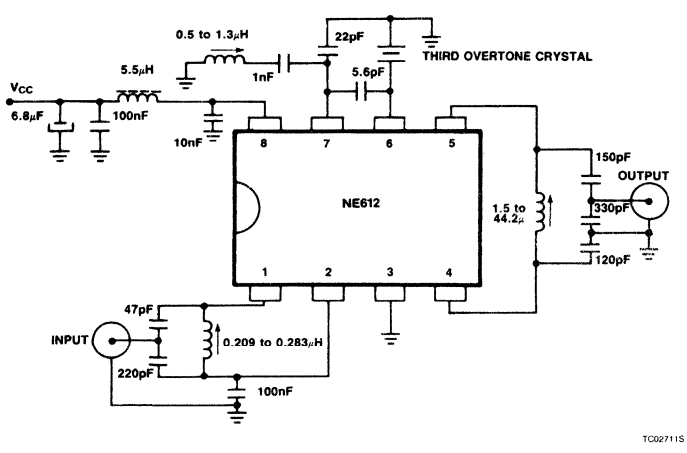


Figure 1. Test Configuration

DESCRIPTION OF OPERATION

The NE612 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE612 is designed for optimum low power performance. When used with the NE614 as a 49MHz cordless telephone system, the NE612 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third-order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE612 should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE612 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k ‖ 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be 200mV$_{P-P}$ minimum to 300mV$_{P-P}$ maximum.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cordless telephones. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

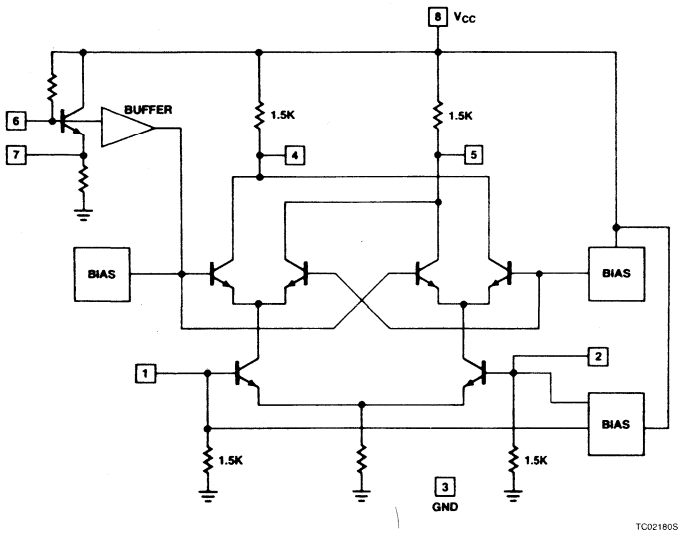
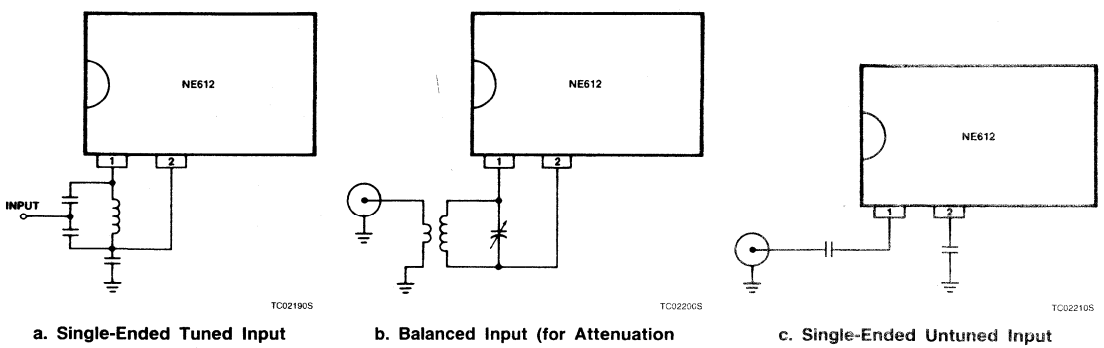


Figure 2. Equivalent Circuit

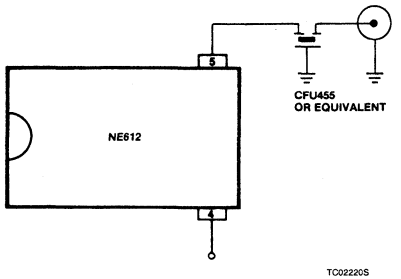


a. Single-Ended Tuned Input

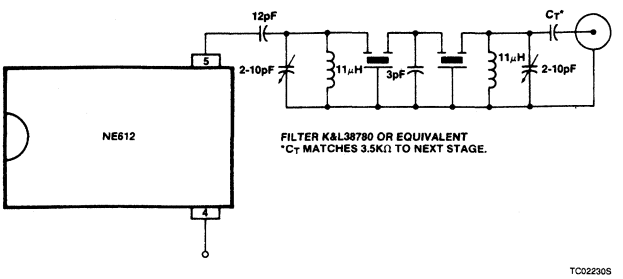
b. Balanced Input (for Attenuation of Second Order Products)

c. Single-Ended Untuned Input

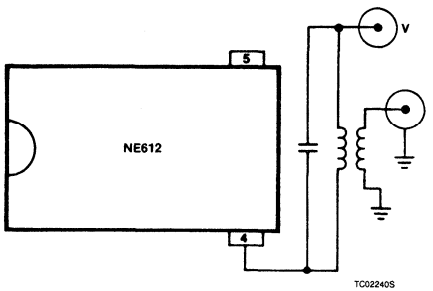
Figure 3. Input Configuration



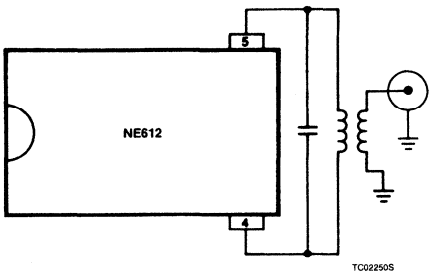
a. Single-Ended Ceramic Filter



b. Single-Ended Crystal Filter

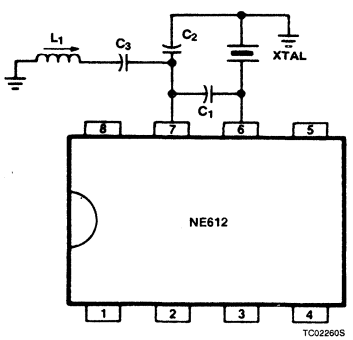


c. Single-Ended IFT

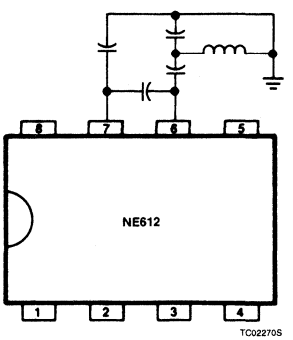


d. Balanced Output

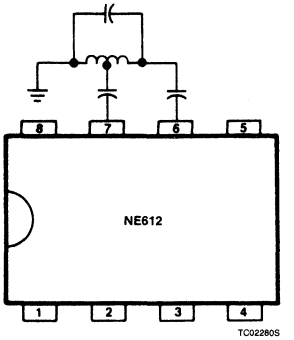
Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)



b. Colpitts L/C Tank Oscillator



c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

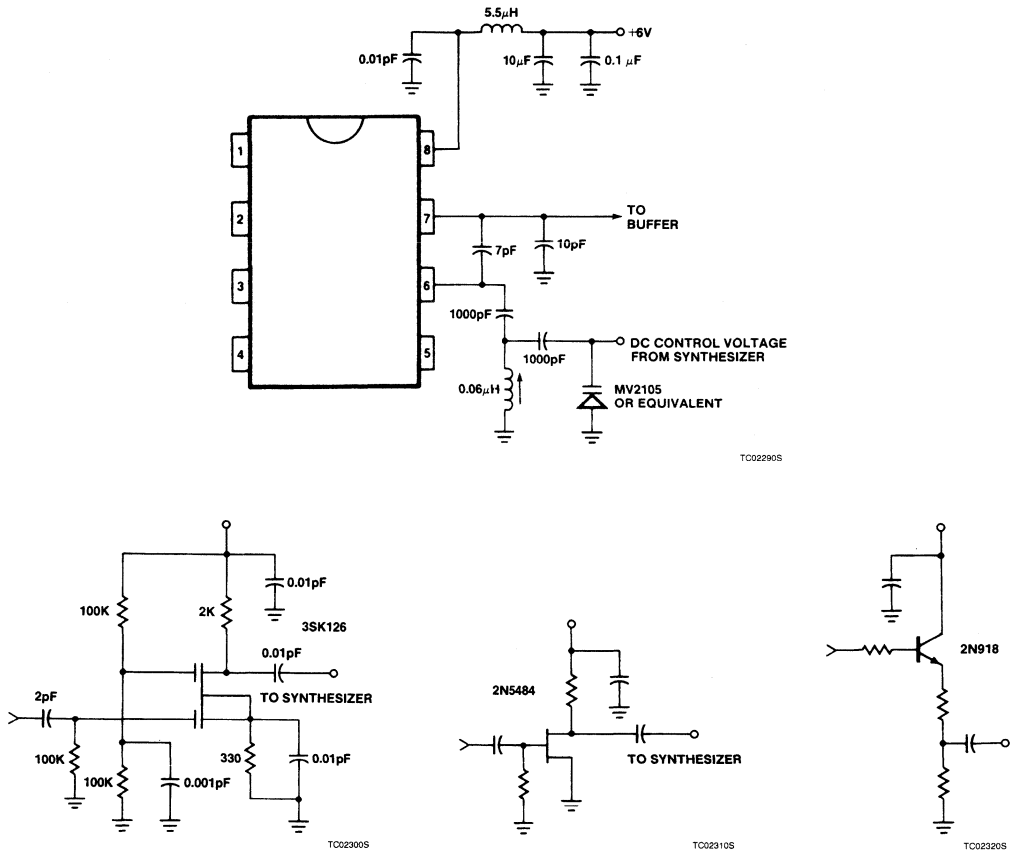


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

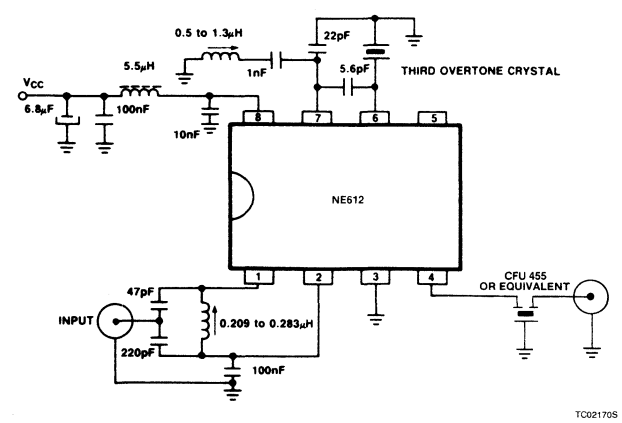


Figure 7. Typical Application for 46/49MHz Cordless Telephone

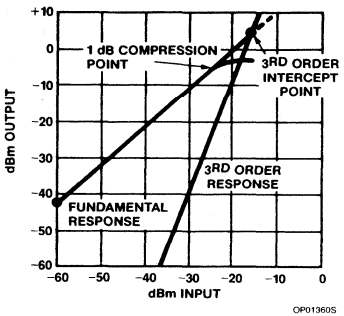


Figure 8. NE612 Third-Order Intermod and 1dB Compression Point Performance

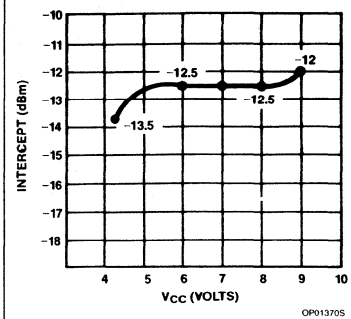


Figure 9. Input Third-Order Intercept Point vs V_{CC}

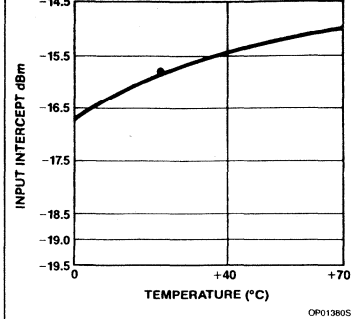


Figure 10. Third-Order Intercept Point vs Temperature

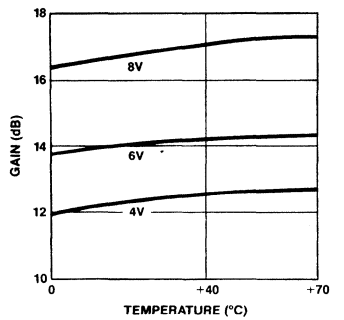


Figure 11

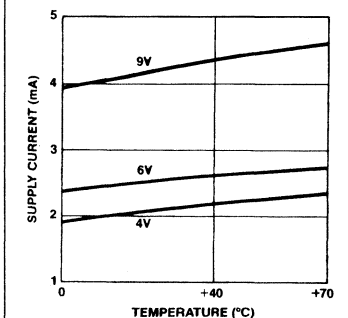


Figure 12

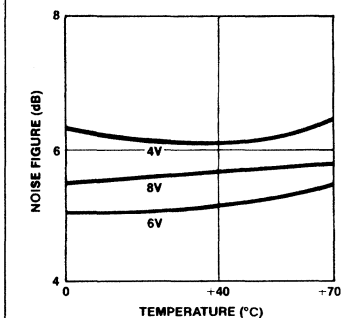


Figure 13

TV VHF MIXER/OSCILLATOR/UHF PREAMPLIFIER

GENERAL DESCRIPTION

The TDA5030A provides VHF local oscillator, VHF mixer and UHF IF preamplifier functions for VHF/UHF television receivers. It includes a buffered output from the VHF local oscillator, a VHF/UHF switching circuit and an IF amplifier stage for an external SAW filter.

Features

- Balanced VHF mixer
- Voltage-controlled VHF local oscillator
- IF amplifier for SAW filter
- UHF IF preamplifier
- Local oscillator buffer output for external prescaler
- Voltage stabilizer
- UHF/VHF switching circuit
- Electrostatic discharge protection diodes at pins 10, 11, 12 and 13

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 15	V_P	10	–	13,2	V
Supply current		I_P	–	42	–	mA
VHF mixer frequency range		f	50	–	470	MHz
Conversion gain			–	24,5	–	dB
Conversion noise	300 MHz		–	10	–	dB
Input signal for 1% cross modulation			–	99	–	dBμV
Storage temperature range		T_{stg}	−55	–	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	–	+ 85	°C

PACKAGE OUTLINE

18-lead DIL, plastic (SOT102).

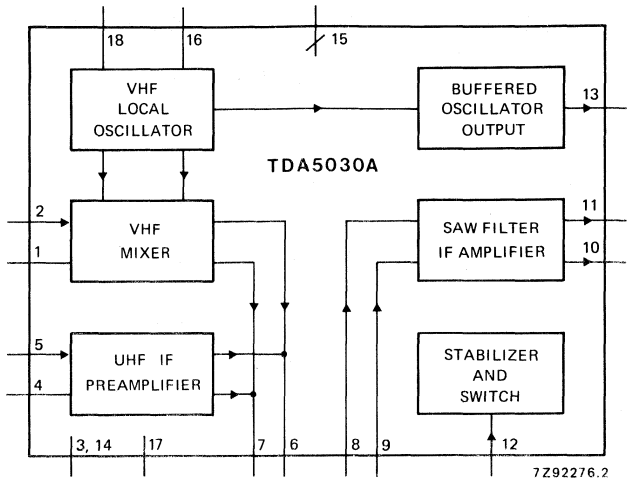


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 15	$V_P = V_{15-3}$	–	14	V
Input voltage	pins 1, 2, 4 and 5	V_i	0	5	V
VHF switching voltage	pin 12	V_{12}	0	$V_{15}+0,3$	V
Output current	pins 10, 11 or 13	$-I_{10, 11, 13}$	–	10	mA
Short-circuit time on outputs	pins 10 and 11	t_{ss}	–	10	s
Storage temperature range		T_{stg}	−55	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 85	°C
Junction temperature range		T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	55 K/W

CHARACTERISTICS

Measured in circuit of Fig. 2, $V_P = V_{15-3} = 12$ V, $T_{amb} = 25$ °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	pin 15	V_{15-3}	10	–	13,2	V
Supply current		I_{15}	–	42	55	mA
Switch voltage level for VHF	pin 12	V_{12}	0	–	2,5	V
Switch voltage level for UHF	pin 12	V_{12}	9,5	–	$V_{15}+0,3$	V
Switch current	UHF selected	I_{12}	–	–	0,7	mA
VHF mixer (including IF amplifier)						
Frequency range		f	50	–	470	MHz
Noise factor	pin 2					
	f = 50 MHz	F	–	7,5	9	dB
	f = 225 MHz	F	–	9	10	dB
	f = 300 MHz	F	–	10	12	dB
	f = 470 MHz	F	–	11	13	dB
Optimum source conductance	pin 2					
	f = 50 MHz	G	–	0,5	–	mS
	f = 225 MHz	G	–	1,1	–	mS
	f = 300 MHz	G	–	1,2	–	mS
Input conductance	pin 2					
	f = 50 MHz	G_i	–	0,23	–	mS
	f = 225 MHz	G_i	–	0,5	–	mS
	f = 300 MHz	G_i	–	0,67	–	mS
Input capacitance	pin 2					
	f = 50 MHz	C_i	–	2,5	–	pF
Input voltage for 1% cross-modulation (in channel)		V_{2-3}	97	99	–	dBμV
Input voltage for 10 kHz pulling (in channel)	f < 300 MHz	V_{2-14}	100	–	–	dBμV
Voltage gain		A_v	22,5	24,5	26,5	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
UHF preamplifier (including IF amplifier)						
Input conductance	pin 5	G_i	–	0,3	–	mS
Input capacitance	pin 5	C_i	–	3,0	–	pF
Noise factor	pin 5	F	–	5	6	dB
Optimum source conductance	pin 5	G	–	3,3	–	mS
Input voltage for 1% cross-modulation (in channel)		$V_{5\text{-}14}$	88	90	–	dBμV
Voltage gain		A_v	31,5	33,5	35,5	dB
VHF mixer						
Conversion transadmittance	pins 2 to 6,7	$Yc_{2\text{-}6,7}$	–	5,7	–	mS
Output impedance	pins 6 and 7	Z_o	–	1,6	–	kΩ
VHF oscillator						
Frequency range		f	70	–	520	MHz
Frequency shift	ΔV_P = 10%; f = 70–330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 15 K; f = 70–330 MHz	Δf	–	–	250	kHz
Frequency drift	between 5 s and 15 min after switch-on	Δf	–	–	200	kHz
SAW filter IF amplifier						
Input impedance	$Z_{10,11}$ = 2 kΩ; f = 36 MHz	$Z_{8,9}$	–	300+ j100	–	Ω
Transimpedance		$Z_{8,9\text{-}10,11}$	–	2,2	–	kΩ
Output reflection coefficient:	f = 36 MHz					
modulus			0,45	0,37	0,41	
phase			–63	–112	–134	deg

parameter	conditions	symbol	min.	typ.	max.	unit
VHF local oscillator output buffer						
Output voltage	pin 13 R_L = 75 Ω					
	f < 100 MHz	V_{13}	14	20	–	mV
	f > 100 MHz	V_{13}	10	20	–	mV
Output impedance	f = 100 MHz	Z_{13}	–	90	–	Ω
RF signal on local oscillator output	R_L = 75 Ω					
	V_i = 1 V; f ≤ 225 MHz	RF/(RF+LO)	–	–	10	dB
	V_i = 0,3 V; f = 225–300 MHz	RF/(RF+LO)	–	–	10	dB
IF signal on local oscillator output	UHF selected; R_L = 75 Ω; V_i = 350 mV	IF/(IF+LO)	–	–	3	mV
Local oscillator harmonics w.r.t. local oscillator output signal	R_L = 75 Ω		–	–	–14	dB

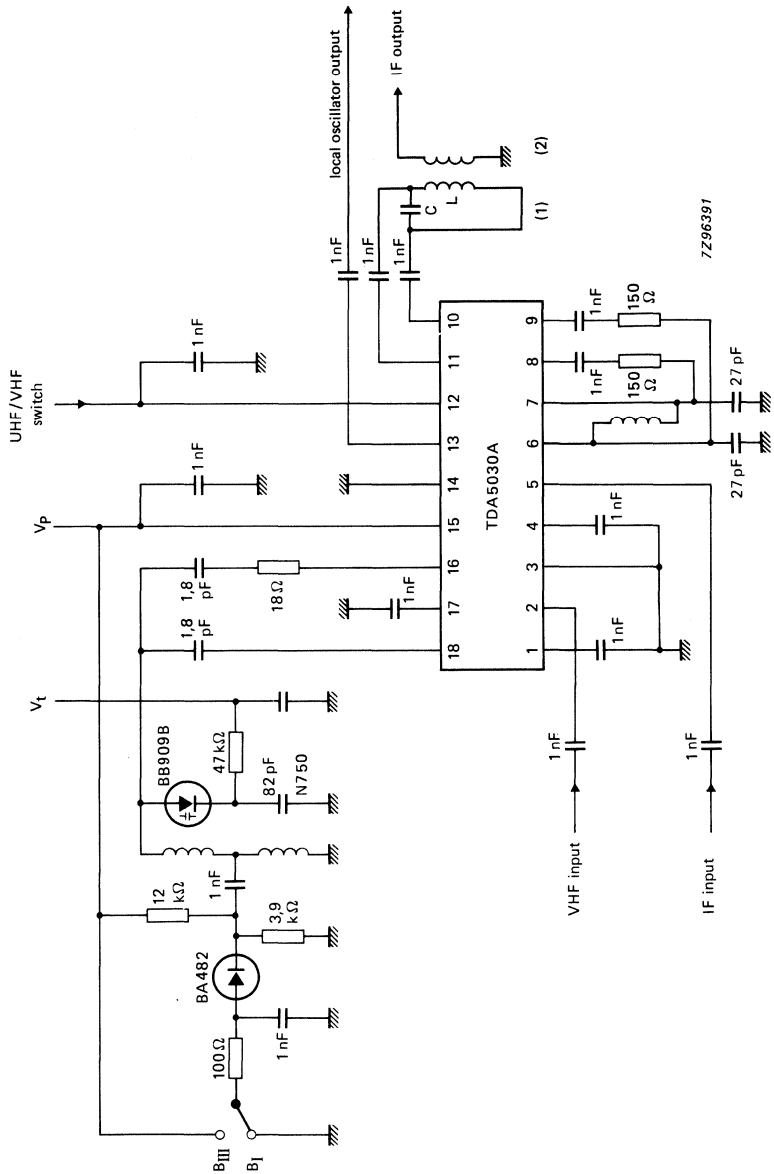


Fig. 2 Test circuit.

(1) C = 18 pF, L = 2,2 μH, f_{CL} = 36,5 MHz.
(2) Turns ratio = 7 : 1, load = 50 Ω.

TV VHF MIXER/OSCILLATOR/UHF PREAMPLIFIER

GENERAL DESCRIPTION

The TDA5030AT provides VHF local oscillator, VHF mixer and UHF IF preamplifier functions for VHF/UHF television receivers. It includes a buffered output from the VHF local oscillator, a VHF/UHF switching circuit and an IF amplifier stage for an external SAW filter.

Features

- Balanced VHF mixer
- Voltage-controlled VHF local oscillator
- IF amplifier for SAW filter
- UHF IF preamplifier
- Local oscillator buffer output for external prescaler
- Voltage stabilizer
- UHF/VHF switching circuit
- Electrostatic discharge protection diodes at pins 11, 12, 13 and 14

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 17)		V_P	10	–	13,2	V
Supply current		I_P	–	42	–	mA
VHF mixer frequency range		f	50	–	470	MHz
Conversion gain			–	25	–	dB
Conversion noise	300 MHz		–	10	–	dB
Input signal for 1% cross modulation			–	99	–	dBμV
Storage temperature range		T_{stg}	–55	–	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	–	+ 80	°C

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).

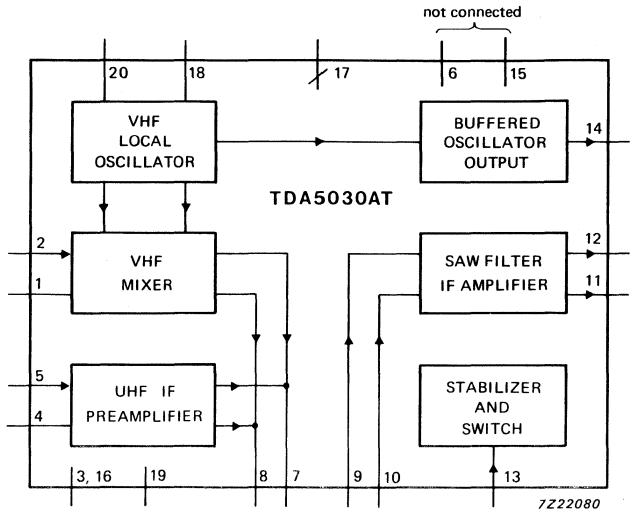


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	$V_P = V_{17-3}$	–	14	V
Input voltage (pins 1, 2, 4 and 5)	V_i	0	5	V
VHF switching voltage (pin 13)	V_{13}	0	V_P+0,3	V
Output current (pins 11, 12 or 14)	$-I_{11,12,14}$	–	10	mA
Short-circuit time on outputs (pins 11, 12 and 14)	t_{sc}	–	10	s
Storage temperature range	T_{stg}	–55	+125	°C
Operating ambient temperature range	T_{amb}	–25	+ 80	°C
Junction temperature range	T_j	–	+150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W

CHARACTERISTICS

$V_P = V_{17-3} = 12$ V; $T_{amb} = 25$ °C; measured in circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 17)		V_{17-3}	10	–	13,2	V
Supply current		I_{17}	–	42	55	mA
Switch voltage level for VHF (pin 13)		V_{13}	0	–	2,5	V
Switch voltage level for UHF (pin 13)		V_{13}	9,5	–	V_P+0,3	V
Switch current	UHF selected	I_{13}	–0,05	–	0,7	mA
VHF mixer (including IF amplifier)						
Frequency range		f	50	–	470	MHz
Noise factor (pin 2)	f = 50 MHz	NF	–	7,5	9	dB
	f = 225 MHz	NF	–	9	10	dB
	f = 300 MHz	NF	–	10	12	dB
	f = 470 MHz	NF	–	11	13	dB
Optimum source conductance (pin 2)	f = 50 MHz	G	–	0,5	–	mS
	f = 225 MHz	G	–	1,1	–	mS
	f = 300 MHz	G	–	1,2	–	mS
	f = 470 MHz	G	–	1,9	–	mS
Input conductance (pin 2)	f = 50 MHz	G_i	–	0,23	–	mS
	f = 225 MHz	G_i	–	0,5	–	mS
	f = 300 MHz	G_i	–	0,67	–	mS
	f = 470 MHz	G_i	–	1,45	–	mS
Input capacitance (pin 2)	f = 50 MHz	C_i	–	2,5	–	pF
Input voltage for 1% cross-modulation (in channel)		V_{2-3}	96	99	–	dBμV
Input voltage for 10 kHz pulling (in channel)	f < 300 MHz	V_{2-16}	100	–	–	dBμV
Input voltage for 100 kHz pulling	f = 470 MHz	V_{2-3}	73	–	–	dBμV
Voltage gain		A_v	23	25	27	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
UHF preamplifier (including IF amplifier)						
Input conductance (pin 5)		G_i	–	0,3	–	mS
Input capacitance (pin 5)		C_i	–	3,0	–	pF
Noise factor (pin 5)		NF	–	5	6	dB
Optimum source conductance (pin 5)		G	–	3,3	–	mS
Input voltage for 1% cross-modulation (in channel)		V_{5-16}	88	90	–	dBμV
Voltage gain		A_v	32	34	36	dB
VHF mixer						
Conversion transadmittance (pins 2 to 7, 8)		$Yc_{2-7,8}$	–	5,7	–	mS
Output impedance (pins 7 and 8)		Z_o	–	1,6	–	kΩ
VHF oscillator						
Frequency range		f	70	–	520	MHz
Frequency shift	ΔV_P = 10%; f = 70 to 330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 15 K; f = 70 to 330 MHz	Δf	–	–	250	kHz
Frequency drift	between 5 s and 15 min after switch-on	Δf	–	–	200	kHz
SAW filter IF amplifier						
Input impedance	$Z_{11,12}$ = 2 kΩ; f = 36 MHz	$Z_{9,10}$	–	300+ j100	–	Ω
Transimpedance		$Z_{9,10-11,12}$	–	2,2	–	kΩ
Output reflection coefficient:	f = 36 MHz					
modulus			0,45	0,37	0,41	
phase			–63	–112	–134	deg

parameter	conditions	symbol	min.	typ.	max.	unit
VHF local oscillator output buffer						
Output voltage (pin 14)	R_L = 75 Ω					
	f < 100 MHz	V_{14}	14	20	–	mV
	f > 100 MHz	V_{14}	10	20	–	mV
Output impedance	f = 100 MHz	Z_{14}	–	90	–	Ω
RF signal on local oscillator output	R_L = 75 Ω					
	V_i = 1 V; f ⩽ 225 MHz	RF/(RF+LO)	–	–	10	dB
	V_i = 0,3 V; f = 225–300 MHz	RF/(RF+LO)	–	–	10	dB
IF signal on local oscillator output	UHF selected; R_L = 75 Ω; V_i = 350 mV	IF/(IF+LO)	–	–	3	mV
Local oscillator harmonics w.r.t. local oscillator output signal	R_L = 75 Ω		–	–	−14	dB

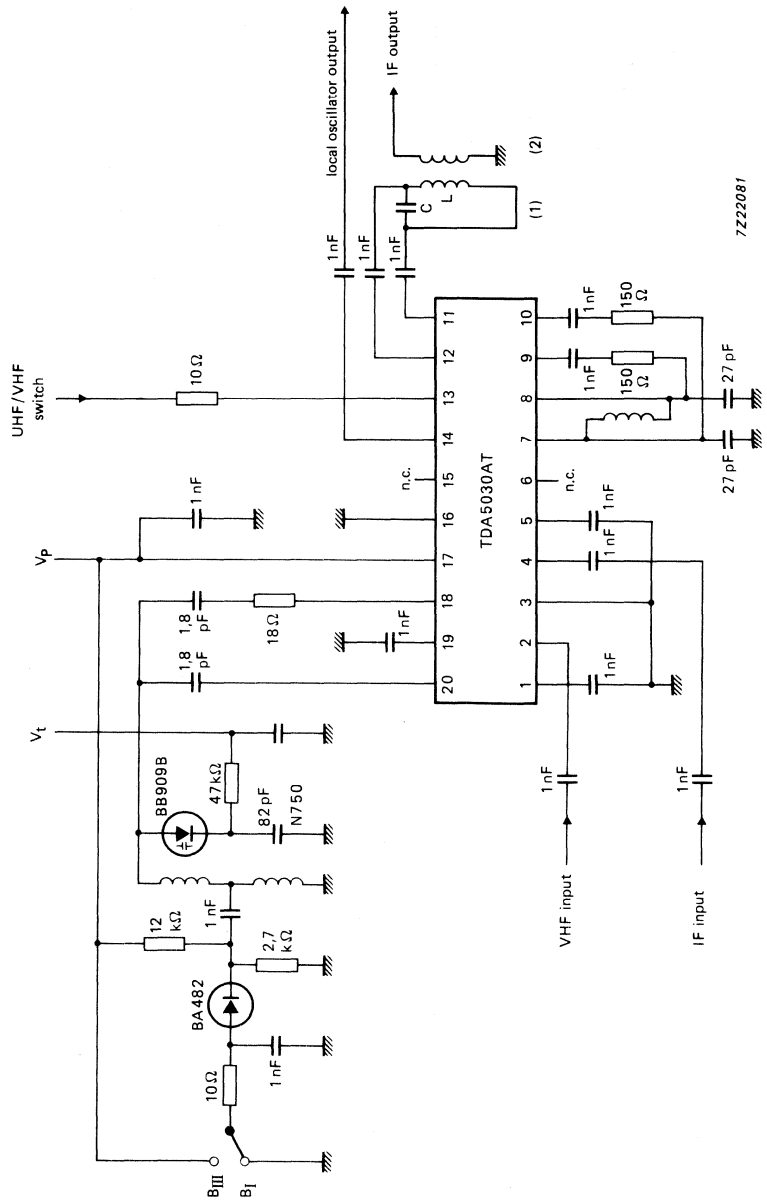


Fig. 2 Test circuit.

(1) C = 18 pF, L = 2,2 μH, f_{CL} = 36,5 MHz.
(2) Turns ratio = 7 : 1, load = 50 Ω.

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Balanced Modulator/ Demodulator Applications Using the MC1496/MC1596

Application Note

BALANCED MODULATOR/ DEMODULATOR APPLICATIONS USING MC1496/MC1596

The MC1496 is a monolithic transistor array arranged as a balanced modulator-demodulator. The device takes advantage of the excellent matching qualities of monolithic devices to provide superior carrier and signal rejection. Carrier suppressions of 50dB at 10MHz are typical with no external balancing networks required.

Applications include AM and suppressed carrier modulators, AM and FM demodulators, and phase detectors.

THEORY OF OPERATION

As Figure 1 suggests, the topography includes three differential amplifiers. Internal connections are made such that the output becomes a product of the two input signals V_C and V_S.

To accomplish this the differential pairs Q1 – Q2 and Q3 – Q4, with their cross-coupled collectors, are driven into saturation by the zero crossings of the carrier signal V_C. With a low level signal, V_S driving the third differential amplifier Q5 – Q6, the output voltage will be full wave multiplication of V_C and V_S. Thus for sine wave signals, V_{OUT} becomes:

$$V_{OUT} = E_x E_y \left[\cos(\omega x + \omega y)t + \cos(\omega x - \omega y)t\right] \quad (1)$$

As seen by equation (1) the output voltage will contain the sum and difference frequencies of the two original signals. In addition, with the carrier input ports being driven into saturation, the output will contain the odd harmonics of the carrier signals. (See Figure 4.)

BIASING

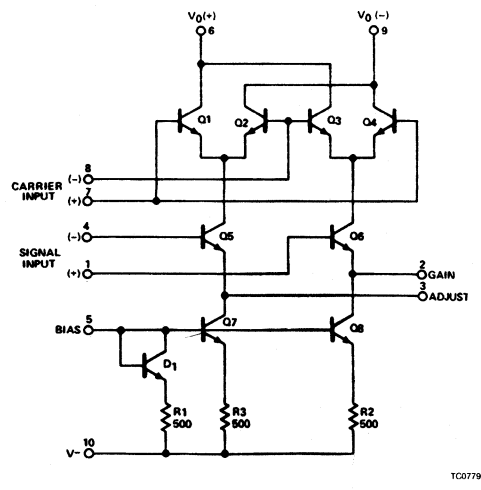
Since the MC1496 was intended for a multitude of different functions as well as a myriad of supply voltages, the biasing techniques are specified by the individual application. This allows the user complete freedom to choose gain, current levels, and power supplies. The device can be operated with single-ended or dual supplies.

Internally provided with the device are two current sources driven by a temperature-compensated bias network. Since the transistor geometries are the same and since V_{BE} matching in monolithic devices is excellent, the currents through Q_7 and Q_8 will be identical to the current set at Pin 5. Figures 2 and 3 illustrate typical biasing arrangements from split and single-ended supplies, respectively.

Of primary interest in beginning the bias circuitry design is relating available power supplies and desired output voltages to device requirements with a minimum of external components.

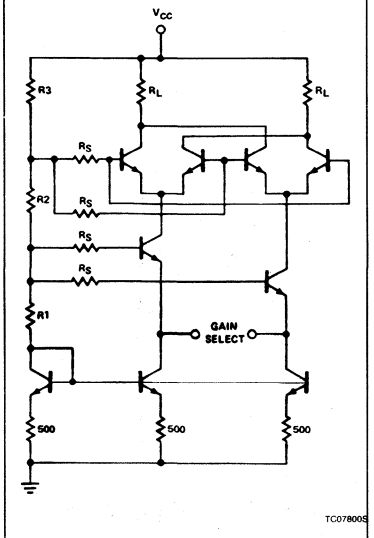
The transistors are connected in a cascode fashion. Therefore, sufficient collector voltage must be supplied to avoid saturation if linear operation is to be achieved. Voltages greater than 2V are sufficient in most applications.

Biasing is achieved with simple resistor divider networks as shown in Figure 3. This configuration assumes the presence of symmetrical supplies. Explaining the DC biasing technique is probably best accomplished by



NOTE:
All resistor values are in ohms

Figure 1. Balanced Modulator Schematic



NOTE:
All resistor values are in ohms

Figure 2. Single-Supply Biasing

Balanced Modulator/Demodulator Applications Using the MC1496/MC1596

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an example. Thus, the initial assumptions and criteria are set forth:

1. Output swing greater than $4V_{P-P}$.
2. Positive and negative supplies of 6V are available.
3. Collector current is 2mA. It should be noted here that the collector output current is equal to the current set in the current sources.

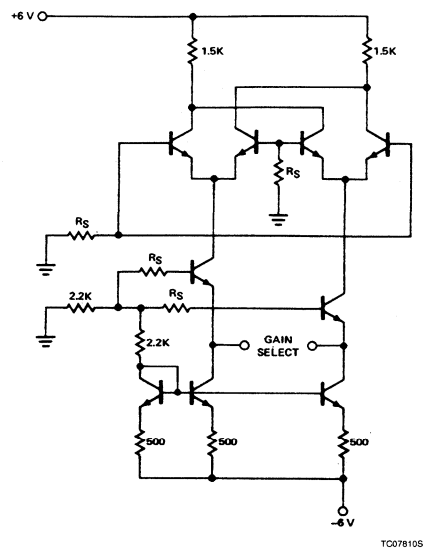
As a matter of convenience, the carrier signal ports are referenced to ground. If desired, the modulation signal ports could be ground referenced with slight changes in the bias arrangement. With the carrier inputs at DC ground, the quiescent operating point of the outputs should be at one-half the total positive voltage or 3V for this case. Thus, a collector load resistor is selected which drops 3V at 2mA or 1.5kΩ. A quick check at this point reveals that with these loads and current levels the peak-to-peak output swing will be greater than 4V. It remains to set the current source level and proper biasing of the signal ports.

The voltage at Pin 5 is expressed by

$$V_{BIAS} = V_{BE} = 500 \times I_S$$

where I_S is the current set in the current sources.

For the example V_{BE} is 700mV at room temperature and the bias voltage at Pin 5 becomes 1.7V. Because of the cascode configuration, both the collectors of the current sources and the collectors of the signal transistors must have some voltage to operate properly. Hence, the remaining voltage of the negative supply (−6V + 1.7V = −4.3V) is split between these transistors by biasing the signal transistor bases at −2.15V.



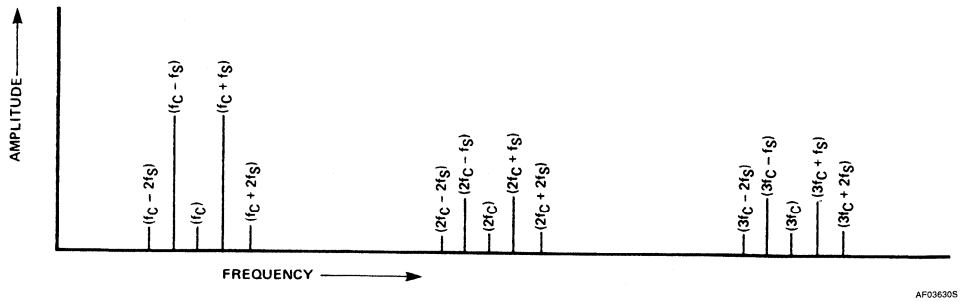
NOTE:
All resistor values are in ohms

Figure 3. Dual Supply Biasing

Countless other bias arrangements can be used with other power supply voltages. The important thing to remember is that sufficient DC voltage is applied to each bias point to avoid collector saturation over the expected signal wings.

BALANCED MODULATOR

In the primary application of balanced modulation, generation of double sideband suppressed carrier modulation is accomplished. Due to the balance of both modulation and carrier inputs, the output, as mentioned, contains the sum and difference frequencies while attenuating the fundamentals. Upper and lower sideband signals are the strongest signals present with harmonic sidebands being of diminishing amplitudes as characterized by Figure 4.



NOTES:
f_C Carrier Fundemental
f_S Modulating Signal
$f_C \pm f_S$ Fundemental Carrier Sidebands
$f_C \pm nf_S$ Fundemental Carrier Sideband Harmonics
nf_C Carrier Harmonics
$nf_C \pm nf_S$ Carrier Harmonic Sidebands

Figure 4. Modulator Frequency Spectrum

Balanced Modulator/Demodulator Applications Using the MC1496/MC1596

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Gain of the 1496 is set by including emitter degeneration resistance located as R_E in Figure 5. Degeneration also allows the maximum signal level of the modulation to be increased. In general, linear response defines the maximum input signal as

$$Vs \leq 15 \cdot R_E(Peak)$$

and the gain is given by

$$A_{VS} = \frac{R_L}{R_E + 2r_e} \qquad (2)$$

This approximation is good for high levels of carrier signals. Table 1 summarizes the gain for different carrier signals.

As seen from Table 1, the output spectrum suffers an amplitude increase of undesired sideband signals when either the modulation or carrier signals are high. Indeed, the modulation level can be increased if R_E is increased without significant consequence. However, large carrier signals cause odd harmonic sidebands (Figure 4) to increase. At the same time, due to imperfections of the carrier waveforms and small imbalances of the device, the second harmonic rejection will be seriously degraded. Output filtering is often used with high carrier levels to remove all but the desired sideband. The filter removes unwanted signals while the high carrier level guards against amplitude variations and maximizes gain. Broadband modulators, without benefit of filters, are implemented using low carrier and modulation signals to maximize linearity and minimize spurious sidebands.

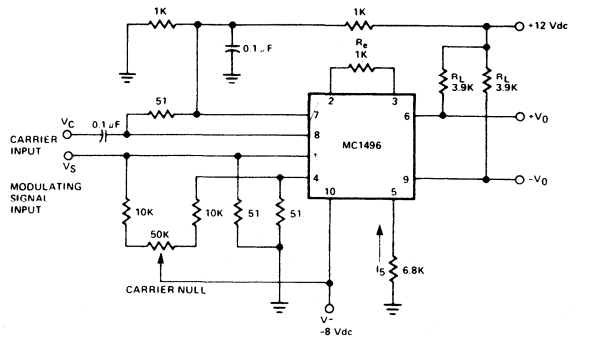
AM MODULATOR

The basic current of Figure 5 allows no carrier to be present in the output. By adding offset to the carrier differential pairs, controlled amounts of carrier appear at the output whose amplitude becomes a function of the modulation signal or AM modulation. As shown, the carrier null circuit is changed from Figure 5 to have a wider range so that wider control is achieved. All connections are shown in Figure 6.

AM DEMODULATION

As pointed out in Equation 1, the output of the balanced mixer is a cosine function of the angle between signal and carrier inputs. Further, if the carrier input is driven hard enough to provide a switching action, the output becomes a function of the input amplitude. Thus the output amplitude is maximum when there is 0° phase difference as shown in Figure 7.

Amplifying and limiting of the AM carrier is accomplished by IF gain block providing 55dB

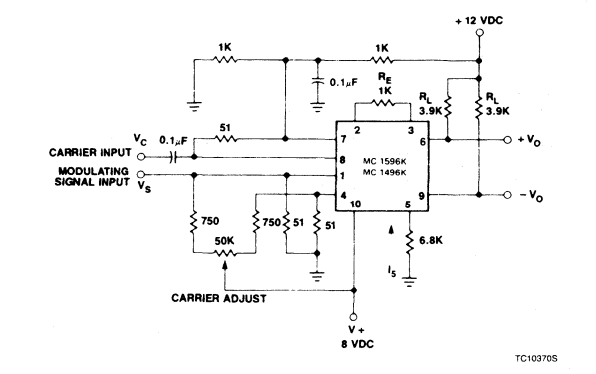


NOTE:
All resistor values are in ohms

Figure 5. Double Sideband Suppressed Carrier Modulator

Table 1. Voltage Gain and Output Spectrum vs Input Signal

CARRIER INPUT SIGNAL (V_C)	APPROXIMATE VOLTAGE GAIN	OUTPUT SIGNAL FREQUENCY(S)
Low-level DC	$\frac{R_L V_C}{2(R_E + 2r_E)\left(\frac{KT}{q}\right)}$	f_M
High-level DC	$\frac{R_L}{R + 2r_e}$	f_M
Low-level AC	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level AC	$\frac{0.637R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$...

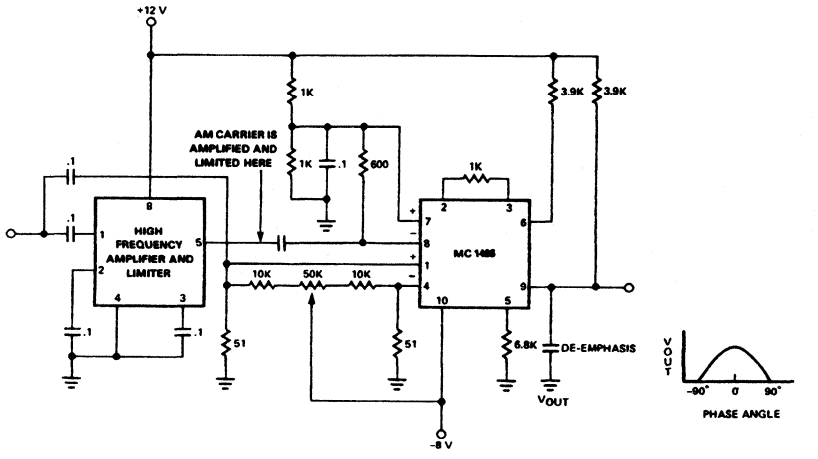


NOTE:
All resistor values are in ohms

Figure 6. AM Modulator

Balanced Modulator/Demodulator Applications Using the MC1496/MC1596

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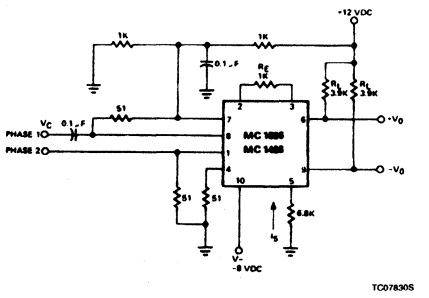


NOTE:
All resistor values are in ohms

Figure 7. AM Demodulator

of gain or higher with limiting of 400μV. The limited carrier is then applied to the detector at the carrier ports to provide the desired switching function. The signal is then demodulated by the synchronous AM demodulator (1496) where the carrier frequency is attenuated due to the balanced nature of the device. Care must be taken not to overdrive the signal input so that distortion does not appear in the recovered audio. Maximum conversion gain is reached when the carrier signals are in phase as indicated by the phase-gain relationship drawn in Figure 7.

Output filtering will also be necessary to remove high frequency sum components of the carrier from the audio signal.



NOTE:
All resistor values are in ohms

Figure 8. Phase Comparator

PHASE DETECTOR

The versatility of the balanced modulator or multiplier also allows the device to be used as a phase detector. As mentioned, the output of the detector contains a term related to the cosine of the phase angle. Two signals of equal frequency are applied to the inputs as per Figure 8. The frequencies are multiplied together producing the sum and difference frequencies. Equal frequencies cause the difference component to become DC while the undesired sum component is filtered out. The DC component is related to the phase angle by the graph of Figure 9. At 90° the cosine becomes zero, while being at maximum positive or maximum negative at 0° and 180°, respectively.

The advantage of using the balanced modulator over other types of phase comparators is the excellent linearity of conversion. This configuration also provides a conversion gain rather than a loss for greater resolution. Used in conjunction with a phase-locked loop, for instance, the balanced modulator provides a very low distortion FM demodulator.

FREQUENCY DOUBLER

Very similar to the phase detector of Figure 8, a frequency doubler schematic is shown in Figure 10. Departure from Figure 8 is primarily the removal of the low-pass filter. The output then contains the sum component which is twice the frequency of the input, since both input signals are the same frequency.

Balanced Modulator/Demodulator Applications Using the MC1496/MC1596

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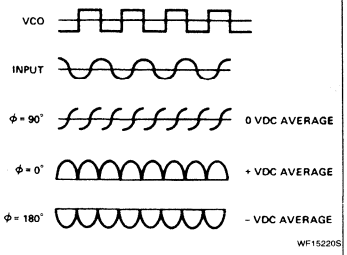
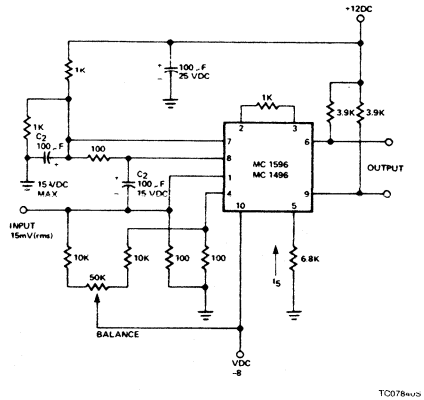


Figure 9. Phase Detector ± Voltages



NOTE:
All resistor values are in ohms

Figure 10. Low Frequency Doubler

AN1981
New Low Power Single Sideband Circuits

Application Note

INTRODUCTION

Several new integrated circuits now permit RF designers to resurrect old techniques of single-sideband generation and detection. The high cost of multi-pole crystal filters limits the use of the SSB mode to the most demanding applications, yet the advantages of SSB over full-carrier AM and FM are well-documented (Ref 1 & 2). The use of multi-pole filters can now be circumvented by reviving some older techniques without sacrificing performance. This has been made possible by the availability of some new RF and digital integrated circuits.

DESCRIPTION

Figure 1 shows the frequency spectrum of a 10MHz full-carrier double-sideband AM signal using a 1kHz modulating tone. This well-known type of signal is used by standard AM broadcast radio stations. Full-carrier AM's advantage is that envelope detection can be used in the receiver. Envelope detection is a simple and economical technique because it simplifies receiver circuitry. Figure 2 shows the time domain "envelope" of the same AM signal.

The 1kHz tone example of Figures 1 and 2 serves as a simple illustration of an AM signal. Typically, the sidebands contain complex waveforms for voice or data communications. In the full-carrier double sideband mode (AM), all the modulation information is contained in both sidebands, while the carrier "rides along" without contributing to the transfer of intelligence. Only one sideband without the carrier is needed to effectively transmit the modulation information. This mode is called "single-sideband suppressed carrier". Because of its reduced bandwidth, it has the advantages of improved spectrum utilization, better signal-to-noise ratios at low signal levels, and improved transmitter efficiency when compared with either FM or full-carrier AM. A finite frequency allocation using SSB can support three times the number of channels when compared with comparable FM or AM full-carrier systems.

There are three basic methods of single-sideband generation. All three use a balanced modulator to produce a double-sideband suppressed carrier signal. The undesired sideband is then removed by phase and amplitude nulling (the phasing method), high Q multi-pole filters (the filter method), or a

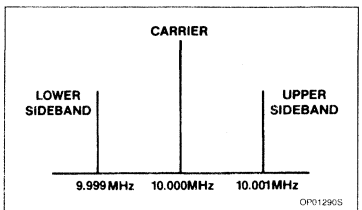


Figure 1. Frequency Domain Display of a 10MHz Carrier AM Modulated by a 1kHz Tone (Spectrum Analyzer Display)

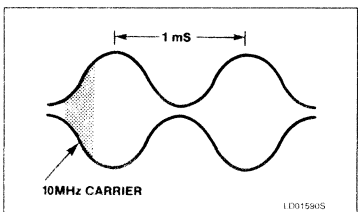


Figure 2. Time Domain Display of the Same Signal Shown in Figure 1. (Oscilloscope Display)

"third" method which is a derivation of the phasing technique called here the "Weaver" method for the apparent inventor. The reciprocal of the generator functions is employed to produce sideband detectors. Generators start with audio and produce the SSB signal; detectors receive the SSB signal and reproduce the audio. Since the sideband signal is typically produced at radio frequencies, it can be amplified and applied to an antenna or used as a subcarrier.

Reproduction of the audio signal in a full-carrier AM receiver is simplified because the carrier is present. The signal envelope, which contains the carrier and the sidebands, is applied to a non-linear device (typically a diode). The effect of envelope detection is to multiply the sideband signal by the carrier; this results in the recovery of the audio waveform. The mathematical basis for this process can be understood by studying trigonometric identities.

Since the carrier is not present in the received SSB signal, the receiver must provide it for proper audio detection. This signal from the local oscillator (LO) is applied to a mixer (multiplier) together with the SSB signal and detection occurs. This technique is called product detection and is necessary in all SSB methods. A major problem in SSB receivers is the ability to maintain accurate LO frequencies to prevent spectral shifting of the audio signal. Errors in this frequency will result in a "Donald Duck" sound which can render the signal unintelligible for large frequency errors.

Theory of Single-Sideband Detection

Figures 3 through 8 illustrate the three methods of SSB generation and detection. Since they are reciprocal operations, the circuitry for generation and detection is similar with all three methods. Duplication of critical circuitry is easy to accomplish in transceiver applications by using appropriate switching circuits.

Figures 3 and 4 show the generation and detection techniques employed in the filter method. In the generator a double sideband signal is produced while the carrier is eliminated with the balanced modulator. Then the undesired sideband is removed with a high Q crystal bandpass filter. A transmit mixer is usually employed to convert the SSB signal to the desired output frequency. The detection scheme is the reciprocal. A receive mixer is used to convert the selected input frequency to the IF frequency, where the filter removes the undesired SSB response. Then the signal is demodulated in the product detector. A major drawback to the filter method is the fact that the filter is fixed-tuned to one frequency. This necessitates the receive and transmit mixers for multi-frequency operation.

Figures 5 and 6 show block diagrams of a generator and demodulator which use the phase method. Figure 6 also includes a mathematical model. The input signal (Cos(Xt)) is fed in-phase to two RF mixers where "X" is the frequency of the input signal. The other inputs to the mixers are fed from a local oscillator (LO) in quadrature (Cos(Yt) and Sin(Yt)), where "Y" is the frequency of the LO signal. By differentiating the output of one of the mixers and then summing with the other, a single sideband response is obtained. Switching the mixer output that is differentiated will change the selected sideband, upper (USB) or lower (LSB). In most cases the mixer outputs will be the audio passband (300 to 3000Hz). Differentiating the passband involves a 90 degree phase shift over more than three octaves. This is the most difficult aspect of using the phasing method for voice band SSB.

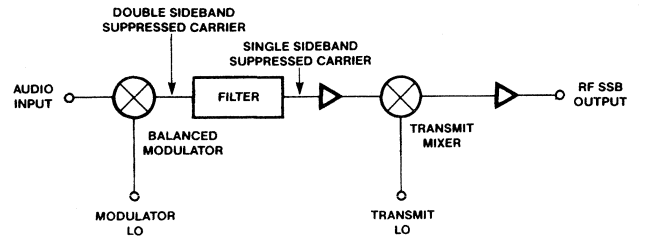


Figure 3. Filter Method SSB Generator

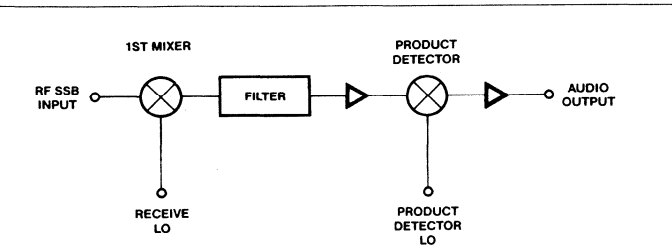


Figure 4. Filter Method SSB Detector

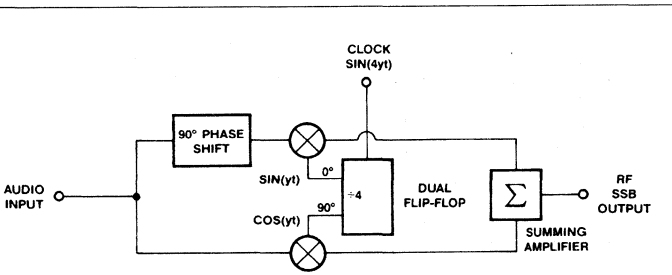


Figure 5. Phasing Method Generator

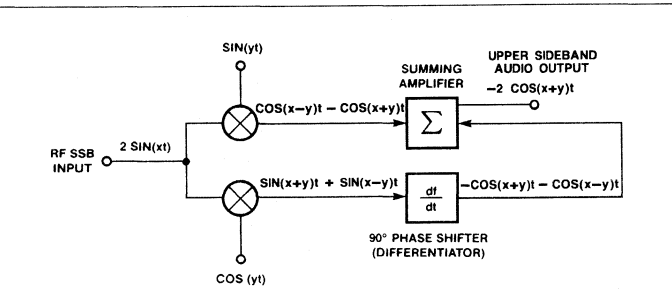


Figure 6. Phasing Method Detector with Simplified Mathematical Model

For voice systems, difficulty of maintaining accurate broadband phase shift is eliminated by the technique used in Figures 7 and 8. The "Weaver" method is similar to the phasing method because both require two quadrature steps in the signal chain. The difference between the two methods is that the Weaver method uses a low frequency (1.8kHz) subcarrier in quadrature rather than the broadband 90 degree audio phase shift. The desired sideband is thus "folded over" the 1.8kHz subcarrier and its energy appears between 0 and 1.5kHz. The undesired sideband appears 600Hz farther away between 2.1 and 4.8kHz. Consequently, sideband rejection is determined by a low-pass filter rather than by phase and amplitude balance. A very steep low-pass response in the Weaver method is easier to achieve than the very accurate phase and amplitude balance needed in the phasing method. Therefore, better sideband rejection is possible with the Weaver method than with the phasing method.

Quadrature Dual Mixer Circuits

One of the two critical stages in the phasing method and both critical stages in the Weaver method require quadrature dual mixer circuits. Figures 9 and 10 show two methods of obtaining quadrature LO signals for dual mixer applications. Other methods exist for producing quadrature LO signals, particularly use of passive LC circuits. LC circuits will not maintain a quadrature phase relationship when the operating frequency is changed. The two illustrated circuits are inherently broad-banded; therefore, they are far more flexible and do not require adjustment. These circuits are very useful for SSB circuits, but also can be applied to FSK, PSK, and QPSK digital communications systems.

The NE602 is a low power, sensitive, active, double-balanced mixer which shows excellent phase characteristics up to 200MHz. This makes it an ideal candidate for this and many other applications.

The circuit in Figure 9 uses a divide-by-four dual flip-flop that generates all four quadratures. Most of the popular dual flip-flops can be used in different situations. The HEF4013 CMOS device uses very little power and can maintain excellent phase integrity at clock rates up to several megahertz. Consequently, the HEF4013 can be used with the ubiquitous 455kHz intermediate frequency with excellent power economy. For higher clock rates (up to 120MHz for up to 30MHz operation), the fast TTL 74F74 is a good choice. It has been tested to 30MHz operating frequencies with good results (> 30 dB SSB rejection). At lower frequencies (5MHz) sideband rejection increases to nearly 40dB with the circuits shown. The ultimate low frequency rejection is mainly a function of the audio phase shifter.

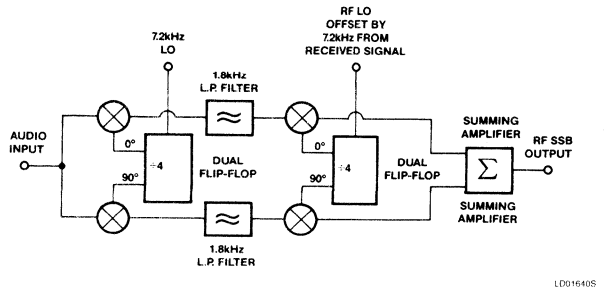


Figure 7. Weaver Method Generator

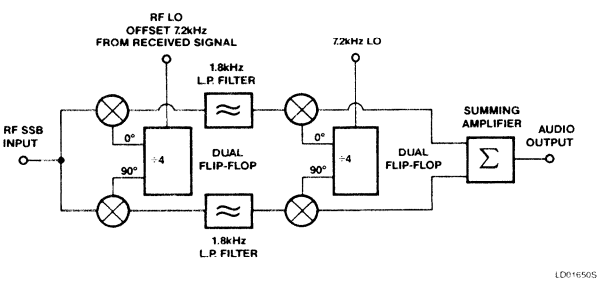


Figure 8. Weaver Method Detector

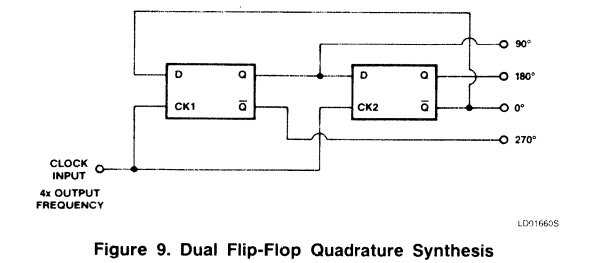


Figure 9. Dual Flip-Flop Quadrature Synthesis

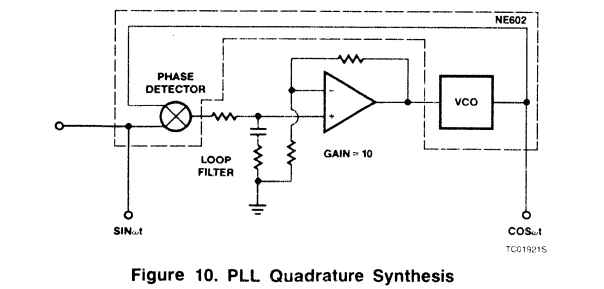


Figure 10. PLL Quadrature Synthesis

Better performance is possible by employing higher tolerance resistors and capacitors.

The circuit in Figure 10 shows another technique for producing a broadband quadrature phase shift for the LO. The advantage of this circuit over the flip-flops is that the clock frequency is identical to the operating frequency; however, phase accuracy is more difficult to achieve. A PLL will maintain a quadrature phase relationship when the loop is closed and the VCO voltage is zero. The DC amplifier will help the accuracy of the quadrature condition by presenting gain to the VCO control circuit. The other problem that can arise is that PLL circuits tend to be noisy. Sideband noise is troublesome in both SSB and FM systems, but SSB is less sensitive to phase noise problems in the LO.

Figure 11 shows a circuit that is effective for driving the 74F74, or other TTL gates, with a signal generator or analog LO. The NE5205 provides about 20dB gain with 50Ω input and output impedances from DC to 450MHz. Minimum external components are required. The 1kΩ resistor is about optimum for "pulling" the input voltage down near the logic threshold. A 50Ω output level of 0dBm can be used to drive the NE5205 and 74F74 to 100MHz. Two NE5205s can be cascaded for even more sensitivity while maintaining extremely wide bandwidth. An advantage of using digital sources for the LO is that low-frequency power supply ripple will not cause hum in the receiver front end. This is a common problem in direct conversion designs.

Figure 12 shows the interface circuitry between the 74F74 and the NE602 LO ports. The total resistance reflects conservative current drain from the 74F74 outputs, while the tap on the voltage divider is optimized for proper NE602 operation. The low signal source impedance further helps maintain phase accuracy, and the isolation capacitor is miniature ceramic for DC isolation.

Audio Amplifiers and Switching

Using active mixers (NE602) in these types of circuits gives conversion gain, typically 18dB. More traditional applications use passive diode ring mixers which yield conversion loss, typically 7dB. Consequently, the detected audio level will be about 25dB higher when using the NE602. This fact can greatly reduce the first audio stage noise and gain requirements and virtually eliminate the "microphonic" effect common to direct conversion receivers. Traditional direct conversion receivers use passive audio LC filters at the mixer output and low noise, discrete JFETs or bipolars in the first stages. The very high audio sensitivity required by these amplifiers makes them respond to mechanical vibration—thus the "microphonics" result. The

New Low Power Single Sideband Circuits

AN1981

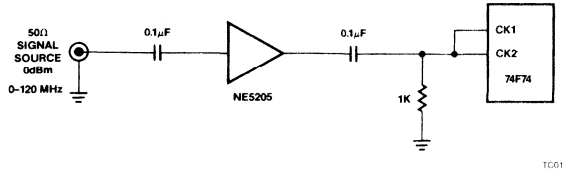


Figure 11. FAST TTL Driver from Analog Signal Source Using NE5205

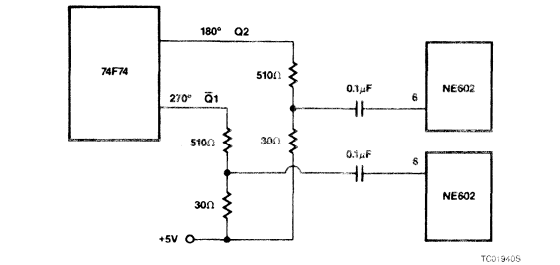


Figure 12. Interface Circuitry Between 74F74 and the NE602s

conversion gain allows use of a simple op amp stage (Figure 13) set up as an integrator to eliminate ultra-sonic and RF instability. The NE5534 is well known for its low noise, high dynamic range, and excellent audio characteristics (Reference 12) and makes an ideal audio amp for the 602 detector.

The sideband select function is easily accomplished with an HEF4053 CMOS analog switch. This triple double-pole switch drives the phase network discussed in the next section and also chooses one of two amplitude balance potentiometers, one for each sideband. Figure 14 illustrates this circuit. A buffer op amp is used with the two sideband select sections to reduce THD, maintain amplitude integrity, and not change the filter network input resistance values. The gain distribution within both legs of the receiver was found to be very consistent (within 1dB), thus the amplitude balance pots may be eliminated in less demanding applications. The NE602s have excellent gain as well as phase integrity.

Audio Phase Shift Circuits

The two critical stages for the phasing method are a dual quadrature mixer and a broadband audio phase shifter (differentiator). There are several broadband, phase shift techniques available. Figure 15 shows an analog all-pass differential phase shift circuit. When the inputs are shorted and driven with a microphone circuit, the outputs will be 90 degrees out-of-phase over the 300 to 3000Hz band. This "splitting" and phase shift is necessary for the phasing generator. For phasing demodulation the two audio detectors are fed to the two inputs. The outputs are then summed to affect the sideband rejection and audio output.

Standard 1% values are shown for the resistors and capacitors, although better gain tolerances can be obtained with 0.1% laser-trimmed integrated resistors. Polystyrene capacitors are preferred for better value tolerance and audio performance. Two quad op amps fit nicely into this application. One op amp serves as a switch buffer and the other three form a phasing section. The NE5514 quad op amps perform well for this application. Careful attention to active filter configurations can yield highly linear and very high dynamic range circuits. Yet these characteristics are much easier to achieve at audio than the common IF RF frequencies. This fact, coupled with the lack of IF tuned circuits, shielding, and higher power requirements make audio IF systems attractive indeed.

Figure 16 shows a "tapped" analog delay circuit which uses weighted values of resistors to affect the phase shift. Excellent phase and amplitude balance are possible with this technique, but the price for components is high. It should be stressed that the audio phase shift accuracy and amplitude balance are the limiting factors for SSB rejection when using the phase method; thus the higher cost may be justified in some applications.

Audio Processing

The summing amplifier is a conventional, inverting op amp circuit. It may be useful to configure a low-pass filter around this amplifier, and thus help the sharp audio filters which follow. Audio filters are necessary to shape the desired bandpass. Steep slope audio bandpass filters can be built from switched capacitor filters or from active filters requiring more op amps. Switched capacitor filters have the disadvantage of requiring a clock frequency in the RF range. Harmonics can cause interference problems if careful design techniques are not used. Also, better dynamic range is obtained with active filter techniques using "real" resistors although much work is being done with SCF's and performance is improving.

Direct conversion receivers rely heavily on audio filters for selectivity. Active analog or switched capacitor filters can produce the high Q and dynamic ranges necessary. Signal strength or "S-meters" can be constructed from the NE602's companion part, the NE604. The "RSSI" or "received signal strength indicator" function on the 604 provides a logarithmic response over a 90dB dynamic range and is easy to use at audio frequencies. Finally, the AGC (automatic gain control) function can also be performed in the audio section. Attack and delay times can be independently set with excellent distortion specifications with the NE572 compandor IC. The audio-derived AGC eliminates the need for gain controlling and RF stage, but relies on an excellent receiver front-end dynamic range. In ACSSB (Amplitude Compandored Single-Side Band) systems transmitter compression and receiver expansion are defined by individual system specifications.

Phasing-Filter Technique

High quality SSB radio specifications call for greater than 70dB sideband rejection. Using the circuits described in this paper for the phasing method, rejection levels of 35dB are obtainable with good reliability. Coupled with an inexpensive two-pole crystal or ceramic filter, the 70dB requirement is obtained. Also, the filtering ahead of the NE602 greatly improves the intermodulation performance of the receiver. Figure 17 shows a complete SSB receiver using the Phasing-Filter technique. The sensitivity of the NE602 allows low gain stages and low power consumption for the RF amplifier and first mixer. A new generation of low power CMOS frequency synthesizers is now available from several manufacturers including the TDD1742 and dual chip HEF4750/51 solutions.

Direct Conversion Receiver

The antenna can be connected directly to the input of the NE602 (via a bandpass filter) to form a direct conversion SSB receiver using

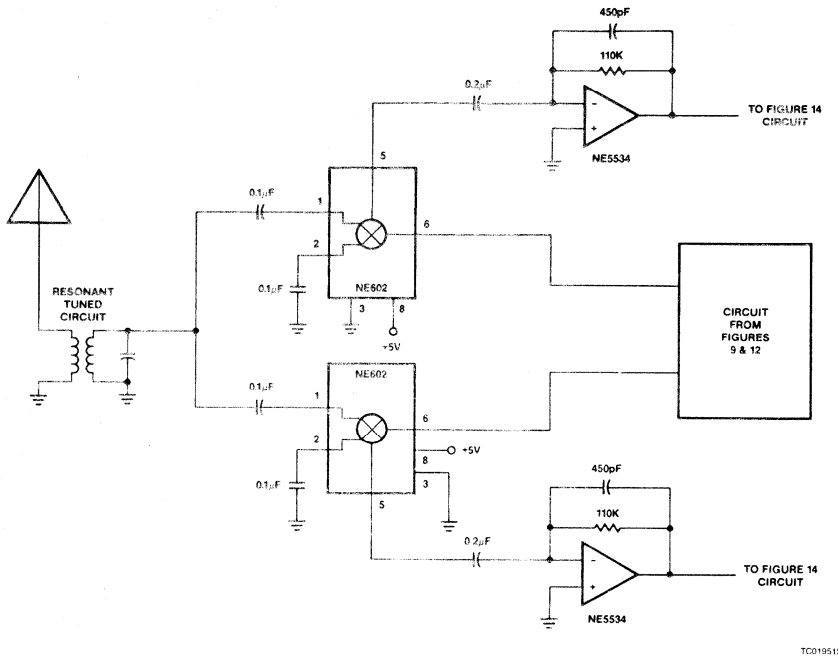


Figure 13. Phasing Method Detector for Direct Conversion Receiver

the phasing method. 35dB sideband rejection is adequate for many applications, particularly where low power and portable battery operation are required. Figure 13 shows a typical circuit for direct conversion applications.

There are many other applications which can make use of SSB technology. Cordless telephones use FM almost exclusively. Eavesdropping could be greatly reduced for systems which employ SSB rather than FM. Furthermore, the better signal-to-noise ratio will extend the range, and battery life will be extended because no carrier is needed.

SSB is also used for subcarriers on microwave links and coaxial lines. Telephone communications networks that use SSB are called FDM or Frequency Domain Multiplex systems. The low power and high sensitivity of the NE602 can offer FDM designers new techniques for system configuration.

Weaver Method Receiver Techniques

The same quadrature dual mixer can be used for the first stage in both the phasing and Weaver method receiver. The subcarrier stage in the Weaver method receiver can use CMOS analog switches (HEF4066) for great power economy. Figure 18 shows a circuit for the subcarrier stage. A 1.8kHz subcarrier requires a 7.2kHz clock frequency. If switched capacitor filters are used for the low-pass and audio filters, a single clock generator can be used for all circuits with appropriate dividers. Furthermore, if the receiver is used as an IF circuit, the fixed LO signal could also be derived from the same clock. This has the added advantage that harmonics from the various circuits will not interfere with the received signal.

Results

The circuit shown in Figures 13, 14, and 15 has a 10dB S/N sensitivity of 0.5μV with a dynamic range of about 80dB. Single-tone audio harmonic distortion is below 0.05% with two-tone intermodulation products below 55dB at RF input levels only 5dB below the 1dB compression point. The sideband rejection is about 38dB at a 9MHz operating frequency. The good audio specifications are a side benefit to direct conversion receivers. When used with inexpensive ceramic or crystal filters, this circuit can provide these specifications with > 70dB sideband rejection.

Conclusions

Single sideband offers many advantages over FM and full-carrier double-sideband modulation. These advantages include: more efficient spectrum use, better signal-to-noise ratios at low signal levels, and better transmitter efficiency. Many of the disadvantages can now be overcome by using old techniques and new state-of-the-art integrated circuits. Effective and inexpensive circuits can use direct conversion techniques with good results. 35dB sideband rejection with less than 1μV sensitivity is obtained with the NE602 circuits. 70dB sideband rejection and superior sensitivity are obtained by using phasing-filter techniques. Either the phasing or Weaver methods can be used in either the direct conversion or IF section applications. The filter and phase-filter methods can be used in only the IF application.

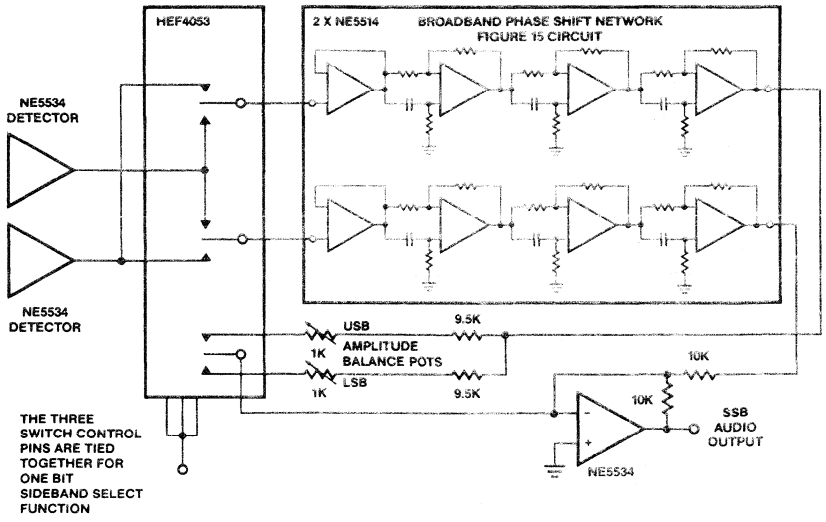


Figure 14. Sideband Select Switching Function

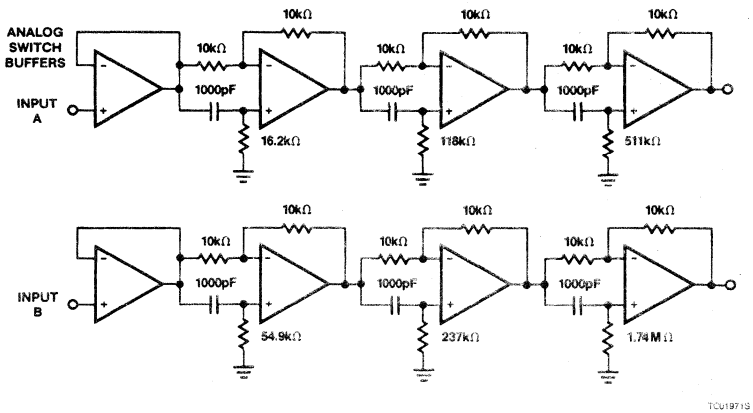


Figure 15

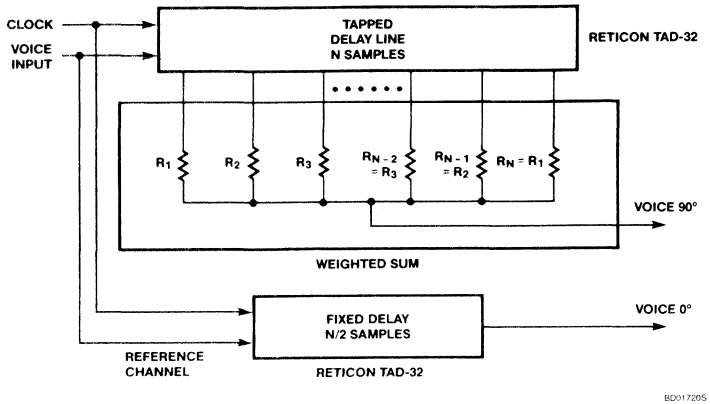
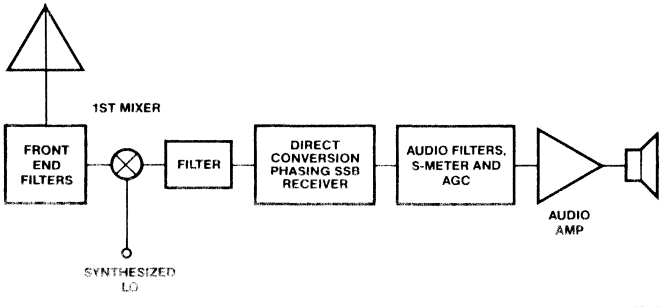


Figure 16. Broadband 90° Audio Phase Shift Technique Using Tapped Delay Line (Reference 4)



Receivers built using this technique can exhibit excellent characteristics without resorting to expensive multi-pole filters or an IF Amplifier chain.

Figure 17. Complete Phasing-Filter Receiver

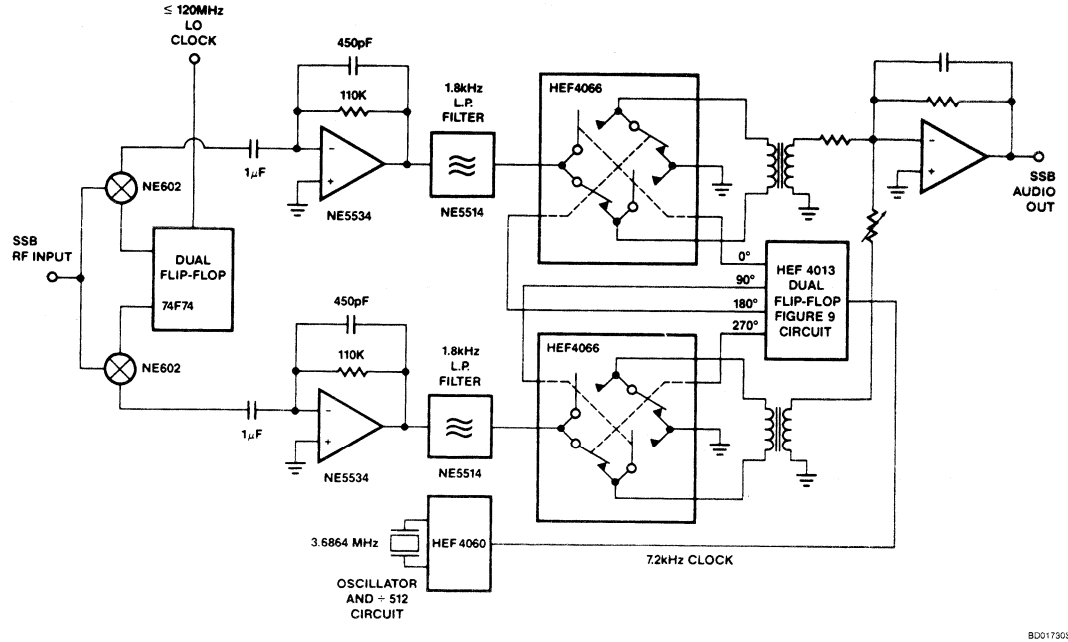


Figure 18. Weaver Method Receiver Concept Example For ≤ 30MHz Operation

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AN1982
Applying the Oscillator of the NE602 in Low Power Mixer Applications

Application Note

INTRODUCTION

For the designer of low power RF systems, the Signetics NE602 mixer/oscillator provides mixer operation beyond 500MHz, a versatile oscillator capable of operation to 200MHz, and conversion gain, with only 2.5mA total current consumption. With a proper understanding of the oscillator design considerations, the NE602 can be put to work quickly in many applications.

DESCRIPTION

Figure 1 shows the equivalent circuit of the device. The chip is actually three subsystems: A Gilbert cell mixer (which provides differential input gain), a buffered emitter follower oscillator, and RF current and voltage regulation. Complete integration of the DC bias permits simple and compact application. The simplicity of the oscillator permits many configurations.

While the oscillator is simple, oscillator design isn't. This article will not address the rigors of oscillator design, but some practical guidelines will permit the designer to accomplish good performance with minimum difficulty.

Either crystal or LC tank circuitry can be employed effectively. Figure 2 shows the four most commonly used configurations in their most basic form.

In each case the Q of the tank will affect the upper frequency limits of oscillation: the higher the Q the higher the frequency. The NE602 is fabricated with a 6GHz process, but the emitter resistor from Pin 7 to ground is nominally 20k. With 0.25mA typical bias current, 200MHz oscillation can be achieved with high Q and appropriate feedback.

The feedback, of course, depends on the Q of the tank. It is generally accepted that a minimum amount of feedback should be used, so even if the choice is entirely empirical, a good trade-off between starting characteristics, distortion, and frequency stability can be quickly determined.

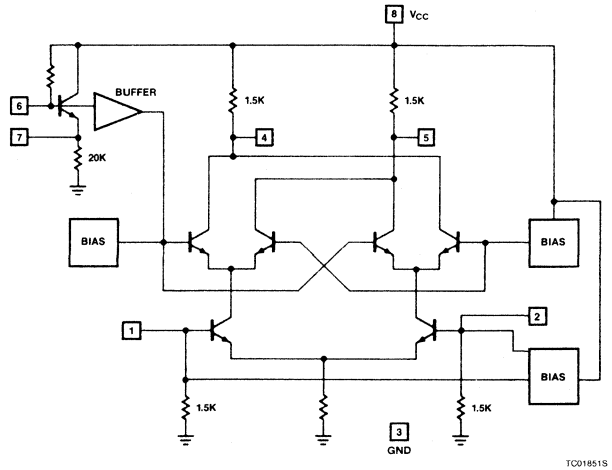
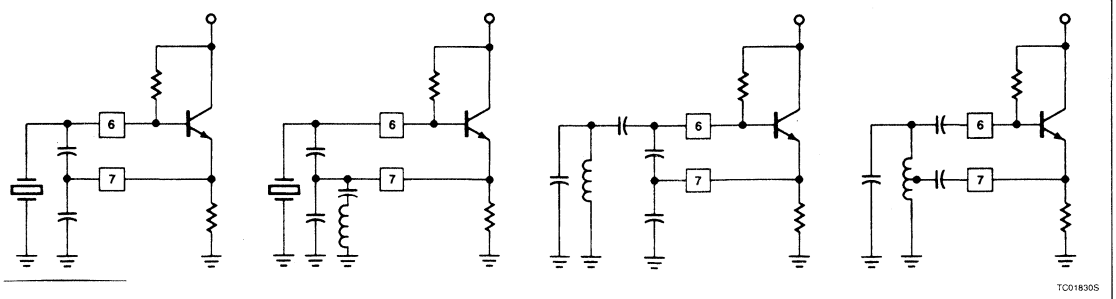


Figure 1



a. Fundamental Crystal **b. Overtone Crystal** **c. Colpitts L/C Tank** **d. Hartley L/C Tank**

Figure 2

Applying the Oscillator of the NE602 in Low Power Mixer Applications

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Crystal Circuit Considerations

Crystal oscillators are relatively easy to implement since crystals exhibit higher Q's than LC tanks. Figure 3 shows a complete implementation of the SA602 (extended temperature version) for cellular radio with a 45MHz first IF and 455kHz second IF.

The crystal is a third overtone parallel mode with 5pF of shunt capacitance and a trap to suppress the fundamental.

LC Tank Circuits

LC tanks present a little greater challenge for the designer. If the Q is too low, the oscillator won't start. A trick which will help if all else fails is to shunt Pin 7 to ground with a 22k resistor. In actual applications this has been effective to 200MHz with high Q ceramic capacitors and a tank inductor of 0.08μH and a Q of 90. Smaller resistor value will upset DC bias because of inadequate base bias at the input of the oscillator. An external bias resistor could be added from V_{CC} to Pin 6, but this will introduce power supply noise to the frequency spectrum.

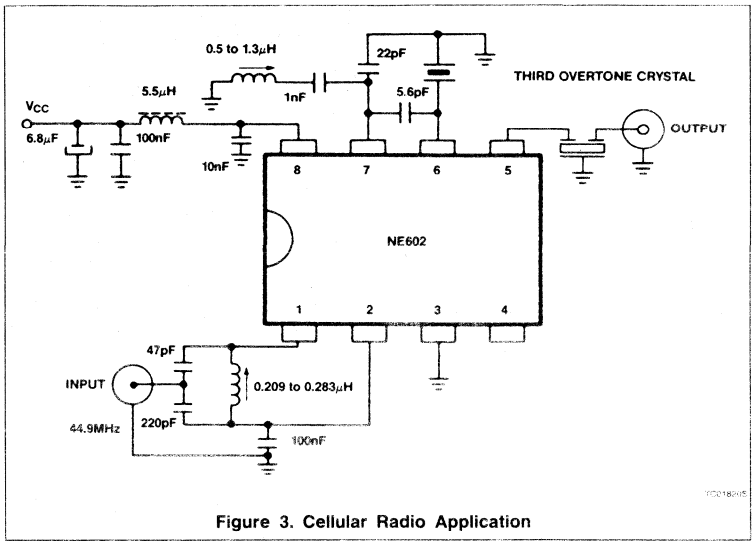


Figure 3. Cellular Radio Application

The Hartley configuration (Figure 2D) offers simplicity. With a variable capacitor tuning the tank, the Hartley will tune a very large range since all of the capacitance is variable. Please note that the inductor must be coupled to Pin 7 with a low impedance capacitor. The Colpitts oscillator will exhibit a smaller tuning range since the fixed feedback capacitors limit variable capacitance range; however, the Colpitts has good frequency stability with proper components.

Synthesized Frequency Control

The NE602 can be very effective with a synthesizer if proper precautions are taken to minimize loading of the tank and the introduction of digital switching transients into the spectrum. Figure 4 shows a circuit suitable for aircraft navigation frequencies (108 – 118MHz) with 10.7MHz IF.

The dual gate MOSFET provides a high degree of isolation from prescaler switching spikes. As shown in Figure 4, the total current consumption of the NE602 and 3SK126 is typically 3mA. The MOSFET input is from the emitter of the oscillator transistor to avoid loading the tank. The Gate 1 capacitance of the MOSFET in series with the 2pF coupling capacitor adds slightly to the feedback capacitance ratio. Use of the 22k resistor at Pin 7 helps assure oscillation without upsetting DC bias.

For applications where optimum buffering of the tank, or minimum current are not mandatory, or where circuit complexity must be minimized, the buffers shown in Figure 5 can be considered.

The effectiveness of the MRF931 (or other VHF bipolar transistors) will depend on frequency and required input level to the prescaler. A bipolar transistor will generally provide the least isolation. At low frequencies the transistor can be used as an emitter follower, but by VHF the base emitter junction will start to become a bidirectional capacitor and the buffer is lost.

The 2N5484 has an IDSS of 5mA max. and the 2SK126 has IDSS of 6mA max. making them suitable for low parts count, modest current buffers. The isolation is good.

Injected LO

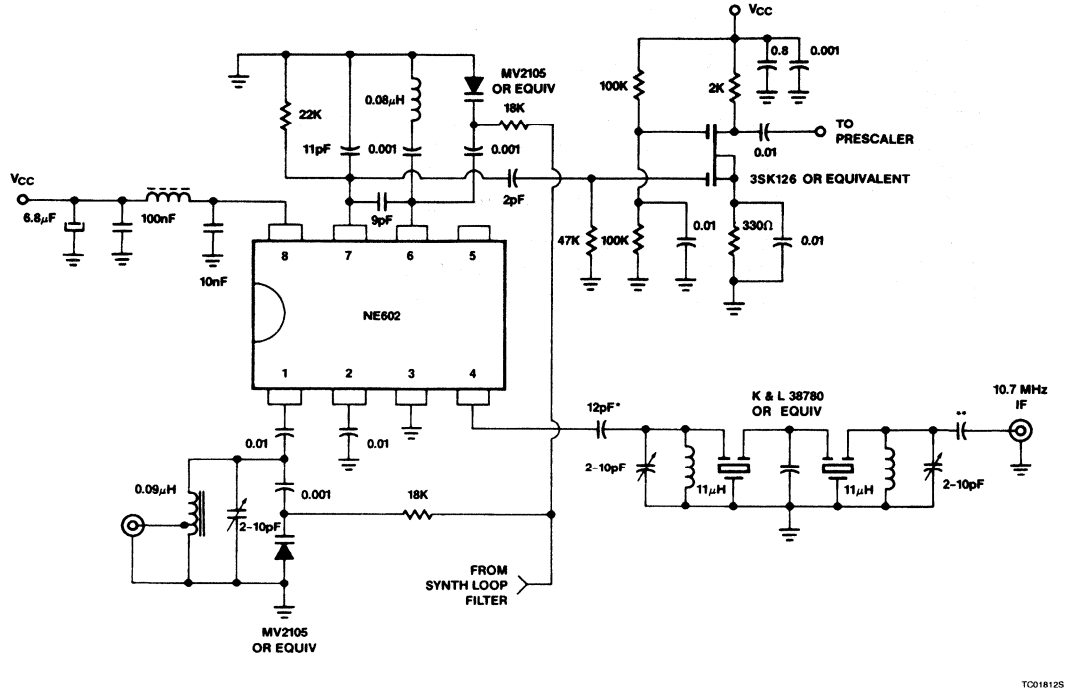
If the application calls for a separate local oscillator, it is acceptable to capacitively-couple 200 to 300mV at Pin 6.

Summary

The NE602 can be an effective low power mixer at frequencies to 500MHz with oscillator operation to 200MHz. All DC bias is provided internal to the device so very compact designs are possible. The internal bias sets the oscillator DC current at a relatively low level so the designer must choose frequency selective components which will not load the transistor. If the guidelines mentioned are followed, excellent results will be achieved.

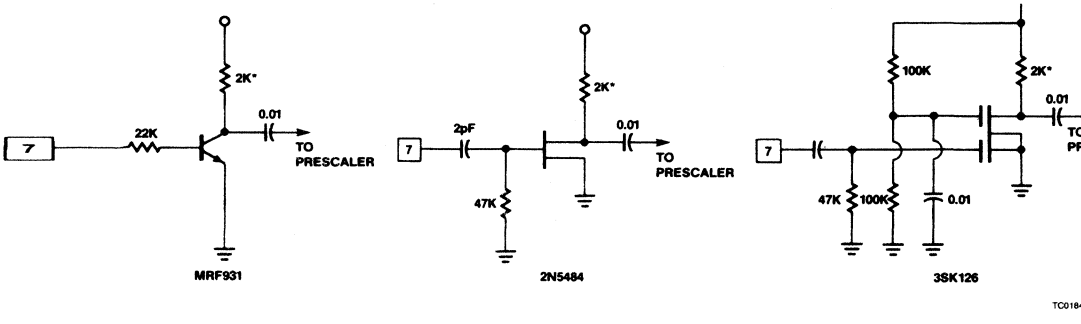
Applying the Oscillator of the NE602 in Low Power Mixer Applications

AN1982



NOTES:
* Permits impedance match of NE602 output, ie: 1.5K//3pF to 3.5K filter impedance.
** Choose for impedance match to next stage.

Figure 4



NOTE:
* 2K or as necessary for current limits or prescaler impedance match.

Figure 5

IF systems

		page
CA3089	FM IF system	1217
MC3361	low-power FM IF system	1223
NE604A	low-power narrow band FM IF system	1226
NE605	low-power FM IF system	1236
NE615	high performance low power mixer FM IF system	1240
SA604A	low-power narrow band FM IF system	1226
SA605	low-power FM IF system	1236
SA615	high performance low-power mixer FM IF system	1240
AN1991	audio decibel level detector with meter driver (NE604A)	1245
AN1992	using the MC3361 demonstration board	1247
AN1993	high sensitivity applications of low-power RF/IF integrated circuits	1253

CA3089
FM IF System

Product Specification

DESCRIPTION

CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM IF system. The block diagram shows the CA3089 features, which include a three-stage FM IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The circuit design of the IF system includes desirable features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8V to +18V.

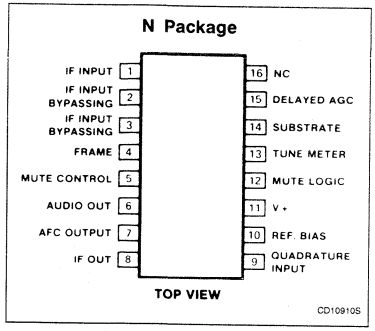
The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089 utilizes a 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40°C to +85°C.

FEATURES

- **Exceptional limiting sensitivity: 10μV typ. at −3dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **High recovered audio: 400mV typ.**
- **Provides specific signal for control of interchannel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply/voltage regulators**

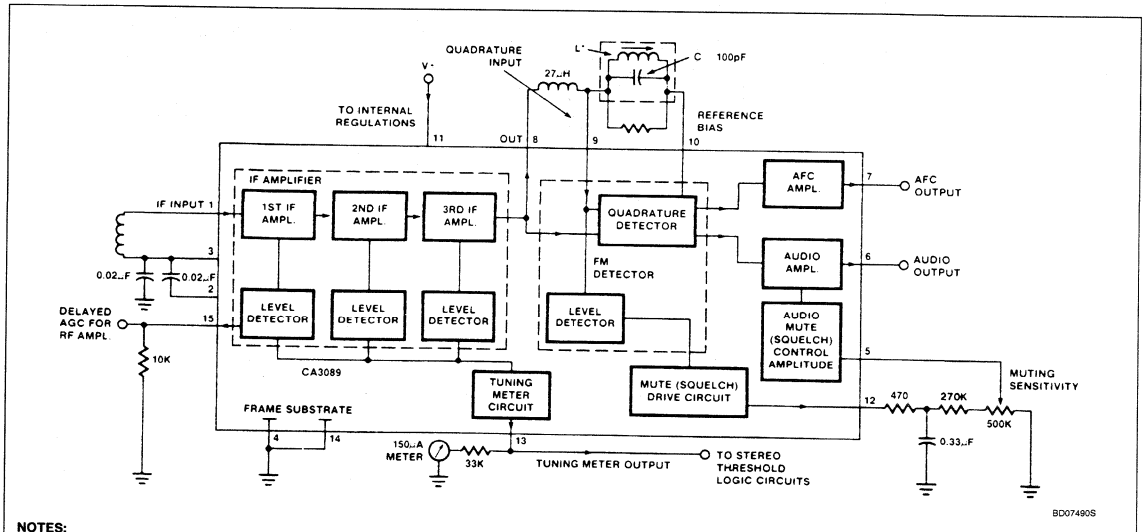
PIN CONFIGURATION



APPLICATIONS

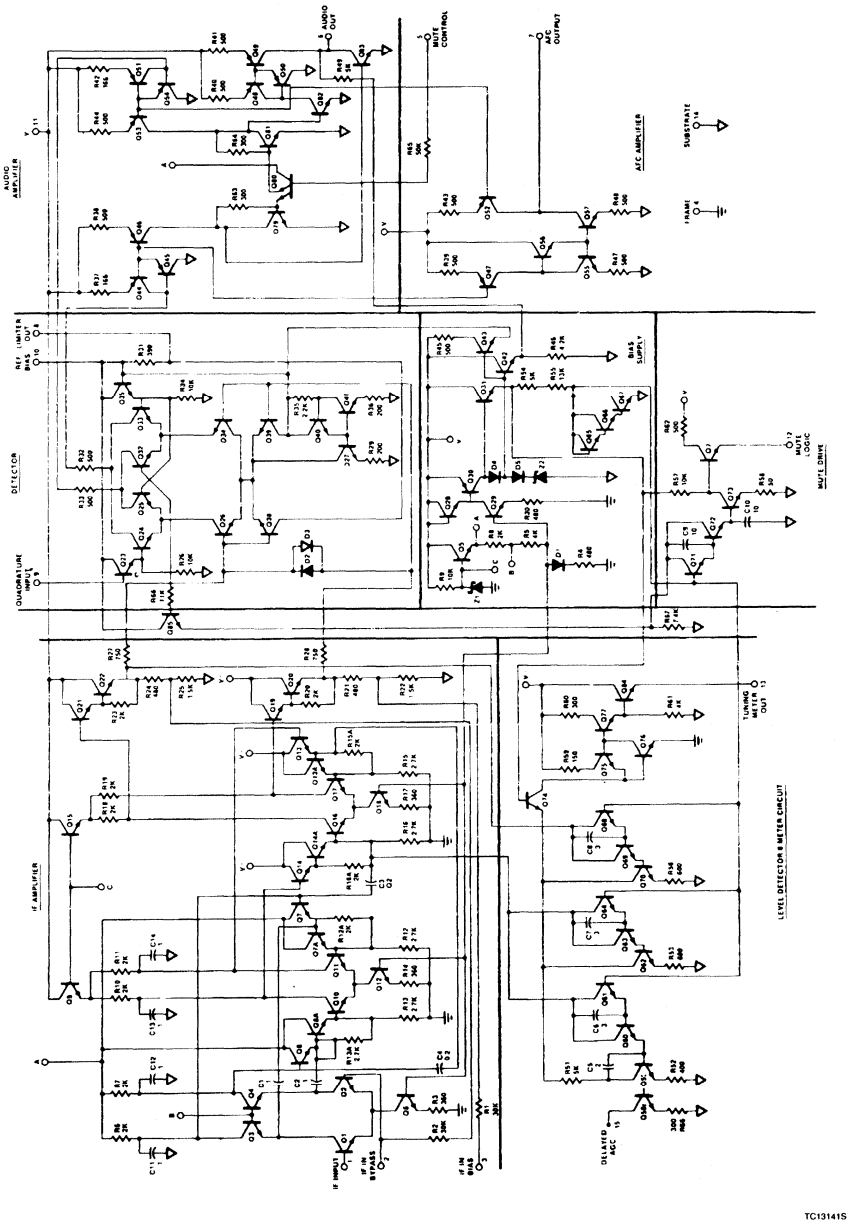
- **High-fidelity FM receivers**
- **Automotive FM receivers**
- **Communications FM receivers**

BLOCK DIAGRAM



NOTES:
1. All resistor values are typical and in ohms. $Q_O \simeq 75$ (G.I. EX27825 or equivalent)
2. L tunes with 100pF (C) at 10.7MHz

EQUIVALENT SCHEMATIC



NOTES:
1. All resistance values are typical and in ohms.
2. All capacitance values are in picofarads.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	−40°C to +85°C	CA3089N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	DC supply voltage: between terminals 11 and 4 between terminals 11 and 14	 18 18	 V V
	DC current (out of Terminal 15)	2	mA
P_D	Device dissipation: up to $T_A = 60°C$ above $T_A = 60°C$	 600 derate linearly 6.7	 mW mW/°C
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

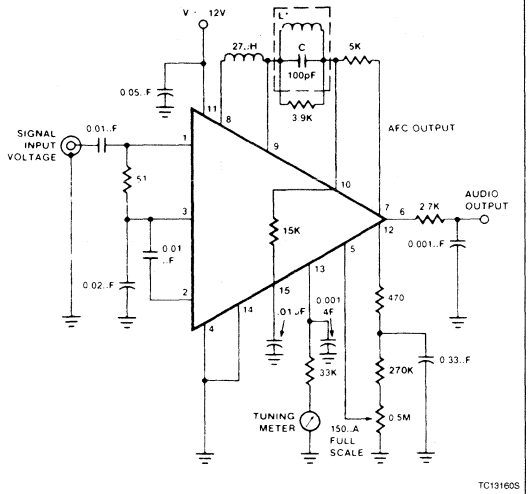
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V^+ = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Static (DC) Characteristics						
I_{11}	Quiescent circuit current	No signal input, non-muted	16	23	30	mA
DC Voltages[4]						
V_1	Terminal 1 (1F input)	No signal input, non-muted	1.2	1.9	2.4	V
V_2	Terminal 2 (AC return to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_3	Terminal 3 (DC bias to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_6	Terminal 6 (audio output)	No signal input, non-muted	5.0	5.6	6.0	V
V_7	Terminal 7 (AFC)	No signal input, non-muted	5.0	5.6	6.0	V
V_{10}	Terminal 10 (DC reference)	No signal input, non-muted	5.0	5.6	6.0	V
Dynamic Characteristics						
$V_{I(LIM)}$	Input limiting voltage (-3dB point)[3]			10	25	μV
	AMR AM rejection (Terminal 6)[4]	$V_{IN} = 0.1V$, $f_O = 10.7MHz$, $f_{MOD} = 400Hz$, AM Mod = 30%	45	55		dB
V_O	Recovered audio voltage (Terminal 6)[3]		400	500	600	mV
	Total harmonic distortion:[1]					
THD	Single tuned (Terminal 6)[3]			0.5	1.0	%
THD	Double tuned (Terminal 6)[4]	$f_{MOD} = 400Hz$, $V_{IN} = 0.1$		0.1		%
S + N/N	Signal plus noise-to-noise ratio (Terminal 6)[3]	Deviation = ± 75kHz, $V_{IN} = 0.1V$	60	70		dB
MU_{IN}	Mute input (Terminal 5)	$V_5 = 2.5V$	50	70		dB
MU_{OUT}	Mute output (Terminal 12)	$V_{IN} = 50\mu V$			0.5	V
		$V_{IN} = 0V$	4.0			V
MTR	Meter output (Terminal 13)	$V_{IN} = 0.1V$	2.5	3.5		V
		$V_{IN} = 500\mu V$	1.0	1.5		V
		$V_{IN} = 0V$			0.7	V
AGC	Delay AGC (Terminal 15)	$V_{IN} = 0.01V$			0.5	V
		$V_{IN} = 10\mu V$	4.0	5.0		V
THD	Double tuned (Terminal 6)[4]	$f_{MOD} = 400Hz$, $V_{IN} = 0.1$		0.1		%

NOTES

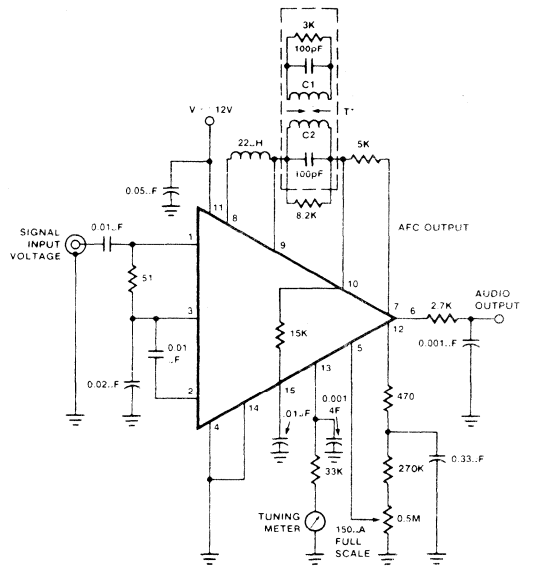
1. THD characteristics and audio level are essentially a function of the phase and Q characteristics of the network connected between Terminals 8, 9, and 10.
2. Test circuit Figure 1.
3. Test circuit Figure 2.
4. Test circuit Figures 1 and 2.

TEST CIRCUITS



NOTES:
1. L tunes with 100pF (C) at 10.7MHz.
2. All resistor values are typical and in ohms.
3. Q_O (unloaded) $\simeq$ 75 (G.I. automatic mfg. div. EX27825 or equivalent).

Figure 1. Test Circuit Using a Single-Tuned Detector Coil

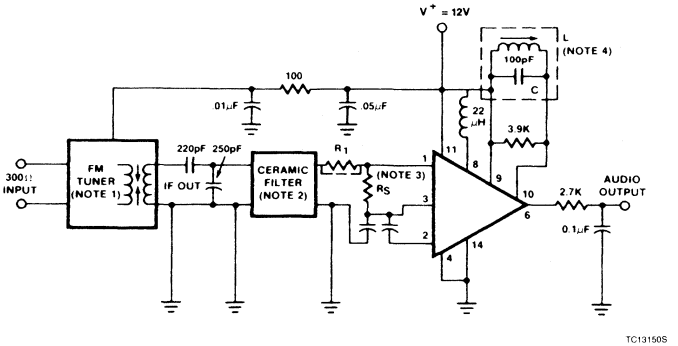


NOTES:
All resistor values are typical and in ohms.

T: Pri — Q_O (unloaded) $\simeq$ 75 (tunes with 100pF (C1) 20 † of 34e on 7/32' dia. form) Sec. – Q (unloaded) $\simeq$ 75 (tunes with 100pF (C2) 20 † of 34e on 7/32' dia. form)
kQ (percent of critical coupling) > 70%
(Adjusted for coil voltage V_C = 150mV)
Above values permit proper operation of mute (squelch) circuit 'E' type slugs, spacing 4mm

Figure 2. Test Circuit Using a Double-Tuned Detector Coil

TEST CIRCUITS



NOTES:
All resistor values are typical and in ohms.
1. Waller 4SN3FIC or equivalent.
2. Murate SFG 10.7mA or equivalent.
3. R_S will affect stability depending on circuit layout. To increase stability R_S is decreased. Range of R_S is 330 to 50Ω, $R_1 + R_S \leq 330\Omega$.
4. L tunes with 100pF (C) at 10.7MHz Q_O unloaded ≃ 75 (G.I. EX27825 or equivalent).

Performance data at f_O = 98MHz, f_{MOD} = 400Hz, deviation = ± 74kHz.
± 74kHz.

– 3dB limiting sensitivity	2μV (antenna level)
20dB quieting sensitivity	1μV (antenna level)
30dB quieting sensitivity	1.5μV (antenna level)

Figure 3. Typical FM Tuner With a Single-Tuned Detector Coil

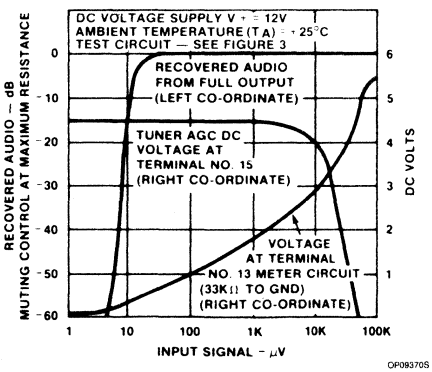
SYSTEM DESIGN CONSIDERATIONS

The CA3089 is a very high gain device and therefore careful consideration must be given to the layout of external components to minimize feedback. The input bypass capacitors should be located close to the input terminals and the values should not be large nor should the capacitors be of the type which might introduce inductive reactance to the circuit. An example of good bypass capacitors would be ceramic disc with values in the range of 0.01 to 0.05μF.

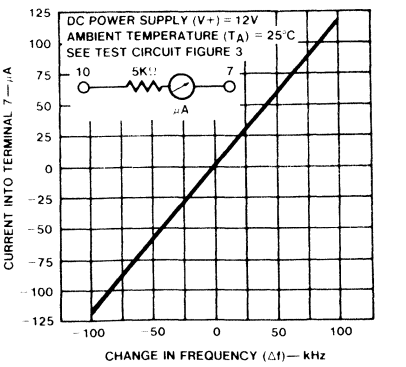
The input impedance of the CA3089 is approximately 10,000Ω. It is *not* recommended to match this impedance. The value of the input termination resistor should be as low as possible without degrading system operation. The lower the value of this resistor the greater the system stability. An input terminating resistor between 50Ω and 100Ω is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

Muting Action, Tuner AGC
(Tuning meter output as a function of input signal voltage.)



AFC Characteristics
(Current at Terminal 7 as a function of change in frequency.)



MC3361
Low Power FM IF

Product Specification

DESCRIPTION

The MC3361 is a monolithic low-power FM IF signal processing system consisting of an oscillator, mixer, limiting amplifier, quadrature detector, filter amplifier, squelch, scan control and mute switch. It is intended for use in narrow band FM dual conversion communications equipment. The MC3361 is available in a 16-lead, dual-in-line plastic package and 16-lead SOL (surface-mounted miniature package).

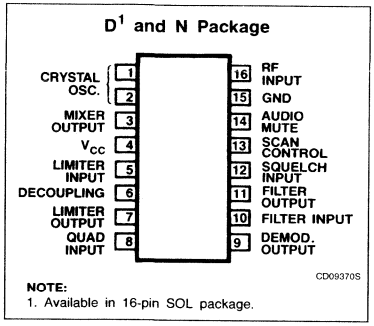
FEATURES

- **2.0V to 8.0V operation**
- **Low current: 4.2mA typ at V_{CC} = 4.0V_{DC}**
- **Excellent sensitivity: 2.0μV for −3dB limiting typ**
- **Low external parts count**
- **Operation to 60MHz**

APPLICATIONS

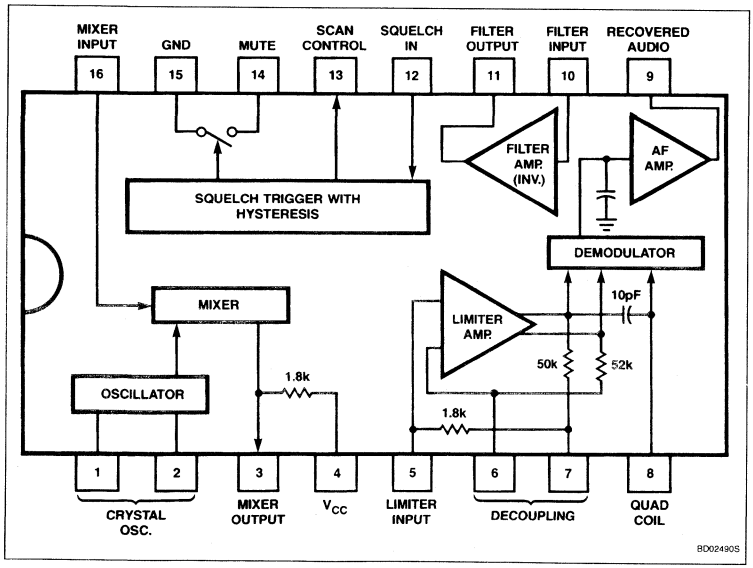
- **Cordless telephone**
- **Narrow band receivers**
- **Remote control**

PIN CONFIGURATION



NOTE:
1. Available in 16-pin SOL package.

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	−40 to +85°C	MC3361N
16-Pin Plastic; SOL	−40 to +85°C	MC3361D

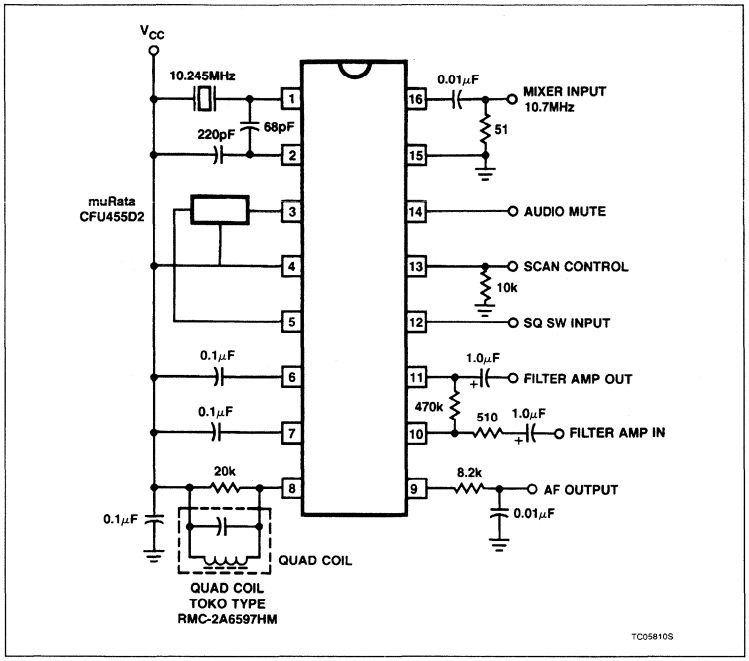
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

SYMBOL	PARAMETER	PIN	RATING	UNIT
V_{CC} (Max)	Power supply voltage	4	10	V_{DC}
V_{CC}	Generating supply voltage range	4	2.0 to 8.0	V_{DC}
	Detector input voltage	8	1.0	V_{P-P}
V_{16}	Input voltage (V_{CC}≥4.0V)	16	1.0	V_{RMS}
V_{14}	Mute function	14	−0.5 to 5.0	V_{PK}
T_J	Junction temperature		150	°C
T_A	Operating ambient temperature range		−40 to +85	°C
T_{STG}	Storage temperature range		−65 to +150	°C

AC AND DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0V_{DC}, f_O = 10.7MHz, Δf = ±3.0kHz, f_{MOD} = 1.0kHz, T_A = 25°C unless otherwise noted.)

PARAMETER	PIN	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Drain current (no signal) squelch off squelch on	4			 4.2 5.4	 7.0 9.0	mA
Input limiting voltage	16	−3.0dB limiting		2.0	6.0	μV
Detector output voltage	9			2.0		V_{DC}
Detector output impedance				450		Ω
Recovered audio output voltage	9	V_{IN} = 10mV_{RMS}	100	150	270	mV_{RMS}
Filter gain (10kHz)		V_{IN} = 1.0mV_{RMS}	40	46		dB
Filter output voltage	11			1.7		V_{DC}
Trigger hysteresis				50		mV
Mute function low	14			10		Ω
Mute function high	14			10		MΩ
Scan function low (mute off)	13	V_{12} = 1.0V_{DC}			0.5	V_{DC}
Scan function high (mute on)	13	V_{12} = GND	3.5			V_{DC}
Mixer conversion gain	3			27		dB
Mixer input resistance	16			3.6		kΩ
Mixer input capacitance	16			2.2		pF

TEST CIRCUIT



NE/SA604A
High-Performance Low-Power FM IF System

Preliminary Specification

DESCRIPTION

The NE/SA604A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA604A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA604A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature package).

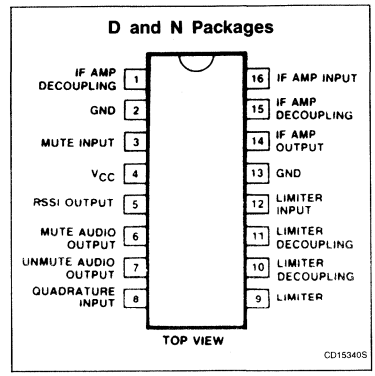
FEATURES

- **Low-power consumption 3.3mA typical**
- **Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Two audio outputs – muted and unmuted**
- **Low external component count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz**
- **SA604A meets cellular radio specifications**

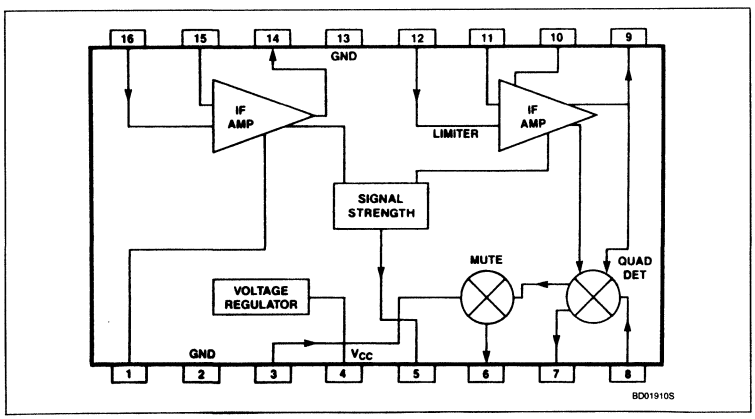
APPLICATIONS

- **Cellular Radio FM IF**
- **High performance communications receivers**
- **Intermediate freqency amplification and detection up to 21MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **FSK and ASK data receivers**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE604AN
16-Pin Plastic SO (Surface-mounted miniature package)	0 to +70°C	NE604AD
16-Pin Plastic DIP	−40 to +85°C	SA604AN
16-Pin Plastic SO (Surface-mounted miniature package)	−40 to +85°C	SA604AD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating temperature NE604A SA604A	 0 to 70 −40 to +85	 °C °C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated

SYMBOL	PARAMETER	TEST CONDITIONS	NE604A			SA604A			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Power supply voltage range		4.5		8.0	4.5		8.0	V
	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (on) (off)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated. IF frequency = 455kHz; IF level = −47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

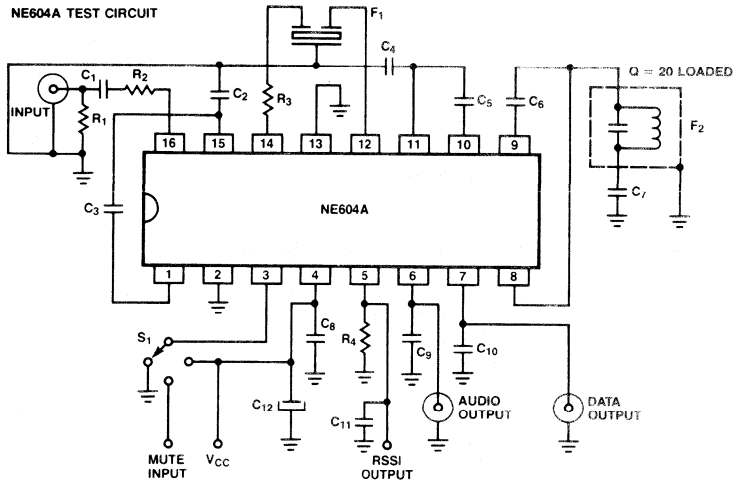
SYMBOL	PARAMETER	TEST CONDITIONS	NE604A			SA604A			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input limiting-3dB	Test at Pin 16		−92			−92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de-emphasis	110	175	250	80	175	260	mV_{rms}
	Recovered audio level	150pF de-emphasis		530			530		mV_{rms}
	SINAD sensitivity	RF level −97dBm		16			16		dB
	THD		−35	−42		−34	−42		dB
	Signal-to-noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = −118dBm	0	160	550	0	160	650	mV
		RF level = −68dBm	2.0	2.65	3.0	1.09	2.65	3.1	V
		RF level = −18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI range	R_4 = 100k Pin 5		90			90		dB
	RSSI accuracy	R_4 = 100k Pin 5		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		Ω

NOTE:

1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

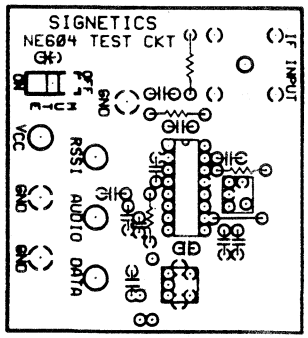
NE604(50)	NE604A (1.5k)/NE605 (1.5k)
−97dBm	−118dBm
−47dBm	−68dBm
+3 dBm	−18dBm

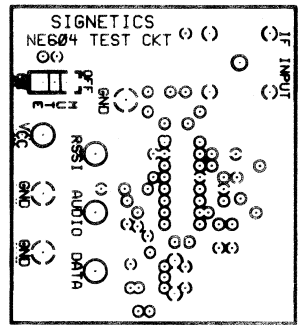
2. The NE605 and NE604A are both derived from the same basic die. The NE605 performance plot NE604A.



NOTES:

C1 10nF +80–20% 63V K10000-Z5V Ceramic
C2 100nF ±10% 50V
C3 100nF ±10% 50V
C4 100nF ±10% 50V
C5 100nF ±10% 50V
C6 10pF ±2% 100V NPO Ceramic
C7 100nF ±10% 50V
C8 100nF ±10% 50V
C9 15nF ±10% 50V
C10 150pF ±2% 100V N1500 Ceramic
C11 1nF ±10% 100V K2000-Y5P Ceramic
C12 6.8uF ±20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter A2549
R1 51Ω ±1% ¼W Metal Film
R2 1500Ω ±1% ¼W Metal Film
R3 1500Ω ±5% ⅛W Carbon Composition
R4 100kΩ ±1% ¼W Metal Film





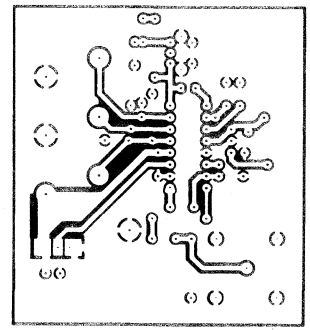


Figure 1. NE604A Test Circuit

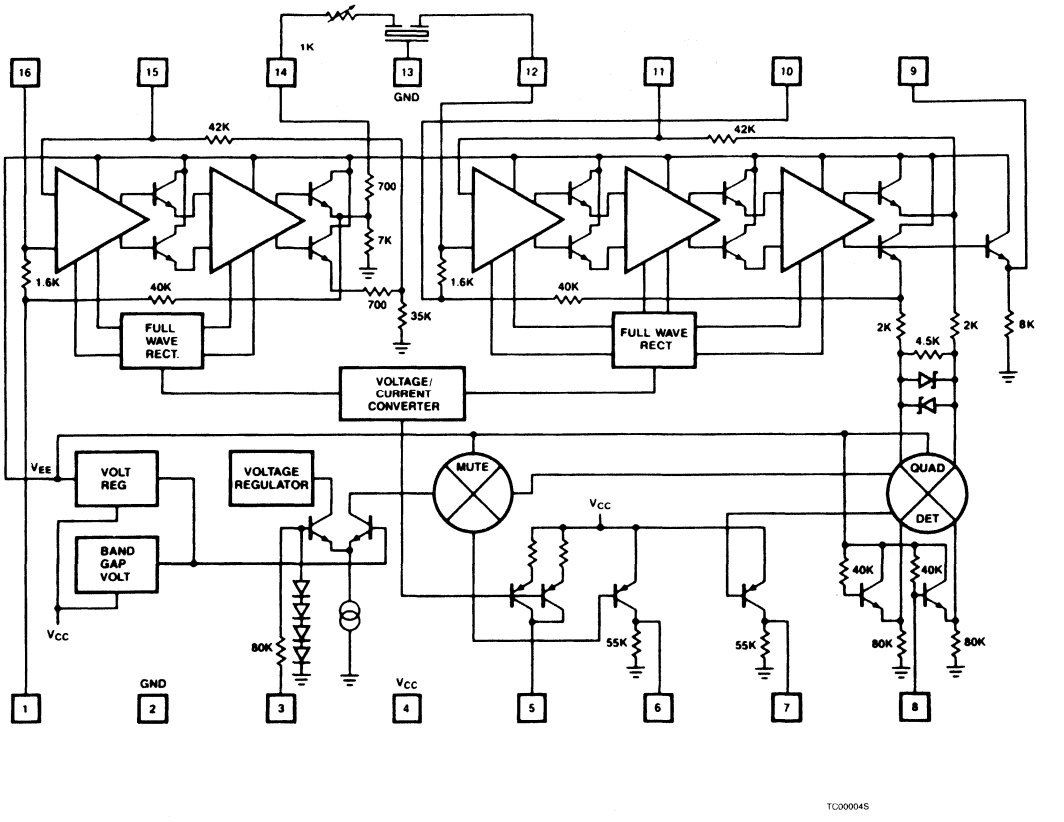


Figure 2. Equivalent Circuit

CIRCUIT DESCRIPTION

The NE/SA604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA604A can not be evaluated independent of circuit, components, and board layout. A physicial layout which correlates to the electrical limits is shown in Figure 1. The configuration can be used as the basis for production layout.

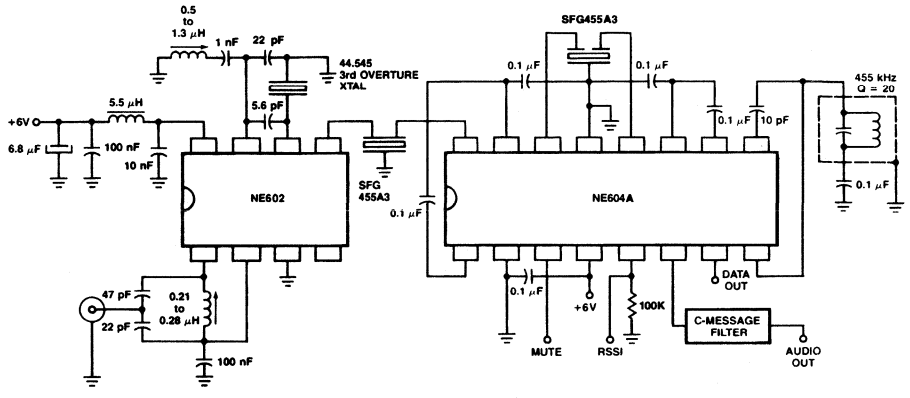
The NE/SA604A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF AMPLIFIERS

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2 the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

Because of the very high gain, bankwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including the RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin



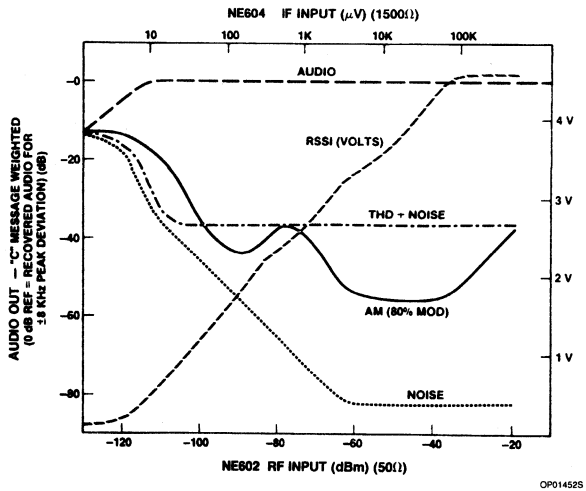


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

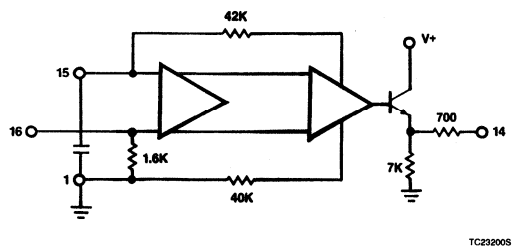


Figure 4. First Limiter Bias

to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 7. Reduce gain will result in reduced limiting sensitivity.

A feature of the NE604A IF amplifiers, which is not specified, is low phase shift. The NE604A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

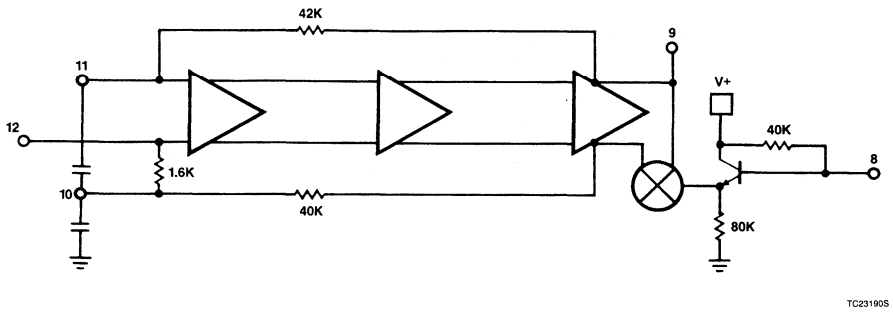


Figure 5. Second Limiter and Quadrature Detector

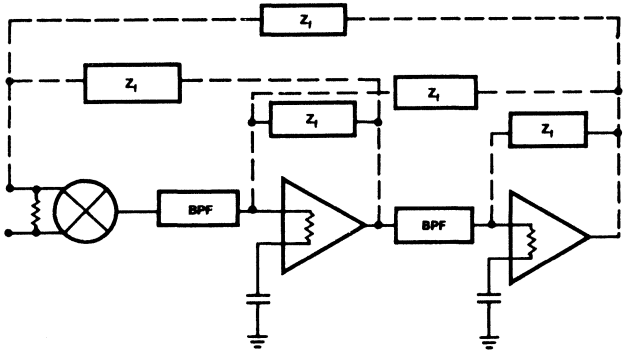


Figure 6. Feedback Paths

Stability Considerations

The high gain and bandwidth of the NE604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and grounds, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1μF monolithic right at the V_{CC} pin, and a 6.8μF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1μF tantalum has proven acceptible with this layout. Every layout must be evaluated on its own merit, don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

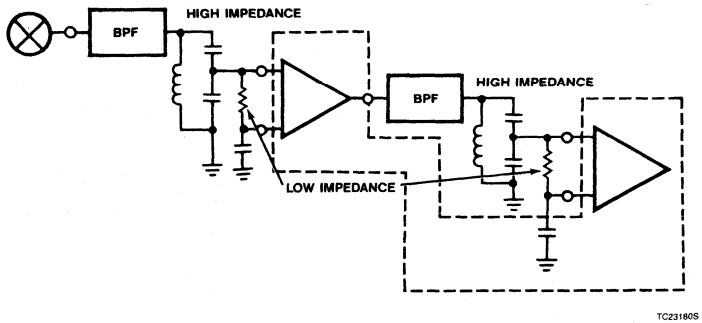
As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrow-band selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean nonexistent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

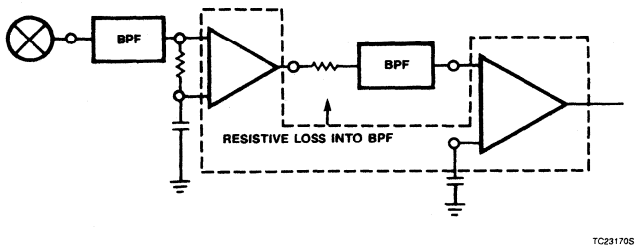
The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single ended to an external capacitor at Pin 9. There is a 90° phase shift across the phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multipler at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.



7a. Terminating High Impedance Filters with Transformation to Low Impedance



7b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

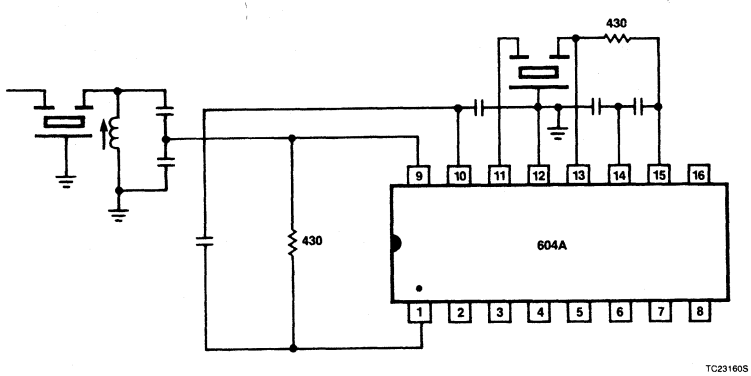


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

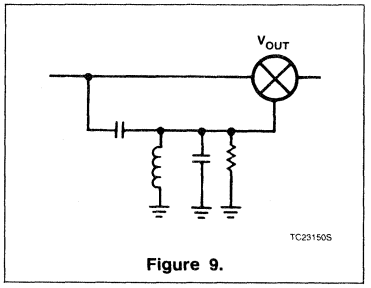


Figure 9.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the nonlinearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first order effects only.

Frequency Discriminator Design Equations for NE604A

$$V_O = \frac{C_S}{C_P + C_S} \cdot \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \cdot V_N \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_3 will be:

$$\phi = \angle V_O - \angle V_N = \text{tg}^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1-\left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10. Is the plot of ϕ vs $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of

$$\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}.$$

The signal V_o would have a phase shift of $\left[\frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \text{ Sin } \omega t$ (3)

$$\rightarrow V_O = A \text{ Sin}\left[\omega t + \frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \cdot V_O = A^2 \text{ Sin } \omega t \quad (4)$$

$$\text{Sin}\left[\omega t + \frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$$

after low pass filtering

$$\rightarrow V_{OUT} = \frac{1}{2}A^2 \quad (5)$$

$$\text{COS}\left[\frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right] = \frac{1}{2}A^2 \text{ Sin}\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1\left(\frac{\omega}{\omega_1}\right) = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} \ll \frac{\pi}{2}$

Which is the discriminated FM output.

NOTE: $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p.311. Example: At 455kHz IF, with ±5kHz FM deviation. The max/min normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the ϕ vs. normalized frequency curves (Figure 10) and draw a vertical

straight line at $\left(\frac{\omega}{\omega_1}\right) = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discrimination FM signal. (Eq.6)

→Choose a Q = 20.

The internal R of the 604A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and $L = 0.7\text{mH}$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10\text{pF}$ and $C_P = 164\text{pF}$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH, should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1\text{pF}$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. This response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Since the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resis-

tance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two outputs differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be the logical output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10 MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE604A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1Ω resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an inband signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

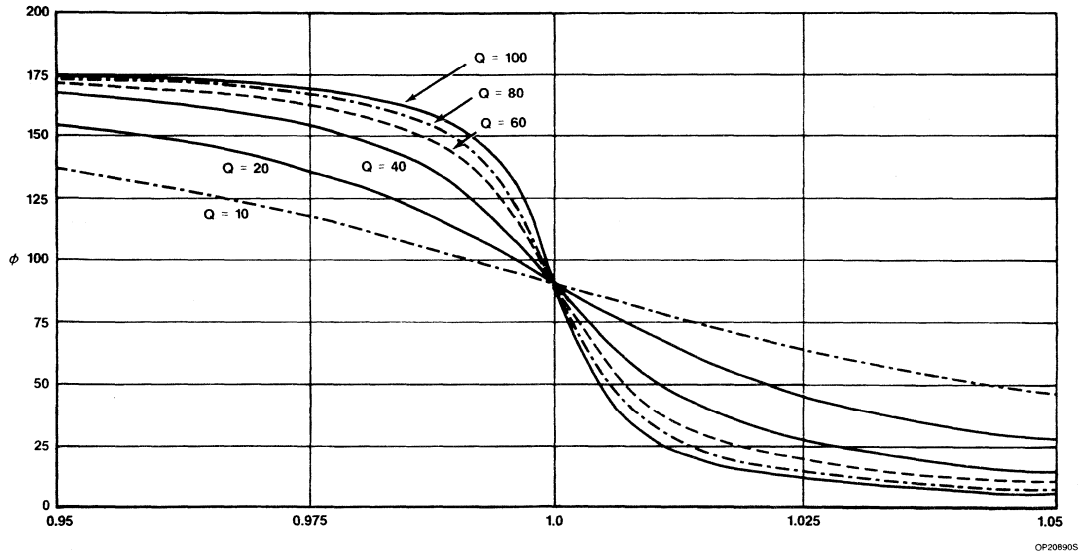


Figure 10. Phase vs. Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

NE/SA605
Low Power FM IF System

Objective Specification

DESCRIPTION

The NE/SA605 is a monolithic, low power FM IF system incorporating VHF monolithic, double-balanced mixer with input amplifier, on-board oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator.

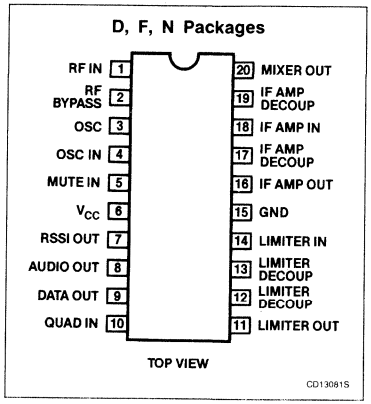
It is intended for high performance, low power communication systems. The guaranteed parameters of the SA605 make this device particularly well-suited to cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 15dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external L.O. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low power, and noise characteristics make the NE/SA605 a superior choice for high-performance battery-operated equipment.

The NE/SA605 is available in 20-lead dual in-line plastic and Cerdip packages and 20-pin SO (surface-mounted miniature) packages.

FEATURES

- **Low power consumption: 5.3mA typical**
- **Excellent noise figure: < 5.0dB typical at 45MHz**
- **High operating frequency**
- **Excellent gain, intercept, and sensitivity**
- **Low external parts count; suitable for crystal/ceramic filters**
- **SA605 meets cellular radio specifications**
- **Logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 80dB**
- **Separate data output**
- **Audio output with muting**
- **Excellent sensitivity: 1.5μV across input pins (0.27μV into 50Ω matching network) for 12dB SINAD (Signal-to-Noise and Distortion ratio) at 455kHz**

PIN CONFIGURATION



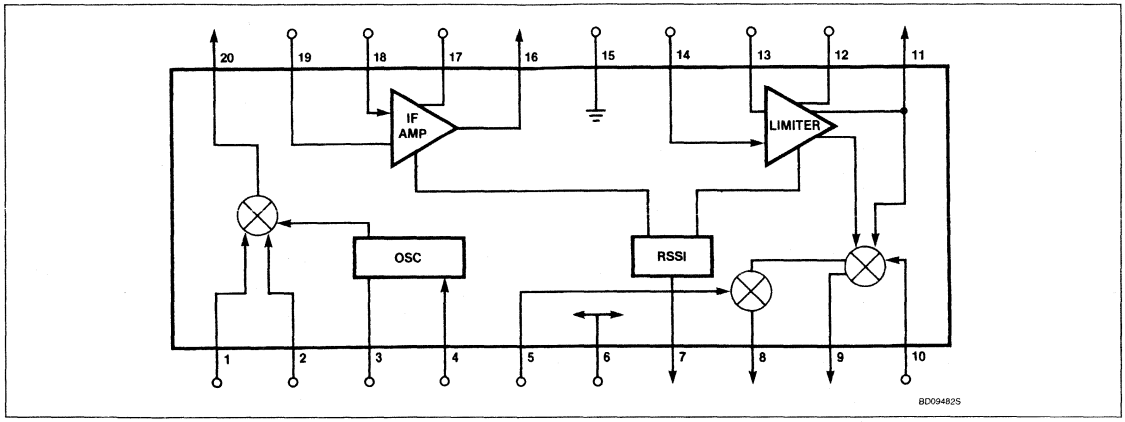
APPLICATIONS

- **Cellular radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 25MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **HF/VHF frequency conversion**
- **Instrumentation frequency conversion**
- **Broadband LANs**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE605N
20-Pin Plastic SO	0 to +70°C	NE605D
20-Pin Ceramic DIP	0 to +70°C	NE605F
20-Pin Plastic DIP	-40°C to +85°C	SA605N
20-Pin Plastic SO	-40°C to +85°C	SA605D
20-Pin Ceramic DIP	-40°C to +85°C	SA605F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating temperature range NE605 SA605	 0 to +70 −40 to +85	 °C °C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			5.3	6.0	mA
	Mute switch input threshold (on) (off)		 1.7		 1.0	 V V

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated. RF frequency = 45MHz; IF frequency = 455MHz; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0		dB
	Third-order intercept point	$RF_{IN} = -45dBm$: $f_1 = 45.0$ $f_2 = 45.06$		−15		dBm
	Conversion gain at 45MHz			15		dB
R_{IN}	RF input resistance	Single-ended input	1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 20)		1.5		kΩ
	Input limiting −3dB	Test at Pin 1		−117		dBm
	AM rejection	80% AM 1kHz	30			dB
	Recovered audio level	After C filter and de-emphasis capacitor	80	100		mV_{RMS}
	Recovered data level		250	350		mV_{RMS}
	SINAD sensitivity	RF level −117dBm	12	15		dB
THD	Total harmonic distortion		−35			dB
S/N	Signal-to-noise ratio	No modulation for noise	70	75		dB
	RSSI output	R_{RSSI} = 100K RF level = −117dBm RF level = −67dBm RF level = −23dBm	 0 2.0 4.0		 400 2.6 5.0	 mV V V
	RSSI range	R_{RSSI} = 100k Pin 7		90		dB
	RSSI accuracy	R_{RSSI} = 100k Pin 7		±1.5		dB
	IF input impedance		1.5			kΩ
	IF output impedance		1.0			kΩ
	Limiter input impedance		1.5			kΩ
	Quadrature detector data output impedance			50		kΩ
	Muted audio output impedance			50		kΩ

Circuit Description

The NE/SA605 is an RF/IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 500MHz. The bandwidth of the IF amplifiers is 25MHz. However, the gain distribution is optimized for 455kHz. The overall system is well-suited to battery operation as well as high-performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 15dB, and input third order intercept of −15dBm. The oscillator will operate well in excess of 200MHz in L/C tank configurations, either Hartley or Colpitts. For crystal oscillators, the Colpitts configuration is used.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The equivalent input impedance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 6dB insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network..

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 92dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability. Alternatively, if gain distribution permits, only the second limiting IF stage can be used. This stage has 57dB of gain.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength indicator completes the circuitry. The output range is greater than 80dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

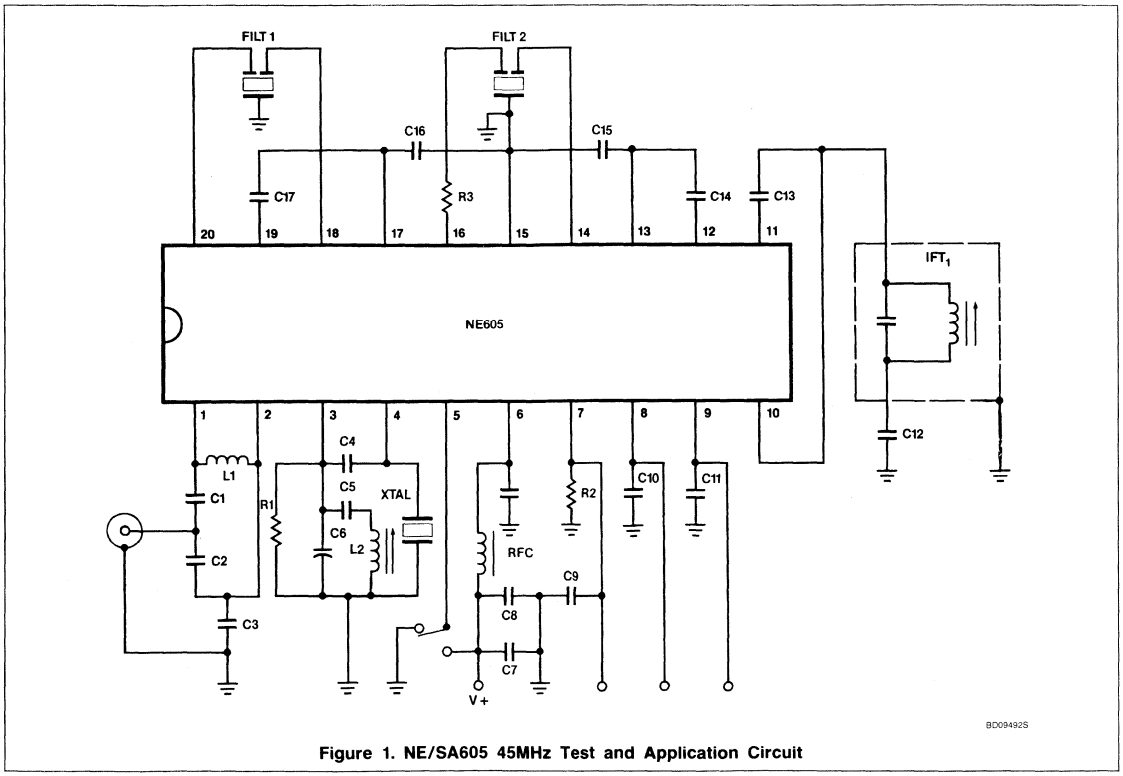


Figure 1. NE/SA605 45MHz Test and Application Circuit

NE/SA615
High-Performance Low Power Mixer FM IF System

Preliminary Specification

DESCRIPTION

The NE/SA615 is a consumer monolithic low power FM IF system incorporating a mixer/osc, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA615 is available in a 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package).

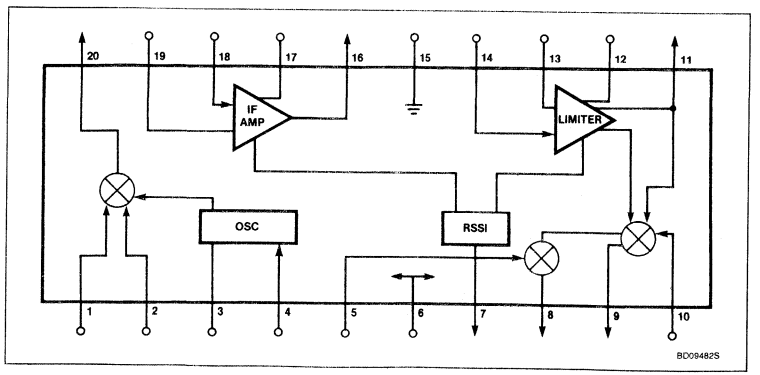
FEATURES

- **Low-power consumption 5.7mA typical at 6V**
- **Mixer input to > 500MHz**
- **Mixer conversion power gain of 13dB at 45MHz**
- **Mixer noise figure of 4.6dB at 45MHz**
- **XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)**
- **102dB of limiter gain**
- **25MHz limiter small signal bandwidth**
- **Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Two audio outputs - muted and unmuted**
- **Low external component count; suitable for crystal/ceramic/LC filters**

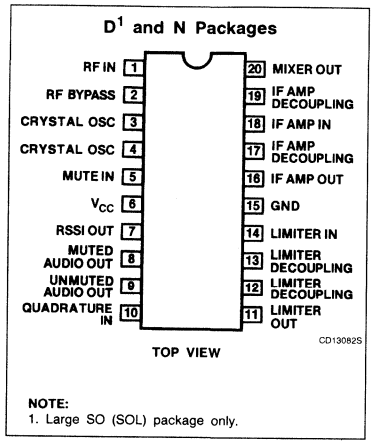
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0°C to +70°C	NE615N
20-Pin Plastic SOL (Surface-mounted)	0°C to +70°C	NE615D
20-Pin Plastic DIP	−40°C to +85°C	SA615N
20-Pin Plastic SOL (Surface-mounted)	−40°C to +85°C	SA615D

BLOCK DIAGRAM



PIN CONFIGURATION



NOTE:
1. Large SO (SOL) package only.

- **Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz**
- **SA615 meets cellular radio specifications**
- **ESD hardened**
- **Will handle IF frequencies up to 25MHz**

APPLICATIONS

- **Consumer cellular radio FM IF**
- **Single conversion VHF/UHF receivers**
- **SCA receivers**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **FSK and ASK data receivers**
- **Log amps**
- **Wideband low current amplification**

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating temperature NE605 SA605	 0 to +70 −40 to +85	 °C °C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			NE/SA615			
			Min	Typ	Max	
	Power supply voltage range		4.5		8.0	V
	DC current drain			5.7	7.4	mA
	Mute switch input threshold (on) (off)		1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated. RF frequency = 45MHz, + 14.5dBV RF input step-up; IF frequency = 455kHz, $R_{17} = 5.1k$; RF level = −45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			NE/SA615			
			Min	Typ	Max	
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order intercept point	f1 = 45.0; f2 = 45.06MHz		−12		dBm
	Conversion power gain	Matched 14.5dBV step-up 50Ω source	8.0	13 −1.7		dB dB
R_{IN}	RF input resistance	Single-ended input	3.0	4.7		kΩ
C_{IN}	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.50		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting −3dB, $R_{17} = 5.1k$	Test at Pin 18		−109		dBm
	AM rejection	80% AM 1kHz	25	33	43	dB
	Audio level, $R_{10} = 100k$	15nF de-emphasis	60	175	260	mV_{RMS}
	Unmuted audio level, $R_{11} = 100k$	150pF de-emphasis		530		mV_{RMS}
	SINAD sensitivity	RF level −118dBm		12		dB
THD	Total harmonic distortion		−30	−42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB

AC ELECTRICAL CHARACTERISTICS (Continued) Typical reading at $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated. RF frequency = 45MHz, + 14.5dBV RF input step-up; IF frequency = 455kHz, $R_{17} = 5.1k$; RF level = −45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			NE/SA615			
			Min	Typ	Max	
	IF RSSI output, $R_9 = 100k$[1]	IF level = −118dBm	0	160	800	mV
		IF level = −68dBm	1.7	2.5	3.3	V
		IF level = −18dBm	3.6	4.8	5.8	V
	RSSI range	$R_9 = 100k\Omega$ Pin 7		80		dB
	RSSI accuracy	$R_9 = 100k\Omega$ Pin 7		±2		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		kΩ
	Unmuted audio output impedance			58		kΩ
	Muted audio output impedance	Test at Pin 18		58		kΩ
RF/IF section (int LO)						
	Unmuted audio level	4.5V = V_{CC}, RF level = −27dBm		480		mV_{RMS}
	System RSSI output	RF level = −27dBm, 4.5V = V_{CC}		4.3		V

NOTE:

1. NE614 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE614 (50)	NE614A (1.5k)/NE615 (1.5k)
−97dBm	−118dBm
−47dBm	−68dBm
+3dBm	−18dBm

The NE615 and NE614 are both derived from the same basic die. The NE615 performance plots are directly applicable to the NE614A.

CIRCUIT DESCRIPTION

The NE/SA615 is an RF/IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz with 39.7dBV of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dBV of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert Cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third order intercept of −10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations, either Hartley or Colpitts. For crystal oscillators, the Colpitts configuration is used up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dBV insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dBV insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength indicator completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

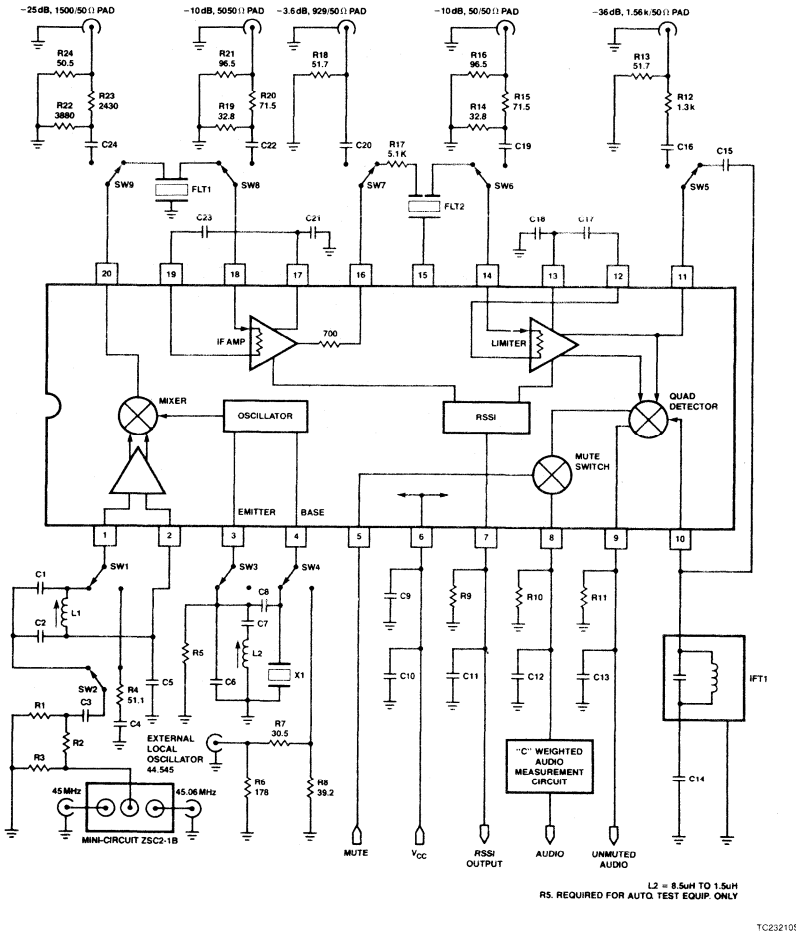
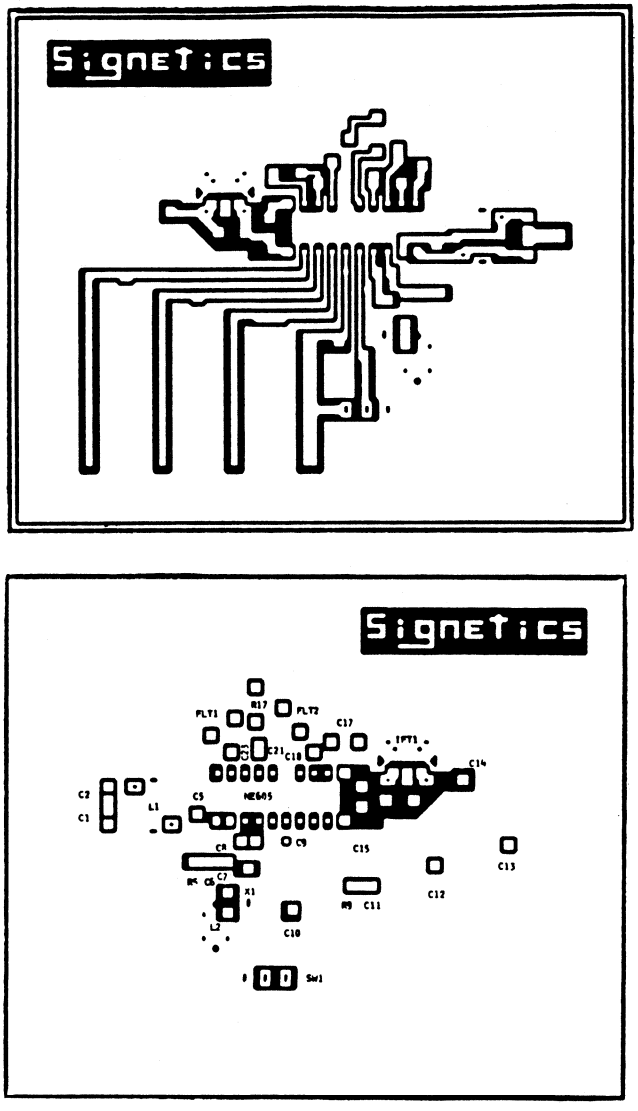


Figure 1. NE/SA615 45MHz Test Circuit and Application Circuit (Relays as shown)

Application Component List

C1 100pF NPO Ceramic
C2 390pF NPO Ceramic
C5 100nF ±10% Monolithic Ceramic
C6 22pF NPO Ceramic
C7 1nF Ceramic
C8 5.6pF NPO Ceramic (minimum)
C9 100nF ±10% Monolithic Ceramic
C10 15μF Tantalum (minimum)
C11 100nF ±10% Monolithic Ceramic
C12 15nF ±10% Ceramic
C13 150pF ±2% N1500 Ceramic
C14 100nF ±10% Monolithic Ceramic
C15 10pF NPO Ceramic
C17 100nF ±10% Monolithic Ceramic
C18 100nF ±10% Monolithic Ceramic
C21 100nF ±10% Monolithic Ceramic
C23 100nF ±10% Monolithic Ceramic
Flt1 Ceramic Filter Murata SFG455A3 or equiv
Flt2 Ceramic Filter Murata SFG455A3 or equiv
IFT1 455kHz (Ce = 180pF) RMC-2A6597H
L1 147-160nH Coilcraft UNI-10/142-04J08S
L2 0.5-1.3μH, 800nH nominal
Coilcraft UNI-10/143-16J12S
Coilcraft SLOTTEN-04-01
Toko 113KN-2K353HM
X1 44.545MHz Crystal ICM4712701
R9 100k ±1% 1/4W Metal Film
R17 5.1k ±5% 1/4W Carbon Composition
R5 Not Used in Application
R10 100k ±1% 1/4W Metal Film (optional)
R11 100k ±1% 1/4W Metal Film (optional)



TC00000S

Figure 2. Layout for NE/SA615 Test and Application Board

AN1991
Audio Decibel Level Detector With Meter Driver

Application Note

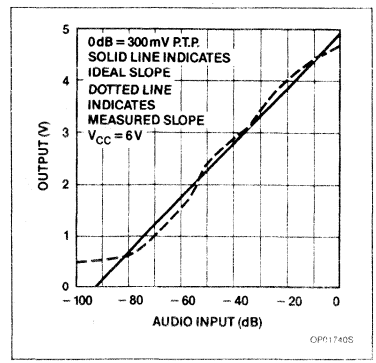
DESCRIPTION

Although the NE604 was designed as an RF device intended for the cellular radio market, it has features which permit other design configurations. One of these features is the Received Signal Strength Indicator (RSSI). In a cellular radio, this function is necessary for continuous monitoring of the received signal strength by the radio's microcomputer. This circuit provides a logarithmic response proportional to the input signal level. The NE604 can provide this logarithmic response over an 80dB range up to a 15MHz operating frequency. This paper describes a technique which optimizes this useful function within the audio band.

A sensitive audio level indicator circuit can be constructed using two integrated circuits: the NE604 and NE532. This circuit draws very little power (less than 5mA with a single 6V power supply) making it ideal for portable battery operated equipment. The small size and low-power consumption belie the 80dB dynamic range and 10.5μV sensitivity.

The RSSI function requires a DC output voltage which is proportional to the $\log_{10}$ of the input signal level. Thus a standard 0 – 5 voltmeter can be linearly calibrated in decibels over a single 80dB range. The entire circuit is composed of 9 capacitors and two resistors along with the two ICs. No tuning or calibration is required in a manufacturing setting.

The Audio Input vs Output Graph shows that the circuit is within 1.5dB tolerance over the 80dB range for audio frequencies from 100Hz to 10kHz. Higher audio levels can be measured by placing an attenuator ahead of the input capacitor. The input impedance is high (about 50k), so lower impedance terminations (50 or 600Ω) will not be affected by the input impedance. If very accurate tracking is required (< 0.5dB accuracy), a 40 or 50dB segment can be "selected". A range switch can then be added with appropriate attenuators if more than 40 or 50dB dynamic range is required.



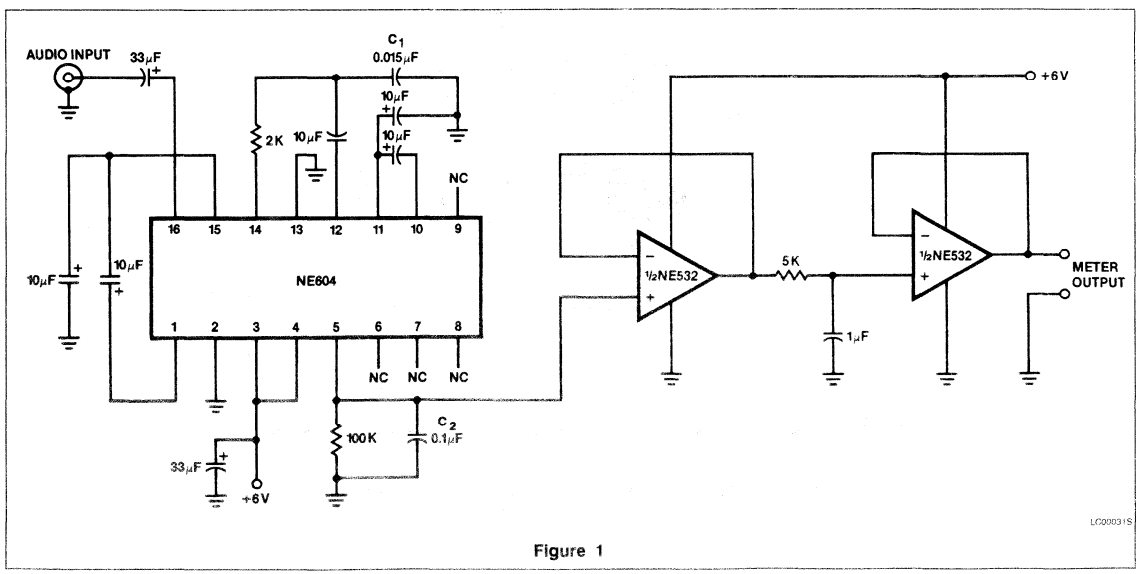


Figure 1

Audio Decibel Level Detector With Meter Driver

AN1991

There are two amplifier sections in the 604 with 2 and 3 stages in the first and second sections respectively. Each stage outputs a sample current to a summing circuit. The summing circuit has a current mirror which appears at Pin 5. This current is proportional to the $\log_{10}$ of the input audio signal. A voltage is dropped across the 100k resistor by the current, and a 0.1μF capacitor is used to bypass and filter the output signal. The 532 op amp is used as a buffer and meter driver, although a digital voltmeter could replace both the op amp and the meter shown. The rest of the capacitors are used for power supply and amplifier input bypassing.

The RC circuit between Pins 14 and 12 forms a low-pass filter which can be adjusted by changing the value of C1. Raising the capacitance will lower the cut-off frequency and also lower the zero signal output resting voltage (about 0.6V). Lowering the capacitance value will have the opposite effect with some reduction in dynamic range, but will raise the frequency response. The 2kΩ resistor value provides the near-ideal inter-stage loss for maximum RSSI linearity. C2 can also be changed. The trade-off here is between output damping and ripple. Most analog and digital metering methods will tend to cancel the effects of small or moderate ripple voltages through integration, but high ripple voltages should be avoided.

A second op amp is used with an optional second filter. This filter has the advantage of a low impedance signal source by virtue of the first op amp. Again, a trade-off exists between meter damping and ripple attenuation. If very low ripple and low damping are both required, a more complex active low-pass filter should be constructed.

Some applications of this circuit might include:

1. Portable acoustic analyzer
2. Microphone tester
3. Audio spectrum analyzer
4. VU meters
5. S-meter for direct conversion radio receiver
6. Audio dynamic range testers
7. Audio analyzers (THD, noise, separation, response, etc.)

AN1992
Using the Signetics MC3361 Demonstration Board

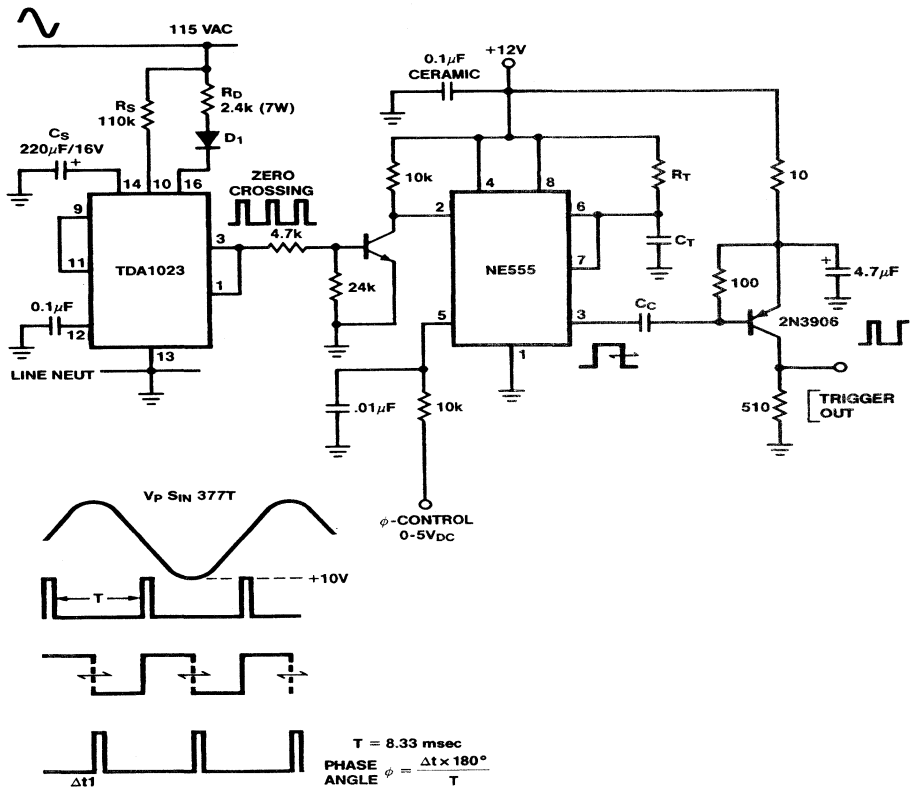
Application Note

INTRODUCTION

Circuit Description

This demo is set up to show the functions of the Signetics MC3361. The MC3361 is a Low Power Narrow-Band FM IF. It is designed for use as the second IF of FM dual conversion communications equipment. The MC3361 includes the following:

- Oscillator
- Mixer
- Limiting amplifier
- Quadrature discriminator
- Active filter
- Squelch
- Scan control
- Mute switch



NOTE:
This is the schematic of the Signetics MC3361 demonstration board. The input and output connections are AC-coupled to protect the device from any DC that may be introduced at the inputs. The supply is capacitively decoupled to ground to help eliminate any AC on the supply line.

Figure 1. Schematic of the Signetics MC3361 Demonstration Board

Using the Signetics MC3361 Demonstration Board

AN1992

The application outlined here does not demonstrate the absolute maximum performance of the Signetics MC3361. It is merely an example given to show the flexibility of the part.

In general, the external components used for each application tend to be the limiting factors in each application. In order to make the demo board suitable for general usage, the Local Oscillator (LO) is supplied externally.

This allows the input frequency to operate anywhere within the limitations of the part. The inputs have not been matched for any one particular frequency.

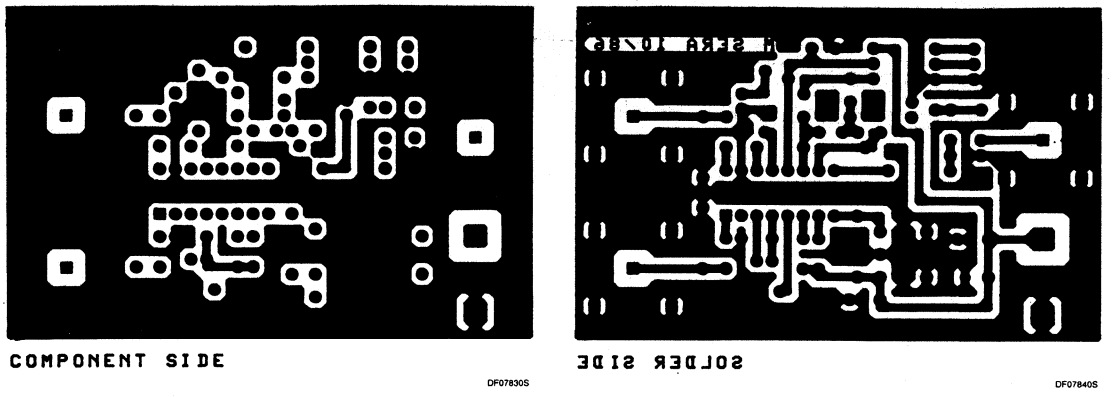


Figure 2. Layout of the Signetics MC3361 Demonstration Board

PARTS LIST

Capacitors

C1	0.1μF
C2	0.1μF
C3	0.1μF
C4	10μF Elect
C5	0.1μF
C6	0.1μF
C7	0.1μF
C8	0.1μF
C9	0.47μF
C10	0.01μF
C11	0.001μF
C12	0.001μF
C13	0.01μF
C14	0.1μF
C15	0.1μF

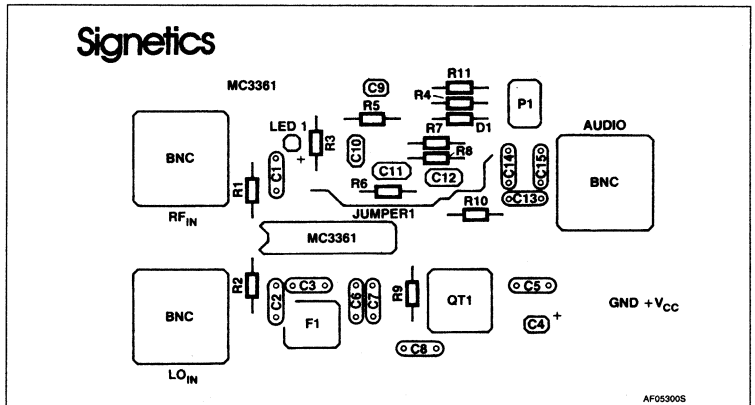


Figure 3. Part Layout for Demonstration Board

Resistors[1]

R1	51	¼ W
R2	51	¼ W
R3	330	¼ W
R4	68k	¼ W
R5	120k	¼ W
R6	390k	¼ W
R7	750	¼ W
R8	18k	¼ W
R9	20k	¼ W
R10	7.5k	¼ W
R11	51k	¼ W

NOTE:
1. All resistors are 5%

Miscellaneous

MC3361	SIGNETICS MC3361
LED1	Red LED
D1	Diode (1N4148)
P1	50k Potentiometer (BOURNS 3299 144C 50K)
Q1	Quad Tank (TOKO RMC 2A6597HK[1])
F1	455kHz Filter (MURUTA CFU455D2[2])
BNC	BNC Connector (KINGS KC-79-232-MO6)

NOTES:
1. TOKO AMERICA INC.
   West Touhy Ave.
   Skokie, IL 60077
   Tel: (213) 677-3640
   CA: (408) 996-7575
2. MURUTA ERIE
   1453 Lincoln Street
   Carlisle, PA 17013
   Tel: (717) 249-2232

Matching the input will increase the sensitivity of the part. See Appendix II for matching network.

LAYOUT

The board layout uses basic RF techniques, i.e., GND on both top and bottom layers, very short input and output lead lengths and wide traces, with decoupling capacitors on the supply lines.

Operation of the MC3361 Demonstration Board

In this application the MC3361 is set up as an FM receiver. The input is mixed with the LO to convert the input signal down to 455kHz. The signal then goes through an external (455kHz) ceramic bandpass filter. Next, the 455kHz signal goes through a limiting amplifier. The audio is finally recovered using an FM demodulator and then amplified by an audio amp.

The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This 'noise band' is monitored by an active filter and a detector. A squelch control circuit mutes the audio output signal when the 'noise band' is above a certain level set by P1. The squelch control circuit also provides a scan control output (Pin 13) which can be used to drive an LED, as we have done on the application board.

DEMONSTRATION BOARD CONNECTIONS AND ADJUSTMENTS

RF_{IN} (RF Input) — An RF signal source with FM content should be connected here. The Maximum frequency is shown on the graph (Figure 2). Set the signal generator to FM and adjust the peak deviation to 3kHz. Set the modulation frequency to 1kHz. The RF amplitude can be varied from as low as 2μV to as high as 1V.

LO_{IN} (Local Oscillator Input) — Should be 455kHz above or below the RF input at approximately 0dBm with *no* deviation. This input is normally configured with a Colpitts crystal oscillator (see Appendix I), but for ease of flexibility we chose to feed the LO externally.

AUDIO (Audio Output) — The audio recovered from the RF signal can be seen at this point. Use an oscilloscope adjusted to trigger at the audio frequency (1kHz). Remember that the RF input must have some FM content in order to see a signal here.

Power Supply — The Signetics MC3361 will operate with a supply voltage as low as 2.0V and up to 8.0V. The demo board will function with a supply voltage as low as 3.5V. The demo board consumes 4.7mA (Mute off) and 8.2mA (Mute on, LED current included) at 5.0V. A regulated supply with at least $+3.5V_{DC}$ should be connected to the $+V_{CC}$ terminal of the board. The same supply's ground should be connected to the GND terminal.

QT1 (Quad Tank) — This is the 'silver can' located near the supply inputs. It has been adjusted at the factory. If it needs to be adjusted, see Testing.

P1 (Potentiometer) — This adjusts the sensitivity of the mute function. This will cause the AUDIO to be muted at varying levels of RF input amplitudes.

The Red LED (Mute ON Indicator) — When lit, the audio signal is muted. P1 (potentiometer located near Audio Out connection) adjusts the mute sensitivity. The sensitivity can be checked by varying the RF input amplitude.

TESTING AND ADJUSTING THE DEMONSTRATION BOARD

Equipment Required

Power Supply: HP 6216A or equivalent

Signal Generator: HP 8640B or equivalent

Signal Generator: HP 8640B or equivalent

Oscilloscope: Philips PM3243 or equivalent

To test the MC3361 demonstration board, you should carefully follow the instructions listed below.

1. Connect a +5V regulated power supply to $+V_{CC}$.
2. Connect the supply ground to GND.
3. Connect #1 Signal Generator to RF_{IN}; note the frequency on the display. Set the signal generator to FM with a peak deviation of 3kHz and a modulation frequency of 1kHz. The amplitude should be adjusted to around −20dBm (22mV_{RMS}).
4. Connect #2 Signal Generator to LO_{IN}, noting the frequency of the #1 Signal Generator connected to RF_{IN}; add or subtract 455kHz from that number and adjust the #2 Signal Generator to this frequency. The amplitude should be set at 0dBm (220mV_{RMS}). Make sure *no* modulation is applied at this input.
5. Connect an oscilloscope to AUDIO. The oscilloscope should trigger off of a signal near 1kHz. The Red LED should not be lit. If the Red LED is lit, adjust P1 until the Red LED turns off.
6. Once all the connections have been made, you should see a clean sine wave on the oscilloscope.
7. Peak the amplitude of the sine wave seen at the AUDIO output by adjusting QT1. This will tune the Quadrature Detector.
8. To test the sensitivity of the circuit, vary the input amplitude of the RF_{IN} signal. The sine wave will start to get noisy around −100dBm. As you decrease the amplitude even more, the 'noise band' will increase, causing the Squelch Control circuit to trigger. When the Squelch Control circuit does trigger, the audio output will go to 0V and the Red LED will be on.
9. The Squelch Control circuit's sensitivity can be controlled by P1. Adjust P1 to trigger at the desired RF input level.
10. The RF_{IN} frequency can also be varied, just as long as the LO_{IN} is 455kHz above or below the RF_{IN} frequency. Figure 4 shows the sensitivity vs. frequency of the demonstration board.

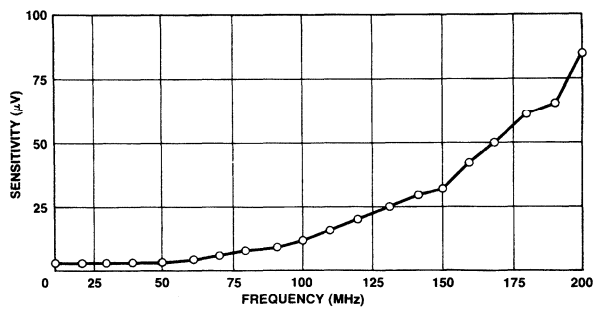


Figure 4. Sensitivity vs Frequency

Using the Signetics MC3361 Demonstration Board

SENSITIVITY VS FREQUENCY

Figure 4 shows the sensitivity of the demonstration board over frequency (V_{CC} = 5.0V). The inputs are 50Ω terminated to suit most inputs. Note that the inputs are not matched for any one frequency; matching the input to one desired frequency will increase the sensitivity.

APPENDIX I

The LO can be supplied using a Colpitts crystal oscillator tuned to the desired frequency. Figure 5 shows a Colpitts crystal oscillator tuned to 10.245MHz, which would accommodate an input of 10.7MHz.

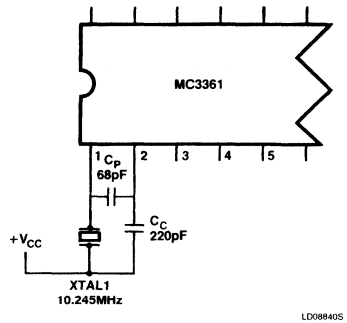


Figure 5. Schematic of a Colpitts Crystal Oscillator

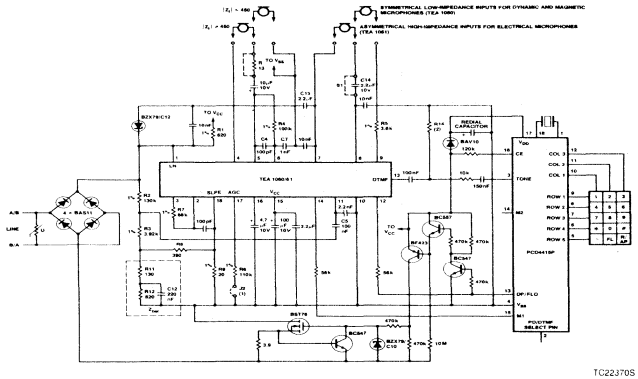
Using the Signetics MC3361 Demonstration Board AN1992

APPENDIX II

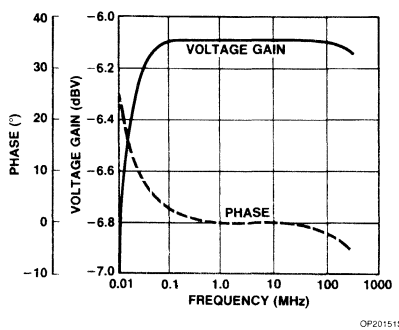
The input has a 50Ω termination resistor for matching the input to most (50Ω) signal sources. This way the device is not limited to any one particular frequency. Figure 6 shows the frequency response of the input as it is on the demonstration board.

Figure 7 uses a matching network tuned to 10MHz. The network is called a capacitor divider. It basically transforms the input impedance to match the device input impedance of 3.3kΩ and 2.2pF at 10MHz. The matched input has an increase gain of 16dBV over the 50Ω termination network.

REF: *Ferromagnetic Core Design Application & Handbook*, Doug DeMaw.

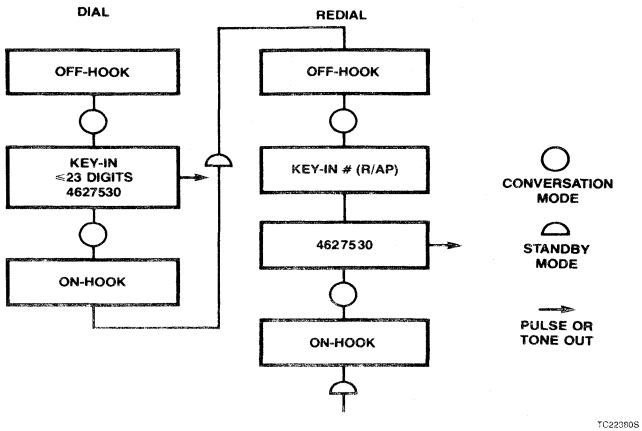


a. Broadband Termination

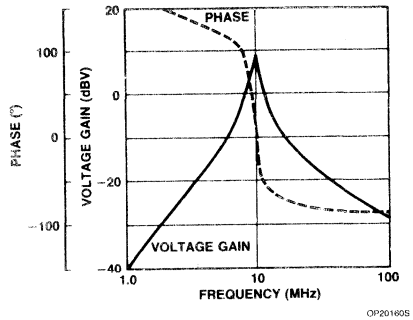


b. Voltage Transfer Ratio With Broadband Termination

Figure 6. Voltage Transfer Ratio of the Demonstration Board



a. Typical Input Matching Network



b. Typical Network Voltage Transfer Ratio Input Matching (at 10.7MHz)

Figure 7

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High Sensitivity Applications of Low-Power RF/IF Integrated Circuits

Application Note

ABSTRACT

This paper discusses four high sensitivity receivers and IF (Intermediate Frequency) strips which utilize intermediate frequencies of 10.7MHz or greater. Each circuit utilizes a low-power VHF mixer and high-performance low-power IF strip. The circuit configurations are

1. 45 or 49MHz to 10.7MHz narrowband,
2. 90MHz to 21.4MHz narrowband,
3. 100MHz to 10.7MHz wideband, and
4. 152.2MHz to 10.7MHz narrowband.

Each circuit is presented with an explanation of component selection criteria, (to permit adaptation to other frequencies and bandwidths). Optional configurations for local oscillators and data demodulators are summarized.

INTRODUCTION

Traditionally, the use of 10.7MHz as an intermediate frequency has been an attractive means to accomplish reasonable image rejection in VHF/UHF receivers. However, applying significant gain at a high IF has required extensive gain stage isolation to avoid instability and very high current consumption to get adequate amplifier gain bandwidth. By enlightened application of two relatively new low power ICs, Signetics NE602 and NE604A, it is possible to build highly producible IF strips and receivers with input frequencies to several hundred megahertz, IF frequencies of 10.7 or 21.4MHz, and sensitivity less than 2μV (in many cases less than 1μV). The Signetics new NE605 combines the function of the NE602 and the NE604A. All of the circuits described in this paper can also be implemented with the NE605. The NE602 and NE604A were utilized for this paper to permit optimum gain stage isolation and filter location.

THE BASICS

First let's look at why it is relevant to use a 10.7 or 21.4MHz intermediate frequency. 455kHz ceramic filters offer good selectivity and small size at a low price. Why use a higher IF? The fundamental premise for the answer to this question is that the receiver architecture is a hetrodyne type as shown in Figure 1.

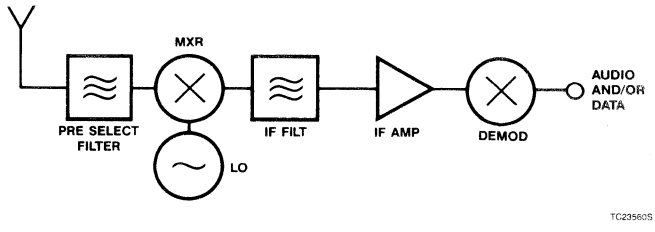


Figure 1. Basic Hetrodyne Receiver

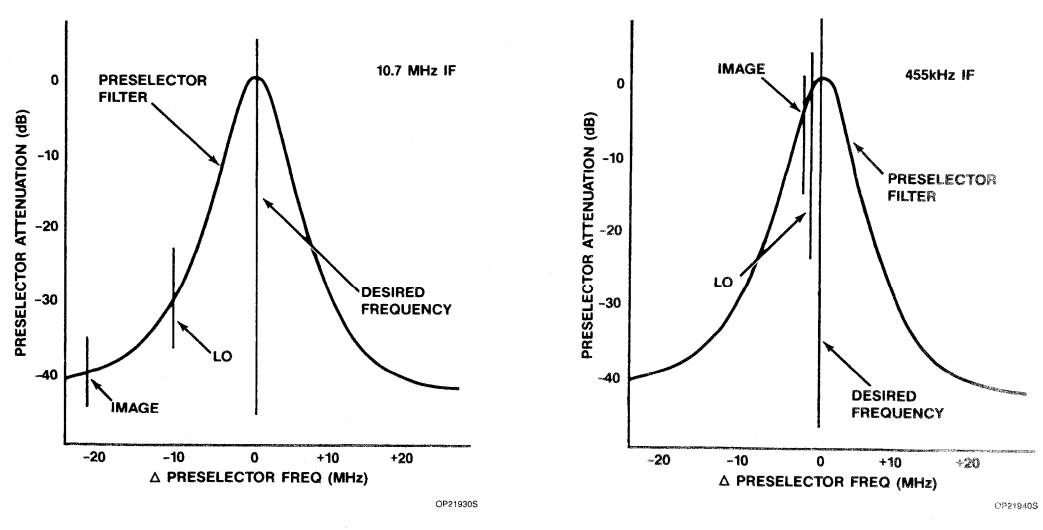


Figure 2. Effects of Preselection on Images

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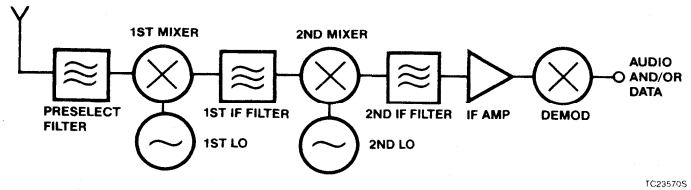


Figure 3. Dual Conversion

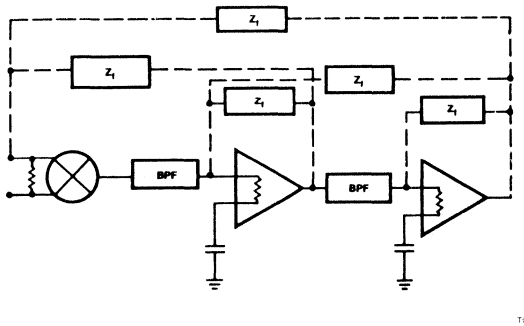


Figure 4. Feedback Paths

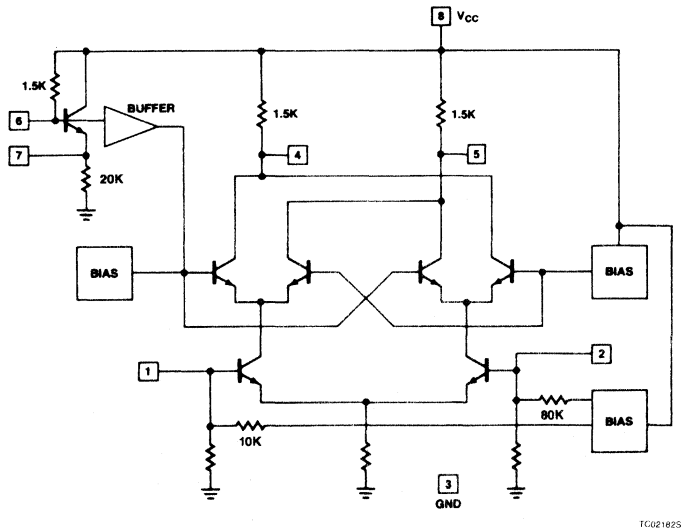


Figure 5. NE602 Equivalent Circuit

A pre-selector (bandpass in this case) precedes a mixer and local oscillator. An IF filter follows the mixer. The IF filter is only supposed to pass the difference (or sum) of the local oscillator (LO) frequency and the preselector frequency.

The reality is that there are always two frequencies which can combine with the LO: The pre-selector frequency and the "image" frequency. Figure 2 shows two hypothetical pre-selection curves. Both have 3dB bandwidths of 2MHz. This type of pre-selection is typical of consumer products such as cordless telephone and FM radio. Figure 2A shows the attenuation of a low side image with 10.7MHz. Figure 2B shows the very limited attenuation of the low side 455kHz image.

If the single conversion architecture of Figure 1 were implemented with a 455kHz IF, any interfering image would be received almost as well as the desired frequency. For this reason, dual conversion, as shown in Figure 3, has been popular.

In the application of Figure 3, the first IF must be high enough to permit the pre-selector to reject the images of the first mixer and must have a narrow enough bandwidth that the second mixer images and the intermod products due to the first mixer can be attenuated. There's more to it than that, but those are the basics. The multiple conversion hetrodyne works well, but, as Figure 3 suggests, compared to Figure 2 it is more complicated. Why, then, don't we use the approach of Figure 2?

THE PROBLEM

Historically there has been a problem: Stability! Commercially available integrated IF amplifiers have been limited to about 60dB of gain. Higher discrete gain was possible if each stage was carefully shielded and bypassed, but this can become a nightmare on a production line. With so little IF gain available, in order to receive signals of less than 10μV it was necessary to add RF gain and this, in turn, meant that the mixer must have good large signal handling capability. The RF gain added expense, the high level mixer added expense, both added to the potential for instabilities, so the multiple conversion started looking good again.

But why is instability such a problem in a high gain high IF strip? There are three basic mechanisms. First, ground and the supply line are potentially feedback mechanisms from stage-to-stage in any amplifier. Second, output pins and external components create fields which radiate back to inputs. Third, layout capacitances become feedback mechanisms. Figure 4 shows the fields and capacitances symbolically.

If Z_F represents the impedance associated with the circuit feedback mechanisms (stray capacitances, inductances and radiated fields), and Z_{IN} is the equivalent input imped-

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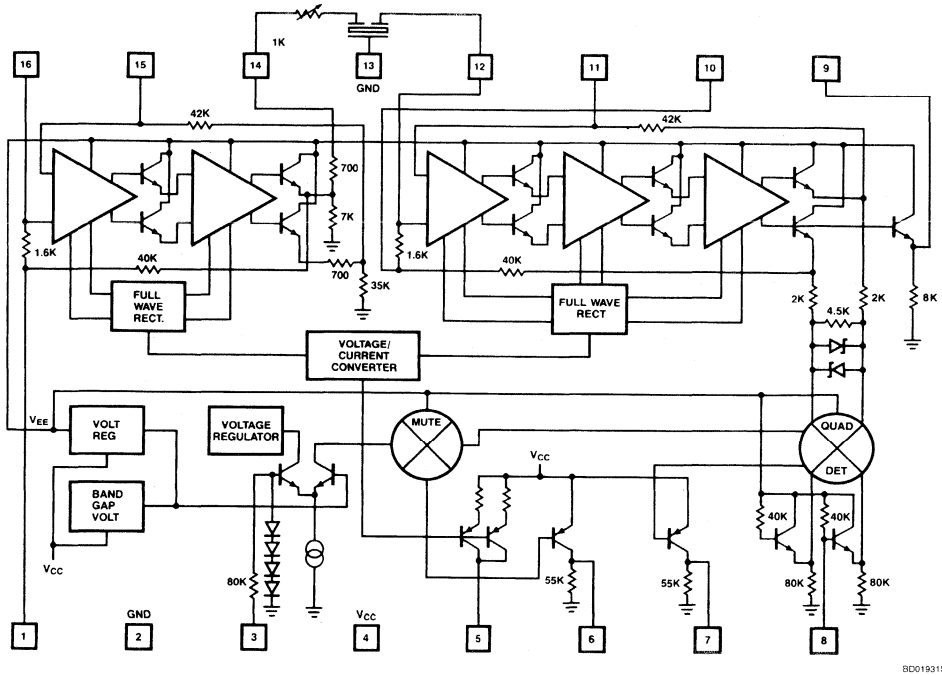


Figure 6. NE604A Equivalent Circuit

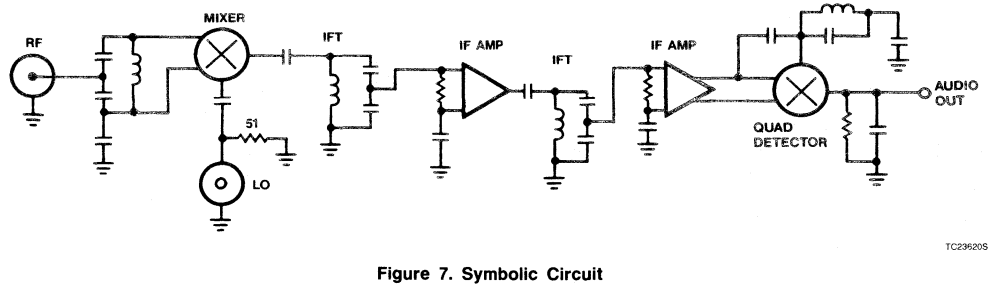


Figure 7. Symbolic Circuit

ance, a divider is created. This divider must have an attenuation factor greater than the gain of the amplifier if the amplifier is to remain stable.

- If gain is increased, the input-to-output isolation factor must be increased.
- As the frequency of the signal or amplifier bandwidth increases, the impedance of the layout capacitance decreases thereby reducing the attenuation factor.

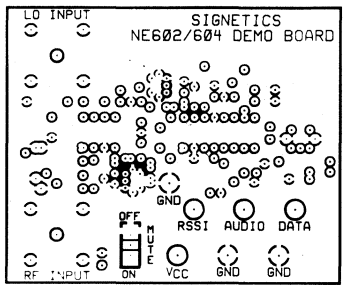
The layout capacitance is only part of the issue. In order for traditional 10.7MHz IF amplifiers to operate with reasonable gain bandwidth, the amount of current in the amplifiers needed to be quite high. The CA3089 operates with 25mA of typical quiescent current. Any currents which are not perfectly differential must be carefully bypassed to ground. The higher the current, the more difficult the challenge. And limiter outputs and quadrature components make excellent field generators which add to the feedback scenario. The higher the current, the larger the field.

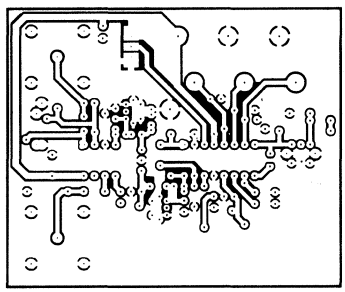
THE SOLUTION

The NE602 is a double balanced mixer suitable for input frequencies in excess of 500MHz. It draws 2.5mA of current. The NE604A is an IF strip with over 100dB of gain and a 25MHz small signal bandwidth. It draws 3.5mA of current. The circuits in this paper will demonstrate ways to take advantage of this low current and 75dB or more of the NE604A gain in receivers and IF strips that would not be possible with traditional integrated circuits. No special tricks are used, only good layout, impedance planning and gain distribution.

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Figure 8. Circuit Board Layout

THE MIXER

The NE602 is a low power VHF mixer with built-in oscillator. The equivalent circuit is shown in Figure 5. The basic attributes of this mixer include conversion gain to frequencies greater than 500MHz, a noise figure of 4.6dB @ 45MHz, and a built-in oscillator which can be used up to 200MHz. LO can be injected.

For best performance with any mixer, the interface must be correct. The input impedance of the NE602 is high, typically 3kΩ in parallel with 3pF. This is not an easy match from 50Ω. In each of the examples which follow, an equivalent 50:1.5k match was used. This compromise of noise, loss, and match yielded good results. It can be improved upon. Match to crystal filters will require special attention, but will not be given focus in this paper.

This oscillator is a single transistor with an internal emitter follower driving the mixer. For best mixer performance, the LO level needs to be approximately 220mV$_{RMS}$ at the base of the oscillator transistor (Pin 6). A number of oscillator configurations are presented at the end of this paper. In each of the prototypes for this paper, the LO source was a signal generator. Thus, a 51Ω resistor was used to terminate the signal generator. The LO is then coupled to the mixer through a DC blocking capacitor. The signal generator is set for 0dBm. The impedance at the LO input (Pin 6) is approximately 20kΩ. Thus, required power is very low, but 0dBm across 51Ω does provide the necessary 220mV$_{RMS}$.

The outputs of the NE602 are loaded with 1.5kΩ internal resistors. This makes interface to 455kHz ceramic filters very easy. Other filter types will be addressed in the examples.

THE IF STRIP

The basic functions of the NE604A are ordinary at first glance: Limiting IF, quadrature detector, signal strength meter, and mute switch. **However, the performance of each of these blocks is superb.** The IF has 100dB of gain and 25MHz bandwidth. This feature will be exploited in the examples. The signal strength indicator has a 90dB log output characteristic with very good linearity. There are two audio outputs with greater than 300kHz bandwidth (one can be muted greater than 70dB). The total supply current is typically 3.5mA. This is the other factor which permits high gain and high IF.

Figure 6 shows an equivalent circuit of the NE604A. Each of the IF amplifiers has a 1.6kΩ input impedance. The input impedance is achieved by splitting a DC feedback bias resistor. The input impedance will be manipulated in each of the examples to aid stability.

BASIC CONSIDERATIONS

In each of the circuits presented, a common layout and system methodology is used. The basic circuit is shown symbolically in Figure 7.

At the input, a frequency selective transformation from 50Ω to 1.5kΩ permits analysis of the circuit with an RF signal generator. A second generator provides LO. This generator second generator provides LO. This generator is terminated with a 51Ω resistor. The output of the mixer and the input of the first limiter are both high impedance (1.5Ω nominal). As indicated previously, the input impedance of the limiter must be low enough to attenuate feedback signals. So, the input impedance of the first limiter is modified with an external resistor. In most of the examples, a 430Ω external resistor was used to create a 330Ω input impedance (430//1.5kΩ). The first IF filter is thus designed to present 1.5kΩ to the mixer and 330Ω to the first limiter.

The same basic treatment was used between the first and second limiters. However, in each of the 10.7MHz examples, this interstage filter is not an L/C tank; it is a ceramic filter. This will be explained in the first example.

After the second limiter, a conventional quadrature detector demodulates the FM or FSK information from the carrier and a simple low pass filter completes the demodulation process at the audio outputs.

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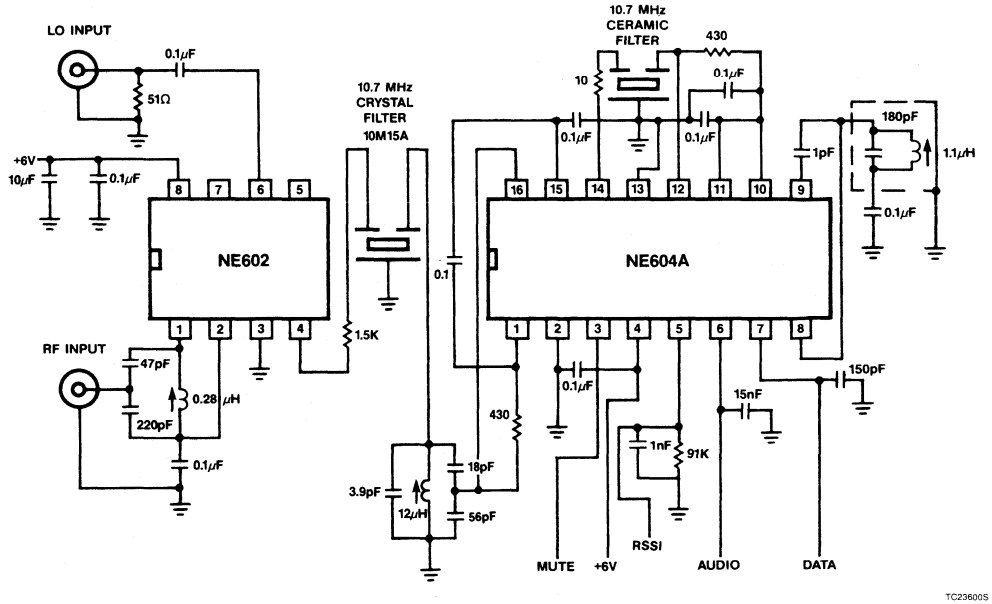


Figure 9. NE602/604A Demonstration Circuit with RF Input of 45MHz and IF of 21.4MHz ± 7.5kHz

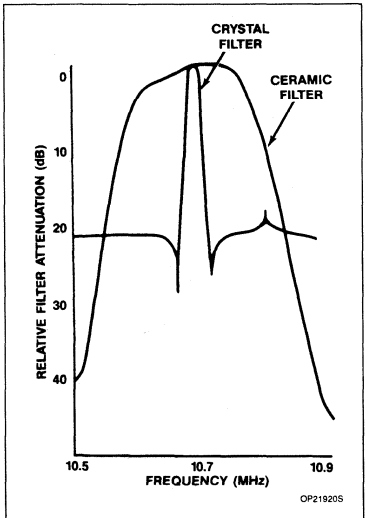
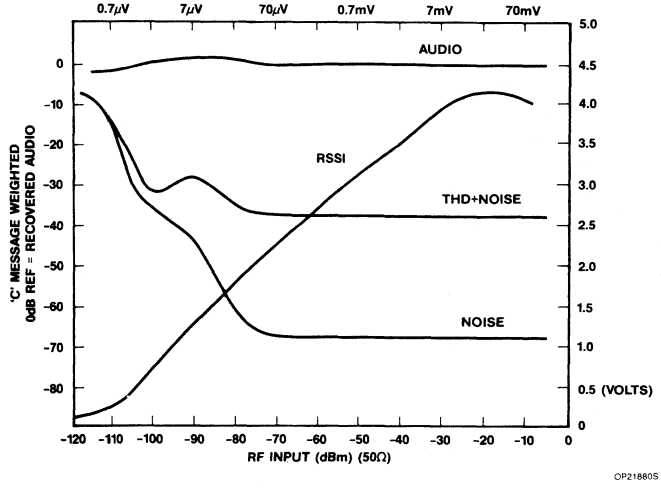


Figure 10. Passband Relationship



- ♦ 45MHz RF Input
- ♦ 55.7MHz LO (0dBm)
- ♦ 10.7MHz IF
- ♦ 15kHz IF BW
- ♦ 7kHz deviation

Figure 11. VHF or UHF 2nd Conversion (Narrow Band)

High Sensitivity Applications of Low-Power RF/IF Integrated Circuits

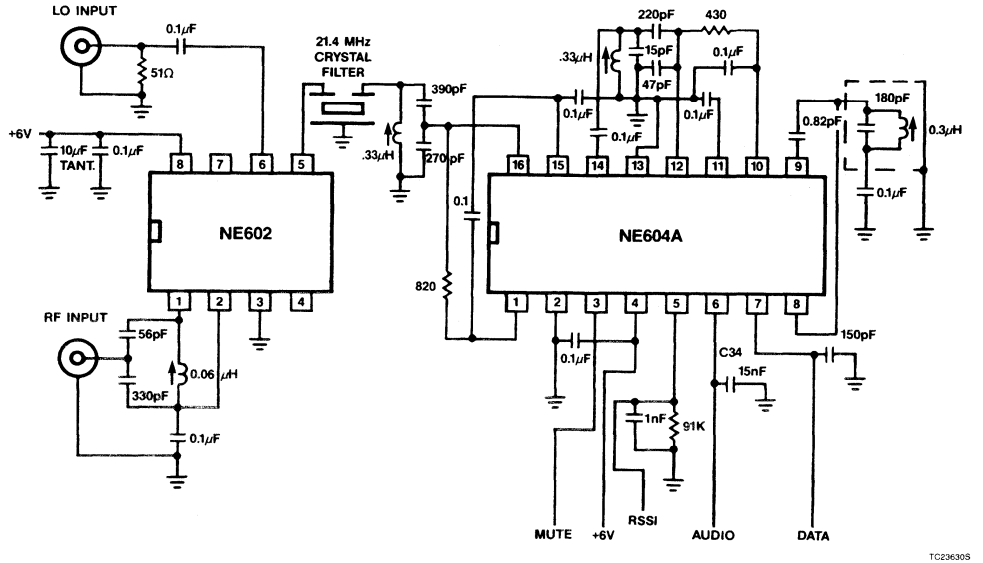


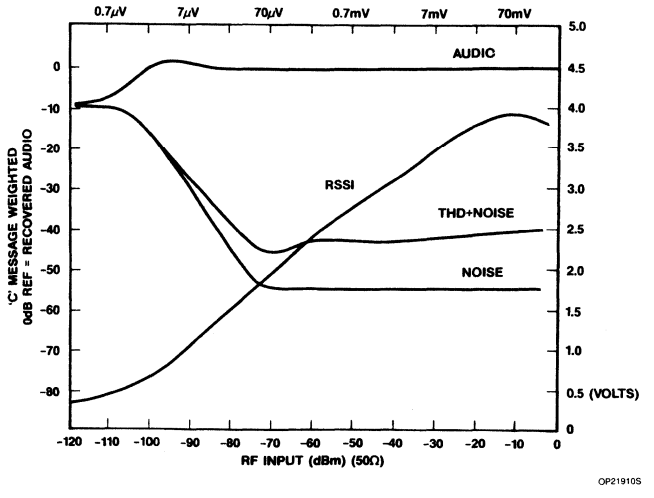
Figure 12. NE602/604A Demonstration Circuit with RF Input of 90MHz and IF of 21.4MHz ± 7.5kHz

As mentioned, a single layout was used for each of the examples. The board artwork is shown in Figure 8. Special attention was given to: (1) Creating a maximum amount of ground plane with connection of the component side and solder side ground at locations all over the board; (2) careful attention was given to keeping a ground ring around each of the gain stages. The objective was to provide a shunt path to ground for any stray signal which might feed back to an input; (3) leads were kept short and relatively wide to minimize the potential for them to radiate or pick up stray signals; finally (and very important), (4) RF bypass was done as close as possible to supply pins and inputs, with a good (10μF) tantalum capacitor completing the system bypass.

EXAMPLE: 45MHz to 10.7MHz NARROWBAND

As a first example, consider conversion from 45MHz to 10.7MHz. There are commercially available filters for both frequencies so this is a realistic combination for a second IF in a UHF receiver. This circuit can also be applied to cordless telephone or short range communications at 46 or 49MHz. The circuit is shown in Figure 9.

The 10.7MHz filter chosen is a type commonly available for 25kHz channel spacing. It has a 3dB bandwidth of 15kHz and a termination requirement of 3kΩ/2pF. To present 3kΩ to the input side of the filter, a 1.5kΩ resistor was used between the NE602 output (which has a 1.5kΩ impedance) and the filter. Layout capacitance was close enough to 2pF that no



- ◆ 90MHz RF Input
- ◆ 68.6MHz LO (0dBm)
- ◆ 21.4MHz IF
- ◆ 15kHz IF BW
- ◆ 7kHz deviation

Figure 13. UHF Second Conversion (Narrow Band) or VHF Single Conversion (Narrow Band)

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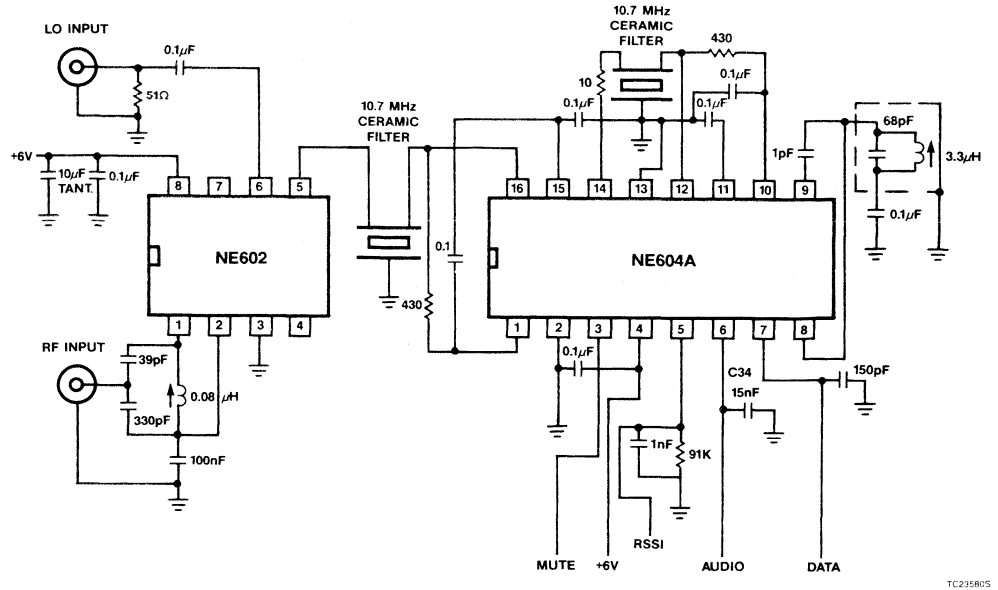


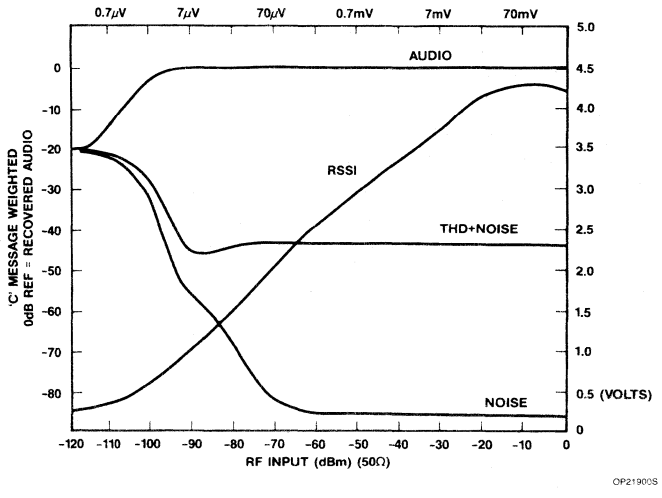
Figure 14. NE602/604A Demonstration Circuit with RF Input of ~ 100MHz and IF of 10.7MHz ± 140kHz

adjustment was necessary. This series-resistance approach introduces an insertion loss which degrades the sensitivity, but it has the benefit of simplicity.

The secondary side of the crystal filter is terminated with a 10.7MHz tuned tank. The capacitor of the tank is tapped to create a transformer with the ratio for 3k:330. With the addition of the 430Ω resistor in parallel with the NE604A 1.6kΩ internal input resistor, the correct component of resistive termination is presented to the crystal filter. The inductor of the tuned load is adjusted off resonance enough to provide the 2pF capacitance needed. (Actual means of adjustment was for best audio during alignment).

If appropriate or necessary for sensitivity, the same type of tuned termination used for the secondary side of the crystal filter can also be used between the NE602 and the filter. If this is desired, the capacitors should be ratioed for 1.5k:3k. Alignment is more complex with tuned termination on both sides of the filter. This approach is demonstrated in the fourth example.

A ceramic filter is used between the first and second limiters. It is directly connected between the output of the first limiter and the input of the second limiter. Ceramic filters act much like ceramic capacitors, so direct connection between two circuit nodes with different DC levels is acceptable. At the input to the second limiter, the impedance is again reduced by the addition of a 430Ω external resistor in parallel with the internal 1.6kΩ input load resistor. This presents the 330Ω



- ♦ 94.7MHz RF Input
- ♦ 84MHz LO (0dBm)
- ♦ 10.7MHz IF
- ♦ 280kHz IF BW
- ♦ 75kHz deviation

Figure 15. FM Broadcast Receiver (Wide Band)

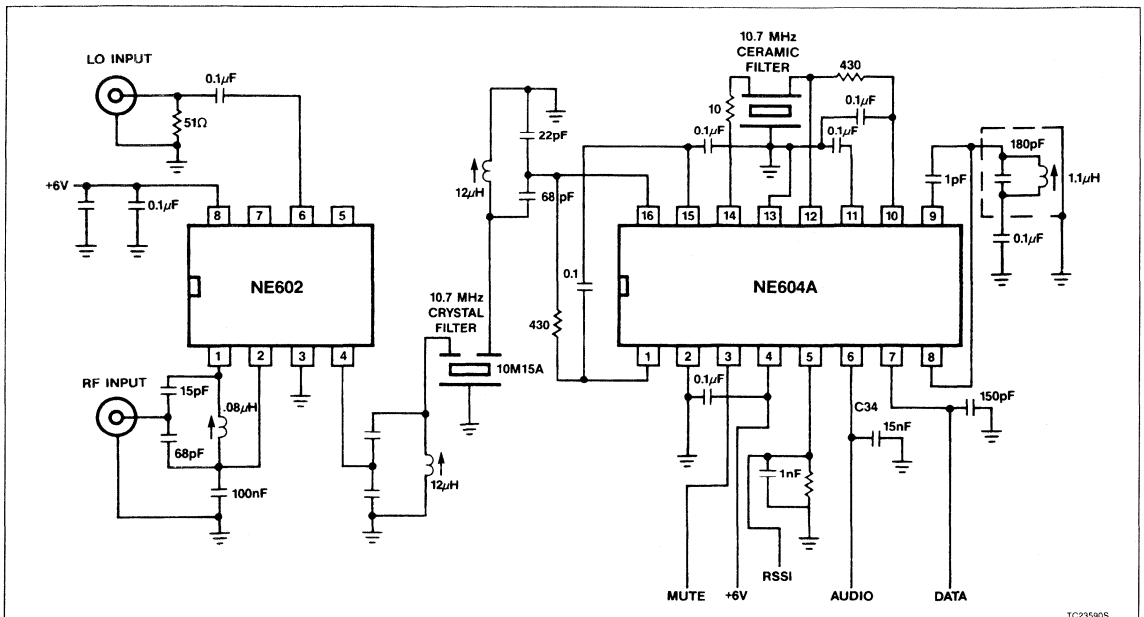
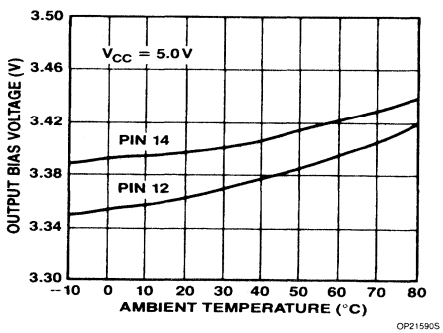


Figure 16. NE602/604A Demonstration Circuit with RF Input of 152.2MHz and IF of 10.7MHz ± 7.5kHz

termination to the ceramic filter which the manufacturers recommend.

On the input side of the ceramic filter, no attempt was made to create a match. The output impedance of the first limiter is nominally 1kΩ. Crystal filters are tremendously sensitive to correct match. Ceramic filters are relatively forgiving. A review of the manufacturers' data shows that the attenuation factor in the passband is affected with improper match, but the degree of change is small and the passband stays centered. Since the principal selectivity for this application is from the crystal filter at the input of the first limiter, the interstage ceramic filter only has to suppress wideband noise. The first filter's passband is right in the center of the ceramic filter passband. (The crystal filter passband is less than 10% of the ceramic filter passband). This passband relationship is illustrated in Figure 10.

After the second limiter, demodulation is accomplished in the quadrature detector. Quadrature criteria is not the topic of this paper, but it is noteworthy that the choice of loaded Q will affect performance. The NE604A is specified at 455kHz using a quadrature capacitor of 10pF and a tuning capacitor of 180pF. (180pF gives a loaded Q of 20 at 455kHz). A careful look at the quadrature equations (Ref 3.) suggests that at 10.7MHz a value of about 1pF should be substituted for the 10pF at 455kHz.



- ◆ 152.2MHz RF Input
- ◆ 141.5MHz LO (0dBm)
- ◆ 10.7kHz IF
- ◆ 15kHz IF BW
- ◆ 7kHz deviation

Figure 17. VHF Single Conversion (Narrow Band)

The performance of this circuit is presented in Figure 11. The −12dB SINAD (ratio of Signal to Noise And Distortion) was achieved with a 0.6μV input.

EXAMPLE: 90MHz to 21.4MHz NARROWBAND

This second example, like the first, used two frequencies which could represent the intermediate frequencies of a UHF receiver. This circuit can also be applied to VHF single conversion receivers if the sensitivity is appropriate. The circuit is shown in Figure 12.

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Most of the fundamentals are the same as explained in the first example. The 21.4MHz crystal filter has a 1.5kΩ/2pF termination requirement so direct connection to the output of the NE602 is possible. With strays there is probably more than 2pF in this circuit, but the performance is good nonetheless. The output of the crystal filter is terminated with a tuned impedance-step-down transformer as in the previous example. Interstage filtering is accomplished with a 1kΩ:330 step-down ratio. (Remember, the output of the first limiter is 1kΩ and a 430Ω resistor has been added to make the second limiter input 330Ω). A DC blocking capacitor is needed from the output of the first limiter. The board was not laid out for an interstage transformer, so an "XACTO" knife was used to make some minor mods. Figure 13 shows the performance. The +12dB SINAD was with 1.6μV input.

EXAMPLE: 100MHz to 10.7MHz WIDEBAND

This example represents three possible applications: (1) low cost, sensitive FM broadcast receivers, (2) SCA (Subsidiary Communications Authorization) receivers and (3) data receivers. The circuit schematic is shown in Figure 14. While this example has the greatest diversity of application, it is also the simplest. Two 10.7MHz ceramic filters were used. The first was directly connected to the output of the NE602. The second was directly connected to the output of the first IF limiter. The secondary sides of both filters were terminated with 330Ω as in the two previous examples. While the filter bandpass skew of this simple single conversion receiver might not be tolerable in some applications, to a first order the results are excellent. (Please note that sensitivity is measured at +20dB in this wideband example.) Performance is illustrated in Figure 15. +20dB SINAD was measured with 1.8μV input.

EXAMPLE: 152.2MHz to 10.7MHz NARROWBAND

In this example (see Figure 16) a simple, effective, and relatively sensitive single conversion VHF receiver has been implemented. All of the circuit philosophy has been described in previous examples. In this circuit, tuned-transformed termination was used on the input and output sides of the crystal filter. Performance is shown in Figure 17. The +12dB SINAD sensitivity was 0.9μV.

OSCILLATORS

The NE602 contains an oscillator transistor which can be used to frequencies greater than 200MHz. Some of the possible configurations are shown in Figures 18 and 19.

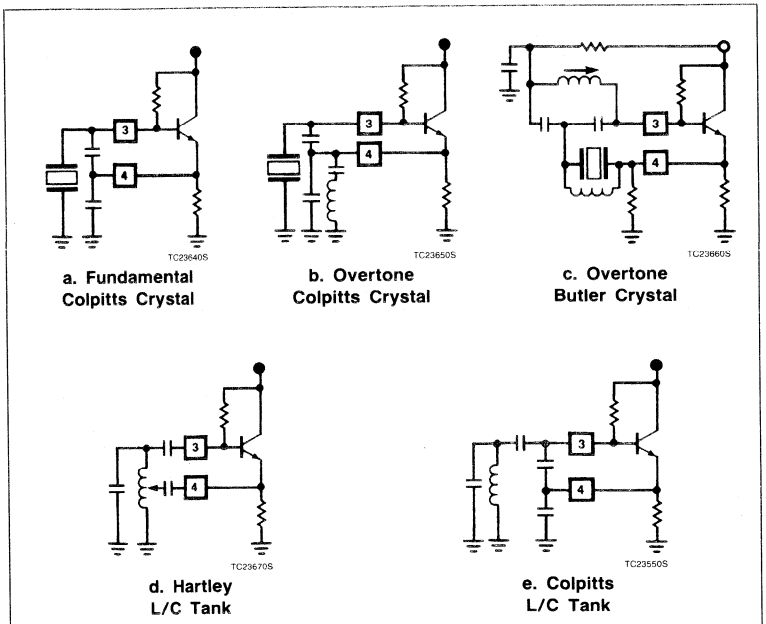


Figure 18. Oscillator Configurations

L/C

When using a synthesizer, the LO must be externally buffered. Perhaps the simplest approach is an emitter follower with the base connected to Pin 7 of the NE602. The use of a dual-gate MOSFET will improve performance because it presents a fairly constant capacitance at its gate and because it has very high reverse isolation.

CRYSTAL

With both of the Colpitts crystal configurations, the load capacitance must be specified. In the overtone mode, this can become a sensitive issue since the capacitance from the emitter to ground is actually the equivalent capacitive reactance of the harmonic selection network. The Butler oscillator uses an overtone crystal specified for series mode operation (no parallel capacitance). It may require an extra inductor (L_o) to null out C_o of the crystal, but otherwise is fairly easy to implement (see references).

The oscillator transistor is biased with only 220μA. In order to assure oscillation in some configurations, it may be necessary to increase transconductance with an external resistor from the emitter to ground. 10kΩ to 20kΩ are acceptable values. Too small a resistance can upset DC bias (see references).

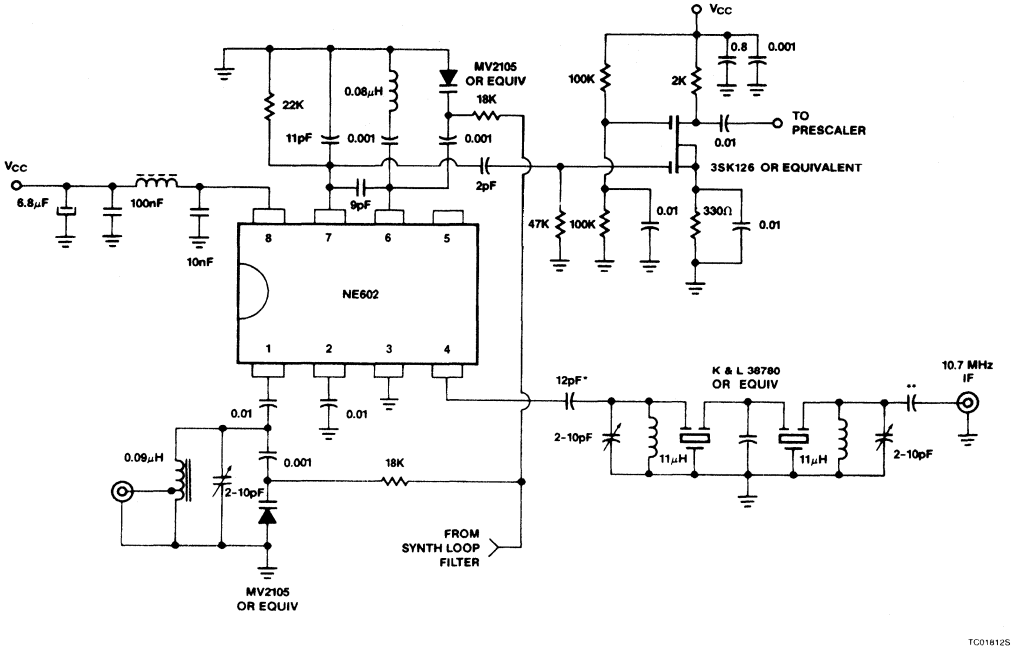
DATA DEMODULATION

It is possible to change any of the examples from an audio receiver to an amplitude shift keyed (ASK) or frequency shift keyed (FSK) receiver or both with the addition of an external op amp(s) or comparator(s). A simple example is shown in Figure 20. ASK decoding is accomplished by applying a comparator across the received signal strength indicator (RSSI). The RSSI will track IF level down to below the limits of the demodulator (−120dBm RF input in most of the examples). When an in-band signal is above the comparator threshold, the output logic level will change.

FSK demodulation takes advantage of the two audio outputs of the NE604A. Each is a PNP current source type output with 180° phase relationship. With no signal present, the quad tank tuned for the center of the IF passband, and both outputs loaded with the same value of capacitance, if a signal is received which is frequency shifted from the IF center, one output voltage will increase and the other will decrease by a corresponding absolute value. Thus, if a comparator is differentially connected across the two out-

High Sensitivity Applications of Low-Power RF/IF Integrated Circuits

puts, a frequency shift in one direction will drive the comparator output to one supply rail, and a frequency shift in the opposite direction will cause the comparator output to swing to the opposite rail. Using this technique, and L/C filtering for a wide IF bandwidth, NRZ data at rates greater than 4Mb have been processed with the new NE605.



* Permits impedance match of NE602 output of 1.8k/8pF to 3.0k filter impedance
* * Choose for impedance match to

Figure 19. Typical Varactor Tuned Application

High Sensitivity Applications of Low-Power RF/IF Integrated Circuits

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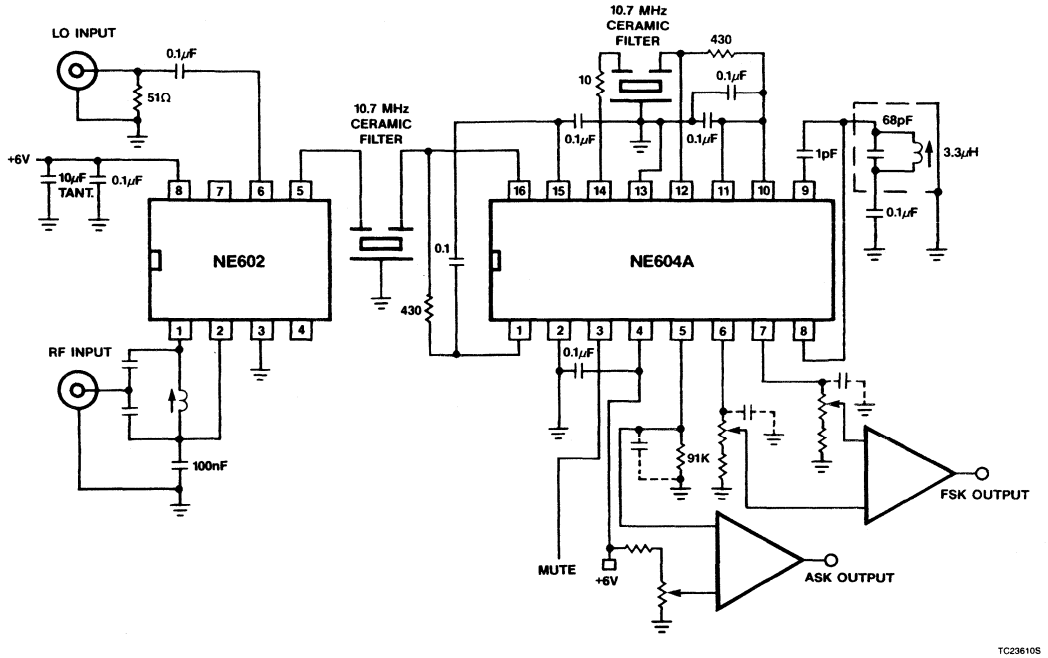


Figure 20. Basic NE602/604A Data Receiver

SUMMARY

The NE602, NE604A and NE605 provide the RF system designer with the opportunity for excellent receiver or IF system sensitivity with very simple circuitry. IFs at 455kHz, 10.7MHz and 21.4MHz with 75 to 90dB gain are possible without special shielding. The flexible configuration of the built-in oscillator of the NE602/605 add to ease of implementation. Either data or audio can be recovered from the NE604A/605 outputs.

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AN177
An Overview of the Phase-Locked Loop (PLL)

Application Note

INTRODUCTION

The basic phase-locked loop (PLL) concept has been known and widely utilized since first being proposed in 1922. Since that time, PLLs have been used in instrumentation, space telemetry, and many other applications requiring a high degree of noise immunity and narrow bandwidth. Techniques and systems involved in these applications frequently are quite complex, requiring a high degree of sophistication. Many of the PLL applications have been at microwave frequencies and employ complex phase shifters, signal splitters, modulation, and demodulation schemes such as biphase and quadraphase. Because of the high frequencies involved in microwave applications, most all components of these PLL systems are made from discrete as opposed to integrated circuits. However, in other communication system applications such as FSK and FM and AM demodulation where frequencies are below approximately 100MHz, monolithic PLLs have found wide application because of their low cost versus high performance.

A block diagram representation of a PLL is shown in Figure 1. Phase-locked loops operate by producing an oscillator frequency to match the frequency of an input signal, f_I. In this locked condition, any slight change in f_I first appears as a change in phase between f_I and the oscillator frequency. This phase shift then acts as an error signal to change the frequency of the local PLL oscillator to match f_I. The locking onto a phase relationship between f_I and the local oscillator accounts for the name phase-locked loop.

A MECHANICAL ANALOG TO THE PLL

To better visualize the frequency and phase relationships in a PLL, consider the mechanical system shown in Figure 2 which is a dual to the electronic PLL. This mechanical system has two identical, heavy disks with two separate center shafts attached to each disk. Each shaft is presumed to be mounted on a bearing that allows each massive disk to be rotated in either direction when some external force is applied. The shafts are coupled together by a spring whose end points are fixed to each shaft. This spring can be twisted in either direction, depending upon the relative positions of the shafts. The spring cannot "kink up" due to the shafts passing through the center of the spring.

Now suppose the sequence of events shown in Figure 3 occurs to the mechanical system. The disks are simply represented like clock faces with positional reference markers. Initially, both disks are stationary in a neutral position. Then the left disk, or input, is advanced slowly clockwise through an angle θ_1 position. The right disk, or output, initially doesn't move as the spring begins to tighten. As the input continues to move and when it reaches θ_2, begins to turn and tracks the input with a positional phase shift error of

$$\theta_e = \theta_2 \qquad (1)$$

At any point in time, with both disks slowly turning at the same speed, there will be some inherent phase error between the disks, or

$$\theta_e = \theta_3 - \theta_4 \qquad (2)$$

This positional phase error in the mechanical system is analogous to the phase error in the electronic PLL. When the input disk coasts to a stop, the output also gradually comes to a stop with a fixed phase error equal to that in Equation 2 or

$$\theta_e = \theta_5 - \theta_6 = \theta_3 - \theta_4 \qquad (3)$$

The spring has a residual stored twist in one direction due to θ_e.

Now consider that the disks are first returned to their neutral positions. Then the input disk is instantaneously rotated through an angle of θ_1 as shown in Figure 4. The output disk can't respond instantaneously because of its large mass. It doesn't move instantaneously and the spring develops considerable torque. Then, as shown in the sequence of events in Figure 4, the output disk begins accelerating after some delay due to the large phase error. It swings past the stopped position of the input disk due to its momentum, reaches a peak overshoot, and gradually ascillates about θ_1 with a damped response, finally coming to rest with some small residual phase error. The input twist of θ_1 represents the application of a step of position or phase to the system, and the response of the output disk is typical for a second-order, underdamped system. This same type of second-order behavior occurs in the PLL system for an instantaneous change of input phase.

As a final example, consider the events in Figure 5 where both disks are rotating at a constant rate. Applying a strobing light (strobotac) simultaneously to both disks and adjusting its flashing rate to one flash per disk rotation will cause the positional markers to appear stationary. There will be a constant phase error in this case just as there was in Figure 3. Now suppose the revolution rate of the input disk gradually increases by a small amount to a new rate. The positional marker will appear to walk around the disk. The output first senses the increased rate of the input through an increase in the phase error.

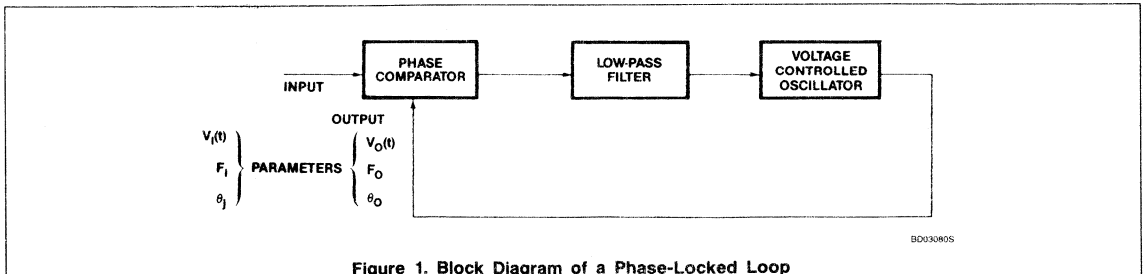


Figure 1. Block Diagram of a Phase-Locked Loop

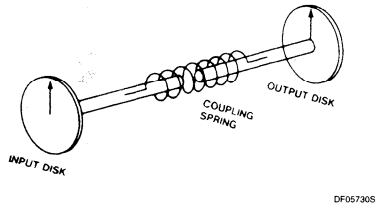


Figure 2. Mechanic Analog to PLL

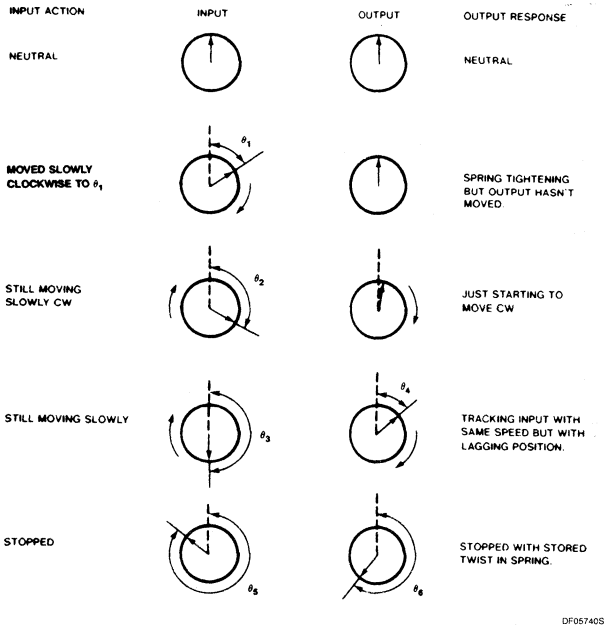


Figure 3. Disk Sequence Showing Output Tracking Input With Phase Error

Then, after some delay, the rate of the output gradually increases to track the input. Both positional markers appear to be walking around each disk at the same rate until the strobotac is adjusted for the higher input and output rate. Then the strobe light again freezes the markers, producing a phase error at this higher rate that is larger than before the input rate was increased. This gradual increase in the input rate to the mechanical system simulates a ramp change in the input frequency to the PLL system. The response to the output disk simulates the behavior of the oscillator in the PLL.

If the rate of the input disk is alternately increased and decreased by some small amount compared to the nominal revolution rate, the positional markers will appear to walk both clockwise and counter clockwise, momentarily appearing stationary when the strobing light rate equals the disk revolution rate. This "walking" represents a changing phase error which is occurring at the modulation rate. Thus the phase error can be thought of as a useable demodulated output signal.

The disk-spring mechanical system is a helpful analog for visualizing frequency, phase, transient, and steady-state responses in the electronic phase-locked loop system. In this example, the positions of the disk marker and rotation rates are analogous to phase and frequency in the electronic PLL system. The spring acts as a phase comparator to constantly sense the relative positions or phases of the disks. The torque developed in this spring acts as the driving force or input signal to turn the second disk.

Thus the spring torque simulates a voltage which controls the rate or frequency of the output disk or oscillator. Hence the second disk is analogous to a voltage-controlled oscillator (VCO). The large mass of the disks together with their angular momentum slows down the systems response time and simulates a low-pass filter in the electronic PLL system. This describes the lagging of the VCO free-running frequency to the input signal in an analog phase-locked loop.

EXAMPLES OF PLL APPLICATIONS

Now consider the action of the voltage-controlled oscillator, phase comparator and low pass filter in the PLL. The VCO generates a signal that is periodic. Normally, the rate or frequency of the VCO is primarily determined by the value of a capacitance connected to this oscillator. This action of starting the VCO running by itself is analogous to disconnecting the spring from one of the shafts in the mechanical system and starting the output disk rotating at a constant rate through some external means such as a motor. In the PLL system this frequency is called the oscillator's free running frequency, (f_O'), because it occurs when the system is unlocked and there is no coupling between input and output frequencies. With the PLL, the VCO frequency can be shifted above and below f_O' by applying a voltage to the optional fine tune input.* This signal generator property is just one of the many uses of the PLL. Specifically with integrated circuit PLLs, frequency ranges from less than 1.0Hz to more than 50MHz can be produced just by selecting the right value of capacitance from a chart on the data sheet.

Selecting f_O' and then changing it by a control voltage makes the VCO well suited for converting digital data that is represented by two different voltage levels into two different frequencies. A "1" voltage level can be related to a frequency called a mark, and an "0" level to a frequency called a space. This technique, called frequency shift keying, or (FSK), is typical of data being transmitted over telephone and radio links where it is impractical to use DC voltage level shifts. Essentially this is what a modem (modulator-demodulator) does as it converts data to tones to go out of the system into a transmission link. Then it reverses the process and converts received tones to "1"s and "0"s at the receiver for the system to use. Sometimes confusion arises because different

*Some oscillators have frequencies controlled by an input current rather than a voltage and are referred to as current-controlled oscillators (CCO).

names are used for the same thing. For example,

A shift up in frequency = "1" = Mark
A shift down in frequency = "0" = Space

If voice or music is applied to the VCO instead of digital data, the oscillator's frequency will move or modulate with the voice or music. This is frequency modulation (FM) and is simply moving the frequency in relation to some input voltage which represents intelligence. Of course, as in the modem case, the process has to be reversed and the PLL can do this also. The PLL is a complete working system that can be used to send and receive signals. In fact the PLL can create the signal, or select a signal, decode it and reproduce it. Now let's look at how this works.

The VCO is connected to a section where its frequency is put together with an incoming signal or signals. In a radio this is known as a "mixer" where signals are mixed together. In a PLL it is usually called a *Phase Comparator.* Other names for this function are *phase detector* or *multiplier* — either analog or digital. (Differences between analog and digital phase comparators will be explained later in this chapter.) The purpose of this phase comparator is to produce an output which represents how far the VCO frequency is from that of the incoming signal. Comparing these frequencies and producing an error signal proportional to their difference allows the VCO frequency to shift from f_O' and become the same frequency as the input signal. This is exactly what happens with the VCO frequency — first "capturing" the input frequency, and then locking onto it. A similar type of action can be visualized in the mechanical system by having the coupling spring disconnected at one end with the two disks rotating at different rates. When their rotation rates are approximately equal, the spring is suddenly connected, and the output disk's speed will gradually become equal to and track the inputs rate as in Figure 5.

When the VCO shifts frequency and locks to the input, the signal frequency is duplicated. If the input signal contains static or noise, the VCO output will be an exact reproduction of the signal frequency without the static or noise. Thus the PLL has accomplished signal reconditioning or reconstitution.

The error signal used to keep the VCO exactly synchronized with an incoming signal can be amplified, filtered, and used to "clock" the signal or give synchronizing information necessary to look at the signal. For example, in some digital memories and transmission systems, data are stored in a code and looked at or strobed at a rate which must be synchronized to the data. This strobing may be at twice or one-half the data rate. By setting f_O' equal to twice or one-half the data rate, the PLL will lock to the data and give an exact synchronized clock. This shows another application of the PLL for multiplying or dividing frequencies.

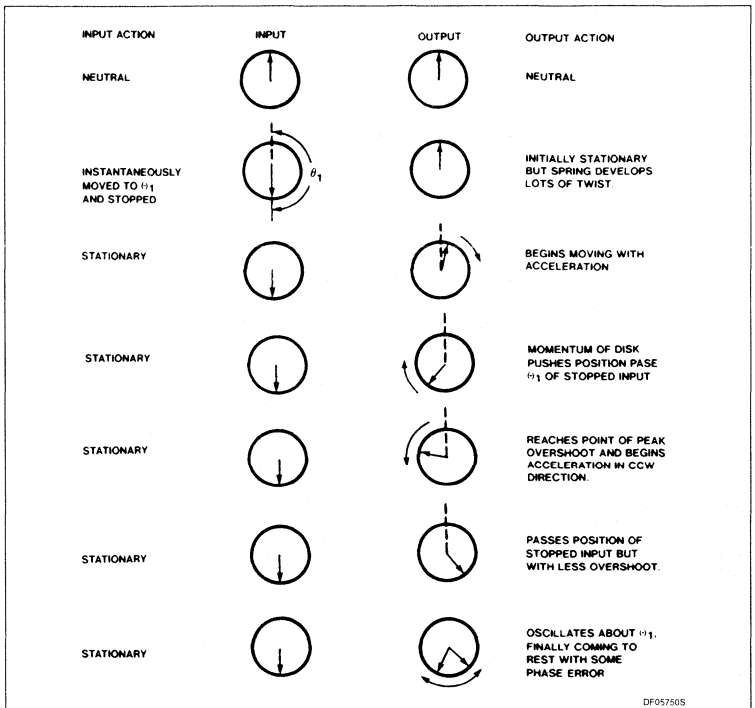


Figure 4. Disk Sequence Showing Ouput Response to a Sudden Position Input

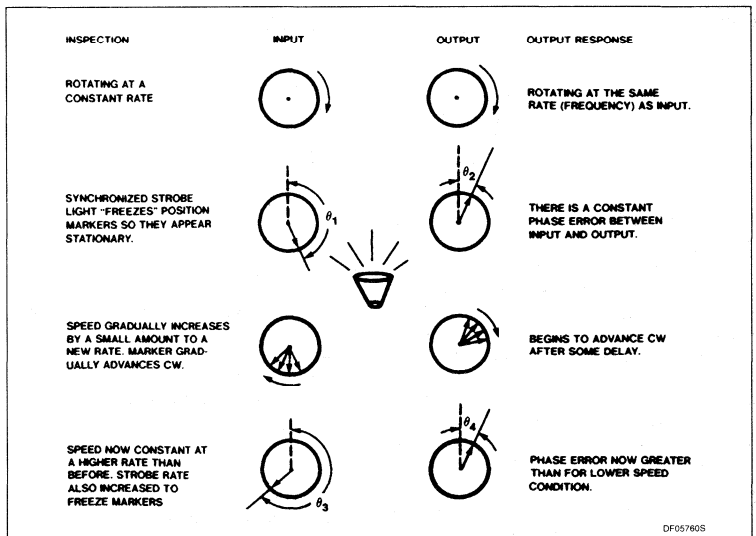


Figure 5. Disk Sequence Showing Output Behavior Due to Changes in Input Speed

An Overview of the Phase-Locked Loop (PLL)

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PLLs can separate a signal of one frequency from among many others as, for example, is done in television and radio reception. This selectivity or capture range is controlled in the PLL by the low-pass filter (LPF) which allows the PLL to only see signals close to the frequency of interest. The time constant of the LPF is set easily by the selection of a resistor and capacitor network. This network determines how far away in frequency an input signal can be from f_O' and still permit the PLL to respond and capture. Once locking is activated, the PLL system will continue to track the input frequency unless the instantaneous phase error exceeds the system's capability.

The error signal which drives the VCO and keeps the system locked is a usable output. In the FSK example the oscillator's frequency is shifted with each "1" or "0" digital input. Converting these frequency shifts back to the "1" and "0" signals automatically occurs in a PLL because a mark input generates an error signal to move the VCO up to that frequency. When the mark changes to a space, the error signal jumps suddenly down, forcing the VCO to follow. The error signal then is exactly the data that generated the FSK signals. *A PLL for FSK can convert data to tones for transmission to a remote point. Then another PLL can reconvert the data tones back to voltage levels, all without tuned circuits.*

The PLL system decodes FM signals in a similar way. The frequency variations caused by voltages from a microphone into one VCO serve as the input signal to another PLL, which reverses the action since the error signal driving the second PLL's VCO is exactly the same as the original microphone voltage.

Decoding of an amplitude-modulated (AM) input signal is another application of the PLL. This application is more involved than FM demodulation because a phase shift network, a second-phase comparator, and another low-pass filter are required. This application is discussed in detail later. However, it should be pointed out that AM demodulation with PLLs offers improved system linearity than the more commonly employed technique of nonlinear diode detection. Tone decoding is a special case of AM demodulation. When performed with PLLs, the second-phase comparator is called a quadrature-phase detector (QPD). The QPD produces a maximum output error voltage whenever the input and oscillator frequencies are locked to the free-running frequency, f_O', unlike the regular phase comparator which has a nominal zero error voltage under this same condition.

These application examples show that with the PLL, a system can:

1. Generate a signal
2. Modulate a signal (encode)
3. Select a signal from among many
4. Demodulate (decode)
5. Recreate (reconstitute) a signal frequency with reduced noise
6. Multiply and divide frequency

TYPES OF PLLS

Generally speaking, the monolithic PLLs can be classified into two groups — digital and analog. While both perform as PLLs, the digital circuits are more suitable for synchronization of digital signals, clock recovery from encoded digital data streams, and other digital applications. Analog monolithic PLLs are used quite extensively in communication systems since they maintain linear relationships between input and output quantities.

The phase comparator is perhaps the most important part of the PLL system since it is here that the input and VCO frequencies are simultaneously compared. Some digital PLLs employ a two-input Exclusive-OR gate as the phase comparator. When the digital loop is locked to f_O', there is an inherent phase error of 90° that is represented by asymmetry in the output waveform. Also, the phase comparator's output has a frequency component of twice the reference frequency. Because of the large logic voltage swings in digital systems, extensive filtering must be performed to remove the harmonic frequencies. For this reason, other types of digital phase comparators achieve locking by synchronizing the "edges" of the input and VCO frequency waveshapes. The phase comparator produces an error voltage that is proportional to the time difference between the edges; i.e., the phase error. This edge-triggering technique for the phase comparator produces lower output noise than with the Exclusive-OR approach. However, time jitter on the input and VCO frequencies is translated into phase error jitter that may require additional filtering within the loop.

Triggering on the edges of digital signals means that only frequency (or period) is important and not duty cycle. This is a key consideration in PLL applications utilizing counters where waveshapes usually aren't symmetrical; i.e., 50% duty cycle. For the TTL family, it is easier to provide the edge matching function on the falling edges ("1" to "0") transition of the waveform. CMOS, I^2L, and ECL are better suited for leading edge triggering ("0" to "1").

Analog PLLs utilize a phase comparator which functions as a four-quadrant analog multiplier to mix the input and VCO signals. Since this mixing is true analog multiplication, the phase comparator's output is a function of input and VCO signal amplitudes, frequencies, phase relationships, and duty cycles. The inherent linearity afforded by this analog multiplication makes the monolithic analog PLL well suited for many general purpose and communication system applications.

Another way of distinguishing between digital and analog phase comparators is by thinking of the similarities and differences between voltage comparators and operational amplifiers. Voltage comparators are specially designed for digital applications where response time between output levels has been minimized at the expense of system linearity. Feedback is seldom used to maintain linear system relationships, with the comparator normally running open-loop. Op amps, on the other hand, are designed for a linear input-output relationship, with negative feedback being employed to further improve the system linearity.

PLL TERMINOLOGY

The following is a brief glossary of frequently encountered terms in PLL literature.

Free-running Frequency (f_O', ω_O') — Also called the *center frequency,* this is the frequency at which the loop VCO operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f_O and ω_O which are used for the general oscillator frequency. (Many references use f_O and ω_O for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context.) The appropriate units for f_O' and ω_O' are Hz and radians per second, respectively.

Lock Range ($2f_L$, $2\omega_L$)* — The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency, unless there is some nonlinearity in the system which limits the frequency deviation on one side of f_O'. The deviations from f_O' are referred to as the *Tracking Range* or *Hold-in Range.* (See Figure 6). The tracking range is therefore one-half of the lock range.

Capture Range ($2f_C$, $2\omega_C$) —** Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The capture range also is centered at f_O' with the equal deviations called the *Lock-in* or

Pull-in Ranges. The capture range can never exceed the lock range.

Lock-up Time (t_L)* — The transient time required for a free-running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the low-pass filter. *The lock-up time is inversely proportional to the selectivity bandwidth.* Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

Phase Comparator Conversion Gain (K_d) — The conversion constant relating the phase comparator's output voltage to the phase difference between input and VCO signals when the loop is locked. At low input signal levels, K_d is also a function of signal amplitude. K_d has units of volts per radian (V/rad).

VCO Conversion Gain (K_O) — The conversion constant relating th e oscillator's frequency shift from f_O' to the applied input voltage. K_O has units of radians per second per volt (rad/sec/V). K_O is a linear function of ω_O' and must be obtained using a formula or graph provided or experimentally measured at the desired ω_O'.

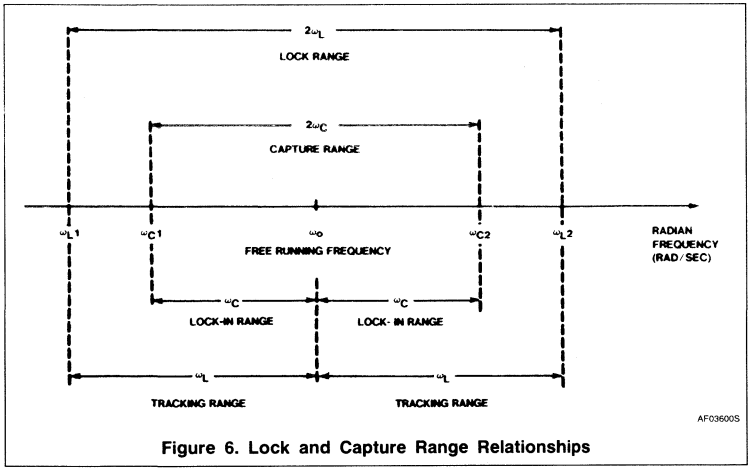


Figure 6. Lock and Capture Range Relationships

Loop Gain (K_V) — The product of K_d, K_O, and the low-pass filters gain at DC. K_d is evaluated at the appropriate input signal level and K_O at the appropriate ω_O'. K_V has units of $(sec)^{-1}$.

Closed-Loop Gain (CLG) — The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by

$$CLG = \frac{K_V}{1 + K_V} \quad (4)$$

Natural Frequency (ω_n) — The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f_O' and at which the phase error swing is the greatest.

Damping Factor (ζ) — The standard damping constant of a second order feedback system. For the PLL, ζ refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

Loop Noise Bandwidth (B_L) — A loop property relating ω_n and ζ which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

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NOTES:
* Also called Synchronization Range.
** Also called Acquisition Range.
***Also called Acquisition Time.

AN178
Modeling the PLL

Application Note

INTRODUCTION

The phase-locked loop is a feedback system comprised of a phase comparator, a low-pass filter and an error amplifier in the forward signal path and a voltage-controlled oscillator (VCO) in the feedback path. The block diagram of a basic PLL system is shown in Figure 1. Perhaps the single most important point to realize when designing with the PLL is that it is a feedback system and, hence, is characterized mathematically by the same equations that apply to other, more conventional feedback systems. However, the parameters in the equations are somewhat different since the feedback error signal in the phase locked system is a phase rather than a current or voltage signal, as is usually the case in conventional feedback systems.

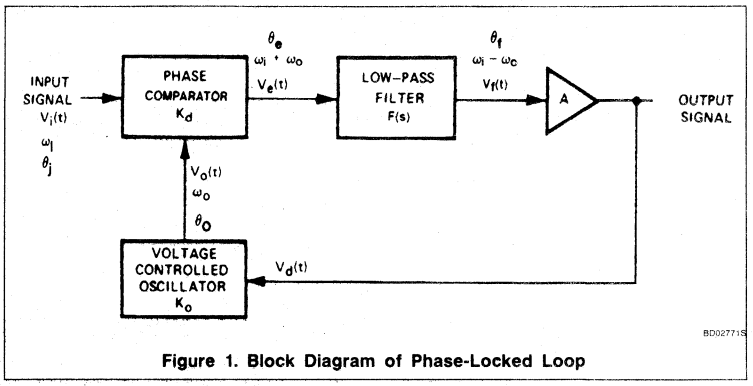


Figure 1. Block Diagram of Phase-Locked Loop

PHASE-LOCKED LOOP OPERATION

The basic principle of the PLL operation can be briefly explained as follows:

With no signal input applied to the system, the VCO control voltage $V_d(t)$ is equal to zero. The VCO operates at a set frequency, f_O' (or the equivalent radian frequency ω_O') which is known as the free-running frequency. When an input signal is applied to the system, the phase comparator compares the phase and the frequency of the input with the VCO frequency and generates an error voltage $V_e(t)$ that is related to the phase and the frequency difference between the two signals. This error voltage is then filtered, amplified, and applied to the control terminal of the VCO. In this manner, the control voltage $V_d(t)$ forces the VCO frequency to vary in a direction that reduces the frequency difference between ω_O and the input signal. If the input frequency ω_I is sufficiently close to ω_O, the feedback nature of the PLL causes the VCO to synchronize or lock with the incoming signal. Once in lock, the VCO frequency is identical to the input signal except for a finite phase difference.

This net phase difference of θ_e where

$$\theta_e = \theta_o - \theta_i \qquad (1)$$

is necessary to generate the corrective error voltage V_d to shift the VCO frequency from its free-running value to the input signal frequency ω_I and thus keep the PLL in lock. This self-correcting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked. The range of frequencies over which the PLL can maintain lock with an input signal is defined as the "lock range" of the system. The band of frequencies over which the PLL can acquire lock with an incoming signal is known as the "capture range" of the system and is never greater than the lock range.

Another means of describing the operation of the PLL is to observe that the phase comparator is in actuality a multiplier circuit that mixes the input signal with the VCO signal. This mix produces the sum and difference frequencies $\omega_I \pm \omega_O$ shown in Figure 1. *When the loop is in lock,* the VCO duplicates the input frequency so that the difference frequency component $(\omega_I - \omega_O)$ is zero; *hence, the output of the phase comparator contains only a DC component.* The low-pass filter removes the sum frequency component $(\omega_I + \omega_O)$ but passes the DC component which is then amplified and fed back to the VCO. Notice that when the loop is in lock, the difference frequency component is always DC, so the lock range is independent of the band edge of the low-pass filter.

LOCK AND CAPTURE

Consider now the case where the loop is not yet in lock. The phase comparator again mixes the input and VCO signals to produce sum and difference frequency components. However, the difference component may fall outside the band edge of the low-pass filter and be removed along with the sum frequency component. If this is the case, no information is transmitted around the loop and the VCO remains at its initial free-running frequency. As the input frequency approaches that of the VCO, the frequency of the difference component decreases and approaches the band edge of the low-pass filter. Now some of the difference component is passed, which tends to drive the VCO towards the frequency of the input signal. This, in turn, decreases the frequency of the difference component and allows more information to be transmitted through the low-pass filter to the VCO. This is essentially a positive feedback mechanism which causes the VCO to snap into lock with the input signal. With this mechanism in mind, the term "capture range" can again be defined as '*the frequency range centered about the VCO initial free-running frequency over which the loop can acquire lock with the input signal*'. The capture range is a measure of how close the input signal must be in frequency to that of the VCO to acquire lock. The "capture range" can assume any value within the lock range and depends primarily upon the band edge of the low-pass filter together with the closed-loop gain of the system. It is this signal capturing phenomenon which gives the loop its frequency-selective properties.

It is important to distinguish the "capture range" from the "lock range" which can, again, be defined as '*the frequency range usually centered about the VCO initial free-running frequency over which the loop can track the input signal once lock has been achieved*'.

When the loop is in lock, the difference frequency component at the output of the phase comparator (error voltage) is DC and will always be passed by the low-pass filter. Thus, the lock range is limited by the range of

error voltage that can be generated and the corresponding VCO frequency deviation produced. The lock range is essentially a DC parameter and is not affected by the band edge of the low-pass filter.

THE CAPTURE TRANSIENT

The capture process is highly complex and does not lend itself to simple mathematical analysis. However, a qualitative description of the capture mechanism may be given as follows. Since frequency is the time derivative of phase, the frequency and the phase errors in the loop can be related as

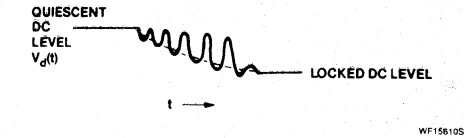
$$\Delta\omega = \frac{d\theta_e}{dt} \qquad (2)$$

where $\Delta\omega$ is the instantaneous frequency separation between the signal and VCO frequencies and θ_e is the phase difference between the input signal and VCO signals.

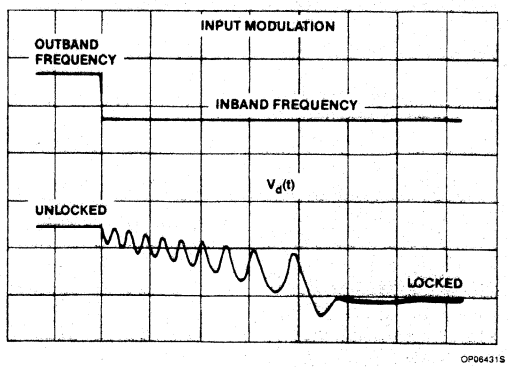
If the feedback loop of the PLL were opened between the low-pass filter and the VCO control input, then for a given condition of ω_O and ω_I the phase comparator output would be a sinusoidal beat note at a fixed frequency $\Delta\omega$. If ω_I and ω_O were sufficiently close in frequency, this beat note would appear at the filter output with negligible attenuation.

Now suppose that the feedback loop is closed by connecting the low-pass filter output to the VCO control terminal. The VCO frequency will be modulated by the beat note. When this happens, $\Delta\omega$ itself will become a function of time. If, during this modulation process, the VCO frequency moves closer to ω_I (i.e., decreasing $\Delta\omega$), then $\frac{d\theta_e}{dt}$ decreases and the output of the phase comparator becomes a slowly varying function of time. Similarly, if the VCO is modulated away from ω_I, $\frac{d\theta_e}{dt}$ increases and the error voltage becomes a rapidly varying function of time. Under this condition the beat note waveform no longer looks sinusoidal; it looks like a series of aperiodic cusps, depicted schematically in Figure 2a. Because of its asymmetry, the beat note waveform contains a finite DC component that pushes the average value of the VCO toward ω_I, and lock is established. When the system is in lock, $\Delta\omega$ is equal to zero and only a steady-state DC error voltage remains.

Figure 2b displays an oscillogram of the loop error voltage $V_d(t)$ in an actual PLL system during the capture process. Note that as lock is approached, $\Delta\omega$ is reduced, the low-pass filter attenuation becomes less, and the amplitude of the beat note increases.



a. VCO Control Voltage Variation During Capture Transient



b. Oscillogram Showing a Capture Process

Figure 2. Asynchronous Error Beat Frequency During the Capture Transient

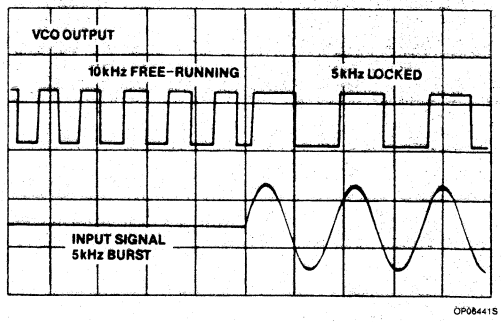


Figure 3. Exhibited by First-Order Fast Capture Transient

The total time taken by the PLL to establish lock is called *the pull-in time.* Pull-in time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low-pass filter bandwidth. Under certain conditions, the pull-in time may be shorter than the period of the beat note and the loop can lock without an oscillatory error transient.

A specific case to illustrate this is shown in Figure 3. The 565 PLL is shown acquiring lock within the first cycle of the input signal. The PLL was able to capture in this short time because it was operated as a first-order loop (no low-pass filter) and the input tone-burst frequency was within its lock and capture range.

EFFECT OF THE LOW-PASS FILTER

In the operation of the loop, the low-pass filter serves a dual function.

First, by attenuating the high frequency error components at the output of the phase comparator, it enhances the interference-rejection characteristics; second, it provides a short-term memory for the PLL and ensures a rapid recapture of the signal if the system is thrown out of lock due to a noise transient. Decreasing the low-pass filter bandwidth has the following effects on system performance (Long Time Constant):

a. The capture process becomes slower, and the pull-in time increases.

b. The capture range decreases.

c. Interference-rejection properties of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low-pass filter.

d. The transient response of the loop (the response of the PLL to sudden changes of the input frequency within the capture range) becomes underdamped.

The last effect also produces a practical limitation on the low-pass loop filter bandwidth and roll-off characteristics from a stability standpoint. These points will be explained further in the following analysis.

MATHEMATICALLY DEFINING PLL OPERATION

As mentioned previously, the phase comparator is basically an analog multiplier that forms the product of an RF input signal, $v_i(t)$, and the output signal, $v_o(t)$, from the VCO. Refer to Figure 1 and assume that the two signals to be multiplied can be described by

$$v_i(t) = V_I \sin \omega_I t \quad (3)$$

$$v_o(t) = V_O \sin (\omega_O t + \theta_e) \quad (4)$$

where ω_I, ω_O, and θ_e are the frequency and phase difference (or phase error) characteristics of interest. The product of these two signals is an output voltage given by

$$v_e(t) = K_1 V_I V_O (\sin \omega_I t)\,[\sin(\omega_O t + \theta_e)] \quad (5)$$

where K_1 is an appropriate dimensional constant. Note that the amplitude of $v_e(t)$ is directly proportional to the amplitude of the input signal V_I. The two cases of an unlocked loop ($\omega_I \neq \omega_O$) and of a locked loop ($\omega_I = \omega_O$) are now considered separately.

Unlocked State ($\omega_I \neq \omega_O$)
When the two frequencies to the phase comparator are not synchronized, the loop is not locked. Furthermore, the phase angle difference θ_e in Equations 4 and 5 is meaningless for this case since it can be eliminated by appropriately choosing the time origin.

Using trigonometric identities, Equation 5 can be rewritten as

$$v_e(t) = \frac{K_1 V_I V_O}{2}\,[\cos(\omega_I - \omega_O)t - \cos(\omega_I + \omega_O)t] \quad (6)$$

When $v_e(t)$ is passed through the low-pass filter, F(s), the sum frequency component is removed, leaving

$$v_f(t) = K_2 V_I V_O \cos\,(\omega_I - \omega_O)t \quad (7)$$

where K_2 is a constant. After amplification, the control voltage for the VCO appears as

$$v_d(t) = AK_2 V_I V_O \cos\,(\omega_I - \omega_O)t \quad (8)$$

This equation shows that a beat frequency effect is established between ω_I and ω_O, causing the VCO's frequency to deviate by $\pm\Delta\omega$ from ω_O' in proportion to the signal amplitude ($AK_2V_IV_O$) passing through the filter. If the amplitude of V_I is sufficiently large and if signal limiting or saturation does not occur, the VCO output frequency will be shifted from ω_O' by some $\Delta\omega$ until lock is established where

$$\omega_I = \omega_O = \omega_O' \pm \Delta\omega \quad (9)$$

If lock cannot be established, then either V_I is too small to drive the VCO to produce the necessary $\pm\Delta\omega$ deviation or ω_I is beyond the dynamic range of the VCO, i.e., $\omega_I \gtrless \omega_O' \pm \Delta\omega$. Remedies for these no lock conditions are:

1. Increase V_I either internally or externally to the loop by providing additional amplification.

2. Increase the internal loop gain by adjusting upward (larger −3dB frequency) the response of the low-pass filter.

3. Shift ω_O' closer to the expected ω_I. Establishing frequency lock leads to the second case where $\omega_I = \omega_O$.

Locked State ($\omega_I = \omega_O$)
When ω_I and ω_O are frequency synchronized, the output signal from the phase comparator for $\omega_I = \omega_O = \omega$ and a phase shift of θ_e is

$$v_e(t) = K_1 V_I V_O (\sin \omega t)\,\sin(\omega t + \theta_e) = \frac{K_1 V_I V_O}{2}\,[\cos\theta_e - \cos\,(2\omega t + \theta_e)] \quad (10)$$

The low-pass filter removes the high frequency, AC component of $v_e(t)$, leaving only the DC component. Thus,

$$v_f(t) = K_2 V_I V_O \cos\theta_e \quad (11)$$

After amplification the DC voltage driving the VCO and maintaining lock within the loop is

$$v_d(t) = V_D = AK_2 V_I V_O \cos\theta_e \quad (12)$$

Suppose ω_I and ω_O are perfectly synchronized to the free-running frequency ω_O'. For this case, V_D will be zero, indicating that θ_e must be $\pm 90°$. Thus V_D is proportional to the phase difference or phase error between θ_i and θ_o centered about a reference phase angle of $\pm 90°$. If ω_I changes slightly from ω_O', the first effect will be a change in θ_e from $\pm 90°$. V_D will adjust and settle out to some nonzero value to correct ω_O; under this condition frequency lock is maintained with $\omega_I = \omega_O$. The phase error will be shifted by some amount $\Delta\theta$ from the reference phase angle of $\pm 90°$. This concept can be simplified by redefining θ_e as

$$\theta_e = \theta_r \pm \Delta\theta \quad (13)$$

where θ_r is the inherent, reference phase shift of $\pm 90°$ and $\Delta\theta$ is the departure from this reference value. Now the VCO control voltage becomes

$$V_D = AK_2 V_I V_O \cos\,(\theta_r \pm \Delta\theta) = \pm AK_2 v_I V_O \sin\Delta\theta \quad (14)$$

Since the sine function is odd, a momentary change in $\Delta\theta$ contains information about which way to adjust the VCO frequency to correct and maintain the locked condition. The maximum range over which $\Delta\theta$ changes can be tracked is $-90°$ to $+90°$. This corresponds to a θ_e range from 0 to 180°.

In addition to being an error signal, V_D represents the demodulated output of an FM input applied as $v_{in}(t)$ assuming a linear VCO characteristic. Thus, FM demodulation can be accomplished with the PLL without the inductively-tuned circuits that are employed with conventional detectors.

DETERMINING PLL MODEL PARAMETERS

Since the PLL is basically an electronic servo loop, many of the analytical techniques developed for control systems are applicable to phase-locked systems. Whenever phase lock is established between $v_i(t)$ and $v_o(t)$ the linear model of Figure 4 can be used to predict the performance of the PLL system. Here θ_i and θ_o represent the phase angles associated with the input/output waveshapes, respectively; F(s) represents a generalized voltage transfer function for the low-pass filter in the s complex frequency domain; and K_d and K_o are conversion gains of the phase comparator and VCO, respectively, each having units as shown. The 1/s term associated with the VCO accounts for the inherent 90° phase shift in the loop since the VCO converts a voltage to a frequency and

since phase is the integral of frequency. Thus the VCO functions as an integrator in the feedback loop.

Specific values of K_d and K_o for all of Signetics' general purpose PLLs can be found in the sections describing the particular loop of interest. However, sometimes it may be desired to determine these conversion gains exactly for a specific device. The measurement scheme shown in Figure 5 can be used to determine K_d and K_o for a loop under lock. The function of the Khron-Hite filters is to extract the fundamental sinusoidal frequency component of their square wave inputs for application to the Gain-Phase Meter. If the input signal from the Function Generator is sinusoidal, then the first Khron-Hite filter may be eliminated. It is recommended to use high impedance oscilloscope probes so as to not distort the input of VCO waveshapes, thereby potentially altering their phase relationships. The frequency counter can be driven from the scope as shown, or connected directly to the input or VCO, provided its input impedance is large.

The procedure to follow for obtaining K_d and K_o is as follows:

1. Establish the desired external bias and gain conditions for the PLL under test.
2. With the Function Generator turned off, set the free-running frequency of the loop via the timing capacitor and timing resistor if appropriate. Monitor f_O' with the Frequency Counter.
3. Turn on the Function Generator and check to make sure the amplitude of the input signal is appropriate for the particular loop under test.
4. Adjust the input frequency for lock. Lock is discernable on a dual-trace scope when the input and VCO waveforms are synchronized and stationary with respect to each other. One should be especially careful to check that locking has not occurred between the VCO and some harmonic frequency. Carefully inspect both waveshapes, making sure each has the same period. (If a second Frequency Counter is available, an alternate scheme can be used to confirm frequency locking. One frequency counter is used to monitor the input signal frequency, and the second counter is used for the VCO frequency. When the two counters display the same frequency, the PLL is locked.)
5. Set the input frequency to the free-running frequency and note the Gain-Phase Meter display. It should be approximately 90°± 10°nominally. Record the phase error, θ_e, the VCO control voltage, V_D, and the input frequency, f_I.

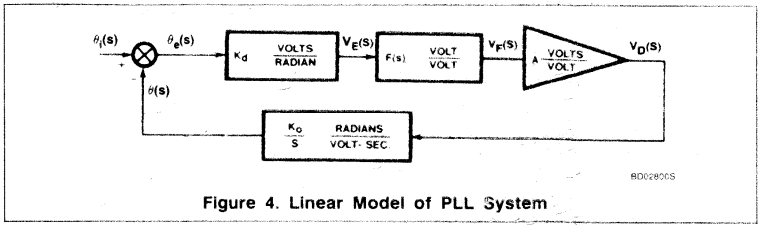


Figure 4. Linear Model of PLL System

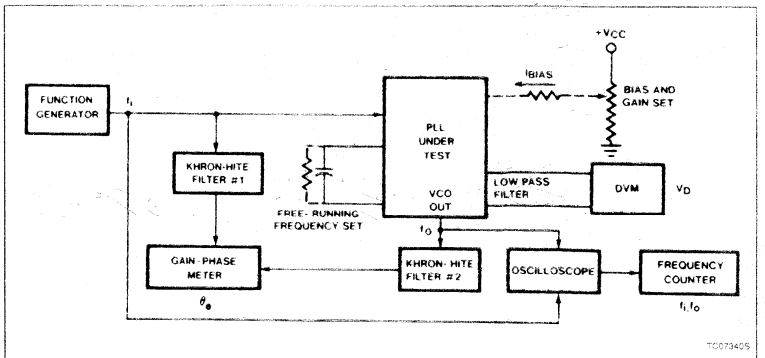


Figure 5. Measurement Scheme for K_d and K_o Determinations

6. Adjust f_I for frequencies above and below f_O' and record θ_e and V_D for each f_I, as appropriate.
7. Making a plot of V_D versus θ_e is useful for checking the measurement data and the system's linearity. The slope of this plot ($\Delta V_D/\Delta\theta_e$) is K_d in units of V/°. Multiplying this slope by $180/\pi$ gives the desired K_d in volts/radian.
8. A plot of $f_I = f_O$ versus V_D while the loop remains locked will check the VCO linearity. The slope of this plot is K_o at the particular free-running frequency. The units of slope taken directly from the graph are Hz/V. Multiplying this slope figure by 2π gives the desired K_o in units of radians/volt-sec.

K_d is generally constant over wide frequency ranges, but is linearly related to the input signal amplitude. K_o is constant with input signal level but does vary linearily with f_O'. Often it is convenient to specify a normalized K_o as

$$K_{O(norm)} = \frac{K_O}{f_O'} \frac{rad}{V} \quad (15)$$

The K_o value at any desired free-running frequency then can be estimated as

$$K_o \ (@ \ any \ f_O') = K_{o(norm)} f_O' \quad (16)$$

The loop gain for the PLL system is

$$K_v = K_d K_o A \quad (17)$$

(Often when the gain A is due to an amplifier internal to the IC, A will be included in either K_d or K_o. This is further illustrated in the article on the 565 PLL.)

MODELING THE PLL SYSTEM WITH VARIOUS LOW-PASS FILTERS

The open-loop transfer function for the PLL is

$$T(s) = \frac{K_V F(s)}{s} \quad (18)$$

Using linear feedback analysis techniques, and assuming that the VCO is in the forward path, the closed-loop transfer characteristics H(s) can be related to the open-loop performance as

$$H(s) = \frac{T(s)}{1 + T(s)} \quad (19)$$

and the roots of the characteristic system polynomial can be readily determined by root-locus techniques.

From these equations, it is apparent that the transient performance and frequency response of the loop is heavily dependent upon the choice of filter and its corresponding transfer characteristic, F(s).

Zero-Order Filter — F(s) = 1

The simplest case is that of the first-order loop where F(s) = 1 (no filter). The closed-loop transfer function then becomes

$$T(s) = \frac{K_V}{S + K_V} \tag{20}$$

This transfer function gives the root locus as a function of the total loop gain K_V and the corresponding frequency response shown in Figure 6a. The open-loop pole at the origin is due to the integrating action of the VCO. Note that the frequency response is actually the amplitude of the difference frequency component versus modulating frequency when the PLL is used to track a frequency-modulated input signal. Since there is no low-pass filter in this case, sum frequency components are also present at the phase comparator output and must be filtered outside of the loop if the difference frequency component (demodulated FM) is to be measured.

First-Order Filter

With the addition of a single-pole low-pass filter F(s) of the form

$$F(s) = \frac{1}{1 + \tau_1 s} \tag{21}$$

where $\tau_1 = R_1C_1$, the PLL becomes a second-order system with the root locus shown in FIgure 6b. Again, an open-loop pole is located at the origin because of the integrating action of the VCO. Another open-loop pole is positioned on the real axis at $-1/\tau_1$ where τ_1 is the time constant of the low-pass filter.

One can make the following observations from the root locus characteristics of Figure 6b:

a. As the loop gain K_V increases for a given choice of τ_1, the imaginary part of the closed-loop poles increases: thus, the natural frequency of the loop increases and the loop becomes more and more underdamped.

b. If the filter time constant is increased, the real part of the closed-loop poles becomes smaller and the loop damping is reduced.

As in any practical feedback system, excess shifts or non-dominant poles associated with the blocks within the PLL can cause the root loci to bend toward the right half plane as shown by the dashed line in Figure 6b. This is likely to happen if either the loop gain or the filter time constant is too large and may cause the loop to break into sustained oscillations.

First-Order Lag-Lead Filter

The stability problem can be eliminated by using a lag-lead type of filter, as indicated in Figure 6c. This type of a filter has the transfer function

$$F(s) = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s} \tag{22}$$

where $\tau_2 = R_2C$ and $\tau_1 = R_1C$. By proper choice of R_2, this type of filter confines the root locus to the left half-plane and ensures stability. The lag-lead filter gives a frequency response dependent on the damping, which can now be controlled by the proper adjustment of τ_1 and τ_2. In practice, this type of filter is important because it allows the loop to be used with a response between that of the first- and second-order loops and it provides an additional control over the loop transient response. If $R_2 = 0$, the loop behaves as a second-order loop and as $R_2 \rightarrow \infty$, the loop behaves as a first-order loop due to a pole-zero cancellation. However, as first-order operation is approached, the noise bandwidth increases and interference rejection decreases since the high frequency error components in the loop are now attenuated to a lesser degree.

Second- and Higher-Order Filters

Second- and higher-order filters, as well as active filters, occasionally are designed and incorporated within the PLL to achieve a particular response not possible or easily obtained with zero- or first-order filters. Adding more poles and more gain to the closed-loop transfer function reduces the inherent stability of the loop. Thus the designer must exercise extreme care and utilize complex stability analysis if second-order (and higher) filters or active filters are to be considered.

CALCULATING LOCK AND CAPTURE RANGES

In terms of the basic gain expression in the system, the lock range of the PLL ω_L can be shown to be numerically equal to the DC loop gain (2-sided lock range).

$$2\omega_L = 4\pi f_L = K_V F(0) \tag{23}$$

where F(0) is the value of the low-pass filters transfer function at DC.

Since the capture range ω_C denotes a transient condition, it is not as readily derived as the lock range. However, an approximate expression for the capture range can be written as (2-sided capture range).

$$2\omega_C = 4\pi f_C \simeq K_V |F(i\omega_C)| \tag{24}$$

where $F(i\omega_C)$ is the magnitude of the low-pass filter transfer function evaluated at ω_C. Solution of Equation 24 frequently involves a "trial and error" process since the capture range is a function of itself. *Note that at all times the capture range is smaller than the lock range.* For the simple first-order lag filter of Figure 6b, the capture range can be approximated as

$$2\omega_c \simeq 2\sqrt{\frac{\omega_L}{\tau_1}} = 2\sqrt{\frac{K_V}{\tau_1}} \tag{25}$$

This approximation is valid for

$$\tau_1 > > \frac{1}{2\omega_L} \tag{26}$$

Equations 23 and 24 show that the capture range increases as the low-pass filter time constant is decreased, whereas the lock range is unaffected by the filter and is determined solely by the loop gain.

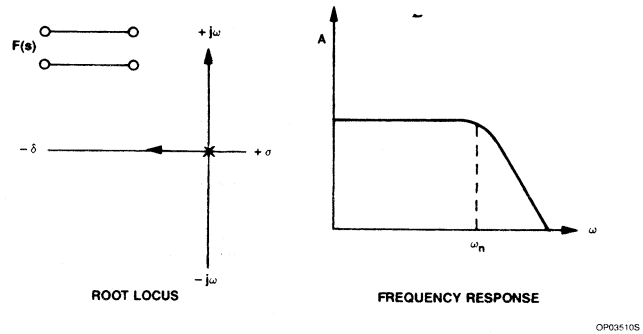
Figure 7 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly over a broad frequency range. The vertical scale is the corresponding loop error voltage. In Figure 7a, the input frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency ω_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input and causes a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of VCO conversion gain ($1/K_o$) and goes through zero as $\omega_i = \omega_O'$. The loop tracks the input until the input frequency reaches ω_2, corresponding to the upper edge of the lock range. The PLL then loses lock and the error voltage drops to zero. If the input frequency is swept slowly back, the cycle repeats itself, but is inverted, as shown in Figure 7b. The loop recaptures the signal at ω_3 and tracks it down to ω_4. The total capture and lock ranges of the system are:

$$2\omega_C = \omega_3 - \omega_1 \tag{27}$$

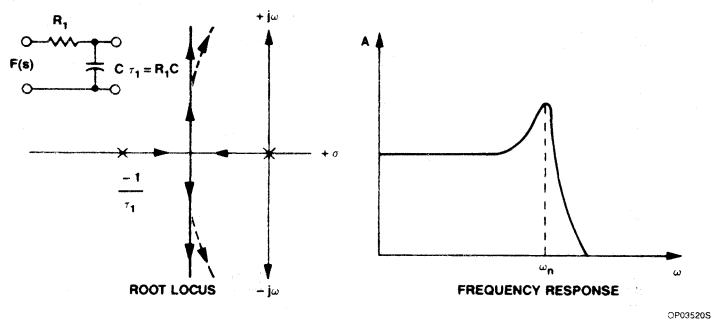
and

$$2\omega_L = \omega_2 - \omega_4 \tag{28}$$

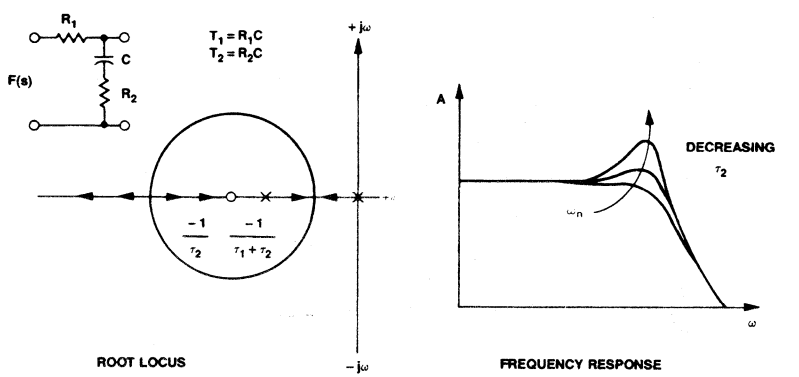
Note that, as indicated by the transfer characteristics of Figure 7, the PLL system has an inherent selectivity about the free-running frequency, ω_O'. It will respond only to the input signal frequencies that are separated from ω_O' by less than ω_C or ω_L, depending on whether the loop starts with or without an initial lock condition. The linearity of the frequency-to-voltage conversion characteristics for the PLL is determined solely by the VCO conversion gain. Therefore, in most PLL applications, the VCO is required to have a highly linear voltage-to-frequency transfer characteristic.



a. Zero-Order Filter



b. First-Order Simple Lag Filter



c. First-Order Lag-Lead Filter

Figure 6. Root Locus and Frequency Response Plots

DETERMINING LOOP RESPONSE

The transient response of a PLL can be calculated using the model of Figure 4 and Equations 18 and 19 as starting points. Combining these equations gives

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_V F(s)}{s + K_V F(s)} \quad (29)$$

The phase error which keeps the system in lock is

$$\theta_e(s) = \theta_i(s) - \theta_o(s) \quad (30)$$

Define a phase error transfer function

$$E(s) = \frac{\theta_e(s)}{\theta_i(s)} = 1 - \frac{\theta_o(s)}{\theta_i(s)}$$

$$= 1 - H(s) \quad (31)$$

As an example of the utilization of these equations, consider the most common case of a loop employing a simple first-order lag filter where

$$F(s) = \frac{1}{1 + s\tau_1} \quad (32)$$

For this filter, Equations 29 and 31 become

$$H(s) = \frac{K_V/\tau_1}{s^2 + s/\tau_1 + K_V/\pi_1} \quad (33)$$

$$E(s) = \frac{s(s + 1/\tau_1)}{s^2 + s/\tau_1 + K_V/\tau_1} \quad (34)$$

Both equations are second-order and have the same denominator which can be expressed as

$$D(s) = s^2 + s/\tau_1 + K_V/\tau_1$$
$$= s^2 + 2\zeta\omega_n s + \omega_n{}^2 \quad (35)$$

Where ω_n and ζ are, respectively, the system's undamped natural frequency and damping factor defined as

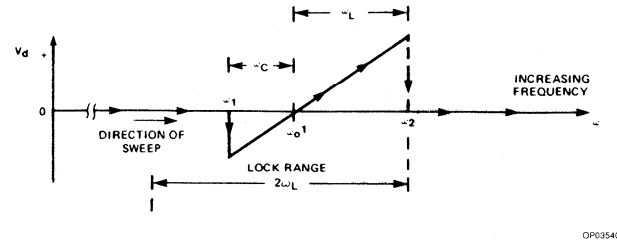
$$\omega_n = \sqrt{K_V/\tau_1} \quad (36)$$

$$\zeta = \frac{1}{2\sqrt{K_V\tau_1}} = \frac{\omega_n}{2K_V} \quad (37)$$

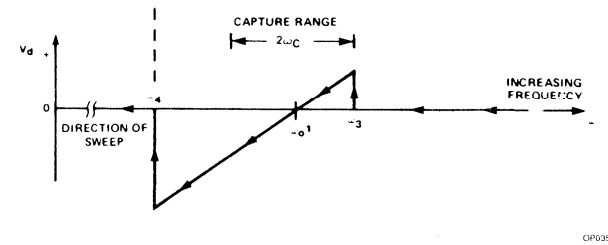
The system is considered overdamped for $\zeta > 1.0$, and critically damped $\zeta = 1.0$. Now examine this PLL system's response to various types of inputs.

Step-of-Phase Input

Consider a unit step-of-phase as the input signal. This input is shown in Figure 8 and can be thought of as simply shifting the time axis by a unit step (one radian or one degree, depending upon the working units) while maintaining the same input frequency. Mathematically this input has the form



a. Input Frequency Increasing



b. Decreasing Input Frequency

Figure 7. Typical PLL Frequency-to-Voltage Transfer Characteristics

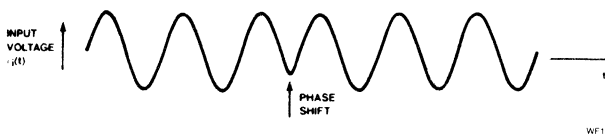


Figure 8. Input Signal Representing a Unit Step of Phase at Constant Frequency

$$\theta_i(s) = \frac{1}{s} \quad (38)$$

The phase of VCO output and the system's phase error are represented by

$$\theta_o(s) = \frac{H(s)}{s} = \frac{\omega_n{}^2}{s(s^2 + 2\zeta\omega_n s + \omega_n{}^2)} \quad (39)$$

$$\theta_e(s) = \frac{E(s)}{s} = \frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n{}^2} \quad (40)$$

(depending upon the working units) while maintaining the same input frequency. Mathematically this input has the form

$$\theta_o(t) = 1 + \frac{e - \zeta\omega_n t}{\sqrt{1 - \zeta^2}} \sin\left(\omega_n t\sqrt{1 - \zeta^2} + \Psi\right) \quad (41)$$

where $\Psi = \arctan\frac{\sqrt{1 - \zeta^2}}{\zeta}$ (42)

and $\zeta \neq 1$.

$$\theta_e(t) = \frac{e - \zeta\omega_n(t)}{\sqrt{1 - \zeta^2}} \sin(\omega_n t\sqrt{1 - \zeta^2} + \Psi) \quad (43)$$

When $\zeta = 1$, these phase responses are

$$\theta_o(t) = 1 - (1 - \omega_n t)e^{-\omega_n t} \quad (44)$$

and

$$\theta_e(t) = (1 + \omega_n t)e^{-\omega_n t} \quad (45)$$

Figure 9 is a plot of the VCO phase response and the phase error transient for various damping factors. Note from this figure that an underdamped system has overshoot which can cause the loop to break lock if this overshoot is too large. The critical condition for maintaining lock is to keep the phase error within the dynamic range for the phase comparator of $-\pi/2$ to $\pi 2$ radians. For the underdamped case, the peak phase-error overshoot is

$$\theta_e(max) = e - \zeta\pi/> \sqrt{1-\zeta^2} \quad (46)$$

which must be less than $\pi/2$ to maintain lock. Lock can also be broken for the overdamped and critically-damped loops if the input phase shift is too large where the phase error exceeds $\pm\pi/2$ radians.

The analysis and equations given are based upon the small-signal model of Figure 4. If the signal amplitudes become too large, one or more functional blocks in the system can saturate, causing a slew rate type limiting action that may break lock.

The *transient change* in the VCO frequency due to the unit step-of-phase input can be found by taking the time derivative of Equation 41 or alternatively by finding the inverse Laplace transform of

$$\omega_O(s) = s\theta_o(s) = \frac{{\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} \quad (47)$$

which is

$$\omega_O(t) = \frac{\omega_n e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin \omega_n t \sqrt{1-\zeta^2} \quad (48)$$

Unit Step-of-Frequency Input

This type of input occurs when the input frequency is instantaneously changed from one frequency to another as is done in FSK and modem applications. For this input, as shown in Figure 10,

$$\theta_i(s) = \frac{1}{s^2} \quad (49)$$

The VCO output phase is

$$\theta_o(s) = \frac{{\omega_n}^2}{s^2(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad (50)$$

The transient time expression for the VCO *phase change* is

$$\theta_o(t) = t - \frac{2\zeta}{\omega_n} + \frac{e^{-\zeta\omega_n t}}{\omega_n\sqrt{1-\zeta^2}} \sin(\omega_n t\sqrt{1-\zeta^2} + 2\Psi) \quad (51)$$

for $\zeta \neq 1$.

The time expression for the VCO *frequency change* for a unit step-of-frequency input is the same as the time response VCO phase change due to a step-of-phase input (Equation 41), or

$\omega_O(t)$ for frequency step input $= \theta_o(t)$ for phase step input Thus

$$\omega_O(t) = 1 + \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin(\omega_n t \sqrt{1-\zeta^2} + \Psi) \quad (52)$$

for $\zeta \neq 1$.

Unit Ramp-of-Frequency Input

This form of input signal represents sweeping the input frequency at a constant rate and direction as shown in Figure 11. The amplitude and phase of the input remain constant; the input frequency changes linearly with time. Since the input signal to the PLL model is a phase, a unit ramp-of-frequency appears as a phase acceleration type input that can be mathematically described as

$$\theta_i(s) = \frac{1}{s^3} \quad (53)$$

The VCO output phase change is

$$\theta_o(s) = \frac{{\omega_n}^2}{s^3(s^2 + 2\zeta\omega_n s + {\omega_n}^2)} \quad (54)$$

The time expression for the VCO phase change is

$$\theta_o(t) = \frac{t^2}{2} - \frac{2\zeta t}{\omega_n} + \frac{2\zeta}{{\omega_n}^2}\left[2\zeta(1-{\omega_n}^2) + \left(\frac{1-4\zeta^2{\omega_n}^2 + 4\zeta^2{\omega_n}^4}{1-\zeta^2}\right)^{1/2} \times e^{-\zeta\omega_n t} \sin(\omega_n t\sqrt{1-\zeta^2} + \Psi')\right] \quad (55)$$

where $\Psi = \arctan \frac{\sqrt{1-\zeta^2}}{\zeta(1-2{\omega_n}^2)} + \Psi$

and Ψ is given in Equation 42.

PLL BUILDING BLOCKS

VCO

Since three different forms of VCO have been used in the Signetics PLL series, the VCO details will not be discussed until the individual loops are described. However, a few general comments about VCOs are in order.

When the PLL is locked to a signal, the VCO voltage is a function of the frequency of the input signal. Since the VCO control voltage is the demodulated output during FM demodulation, it is important that the VCO voltage-to-frequency characteristic be linear so that the output is not distorted. Over the linear range of the VCO, the conversion gain is given by K_O (in radian/V-sec)

$$K_O = \frac{\Delta\omega_O}{\Delta V_d} \quad (56)$$

Since the loop output voltage is the VCO voltage, we can get the loop output voltage as

$$\Delta V_d = \frac{\Delta\omega_O}{K_O} \quad (57)$$

The gain K_O can be found from the data sheet. When the VCO voltage is changed, the frequency change is virtually instantaneous.

Phase Comparator

All of Signetics' analog phase-locked loops use the same form of phase comparator — often called the doubly-balanced multiplier or mixer. Such a circuit is shown in Figure 12.

The input stage formed by transistors Q1 and Q2 may be viewed as a differential amplifier which has an equivalent collector resistance R_C and whose differential gain at balance is the ratio of R_C to the dynamic emitter resistance, r_e, of Q1 and Q2.

$$A_d = \frac{R_C}{r_e} = \frac{R_C}{\frac{0.026}{I_E/2}} = \frac{R_C I_E}{0.052} \quad (58)$$

where I_E is the total DC bias current for the differential amplifier pair.

The switching stage formed by Q3 – Q6 is switched on and off by the VCO square wave. Since the collector current swing of Q2 is the negative of the collector current swing of Q1, the switching action has the effect of multiplying the differential stage output first by +1 and then by –1. That is, when the base of Q4 is positive, R_{C2} receives I_1 and when the base of Q6 is positive, R_{C2} receives $i_2 = i_1$. Since the circuit is called a multiplier, performing the multiplication will gain further insight into the action of the phase comparator.

Consider an input signal which consists of two added components: a component at frequency ω_i which is close to the free-running frequency and a component at frequency ω_k which may be at any frequency. The input signal is

$$v_i(t) + v_k(t) = V_i\sin(\omega_i t + \theta_i) + v_k\sin(\omega_k t + \theta_k) \quad (59)$$

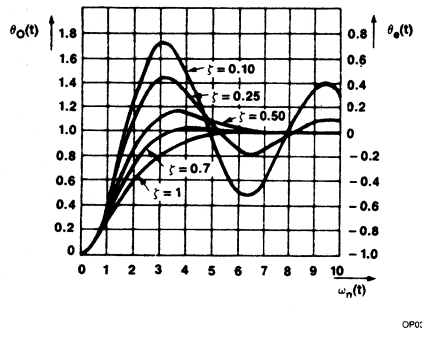


Figure 9. VCO Phase and Loop Phase Error Transient Responses for Various Damping Factors

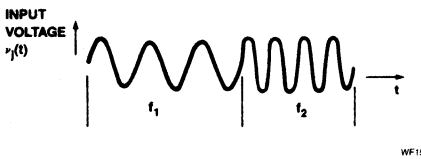


Figure 10. Input Signal for a Unit Step-of-Frequency at Constant Phase

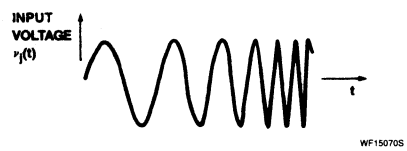


Figure 11. Input Signal for a Unit Ramp-of-Frequency Input

where θ_i and θ_k are the phase in relation to the VCO signal. The unity square wave developed in the multiplier by the VCO signal is

$$v_o(t) = \sum_{n=0}^{\infty} \frac{4}{\pi(2n+1)} \sin[(2n+1)\omega_O t] \quad (60)$$

where ω_O is the VCO frequency. Multiplying the two terms, using the appropriate trigonometric relationships, and inserting the differential stage gain A_d gives:

$$v_e(t) = \frac{2A_d}{\pi} \left[\sum_{n=0}^{\infty} \frac{V_I}{(2n+1)} \cos[(2n+1)\omega_O t - \omega_I t - \theta_i] - \sum_{n=0}^{\infty} \frac{V_I}{(2n+1)} \cos[(2n+1)\omega_O t + \omega_I t + \theta_i] + \sum_{n=0}^{\infty} \frac{V_k}{(2n+1)} \cos[(2n+1)\omega_O t - \omega_k t - \theta_k] - \sum_{n=0}^{\infty} \frac{V_k}{(2n+1)} \cos[(2n+1)\omega_O t + \omega_k t + \theta_k] \right] \quad (61)$$

Assuming that temporarily V_k is zero, if ω_1 is close to ω_O, the first term (n = 0) has a low frequency difference frequency component. This is the beat frequency component that feeds around the loop and causes lock-up by modulating the VCO. As ω_O is driven closer to ω_I, this difference component becomes lower and lower in frequency until $\omega_O = \omega_I$ and lock is achieved. The first term then becomes

$$v_e(t) = V_E = \frac{2A_d V_I}{\pi} \cos\theta_i \quad (62)$$

which is the usual phase comparator formula showing the DC component of the phase comparator during lock. This component must equal the voltage necessary to keep the VCO at ω_O. It is possible for ω_O to equal ω_I momentarily during the lock-up process and, yet, for the phase to be incorrect so that ω_O passes through ω_I without lock being achieved. This explains why lock is usually not achieved instantaneously, even when $\omega_I = \omega_O$ at t = 0.

If $n \neq 0$ in the first term, the loop can lock when $\omega_I = (2n+1)\omega_O$, giving the DC phase comparator component

$$V_e(t) = V_E = \frac{2A_d V_I}{\pi(2n+1)} \cos\theta_i \quad (63)$$

showing that the loop can lock to odd harmonics of the free-running frequency. The (2n + 1) term in the denominator shows that the phase comparator's output is lower for harmonic lock, which explains why the lock range decreases as higher and higher odd harmonics are used to achieve lock.

Note also that the phase comparator's output during lock is (assuming A_d is constant) also a function of the input amplitude V_I. Thus, for a given DC phase comparator output V_E, an input amplitude decrease must be accompanied by a phase change. Since the loop can remain locked only for θ_i between 0 and 180°, the lower V_I becomes, the more the lock range is reduced.

Note from the second term that during lock the lowest possible frequency is $\omega_O + \omega_I = 2\omega_I$. A sum frequency component is always present at the phase comparator output. This component is usually greatly attenuated by the low-pass filter capacitor connected to the phase comparator output. However, when rapid tracking is required (as with high-speed FM detection or FSK), the requirement for a relatively high frequency cutoff in the low-pass filter may leave this component unattenuated to the extent that it interferes with detection. At the very least, additional filtering may be required to remove this component. Components caused by $n \neq 0$ in the second term are both attenuated and of much higher frequency, so they may be neglected.

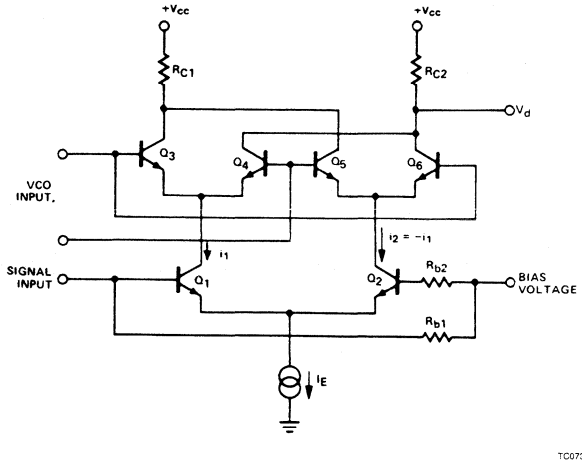


Figure 12. Integrated Phase Comparator Circuit

Suppose that other frequencies represented by V_k are present. What is their effect for $V_k \neq 0$?

The third term shows that V_k introduces another difference frequency component. Obviously, if ω_k is close to ω_I, it can interfere with the locking process since it may form a beat frequency of the same magnitude as the desired locking beat frequency. However, suppose lock has been achieved so that $\omega_O = \omega_I$. In order for lock to be maintained, the average phase comparator output must be constant. If $\omega_O = \omega_k$ is relatively low in frequency, the phase θ_i must change to compensate for this beat frequency. Broadly speaking, any signal in addition to the signal to which the loop is locked causes a phase variation. Usually this is negligible since ω_k is often far removed from ω_I. However, it has been stated that the phase θ_i can move only between 0 and 180°. Suppose the phase limit has been reached and V_k appears. Since it cannot be compensated for, it will drive the loop out of lock. This explains why extraneous signals can result in a decrease in the lock range. If V_k is assumed to be an instantaneous noise component, the same effect occurs. When the full swing of the loop is being utilized, noise will decrease the lock or tracking range. This effect can be reduced by decreasing the cutoff frequency of the low-pass filter so that the $\omega_O - \omega_k$ is attenuated to a greater extent, which illustrates that noise immunity and out-band frequency rejection is improved (at the expense of capture range since $\omega_O - \omega_I$ is likewise attenuated) when the low-pass filter capacitor is large.

The third term can have a DC component when ω_k is an odd harmonic of the locked frequency so that $(2n + 1)(\omega_O - \omega_I)$ is zero and θ_k makes its appearance. This will have an effect on θ_1 which will change the θ_1 versus frequency ω_1. This is most noticeable when the waveform of the incoming signal is, for example, a square wave. The θ_k term will combine with the θ_i term so that the phase is a linear function of input frequency. Other waveforms will give different phase versus frequency functions. When the input amplitude V_I is large and the loop gain is large, the phase will be close to 90° throughout the range of VCO swing, so this effect is often unnoticed.

The fourth term is of little consequence except that if ω_k approaches zero, the phase comparator output will have a component at the locked frequency ω_O at the output. For example, a DC offset at the input differential stage will appear as a square wave of fundamental ω_O at the phase comparator output. This is usually small and well attenuated by the low-pass filter. Since many out-band signals or noise components may be present, many V_k terms may be combining to influence locking and phase during lock. Fortunately, only those close to the locked frequency need be considered.

Quadrature-Phase Detector (QPD)

The quadrature-phase detector action is exactly the same except that its output is proportional to the sine of the phase angle. When the phase θ_i is 90°, the quadrature-phase detector output is then at its maximum, which explains why it makes a useful lock or amplitude detector. The output of the quadrature-phase detector is given by

$$V_q = \frac{2A_qV_I}{\pi} \sin \theta_i \quad (64)$$

where V_I is the constant or modulated AM signal and $\theta_i \approx 90°$ in most cases so that sine $\theta_i = 1$ and

$$V_q = \frac{2A_qV_I}{\pi} \quad (65)$$

This is the demodulation principle of the autodyne receiver and the basis for the 567 tone decoder operation.

INITIAL PLL SETUP CHOICES

In a given application, maximum PLL effectiveness can be achieved if the designer understands the tradeoffs which can be made. Generally speaking, the designer is free to select the frequency, lock range, capture range, and input amplitude.

FREE-RUNNING FREQUENCY SELECTION

Setting the center or free-running frequency is accomplished by selecting one or two external components. The center frequency is usually set in the center of the expected input frequency range. Since the loop's ability to capture is a function of the *difference* between the incoming and free-running frequencies, the band edges of the capture range are *always* an equal distance (in Hz) from the center frequency. Typically, the lock range is also centered about the free-running frequency. Occasionally, the center frequency is chosen to be offset from the incoming frequency so that the tracking range is limited on one side. This permits rejection of an adjacent higher or lower frequency signal without paying the penalty for narrow-band operation (reduced tracking speed).

All of Signetics' loops use a phase comparator in which the input signal is multiplied by a unity square wave at the VCO frequency. The odd harmonics present in the square wave permit the loop to lock to input signals at these odd harmonics. Thus, the center frequency may be set to, say, ⅓ or ⅕ of the input signal. The tracking range, however, will be considerably reduced as the higher harmonics are utilized.

The foregoing phase comparator discussion would suggest that the PLL cannot lock to subharmonics because the phase comparator cannot produce a DC component if ω_I is less than ω_O.

The loop can lock to both odd harmonic and subharmonic signals in practice because such signals often contain harmonic components at ω_O. For example, a square wave of fundamental $\omega_O/3$ will have a substantial component at ω_O to which the loop can lock. Even a pure sine wave input signal can be used for harmonic locking if the PLL input stage is overdriven. (The resultant internal limiting generates harmonic frequencies.) Locking to even harmonics or subharmonics is the least satisfactory, since the input or VCO signal must contain second harmonic distortion. If locking to even harmonics is desired, the duty cycle of the input and VCO signals must be shifted away from the symmetrical to generate substantial, even harmonic, content.

In evaluating the loop for a potential application, it is best to actually compute the magnitude of the expected signal component nearest ω_O. This magnitude can be used to estimate the capture and lock ranges.

All of Signetics' loops are stabilized against center frequency drift due to power supply variations. Both the 565 and the 567 are temperature-compensated over the entire military temperature range (−55 to +125°C). To benefit from this inherent stability, however, the designer must provide equally stable (or better) external components. For maximum cost effectiveness in some noncritical applications, the designer may wish to trade some stability for lower cost external components.

GUIDELINES FOR LOCK RANGE CONTROL

Two things limit the lock range. First, any VCO can swing only so far; it the input signal frequency goes beyond this limit, lock will be lost. Second, the voltage developed by the phase comparator is proportional to the product of *both* the phase and the amplitude of the in-band component to which the loop is locked. If the signal amplitude decreases, the phase difference between the signal and the VCO must increase in order to maintain the same output voltage and, hence, the same frequency deviation. The 564 contains an internal limiter circuit between the signal input and one input to the phase comparator. This circuit limits the amplitude of large input signals such as those from TTL outputs to approximately 100mV before they are applied to the phase comparator. The limiter significantly improves the AM rejection of the PLL for input signal amplitudes greater than 100mV.

This happens so often with low input amplitudes that even the full ±90° phase range of the phase comparator cannot generate enough voltage to allow tracking wide deviations. When this occurs, the effective lock range is reduced. Weak input signals cause a reduction of tracking capability and greater phase errors. Conversely, a strong input signal will allow the use of the entire VCO swing capability and keeps the VCO phase (referred to the input signal) very close to 90° throughout the range. Note that the lock range does not depend on the low-pass filter. However, if a low-pass filter *is* in the loop, it will have the effect of limiting the maximum rate at which tracking can occur. Obviously, the LPF capacitor voltage cannot change instantly, so lock may be lost when large enough step changes occur. Between the constant frequency input and the step-change frequency input is some limiting frequency slew rate at which lock is just barely maintained. When tracking at this rate, the phase difference is at its limit of 0° or 180°. It can be seen that if the LPF cutoff frequency is low, the loop will be unable to track as fast as if the LPF cutoff frequency is higher. Thus, when maximum tracking rate is needed, the LPF should have a high cutoff frequency. However, a high cutoff frequency LPF will attenuate the sum frequencies to a lesser extent so that the output contains a significant and often bothersome signal at twice the input frequency. The phase comparator's output contains both sum and difference frequencies. During lock, the difference frequency is zero, but the sum frequency of twice the locked frequency is still present. This sum frequency component can then be filtered out with an external low-pass filter.

INPUT LEVEL AMPLITUDE SELECTION

Whenever amplitude limiting of the in-band signal occurs, whether in the loop input stages or prior to the input, the lock and capture ranges become independent of signal amplitude.

Better noise and out-band signal immunity is achieved when the input levels are below the limiting threshold, since the input stage is in its linear region and the creation of cross-modulation components is reduced. Higher input levels will allow somewhat faster operation due to greater phase comparator gain and will result in a lock range which becomes constant with amplitude as the phase comparator gain becomes constant. Also, high input levels will result in a linear phase versus frequency characteristic.

CAPTURE RANGE CONTROL

There are two main reasons for making the low-pass filter time constant large. First, a large time constant provides an increased memory effect in the loop so that it remains at or near the operating frequency during momentary fading or loss of signal. Second, the large time constant integrates the phase comparator's output so that increased immunity to noise and out-band signals is obtained.

Besides the lower tracking rates attendant to large loop filters, other penalties must be paid for the benefits gained. The capture range is reduced and the capture transient becomes longer. Reduction of capture range occurs because the loop must utilize the magnitude of the difference frequency component at the phase comparator to drive the VCO towards the input frequency.

If the LPF cutoff frequency is low, the difference component amplitude is reduced and the loop cannot swing as far. Thus, the capture range is reduced.

LOCK-UP TIME AND TRACKING SPEED CONTROL

In tracking applications, lock-up time is normally of little consequence, but occasions do arise when it is desirable to keep lock-up time short to minimize data loss when noise or extraneous signals drive the loop out of lock. Lock-up time is of great importance in tone decoder type applications. Tracking speed is important if the loop is used to demodulate an FM signal. Although the following discussion dwells largely on lock-up time, the same comments apply to tracking speeds.

No simple expression is available which adequately describes the acquisition or lock-up time. This may be appreciated when we review the following factors which influence lock-up time.

a. Input phase

b. Low-pass filter characteristic

c. Loop damping

d. Deviation of input frequency from center frequency

e. In-band input amplitude

f. Out-band signals and noise

g. Center frequency

Fortunately, it is usually sufficient to know how to improve the lock-up time and what must be sacrificed to get faster lock-up. Consider an operational loop or tone decoder where occasionally the lock-up transient is too long. What can be done to improve the situation — keeping in mind the factors that influence lock?

a. Initial phase relationship between incoming signal and VCO — This is the greatest single factor influencing the lock time. If the initial phase is wrong, it first drives the

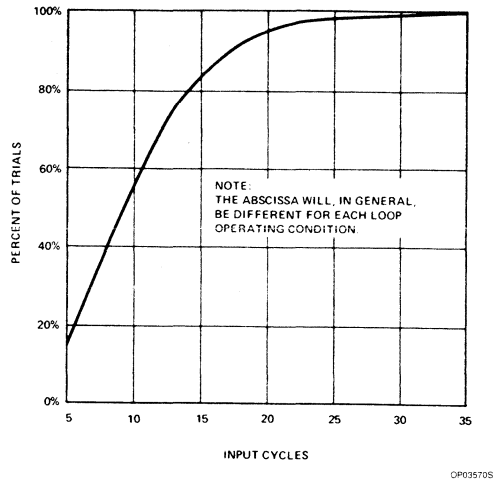


Figure 13. Probability of Lock vs Input Cycles

VCO frequency *away* from the input frequency so that the VCO frequency must walk back on the beat notes. Figure 13 gives a typical distribution of lock-up times with the input pulse initiated at random phase. The only way to overcome this variation is to send phase information all the time so that a favorable phase relationship is guaranteed at t = 0. For example, a number of PLLs or tone decoders may be weakly locked to low amplitude harmonics of a pulse train and the transmitted tone phase related to the same pulse train. Usually, however, the incoming phase cannot be controlled.

b. Low-pass filter — The larger the low-pass filter time constant, the longer will be the lock-up time. The lock-up time can be reduced by decreasing the filter time constant, but in doing so, some of the noise immunity and out-band signal rejection will be sacrificed. This is unfortunate, since this is what necessitated the use of a large filter in the first place. Also present will be a sum frequency (twice the VCO frequency) component at the low pass filter and greater phase jitter resulting from out-band signals and noise. In the case of the tone decoder (where control of the capture range is required since it specifies the device bandwidth) a lower value of low-pass capacitor automatically increases the bandwidth. Speed is gained only at the expense of added bandwidth.

c. Loop damping — A simple first-order low-pass filter of the form

$$F(s) = \frac{1}{1 + s\tau} \quad (66)$$

produces a loop damping of

$$\zeta = \tfrac{1}{2}\sqrt{\frac{1}{\pi K_V}} \quad (67)$$

Damping can be increased not only by reducing τ, as discussed above, but also by reducing the loop gain K_V. Using the loop gain reduction to control bandwidth or capture and lock ranges achieves better damping for narrow bandwidth operation. The penalty for this damping is that more phase comparator output is required for a given deviation so that phase errors are greater and noise immunity is reduced. Also, more input drive may be required for a given deviation.

d. Input frequency deviation from free-running frequency — Naturally, the further an applied input signal is from the free-running frequency of the loop, the longer it will take the loop to reach that frequency due to the charging time of the low-pass filter capacitor. Usually, however, the effect of this frequency deviation is small compared to the variation resulting from the initial phase uncertainty. Where loop damping is very low, however, it may be predominant.

e. In-band input amplitude — Since input amplitude is one factor in the phase comparator's gain K_d, and since K_d is a factor in the loop gain K_V damping is also a function of input amplitude. When the input amplitude is low, the lock-up time may be limited by the rate at which the low-pass capacitor can charge with the reduced phase comparator output (see d above).

f. Out-band signals and noise — Low levels of extraneous signals and noise have little effect on the lock-up time, neither improving or degrading it. However, large levels may overdrive the loop input stage so that limiting occurs, at which point the in-band signal starts to be suppressed. The lower effective input level can cause the lock-up time to increase, as discussed in e above.

g. Center frequency — Since lock-up time can be described in terms of the number of cycles to lock, fastest lock-up is achieved at higher frequencies. Thus, whenever a system can be operated at a higher frequency, lock will typically take place faster. Also, in systems where different frequencies are being detected, the higher frequencies, on the average, will be detected before the lower frequencies.

However, because of the wide variation due to initial phase, the reverse may be true for any single trial.

PLL MEASUREMENT TECHNIQUES

This section deals with measurements of PLL operation. The techniques suggested are meant to help the designer in evaluating the performance of the PLL during the initial setup period as well as to point out some pitfalls that may obscure loop evaluation. Recognizing that the test equipment may be limited, techniques are described which require a minimum of standard test items.

The majority of the PLL tests described can be done with a signal generator, a scope and a frequency counter. Most laboratories have these. A low cost digital voltmeter will facilitate accurate measurement of the VCO conversion gain. Where the need for a FM generator arises, it may be met in most cases by the VCO of a Signetics PLL. Any of the loops may be set up to operate as a VCO by simply applying the modulating voltage to the low-pass filter terminal(s). The resulting generator may be checked for linearity by using the counter to check frequency as a function of modulating voltage. Since the VCOs may be modulated right down to DC, the calibration may be done in steps. Moreover, loop measurements may be made by applying a constant frequency to the loop input and the modulating signal to the low-pass filter terminal to simulate the effect of a FM input so that an FM generator may be omitted for many measurements.

FREE-RUNNING FREQUENCY

Free-running frequency measurements are easily made by connecting a frequency counter or oscilloscope to the VCO output of the

loop. The loop should be connected in its final configuration with the chosen values of input, bypass, and low-pass filter capacitors. No input signal should be present. As the free-running frequency is read out, it can be adjusted to the desired value by the adjustment means selected for the particular loop. It is important not to make the frequency measurement directly at the timing capacitor, unless the capacity added by the measurement probe is much less than the timing capacitor value, since the probe capacity will then cause a frequency error.

When the frequency measurement is to be converted to a DC voltage for production readout or automated testing, a calibrated phase-locked loop can be used as a frequency meter.

CAPTURE AND LOCK RANGES

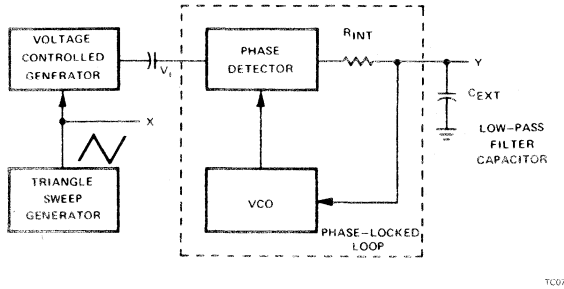
Figure 14a shows a typical measurement setup for capture and lock range measurements. The signal input from a variable frequency oscillator is swept linearly through the frequency range of interest and the loop FM output is displayed on a scope or (at low frequencies) X-Y recorder. The sweep voltage is applied to the X axis.

Figure 14b shows the type of trace which results. The lock range is given by the outer lines on the trace, which are formed as the incoming frequency sweeps away from the center frequency. The inner trace, formed as the frequency sweeps toward the center frequency, designates the capture range. Linearity of the VCO is revealed by the straightness of the trace portion within the lock range. The slope ($\Delta f/\Delta V$) is the conversion gain K_o for the VCO at the particular free-running frequency.

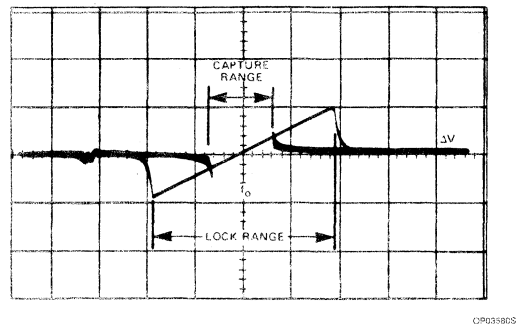
By using the sweep technique, the effect on free-running frequency, capture range, and lock range of the input amplitude, supply voltage, low-pass filter and temperature can be examined.

Because of the lock-up time duration and variation, the sweep frequency must be much lower than the free-running frequency, especially when the capture range is below 10% of the free-running frequency. Otherwise, the *apparent* capture and lock range will be functions of sweep frequency. It is best to start sweeping as slowly as possible and, if desired, increase the rate until the capture range begins to show an apparent reduction — indicating that the sweep is too fast. Typical sweep frequencies are in the range of 1/1000 to 1/100,000 of the free-running frequency. In the case of the 567, the quadrature detector output may be similarly displayed on the Y axis, as shown in Figure 15, showing the output level versus frequency for one value of input amplitude.

Capture and lock range measurements may also be made by sweeping the generator manually through the band of interest. Sweeping must be done very slowly as the edges of the capture range are approached (sweeping toward center frequency) or the lock-up transient delay will cause an error in reading the band edge. Frequency should be read from the generator rather than the loop



a. Measurement Setup



b. Oscilloscope Display

Figure 14. Capture and Lock Ranges

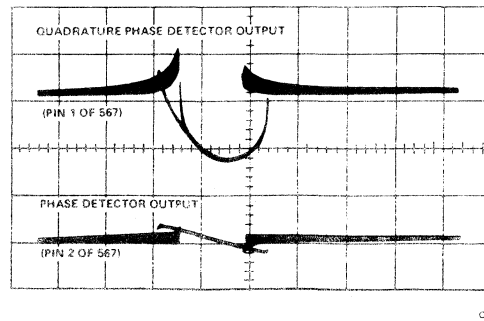


Figure 15. Quadrature-Phase Detector and Phase Comparator Outputs of the NE567 PLL

VCO because the VCO frequency gyrates wildly around the center frequency just before and after lock. Lock and unlock can be readily detected by simultaneously monitoring the input and VCO signals, the DC voltage at the low-pass filter, or the AC beat frequency components at the low-pass filter. The latter are greatly reduced during lock as opposed to frequencies just outside of lock.

FM AND AM DEMODULATION DISTORTION

These measurements are quite straight-forward. The loop is simply set up for FM detection and the test signal is applied to the input. A spectrum analyzer or distortion analyzer (HP333A) can be used to measure distortion at the FM output.

For FM demodulation, the input signal amplitude must be large enough so that lock is not lost at the frequency extremes. The data sheets give the lock (or tracking) range as a function of input signal and the optional range control adjustments. Due to the inherent linearity of the VCOs, it makes little difference whether the FM carrier is at the free-running frequency or offset slightly as long as the tracking range limits are not exceeded.

The faster the FM modulation in relation to the center frequency, the lower the value of the capacitor in the low pass filter must be for satisfactory tracking. As this value decreases, however, it attenuates the sum frequency component of the phase comparator output less. The demodulated signal will appear to have greater distortion unless this component is filtered out before the distortion is measured.

NATURAL FREQUENCY AND DAMPING

Circuits and mathematical expressions for the natural frequencies and dampings are given in Figure 16 for two first-order low-pass filters. Because of the integrator action of the PLL in converting frequency to phase, the order of the loop always will be one greater than the order of the LPF. Hence, both these first-order LPFs produce a second-order PLL system.

The natural frequency (ω_n) of a loop in its final circuit configuration can be measured by applying a frequency-modulated signal of the desired amplitude to the loop. Figure 16 shows that the natural frequency is a function of K_d, which is, in turn, a function of input amplitude. As the modulation frequency (ω_m) is increased, the phase relationship between the modulation and recovered sine wave will go through 90° at $\omega_m = \omega_n$ and the output amplitude will peak.

Damping is a function of K_d, K_o, and the low-pass filter. Since K_o and K_d are functions of the free-running frequency and input amplitude, respectively, damping is highly dependent on the particular operating condition of the loop. Damping estimates for the desired operating condition can be made by applying an input signal which is frequency-modulated within the lock range by a square wave. The low-pass filter voltage is then monitored on an oscilloscope which is synchronized to the modulating waveform, as shown in Figure 17. Figure 18 shows typical waveforms displayed. The loop damping can be estimated by comparing the number and magnitude of the overshoots with the graph of Figure 19, which gives the transient phase error due to a step in input frequency.

An expression for calculating the damping for any underdamped second-order system ($\zeta < 1.0$) when the normalized peak overshoot is known is

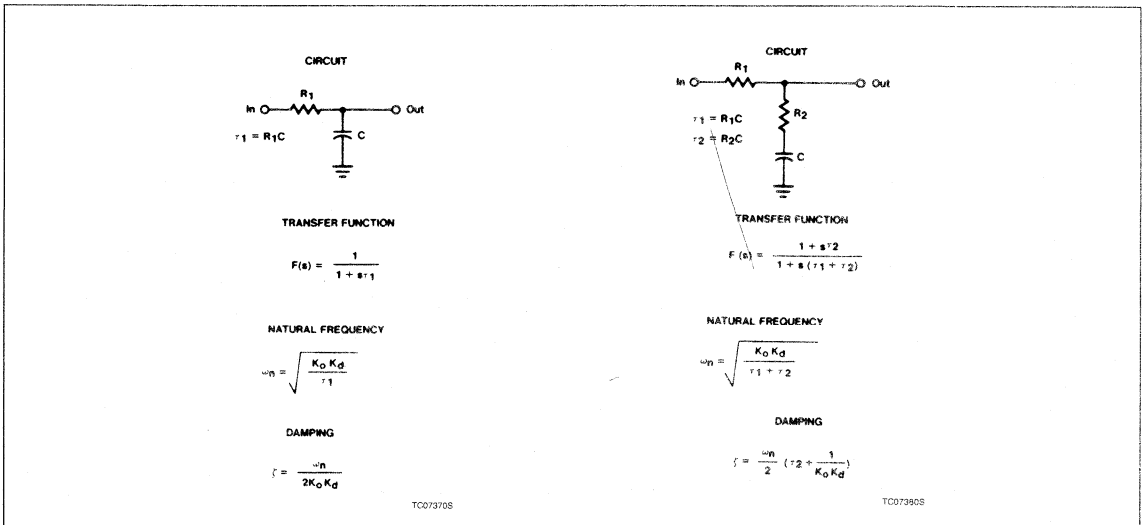
$$M_p = 1 + e^{-\zeta\pi/\sqrt{1-\zeta^2}} \qquad (68)$$

Examination of Figure 18 shows that the normalized peak overshoot of the error voltage is approximately 1.4. Using this value for M_p in Equation 68 gives a damping of $\zeta \cong 0.28$.

Another way of estimating damping is to make use of the frequency response plot measured for the natural frequency (ω_n) measurement. For low damping constants, the frequency response measurement peak will be a strong function of damping. For high damping constants, the 3dB down point will give the damping. Figure 19 tabulates some approximate relationships.

NOISE

The effect of input noise on loop operation is very difficult to predict. Briefly, the input noise



a. Simple b. Lag-Lead

Figure 16. First-Order Low-Pass Filters

components near the center frequency are converted to phase noise. When the phase noise becomes so great that the ± 90° permissible phase variation is exceeded, the loop drops out of lock or fails to acquire lock. The best technique is to actually apply the anticipated noise amplitude and bandwidth to the input and then perform the capture and lock range measurements as well as perform operating tests with the anticipated input level and modulation deviations. By including a small safety factor in the loop design to compensate for small processing variations, satisfactory operation can be assured.

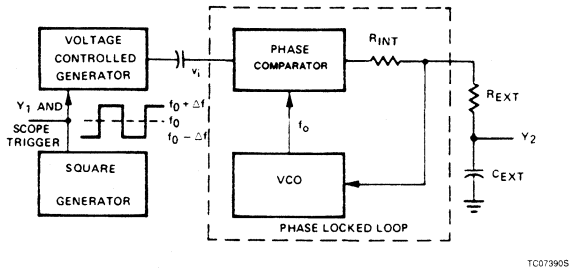
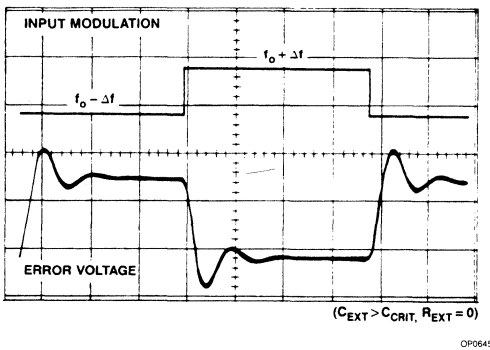
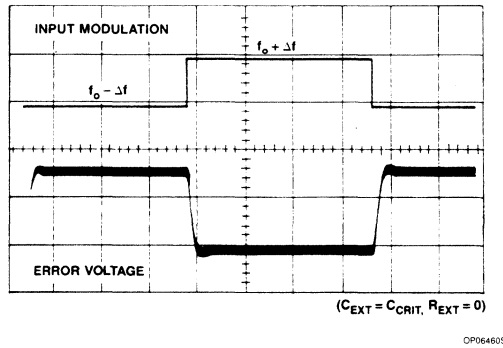


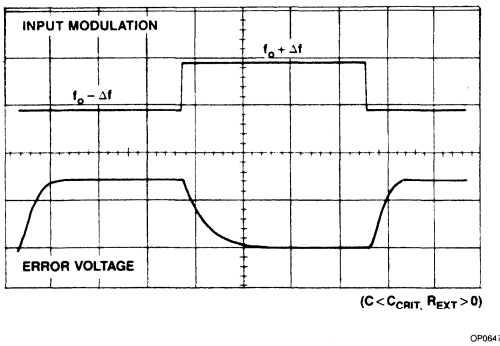
Figure 17. Measurement Setup for Display of PLL Transient Response



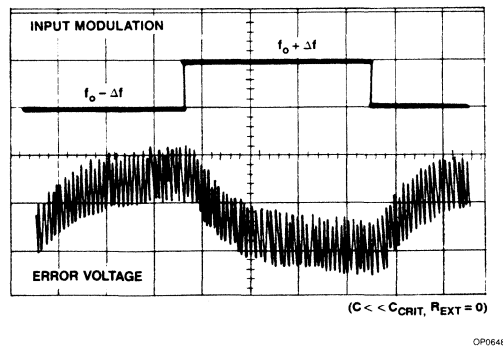
a. Underdamped With $\zeta \simeq 0.28$



b. Critically Damped With $\zeta \simeq 1.0$

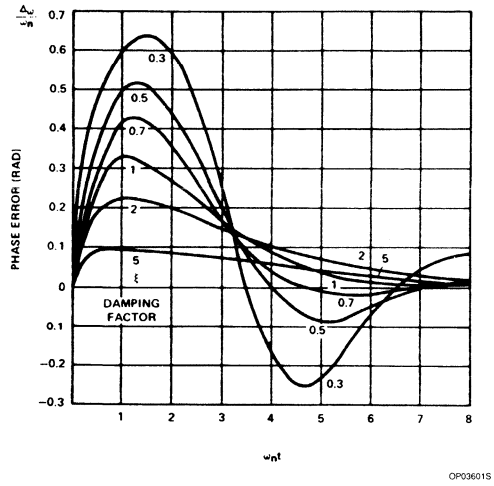


c. Overdamped With $\zeta \simeq 10$



d. Highly Overdamped With $\zeta > 10$

Figure 18. Transient Response of PLL Error Voltage to Square Wave Frequency Modulation for Various Damping Conditions



a. Transient Phase Error as an Indication of Damping

ζ	PEAK AMPLITUDE / LOW FREQUENCY AMPLITUDE	ω − 3dB / ωn
0.3	6.0dB	1.8
0.5	3.2dB	2.1
0.7	2.2dB	2.5
1.0	1.3dB	4.3
5.0	0.5dB	10

b. Ratio of Peak Amplitude to Low Frequency Amplitude of Error Voltage From Modulating Frequency Response

Figure 19. Estimating the Damping in a Second-Order PLL

NE/SE564
Phase-Locked Loop

Product Specification

DESCRIPTION

The NE564 is a versatile, high guaranteed frequency phase-locked loop designed for operation up to 50MHz. As shown in the Block Diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

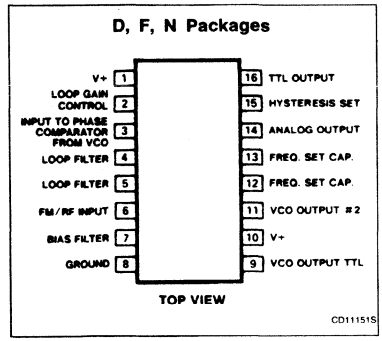
FEATURES

- **Operation with single 5V supply**
- **TTL-compatible inputs and outputs**
- **Guaranteed operation to 50MHz**
- **External loop gain control**
- **Reduced carrier feedthrough**
- **No elaborate filtering needed in FSK applications**
- **Can be used as a modulator**
- **Variable loop gain (externally controlled)**

APPLICATIONS

- **High-speed modems**
- **FSK receivers and transmitters**
- **Frequency synthesizers**
- **Signal generators**
- **Various satcom/TV systems**

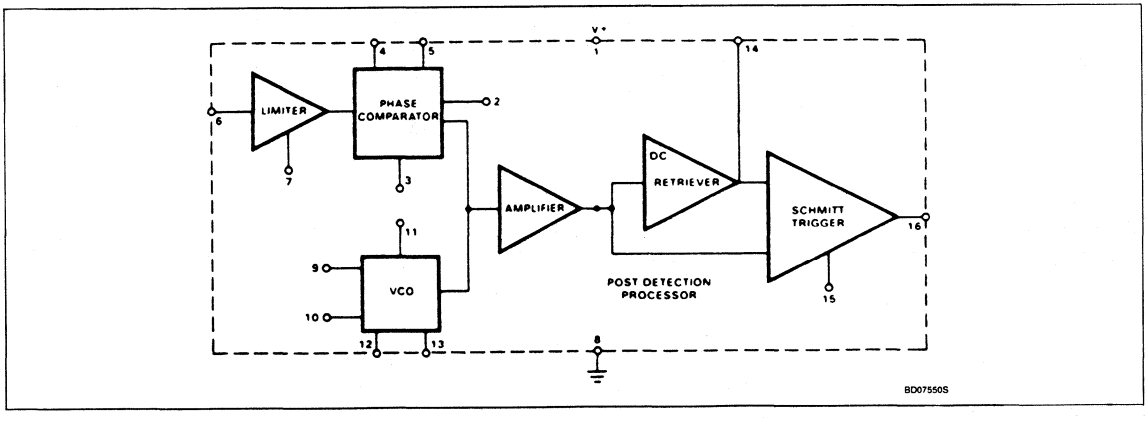
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE564D
16-Pin Plastic DIP	0 to +70°C	NE564N
16-Pin Plastic DIP	-55°C to +125°C	SE564N
16-Pin Cerdip	-55°C to +125°C	SE564F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+	Supply voltage Pin 1 Pin 10	 14 6	V
I_{OUT}	(Sink) Max (Pin 9)	10	mA
P_D	Power dissipation	600	mW
T_A	Operating ambient temperature NE SE	 0 to +70 −55 to +125	°C
T_{STG}	Storage temperature	−65 to +150	°C

NOTE:
Operation above 5V will require heatsinking of the case.

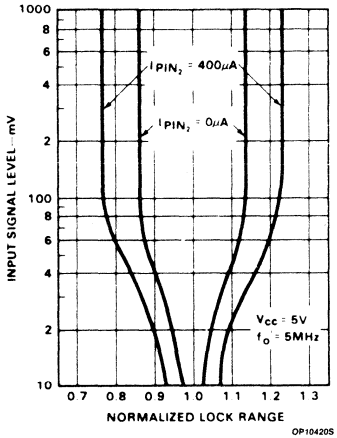
DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C, f_O = 5MHz, I_2 = 400μA, unless otherwise specified.

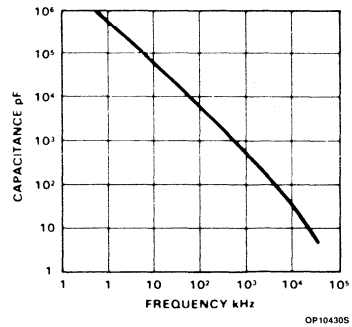
SYMBOL	PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Maximum VCO frequency	C_1 = 0 (stray)	50	65		45	60		MHz
	Lock range	Input ≥ 200mV$_{RMS}$ T_A = 25°C T_A = 125°C T_A = −55°C T_A = 0°C T_A = 70°C	40 20 50	70 30 80		40	70 70 40		% of f_O
	Capture range	Input ≥ 200mV$_{RMS}$, R_2 = 27Ω	20	30		20	30		% of f_O
	VCO frequency drift with temperature	f_O = 5MHz, T_A = −55°C to +125°C T_A = 0 to +70°C = 0 to +70°C f_O = 500kHz, T_A = −55°C to +125°C T_A = 0 to +70°C		500 300	1500 800		 600 500		PPM/°C
	VCO free-running frequency	C_1 = 91pF R_C = 100Ω "Internal"	4	5	6	3.5	5	6.5	MHz
	VCO frequency change with supply voltage	V_{CC} = 4.5V to 5.5V		3	8		3	8	% of f_O
	Demodulated output voltage	Modulation frequency: 1kHz f_O = 5MHz, input deviation: 2%T = 25°C 1%T = 25°C 1%T = 0°C 1%T = −55°C 1%T = 70°C 1%T = 125°C	 16 8 6 12	 28 14 10 16		 16 8	 28 14 13 15		 mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$
	Distortion	Deviation: 1% to 8%		1			1		%
S/N	Signal-to-noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
	AM rejection	Std. condition, 30% AM		35			35		dB
	Demodulated output at operating voltage	Modulation frequency: 1kHz f_O = 5MHz, input deviation: 1% V_{CC} = 4.5V V_{CC} = 5.5V	 7 8	 12 14		 7 8	 12 14		 mV$_{RMS}$ mV$_{RMS}$
I_{CC}	Supply current	V_{CC} = 5V I_1, I_{10}		45	60		45	60	mA
	Output "1" output leakage current "0" output voltage	 V_{OUT} = 5V, Pins 16, 9 I_{OUT} = 2mA, Pins 16, 9 I_{OUT} = 6mA, Pins 16, 9		 1 0.3 0.4	 20 0.6 0.8		 1 0.3 0.4	 20 0.6 0.8	 μA V V

TYPICAL PERFORMANCE CHARACTERISTICS

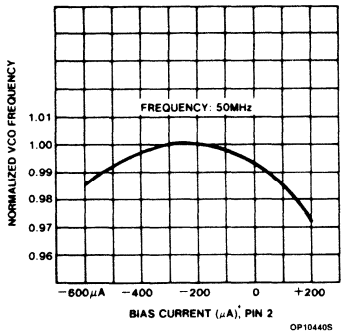
Lock Range vs Signal Input



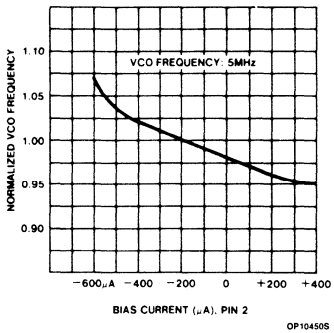
VCO Capacitor vs Frequency



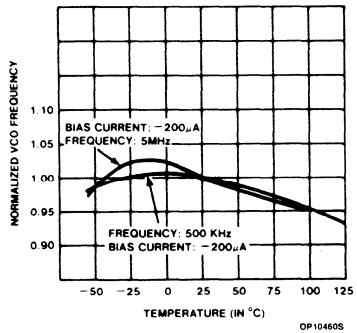
Typical Normalized VCO Frequency as a Function of Pin 2 Bias Current



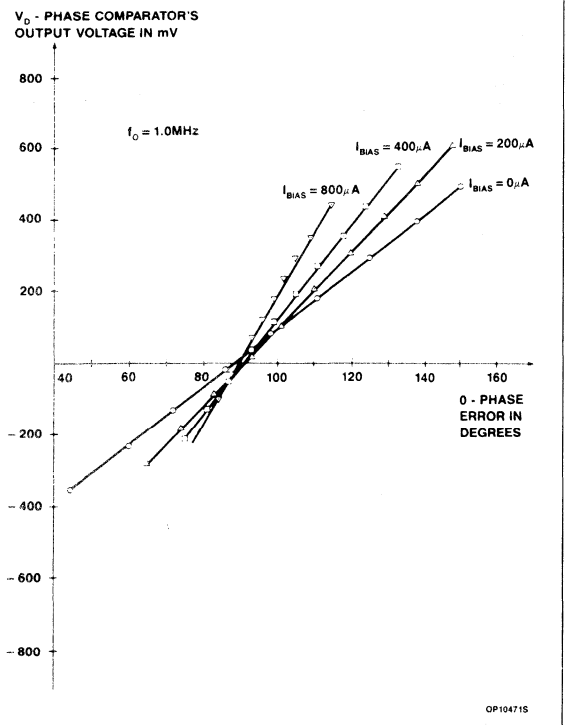
Typical Normalized VCO Frequency as a Function of Pin 2 Bias Current



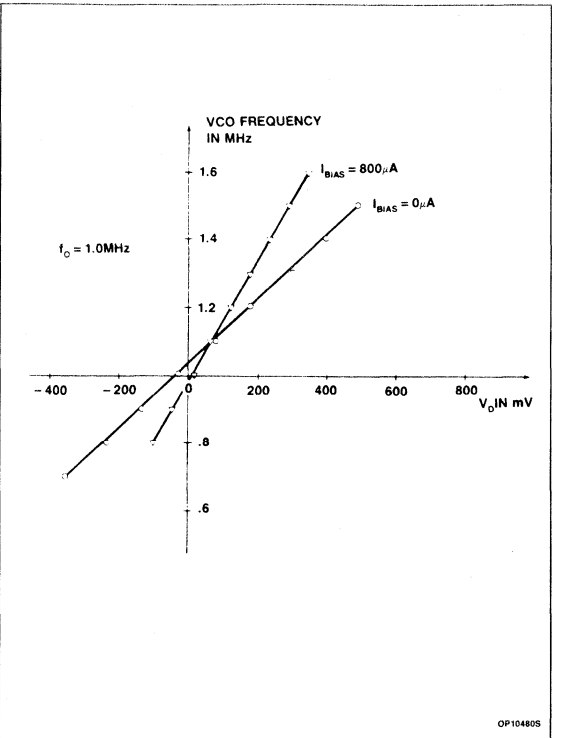
Normalized VCO Frequency as a Function of Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

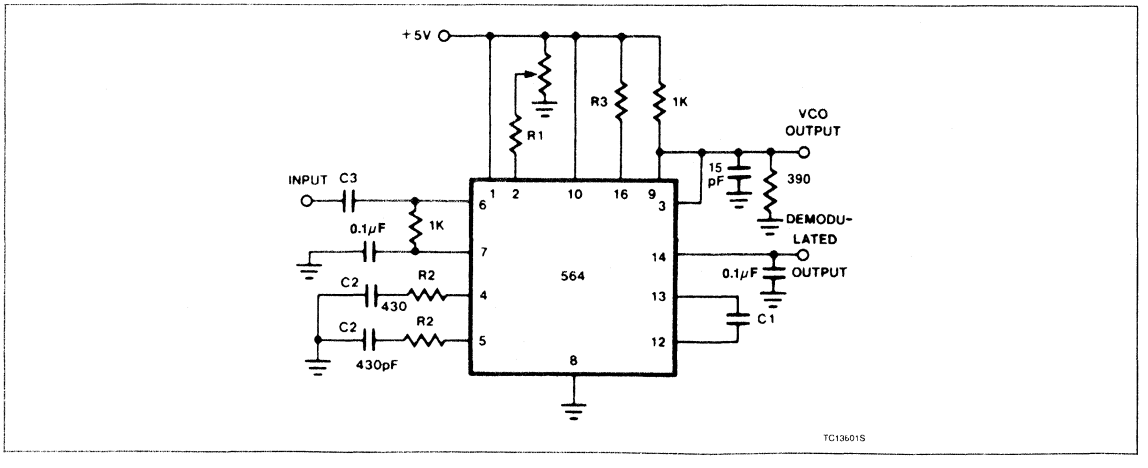


Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current (K_D)



VCO Output Frequency as a Function of Input Voltage and Bias Current (K_O)

TEST CIRCUIT



FUNCTIONAL DESCRIPTION (Figure 1)

The NE564 is a monolithic phase-locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz.

In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{IN} - f_O)}{K_{VCO}} \quad (1)$$

K_{VCO} = conversion gain of the VCO

f_{IN} = frequency of the input signal

f_O = free-running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{IN} from f_O. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at Pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free-running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the DC levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow-band signals where the deviation in f_{IN} itself may be less than the change in f_O due to temperature. This effect can be eliminated if the DC or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the DC levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high-frequency performance, an emitter-coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q_{21} and Q_{23} with current sources $Q_{25} - Q_{26}$ form the basic oscillator. The approximate free-running frequency of the oscillator is shown in the following equation:

$$f_O \simeq \frac{1}{22\ R_C\ (C_1 + C_S)} \quad (2)$$

EQUIVALENT SCHEMATIC

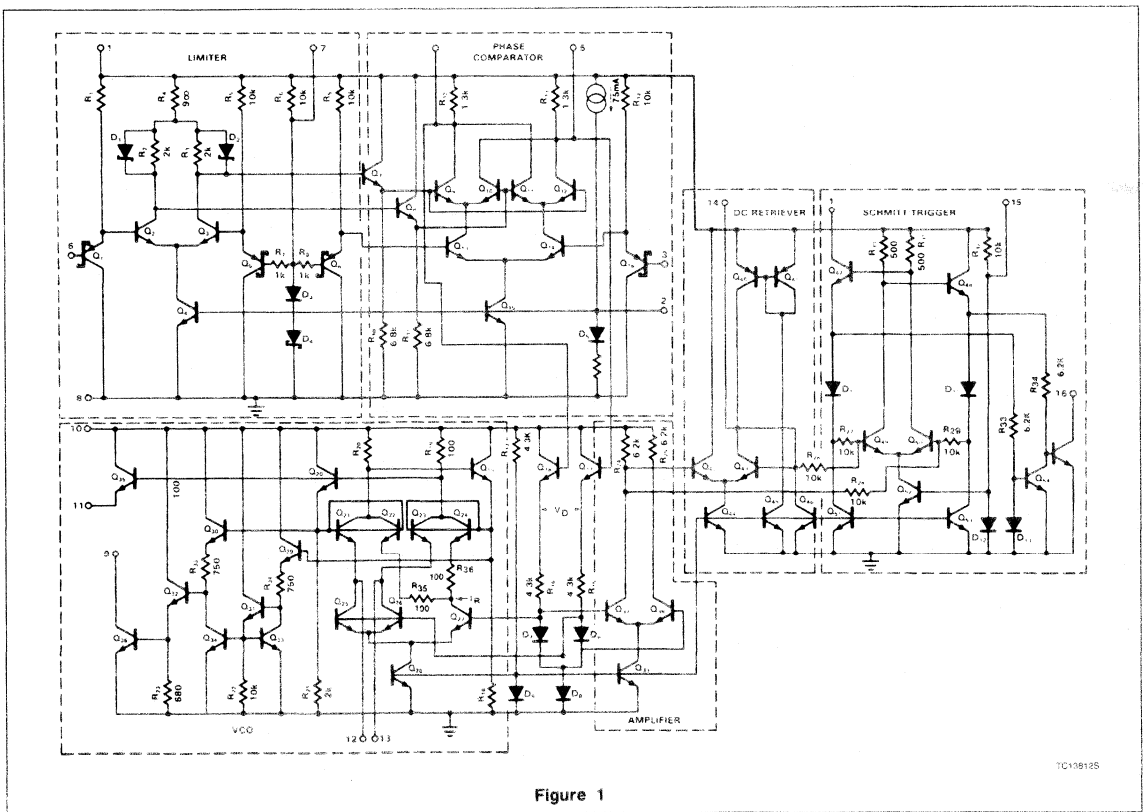


Figure 1

$R_C = R_{19} = R_{20} = 100\Omega$ (INTERNAL)

C_1 = external frequency setting capacitor

C_S = stray capacitance

Variation of V_D (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double-balanced modulator with a limiter amplifier to improve AM rejection. Schottky-clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at Pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a DC retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the DC retriever is formed by the transductance amplifier $Q_{42} - Q_{43}$ together with an external capacitor which is connected at the amplifier output (Pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_M}{C_2} V_{IN} dt \qquad (3)$$

g_M = transconductance of the amplifier

C_2 = capacitor at the output (Pin 14)

V_{IN} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the DC or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

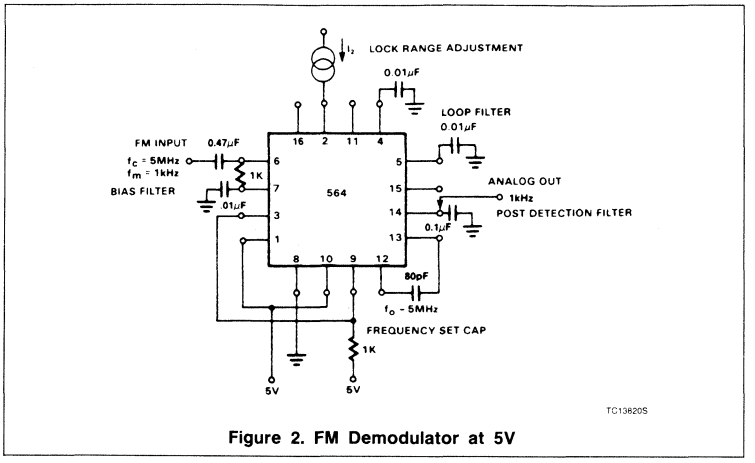


Figure 2. FM Demodulator at 5V

The comparator with hysteresis is made up of $Q_{49} - Q_{50}$ with positive feedback being provided by $Q_{47} - Q_{48}$. The hysteresis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a DC control, provides symmetric variation around the nominal value.

Design Formula

The free-running frequency of the VCO is shown by the following equation:

$$f_O \simeq \frac{1}{22\ R_C\ (C_1 + C_S)} \qquad (4)$$

$R_C = 100\Omega$

C_1 = external cap in farads

C_S = stray capacitance

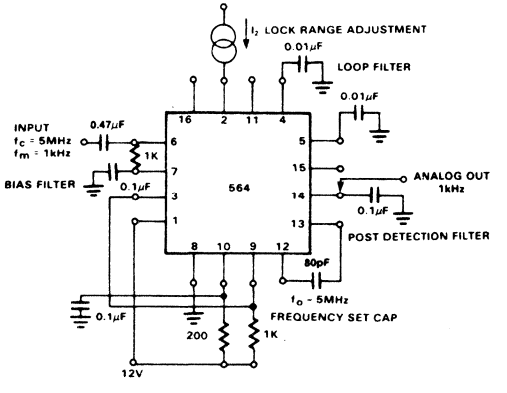


Figure 3. FM Demodulator at 12V

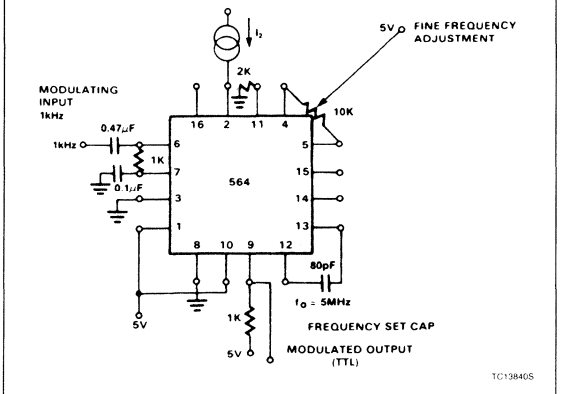


Figure 4. Modulator

The loop filter diagram shown is explained by the following equation:

$$F_S = \frac{1}{1 + sRC_3} \text{ (First Order)} \quad (5)$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (Internal)*

By adding capacitors to Pins 4 and 5, a pole is added to the loop transfer function at

$$\omega = \frac{1}{RC_3}$$

NOTE:
*Refer to Figure 1.

APPLICATIONS

FM Demodulator

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in Figures 2 and 3, respectively. The input signal is AC coupled with the output signal being extracted at Pin 14. Loop filtering is provided by the capacitors at Pins 4 and 5 with additional filtering being provided by the capacitor at Pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be 1% or higher.

Modulation Techniques

The NE564 phase-locked loop can be modulated at either the loop filter ports (Pins 4 and 5) or the input port (Pin 6) as shown in Figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in Figure 5. This curve will be appropriate for signals injected into Pins 4 and 5 as shown in Figure 4.

FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5V power supply. Demodulated DC voltages associated with the mark and space frequencies are recovered with a single external capacitor in a DC retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high-frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 5 shows a high-frequency FSK decoder designed for input frequency deviations of ± 1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from Figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' to 10.8MHz.

The lock range graph indicates that the ± 1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero Pin 2 bias current. (While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_O' frequencies).

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 7 for 20k, 500k, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators' output voltages with respect to each other and to the FSK output. The high-frequency sum components of the input and VCO frequency also are visible as noise on the phase comparator's outputs.

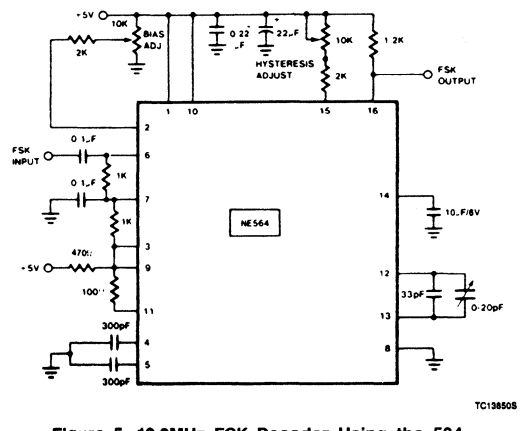
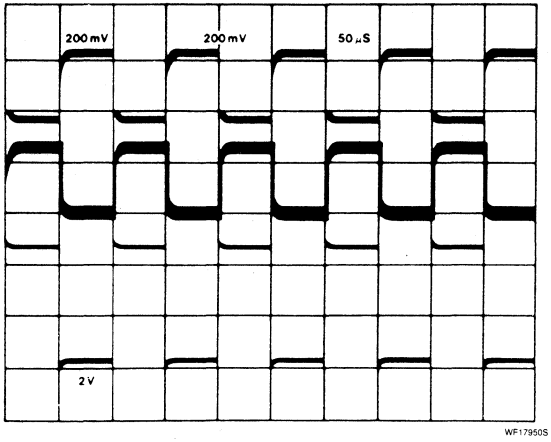
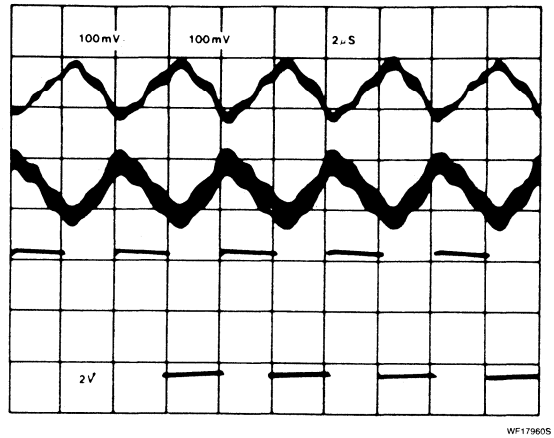


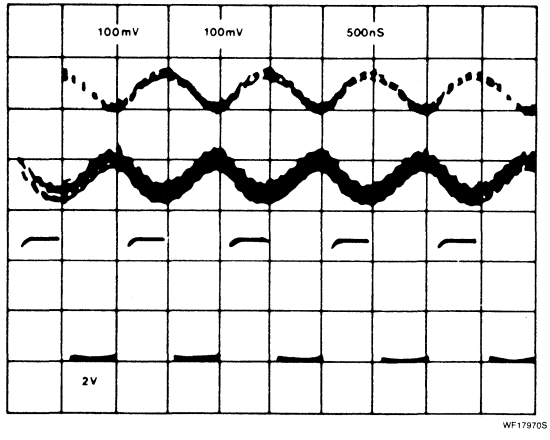
Figure 5. 10.8MHz FSK Decoder Using the 564



a. Data Rate = 20k Baud



b. Data Rate = 500k Baud



c. Data Rate = 2.0m Baud

NOTES:
1. Top trace = Pin 4
2. Center trace = Pin 5
3. Bottom trace = Pin 16

Figure 6. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs

OUTLINE OF SETUP PROCEDURE

1. Determine operating frequency of the VCO:

   If ÷ N in feedback loop, then $f_O = N \times f_{IN}$.
2. Calculate value of the VCO frequency set capacitor:

$$C_O \simeq \frac{1}{2200\ f_O}$$

3. Set I_2 (current sinking into Pin 2) for ≅ 100μA. After operation is obtained, this value may be adjusted for best dynamic behavior.
4. Check VCO output frequency with digital counter at Pin 9 of device (loop open, VCO to ϕ det.). Adjust C_O trim or frequency adj. Pins 4 – 5 for exact center frequency, if needed.
5. Close loop and inject input signal to Pin 6. Monitor Pins 3 and 6 with two-channel scope. Lock should occur with $\Delta\phi_{3-6}$ equal to 90° (phase error).
6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pins 4 and 5. (See PLL application section).
7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not 50% in

duty cycle, DC offsets will occur in the loop which tend to create an artificial or biased VCO offset.

8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of 10 – 50μF on Pins 4, 5. Also, careful supply decoupling may be necessary. This includes the counter chain V_{CC} lines.

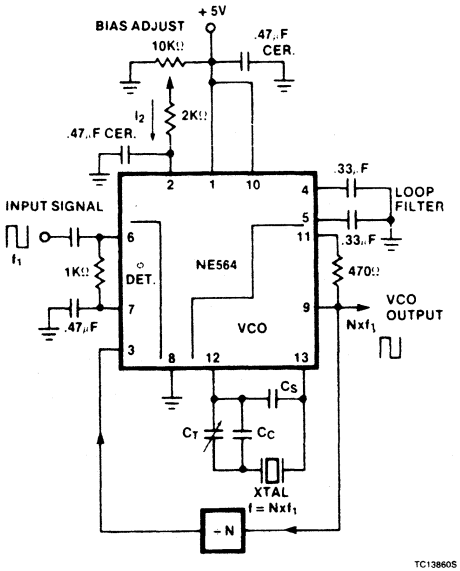


Figure 7. NE564 Phase-Locked Frequency Multiplier with VCXO

NE/SE565
Phase-Locked Loop

Product Specification

DESCRIPTION

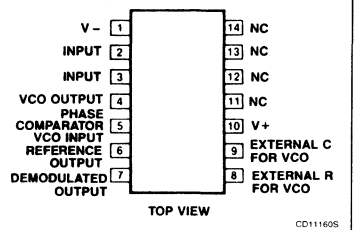
The NE/SE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low pass filter as shown in the Block Diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

FEATURES

- **Highly stable center frequency (200ppm/°C typ.)**
- **Wide operating voltage range (± 6V to ± 12V)**
- **Highly linear demodulated output (0.2% typ.)**
- **Center frequency programming by means of a resistor or capacitor, voltage or current**
- **TTL and DTL compatible square wave output; loop can be opened to insert digital frequency divider**
- **Highly linear triangle wave output**
- **Reference output for connection of comparator in frequency discriminator**
- **Bandwidth adjustable from < ± 1% to > ± 60%**
- **Frequency adjustable over 10 to 1 range with same capacitor**

PIN CONFIGURATIONS

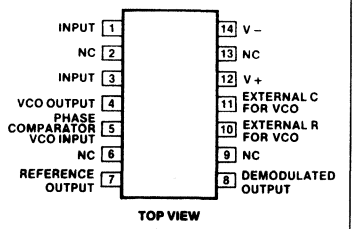
F, N Packages



TOP VIEW

CD11160S

D Package[1]

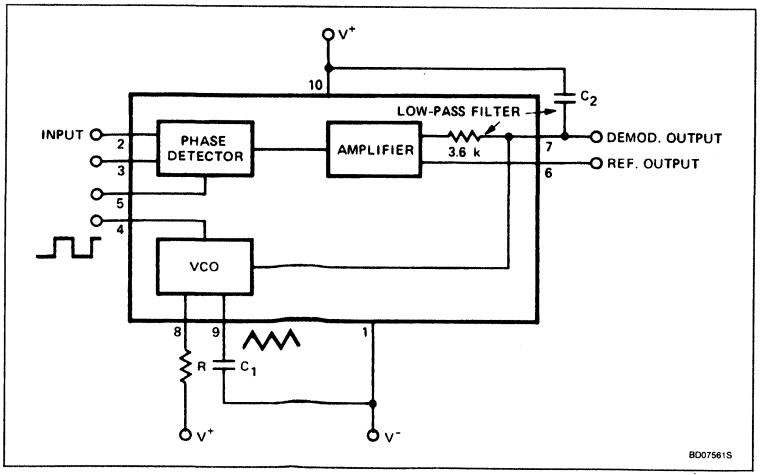


TOP VIEW

CD11170S

NOTE:
1. SO and non-standard pin out.

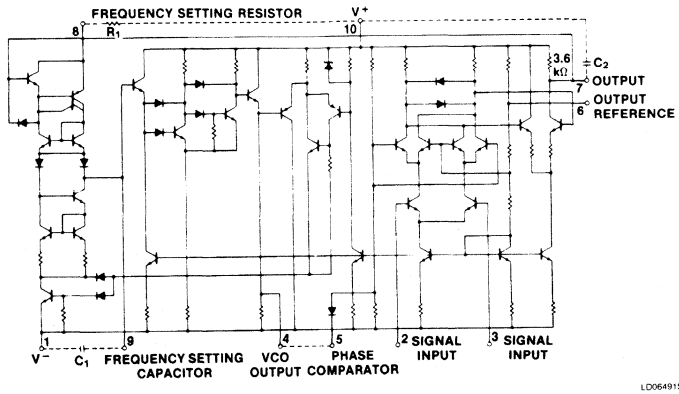
BLOCK DIAGRAM



APPLICATIONS

- **Frequency shift keying**
- **Modems**
- **Telemetry receivers**
- **Tone decoders**
- **SCA receivers**
- **Wide-band FM discriminators**
- **Data synchronizers**
- **Tracking filters**
- **Signal restoration**
- **Frequency multiplication & division**

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE565D
14-Pin Cerdip	0 to +70°C	NE565F
14-Pin Plastic DIP	0 to +70°C	NE565N
14-Pin Cerdip	−55°C to +125°C	SE565F
14-Pin Plastic DIP	−55°C to +125°C	SE565N

ABSOLUTE MAXIMUM RATINGS T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V+	Maximum operating voltage	26	V
V_{IN}	Input voltage	3	V_{P-P}
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range NE565 SE565	 0 to +70 −55 to +125	 °C °C
P_D	Power dissipation	300	mW

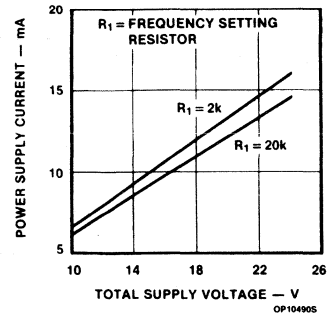
DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 6V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE565			NE565			UNIT
			Min	Typ	Max	Min	Typ	Max	
Supply requirements									
V_{CC}	Supply voltage		±6		±12	±6		±12	V
I_{CC}	Supply current			8	12.5		8	12.5	mA
Input characteristics									
	Input impedance[1]		7	10		5	10		kΩ
	Input level required for tracking	f_O = 50kHz, ±10% frequency deviation	10			10			mV_{RMS}
VCO characteristics									
f_C	Center frequency Maximum value distribution[2]	 Distribution taken about f_O = 50kHz, R_1 = 5.0kΩ, C_1 = 1200pF	300 −10	500 0	 +10	 −30	500 0	 +30	kHz %
	Drift with temperature Drift with supply voltage	f_O = 50kHz f_O = 50kHz, V_{CC} = ±6 to ±7V		500 0.1	 1.0		600 0.2	 1.5	ppm/°C %/V
	Triangle wave output voltage level linearity		1.9	2.4 0.2	3	1.9	2.4 0.5	3	V_{P-P} %
	Square wave logical "1" output voltage logical "0" output voltage	 f_O = 50kHz f_O = 50kHz	 +4.9	 +5.2 −0.2	 +0.2	 +4.9	 +5.2 −0.2	 +0.2	 V V
	Duty cycle	f_O = 50kHz	45	50	55	40	50	60	%
t_R	Rise time			20	100		20		ns
t_F	Fall time			50	200		50		ns
I_{SINK}	Output current (sink)		0.6	1		0.6	1		mA
I_{SOURCE}	Output current (source)		5	10		5	10		mA
Demodulated output characteristics									
V_{OUT}	Output voltage level	Measured at Pin 7	4.25	4.5	4.75	4.0	4.5	5.0	V
	Maximum voltage swing[3]			2			2		V_{P-P}
	Output voltage swing	±10% frequency deviation	250	300		200	300		mV_{P-P}
THD	Total harmonic distortion			0.2	0.75		0.4	1.5	%
	Output impedance[4]			3.6			3.6		kΩ
V_{OS}	Offset voltage (V6 − V7)			30	100		50	200	mV
	Offset voltage vs temperature (drift)			50			100		µV/°C
	AM rejection		30	40			40		dB

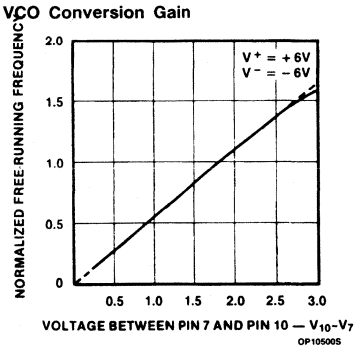
NOTES:
1. Both input terminals (Pins 2 and 3) must receive identical DC bias. This bias may range from 0V to −4V.
2. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20kΩ.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS

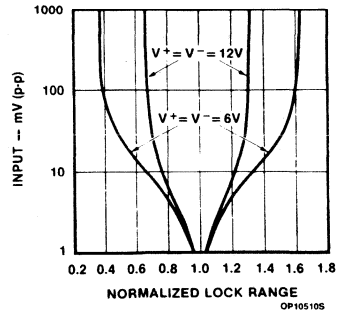
Power Supply Current as a Function of Supply Voltage



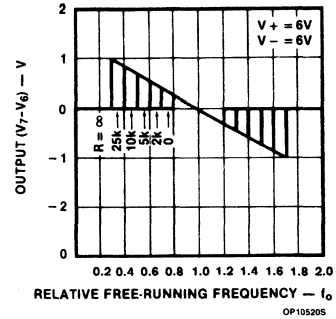
VCO Conversion Gain



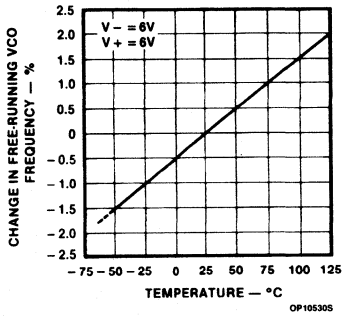
Lock Range as a Function of Input Voltage



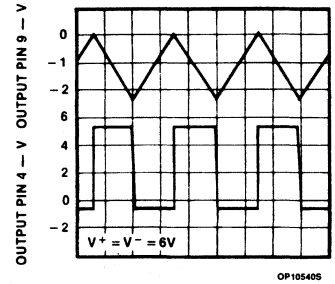
Lock Range as a Function of Gain Setting Resistance (Pins 6 – 7)



Change in Free-Running VCO Frequency as a Function of Temperature



VCO Output Waveform



DESIGN FORMULAS (See Figure 1)

Free-running frequency of VCO:

$$f_O \simeq \frac{1.2}{4R_1C_1} \text{ in Hz}$$

Lock range: $f_L = \pm \frac{8f_O}{V_{CC}}$ in Hz

Capture range: $f_C \simeq \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6 \times 10^3) \times C_2$

TYPICAL APPLICATIONS

FM Demodulation

The 565 Phase-Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average DC level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically ± 60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$$f_O \simeq \frac{1.2}{4R_1C_1}$$

and should be adjusted to be at the center of the input signal frequency range. C_1 can be any value, but R_1 should be within the range of 2000 to 20,000Ω with an optimum value on the order of 4000Ω. The source can be direct coupled if the DC resistances seen from Pins 2 and 3 are equal and there is no DC voltage difference between the pins. A short between Pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a DC reference voltage that is close to the DC potential of the demodulated output (Pin 7). Thus, if a resistance is connected between Pins 6 and 7, the gain of the output stage can be reduced with little change in the DC voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ± 60% of f_O to approximately ± 20% of f_O (at ± 6V).

A small capacitor (typically 0.001μF) should be connected between Pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between Pin 7 and the positive supply, and an internal resistance of approximately 3600Ω.

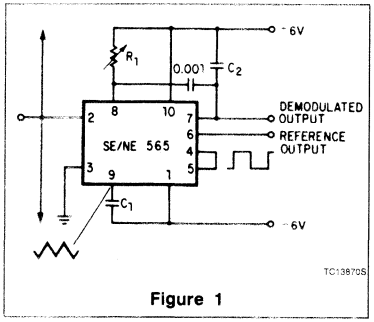


Figure 1

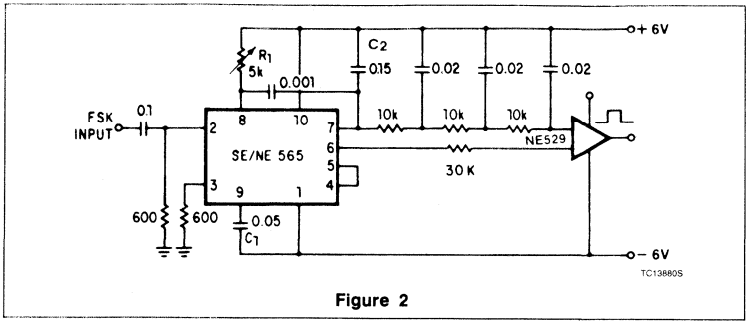


Figure 2

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" to "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding DC shift at the output.

The loop filter capacitor C_2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and Pin 6 of the loop. The free-running frequency is adjusted with R_1 so as to result in a slightly-positive voltage at the output with f_{IN} = 1070Hz.

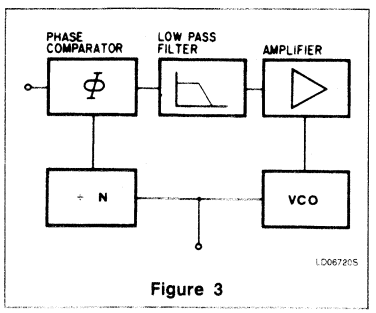


Figure 3

The input connection is typical for cases where a DC voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect at 600Ω input impedance).

Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R_1 and C_1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C_2, should be large enough to eliminate variations in the demodulated output voltage (at Pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_{IN}) as long as the loop is in lock.

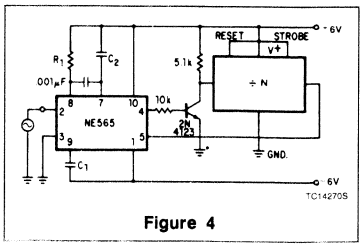


Figure 4

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use. To do this, a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase-Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (Pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000Ω.

Phase-Locked Loop

NE/SE565

The Phase-Locked Loop is tuned to 67kHz with a 5000Ω potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (Pin 7) passes through a three-stage low pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at Pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.

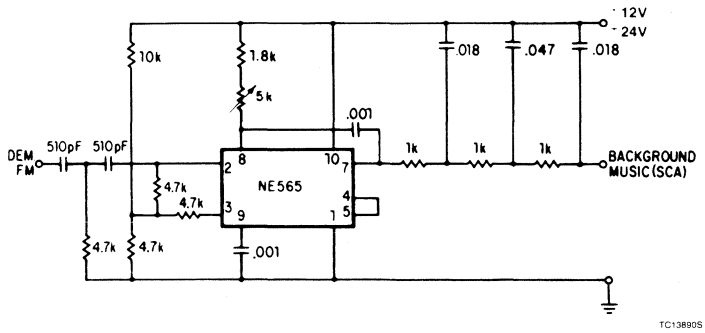


Figure 5

NE/SE566
Function Generator

Product Specification

DESCRIPTION

The NE/SE566 Function Generator is a voltage-controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten-to-one frequency range by proper selection of an external resistance and modulated over a ten-to-one range by the control voltage, with exceptional linearity.

FEATURES

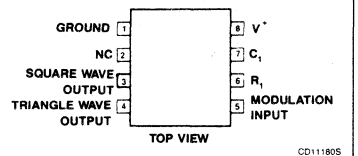
- **Wide range of operating voltage (up to 24V; single or dual)**
- **High linearity of modulation**
- **Highly stable center frequency (200ppm/°C typical)**
- **Highly linear triangle wave output**
- **Frequency programming by means of a resistor or capacitor, voltage or current**
- **Frequency adjustable over 10-to-1 range with same capacitor**

APPLICATIONS

- **Tone generators**
- **Frequency shift keying**
- **FM modulators**
- **Clock generators**
- **Signal generators**
- **Function generators**

PIN CONFIGURATIONS

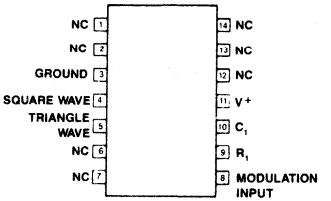
D, N Packages



TOP VIEW

CD11180S

F Package



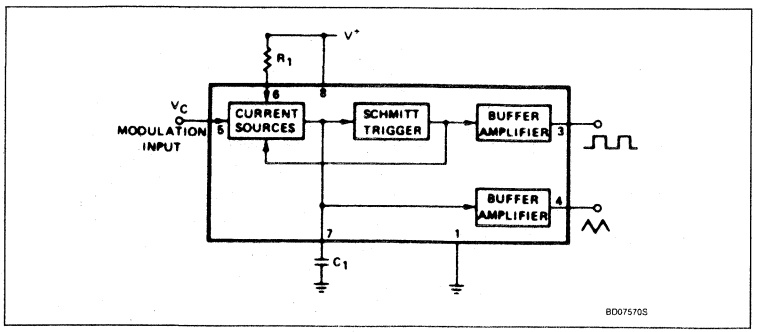
TOP VIEW

CD11191S

ORDERING INFORMATION

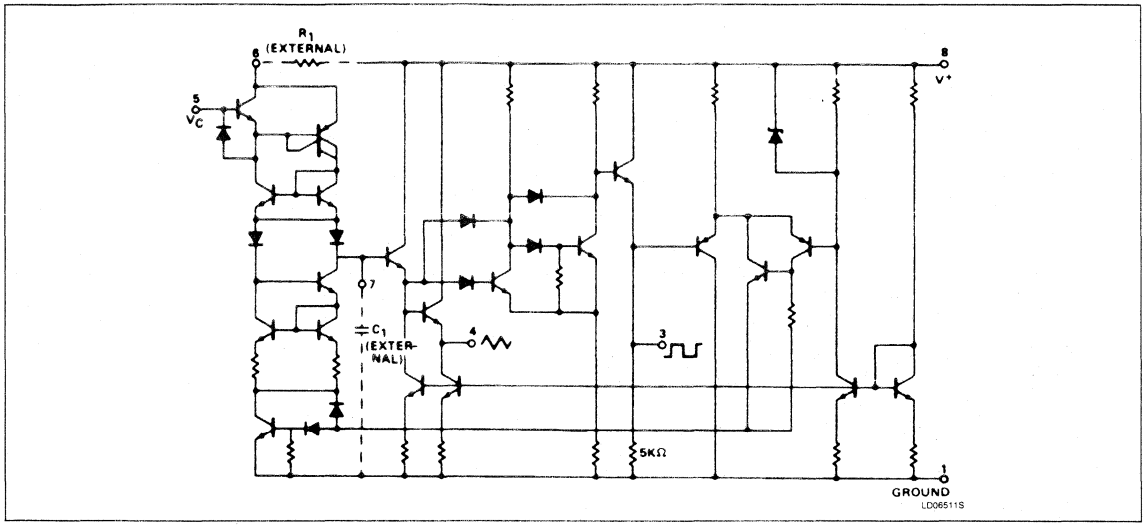
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE566D
14-Pin Cerdip	0 to +70°C	NE566F
8-Pin Plastic DIP	0 to +70°C	NE566N
14-Pin Cerdip	−55°C to +125°C	SE566F
8-Pin Plastic DIP	−55°C to +125°C	SE566N

BLOCK DIAGRAM



BD07570S

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+	Maximum operating voltage	26	V
V_{IN}	Input voltage	3	V_{P-P}
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range		
	NE566	0 to +70	°C
	SE566	−55 to +125	°C
P_D	Power dissipation	300	mW

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise specified.

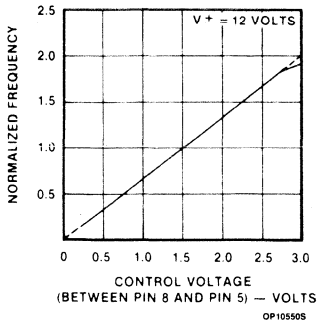
SYMBOL	PARAMETER	SE566			NE566			UNIT
		Min	Typ	Max	Min	Typ	Max	
General								
T_A	Operating ambient temperature range	−55		125	0		70	°C
V_{CC}	Operating supply voltage	±6		±12	±6		±12	V
I_{CC}	Operating supply current		7	12.5		7	12.5	mA
VCO[1]								
f_{MAX}	Maximum operating frequency		1			1		MHz
	Frequency drift with temperature		500			600		ppm/°C
	Frequency drift with supply voltage		0.1	1		0.2	2	%/V
	Control terminal input impedance[2]		1			1		MΩ
	FM distortion (±10% deviation)		0.2	0.75		0.4	1.5	%
	Maximum sweep rate		1			1		MHz
	Sweep range		10:1			10:1		
Output								
	Triangle wave output							
	impedance		50			50		Ω
	voltage	1.9	2.4		1.9	2.4		V_{P-P}
	linearity		0.2			0.5		%
	Square wave input							
	impedance		50			50		Ω
	voltage	5	5.4		5	5.4		V_{P-P}
	duty Cycle	45	50	55	40	50	60	%
t_R	Rise time		20			20		ns
t_F	Fall Time		50			50		ns

NOTES:

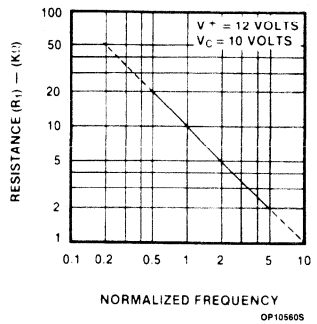
1. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20kΩ.
2. The bias voltage (V_C) applied to the control terminal (Pin 5) should be in the range $\frac{3}{4}V+ \leqslant V_C \leqslant V+$.

TYPICAL PERFORMANCE CHARACTERISTICS

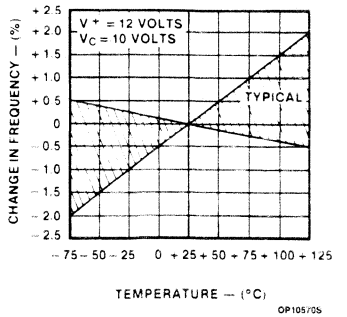
Normalized Frequency as a Function of Control Voltage



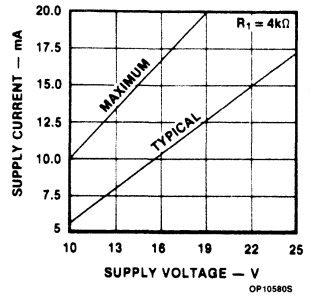
Normalized Frequency as a Function of Resistance (R1)



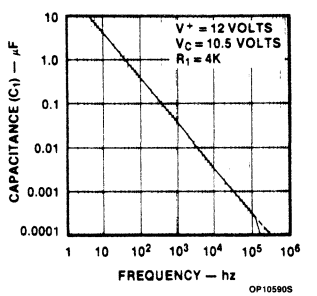
Change in Frequency as a Function of Temperature



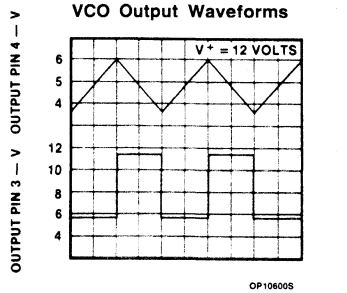
Power Supply Current as a Function of Supply Voltage



Frequency as a Function of Capacitance (C1)



VCO Output Waveforms



OPERATING INSTRUCTIONS

The NE/SE566 Function Generator is a general purpose voltage-controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1MHz. A typical connection diagram is shown in Figure 1. The control terminal (Pin 5) must be biased externally with a voltage (V_C) in the range

$$\tfrac{3}{4}V+ \leqslant V_C \leqslant V+$$

where V_{CC} is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3. The modulating signal is then AC coupled with the capacitor C_2. The modulating signal can be direct coupled as well, if the appropriate DC bias voltage is applied to the control terminal. The frequency is given approximately by

$$f_O = \frac{2[(V+) - (V_C)]}{R_1 C_1 V+}$$

and R_1 should be in the range $2k\Omega < R_1 < 20k\Omega$.

A small capacitor (typically $0.001\mu F$) should be connected between Pins 5 and 6 to eliminate possible oscillation in the control current source.

If the VCO is to be used to drive standard logic circuitry, it may be desirable to use a dual supply as shown in Figure 2. In this case the square wave output has the proper DC levels for logic circuitry. RTL can be driven directly from Pin 3. For DTL or TTL gates, which require a current sink of more than 1mA, it is usually necessary to connect a $5k\Omega$ resistor between Pin 3 and negative supply. This increases the current sinking capability to 2mA. The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for TTL circuitry which requires a fast fall time (< 50ns) and a large current sinking capability.

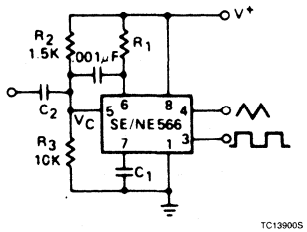


Figure 1

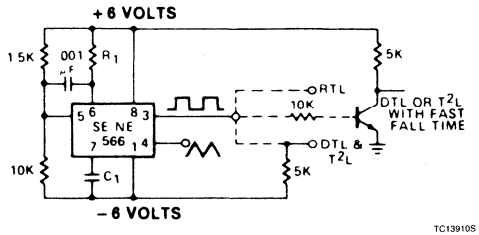


Figure 2

NE/SE567
Tone Decoder/Phase-Locked Loop

Product Specification

DESCRIPTION

The NE/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

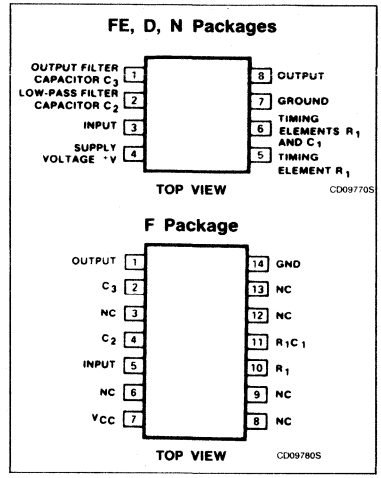
FEATURES

- **Wide frequency range (.01Hz to 500kHz)**
- **High stability of center frequency**
- **Independently controllable bandwidth (up to 14%)**
- **High out-band signal and noise rejection**
- **Logic-compatible output with 100mA current sinking capability**
- **Inherent immunity to false signals**
- **Frequency adjustment over a 20-to-1 range with an external resistor**
- **Military processing available**

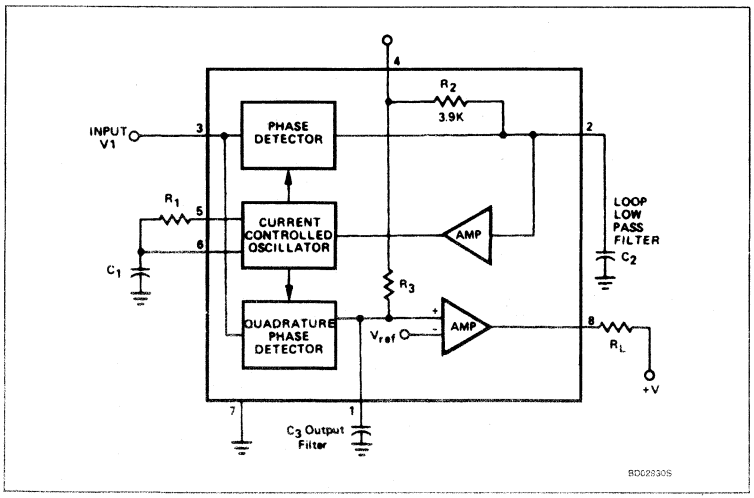
APPLICATIONS

- **Touch-Tone® decoding**
- **Carrier current remote controls**
- **Ultrasonic controls (remote TV, etc.)**
- **Communications paging**
- **Frequency monitoring and control**
- **Wireless intercom**
- **Precision oscillator**

PIN CONFIGURATIONS

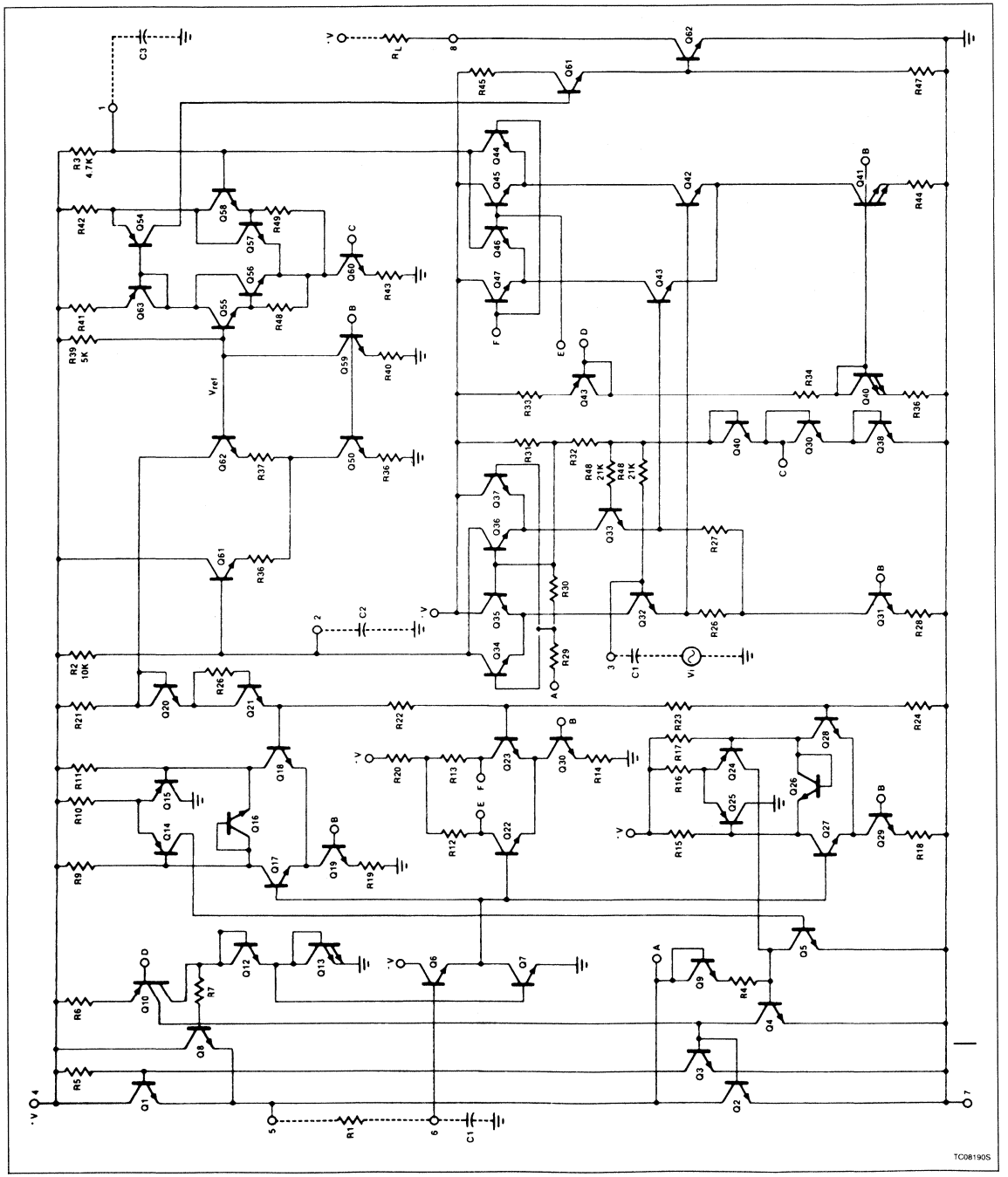


BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT & T.

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE567D
14-Pin Cerdip	0 to +70°C	NE567F
8-Pin Cerdip	0 to +70°C	NE567FE
8-Pin Plastic DIP	0 to +70°C	NE567N
8-Pin Plastic SO	−55°C to +125°C	SE567D
14-Pin Cerdip	−55°C to +125°C	SE567F
8-Pin Cerdip	−55°C to +125°C	SE567FE
8-Pin Plastic DIP	−55°C to +125°C	SE567N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature NE567 SE567	 0 to +70 −55 to +125	 °C °C
V_{CC}	Operating voltage	10	V
V+	Positive voltage at input	0.5 + V_S	V
V−	Negative voltage at input	−10	V_{DC}
V_{OUT}	Output voltage (collector of output transistor)	15	V_{DC}
T_{STG}	Storage temperature range	−65 to +150	°C
P_D	Power dissipation	300	mW

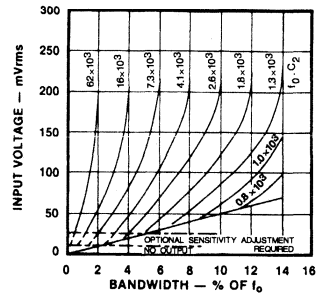
DC ELECTRICAL CHARACTERISTICS $V+ = 5.0V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
			Min	Typ	Max	Min	Typ	Max	
Center frequency[1]									
f_O	Highest center frequency			500			500		kHz
f_O	Center frequency stability[2]	−55 to +125°C 0 to +70°C		35 ±140 35 ±60			35 ±140 35 ±60		ppm/°C ppm/°C
f_O	Center frequency distribution	$f_O = 100kHz = \frac{1}{1.1\ R_1C_1}$	−10	0	+10	−10	0	+10	%
f_O	Center frequency shift with supply voltage	$f_O = 100kHz = \frac{1}{1.1\ R_1C_1}$		0.5	1		0.7	2	%/V
Detection bandwidth									
BW	Largest detection bandwidth	$f_O = 100kHz = \frac{1}{1.1\ R_1C_1}$	12	14	16	10	14	18	% of f_O
BW	Largest detection bandwidth skew			2	4		3	6	% of f_O
BW	Largest detection bandwidth — variation with temperature	$V_I = 300mV_{RMS}$		±0.1			±0.1		%/°C
BW	Largest detectionbandwidth — variation with supply voltage	$V_I = 300mV_{RMS}$		±2			±2		%/V
Input									
R_{IN}	Input resistance		15	20	25	15	20	25	kΩ
V_I	Smallest detectable input voltage[4]	$I_L = 100mA$, $f_I = f_O$		20	25		20	25	mV_{RMS}
	Largest no-output input voltage[4]	$I_L = 100mA$, $f_I = f_O$	10	15		10	15		mV_{RMS}
	Greatest simultaneous out-band signal-to-in-band signal ratio			+6			+6		dB
	Minimum input signal to wide-band noise ratio	$B_n = 140kHz$		−6			−6		dB
Output									
	Fastest on-off cycling rate			$f_O/20$			$f_O/20$		
	"1" output leakage current	$V_8 = 15V$		0.01	25		0.01	25	μA
	"0" output voltage	$I_L = 30mA$ $I_L = 100mA$		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V V
t_F	Output fall time[3]	$R_L = 50Ω$		30			30		ns
t_R	Output rise time[3]	$R_L = 50Ω$		150			150		ns
General									
V_{CC}	Operating voltage range		4.75		9.0	4.75		9.0	V
	Supply current quiescent			6	8		7	10	mA
	Supply current — activated	$R_L = 20kΩ$		11	13		12	15	mA
t_{PD}	Quiescent power dissipation			30			35		mW

NOTES:
1. Frequency determining resistor R_1 should be between 2 and 20kΩ.
2. Applicable over 4.75V to 5.75V. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.
4. With $R_2 = 130kΩ$ from Pin 1 tc V+. See Figure 1.

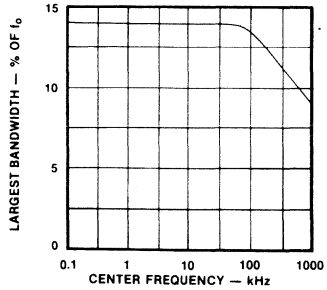
TYPICAL PERFORMANCE CHARACTERISTICS

Bandwidth vs Input Signal Amplitude



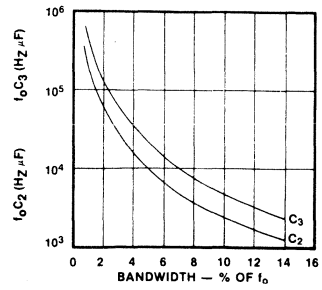
OP04280S

Largest Detection Bandwidth vs Operating Frequency



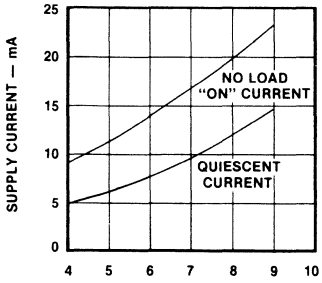
OP04290S

Detection Bandwidth as a Function of C_2 and C_3



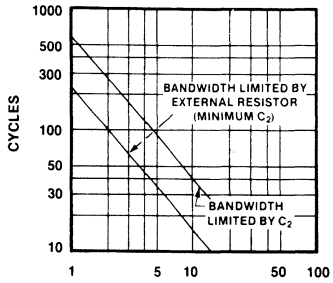
OP04300S

Typical Supply Current vs Supply Voltage



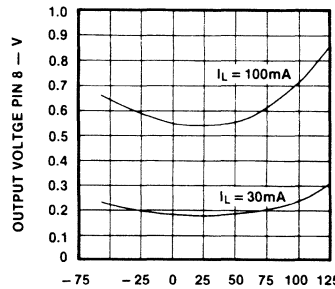
OP04310S

Greatest Number of Cycles Before Output

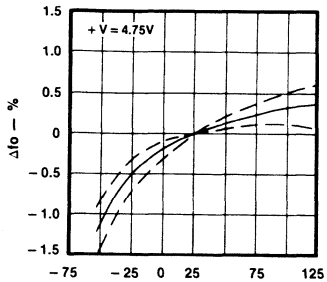


OP04320S

Typical Output Voltage vs Temperature

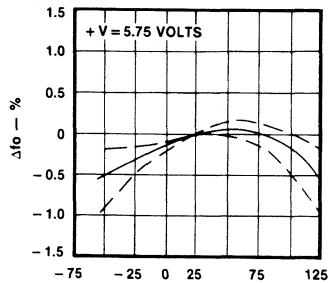


Typical Frequency Drift With Temperature (Mean and SD)



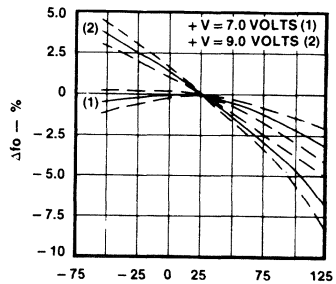
OP04340S

Typical Frequency Drift With Temperature (Mean and SD)



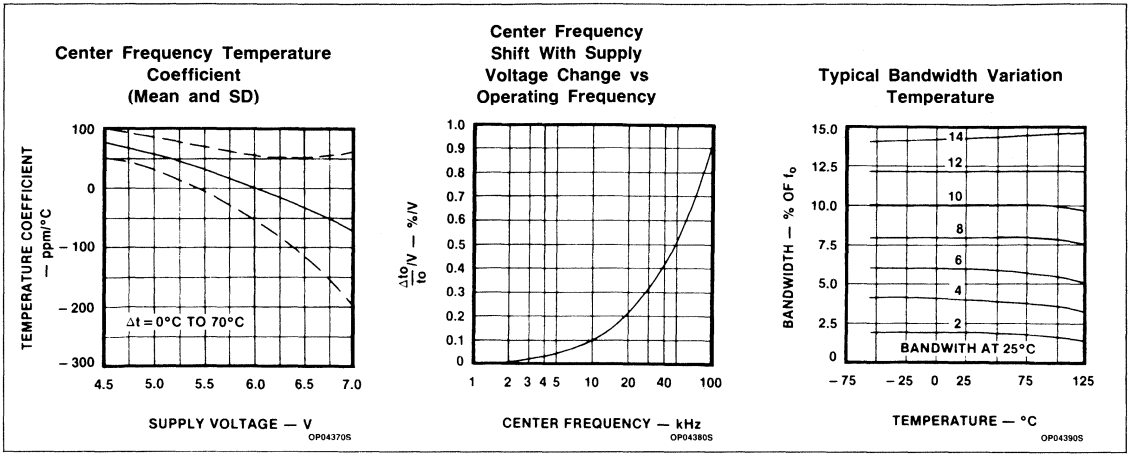
OP04350S

Typical Frequency Drift With Temperature (Mean and SD)



OP04360S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



DESIGN FORMULAS

$$f_O \cong \frac{1}{1.1R_1C_1}$$

$$BW \simeq 1070\sqrt{\frac{V_I}{f_OC_2}} \text{ in \% of } f_O,$$

$$V_I \leqslant 200mV_{RMS}$$

Where

V_I = Input voltage (V_{RMS})

C_2 = Low-pass filter capacitor (μF)

PHASE-LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (f_O)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_O, within which an input signal above the threshold voltage (typically $20mV_{RMS}$) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

A measure of how well the detection band is centered about the center frequency, f_O. The skew is defined as $(f_{MAX}+f_{MIN}-2f_O)/2f_O$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

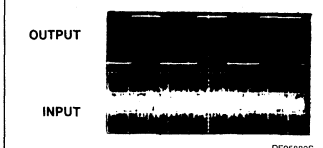
1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R_1C_1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.

TYPICAL RESPONSE



NOTE:
$R_L = 100\Omega$

Response to $100mV_{RMS}$ Tone Burst



NOTES:
S/N = –6dB
$R_L = 100\Omega$
Noise Bandwidth = 140Hz

Response to Same Input Tone Burst With Wideband Noise

2. Select the low-pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude Variation is known, the appropriate value of f_OC_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constand bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_OC_2 product (f_O (Hz), $C_2(\mu F)$).
3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low-pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the

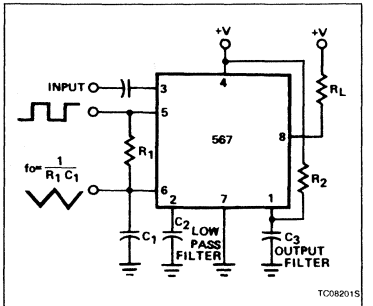


Figure 1

output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

4. Optional resistor R_2 sets the threshold for the largest "no output" input voltage. A value of 130kΩ is used to assure the tested limit of $10mV_{RMS}$ min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the "optional controls" section which follows.

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, Pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_O with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{BE}) \approx (+V - 1.4V)$ having a DC average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of $1V_{P-P}$ with an average DC level of +V/2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the inband signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_O/3$, $f_O/5$, etc.
2. The 567 will lock onto signals near $(2n + 1)$ f_O, and will give an output for signals near $(4n + 1)$ f_O where n = 0, 1, 2, etc. Thus, signals at $5f_O$ and $9f_O$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and out-band signals is afforded in the low input level (below $200mV_{RMS}$) and reduced bandwidth operating mode. However, decreased loop damping causes the worst-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can

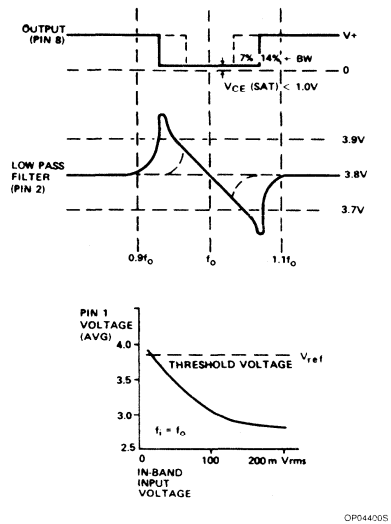


Figure 2

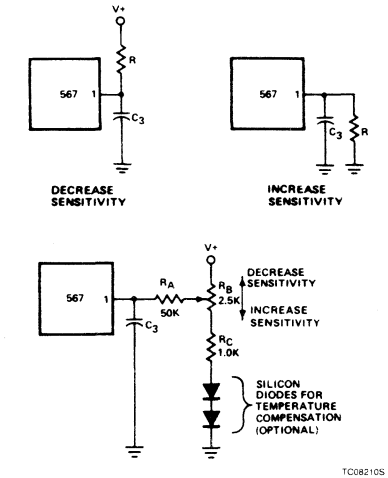


Figure 3

cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_O/10$ baud.

$$C_2 = \frac{130}{f_O}\mu F$$

$$C_3 = \frac{260}{f_O}\mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emmitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

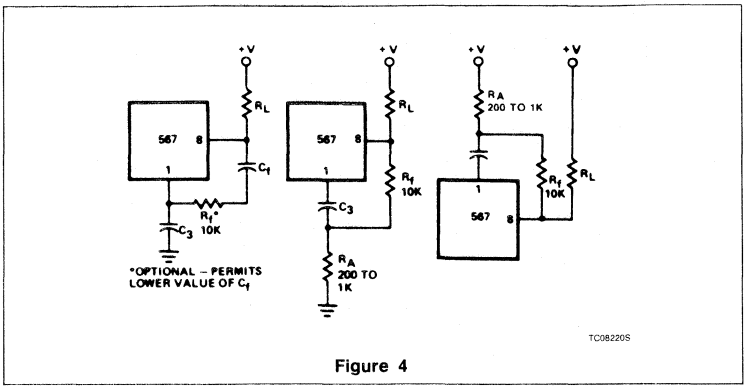


Figure 4

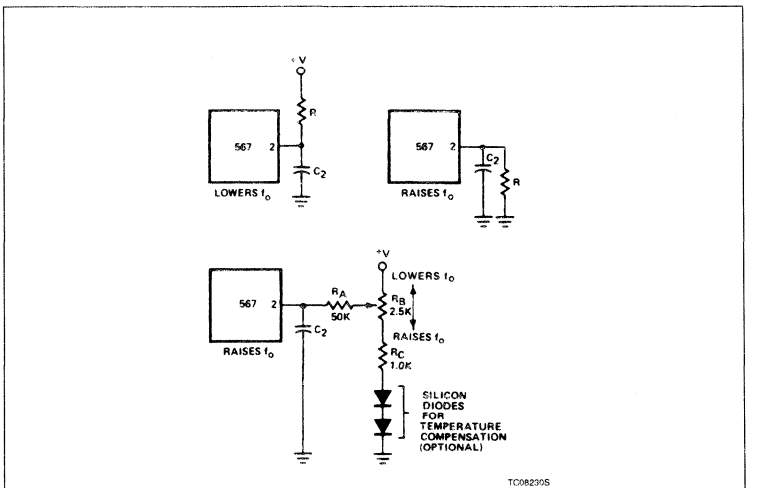


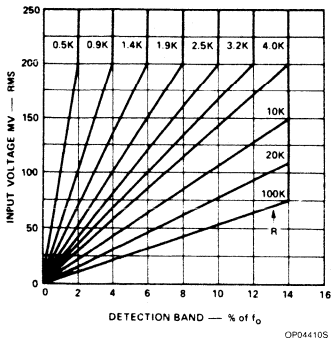
Figure 5

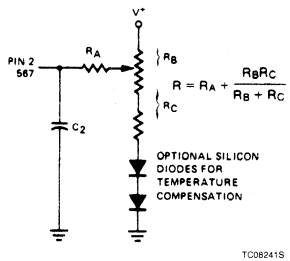
SENSITIVITY ADJUSTMENT

(Figure 3)

When operated as a very narrow-band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and out-band signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the out-band beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.





NOTE:

$$\frac{130}{f_O}\left(\frac{10k+R}{R}\right) < C_2 < \frac{1300}{f_O}\left(\frac{10k+R}{R}\right)$$

Adjust control for symmetry of detection band edges about f_O.

Figure 6

CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (Pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

(Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

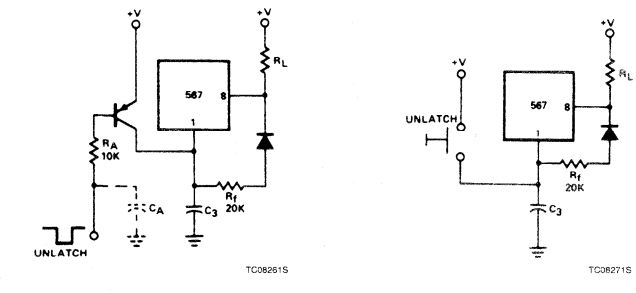
REDUCTION OF C1 VALUE

(Figure 8)

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage-follower between the R_1 C_1 junction and Pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

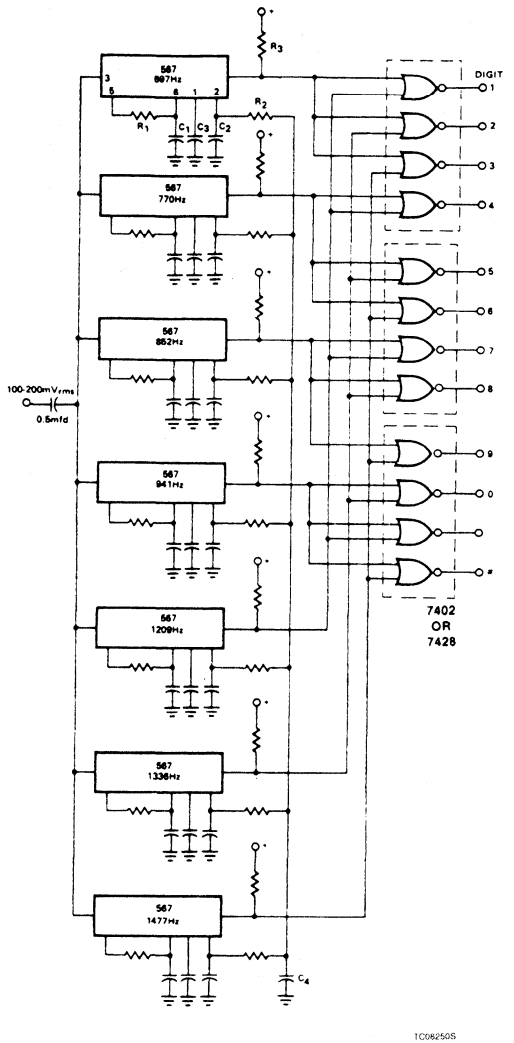
To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating NPN transistors.



NOTE:
C_A prevents latch-up when power supply is turned on.

Figure 7. Output Latching

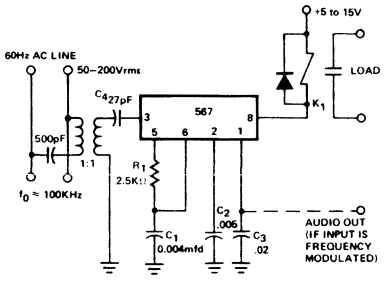
TYPICAL APPLICATIONS



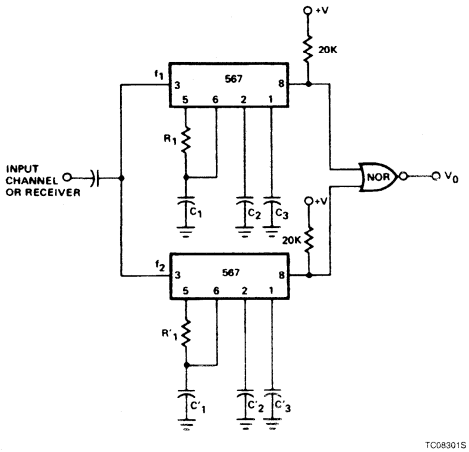
Touch-Tone® Decoder

NOTES:
Component values (Typical)
R_1 = 26.8 to 15kΩ
R_2 = 24.7kΩ
R_3 = 20kΩ
C_1 = 0.10mF
C_2 = 1.0mF 5V
C_3 = 2.2mF 6V
C_4 = 250μF 6V

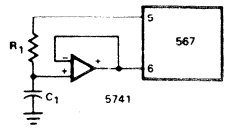
TYPICAL APPLICATIONS (Continued)



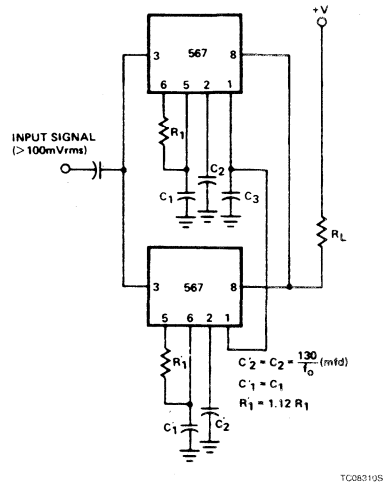
Carrier-Current Remote Control or Intercom



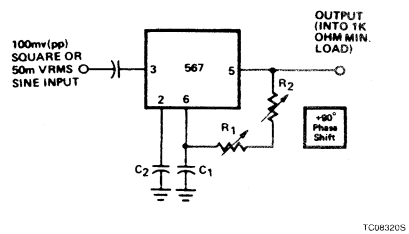
Dual-Tone Decoder



Precision VLF



24% Bandwidth Tone Decoder

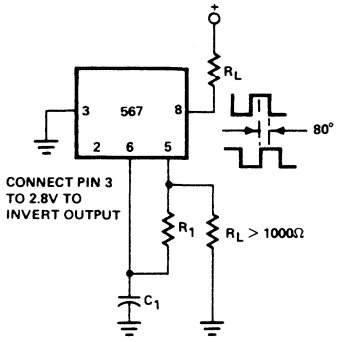


NOTES
$R_2 = R_1/5$
Adjust R_1 so that $\phi = 90°$ with control midway.

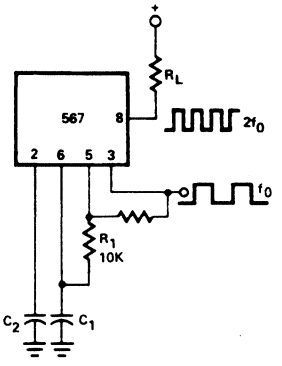
0° to 180° Phase Shifter

NOTES:
1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

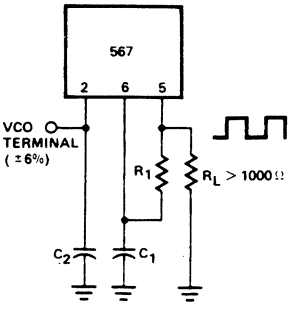
TYPICAL APPLICATIONS (Continued)



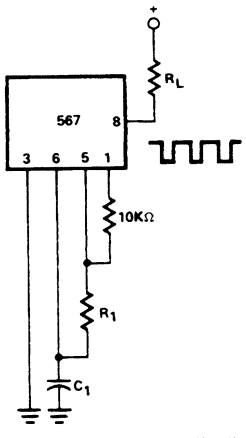
Oscillator With Quadrature Output



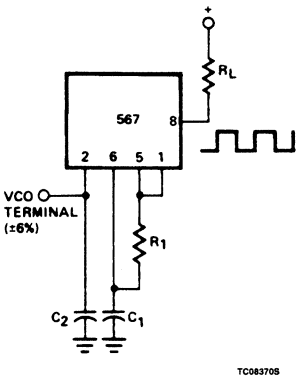
Oscillator With Double Frequency Output



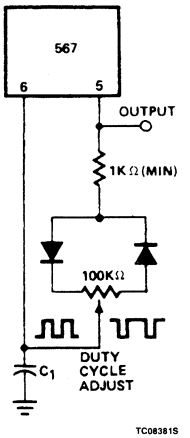
Precision Oscillator With 20ns Switching



Pulse Generator With 25% Duty Cycle



Precision Oscillator to Switch 100mA Loads



Pulse Generator

NE568
150MHz Phase-Locked Loop

Preliminary Specification

DESCRIPTION

The NE568 is a monolithic phase-locked loop (PLL) which operates from 1Hz to frequencies in excess of 150MHz. The integrated circuit consists of a limiting amplifier, a current-controlled oscillator (ICO), a phase detector, a level shift circuit, V/I and I/V converters, an output buffer, and bias circuitry with temperature and frequency compensating characteristics. The design of the NE568 is particularly well-suited for demodulation of FM signals with extremely large deviation in systems which require a highly linear output. In satellite receiver applications with a 70MHz IF, the NE568 will demodulate ±20% deviations with less than 1.0% typical non-linearity. In addition to high linearity, the circuit has a loop filter which can be configured with series or shunt elements to optimize loop dynamic performance. The NE568 is available in 20-pin dual in-line and 20-pin SO (surface-mounted) plastic packages.

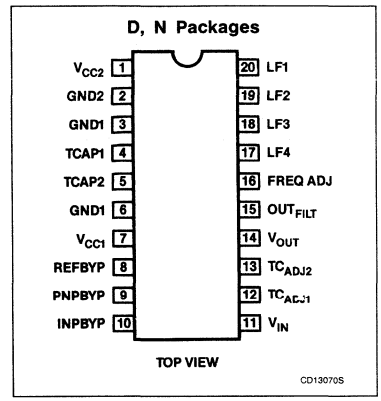
FEATURES

- **Operation to 150MHz**
- **High linearity buffered output**
- **Series or shunt loop filter component capability**
- **Temperature compensated**

APPLICATIONS

- **Satellite receivers**
- **Fiber-optic video links**
- **VHF FSK demodulators**
- **Clock recovery**

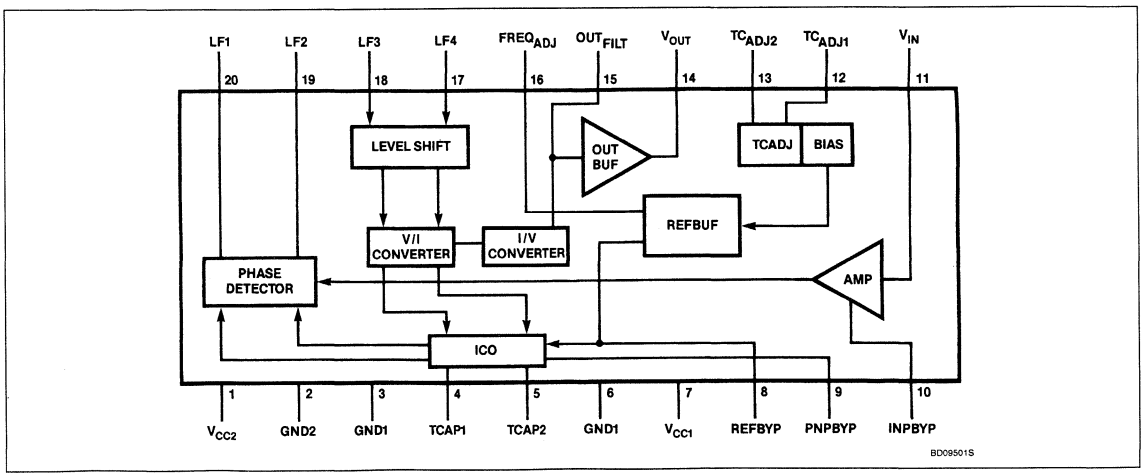
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL Package	0 to +70°C	NE568D
20-Pin Plastic DIP	0 to +70°C	NE568N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	6	V
T_A	Operating free-air ambient temperature range	0 to +70	°C
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{DMAX}	Maximum power dissipation	500	mW

ELECTRICAL CHARACTERISTICS

The electrical characteristics listed below are actual tests (unless otherwise stated) performed on each device with an automatic IC tester prior to shipment. Performance of the device in automated test setup is not necessarily optimum. The NE568 is layout-sensitive. Evaluation of performance for correlation to the data sheet should be done with the circuit and layout of Figures 1 – 3 with the evaluation unit soldered in place. (Do not use a socket!)

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 5V$, $f_O = 70MHz$, Test Circuit Figure 1, $f_{IN} = -20dBm$, $R_4 = 0\Omega$ (ground), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{CC}	Supply current			60	75	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_{OSC}	Maximum oscillator operating frequency[3]		150			MHz
	Input signal level		50 −20[1]		2000 +10	mV_{P-P} dBm
BW	Demodulated bandwidth			$f_O/7$		MHz
	Non-linearity[5]	Dev = ±20%, Input = −20dBm		1.0	4.0	%
	Lock range[2]	Input = −20dBm	±25	±35		% of f_O
	Capture range[2]	Input = −20dBm	±20	±30		% of f_O
	TC of f_O	Figure 1		100		ppm/°C
R_{IN}	Input resistance[4]		1			kΩ
	Output impedance			6		Ω
	Demodulated V_{OUT}	Dev = ±20% of f_O measured at Pin 14	0.40	0.52		V_{P-P}
	AM rejection	V_{IN} = −20dBm (30% AM) referred to ±20% deviation		50		dB
f_O	Distribution[6]	Centered at 70MHz, $R_2 = 1.2k\Omega$, $C_2 = 17pF$, $R_4 = 0\Omega$ ($C_2 + C_{STRAY} = 20pF$)	−15	0	+15	%
f_O	Drift with supply	4.75V to 5.25V		1		%/V

NOTES:

1. Signal level to assure all published parameters. Device will continue to function at lower levels with varying performance.
2. Limits are set symmetrical to f_O. Actual characteristics may have asymmetry beyond the specified limits.
3. Not 100% tested, but guaranteed by design.
4. Input impedance depends on package and layout capacitance. See Figures 4 and 5.
5. Linearity is tested with incremental changes in input frequency and measurement of the DC output voltage at Pin 14 (V_{OUT}). Nonlinearity is then calculated from a straight line over the deviation range specified.
6. Free-running frequency is measured as feedthrough to Pin 14 (V_{OUT}) with no input signal applied.

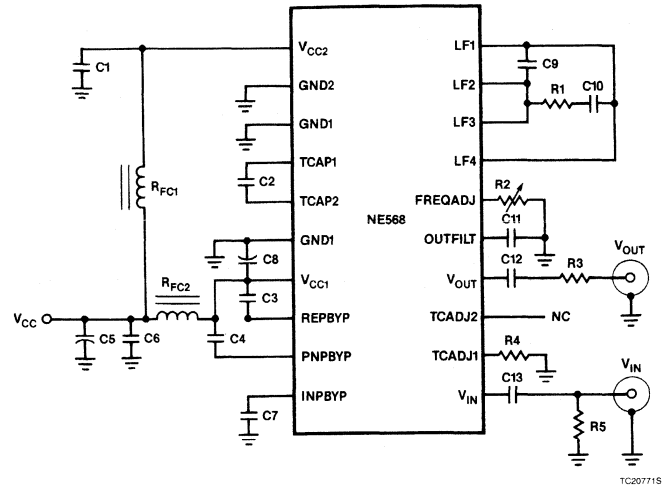


Figure 1. Test and Application Circuit

FUNCTIONAL DESCRIPTION

The NE568 is a high-performance phase-locked loop (PLL). The circuit consists of conventional PLL elements, with special circuitry for linearized demodulated output, and high-frequency performance. The process used has NPN transistors with $f_T > 6GHz$. The high gain and bandwidth of these transistors make careful attention to layout and bypass critical for optimum performance. The performance of the PLL cannot be evaluated independent of the layout. The use of the application layout in this data sheet and surface-mount capacitors are highly recommended as a starting point.

The input to the PLL is through a limiting amplifier with a gain of 200. The input of this amplifier is differential (Pins 10 and 11). For single-ended applications, the input must be coupled through a DC-blocking capacitor with low impedance at the frequency of interest. The single-ended input is normally applied to Pin 11 with Pin 10 AC-bypassed with a low-impedance capacitor. The input impedance is characteristically slightly above 500Ω. Impedance match is not necessary, but loading the signal source should be avoided. When the source is 50 or 75Ω, a DC-blocking capacitor is usually all that is needed.

Input amplification is low enough to assure reasonable response time in the case of large signals, but high enough for good AM rejection. After amplification, the input signal drives one port of a multiplier-cell phase detector. The other port is driven by the current-controlled oscillator (ICO). The output of the phase comparator is a voltage proportional to the phase difference of the input and ICO signals. The error signal is filtered with a low-pass filter to provide a DC-correction voltage, and this voltage is converted to a current which is applied to the ICO, shifting the frequency in the direction which causes the input and ICO to have a 90° phase relationship.

The oscillator is a current-controlled multivibrator. The current control affects the charge/discharge rate of the timing capacitor. It is common for this type of oscillator to be referred to as a voltage-controlled oscillator (VCO), because the output of the phase comparator and the loop filter is a voltage. To control the frequency of an integrated ICO multivibrator, the control signal must be conditioned by a voltage-to-current converter. In the NE568, special circuitry predistorts the control signal to make the change in frequency a linear function over a large control-voltage range.

The free-running frequency of the oscillator depends on the value of the timing capacitor connected between Pins 4 and 5. The value of the timing capacitor depends on internal resistive components and current sources. When $R_2 = 1.2k\Omega$ and $R_4 = 0\Omega$, a very close approximation of the correct capacitor value is:

$$C^* = \frac{0.0014}{f_O} \text{ F}$$

where

$$C^* = C_2 + C_{STRAY}.$$

The temperature-compensation resistor, R_4, affects the actual value of capacitance. This equation is normalized to 70MHz. See Figure 6 for correction factors.

The loop filter determines the dynamic characteristics of the loop. In most PLLs, the phase detector outputs are internally connected to the ICO inputs. The NE568 was designed with filter output to input connections from Pins 20 (ϕ DET) to 17 (ICO), and Pins 19 (ϕ DET) to 18 (ICO) external. This allows the use of both series and shunt loop-filter elements. The loop constants are:

$K_D = 0.127V/Radian$ (Phase Detector Constant)

$$K_O = 4.2 \times 10^9 \frac{\text{Radians}}{\text{V-sec}} \text{ (ICO Constant)}$$

The loop filter determines the general characteristics of the loop. Capacitors C_9, C_{10}, and resistor R_1, control the transient output of the phase detector. Capacitor C_9 suppresses 70MHz feedthrough by interaction with 100Ω load resistors internal to the phase detector.

$$C_9 = \frac{1}{2\pi\ (50)(f_O)} \text{ F}$$

At 70MHz, the calculated value is 45pF. Empirical results with the test and application board were improved when a 56pF capacitor was used.

The natural frequency for the loop filter is set by C_{10} and R_1. If the center frequency of the loop is 70MHz and the full demodulated bandwidth is desired, i.e., $f_{BW} = f_O/7 = 10MHz$, and a value for R_1 is chosen, the value of C_{10} can be calculated.

$$C_{10} = \frac{1}{2\pi\ R_1 f_{BW}} \text{ F}$$

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568D

C_1	100nF	±10%	Ceramic chip	1206
C_2[1]	18pF	±2%	Ceramic chip	0805
C_2[2]	34pF	±2%	Ceramic OR chip	
C_3	100nF	±10%	Ceramic chip	1206
C_4	100nF	±10%	Ceramic chip	1206
C_5	6.8μF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic chip	1206
C_7	100nF	±10%	Ceramic chip	1206
C_8	100nF	±10%	Ceramic chip	1206
C_9	56pF	±2%	Ceramic chip	0805 or 1206
C_{10}	560pF	±2%	Ceramic chip	0805 or 1206
C_{11}	47pF	±2%	Ceramic chip	0805 or 1206
C_{12}	100nF	±10%	Ceramic chip	1206
C_{13}	100nF	±10%	Ceramic chip	1206
R_1	27Ω	±10%	Chip	⅛W
R_2	1.2kΩ		Trim pot	⅛W
R_3[3]	43Ω	±10%	Chip	⅛W
R_4[4]	4.7kΩ	±10%	Chip	⅛W
R_5[3]	· 50Ω	±10%	Chip	⅛W
RFC_1[5]	10μH	±10%	Surface mount	
RFC_2[5]	10μH	±10%	Surface mount	

NOTES:
1. $C_2 + C_{STRAY} = 20pF$.
2. $C_2 + C_{STRAY} = 36pF$ for temperature-compensated configuration with $R_4 = 4.7k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$, $R_3 = 62\Omega$, $R_5 = 75\Omega$ for 75Ω application.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 18pF$.
5. 0Ω chip resistors (jumpers) may be substituted with minor degradation of performance.

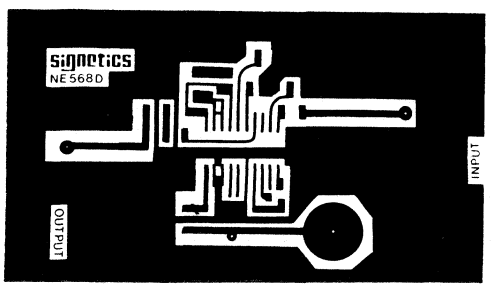
For the test circuit, R_1 was chosen to be 27Ω. The calculated value of C_{10} is 590pF; 560pF was chosen as a production value. (In actual satellite receiver applications, improved video with low carrier/noise has been observed with a wider loop-filter bandwidth.)

A typical application of the NE568 is demodulation of FM signals. In this mode of operation, a second single-pole filter is available at Pin 15 to minimize high frequency feedthrough to the output. The roll-off frequency is set by an internal resistor of 350Ω ±20%, and an external capacitor from Pin 15 to ground. The value of the capacitor is:

$$C11 = \frac{1}{2\pi\ (350) f_{BW}}\ F$$

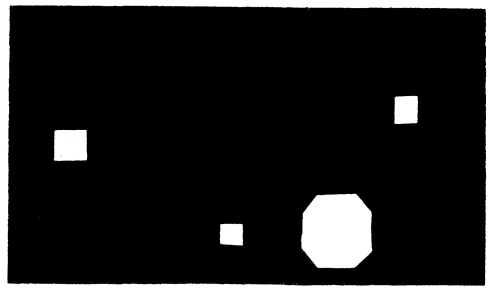
Two final components complete the active part of the circuitry. A resistor from Pin 12 to ground sets the temperature stability of the circuit, and a potentiometer from Pin 16 to ground permits fine tuning of the free-running oscillator frequency. The Pin 16 potentiometer is normally 1.2kΩ. Adjusting this resistance controls current sources which affect the charge and discharge rates of the timing capacitor and, thus, the frequency. The value of the temperature stability resistor is chosen from the graph in Figure 6; the respective timing capacitor needs to be changed.

The final consideration is bypass capacitors for the supply lines. The capacitors should be ceramic chips, preferably surface-mount types. They must be kept very close to the device. The capacitors from Pins 8 and 9 return to V_{CC1} before being bypassed with a separate capacitor to ground. This assures that no differential loops are created which might cause instability. The layouts for the test circuits are recommended.



DF07740S

a. Component Side Top of Board



DF07730S

b. Back of Board

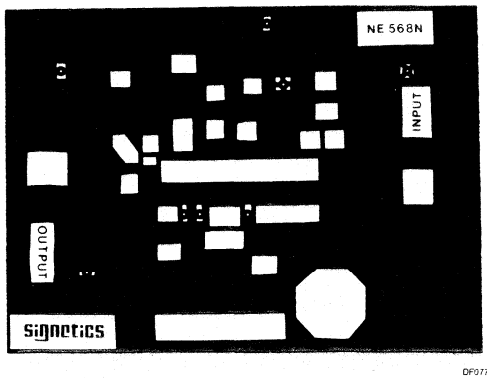
NOTES:
1. Board is laid out for King BNC Connector P/N KC-79-243-M06 or equivalent. Mount on bottom (back) of board. Add stand-off in each corner.
2. Back and top side ground must be connected at 8 point minimum.

Figure 2

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568N

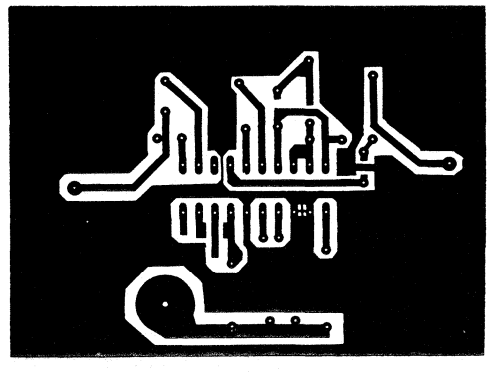
C_1	100nF	±10%	Ceramic chip	50V
C_2[1]	17pF	±2%	Ceramic OR chip	50V
C_2[2]	34pF	±2%	Ceramic chip	0805
C_3	100nF	±10%	Ceramic chip	50V
C_4	100nF	±10%	Ceramic chip	50V
C_5	6.8μF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic OR chip	50V
C_7	100nF	±10%	Ceramic chip	50V
C_8	100nF	±10%	Ceramic chip	50V
C_9	56pF	±2%	Ceramic chip	50V
C_{10}	560pF	±2%	Ceramic chip	50V
C_{11}	47pF	±2%	Ceramic OR chip	50V
C_{12}	100nF	±10%	Ceramic OR chip	50V
C_{13}	100nF	±10%	Ceramic OR chip	50V
R_1	27Ω	±10%	Carbon	¼W
R_2	1.2kΩ		Trim pot	
R_3[3]	43Ω	±10%	Carbon	¼W
R_4[4]	4.7kΩ	±10%	Carbon	¼W
R_5[3]	50Ω	±10%	Carbon	¼W
RFC_1	10μH	±10%		
RFC_2	10μH	±10%		

NOTES:
1. $C_2 + C_{STRAY} = 20pF$ for test configuration with $R_4 = 0\Omega$.
2. $C_2 = 34pF$ for temperature-compensated configuration with $R_4 = 4.7k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$; $R_3 = 75\Omega$ for 75Ω applications.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 17pF$.



DF97750S

a. Component Side for Leaded Components



DF07760S

b. Solder Side of Board and Chip Capacitors

NOTES:
1. Board is laid out for King BNC Connector P/N KC-79-243-M06 or equivalent mounted on the component side of the board.
2. Component side and solder side ground planes must be connected at 8 points minimum.

Figure 3

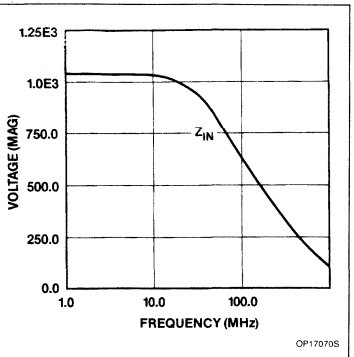


Figure 4. NE568 Input Impedance with CP = 0.5pF 20-Pin SO Package

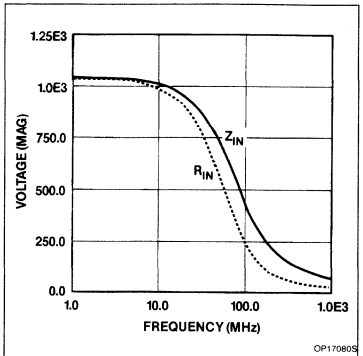


Figure 5. NE568 Input Impedance with CP = 1.49pF 20-Pin Dual In-Line Plastic Package

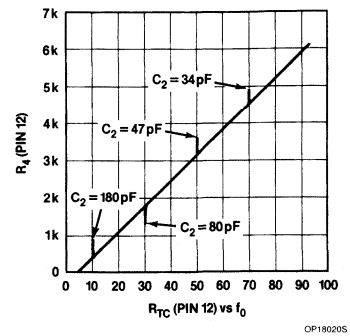


Figure 6

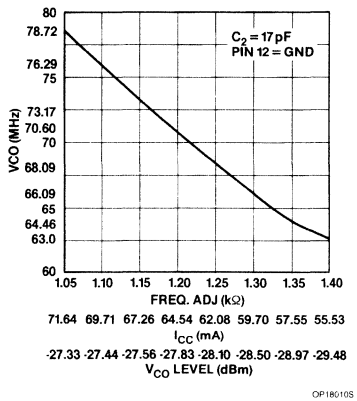


Figure 7. Typical VCO Frequency vs R_2 Adjustment

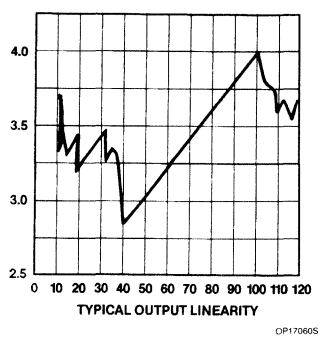


Figure 8. Typical Output Linearity

NE5900
Call Progress Decoder

Product Specification

DESCRIPTION

The NE5900 call progress decoder (CPD) is a low cost, low power CMOS integrated circuit designed to interface with a microprocessor-controlled smart telephone capable of making preprogrammed telephone calls. The call progress decoder provides information to permit microprocessor decisions whether to initiate, continue, or terminate calls. A tri-state, 3-bit output code indicates the presence of dial tone, audible ringback, busy signal, or reorder tones.

A front-end bandpass filter is accomplished with switched capacitors. The bandshaped signal is detected and the cadence is measured prior to output decoding. In addition to the three data bits, a buffered bandpass output and envelope output are available. All logic inputs and outputs can interface with LSTTL, CMOS, and NMOS.

Circuit features include low power consumption and easy application. Few and inexpensive external components are required. A typical application requires a 3.58MHz crystal or clock, 470kΩ resistor, and two bypass capacitors. The NE5900 is effective where traditional call progress tones, PBX tones, and precision call progress tones must be correctly interpreted with a single circuit.

FEATURES

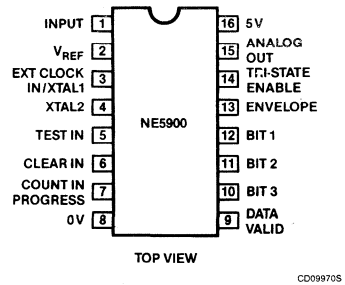
- **Fully decoded tri-state call progress status output**
- **Works with traditional, precision, or PBX call progress tones**
- **Low power consumption**
- **Low cost 3.58MHz crystal or clock**
- **No calibration or adjustment**
- **Interfaces with LSTTL, CMOS, NMOS**
- **Easy application**

APPLICATIONS

- **Modems**
- **PBXs**
- **Security equipment**
- **Auto dialers**
- **Answering machines**
- **Remote diagnostics**
- **Pay telephones**

PIN CONFIGURATION

D[1] and N Packages

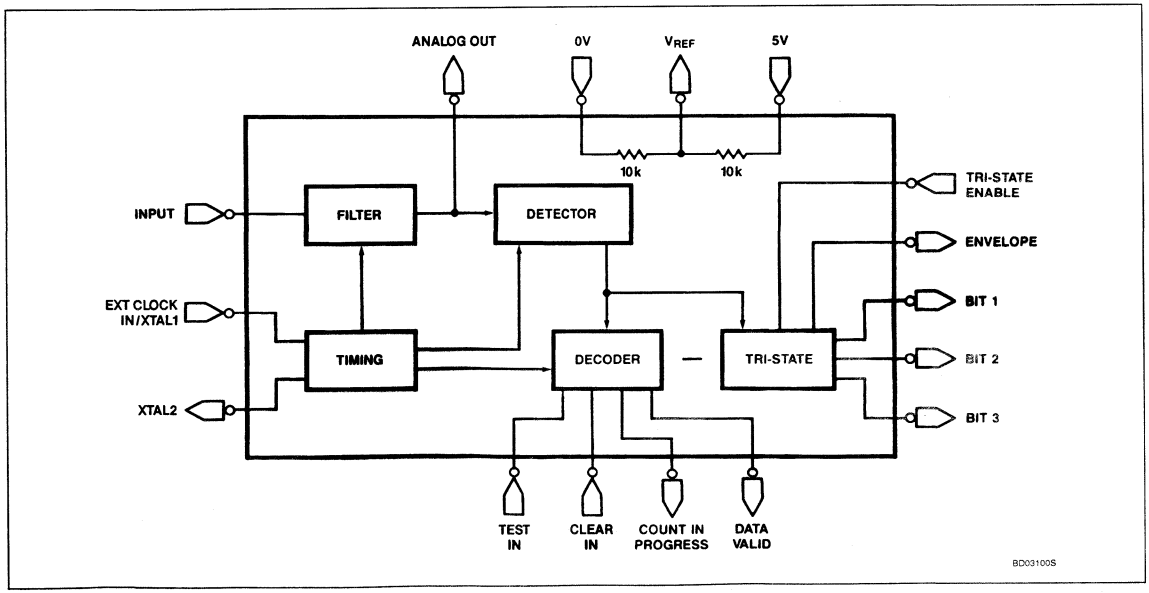


TOP VIEW

CD09970S

NOTE:
1. SOL — Released in large SO package only.

BLOCK DIAGRAM CPD



ORDERING INFORMATION

DESCRIPTION	AMBIENT TEMPERATURE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE5900D
16-Pin Plastic DIP	0 to +70°C	NE5900N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Power supply voltage	9	V
V_{IN}	Logic control input voltages	−0.3 to +16	V
V_{IN}	All other input voltages[1]	−0.3 to V_{CC} +0.3	V
V_{OUT}	Output voltages	−0.3 to V_{CC} +0.3	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating temperature range	0 to +70	°C
T_{SOLD}	Lead soldering temperature (10s)	+300	°C
T_J	Junction temperature	+150	°C

NOTE:
1. Includes Pin 3 — Ext Clock In

DC ELECTRICAL CHARACTERISTICS Unless otherwise stated, V_{DD} = +5.0V; Pin 3 f_{OSC} = 3.58MHz; Ambient Temperature = 0 to +70°C. Pin 5 = 0V, Pin 14 = V_{DD}.

SYMBOL	PARAMETER	TEST CONDITONS	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Power supply voltage	Pin 16 Pin 14 = V_{DD} Pins 5, 6 = 0V	4.5	5.0	5.5	V
	Quiescent current	As above with no output loads.		2.0	4.0	mA
	Input threshold	Pin 1 level, frequency = 460Hz, V_{DC} = V_{REF} Output Pin 13 = V_{DD}		−39	−35	dB[1]
	Signal rejection	Pin 1 level, 300Hz frequency, V_{DC}=V_{REF} Output Pin 13 = 0V			−50	dB[1]
	Low frequency[2] rejection	Pin 1 frequency, 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V			180	Hz
	High frequency[2] rejection	Pin 1 frequency 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V	800			Hz
V_{IH}	Logic 1 input voltage	Pins 6, 14	2.0		15	V
V_{IL}	Logic 0 input voltage	Pins 6, 14	0		0.8	V
I_{HL}	Logic 1 input current	Pins 3, 6, 14 = V_{DD}	−1.0		1.0	μA
I_{IL}	Logic 0 input current	Pins 3, 6, 14 = 0V	−1.0		1.0	μA
V_{IH}	Logic 1 input voltage	Pin 3 External Clock In/XTAL	V_{DD} − 1		V_{DD}	V
V_{IL}	Logic 0 input voltage	Pin 3 External Clock In/XTAL	0		1.0	V
V_{OL}	Logic 0 output voltage	I_{SINK} = 1.6mA Pins 7, 9, 10, 11, 12, 13	0		0.4	V
V_{OH}	Logic 1 output voltage	I_{SOURCE} = 0.5mA Pins 7, 9, 10, 11, 12, 13	V_{DD} − 0.4		V_{DD}	V
I_{OZ}	Tri-state leakage	V_{OUT} = V_{DD} or 0V Pins 10, 11, 12, 13 Pin 14 = 0V	−3.0		3.0	μA
	Filter output gain	Input Pin 1, 460Hz − 20dB, V_{DC} = V_{REF} Output Pin 15, R_{LOAD} = 1MΩ	6.5	8.5	10.5	dB
	Filter frequency response	As above from 300Hz to 630Hz, referenced to 460Hz	−1.0		1.0	dBmo
	Input impedance[2]	Pin 1, frequency = 460Hz	1			MΩ
V_{REF}	Reference voltage	Pin 2, V_{DD} = 5V	2.4	2.5	2.6	V
R_{REF}	Reference resistance	Pin 2		5		Ω
	Envelope response time	Time from removal or application of 460Hz − 20dB (V_{DC} = V_{REF} on Pin 1) to response of Pin 13		38		ms

NOTES:
1. 0dB = 0.775V_{RMS}.
2. By design; not tested.

The NE5900 uses the signal in the call progress tone passband and the cadence or interrupt rate of the signal to determine which call progress tone is present.

Figure 1 shows a detailed block diagram of the NE5900.

The signal input from the phone line is coupled through a 470kΩ resistor which, together with two internal capacitors and an internal resistor, form an anti-aliasing filter. This passive low pass filter strongly rejects AM radio interference. Insertion loss is typically 1.5dB at 460Hz. The 470kΩ resistor also provides protection from line transients. The input (Pin 1) DC voltage can be derived from V_{REF} (Pin 2) or allowed to self-bias through a series coupling capacitor (10nF minimum).

Following this is a switched capacitor bandpass filter which accepts call progress tones and inhibits tones not in the call progress band of 300Hz to 630Hz. The bandpass limits are determined by the input clock frequency of 3.58MHz. An on-board inverter between Pins 3 and 4 can be used either as a crystal oscillator or as a buffer for an external 3.58MHz clock signal. The switched capacitor filters provide typical rejection of greater than 40dB for frequencies below 120Hz and above 1.6kHz.

The decoder responds to signals between 300Hz and 630Hz with a threshold of −39dB typical (0dB = $0.775V_{RMS}$). The decoder will not respond to any signals below −50dB or to tones up to 0dB which are below 180Hz or above 800Hz. Dropouts of 20ms or bursts of only 20ms duration are ignored. A gap of 40ms or a valid tone of 40ms is detected.

The buffered output of the switched capacitor filter is available at the analog output, Pin 15. A logic output representing the detected envelope of this signal is available at the envelope output, Pin 13.

At the start of an in-band tone (envelope output goes high), a 2.3-second interval is timed out. Transitions of the envelope during this interval are counted to determine the signal present. At 2.3 seconds, the three bits of data representing this decision are stored in the latch and appear at the outputs. A data valid signal goes high at this time, signaling that the data bits, Pins 10 – 12, can be read.

The output code is as follows:

	PIN 12	PIN 11	PIN 10
DIAL TONE	0	0	0
RINGING SIGNAL	1	0	0
BUSY SIGNAL	0	1	0
REORDER TONE	0	0	1
OVERFLOW	1	1	1

The overflow condition occurs in the event that too many transitions occur during the 2.3-second interval. This can result from noise, voice, or other line disturbances not normally present during the post-dialing interval. Note that the end of dial tone is interpreted as a valid ringing signal.

The clear input resets all internal registers and the output latch, and is to be set low after the completion of dialing. The clear input should be pulsed high for proper operation. Recommended pulse width is between 0.2μs and 20ms. If clear is held high when envelope is high, a false output pulse (Pin 13) can result when clear is returned low.

For applications where dialing is done by a person rather than by a microprocessor, an uncertainty exists about the number of digits to be dialed (local vs long distance). In such situations it is possible to clear the NE5900 by application of the DTMF signal or dial pulses to the clear pin (Pin 6). When dialing is complete, the device is cleared and ready to respond to the next call progress unit.

Enable is held at 5V to enable Pins 10, 11, 12, and 13. When enable is brought low, data valid is also set low. Enable must remain high while the data is being read. The test pin is for production test only and must be kept low in all user applications.

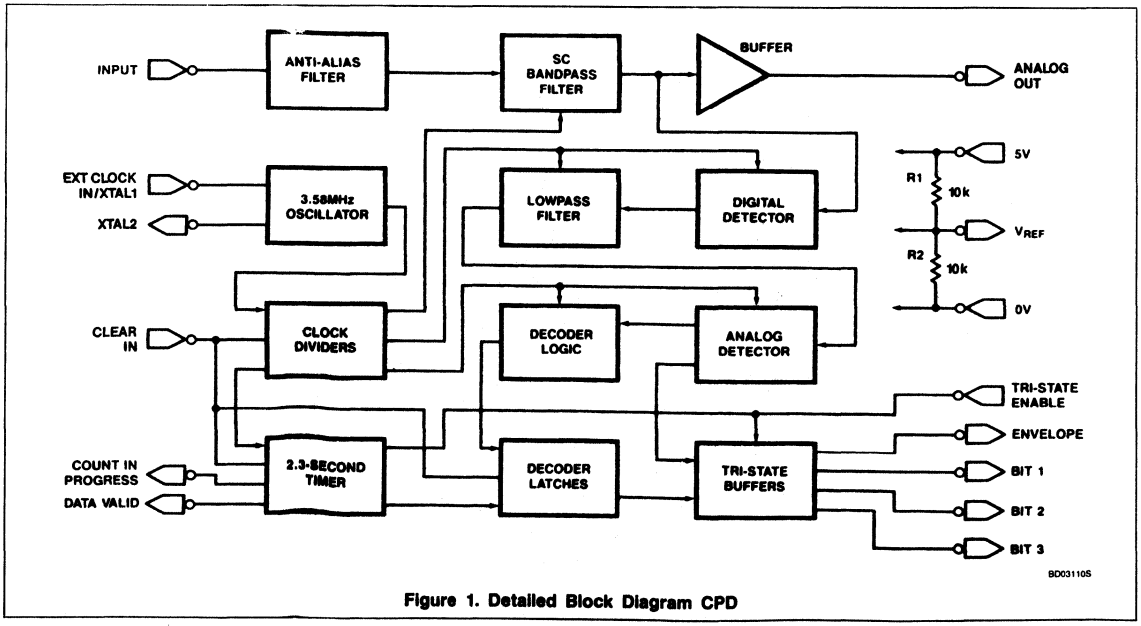


Figure 1. Detailed Block Diagram CPD

Call Progress Decoder

NE5900

Figure 2 shows a typical application of the call progress decoder.

In this application only one external component is needed and no microprocessor activity other than clear is required.

Figure 3 shows the recommended direct interface to the telephone line. Bus connection is possible by utilizing tri-state, and internal timing is accomplished with a 3.58MHz crystal.

The designer can utilize the input signal, clock, bus, or microprocessor interface which best serves the application. Figure 4 gives a typical timing diagram for the application of Figures 2 and 3.

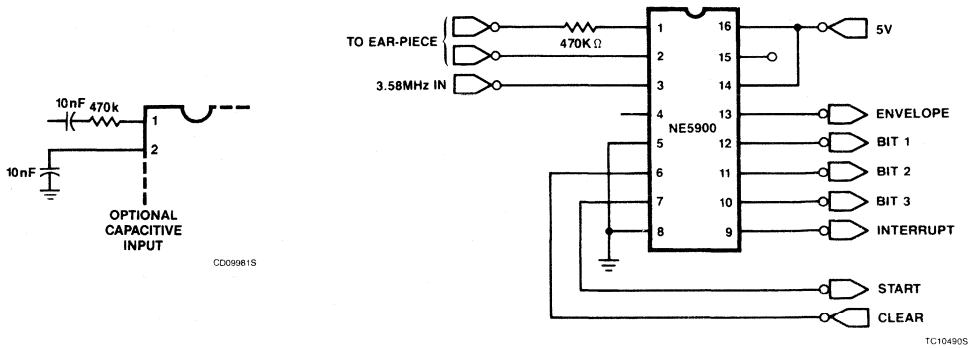


Figure 2. Typical Application

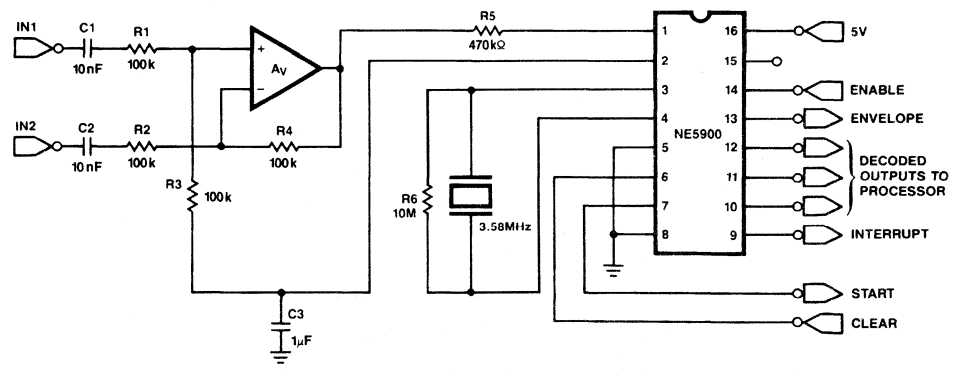


Figure 3. Typical Two-Wire Application

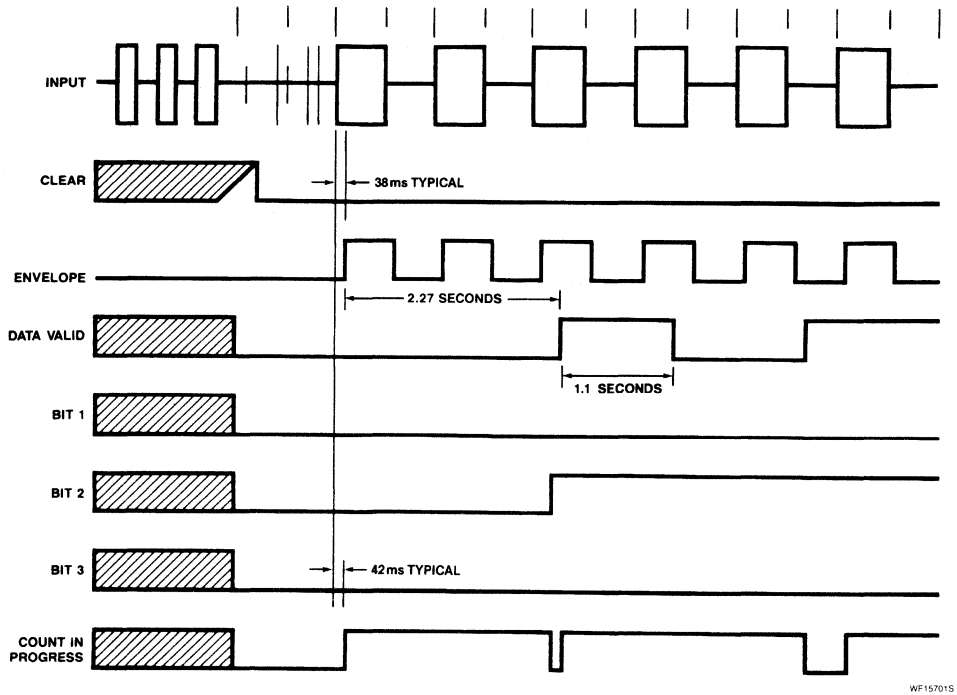
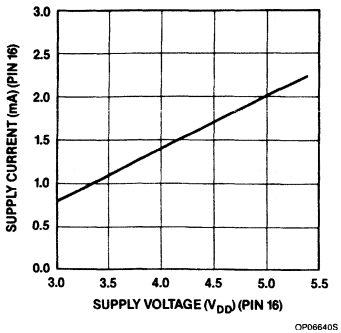

INPUT
CLEAR
38ms TYPICAL
ENVELOPE
2.27 SECONDS
DATA VALID
1.1 SECONDS
BIT 1
BIT 2
BIT 3
42ms TYPICAL
COUNT IN PROGRESS
WF15701S

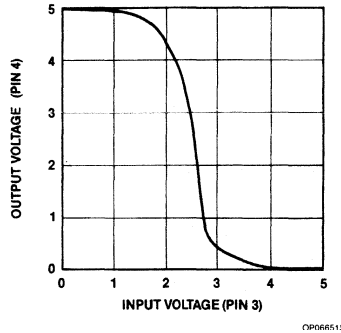
Figure 4

TYPICAL PERFORMANCE CHARACTERISTICS

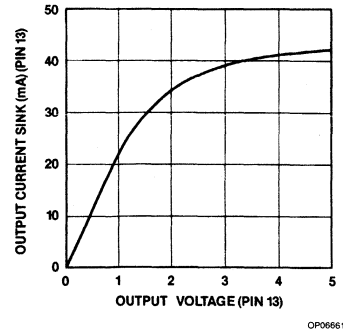
Power Supply Current vs V_{DD}



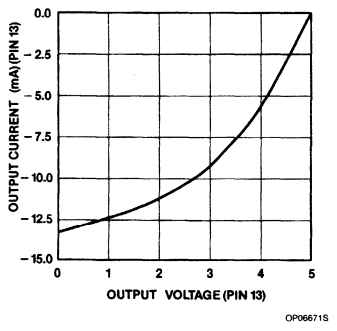
Voltage Transfer Curve



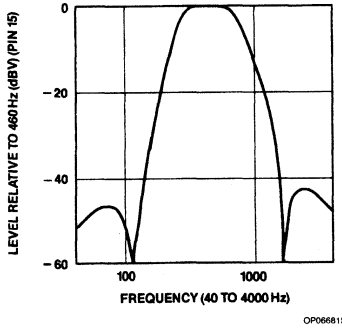
Output Voltage Current Curve Digital Output Low



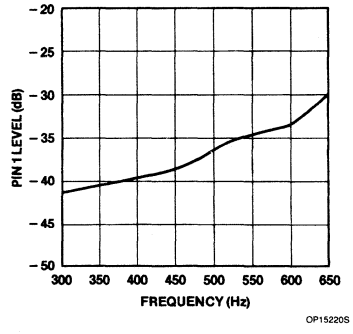
Output Voltage Current Curve Digital Output High



Filter Frequency Response



Typical Threshold



μA758
FM Stereo Multiplex Decoder, Phase-Locked Loop

Product Specification

DESCRIPTION

The μA758 is a monolithic phase-locked loop FM stereo multiplex decoder. The device decodes an FM stereo multiplex signal into right and left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. The device includes automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a large voltage range and requires a minimum number of external components. A simple setting of an external potentiometer adjusts the oscillator frequency. No coils are required.

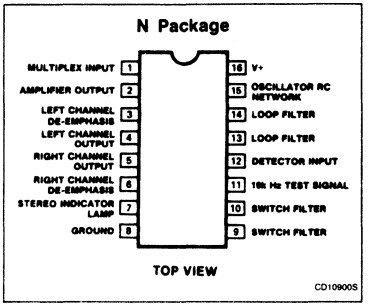
FEATURES

- **45dB channel separation**
- **Automatic stereo/mono switching**
- **70dB SCA rejection**
- **10V to 16V supply range**
- **High impedance input — low impedance output**

APPLICATIONS

- **Stereo decoder for radios**

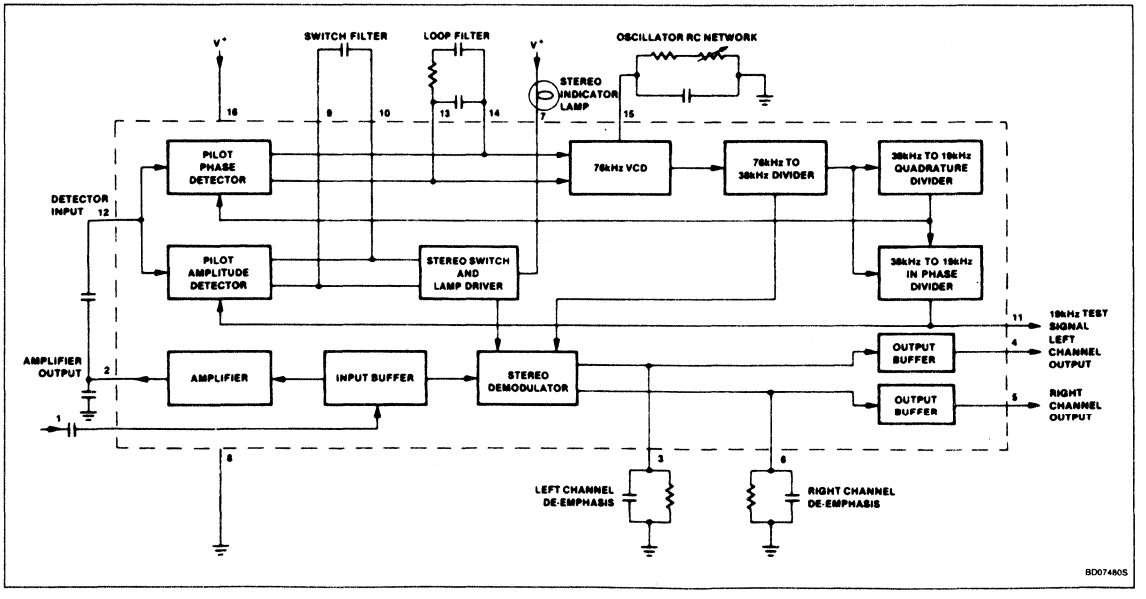
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	−40°C to +85°C	μA758N

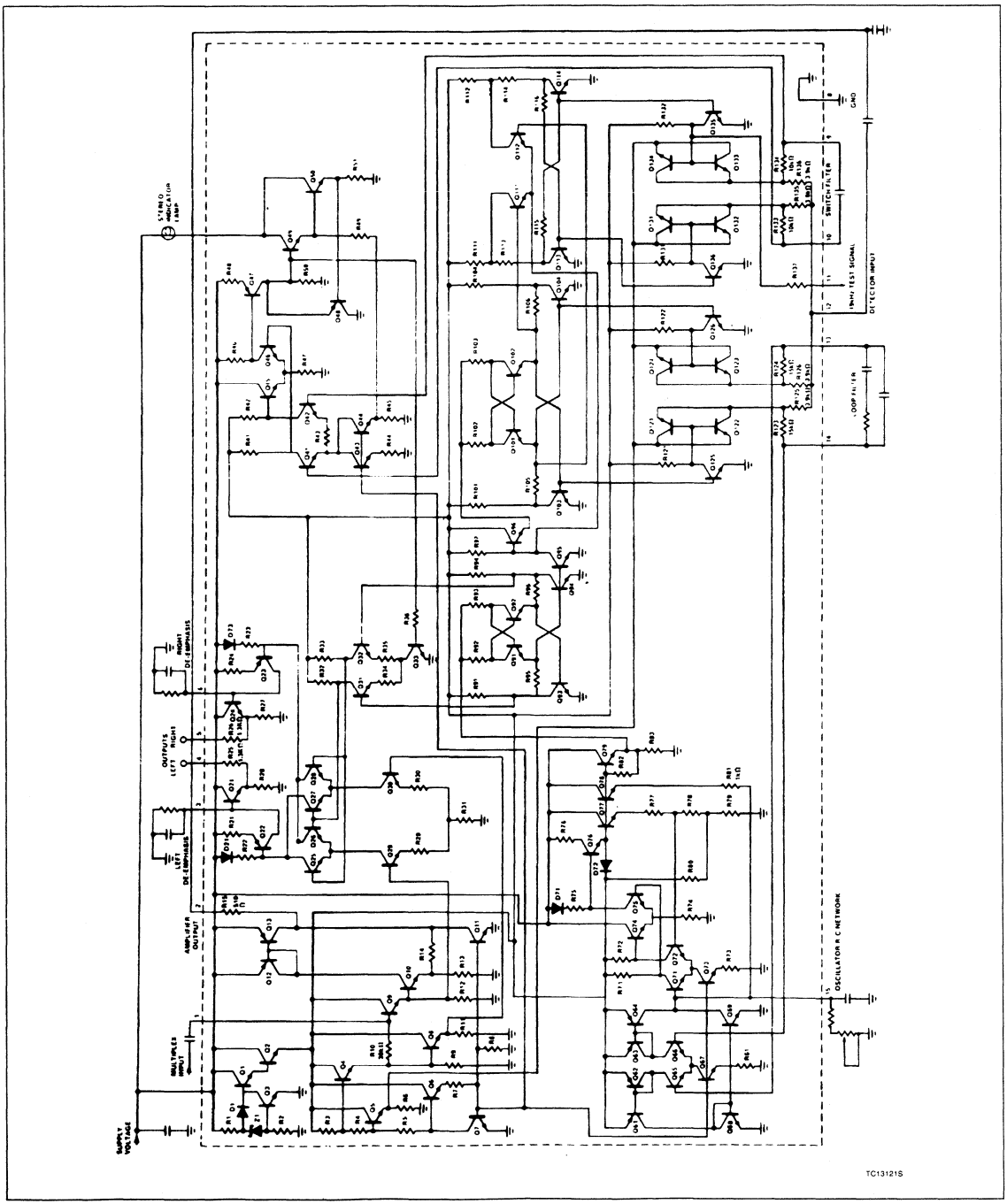
BLOCK DIAGRAM



FM Stereo Multiplex Decoder, Phase-Locked Loop

μA758

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+18	V
V_{CC}	Supply voltage ($\leq$ 15 seconds)	+22	V
	Voltage at lamp driver terminal (Lamp OFF)	+22	V
P_D	Internal power dissipation	730	mW
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +125	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V+ = +12V, 19kHz pilot level = 30mV$_{RMS}$, multiplex signal (L = R, pilot OFF) = 300V$_{RMS}$, modulation frequency = 400Hz or 1Hz, Test Circuit 1, unless otherwise specified .

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I_{CC} I_L	Supply current Maximum available lamp current	Lamp OFF	 75	31 150	38	mA mA
V_7	Voltage at lamp driver terminal	Lamp = 50mA		1.3	1.8	V
R_{IN}	Input resistance		20	35		kΩ
R_{OUT}	Output resistance		0.9	1.3	2.0	kΩ

AC ELECTRICAL CHARACTERISTICS

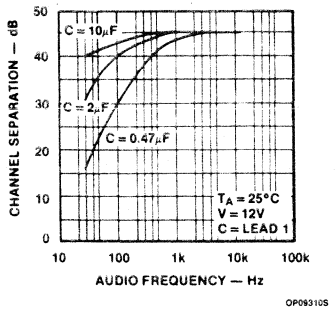
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
$\Delta(V_4\&V_5)$	DC voltage shift at either output terminal	Stereo to mono operation		30	150	mV
PSRR	Power supply ripple rejection	200Hz, 200mV$_{RMS}$	35			dB
SEP	Channel separation	100Hz 400Hz 10kHz	30	40 45 45		dB dB dB
BAL	Channel balance			0.3	1.5	dB
A_V	Voltage gain	1kHz	0.5	0.9	1.4	V/V
	Pilot input level	Lamp turn-on Lamp turn-off	 2.0	18 7.0	25	mV$_{RMS}$ mV$_{RMS}$
	Pilot input level hysteresis	Lamp turn-off to turn-on	3.0	7.0		dB
THD	Capture range Total harmonic distortion	Multiplex level = 600mV$_{RMS}$ pilot OFF	2.0	4.0 0.4	6.0 1.0	% %
	19kHz rejection 38kHz rejection SCA rejection[1]		25 25	35 45 70		dB dB dB
VCO	Tuning resistance[2]		21.0	23.3	25.5	kΩ
VCO	Frequency drift	0°C $\leq T_A \leq$ 25°C 25°C $\leq T_A \leq$ 70°C		+0.1 −0.4	±2 ±2	% %

NOTES:
1. Measured with a stereo composite consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
2. Total resistance from Pin 15 to ground, in Test Circuit, required to set reference frequency at Pin 11 to 19kHz ± 10Hz.

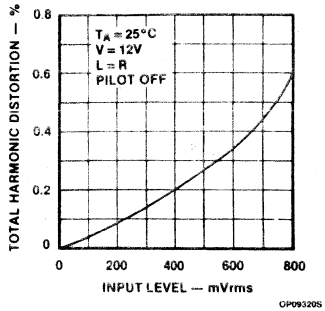
FM Stereo Multiplex Decoder, Phase-Locked Loop μA758

TYPICAL PERFORMANCE CHARACTERISTICS

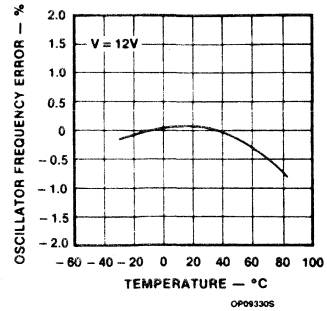
Channel Separation vs Audio Frequency



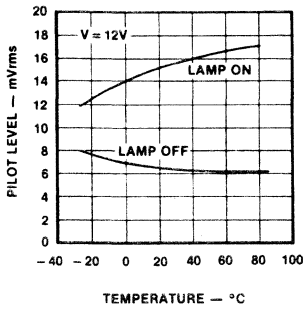
Harmonic Distortion vs Input Level



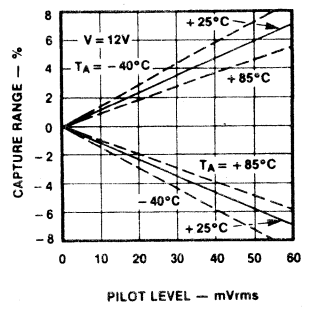
Oscillator Free-Running Frequency Error vs Ambient Temperature



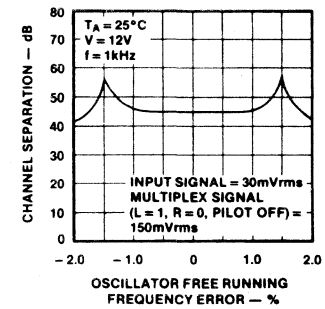
Lamp Turn-On & Turn-Off Sensitivity vs Ambient Temperature



Capture Ranges vs Pilot Level

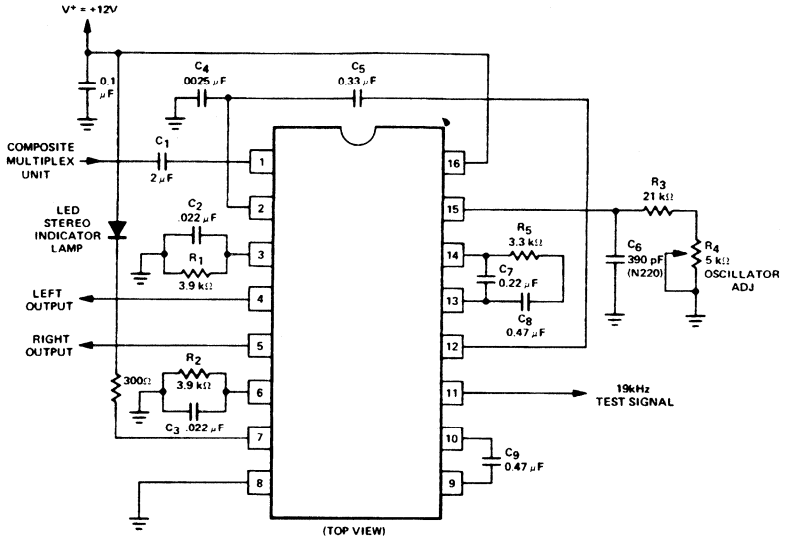


Channel Separation vs Oscillator Free-Running Frequency Error



FM Stereo Multiplex Decoder, Phase-Locked Loop — μA758

TEST CIRCUIT AND TYPICAL APPLICATION



NOTE:
Tolerance on resistors is ±5% and tolerance on capacitors is ±20%, unless otherwise specified. C_1 tolerance = +100%; −20%, C_6 tolerance = ±1% in test circuit and ±5% in typical applications. R_3 tolerance = ±1%, R_4 tolerance = ±10%, R_1 and R_2 tolerance = ±1% in Test Circuit and ±5% in Typical Application.

AN179
Circuit Description of the NE564

Application Note

CIRCUIT DESCRIPTION Of The NE564

The 564 contains the functional blocks shown in Figure 1. In addition to the normal PLL functions of phase comparator, VCO, amplifier and low-pass filter, the 564 has internal circuitry for an input signal limiter, a DC retriever, and a Schmitt trigger. The complete circuit for the 564 is shown in Figure 1.

Limiter

The input limiter functions to produce a near constant amplitude output that serves as the input for the phase comparator. Eliminating amplitude variations in the FM input signal improves the AM rejection of the PLL. Additional features of the 564's limiter are that it is capable of accepting TTL signals, operates at high frequencies up to 50MHz, and remains functional with variable supply voltages between 5 and 12V.*

Signal limiting is accomplished in the 564 with a differential amplifier whose output voltage is clipped by diodes D_1 and D_2 (see Figure 2). Schottky diodes are used because their limiting occurs between 0.3 to 0.4V instead of the 0.6 to 0.7V for regular IC diodes. This lower limiting level is helpful in biasing, especially for 5V operation. When limiting, the DC voltage across R_2 R_3 remains at the Schottky diode voltage. Good high-frequency performance for Q_2 and Q_3 is achieved with current levels in the low mA range. Current-source biasing is established via the current mirror of D_5 and Q_4 (See Figure 1).

Base biasing for Q_3 is of concern because of the nature of the input signal which can be either a TTL digital signal of 0 to 5V amplitude or a low-level, AC coupled analog signal. Compatibility for either type is achieved by modifying the limiter of Figure 2 with the addition of the vertical Schottky PNP transistors Q_1 and Q_5 as shown in Figure 3. The input signal voltage appears as a collector-base voltage for Q_1, which presents no problems for either high TTL level inputs or low-level analog inputs. Q_5 is in turn diode-biased by D_3 and D_4 (see Figure 1) which places the base voltages of Q_1 and Q_5 at approximately 1.0V. This same biasing network establishes a 1.3V bias at the base of Q_{13} for biasing the phase comparator section. A differential output signal from the input limiter is applied to one input of the phase comparator (Q_9 through Q_{12}) after buffering the level shifting through the $Q_7 - Q_8$ emitter-followers.

*When operating above $5V_{DC}$, a limiting resistor must be used from V_{CC} to Pin 10 of the 564.

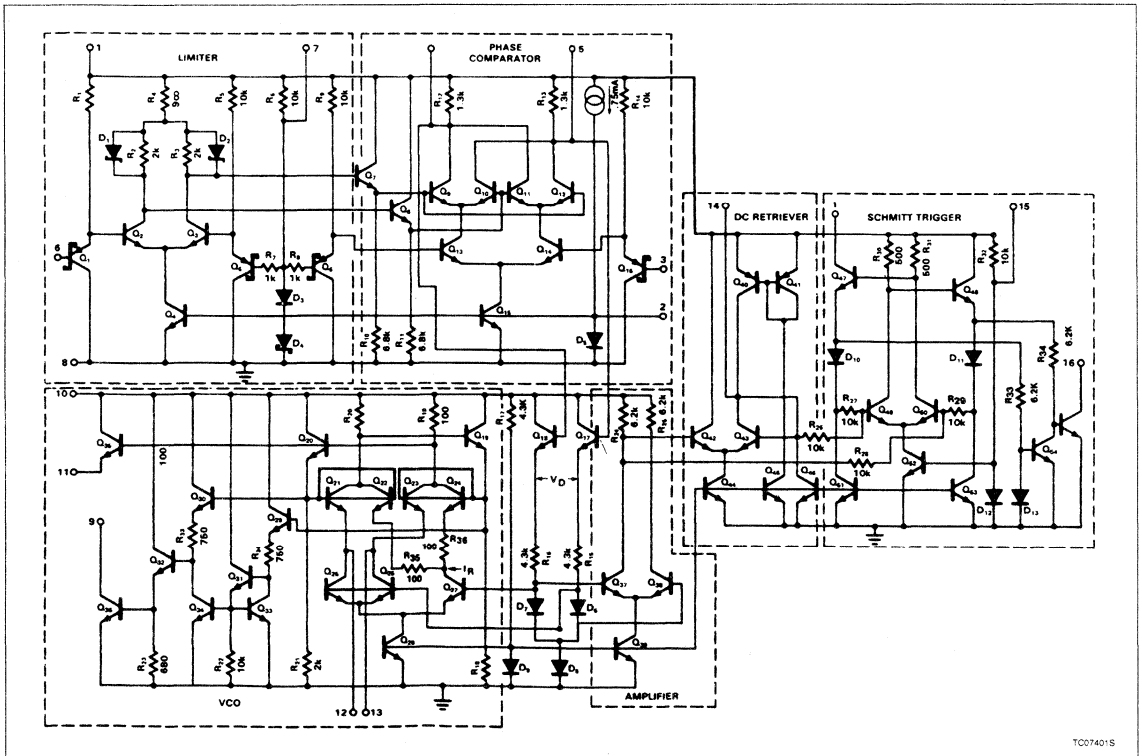


Figure 1. Schematic Diagram of NE564

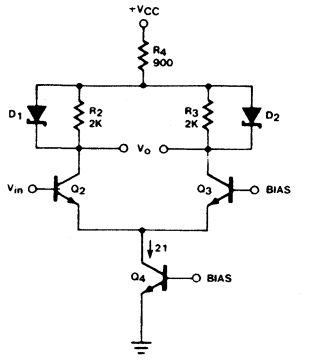


Figure 2. Basic Limiter Stage

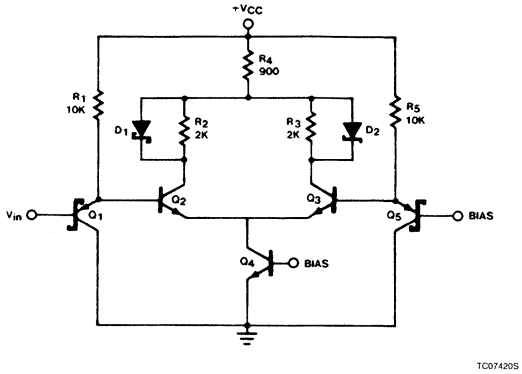


Figure 3. Limiter Stage With Input Buffering

Phase Comparator

The phase comparator section of the 564 is shown in Figure 4. It is basically the conventional, double-balanced mixer commonly used in PLL circuits, with a few exceptions. The transconductance, g_M, for the $Q_{13} - Q_{14}$ differential amplifier is directly proportional to the mirror current in Q_{15}. Thus, by externally sinking or sourcing current at Pin 2, g_M can be changed to alter the phase comparator's conversion gain, K_d. The nominal current injected into this node by the internal current source is 0.75mA for 5V operation. If the current is externally removed by gating, the phase comparator can be disabled and the VCO will operate at its free-running frequency.

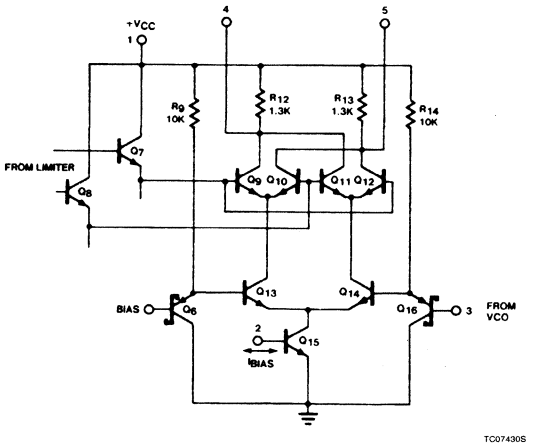


Figure 4. Phase Comparator Section

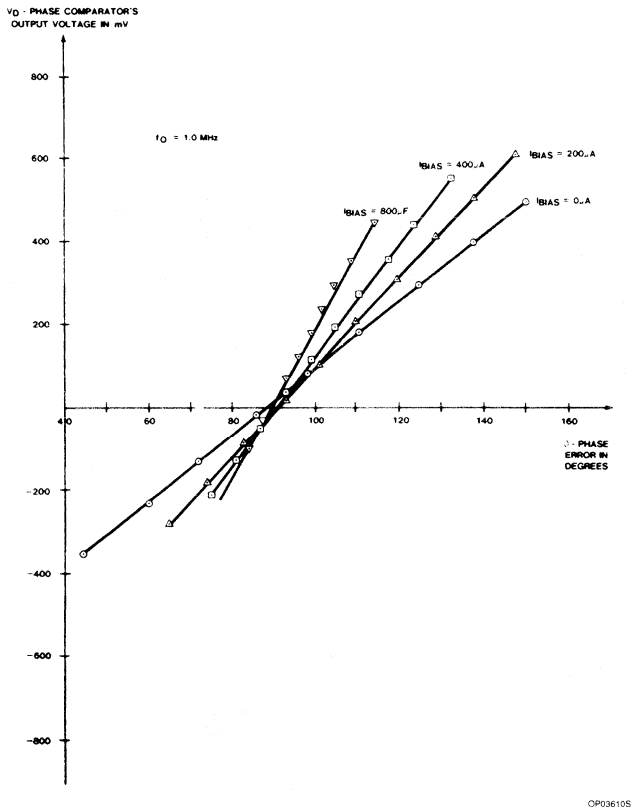


Figure 5. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current

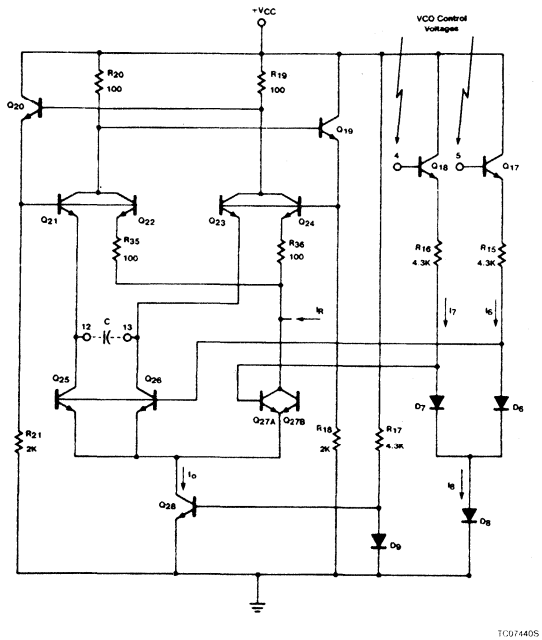


Figure 6. VCO Section of NE564

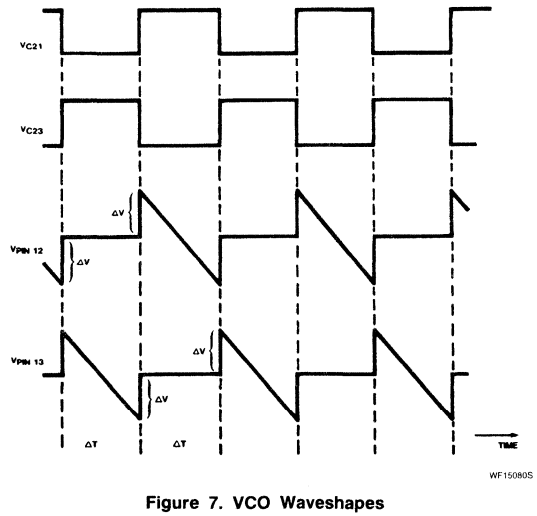


Figure 7. VCO Waveshapes

The variation of K_d with bias current at Pin 2 is shown in the experimental results of Figure 5. Note that the inherent 90° phase error in the loop produces an approximate zero-phase comparator output voltage. For any particular bias current, the slope of the line is the K_d conversion gain for the phase comparator. Numerically the data of Figure 5 can be expressed as

$$K_d \simeq 0.46\left(\frac{\text{volts}}{\text{rad}}\right) + 7.3 \times 10^{-4}\left(\frac{\text{volts}}{\text{rad} \times \mu A}\right) \times I_{BIAS}\ (\mu A) \quad (1)$$

Equation 1 is valid for bias current less than 800μA where saturation occurs within the phase comparator.

The current level established in Q_{15} of Figure 3 determines all other quiescent currents in the phase comparator (Q_9 through Q_{14}). Currents through R_{12} and R_{13} set the common-mode output voltage from the phase comparator (Pins 4 and 5). Since this common-mode voltage is applied to the VCO to establish its quiescent currents, the VCO conversion gain (K_o) also depends upon the bias current at Pin 2.

VCO

The VCO is of the basic emitter-coupled astable type with several modifications included to achieve the high frequency, TTL compatible operation while maintaining low frequency drift with temperature changes. The basic oscillator in Figure 6 consists of Q_{19}, Q_{20}, Q_{21}, and Q_{23} with current sinks of Q_{25} and Q_{26}. The master current sink of Q_{28} keeps the total current constant by altering the ratio of currents in $Q_{25} - Q_{26}$ and the dummy current sink of Q_{27}.

The input drive voltage for the VCO is made up of common-mode and difference-mode components from the phase comparator. After buffering the level shifting through $Q_{17} - Q_{18}$ and $R_{15} - R_{16}$, the VCO control voltage is applied differentially to the base of Q_{27} and to the common bases of Q_{25} and Q_{26}.

The VCO control voltages from the phase comparator are the Pin 4 and Pin 5 voltages or

$$V_4 = V_{C9} = V_{B18} = V_{CM} + \tfrac{1}{2}V_{DM} \quad (2)$$

$$V_5 = V_{C12} = V_{B17} = V_{CM} - \tfrac{1}{2}V_{DM} \quad (3)$$

where V_{CM} and V_{DM} are the respective common-mode and difference-mode voltages.

Emitter-followers Q_{17} and Q_{18} convert these control voltages into control currents through D_6 and D_7 of the form

$$I_6 = \frac{1}{R_{15}}\left[V_{CM} - \tfrac{1}{2}V_{DM} - 3\ V_{BE}\right] \quad (4)$$

$$I_7 = \frac{1}{R_{16}}\left[V_{CM} + \tfrac{1}{2}V_{DM} - 3V_{BE}\right] \quad (5)$$

These individual currents are summed in D_8 and become with $R_{15} = R_{16} = R$.

$$I_8 = I = I_6 + I_7 = \tfrac{2}{R}(V_{CM} - 3\ V_{BE}) \quad (6)$$

Writing I_6 and I_7 as functions of the total I current gives

$$I_6 = \frac{I}{2}\left(1 - \frac{V_{DM}}{RI}\right) \quad (7)$$

$$I_7 = \frac{I}{2}\left(1 + \frac{V_{DM}}{RI}\right) \quad (8)$$

Now consider variations in I_6 and I_7 while I remains constant.

Let 'x' indicate the current imbalance such that

$$I_6 = (1 - x)I = \frac{I}{2}\left(1 - \frac{V_{DM}}{RI}\right) \quad (9)$$

$$I_7 = xI = \frac{I}{2}\left(1 + \frac{V_{DM}}{RI}\right) \quad (10)$$

where $0 \leqslant x \leqslant 1$. Thus x is defined to be

$$x = \frac{I}{2}\left(1 + \frac{V_{DM}}{RI}\right) \quad (11)$$

Currents I_6 and I_7 establish proportional currents in Q_{25}, Q_{26}, and Q_{27} in a manner similar to the analysis above since the current in Q_{28} is a constant, or

$$I_O = I_{C28} = I_{E25} + I_{E26} + I_{E27A} + I_{E27B}$$

It can be shown that the $D_7 - D_8$ diode pair will cause identical differential currents to be reflected in both the $Q_{25} - Q_{26}$ and the $Q_{27A} - Q_{27B}$ differential amplifier pairs. Consequently, the constant-current of I_O, jointly shared by the differential amplifier pairs, will divide in each pair with the same x factor imbalance as in Equation 11.

$$I_{E25} + I_{E26} = xI_O \quad (12)$$

$$I_{E25} = I_{E26} = \frac{x}{2}I_O \quad (13)$$

$$I_{E27A} + I_{E27B} = (1 - x)I_O \quad (14)$$

$$I_{E27A} = I_{E27B} = \left(\frac{1-x}{2}\right)I_O \quad (15)$$

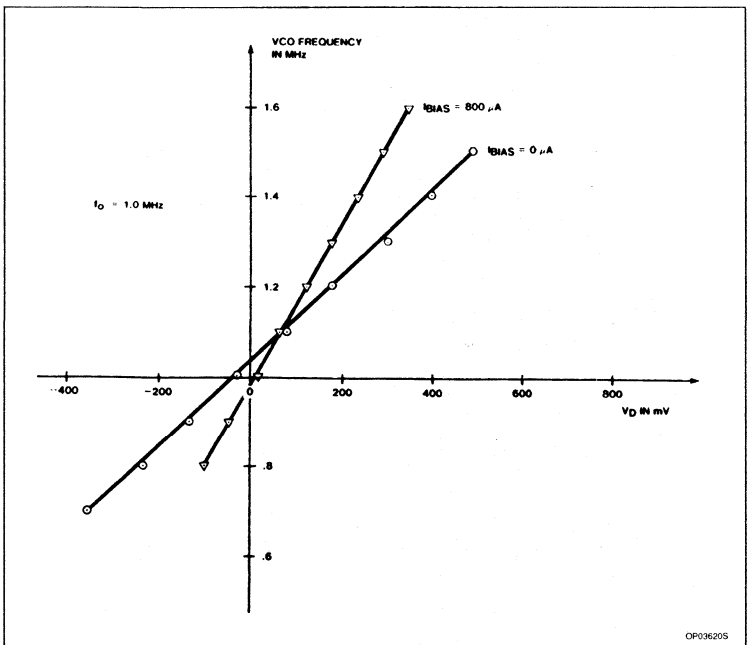


Figure 8. VCO Output as a Function of Input Voltage and Bias Current

Now consider placing a capacitor between the collectors of Q_{25} and Q_{26} (Pins 12 and 13). Oscillation will occur with the capacitor alternately being charged by Q_{21} and Q_{23} and constantly discharged by Q_{25} and Q_{26}. When the Q_{21} and Q_{22} pair conducts, Q_{23} and Q_{24} will be off, causing a negative ramp voltage to appear at Pin 13 and a constant voltage at Pin 12 as shown in Figure 7. During the next half-cycle, the transistor roles and voltages are reversed. Capacitor discharge is via Q_{25} and Q_{26}, which act as constant-current sinks with current amplitudes as in Equation 13.

During each half-cycle, the capacitor voltage changes linearly by $2\Delta V$ volts in ΔT seconds where

$$\Delta V = 2R_{20}I_O\left(\frac{x}{2} + \frac{1-x}{2}\right) = R_{20}I_O \quad (16)$$

and

$$\Delta T = \frac{C2\Delta V}{I_{E25}}. \quad (17)$$

Combining these two equations with Equation 13 gives a half period of

$$\Delta T = \frac{4C\ R_{20}}{x} \quad (18)$$

Utilizing Equation 11 with the ΔT expression gives the desired VCO frequency expression of

$$f_O = f_O'\left(1 + \frac{V_{DM}}{RI}\right) = f_O'\left[\frac{V_{DM}}{2(V_{CM} - 3\ V_{BE})}\right] \quad (19)$$

where f_O' is the VCO's free-running frequency given by

$$f_O' = \frac{1}{22\ R_{20}C} \quad (20)$$

Equation 19 shows that the oscillator frequency is a linear function of the differential voltage from the phase comparator. Resistors R_{35} and R_{36} function to insure that an initial current imbalance exists between the $Q_{25} - Q_{26}$ transistor pair and the dummy Q_{27}. This imbalance insures that the oscillator is self-starting when power is first applied to the circuit.

The VCO conversion gain is determined as

$$K_o = \frac{\partial f_O}{\partial V_{DM}} = \frac{f_O'}{RI}\ Hz/V \quad (21)$$

which is valid as long as the transistor's V_{BE} changes are small with respect to the common-mode voltage. Both f_O and K_o are in-

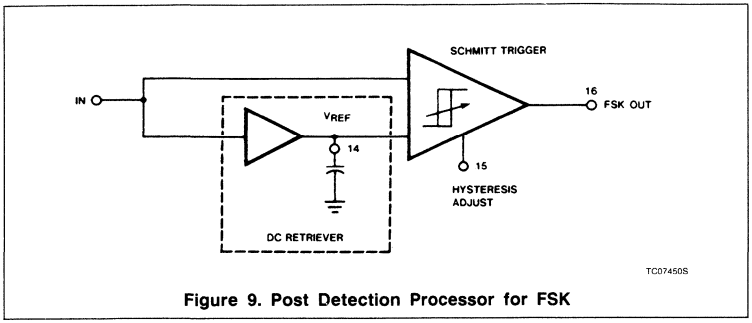


Figure 9. Post Detection Processor for FSK

versely proportional to R, which has a strong positive temperature coefficient. An internal current I_R having an equal and opposite negative temperature coefficient is inserted into the VCO as shown in Figure 6.

Experimental determination of K_o can be found from the data of Figure 8 where K_o is the slope of either line. Numerically these results are for $I_{BIAS} = 0$.

$$K_o = 0.95\frac{\text{MHz}}{\text{V}} = 5.9 \times 10^6\frac{\text{rad}}{\text{volt-sec}} \quad (22)$$

and for $I_{BIAS} = 800\mu A$

$$K_o = 1.7\frac{\text{MHz}}{\text{V}} = 10.45 \times 10^6\frac{\text{rad}}{\text{volt-sec}} \quad (23)$$

It must be noted that the specific values obtained for K_o in the manner above are valid only for the 1.0MHz free-running frequency where the data was taken. However, good estimates for K_o at other free-running frequencies can be obtained by linearly scaling K_o to the desired f_O'. Thus, it is sometimes convenient to define a normalized K_o as

$$K_{o(norm)} = \frac{K_o}{f_O'} = 5.9\ \frac{\text{rad}}{\text{V}}(I_{BIAS} = 0)$$

$$= 10.45\frac{\text{rad}}{\text{V}}(I_{BIAS} = 800\mu A) \quad (24)$$

The K_o estimate for any bias then can be obtained by multiplying the normalized conversion gain by the desired free-running frequency, or

$$K_o(\text{any } f_O') = K_{o(norm)} f_O'. \quad (25)$$

The additional VCO circuitry of Q_{29} through Q_{36} functions to produce the TTL and ECL compatible outputs at Pins 9 and 11.

Amplifier

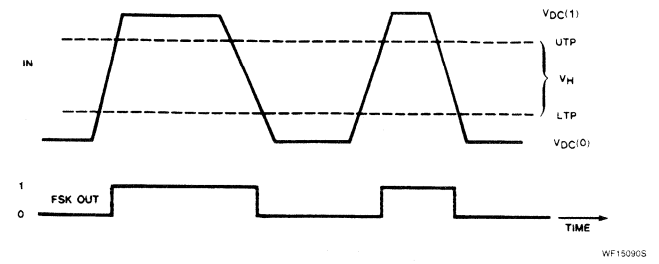
The difference-mode voltage from the phase comparator is extracted and amplified by the amplifier in Figure 1. The single-ended output from this amplifier serves as input signals for both the Schmitt Trigger and a second differential amplifier. Low-pass filtering with a large capacitance at Pin 14 produces a stable DC reference level as the second input to the Schmitt Trigger. When the PLL is locked, the voltage at Pin 14 is directly proportional to the difference between the input frequency and f_O'. Thus Pin 14 provides the demodulated output for an FM input signal.

Schmitt Trigger

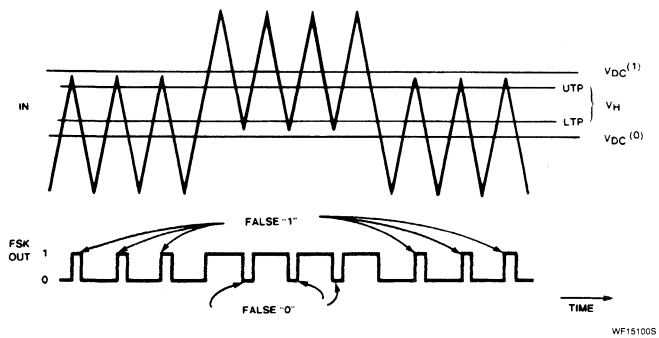
In FSK applications, the Pin 14 voltage will assume two different voltage levels corresponding to the mark and space input frequencies. A voltage comparator could be used to sense and convert these two voltage levels to logic compatible levels. However, at high data rates, V_{DM} will contain a considerable amount of carrier signal which can be removed by extensive filtering. Normally this complex filtering requires quite a few components, most all of which are external to the monolithic PLL. Also, since the control voltage for the comparator depends upon K_o and the deviations of the mark and space frequencies from f_O', the filtering has to be optimized for each different system utilized. However the necessary DC reference level for the comparator is present in the PLL but buried in carrier-frequency feedthrough which appears as noise in the system. A Schmitt trigger with variable hysteresis can be used successfully to decode the FSK data without the need for extensive filtering.

Consider the system shown in Figure 9 where the input signal is the single-ended output derived from the amplifier section of the 564. The DC retriever functions to establish a DC reference voltage for the Schmitt trigger. The upper and lower trigger points are adjustable externally around the reference voltage giving the variable hysteresis. For very low data rates, carrier feedthrough will be negligible and the ideal situation depicted in Figure 10 results. Increased data rate produces the carrier feedthrough shown in Figure 10b, where false FSK outputs result because the feedthrough amplitude exceeds the hysteresis voltage. Having the capability to increase the hysteresis, as in Figure 10c, produces the desired FSK output in the presence of carrier feedthrough.

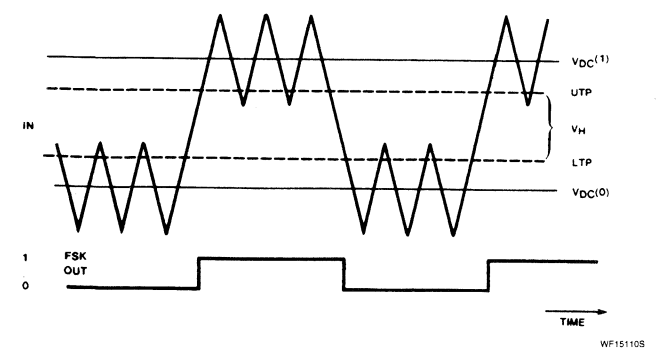
Another important factor to be considered is the temperature drift of the f_O' in the VCO. Small changes in f_O' will change the DC level of the input voltage to the Schmitt trigger. This DC voltage shift would produce errors in the FSK output in narrow-band systems where the mark and space deviations in f_{IN} are less than the f_O' change with temperature. However, this effect can be eliminated if the DC or average value of the amplifier signal is retrieved and used as the reference voltage for the Schmitt trigger. In this manner, variations in the f_O' with temperature do not affect the FSK output.



a. Low Data Rates With Negligible Carrier Feedthrough



b. False FSK Outputs Due to Feedthrough and Low Hysteresis



c. Increased Hysteresis Restores Proper FSK Output in the Presence of Feedthrough

Figure 10. Waveshapes for FSK Decoding in the Post Detection Processor

AN180
Frequency Synthesis with the NE564

Application Note

FREQUENCY SYNTHESIS WITH THE NE564

Frequency multiplication can be achieved with the PLL in two ways:

a. Locking to a harmonic of the input signal.
b. Insertion of a counter (digital frequency divider) in the loop.

Harmonic locking is simpler and usually can be achieved by setting the VCO free-running frequency to a multiple of the input frequency and allowing the PLL to lock. However, a limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. This limits the practical harmonic locking range to multiples of approximately less than ten. For larger multiples, the second scheme is more desirable.

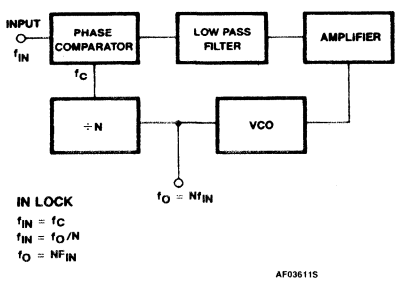
A block diagram of the second scheme is shown in Figure 1a. Here, the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the divided VCO frequency is locked to the input reference frequency so that the VCO is actually running at a multiple of the reference frequency. The amount of multiplication is determined by the counter. An obvious practical application of this multiplication property is the use of the PLL in wide range frequency synthesizers.

In frequency multiplication applications, it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency is DC and is the error voltage which drives the VCO to keep the PLL in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal), if not well filtered, will induce incidental FM on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication, it is generally necessary to filter quite heavily to remove this sum frequency component. The tradeoff, of course, is a reduced capture range and a more under-damped loop transient response.

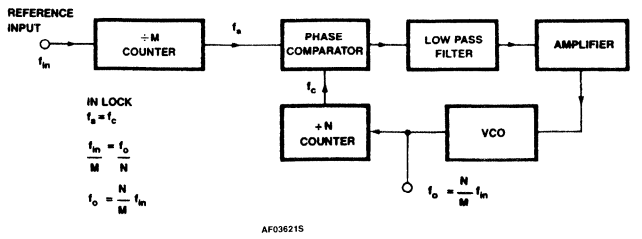
Producing a large number of frequencies with close spacing requires a counter with a large N for the system of Figure 1a. Large N values, in turn, require reference frequencies too low to be practical for commercially available crystals. To overcome this difficulty, a second counter (÷M) is inserted as a prescaler as in Figure 1b to divide down the reference frequency input. This also gives more programming flexibility, since the synthesized output frequencies are functions of both M and N integers, each of which can be changed separately. As an example of fractional frequency synthesis, the two counters can be set to generate an output frequency exactly 16/3 of the input reference frequency. In this case N = 16, M = 3, and the initial f_O' is set to approximately 16/3 times the reference frequency input. The output always will be exactly 16/3 of the input frequency as long as the PLL remains in lock.

PLL frequency synthesizers based upon Figure 1b find wide applications in many types of communications systems that require precisely spaced channels having narrow bandwidths which are centered around relatively high frequencies. For example, Citizens Band (CB) transceiver applications require forty channels corresponding to forty different reference frequencies, each separated by 10kHz bandwidths and centered in the 26 – 27MHz range. Channel 4 uses 27.005MHz; Channel 5 uses 27.015MHz; Channel 6 uses 27.025MHz; and so on. These frequencies could be produced by using forty different crystals — one for each channel. However, this becomes expensive and adds unnecessary complexity to the system. Frequency-mixing techniques have been employed to reduce the number of crystals needed to less than one crystal per channel. For example, one common mixer design uses 14 crystals for 23 channels. As a general rule, most practical approaches that use numerous crystals and mixers to produce discrete frequencies require more than one crystal for every two channel frequencies produced. As the number of channels grows large, frequency synthesis using PLLs becomes more attractive, especially since usually only one or two crystals are needed. Frequency stability of all channels will be essentially the same as that of the crystal reference frequency. Reduced system complexity, size, weight, and power consumption are key advantages of PLL synthesizers.

Since the function of frequency synthesizers is to generate frequencies and not to linearly decode or demodulate input signals, digital PLLs are more commonly used than analog loops.

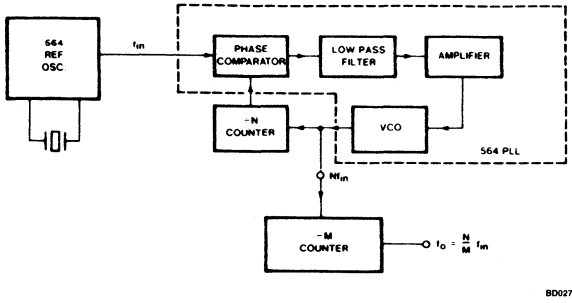


a. Frequency Multiplication

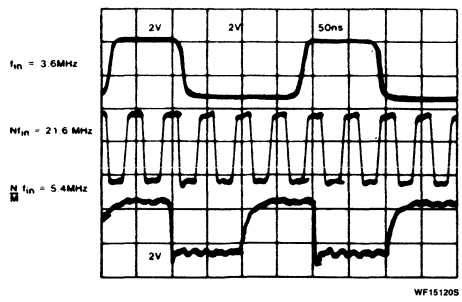


b. Fractional-Frequency Synthesis

Figure 1. Frequency Synthesis Using PLLs

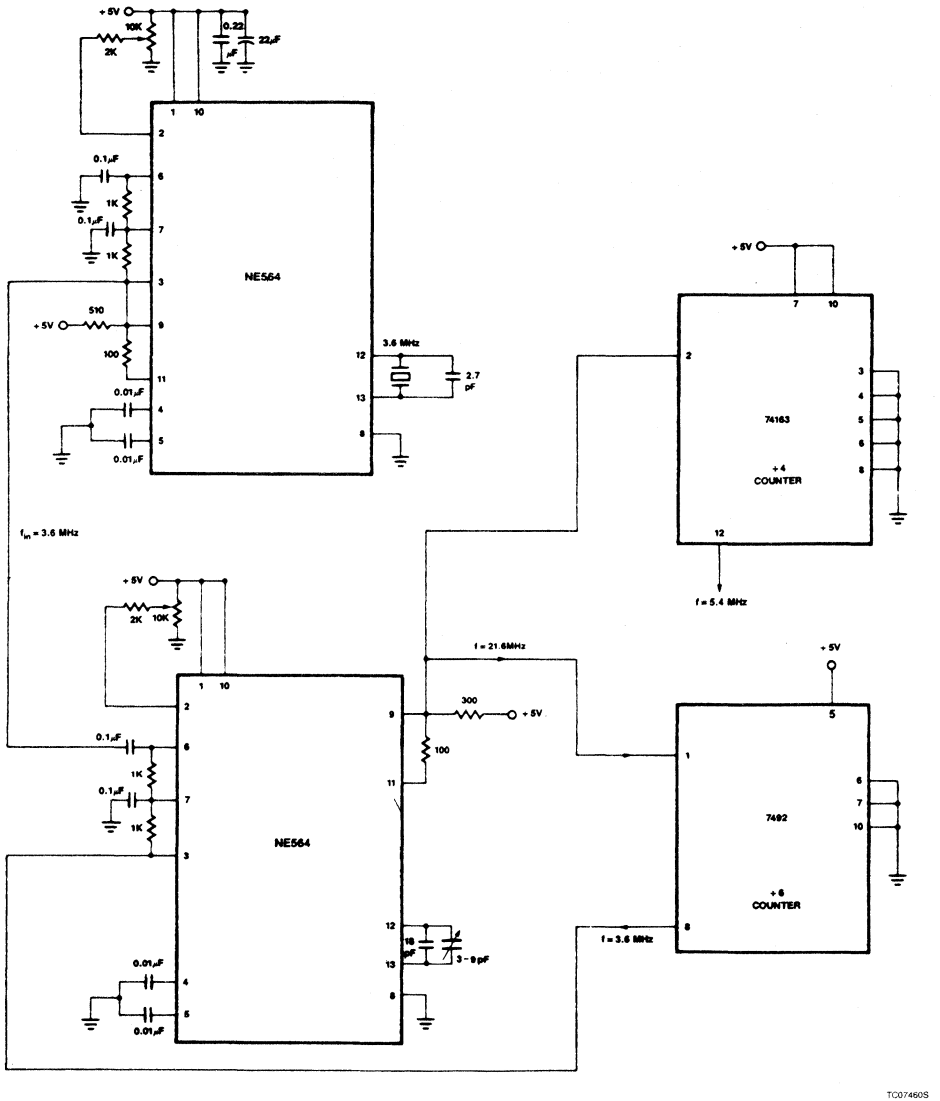


a. Block Diagram Organization



b. Waveshapes

Figure 2. Fractional Frequency Synthesis With the 564



c. Circuit Implementation

Figure 2. Fractional Frequency Synthesis With the 564 (Continued)

Frequency Synthesis with the NE564

AN180

Analog PLLs also can be used for frequency synthesis applications. The 564 is particularly well suited for these applications because the loop is open between the VCO output and the phase comparator input. Also, the phase comparator input and VCO output are compatible with TTL counters.

NE564 FREQUENCY SYNTHESIS WITH CRYSTAL CONTROL

The system shown in Figure 2 has been used to generate frequencies of 5.4MHz and 21.6MHz from a 3.6MHz crystal-controlled source. This reference signal input is produced by using the crystal as the frequency-determining element in the VCO of a second PLL. The thermal stability of all three frequencies will be the same as the stability afforded by the crystal. It may be necessary to place a small detuning capacitor in parallel with the crystal to precisely tune the PLL to the crystal's resonant frequency and to prevent oscillations at harmonics of the resonant frequency. The value of this tuning capacitance must always be kept considerably less than the value required to produce an f_O' without the crystal present. Otherwise the crystal will lose control and the input reference frequency will be set by the capacitor alone.

A recommendation for improved 564 operation is to utilize a divide-by-N counter in the loop which produces "square" waves for the phase comparator that have as close to a 50% duty cycle as possible. Normally, counters with even N values produce square wave outputs perfectly compatible for the phase comparator. Counters for odd N values more commonly produce unsymmetrical outputs that can be less desirable inputs to the phase comparator. An easy modification to "square up" odd divide-by-N counter outputs is to insert a single toggling flip-flop stage between the counter output and the phase comparator's input. This produces an effective 2N multiplication of the input frequency within the PLL. The extra factor of two is removed by a second toggle flip-flop whose input is the output from the first flip-flop. This is the same system as was previously shown in Figure 2a where the +N counter becomes a +2N and M = 2 for the second counter.

AN181
A 6MHz FSK Converter Design Example for the NE564

Application Note

Design Example

It is desired to design an FSK converter operating at 6MHz with deviation of ±1%. Supply voltage is 5V. Input to the 564 is from a radio receiver with an amplitude of $0.5V_{RMS}$. Worst case S/N is 10dB. An overall loop damping factor of 0.5 is specified (ζ).

Using the circuit in Figure 1

First the frequency determining capacitor must be established. Using the equation

$$f_O = \frac{1}{22R_CC_O}$$

where R_C is the internal resistance in the VCO oscillator equal to 100Ω. Given two parameters the third is calculated f_O = 6MHz; therefore

$$C_O = \frac{1}{22 \times 100 \times 6 \times 10^6} = 75pF.$$

A parallel 2 – 20pF trimmer and a 68pF ±5% fixed mica capacitor is chosen.

Next, signal level versus bias current and lock range is examined.

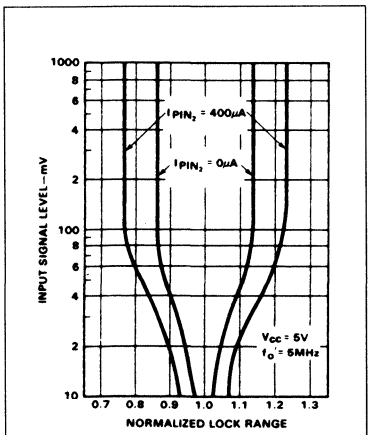


Figure 2. Lock Range vs Signal Input

The signal input to the 564 is specified to be $0.5V_{RMS}$; in the lock range graph, the input level is well within the limiting region of the 564. Thus, no external AM limiter circuit is required and a 10dB S/N (3.1:1) min. should provide reliable communication with a narrow deviation of ±1% (±60kHz) and there is no problem with adequate lock range as it pertains to bias current. We are free to use any loop gain necessary. The bias current sinking into Pin 2 is set to an initial value of 200μA.

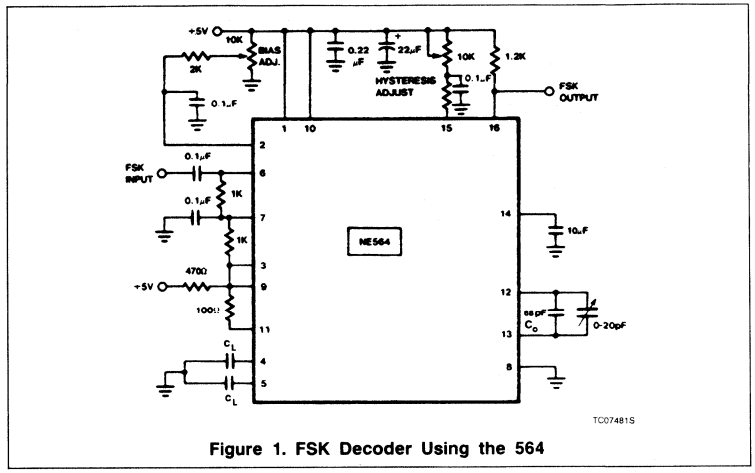


Figure 1. FSK Decoder Using the 564

It's now possible to determine the damping factor of the closed-loop. First, the natural frequency of the loop is calculated from the relationship

$$\omega_n = \sqrt{\frac{K_OK_D}{\tau}} \qquad (1)$$

where

K_O = VCO conversion gain in $\frac{\text{radians}}{\text{sec}\cdot\text{volt}}$

K_D = Phase detector conversion gain in $\frac{\text{volts}}{\text{radian}}$

τ = loop filter time constant in seconds.

For f_O = 6MHz and I_B = 200μA, K_O may be derived from Figure 3a by first constructing an extrapolated transfer line with slope one-quarter of the angle between the existing I_B = 0 and I_B = 800 plots.

Interpolation gives

$$K_O \cong \frac{(1.48 - 1.25MHz)}{(0.4 - 0.2V)} = \frac{\Delta f_O}{\Delta V_O};$$

Multiplying Δf_O by 2π results in

$$K_O = \frac{1.45 \times 10^6 \text{rad/sec}}{0.2V}$$

$$= 7.2 \times 10^6 \frac{\text{radians}}{\text{sec}\cdot\text{volt}}$$

Next, using the K_D graph (Figure 3b), ±1 radian (−90° ±57°); i.e., $\Delta\theta$ = 1 radian, results in an output of 0.6V/rad.

Therefore, $K_D = \frac{0.6}{\text{rad}} = 0.6$ V/rad at I_B = 200μA.

The value obtained for K_O is for data taken at 1MHz and must be multiplied by 6 in order to find the correct value.

Therefore, $K_O = 6 \times 7.2 \times 10^6 \frac{\text{radians}}{\text{sec}\cdot\text{volt}}$

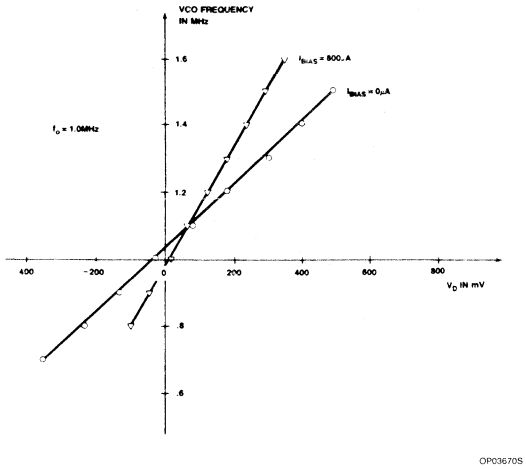
$$(6MH_z) = 4.34 \times 10^7 \frac{\text{radians}}{\text{sec}\cdot\text{volt}}$$

$$K_OK_D = K_V = (4.34 \times 10^7)(0.6) = 2.6 \times 10^7$$

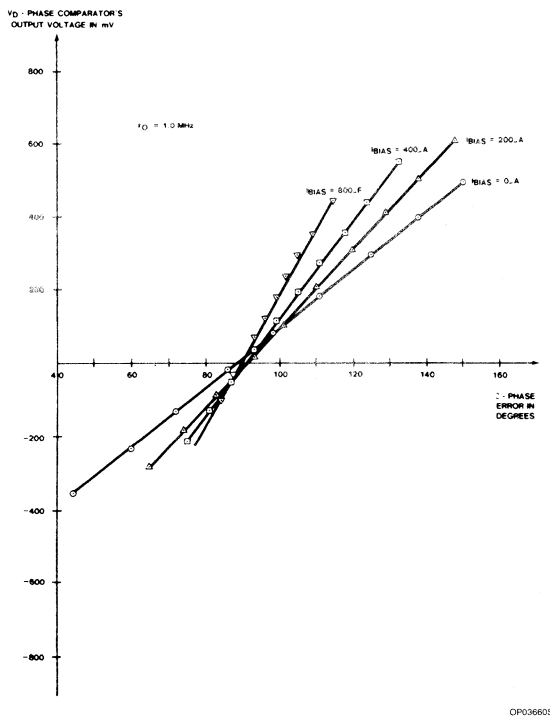
The damping factor specified (0.5) is now used to determine the necessary filter time constant (Pins 4, 5).

$$\zeta = \frac{1}{2\tau}\sqrt{\frac{K_O K_D}{\tau}} = \frac{1}{2\sqrt{K_V\tau}} = \frac{\omega_n}{2K_V} \qquad (2)$$

$$\therefore \tau = \frac{1}{(4)(2.6 \times 10^7)(0.5)^2} = 38ns$$



a. VCO Output Frequency as a Function of Input Voltage and Bias Current (K_O)



b. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current (K_D)

Figure 3.

Note that the filters on Pins 4 and 5 operate differentially with the net effect that break frequency is

$$\omega_p = \frac{1}{RC} \text{ (single pole filter } -3\text{dB freq.)}$$

Now solving for ω_n using (1):

$$\omega_n = \left[\frac{(2.6 \times 10^7)}{(3.8 \times 10^{-8})}\right]^{1/2} = 26 \times 10^6 \text{ radians/sec}$$

f_n = 4.16MHz (natural frequency of the loop and approximate one-sided capture B.W.)

The value of the loop filter capacitor may be determined by dividing the time constant by the value of the internal resistance, 1.3kΩ.

$$C_L = \frac{\tau}{1.3k\Omega} = \frac{3.8 \times 10^{-8}}{1.3 \times 10^3} = 29pF$$

This value filter time constant will give a less-than-critically-damped response allowing the fast excursion in V_{CO} frequency necessary to good FSK reception. The tradeoff between response speed and carrier frequency harmonic rejection will have to be considered. A longer time constant gives more carrier rejection but slower response and less damping (Refer to equation 2).

The next step is to test the circuit under actual operating conditions with the specified FSK signal. The level on Pin 15 (hysteresis adjust) must be set in the vicinity of + 1.4V in order to attain proper FSK demodulation. Final signal tests may be carried out with noise injected through a resistive summing network at the input (Pin 6) to simulate the 10dB S/N.

Note that the loop filter response actually operates on the frequency spectrum above (+) and below (–) the carrier center frequency, or center of deviation, for a symmetric FM or FSK signal. This may be seen in Figure 4.

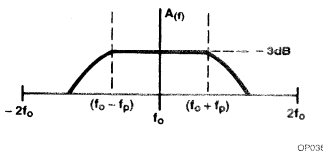


Figure 4. Bandpass Effect of Loop Filter

AN182
Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

Application Note

INTRODUCTION

In order to obtain a local clock signal in Multiplexed Data Transmission systems, a phase and frequency coherent method of signal extraction is required. A Master-Slave system using the quartz crystal as the primary frequency determining element in a phase-lock loop VCO is used to reproduce a phase coherent clock from an asynchronous Data Stream.

The NE564, a versatile phase-locked loop (PLL) operating at frequencies to 50MHz, has inputs and outputs designed to be TTL compatible. The Signetics NE564 is used to generate the phase-locked, crystal-stabilized clock reference signal.

Its particular adaptation, for use with a crystal-controlled VCO instead of the usual RC control elements, requires a brief review of the principles of the Phase-Lock Loop design.

The NE564 Phase-Locked Loop is a fully contained system, including limiter, phase detector, VCO, DC amplifiers, DC retriever and output comparator (reference Figure 1). For the clock regeneration system to be discussed, the portions of the NE564 implemented are the input limiter, phase detector and VCO.

The signal limiter amplifies low level inputs (until saturation is reached, which is typically 60mV$_{P-P}$ for the NE564). The signal limiter output is fed to the phase detector, where the "unknown" input is compared to the "known" VCO frequency of the NE564. The differential error signal that is generated is fed through a DC amplifier and a voltage-to-current converter. The change in the current generated forces the VCO frequency to vary in its frequency and/or phase relationship, such that a θ of 90° lagging is obtained (the actual phase relationship may be somewhat less than 90° depending upon the K_dK_o (gain) product of the NE564 at the operating frequency and bias current). The external filtering incorporated at Pins 4 and 5 control the dynamic frequency response and loop stability criteria.

The NE564 is a first order system; therefore, the use of single capacitors (at Pins 4 and 5) will automatically create a "second-order" system. An RC series filter combination will cause a lead-lag condition that will permit dynamic selectivity, along with closed-loop stability.

LOOP GAIN FUNCTIONS

The phase detector conversion gain (K_d) and the VCO conversion gain (K_o) determine, in large part, the lock range, capture range and linearity characteristics of the NE564. These device parameters are both dependent upon bias current and operating frequency. Some typical curves for each of the parameters are shown for the NE564 in Figures 2 and 3.

THE CLOCK REGENERATOR CIRCUIT

The basic building blocks of the clock regenerator circuit are shown in Figure 4. The PLL is shown as a frequency multiplier incorporating a divide by "N" in the VCO phase detector feedback loop. The functions of the ringing circuit and the NE527 high-speed comparator will be discussed later.

The waveforms of Figure 5 indicate the waveforms transmitted over a T1 line. The bipolar signal transmitted has "no" DC components induced in the transmission line (reference should be made to the effect of normal mode and common effects on signal information). When transmitted over telephone wire pairs, the resultant signal (at the receive end) will have been degraded in both waveshape and signal-to-noise ratios. Typical attenuation factors for a T1 line are −30dB per 6000 feet.

In addition, pair-to-pair crosstalk can degrade signal-to-noise ratios. The energy transmitted in the bipolar system of signal transfer is centered at 772kHz (generated by the bit format).

At the receiving end the bipolar signal information is converted to a unipolar pulse train after being amplified, filtered and fed through an automatic level control circuit. Some types

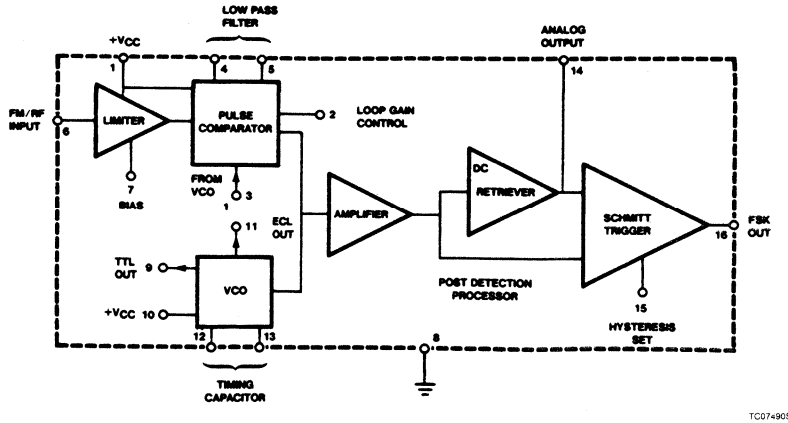


Figure 1

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

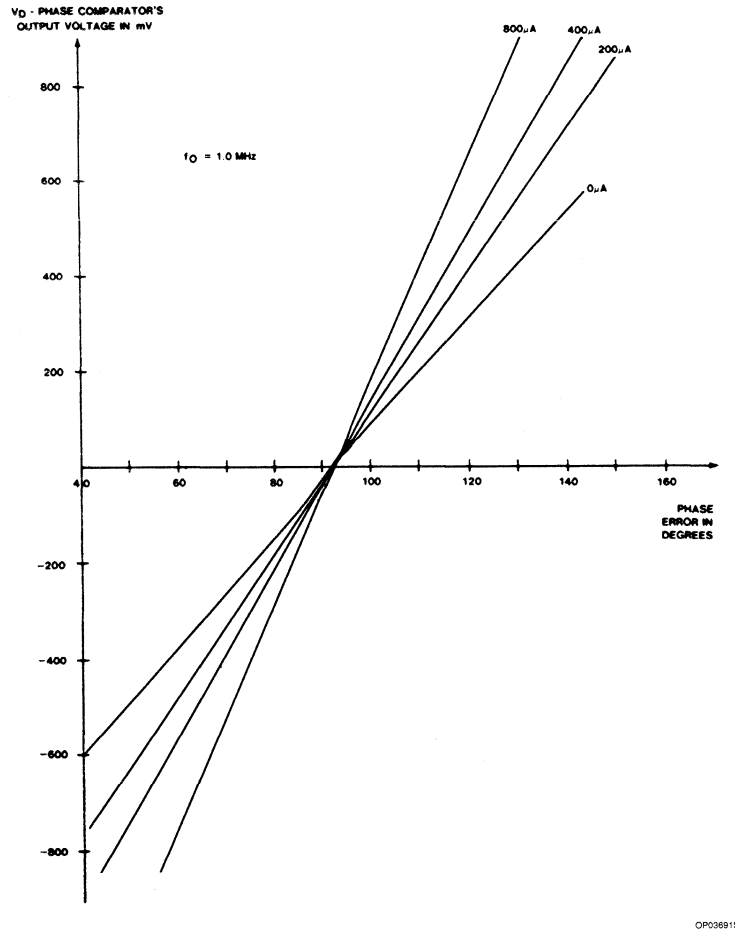


Figure 2. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

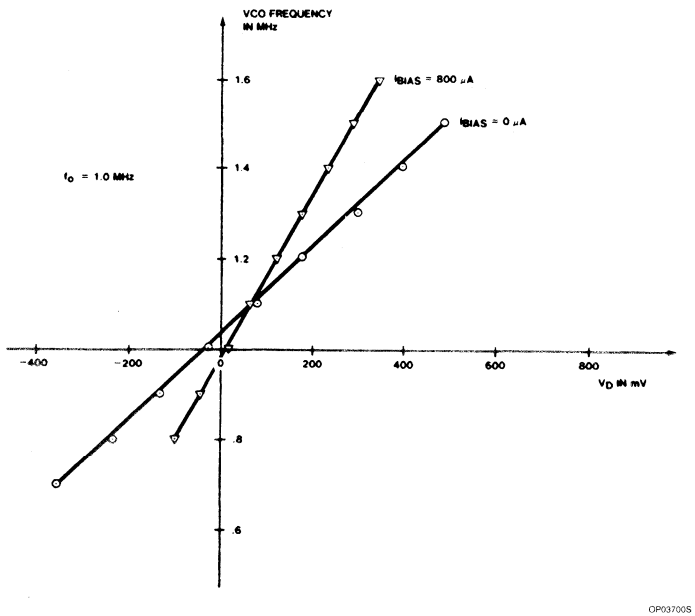


Figure 3. VCO Output Frequency as a Function of Input Voltage and Bias Current

of PCM systems use the rectified and filtered DC (average) to control the phase of the regenerator clock; however, in newer systems, bipolar signals are preprocessed (or preconditioned) by terminal common equipment resulting in unipolar information.

T1 Data Transmission

The bipolar signal, as transmitted on a T1 line, appears below with the original binary, converted unipolar and clock waveform (reference Figure 5).

The bipolar signal, when transmitted over standard wire pairs, will be degraded both in wave shape and signal-to-noise by the time it reaches the signal repeater. This is due to the attenuation factor of the cable which is nearly -30dB for 6000 ft. In addition, pair to pair crosstalk degrades signal-to-noise. The energy in the transmitted bipolar signal is centered at 772kHz due to the particular bit format. Bipolar signals have no DC offset.

At each receiving station the bipolar signal is amplified, filtered and fed through an automatic level control circuit. A full wave rectified signal is then sent to the clock regeneration circuit. This is essentially the format followed by some of the original T1 repeater equipment. The clock regeneration circuit described here could be adapted to this system.

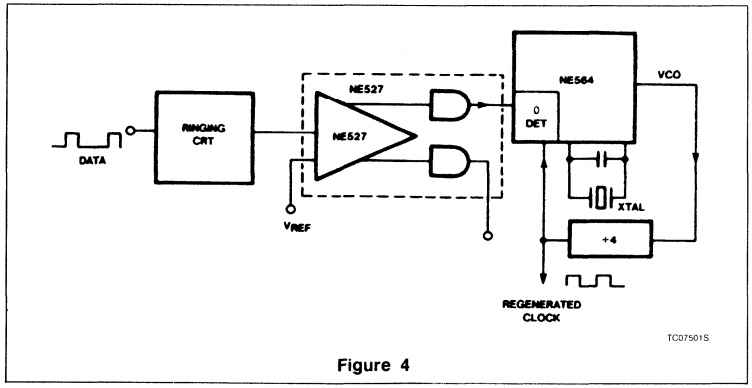


Figure 4

THE T1 SPECTRUM

The bipolar signal is similar to NRZ data in that it does not contain carrier information. In order to give the PLL coherent frequency information sufficient to obtain "capture" and lock, carrier components must be obtained from the data stream. The time duration of the frequency information fed to the PLL is also important in order to obtain accurate and stable information to update the PLL. In order to begin the extraction of frequency information, the positive-going portions of the bipolar data signals are used to drive a class "C" transistor tank circuit (reference Figure 4) which is sharply tuned to the basic clock frequency (1.544MHz). Each positive half cycle of data then starts a wave train of coherent information which is phase synchronous with each succeeding positive data bit. When the LC tank is optimally tuned, relatively extended periods without data bits can be tolerated with minimal loss of frequency and phase information. The combination of good short-term frequency stability of the high "Q" LC tank, coupled with the long-term stability of the crystal-controlled VCO, is the founda-

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

AN182

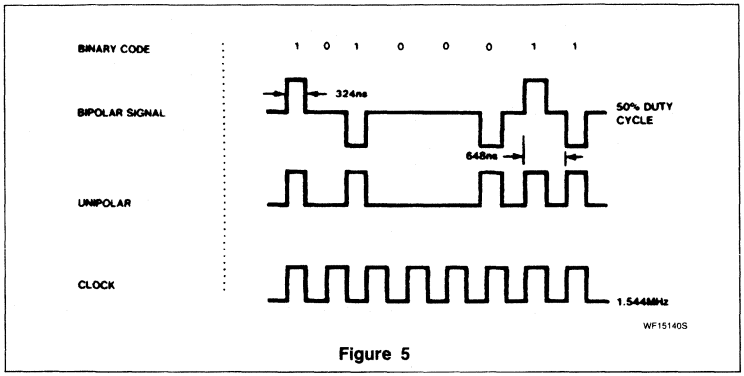


Figure 5

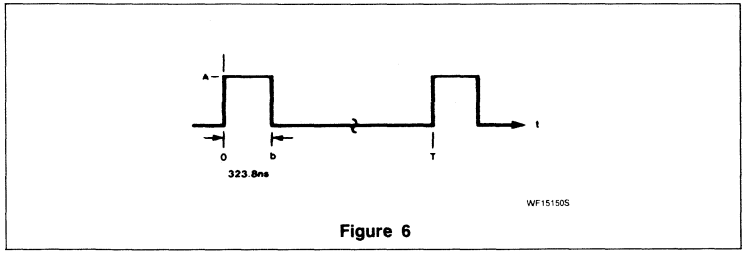


Figure 6

tion of the NE564 clock regeneration system accuracy.

It must be emphasized that data pulse synchronization of the preprocessing circuit must be frequency coherent with the fundamental period of the time base to be extracted. That is, if the time period of the clock is $1/f_C = T$, where f_C is the clock frequency, then the spacing between any positive code bit sequence must be $n \times T$ (reference Figure 6).

Looking at the spectral analysis of the relative energy available to the clock extraction circuitry (with a worst-case duty cycle of 1 of 16) will demonstrate the need for enchancing the particular desired frequency component before applying the signal to the Phase-Lock Loop. For $f_O = 1.544MHz$, the period is $T = 647.67ns$. The pulse or bit width is 323.8ns.

Here the bit duration 323.8ns = b. The Fourier expansion of the discrete spectrum is related by the following equation:

$$F_{(n)} = \frac{(Ab)}{T}\left|\frac{\sin(\frac{n\pi b}{t})}{\frac{n\pi b}{t}}\right| \quad n = 0,1,2\ldots \quad (1)$$

The basic frequency component resulting from various bit spacing factors is defined by the equation

$$f = \frac{1}{T} \quad (2)$$

where $f \leqslant f_O = 1.544MHz$

If we consider the special case of a single pulse present out of 16 bipolar or 32NRZ periods, then

T = 16 bipolar bit times
= 16 × 647.67ns = 10.36μs
f = 96.5kHz

Accordingly, the spectral lines will be spaced in multiples of 96.5kHz. The spectrum for this particular worst case condition is shown in Figure 7 below.

Solving equation 1 for the relative amplitude of the 1.544MHz spectral component with the pulse spacing shown,

$$F_{(16)}\left(\frac{Ab}{T}\right)\left|\frac{\sin(\frac{16\pi b}{t})}{(\frac{16\pi b}{t})}\right|$$

where T = 2nb, n = 16.

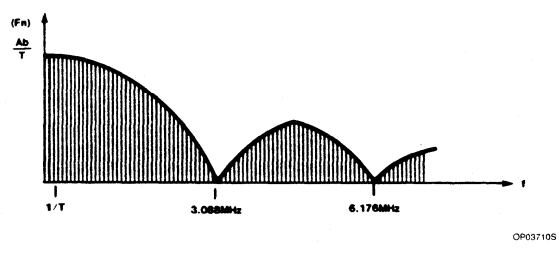
$$= \left(\frac{Ab}{(2)(16)b}\right)\frac{\sin(\frac{16\pi b}{32b})}{(\frac{16\pi b}{32b})} = \frac{A}{32}\,\frac{2}{\pi}$$

$$= (0.02)A$$

$$= -34dB$$

It is evident that as the bit spacing increases to the point where f_O is the 16th harmonic of the fundamental, very little f_O energy is available to drive a phase-lock regeneration circuit. $F_{(16)}$ is also ineffective since it is an even subharmonic of f_O. The PLL will not normally lock to even harmonics; in fact, an error signal is produced which tends to force the VCO out of lock. This fact further stresses the need for preprocessing in the frequency domain. The class "C" pulsed resonant tank significantly multiplies the magnitude of the f_O spectral component and filters out unwanted subharmonics.

The loop error voltage available from the phase detector for phase correction of the VCO is directly related to the product of the incoming coherent spectral energy multiplied in the balanced mixer with the reference signal derived from the VCO. Since the phase error information is integrated in the loop filters, the instantaneous magnitude of the DC error voltage is proportional to the time integral of coherent mixer products. Thus, as the magnitude and time duration of the desired frequency component is increased in the



NOTE:
= 96.5kHz spacing

Figure 7

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

preprocessing circuitry, the VCO phase accuracy is greatly improved. Capture time is obviously enhanced also.

The signal from the tuned tank is buffered by a FET follower N-channel enhancement mode device (reference Figure 12). This provides power gain with virtually no loading on the tank circuit and avoids degrading the "Q". The NE527 comparator is used to provide waveform shaping and symmetry correction. The voltage threshold is set up by a resistive divider with adjustment set for equal duty cycle symmetry. (Note: Recent tests have shown that best crystal lock range symmetry is achieved when the input signal to Pin 6 of the NE564 is maintained at a level between 500 to 800mVP-P.) The coupling network provides the necessary attenuation plus a low impedance signal source which is critical to good Phase Detector operation.

In the particular circuit shown in Figure 12, the 1.544MHz information is applied to the phase detector input of the NE564 Phase-Lock Loop. The VCO, however, is operated at four (4) times this frequency to order to take advantage of economical and readily available crystals. The VCO signal is fed through a divide-by-four counter (74HCT73) to provide the Phase Detector reference and final regenerated clock signal. To avoid loading, the clock signal (1.544MHz) is buffered by the 75451 peripheral driver which provides a high-speed open collector TTL output. The input signal is AC coupled in order to reduce DC bias errors in the Phase Detector caused by "O" level variations.

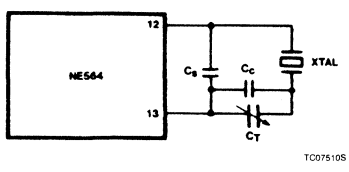


Figure 8

The Crystal[1]

The crystal used was chosen to match the NE564 VCO drive characteristics. It is an "AT" cut oscillator crystal which operates near the anti-resonate or "parallel" mode in this circuit. The crystal may have to be fine-tuned, as indicated in Figure 8. The pulling characteristic of the crystal is adequate to allow for 0 to 70°C operational drift plus initial and aging accuracy tolerance factors and still retain lock between master and slave station VCXOs. The average lock range at room temperature with one of sixteen data bits present is typically 1000Hz for a 6.176MHz crystal with a capture range greater than 500Hz.

For VCO operation at 6.176MHz, C_S is 22pF, C_C is 18pF, and C_t, a 1 – 8pF trimmer capacitor (reference Figure 8).

NE564 CRYSTAL-CONTROLLED VCO

As shown in Figure 8, the crystal is operated with a series capacitor. When properly trimmed, this allows the crystal to operate near the series resonant mode. A crystal manufactured to operate in the series resonant mode will do so only if it sees a pure resistance looking into the oscillator terminals. The circuit below shows an oscillator which looks inductive with the equivalent crystal circuit and trimmer capacitor C_t (reference Figure 9).

If L_O is small and the internal gain of the device high over a wide frequency range, L_O may resonate with the C_O of the crystal at a very high frequency. Under certain conditions the circuit may even tend to operate in the 3rd overtone mode unless measures are taken to roll-off the circuit gain. This is the purpose of C_S in Figure 8. Since the gain of the VCO is a factor in spurious oscillation, the current injected into Pin 2 will also have an effect in this respect. (K_O increases with I_2). At higher operating frequencies this parameter may become more critical in attaining stable start ups in the desired frequency mode. Obviously the size of C_S must be smaller than the value needed to cause free running near the desired frequency without the crystal connected.

CRYSTAL SPECIFICATION

Crystals may be manufactured to operate in either the series mode with no external capacitance (purely resistive load) or in the parallel mode with a specified value of load capacitance. The 564 tends to operate at a frequency above the specified value when a series mode crystal is used. For a design frequency of 6.176000MHz and zero load capacitance. Referring to Figure 8, for C_s = 10pF and C_T = 10pF the average center frequency for an NE564 sample measured in the lab was 6181.192kHz. For the same C_s, but with C_T equal to 60pF, f_O measured 6176.565kHz. A second crystal showed a spread of 6176.600kHz to 6180.855kHz. The effect of the VCO was to pull the crystal to a frequency above its design value. This effect is then nearly tuned out by the external capacitances C_S and C_T. If C_T is sufficiently increased, the crystal will see a purely resistive load and operate at its rated frequency.

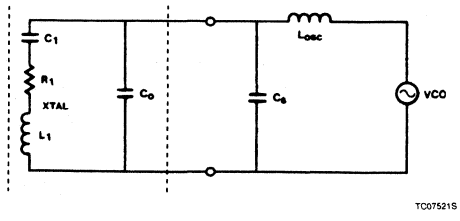
A second approach is to specify a crystal which is to operate near the anti-resonate or parallel mode. Normally this is done with a certain value of external load capacitance specified by the customer which matches the existing circuit parameters. The maximum difference between series and parallel resonance for any crystal is 0.5% of f_O (series resonant mode); for f_r = 6.126MHz, 0.5% of f_r = 30kHz. The usual value would be lower than this.

$$f_a = f_r \sqrt{1 + \frac{1}{r_O}}$$

r_O = electromechanical coupling factor, f_a = parallel resonant frequency). The particular cut of the crystal material determines the drift response over temperature. For oscillator applications, the AT cut offers the best overall stability over a wide frequency and temperature range. Final design uses second approach.

For a stability or total tolerance of ±15ppm over the rated operating range of −20°C to +70°C, a certain manufacturer's crystal actually performed as shown above (Refer to Figure 11).

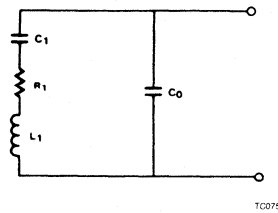
Calibration accuracy is the allowable frequency tolerance at the reference temperature, i.e., ±10ppm @ 25°C.



NOTES:
C_0 = XTAL Shunt capacitors
C_1 = Equivalent XTAL series resonant arm capacitance
L_1 = Equivalent Motional Inductance
R_1 = Equivalent crystal series resistance
C_5 = External shunt or stray capacitance

Figure 9

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)



NOTES:
C_1 = Motional capacitance
C_0 = Shunt capacitance
R_1 = Equivalent Resistance
L_1 = Equivalent inductance

Figure 10. Basic Crystal Equivalent Circuit



Figure 11. Design Example

Third, is a long-term drift spec which determines the customer's maximum allowable drift due to aging effects. An acceptable value in quality crystals is ±2ppm/year.

Using our reference crystal of 6.176MHz and the above specifications, the crystal limits over a 1 year period would be:

Temperature stability:	±15ppm × 6.176 =±93Hz
Calibration tolerance:	±10ppm × 6.176 =±62Hz
@25°C Long term drift:	±2ppm × 1 × 6.176 =±12Hz
Total:	(±167Hz)

The above figure of ±167Hz then determines the capture and lock range over which two crystal stabilized VCOs must track under worst case conditions when the exact same crystal specifications are used for master and slave units within an operational system.

Crystal Specifications

'AT' Cut Oscillator Type

Fundamental mode operation HC-33 Case (Standard)

Calibration tolerance:
±10ppm @ 25°C

Temperature stability:
±15ppm; −15°C to +65°C

Circuit operating condition:
Parallel resonance

Frequency specified: 6.176000MHz

Part designation:
Croven #A330 DEF-32 or equivalent

Setup Procedure[2]

Referring to Figure 12, the following setup procedure will aid the user in establishing proper circuit operation.

Regulated supply voltage of +5V and −6V are required. Current drain on the +5V line is ~ 100mA, and 6mA for the −6V.

With proper voltage applied, (1) First check the supply currents to be sure they are in the range indicated above. (2) Check the operation of the NE564 VCXO by looking at Pin 9 with an oscilloscope (see Figure 13). A reasonably symmetric square wave should be present, having a frequency near 6.1MHz. (3) Attach a DVM across the 2k resistor which feeds Pin 2 of the NE564 and adjust for a reading of 2.00V, indicating a 1mA $_{DC}$ current flowing into Pin 2 (The (+) lead of the DVM should be connected to the end of the 2k resistor which ties to the wiper of the 10k pot and the (−) lead to Pin 2 of the 564; reference Figure 14). (4) The exact center frequency is set by adjusting C_t, the crystal trimmer cap, for exactly 6.176000MHz with no signal input (this sets the center frequency of the VCXO to free-run in the center of the capture range). (5) Enable strobe 'A' and 'B' with a +2.7V min. to +5V max. level. Apply a standard 1.544MBS NRZ data signal to the input terminal, terminated in 50Ω. The amplitude should be +3 to +5V (0 to peak). Set the duty cycle for 1 bit in a 16-bit period. Note the data generator must be driven from a crystal-controlled master oscillator also adjusted for a center data rate of 1.544 000MBS. Monitor the buffered output of the ringing circuit with a scope connected to the source of the SD213 (Figure 15). The waveform should appear as in Figure 17. (6) Adjust tank trimmer cap C_T for a maximum amplitude and note that the cycle period should be 647ns. (7) Now monitor the comparator output signal at Pin 7 and adjust R_t for a 50% duty cycle. The same signal will appear at Pin 5 of the NE527 except it will be inverted. The signal on Pin 7 of the NE527 and Pin 6 of the NE564 should appear as shown in Figure 19. Now attach one lead of a dual-trace scope to Pin 7 of the NE527 and the other to Pin 3 of the NE564 as shown (Figure 16).

The two signals should be in phase-locked with an approximate 90° differential as shown in Figure 20 (data signal applied to @ 1.544MBS). If lock does not occur, a slight trimming of the crystal trimmer C_T should correct for slight differences in master-to-slave crystal tolerance. It is recommended that master and slave crystals be of the exact same design and specification to insure optimal tracking over time and temperature. A recommended manufacturer and part number appears at the end of this application note for your convenience.

Once lock is attained, move one lead of the dual-trace scope to the buffered output of the 75451 Pin 3, leaving the other scope probe on Pin 6 of the NE564. The phase-locked waveform should appear as in Figure 25. If a data word generator is being used, you may check overall operation for various bit patterns by synchronizing the scope trigger on the "end of word" pulse, then observe the phase error effect as different combinations are fed in.

PHASE JITTER[3]

When operating with real-time data transmission, the PLL loop filters must be optimized to minimize regenerated clock jitter. A good grade of mylar capacitor is recommended as connected to Pins 4 and 5 of the NE564. A simple pair of shunt-connected loop filter caps of 0.33μF to 0.76μF was found to be adequate.

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

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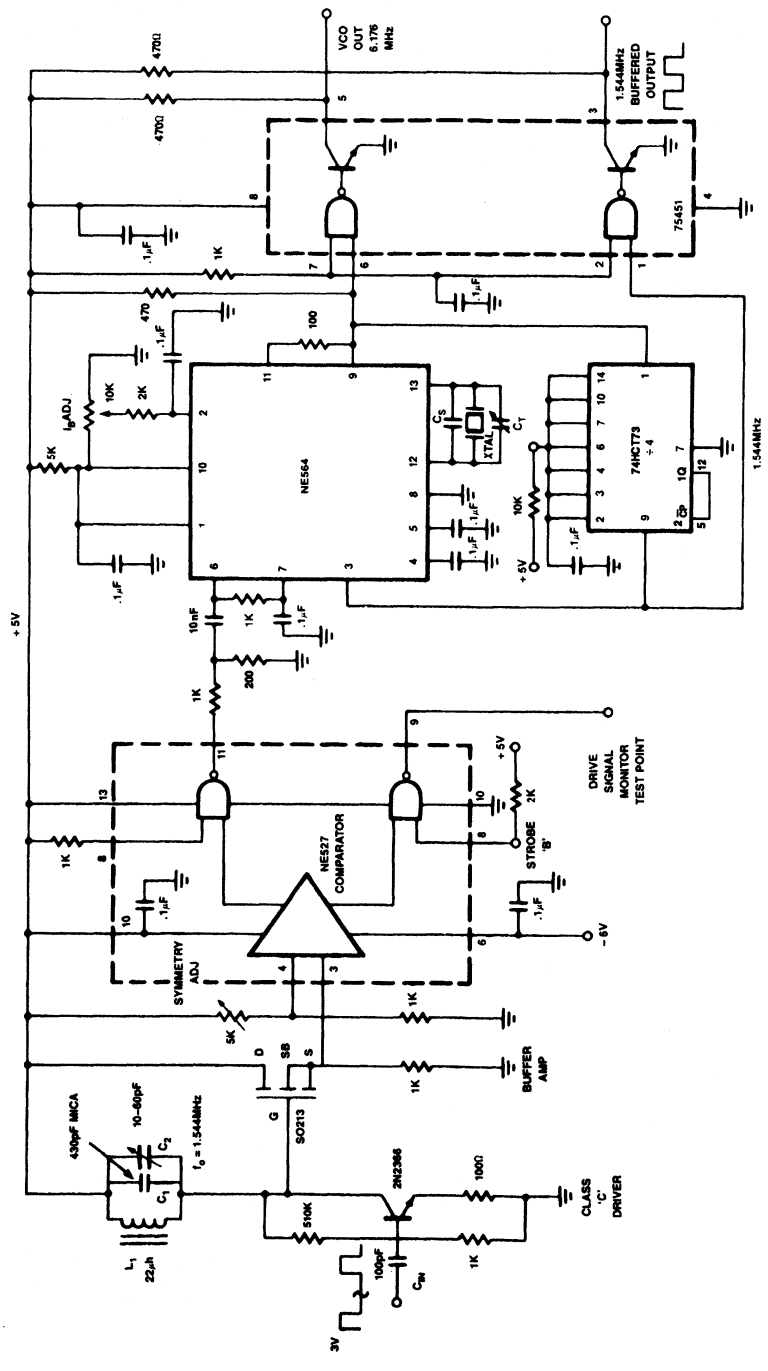
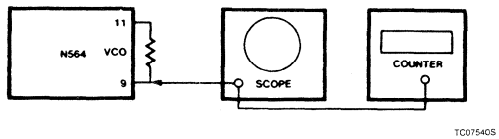


Figure 12. Data Transmission System Clock Regenerator

NOTES:
C_S = 100pF silver mica
C_T = 1-8pF trimmer
XTAL = crven A330 Def-32
'AT' cut oscillator or equivalent
crystal f_O = 6.176000MHz.

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

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NOTE:
Check VCO free-running frequency and output waveshape.

Figure 13. Check VCO Free-Running Frequency and Output Waveshape

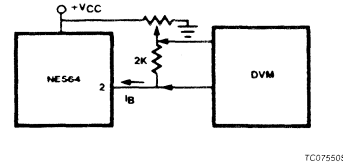


Figure 14

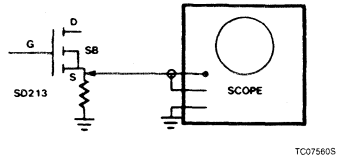


Figure 15

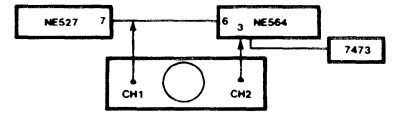


Figure 16

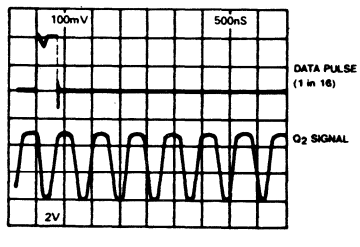


Figure 17. Ringing Circuit Response (1 Data Pulse in 16)

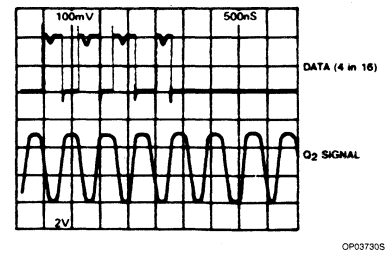


Figure 18. Ringing Circuit Response (4 Data Pulses in 16)

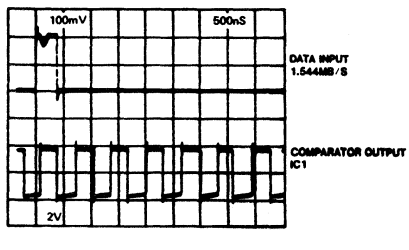


Figure 19. Ringing Circuit to Square Wave Conversion

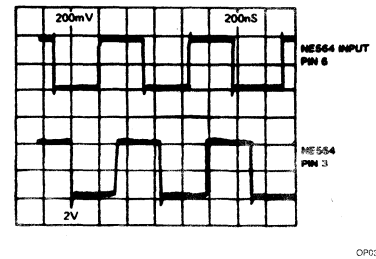


Figure 20. Phase Comparator Signals (in Lock)

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

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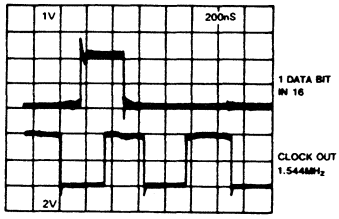


Figure 21. Regenerated Clock Signals

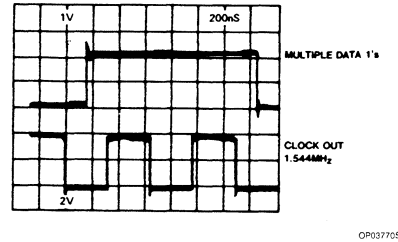


Figure 22. Regenerated Clock Signals

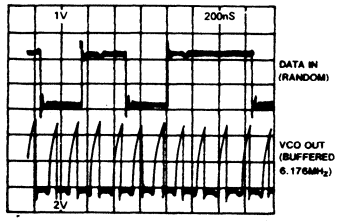


Figure 23. Regenerated Clock Signals Relative to NE564 VCO Signal

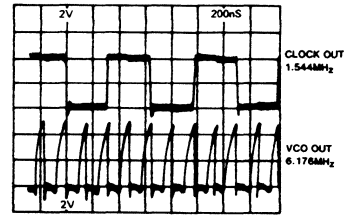


Figure 24. Regenerated Clock Signal Relative to NE564 VCO Signal

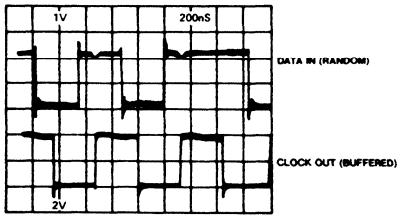


Figure 25. Regenerated Clock Signal Relative to Random NRZ Data Signal

NOTES:
1. Recent versions of this circuit no longer require series capacitors C_C and C_T. See Figure 12.
2. Input levels to the NE564 have been reduced for this application to $\simeq$ 800mVp-p. See Figure 12.
3. Improved operation regarding clock jitter is obtained by carefully decoupling the divider counter ICs and the PLL's V_{CC} line. This is accomplished by adding a small series "R" into the V_{CC} line with the bypass capacitor to ground.

References

1. "Fourier Analysis" by Hwei P. Hsu. Simon & Schuster Tech Outlines
2. "Pulse and Digital Circuits" by Millman and Taub McGraw Hill
3. "Phaselock Techniques" by Floyd M. Gardner Wiley, 1966

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Circuit Description of the NE565 PLL

Application Note

CIRCUIT DESCRIPTION OF THE NE565 PLL

The 565 is a general purpose PLL designed to operate at frequencies below 1MHz. The loop is broken between the VCO and phase comparator to allow the insertion of a counter for frequency multiplication applications. With the 565, it is also possible to break the loop between the output of the phase comparator and the control terminal of the VCO to allow additional stages of gain or filtering. This is described later in this section.

The VCO is made up of a precision current source and a non-saturating Schmitt trigger. In operation, the current source alternately charges and discharges an external timing capacitor between two switching levels of the Schmitt trigger, which in turn controls the direction of current generated by the current source.

A simplified diagram of the VCO is shown in Figure 1. I_1 is the charging current created by the application of the control voltage V_C. In the initial state, Q_3 is off and the current I_1 charges capacitor C_1 through the diode D_2. When the voltage on C_1 reaches the upper triggering threshold, the Schmitt trigger changes state and activates the transistor Q_3. This provides a current sink and essentially grounds the emitters of Q_1 and Q_2. The charging current I_1 now flows through D_1, Q_1 and Q_3 to ground. Since the base-emitter voltage of Q_2 is the same as that of Q_1, an equal current flows through Q_2. This discharges the capacitor C_1 until the lower triggering threshold is reached, at which point the cycle repeats itself. Because the capacitor C_1 is charged and discharged with the constant current I_1, the VCO produces a triangle waveform as well as the square wave output of the Schmitt trigger.

The complete circuit for the 565 is shown in Figure 2. Transistors $Q_1 - Q_7$ and diodes $D_1 - D_3$ form the precision current source. The base of Q_1 is the control voltage input to the VCO. This voltage is transferred to Pin 8 where it is applied across the external resistor R_1. This develops a current through R_1 which enters Pin 8 and becomes the charging current for the VCO. With the exception of the negligible Q_1 base current, all the current that enters Pin 8 appears at the anodes of diodes D_2 and D_3. When Q_8 (controlled by the Schmitt trigger) is on, D_3 is reverse-biased and all the current flows through D_2 to the duplicating current source $Q_5 - Q_7$, $R_2 - R_3$ and appears as the capacitor discharge current at the collector of Q_5. When Q_8 is off, the duplicating current source $Q_5 - Q_7$, $R_2 - R_3$ floats and the charging current passes through D_3 to charge C_1.

The Schmitt trigger (Q_{11}, Q_{12}) is driven from the capacitor triangle waveform by the emitter-follower Q_9. Diodes $D_6 - D_9$ prevent saturation of Q_{11} and Q_{12}, enhancing the switching speed. The Schmitt trigger output is buffered by emitter-follower Q_{13} and is brought out to Pin 4, and is also connected back to the current source by the differential amplifier ($Q_{14} - Q_{16}$).

When operated from dual symmetrical supplies, the square wave on Pin 4 will swing between a low level of slightly (0.2V) below ground to a high level of one diode voltage drop (0.7V) below the positive supply. The triangle waveform on Pin 9 is approximately centered between the positive and negative supplies and has an amplitude of 2V with supply voltages of ±5V. The amplitude of the triangle waveform is directly proportional to the supply voltages.

The phase comparator is again of the doubly-balanced modulator type. Transistors Q_{20} and Q_{24} form the signal input stage, and must be biased externally. If dual symmetrical supplies are used, it is simplest to bias Q_{20} and Q_{24} through external resistors to ground.

The switching stage Q_{18}, Q_{19}, Q_{22} and Q_{23} is driven from the Schmitt trigger via Pin 5 and D_{11}. Diodes D_{12} and D_{13} limit the phase comparator output, and differential amplifier Q_{26} and Q_{27} provides increased loop gain.

The loop low pass filter is formed with an external capacitor (connected to Pin 7) and the collector resistance R_{24} (typically 3.6kΩ). The voltage on Pin 7 becomes the error voltage which is then connected back to the control voltage terminal of the VCO (base of Q_1). Pin 6 is connected to a tap on the bias resistor string and provides a reference voltage which is nominally equal to the output voltage on Pin 7. This allows differential stages to be both biased and driven by connecting them to Pins 6 and 7.

The free-running center frequency of the 565 is adjusted by means of R_1 and C_1 and is given approximately by

$$f_O' \simeq \frac{1.2}{4R_1C_1} \qquad (1)$$

When the phase comparator is in the limiting mode ($V_{IN} \geqslant 200mV_{P-P}$), the lock range can be calculated from the expression:

$$2\omega_L = 2K_oK_dA\theta_d \qquad (2)$$

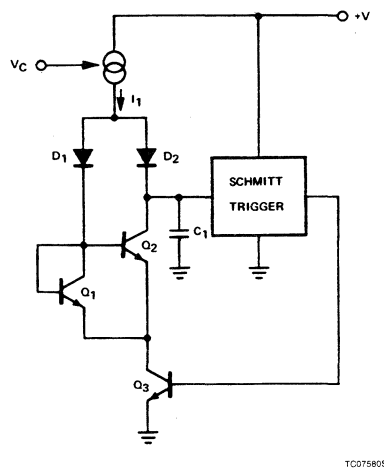


Figure 1. Simplified Diagram of NE565 VCO

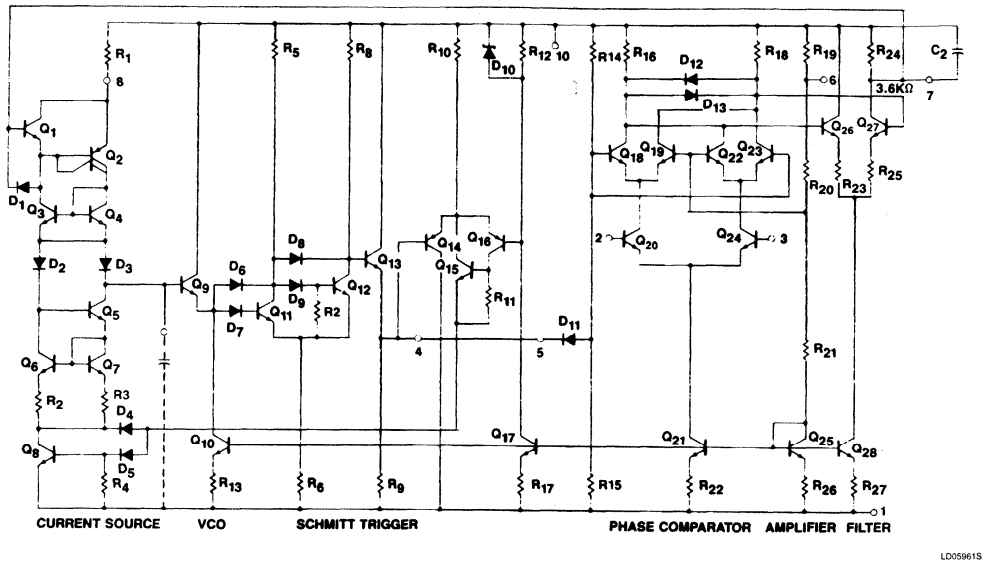


Figure 2. Circuit Diagram of 565

where K_o is the VCO conversion gain, K_d is the phase comparator's conversion gain, A is the amplifier gain, and θ_d is the maximum phase error over which the loop can remain in lock. Specific values for the terms of Equation 2 for the 565 are

$$K_d = \frac{1.4}{\pi} V/rad \quad (3)$$

$$A = 1.4 \quad (4)$$

$$e_d = \frac{\pi}{2} rad \quad (5)$$

$$K_o = \frac{50 f_O'}{V_{CC}} \frac{rad}{Volt\text{-}sec} \quad (6)$$

where V_{CC} is the total supply voltage applied to the circuit.

The tracking range for the 565 then becomes:

$$f_L \cong \pm \frac{\omega_L}{2\pi} \cong \pm \frac{8 f_O}{V_{CC}} Hz \quad (7)$$

to each side of the free-running frequency, or a total lock range of:

$$2f_L \cong \pm \frac{16 f_O}{V_{CC}} Hz \quad (8)$$

The capture range, over which the loop can acquire lock with the input signal, is given approximately by:

$$2\omega_C \cong 2\sqrt{\frac{\omega_L}{\tau}} \quad (9)$$

where ω_L is the one-sided tracking range

$$\omega_L = 2\pi f_L \quad (10)$$

and τ is the time constant of the loop filter

$$\tau = RC_2 \quad (11)$$

The lock-in range can be written as:

$$f_C \cong \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}} = \pm \frac{1}{2\pi} \sqrt{\frac{32\pi f_O'}{V_{CC}}} \quad (12)$$

to each side of the free-running frequency or a total capture range of:

$$f_C \cong \frac{1}{\pi} \sqrt{\frac{32\pi f_O'}{\tau V_{CC}}} \quad (13)$$

This approximation works well for narrow capture ranges ($f_C = 1/3 f_L$) but becomes too large as the limiting case is approached ($f_C = f_L$).

When it is desired to operate the 565 out of its limiting mode ($V_{IN} < 200mV_{P\text{-}P}$ or $32mV_{RMS}$), K_d can be estimated from the graph in Figure 3 for the specific input voltage anticipated. The previous calculations for the lock and capture ranges remain valid with the new value of K_d from the graph being used to replace the K_dA product in Equation 2. In Figure 3, the DC amplifier gain A has been included in the K_d value.

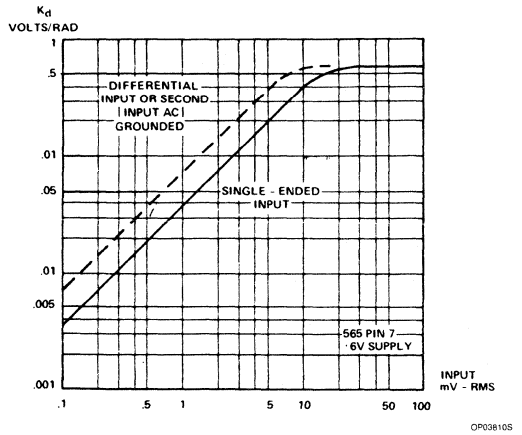


Figure 3. Phase Comparator's Conversion Gain, K_d, for the 565 as a Function of Input Signal Amplitude

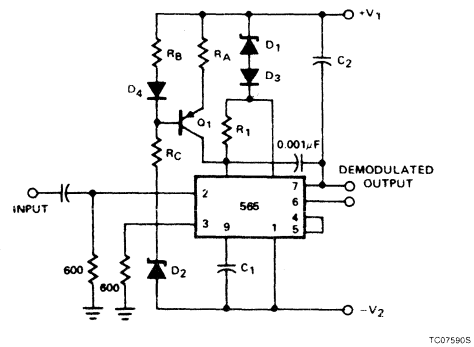


Figure 4. Narrow Bandwidth FM Demodulator Using the 565

For applications where both a narrow lock range and a large output voltage swing are required, it is necessary to inject a constant current into Pin 8 and increase the value of R_1. One scheme for this is shown in Figure 4. The basis for this scheme is the fact that the output voltage controls only the current through R_1, while the current through Q_1 remains constant. Thus, if most of the charging current is due to Q_1 the total current can be varied only a small amount due to the small change in current through R_1. Consequently, the VCO can track the input signal over a small frequency range, yet the output voltage of the loop (control voltage of the VCO) will swing its maximum value.

Diode D_1 is a Zener diode, used to allow a larger voltage drop across R_A than would otherwise be available. D_4 is a diode which should be matched to the emitter-base junction of Q_1 for temperature stability. In addition, D_1 and D_2 should have the same breakdown voltages and D_3 and D_4 should be similar so that the voltage seen across R_B and R_C is the same as that seen across Pins 10 and 1 of the phase-locked loop. This causes the frequency of the loop to be insensitive to power supply variations. The free-running frequency can be found by:

$$f_O' \simeq \frac{2R_B}{(R_B + R_C)R_AC_1} + \frac{1}{4R_1C_1}\ \text{Hz} \qquad (14)$$

and the total range is given by:

$$2f_L \cong \frac{22.4V_D(R_B + R_C)R_Af_O'}{(|V_1| + |V_2| - V_Z - V_D)[8R_BR_1 + R_A(R_B + R_C)]}\ \text{Hz} \qquad (15)$$

where V_D is the forward-biased diode voltage ($\simeq$0.7V), V_Z is the zener diode breakdown voltage, V_1 is the positive supply voltage, and V_2 is the negative supply voltage.

When the output excursion at Pin 7 need be only a volt or so, diodes D_1, D_2 and D_3 may be replaced by short circuits.

The value of R_1 can be selected to give a prescribed output voltage for a given frequency deviation.

$$R_1 = \frac{R_A(R_B + R_C)f_O'}{R_B(|V_1| + |V_2| - 0.7)\Delta f} \qquad (16)$$

where Δf is the desired frequency deviation per volt of output.

In most instances, R_B and R_A are chosen to be equal so that the voltage drop across them is about 200mV. For best temperature stability, diode D_1 should be a base-collector shorted transistor of the same type as Q_1.

When the 565 is connected normally, feedback to the VCO from the phase comparator is internal. That is, an amplifier makes the Pin 8 voltage track the Pin 7 (phase comparator output) voltage. Since the capacitor C_1 charge current is determined by the current through resistance R_1, the frequency is a function of the voltage at Pin 8. It is possible, however, to bypass and swamp the internal loop amplifier so that the current into Pin 8 is no longer a function of the Pin 8 voltage but only of the Pin 7 voltage. This makes a greater charge-discharge current variation possible, allowing a greater lock range. Figure 5 shows such a circuit in which the μA741 operational amplifier is set for a differential gain of 5, feeding current to Pin 8 through the 33kΩ resistor (simulating a current source). Not only is the tracking range greatly expanded, but the output voltage as a function of frequency is five times greater than normal. In setting up such a circuit, the designer should keep in mind that for best frequency stability, the charge-discharge current should be in the range of 50 to 1500μA, which also specifies the Pin 8 input current range, showing that a ratio of upper to lower lock extremes of about 30 can be achieved.

Many times it would be advantageous to be able to break the feedback connection between the output (Pin 7) and the control voltage terminal (Q_1) of the VCO. This can be easily done once it is seen that it is the *current* into Pin 8 which controls the VCO frequency. Replacing the external resistor R_1 with a current source, such as in Figure 6, effectively breaks the internal voltage feedback connection. The current flowing into Pin 8 is now independent of the voltage on Pin 8. The output voltage (on Pin 7) can now be amplified or filtered and used to drive the current source by a scheme such as that shown in Figure 6. This scheme allows the addition of enough gain for the loop to stay in lock over a 100:1 frequency range or, conversely, to stay in lock with a precise phase difference (between input and VCO signals) which is almost independent of frequency variation. Adjustment of the voltage to the non-inverting input of the op amp, together with a large enough loop gain allows the phase difference to be set at a constant value between 0° and 180°. In addition, it is now possible to do special filtering to improve the performance in certain applications. For in-

stance, in frequency multiplication applications, it may be desirable to include a notch filter tuned to the sum frequency component to minimize incidental FM without excessive reduction of capture range.

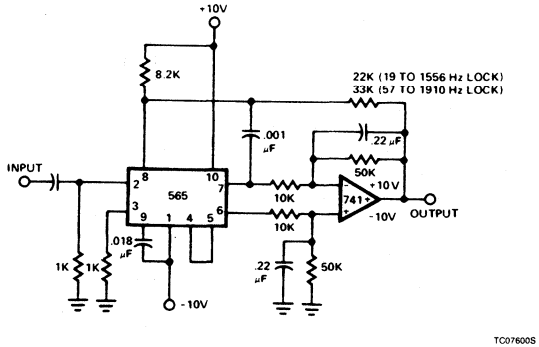


Figure 5. Expanded Lock Range Configuration for the 565

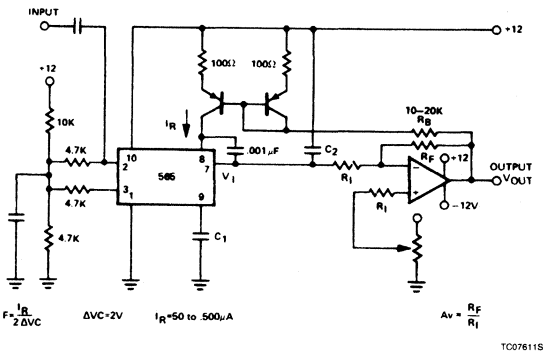


Figure 6. Increased Loop Gain and Lock Range for the 565

AN184
Typical Applications with NE565

Application Note

FSK DEMODULATION

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

FSK Demodulation with the 565

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 1. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding DC shift at the output (Pin 7).

The loop filter capacitor C_2 is chosen to set the proper overshoot on the output and a three-stage RC ladder filter is used to remove the sum frequency components. The band edge of the ladder filter is chosen to be approximately half-way between the maximum keying rate (300 baud or bits per second, or 150Hz). The free-running frequency should be adjusted (with R_1) so that the DC voltage level at the output is the same as that at Pin 6 of the loop. The output signal can now be made logic compatible by connecting a voltage comparator between the output and Pin 6.

The input connection is typical for cases where a DC voltage is present at the source and, therefore, a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to achieve a 600Ω input impedance).

A more sophisticated approach primarily useful for narrow frequency deviations is shown in Figure 2. Here, a constant current is injected into Pin 8 by means of transistor Q_1. This has the effect of decreasing the lock range and increasing the output voltage sensitivity to the input frequency shift. The basis for this scheme is the fact that the output voltage (control voltage for the VCO) controls only the current through R_1, while the current through Q_1 remains constant. Thus, if most of the capacitor charging current is due to Q_1, the current variation due to R_1 will be a small percentage of the total charging current and, consequently, the total frequency deviation of the VCO will be limited to a small percentage of the center frequency. A 0.25μF loop filter capacitor gives approximately 30% overshoot on the output pulse, as seen in the accompanying photographs. Figure 3 shows the output of the μA710 comparator and the output of the 565 phase-locked loop.

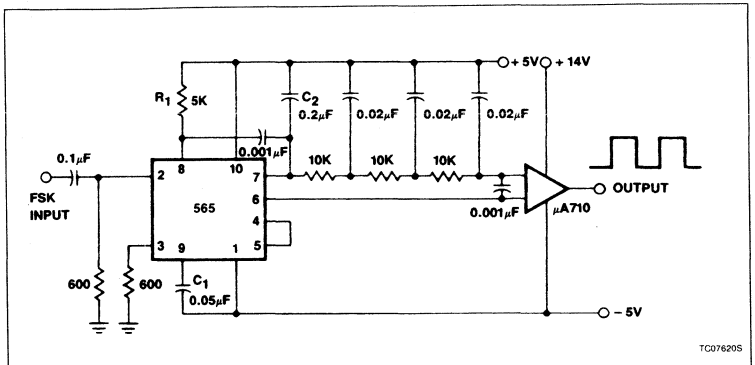


Figure 1. FSK Decoder Using the 565

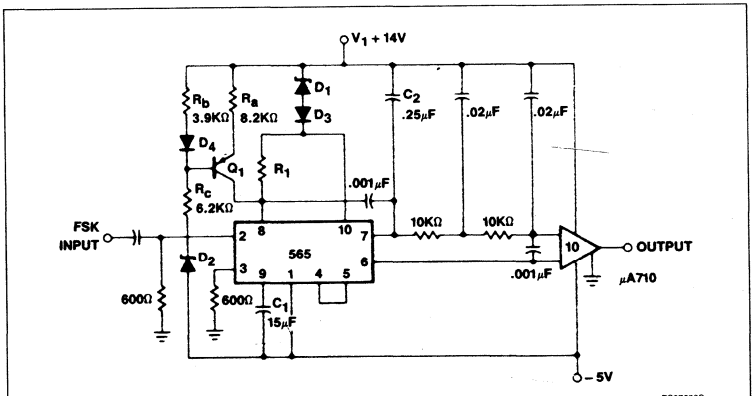
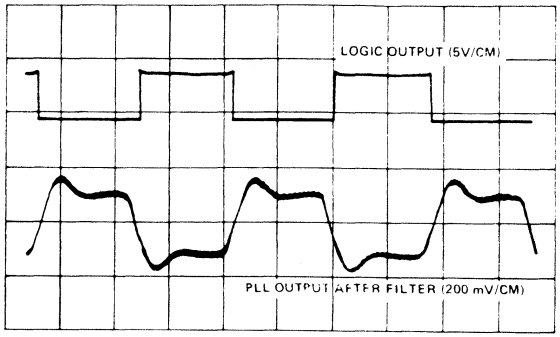
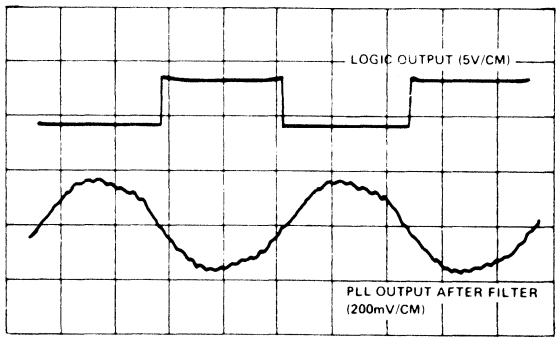


Figure 2. FSK Decoder With Expanded 565 Output Voltage Range



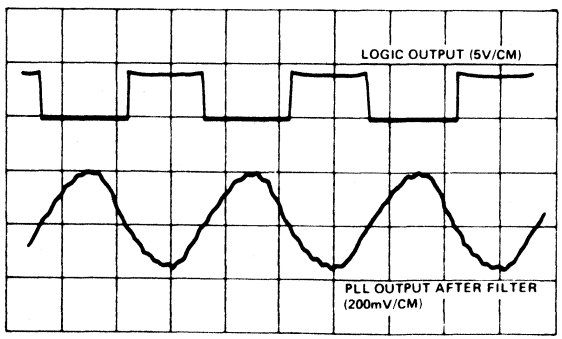
OP06490S

a. 100 Baud



OP06500S

b. 200 Baud



OP06510S

c. 300 Baud

Figure 3

Typical Applications with NE565

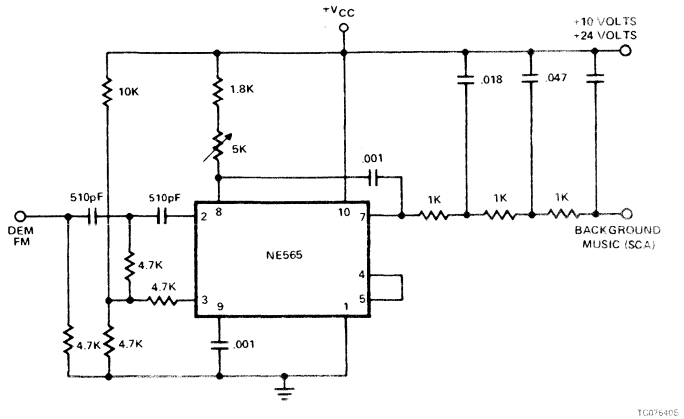


Figure 4. SCA Decoder

SCA Demodulator Using the 565

This application involves demodulation of a frequency-modulated subcarrier of the main channel. A popular example here is the use of the PLL to recover the SCA (Subsidiary Carrier Authorization or storecast music) signal from the combined signal of many commercial FM broadcast stations. The SCA signal is a 67kHz frequency-modulated subcarrier which puts it above the frequency spectrum of the normal stereo or monaural FM program material. By connecting the circuit of Figure 4 to a point between the FM discriminator and the de-emphasis filter of a commercial band (home) FM receiver and tuning the receiver to a station which broadcasts an SCA signal, one can obtain hours of commercial-free background music.

AN185
Circuit Description of the NE566

Application Note

CIRCUIT DESCRIPTION OF THE 566 PLL

The 566 is the voltage-controlled oscillator portion of the 565. The basic die is the same as that of the 565; modified metalization is used to bring out only the VCO. The 566 circuit diagram is shown in Figure 1. Transistor Q_{18} provides a buffered triangle waveform output. (The triangle waveform is available at capacitor C_1 also, but any current drawn from Pin 7 will alter the duty cycle and frequency.) The square wave output is available from Q_{19} by Pin 4. The circuit will operate at frequencies up to 1MHz and may be programmed by the voltage applied on the control terminal (Pin 5), by injecting current into Pin 6, or by changing the value of the external resistor and capacitor (R_1 and C_1).

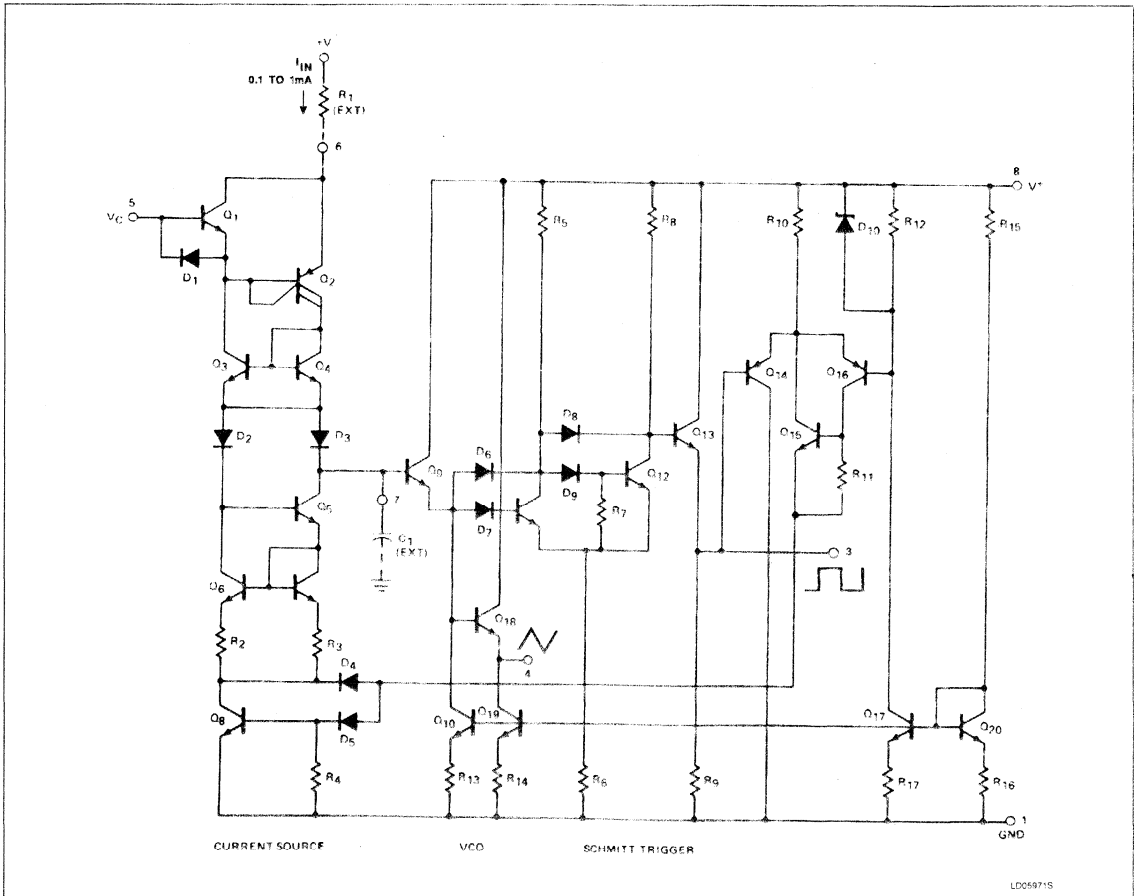


Figure 1. Circuit Diagram of the NE566

AN186
Waveform Generators With the NE566

Application Note

WAVEFORM GENERATORS

The oscillator portion of many of the PLLs can be used as a precision, voltage-controllable waveform generator. Specifically, the 566 Function Generator contains the oscillator of the 565 PLL. Most of the applications which follow are designs using the 566. Many of these designs can be modified slightly to utilize the oscillator section of the 564 if higher frequency performance is desired.

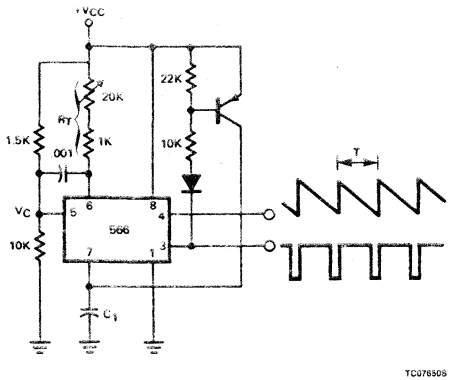
Ramp Generators

Figure 1 shows how the 566 can be wired as a positive or negative ramp generator. In the positive ramp generator, the external transistor driven by the Pin 3 output rapidly discharges C_1 at the end of the charging period so that charging can resume instantaneously. The PNP transistor of the negative ramp generator likewise rapidly charges the timing capacitor C_1 at the end of the discharge period. Because the circuits are reset so quickly, the temperature stability of the ramp generator is excellent. The period

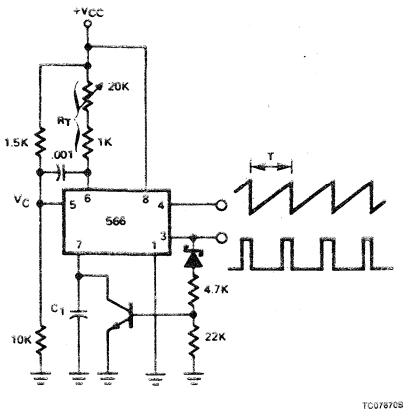
$$T \text{ is } \frac{1}{2f_O}$$

where f_O is the 566 free-running frequency in normal operation. Therefore,

$$T = \frac{1}{2f_O} = \frac{R_1C_1V_{CC}}{5(V_{CC} - V_C)} \quad (1)$$

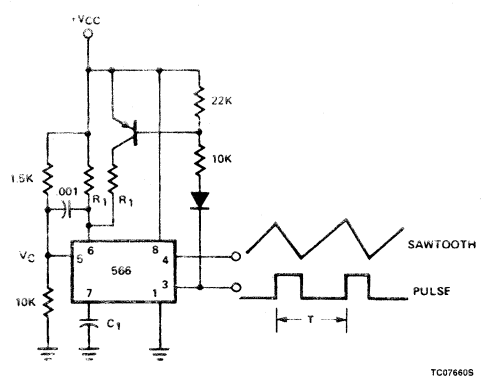


a. Negative Ramp

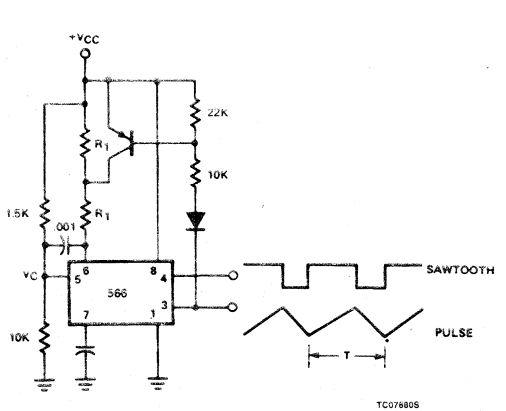


b. Positive Ramp

Figure 1. Ramp Generators



a. Positive Sawtooth



b. Negative Sawtooth

Figure 2. Sawtooth and Pulse Generators

where V_C is the bias voltage at Pin 5 and R_T is the total resistance between Pin 6 and V_{CC}. Note that a short pulse is available at Pin 3. (Placing collector resistance in series with the external transistor collector will lengthen the pulse.)

Sawtooth and Pulse Generator

Figure 2 shows how the Pin 3 output of the 566 can be used to provide different charge and discharge currents for C_1 so that a sawtooth output is available at Pin 4 and a pulse at Pin 3. The PNP transistor should be well saturated to preserve good temperature stability. The charge and discharge times may be estimated by using the formula

$$T = \frac{R_T C_1 V_{CC}}{5(V_{CC} - V_C)} \quad (2)$$

where R_T is the combined resistance between Pin 6 and V_{CC} for the interval considered.

Triangle-to-Sine Converters

Conversion of triangle wave shapes to sinusoids is usually accomplished by diode-resistor shaping networks, which accurately reconstruct the sine wave segment by segment. Two simpler and less costly methods may be used to shape the triangle waveform of the 566 into a sinusoid with less than 2% distortion.

In Figure 3, the non-linear $I_{DS} \cdot V_{DS}$ transfer characteristic of a P-channel junction FET is used to shape the triangle waveform.

The amplitude of the triangle waveform is critical and must be carefully adjusted to achieve a low distortion sinusoidal output. Naturally, where additional waveform accuracy is needed, the diode-resistor shaping scheme can be applied to the 566 with excellent results since it has very good output amplitude stability when operated from a regulated supply.

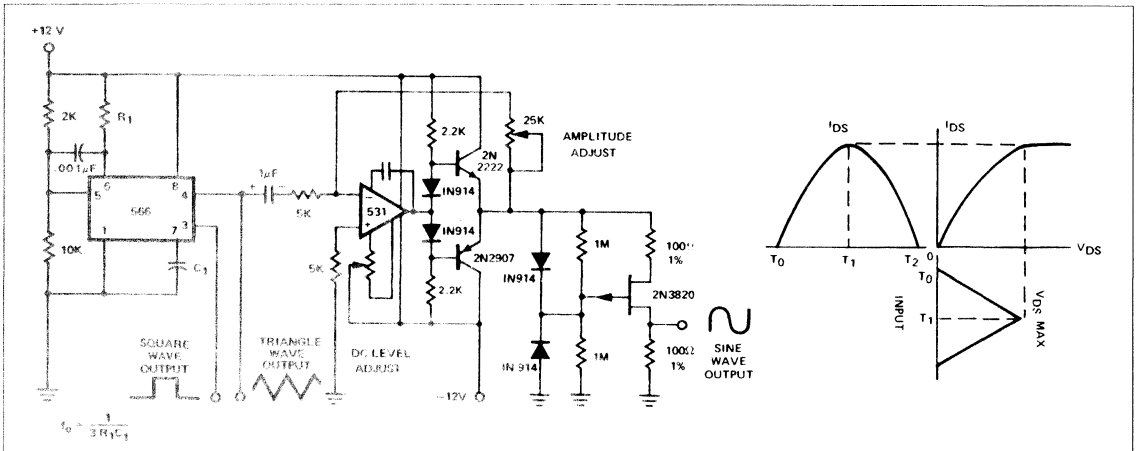


Figure 3. Triangle-to-Sine Converters

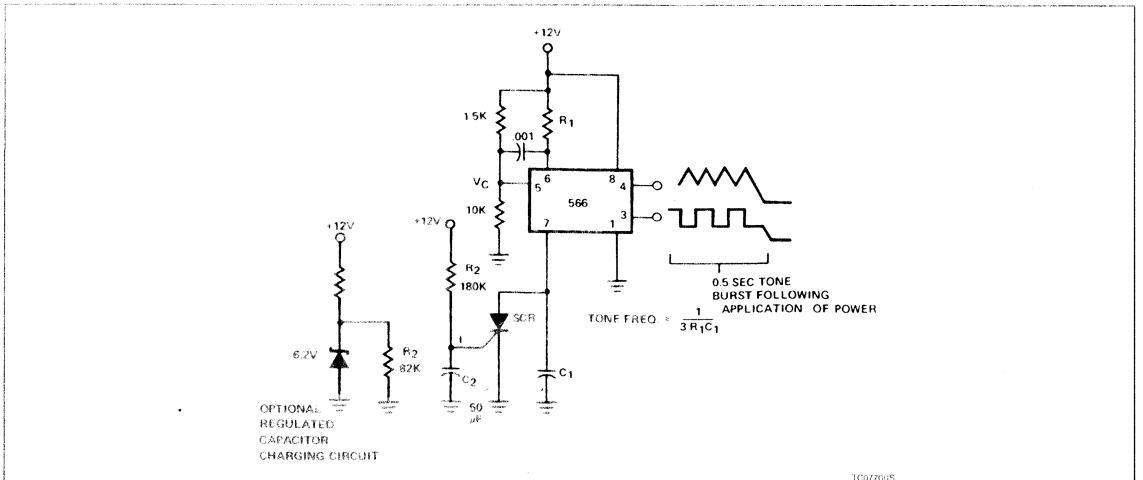
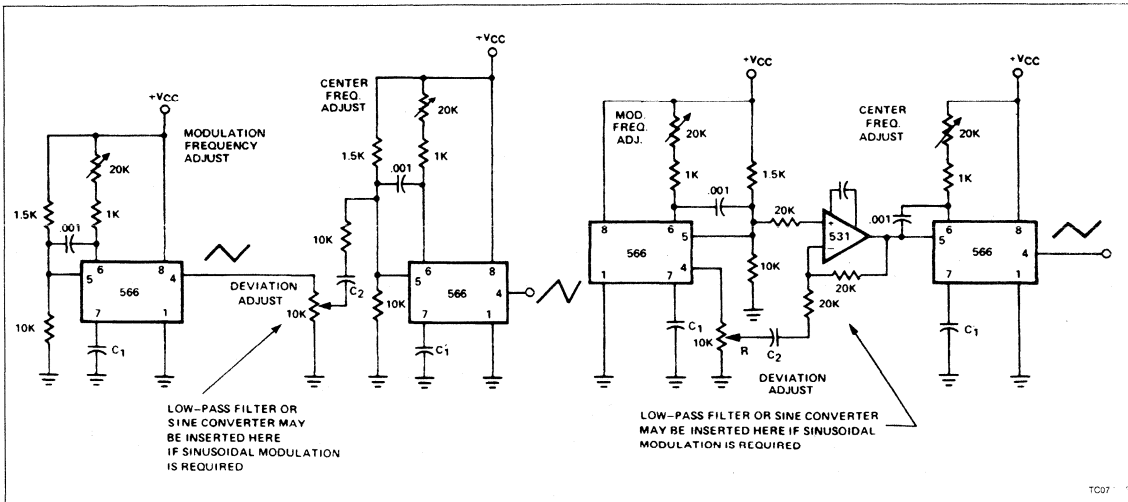


Figure 4. Single-Burst Tone Generator



a. Small Frequency Deviations to ±20% **b. Large Frequency Deviations to ±100%**

Figure 5. Frequency-Modulated Generators

Single-Tone Burst Generator

Figure 4 is a tone burst generator which supplies a tone for one-half second after the power supply is activated; its intended use is a communications network alert signal. Cessation of the tone is accomplished at the SCR, which shunts the timing capacitor C_1 charge current when activated. The SCR is gated on when C_2 charges up to the gate voltage which occurs in 0.5 seconds. Since only 70μA are available for triggering, the SC must be sensitive enough to trigger at this level. The triggering current can be increased, of course, by reducing R_2 (and increasing C_2 to keep the same time constant). If the tone duration must be constant under widely varying supply voltage conditions, the optional Zener diode regulator circuit can be added, along with the new value for R_2, $R_2' = 82k\Omega$.

If the SCR is replaced by an NPN transistor, the tone can be switched on and off at will at the transistor base terminal.

Low Frequency FM Generators

Figure 5 shows FM generators for low frequency (less than 0.5MHz center frequency) applications. Each uses a 566 function generator as a modulation generator and a second 566 as the carrier generator.

Capacitor C_1 selects the modulation frequency adjustment range and C_1' selects the center frequency. Capacitor C_2 is a coupling capacitor which only needs to be large enough to avoid distorting the modulating waveform.

If a frequency sweep in only one direction is required, the 566 ramp generators given in this section may be used to drive the carrier generator.

AN187
Circuit Description of the NE567 Tone Decoder

Application Note

CIRCUIT DESCRIPTION OF THE NE567 TONE DECODER

The NE567 is a PLL designed specifically for frequency sensing or tone decoding. The NE567 has a controlled oscillator, a phase comparator and a second auxiliary or quadrature-phase detector. In addition, however, it contains a power output stage which is driven directly by the quadrature-phase detector output. During lock, the quadrature-phase detector drives the output stage on, so the device functions as a tone decoder or frequency relay. The tone decoder free-running frequency and bandwidth are specified by the free-running frequency and capture range of the loop portion. Since a tone decoder, by definition, responds to a stable frequency, the lock or tracking range is relatively unimportant except as it limits the maximum attainable capture range. The complete circuit diagram of the NE567 is shown in Figure 1.

The current-controlled oscillator is shown in simplified form in Figure 2. It provides both a square wave output and a quadrature output. The control current I_C sweeps the oscillator ±7% of the free-running frequency, which is set by external components R_1 and C_1.

Transistors Q_1 through Q_6 form a flip-flop which can switch Pin 5 between V_{BE} and $+V - V_{BE}$. Thus, the R_1C_1 network is driven from a square wave of $+V - 2V_{BE}$ peak-to-peak volts. On the positive portion of the square wave, C_1 is charged through R_1 until V_1 is reached. A comparator circuit driven from C_1 at Pin 6 then supplies a pulse which resets the flip-flop so that Pin 5 switches to V_{BE} and C_1 is discharged until V_2 is reached. A second comparator then supplies a pulse which sets the flip-flop, and C_1 resumes charging.

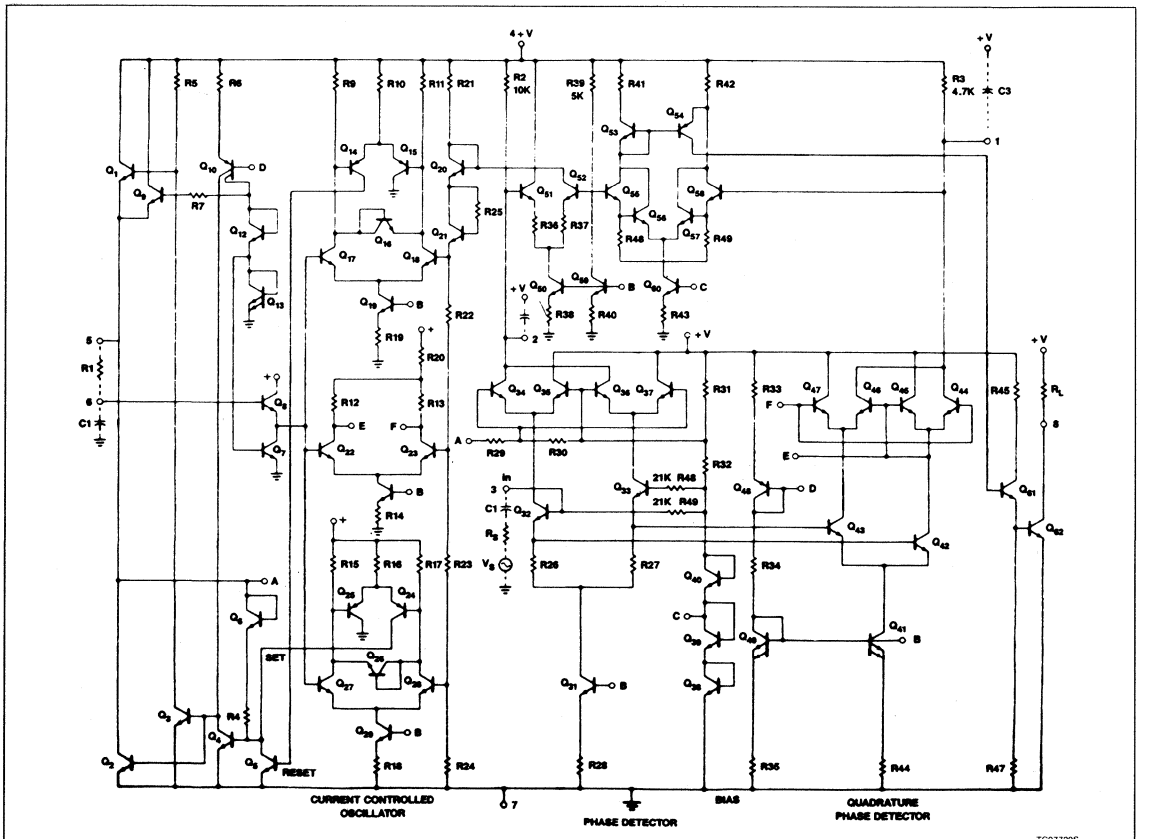


Figure 1. Circuit Diagram of NE567

Circuit Description of the NE567 Tone Decoder

AN187

The total swing of the capacitor voltage, as determined by the comparator sensing voltages, is

$$V_1 - V_2 = (+V - 2V_{BE})\left[\frac{R_{22} + R_{23}}{R_{21} + R_{22} + R_{23} + R_{24}}\right]$$

$$= K(+V - 2V_{BE}) \quad (1)$$

Due to the excellent matching of integrated resistors, the resistor ratio K may be considered constant. Figure 3 shows the Pin 5 and Pin 6 voltages during operation. It is obvious from the proportion that $t_1 + t_2$ is independent of the magnitude of +V and dependent only on the time constant R_1C_1 of the external components. Moreover, if $(V_1 + V_2)/2 = +V/2$, then $t_1 = t_2$ and the duty cycle is 50%. Note that the triangular waveform is phase-shifted from the square wave.

A differential stage (Q_{22} and Q_{23}) amplifies the triangular wave with respect to $(V_1 + V_2)/2$ to provide the quadrature output. (Due to the exponential distortion of the triangle wave, the quadrature output is actually phase-shifted about 80°, but no operating compromises result from this slight deviation from true quadrature.)

One source of error in this oscillator scheme is current drawn by the comparators from the R_1C_1 mode. An emitter-follower, therefore, is inserted at X to minimize this drain and Q_{21} placed in series with Q_{20} to drop the comparator sensing voltage one V_{BE} to compensate for the V_{BE} drop in the emitter-follower.

In order to insure that the square wave drops quickly and accurately to V_{BE}, an active clamp scheme is applied to the collector of Q_2. The base of Q_9 is held at $2V_{BE}$ so that as Q_2 is turned on its base current, its collector

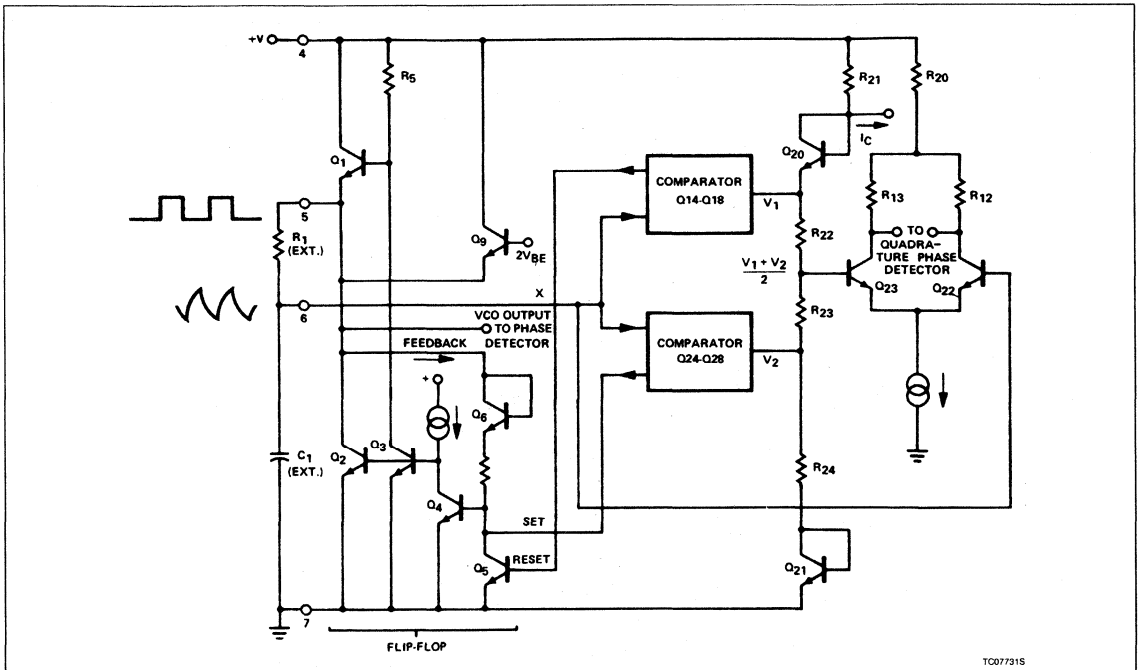


Figure 2. Simplified Diagram of NE567 Tone Decoder Current-Controlled Oscillator

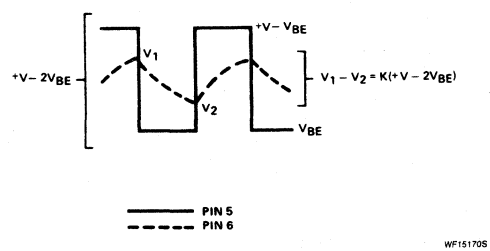


Figure 3. Current-Controlled Oscillator Waveshapes in the NE567

Circuit Description of the NE567 Tone Decoder

is held at V_{BE}. Because Q_2 and Q_3 have the same geometry and their base-emitter voltages are the same, the maximum Q_2 current, when clamped, is essentially the same as the collector current of Q_3 (as limited by R_5). The flip-flop was optimized for maximum switching speed to reduce frequency drift due to switching speed variations.

Current control of the frequency is achieved by making R_{21} somewhat less than R_{24} and restoring the proper voltage for 50% duty cycle by drawing I_C of 100μA for the R_{21}, Q_{20} junction. When I_C is then varied between 0 and 200μA, the frequency changes by ±7%. Because of the slight shift in the voltage levels V_1 and V_2 with I_C, the square wave duty cycle changes from about 47% to about 53% over the control range. To avoid drift of free-running frequency with temperature and supply voltage changes when $I_C \neq 0$, I_C is also made a function of $+V - 2V_{BE}$.

A doubly balanced multiplier formed by Q_{32} through Q_{37} (Figure 1) functions as the phase comparator. The input signal is applied to the base of Q_{32}. Transistors $Q_{34} - Q_{37}$ are driven by a square wave taken from the CCO at the collector of Q_2. Phase comparator input bias is provided by three diodes, Q_{38} through Q_{40}, connected in series, assuring good bias voltage matching from run to run. Emitter resistors R_{26} and R_{27}, in addition to providing the necessary dynamic range at the input, help stabilize the gain over the wide temperature range.

The loop DC amplifier is formed by Q_{51} and Q_{52}. Having a current gain of 8, it permits even a small phase detector output to drive the CCO the full ±7%. Therefore, full detection bandwidth can be obtained for any in-band input signal greater than about 70mV_{RMS}. However, the main purpose of high loop gain in the tone decoder is to keep the locked phase as close to $\pi/2$ as possible for all but the smallest input levels, since this greatly facilitates operation of the quadrature lock detector. Emitter-resistors R_{36} and R_{37} help stabilize the gain over the required temperature range. Another function of the DC amplifier is to allow a higher impedance level at the low pass filter terminal (Pin 2) so that a smaller capacitor can be used for a given loop cutoff frequency. Once again, emitter-resistors help stabilize the loop gain over the temperature range.

The quadrature-phase detector (QPD), formed by a second doubly-balanced multiplier $Q_{42} - Q_{47}$ is driven from the quadrature output (E, F, in Figure 1) of the CCO. The signal input comes from the emitters of the input transistors Q_{32} and Q_{33}.

The output stage, Q_{53} through Q_{62}, compares the average QPD current in the low pass output filter R_3C_3 with a temperature-compensated current in R_{39} (forming the threshold voltage V_t).

Since R_3 is slightly lower in value than R_{39}, the output stage is normally off. When the lock and the QPD current I_q occurs, Pin 1 voltage drops below the threshold voltage V_t and the output stage is energized.

The uncommitted collector (Pin 8) of the power NPN output transistor can drive both 100 - 200mA loads and logic elements, including TTL.

The K_o conversion gain for the NE567 tone decoder is given by

$$K_o = 0.44\omega_O' \left(\frac{\text{radians}}{\text{volt-sec}} \right) \qquad (2)$$

while the K_d conversion gain depends upon the input signal level as shown in Figure 4. These parameters can be used to calculate the lock and capture range as has been illustrated previously.

The NE567 tone decoder is a specialized loop which can be setup to respond to a given tone (constant frequency) within its bandwidth. The free-running frequency is set by a resistor R_1 and capacitor C_1. The bandwidth is controlled by the low-pass filter capacitor C_2. A third capacitor C_3 integrates the output of the quadrature-phase detector (QPD) so that the DC lock-indicating component can switch the power output stage on when lock is present. The NE567 is optimized for stability and predictability of free-running frequency and bandwidth.

Two events must occur before an output is given. First, the loop portion of the NE567 must achieve lock. Second, the output capacitor C_3 must charge sufficiently to activate the output stage. For minimum response time, these events must be as brief as possible.

As previously discussed, the lock time of a loop can be minimized by reducing the response time of the low-pass filter. Thus, C_2 must be as small as possible. However, C_2 also controls the bandwidth. Therefore, the response time is an inverse function of bandwidth as shown by Figure 5, reprinted from the NE567 data sheet. The upper curve denotes the expected worst-case response time when the bandwidth is controlled solely by C_2 and the input amplitude is 200mV_{RMS} or greater. The response time is given in cycles of free-running frequency. For example, a 2% bandwidth at a free-running frequency of 1000 cycles can require as long as 280 cycles (280ms) to lock when the initial phase relationship is at its worst. Figure 6 gives a typical distribution of response time versus input phase. Note that, assuming random initial input phase, only $^{30}/_{180} = 1/6$ of the time will the lock-up time be longer than half the worst-case lock-up time. Figure 7 shows some actual measurements of lock-up time for a setup having a worst-case lock-up time of 27 cycles and a best-case lock-up time of four input cycles.

The lower curve on the graph of Figure 5 shows the worst-case lock-up time when the loop gain is reduced as a means of reducing the bandwidth (see data sheet, Alternate Method of Bandwidth Reduction). The value of C_2 required for this minimum response time is

$$C_{2(min)} = \frac{130}{f_O'} \left[\frac{10k + R_A}{R_A} \right] \mu F \qquad (3)$$

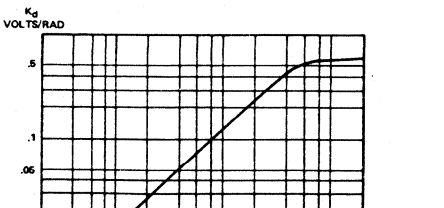


Figure 4. Phase Comparator Conversion Gain, K_d, for the NE567 Tone Decoder

Circuit Description of the NE567 Tone Decoder

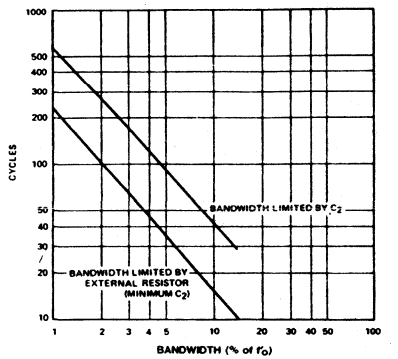


Figure 5. Greatest Number of Cycles Before Output for the NE567 Tone Decoder

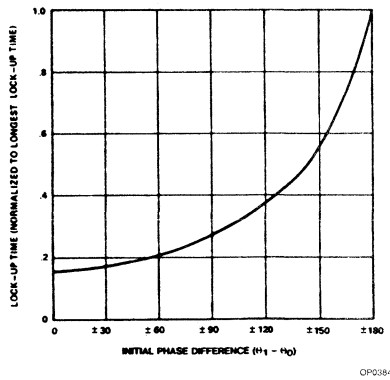


Figure 6. Lock-Up Time vs Initial Phase for the NE567 Tone Decoder

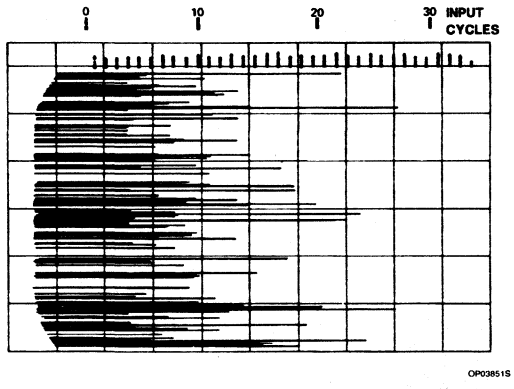


Figure 7. Lock-Up Time Variation Due to Random Initial Phase for the NE567 Tone Decoder

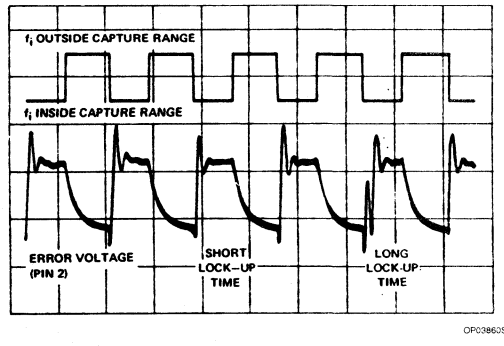


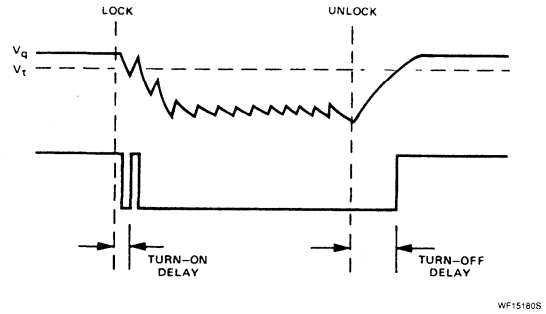
Figure 8. Lock-Up Transient Response for NE567 Tone Decoder

It is important to note that noise immunity and rejection of out-band tones suffer somewhat when this minimum value of C_2 is used so that response time is gained at their expense. Except at very low input levels, input amplitude has only a minor effect on the lock-up time — usually negligible in comparison to the variation caused by input phase.

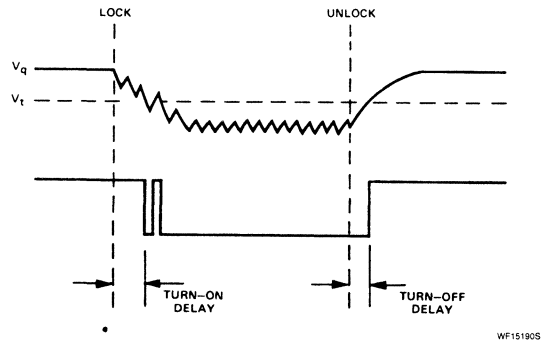
Lock-up transients can be displayed on a two-channel scope with case. Figure 8 shows the display which results. The top trace shows the square wave which either gates the input generator signal off and on (or shifts the frequency in and out of the band if you have a generator which has a frequency control input only). The lower trace shows the voltage at Pin 2, the low-pass filter voltage. The input frequency is offset slightly from the free-running frequency so that the locked and unlocked voltages are different. It is apparent that, while the C_2 decay during unlock is always the same, the lock transient is different each time.

This is because the turn-on repetition rate is such that a different initial phase relationship occurs with each appearance of the in-band signal. It is tempting to adjust the repetition rate so that a fast, constant lock-up transient is displayed. However, in doing so, a favorable initial phase is created that is not present in actual operation. On the contrary, it is most realistic to adjust the repetition rate so that the longest lock-up time is displayed, such as the fifth lock transient shows. Once this display is achieved, the effect of various adjustments in C_2 or input amplitude is seen. However, the *repetition rate must be readjusted for worst-case lock-up after each such change.*

Once lock is achieved, the quadrature-phase detector output at Pin 1 is integrated by C_3 to extract the DC component. As C_3 charges from its quiescent value V_q (see Figure 9) to its final value ($V_q \cdot \Delta V$), it passes through the output stage threshold, turning it on. The total voltage change is a function of input amplitude. Since the unadjusted V_q is very close (within 50mV) to V_t, the output stage turns on very soon after lock. Only a small fraction of the output stage time constant ($\tau = 4700C_3$) expires before V_t is crossed so that C_3 does not greatly influence the response time. However, as shown in Figure 9a, the turn-off delay time can be quite long when C_3 is large. Figure 9b shows how desensitizing the output stage by connecting a high-value resistor between Pin 1 and Pin 4 (positive supply voltage) can equalize the turn-on and turn-off time. If turn-off delay is important in the



a. V_q Slightly Greater Than V_t



b. V_q Much Greater Than V_t

Figure 9. Effect of Threshold Voltage Adjustment on Tone Decoder Turn-On and Turn-Off Delay

overall response time, then desensitizing can reduce the total delay.

But why not make C_3 very small so that these delays can be totally neglected? The problem here is that the QPD output has a large second harmonic component of the free-running frequency that must be filtered out. Also, noise, out-band signals, and difference frequencies formed by close out-band frequencies beating with the VCO frequency appear at the QPD output. All these must be attenuated by C_3 or the output stage will chatter on and off as the threshold is approached. The more noisy the input signal and the larger the near-band signals, the greater C_3 must be to reject them. Thus, there is a complicated relationship between the input spectrum and the size of C_3. What must be done, then, is to make C_3 more than sufficient for proper operation (no false outputs or missed signals) under actual operating conditions and then reduce its value in small steps until either the required response time is obtained or operation becomes unsatisfactory.

In setting up the tone decoder for maximum speed, it is best to proceed as follows:

a. After the center frequency has been set, adjust C_2 to give the desired bandwidth or, if the graph of response time in cycles (Figure 7) suggests that worst-case lock-up time will be too long, incorporate the loop gain reduction scheme as an alternate means of bandwidth reduction (see data sheet).

b. Check lock-up time by observing the waveform at Pin 2 while pulsing the input signal on and off (or in and out of the band when a FM generator is used). Adjust repetition rate to reveal worst lock-up time.

c. Starting with a large value of C_3 (say 10 C_2), reduce it as much as possible in steps while monitoring the output to be certain that no false outputs or missed signals occur. The full input spectrum should be used for this test. Ignore brief transients or chatter during turn-on and turn-off as they can be eliminated with the chatter prevention feedback technique described in the data sheet.

d. Use the desensitizing technique, also described in the data sheet, to balance turn-on and turn-off delay.

e. Apply the chatter prevention technique to clean up the output.

If this procedure results in a worst-case response time that is too slow, the following suggestions may be considered:

a. Relax the bandwidth requirement.

b. Operate the entire system at higher frequency when this option is available.

c. Use two tone decoders operating at slightly different frequencies and OR the outputs. This will reduce the statistical occurrence of the worst-case lock-up time so that excessive lock-up time occurs. For example, if the lock-up time is marginal 10% of the time with one unit, it will drop to 1% with two units.

d. Control the in-band input amplitude to stabilize the bandwidth, set up two tone decoders for maximum bandwidth, and overlap the detection bands to make the desired frequency range equal to the overlap. Since both tone decoders are on only when a tone appears within the overlap range, the outputs can be ANDed to provide the desired selectivity.

e. If the system design permits, send the tone to be detected continuously at a low level (say 25mV$_{RMS}$) to keep the loop in lock at all times. The output stage, slightly desensitized, can then be gated on as required by increasing the signal amplitude during the on time. Naturally, the signal phase should be maintained as the amplitude is changed. This scheme is extremely fast, allowing repetition rates as fast as ⅓ to ½ the free-running frequency when C_3 is small. This is equivalent to ASK (amplitude shift keying).

AN188
Selected Circuits Using the NE567

Application Note

Touch-Tone® Decoder

Touch-Tone® decoding is of great interest since all sorts of remote control applications are possible if you make use of the encoder (the pushbutton dial) that will ultimately be part of every phone. A low cost decoder can be made as shown in Figure 1. Seven 567 tone decoders, their inputs connected in common to a phone line or acoustical coupler, drive three integrated NOR gate packages. Each tone decoder is tuned, by means of R_1 and C_1, to one of the seven tones. The R_2 resistor reduces the bandwidth to about 8% at 100mV and 5% at 50mV$_{RMS}$. Capacitor C_4 decouples the seven units. The seven R_2 resistors and capacitor C_4 can be eliminated at the expense of a somewhat slower response at low input voltages (50 to 100mV$_{RMS}$). The bandwidth can be controlled in the normal manner by selecting C_2 to be 4.7μF for the three lower frequencies and 2.2μF for the four higher frequencies.

The only unusual feature of this circuit is the means of bandwidth reduction using the R_2 resistors. An external resistor R_A can be used to reduce the loop gain and, therefore, the bandwidth. Resistor R_2 serves the same function as R_A except that instead of going to a voltage divider for DC bias, it goes to a common point with the six other R_2 resistors. In effect, the five 567s which are not being activated during the decoding process serve as bias voltage sources for the R_2 resistors of the two NE567s which are being activated. Capacitor C_4 decouples the AC currents at the common point.

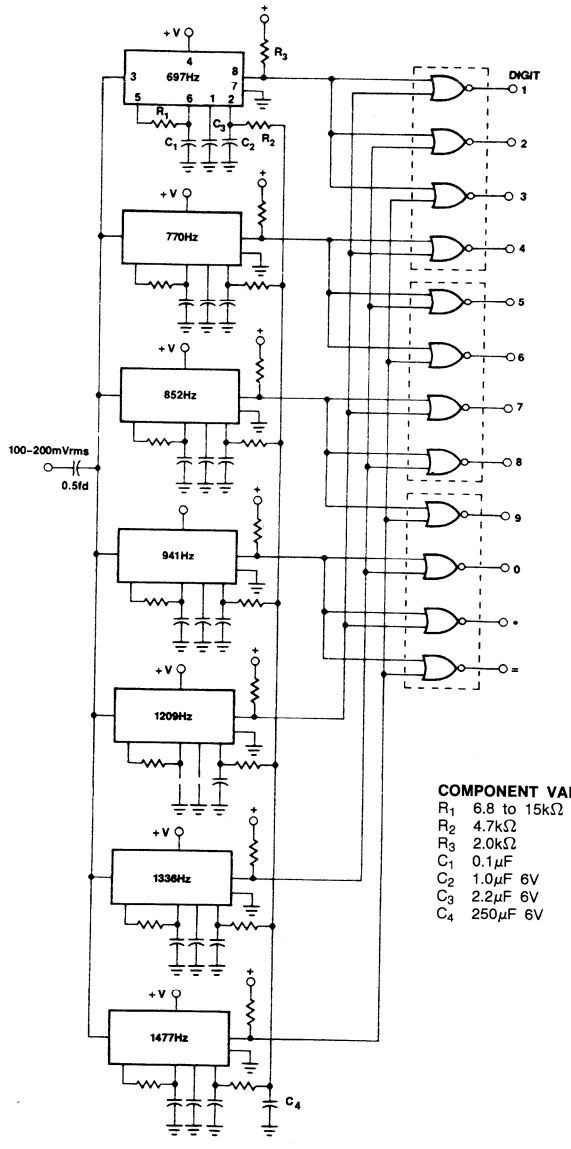
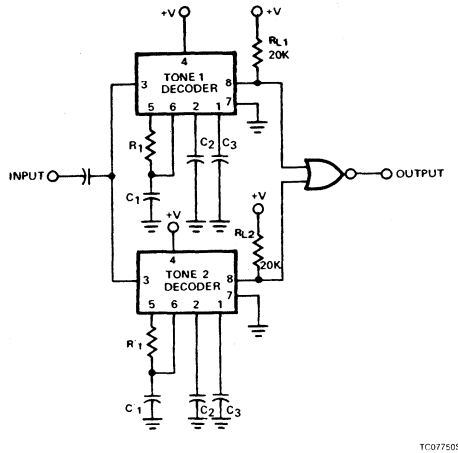


Figure 1. Low Cost Touch-Tone® Decoder

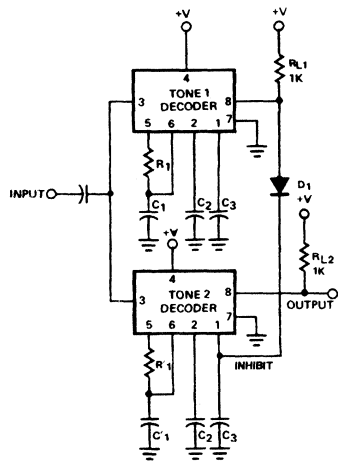
TONE DECODER APPLICATIONS (NE567)

The NE567 is a special purpose PLL intended solely for use as a tone decoder. It contains a complete PLL including VCO, phase comparator, and amplifier as well as a quadrature-phase detector of multiplier. If the signal amplitude at the lock frequency is above a minimal value, the driver amplifier turns on, driving a load with as much as 200mA. Thus the 567 gives an output whenever an in-band tone is present. The 567 is optimized for both free-running frequency and bandwidth stability.

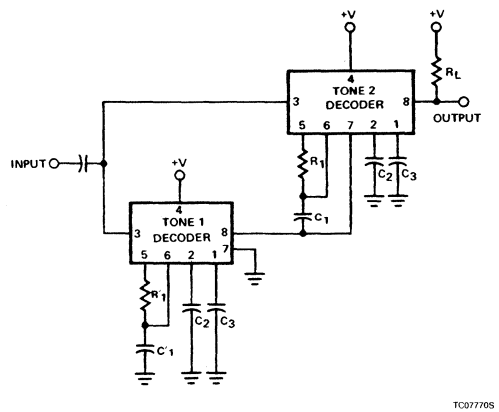
®Touch-Tone is a registered trademark of Bell Laboratories.



a. NORing Outputs Together



b. Disabling the Second Decoder Until Enabled by the First



c. Blocking Power to the Second Decoder (Pin 7) Until the First is Enabled

Figure 2. Detection of Two Simultaneous or Sequential Tones

Dual-Tone Decoder

Two 567 tone decoders connected as shown in Figure 2a permit decoding of simultaneous or sequential tones. Both units must be on before an output is given. R_1 C_1 and R_1' C_1' are chosen respectively for tones 1 and 2. If sequential tones (tone 1 followed by tone 2) are to be decoded, then C_3 is made very large to delay turn off of unit 1 until unit 2 has turned on and the NOR gate is activated. Note that the wrong sequence (tone 2 followed by tone 1) will not provide an output since unit 2 will turn off before unit 1 comes on. Figure 2b shows a circuit variation which eliminates the NOR gate. The output is taken from unit 2, but the unit 2 output stage is biased off by R_{L1} and D_1 until activated by tone 1. A further variation is given in Figure 2c. Here, unit 2 is turned on by the unit 1 output when tone 1 appears, reducing the standby power to half. Thus, when unit 2 is on, tone 1 is or was present. If tone 2 is now present, unit 2 comes on also and an output is given. Since a transient output pulse may appear during unit 1 turn on, even if tone 2 is not present, the load must be slow in response to avoid a false output due to tone 1 alone.

High-Speed, Narrow-Band Tone Decoder

The circuit of Figure 2a may be used to obtain a fast, narrow-band tone decoder. The detection bandwidth is achieved by overlapping the detection bands of the two tone decoders. Thus, only a tone within the overlap portion will result in an output. The input amplitude should be greater than $70mV_{RMS}$ at all times to prevent detection band shrinkage and C_2 should be between $130/f_O$ and $1300/f_O\mu F$ where f_O is the nominal detection frequency. The small value of C_2 allows operation at the maximum speed so that worst-case output delay is only about 14 cycles.

Low-Cost Frequency Indicator

Figure 3 shows how two tone decoders set up with overlapping detection bands can be used for a go/no-go frequency meter. Unit 1 is set 6% above the desired sensing frequency and unit 2 is at 6% below the desired frequency. Now, if the incoming frequency is within 13% of the desired frequency, either unit 1 or unit 2 will give an output. If both units are on, it means that the incoming frequency is within 1% of the desired frequency. Three light bulbs and a transistor allow low cost read-out.

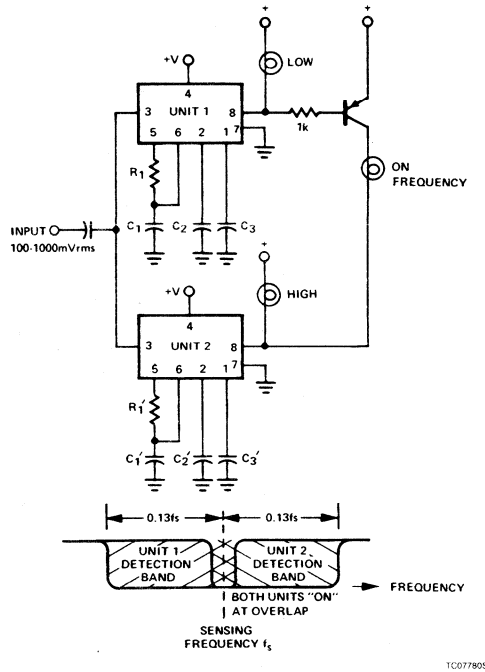
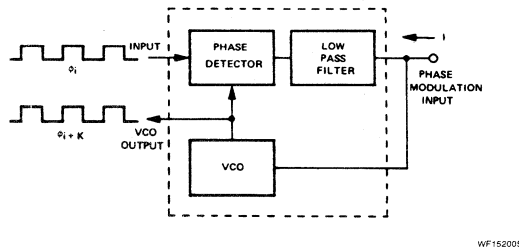


Figure 3. Low Cost Frequency Detector With Lamp Readout

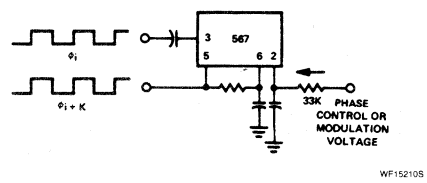
Phase Modulator

If a phase-locked loop is locked onto a signal at the free-running frequency, the phase of the VCO will be 90° with respect to the input signal. If a current is injected into the VCO terminal (the low-pass filter output), the phase will shift sufficiently to develop an opposing average current out of the phase comparator so that the VCO voltage is constant and lock is maintained. When the input signal amplitude is low enough so that the loop frequency swing is limited by the phase comparator output rather than the VCO swing, the phase can be modulated over the full range of 0 to 180°. If the input signal is a square wave, the phase will be a linear function of the injected current.

A block diagram of the phase modulator is given in Figure 4a. The conversion factor K is a function of which loop is used, as well as the input square wave amplitude. Figure 4b shows an implementation of this circuit using the 567.



a. Block Diagram



b. Circuit Implementation With the NE567

Figure 4. Phase Modulation Using the PLL

AN1801
10.8MHz FSK Decoder With NE564

Application Note

FSK DEMODULATION WITH THE 564

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5V power supply. Demodulated DC voltages associated with the mark and space frequencies are recovered with a single external capacitor in a DC retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 1 shows a high-frequency FSK decoder designed for input frequency deviations of ±1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from Figure 4a to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' to 10.8MHz.

Figure 2b indicates that the ±1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero Pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_O' frequencies.

A more thorough analysis confirms these lock range conclusions and serves as a guide for designing other systems. The closed-loop gain of the PLL is equal to the system's lock range and is found as the product of K_d and K_o adjusted to 10.8MHz

$$2\omega_L = K_V = K_d K_o \qquad (1)$$

$$2\omega_L = \left(0.46 \frac{\text{volt}}{\text{radian}}\right)\left(0.875 \frac{\text{MHz}}{\text{volt}}\right) \times \left(2\pi \times 10.8 \times 10^6 \frac{\text{radian}}{\text{sec}}\right)$$

$$2\omega_L = 2.73 \times 10^7 \frac{\text{radian}}{\text{sec}} \quad \text{(Lock range total)}$$

Thus Pin 2 could be left as an open circuit and the internally set closed-loop gain would be adequate for tracking the mark and space input frequencies. However, to be safe, a bias adjustment as shown in Figure 1 is recommended to allow for K_d and K_o variations from device to device.

Designing for a capture range of approximately 700kHz gives a low-pass filter time constant of

$$\omega_c \cong \sqrt{\frac{\omega L}{\tau}} \quad 2\omega_L = K_V = 2.73 \times 10^7 \qquad (2)$$

$$(2\pi \times 700 \times 10^3) \cong \sqrt{\frac{2.73 \times 10^7}{\tau}}$$

$$\tau = 1.18\text{ms}$$

Therefore, choose the low-pass filter capacitor as

$$C = \frac{\tau}{R} = \frac{1.41\mu s}{1.3k} \simeq 1\text{nF} \qquad (3)$$

Two 1nF capacitors were selected for the design.

Capacitive coupling was used for the FSK input and is recommended to avoid DC feedthrough. This DC voltage would act as a DC offset to shift f_O' from 10.8MHz. Balanced biasing with the 1.0kΩ resistors from Pin 7 to Pins 3 and 6 also is recommended to establish symmetrical, quiescent current conditions in the limiter and phase comparator sections of the 564. The 470Ω pull-up resistor for the VCO output was found to give a rise time less than 10ns. This rise time was further reduced by adding the 100Ω resistor between Pins 9 and 11. Figure 3 shows an unmodulated 10.8MHz input signal and the VCO output. Note the approximate 90° phase lag of the VCO output.

A 0.1μF DC retriever capacitor (Pin 14) has less than 1Ω impedance at f_O, and represents a good compromise between high baud rates (~100k baud) at f_O' and higher-order filtering. If very high baud rates are used, this capacitor could be made smaller with an accompanying increase in the Schmitt trigger hysteresis voltage. The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 5 for 20k, 500k, and 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparator's output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparator's outputs.

The phase comparator's outputs exhibit the waveshapes shown in Figure 4 when the FM input is changed from a square wave FSK modulation to a triangular sweep at a 100Hz modulation rate. The amplitude of the triangular sweep was increased from that used with square wave modulation, causing the loop to be driven in and out of lock. The loop is locked during the smooth, linear portions of the phase comparator's waveshapes and locked during the remaining portions. Lock and capture frequencies were measured for a Pin 2 bias current of 375μA and f_O' = 10.8MHz as:

Lock: $f_{L1} = 6.2\text{MH}_z$ $f_{L2} = 16.4\text{MH}_z$

Capture: $f_{C1} = 9.3\text{MH}_z$ $f_{C2} = 12.2\text{MH}_z$ *P

When the loop is locked, the phase detector's outputs represent the demodulated FM output. When unlocked, high frequency harmonics are present, increasing in amplitude until lock is achieved.

10.8MHz FSK Decoder With NE564

AN1801

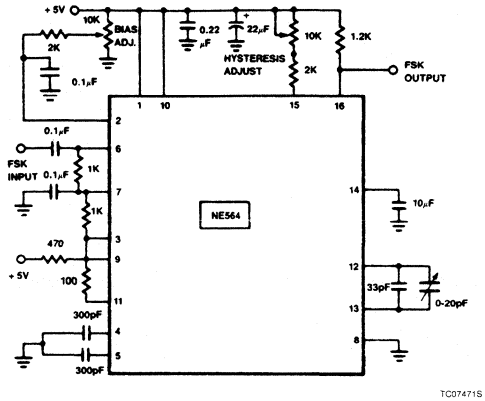
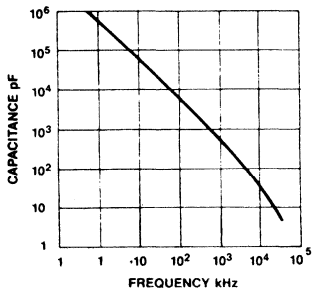
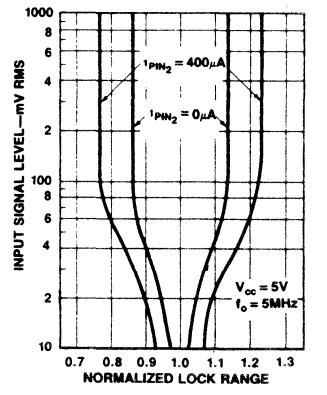


Figure 1. 10.8MHz FSK Decoder Using the NE564



a. VCP Timing Capacitor vs Frequency



b. Lock Range vs Input Signal Level and Bias Current

Figure 2. NE564 Characteristics

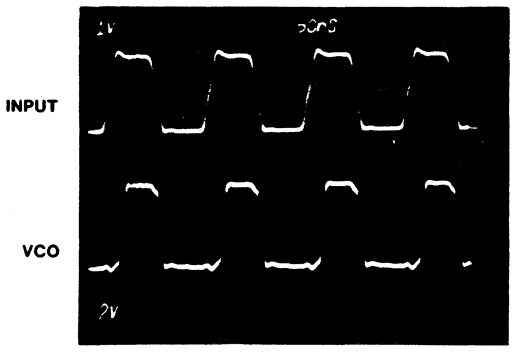


Figure 3. PLL Input and VCO Output for Phase and Frequency Lock at 10.8MHz

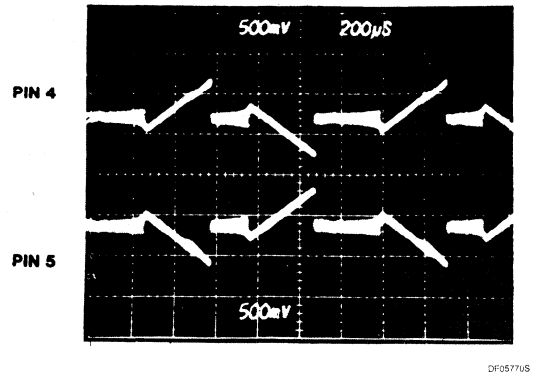
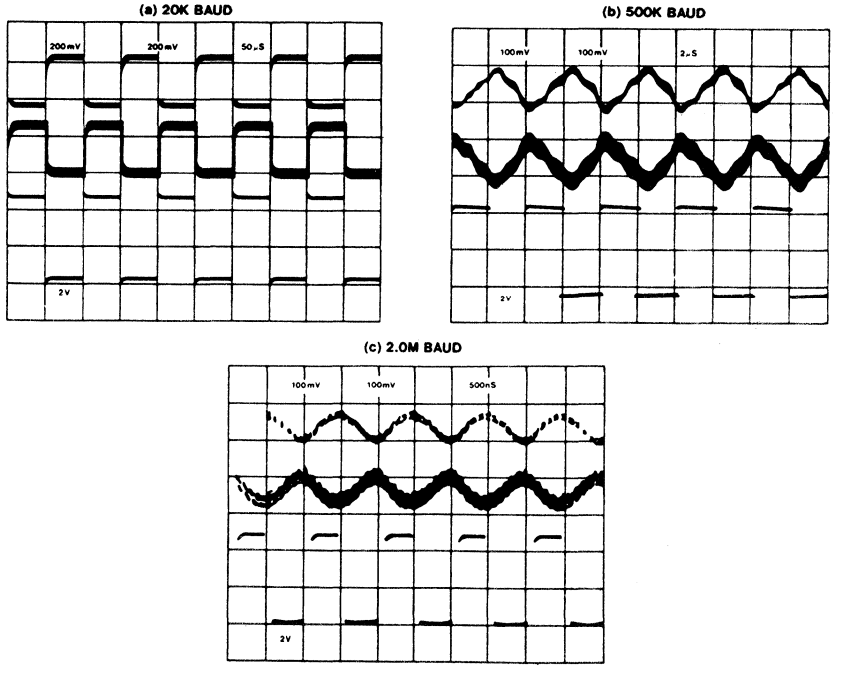


Figure 4. Phase Comparator Outputs Showing Lock and Capture Ranges



NOTE:
Top trace — Pin 4
Center trace — Pin 5
Bottom trace — Pin 16

Figure 5. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs for Various Data Rates

Compandors

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SA571	compandor	1393
SA572	programmable analogue compandor	1400
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AN176
Compandor Cookbook

Application Note

Compandors are versatile, low cost, dual-channel gain control devices for audio frequencies. They are used in tape decks, cordless telephones, and wireless microphones performing noise reduction. Electronic organs, modems and mobile telephone equipment use compandors for signal level control.

So what is companding? Why do it at all? What happens when we do it? Compandor is the contraction of the two words compressor and expandor. There is one basic reason to compress a signal before sending it through a telephone line or recording it on a cassette tape: to process that signal (music, speech, data) so that all parts of it are above the inherent noise floor of the transmission medium and yet not running into the max. dynamic range limits, causing clipping and distortion. The diagrams below demonstrate the idea; they are not totally correct because in the real world of electronics the 3kHz tone is riding on the 1kHz tone. They are shown separated for better explanation.

Figure 1 is the signal from the source. Figure 2 shows the noise always in the transmission medium. Figure 3 shows the max limits of the transmission medium and what happens when a signal larger than those limits is sent through it. Figure 4 is the result of compressing the signal (note that the larger signal would *not* be clipped when transmitted).

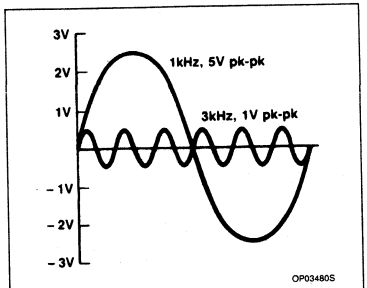


Figure 1. Original Signal Input



Figure 2. Wide-Band Noise Floor of Transmission Line

The received/playback signal is processed (expanded) in exactly the same — only inverted — ratio as the input signal was compressed. The end result is a clean, undistorted signal with a high signal-to-noise ratio.

This document has been designed to give the reader a basic working knowledge of the Signetics Compandor family. The analyses of

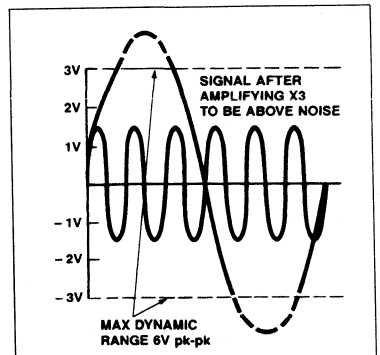


Figure 3

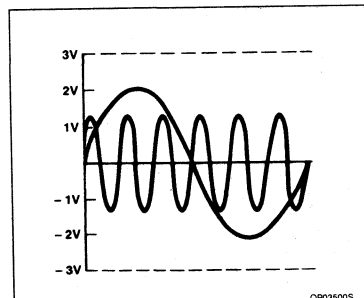
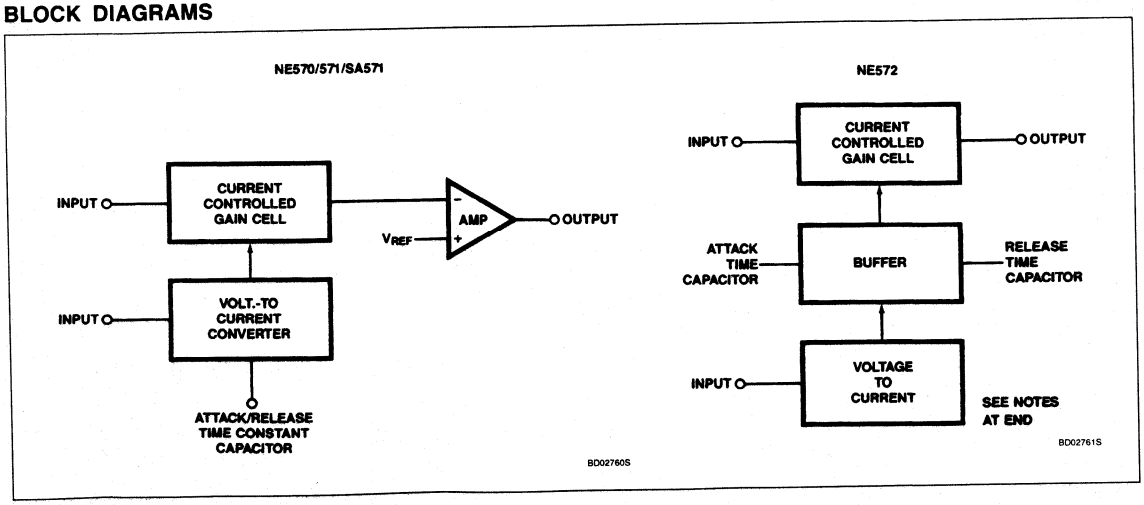


Figure 4. Signal After Compression

BLOCK DIAGRAMS



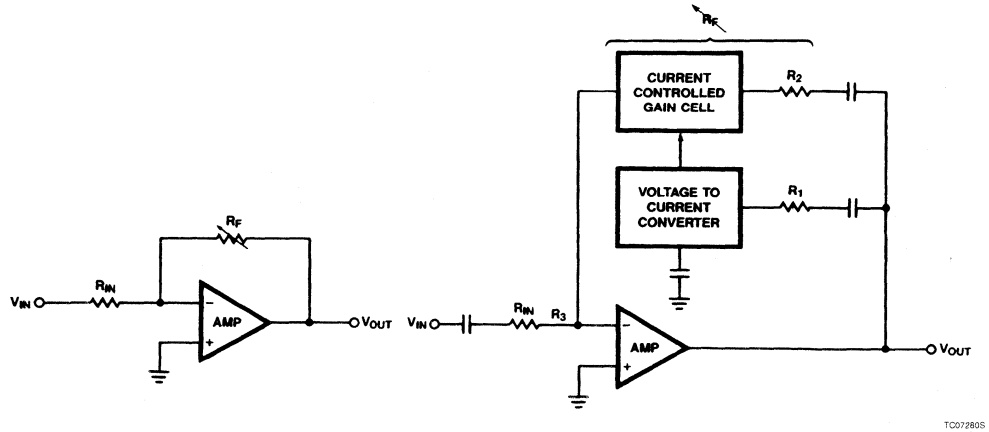


Figure 5. Basic Compressor

three primary applications will be accompanied by "recipes" describing how to select external components (for both proper operation and function modification). Schematic and artwork for an application board are also provided. For comprehensive technical information consult the Compandor Product Guide or the Linear Data Manual.

The basic blocks in a compandor are the current-controlled variable gain cell (ΔG), voltage-to-current converter (rectifier), and operational amplifier. Each Signetics compandor package has two identical, independent channels with the following block diagrams (notice that the 570/71 is different from the 572).

The operational amplifier is the main signal path and output drive.

The full-wave averaging rectifier measures the AC amplitude of a signal and develops a control current for the variable gain cell.

The variable gain cell uses the rectifier control current to provide variable gain control for the operational amplifier gain block.

The compandor can function as a Compressor, Expandor, and Automatic Level Controller or as a complete compressor/expandor system as described in the following:

1) The COMPRESSOR function processes uncontrolled input signals into controlled output signals. The purpose of this is to avoid distortion caused by a narrow dynamic range medium, such as telephone lines, RF and satellite transmissions, and magnetic tape. The Compressor can also limit the level of a signal.
2) The EXPANDOR function allows a user to increase the dynamic range of an incoming compressed signal such as radio broadcasts.
3) The compressor/expandor system allows a user to retain dynamic range and reduce the effects of noise introduced by the transmission medium.
4) The AUTOMATIC LEVEL CONTROL (ALC) function (like the familiar automatic gain control) adjusts its gain proportionally with the input amplitude. This ALC circuit therefore transforms a widely varying input signal into a fixed amplitude output signal without clipping and distortion.

HOW TO DESIGN COMPANDOR CIRCUITS

The rest of the cookbook will provide you with basic compressor, expandor, and automatic level control application information. A NE570/571 has been used in all of the circuits. If high-fidelity audio or separately programmable attack and decay time are needed, the NE572 with a low noise op amp should be used.

The compressor (see Figure 5) utilizes all basic building blocks of the compandor. In this configuration, the variable gain cell is placed in the feedback loop of the standard inverting amplifier circuit. The gain equation is $A_V = -R_F/R_{IN}$. As shown above, the variable gain cell acts as a variable feedback resistor (R_F) (See Figure 5).

As the input signal increases above the crossover level of 0dB, the variable resistor decreases in value. This causes the gain to decrease, thus limiting the output amplitude.

Below the crossover level of 0dB, an increase in input signal causes the variable resistor to increase in value, thereby causing the output signal's amplitude to increase.

In the compressor configuration, the rectifier is connected to the output.

The complete equation for the compressor gain is:

$$\text{Gain comp.} = \left[\frac{R_1 R_2 I_B}{2\ R_3 V_{IN(avg)}}\right]^{1/2}$$

where: $R_1 = 10k$
$R_2 = 20k$
$R_3 = 20k$
$I_B = 140\mu A$

$V_{IN(avg)} = 0.9(V_{IN(RMS)})$

COMPRESSOR RECIPE

1) DC bias the output half way between the supply and ground to get maximum headroom. The circuit in Figure 6 is designed around a system supply of 6V, thus the output DC level should be 3V.

$$V_{OUT\ DC} = (1 + (2R_{DC}/R_4))\ V_{REF}$$

where: $R_4 = 30k$
$V_{REF} = 1.8V$
R_{DC} is external

manipulating the equation, the result is. . .

$$R_{DC} = \left(\left(\frac{V_{OUT}}{V_{REF}}\right) - 1\right)\frac{R_4}{2}$$

Note that the $C_{(DC)}$ should be large enough to totally short out any AC in this feedback loop.

2) Analyze the OUTPUT signal's anticipated amplitude.

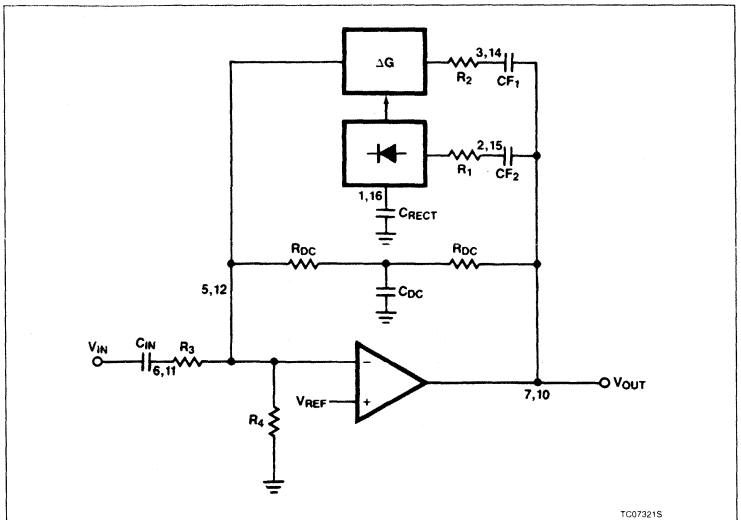
   a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section)

   b) if larger than 3.0V peak, R_1 will *also* need to be increased.

By limiting the peak input currents we avoid signal distortion.

3) The input and output coupling caps need to be large enough not to attenuate any desired frequencies ($X_C = 1/(6.28xf)$).
4) The C_{RECT} should be 1μF to 2μF for initial setup. This directly affects Attack and Release times.
5) An input buffer may be necessary if the source's output impedance needs matching.
6) Pre-emphasis may be used to reduce noise-pumping, breathing, etc., if present. See the NE570/571 data sheet for specific details.
7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. Refer to data sheet for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.
8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network. (This technique prevents infinite compression at low input levels.)

The EXPANDOR utilizes all the basic building blocks of the compandor (see Figure 7). In this configuration the variable gain cell is placed in the inverting input lead of the operational amplifier and acts as a variable input resistance, R_{IN}. The basic gain equation for operational amplifiers in the standard inverting feedback loop is $A_V = -R_F/R_{IN}$.



NOTES:
Max AC current into:
- Gaincell is 140μA peak
- Rectifier is 300μA peak

All components are internal, except the caps and R_{DC}

Figure 6. Basic Compressor

As the input amplitude increases above the crossover level of 0dBM, this variable resistor decreases in value, causing the gain to increase, thus forcing the output amplitude to increase (refer to Figure 10).

Below the crossover level, an increase in input amplitude causes the variable resistor to increase in value, thus forcing the output amplitude to decrease.

In the expandor configuration the rectifier is connected to the input.

The complete equation for the expandor gain is:

$$\text{Gain expandor} = (2R_3V_{IN}(avg))/R_1R_2I_B$$

where: R_1 = 10k
R_2 = 20k
R_3 = 20k
I_B = 140μA
$V_{IN}(avg)$ = 0.9 ($V_{IN(RMS)}$)

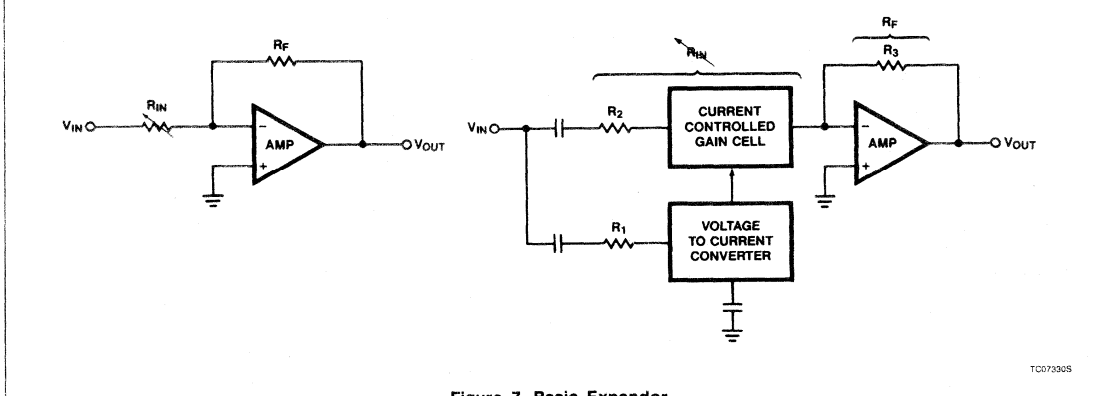


Figure 7. Basic Expandor

EXPANDOR RECIPE

1) DC bias the output halfway between the supply and ground to get maximum headroom. The circuit in Figure 8 is designed around a system supply of 6V so the output DC level should be 3V.

$V_{OUT\ DC} = (1 + R_3/R_4)V_{REF}$
where: R_3 = 20k
R_4 = 30k
V_{REF} = 1.8V

Note that when using a supply voltage higher than 6V the DC output level should be adjusted. To increase the DC output level, it is recommended that R_4 be decreased by adding parallel resistance to it. (Changing R_3 would also affect the expandor's AC gain and thus cause a mismatch in a companding system.)

2) Analyze the input signal's anticipated amplitude:

a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section)

b) if larger than 3.0V peak, R_1 will *also* need to be increased. (see INGREDIENTS)

By limiting the peak input currents we avoid signal distortion.

3) The input and output decoupling caps need to be large enough not to attenuate any desired frequencies.
4) The C_{RECT} should be 1μF to 2μF for initial setup.
5) An input buffer may be necessary if the source's output impedance needs matching.
6) De-emphasis would be necessary if the complementary compressor circuit had been pre-emphasized (as in a tape deck application). See the Hi-Fi Expandor application in the Linear Data Manual.
7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. See Linear Data Manual for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.
8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network (see Linear Data Manual). (This technique prevents infinite expansion at low input levels.)

In the ALC configuration, (Figure 9), the variable gain cell is placed in the feedback loop of the operational amplifier (as in the Compressor) and the rectifier is connected to the input.

As the input amplitude increases above the crossover point, the overall system gain decreases proportionally, holding the output amplitude constant.

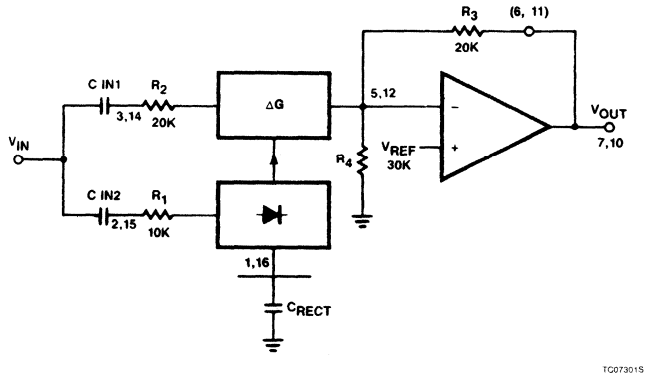
As the input amplitude decreases below the crossover point, the overall system gain increases proportionally, holding the output amplitude at the same constant level.

The complete gain equation for the ALC is:

$$\text{Gain} = \frac{R_1 R_2 I_B}{2\ R_3\ V_{IN(avg)}}$$

$$\text{Output level} = \frac{R_1 R_2 I_B}{2\ R_3}\left(\frac{V_{IN}}{V_{IN(avg)}}\right)$$

$$\text{where}\ \frac{V_{IN}}{V_{IN(avg)}} = \frac{\pi}{2\sqrt{2}} = 1.11\ \text{(for sine wave)}$$



NOTE:
All components are internal except caps.

Figure 8. Basic Expandor

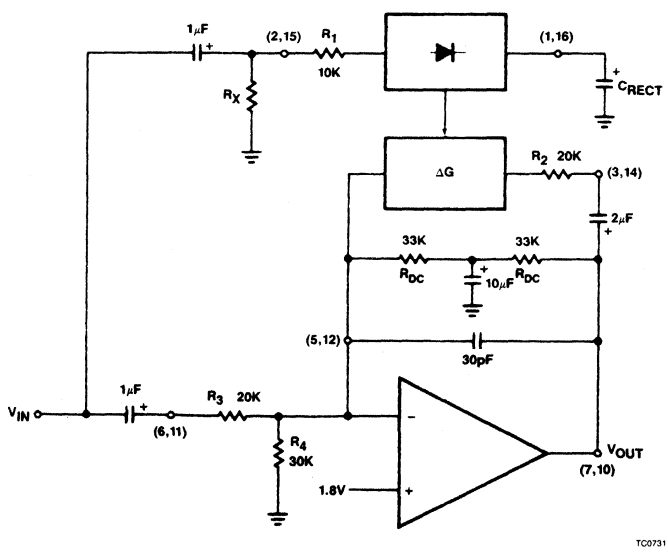


Figure 9. Automatic Level Control

Note that for very low input levels, ALC may not be desired and to limit the maximum gain, resistor R_X has been added. The modified gain equation is:

$$\text{Gain max.} = \frac{\left(\frac{R_1 + R_X}{1.8V}\right) \times R_2 \times I_B}{2\ R_3}$$

$R_X \cong$ ((desired max gain) $\times$ 26k) – 10k

INGREDIENTS

[Application guidelines for internal and external components (and input/output constraints) needed to tailor (cook) each of the three entrees (applications) to your taste.]

R_1 (10kΩ) limits input current to the rectifier. This current should not exceed an AC peak value of ± 300μA. An external resistor may be placed in series with R_1 if the input voltage to the rectifier will exceed ±3.0V peak (i.e., 10k × 300μA = 3.0V).

R_2 (20kΩ) limits input current to the variable gain cell. This current should not exceed an AC peak value of ± 140μA. Again, an external resistor has to be placed in series with R_2 if the input voltage to the variable gain cell exceeds ±2.8V (i.e., 20k × 140μA).

R_3 (20kΩ) acts in conjunction with R_4 as the feedback resistor (R_F) (expandor configuration) in the equation. (R_3's value can be either reduced or increased externally.) However, it is recommended that R_4 be the one to change when adjusting the output DC level.

R_4 (30kΩ) acts as the input resistor (R_{IN}) in the standard non-inverting op amp circuit. (Its value can only be reduced.)

$V_{OUT\ DC} = (1 + (R_3/R_4))V_{REF}$
(for the Expandor)
$V_{OUT\ DC} = (1 + (2R_{DC}/R_4))V_{REF}$
(for the Compandor, ALC)

[The purpose of these DC biasing equations is to allow the designer to set the output halfway between the supply rails for largest headroom (usually some positive voltage and ground).]

C_{DC} acts as an AC shunt to ground to totally remove the DC biasing resistors from the AC gain equation.

C_F caps are AC signal coupling caps.

C_{RECT} acts as the rectifier's filter cap and directly affects the response time of the circuit. There is a trade-off, though, between fast attack and decay times and distortion.

The time constant is: 10k × C_{RECT}

The total harmonic distortion (THD) is approximated by:

$THD \cong (1\mu F/C_{RECT})(1kHz/freq.) \times 0.2\%$

NOTES:
The NE572 differs from the 570/571 in that:
1. There is no internal op amp.
2. The attack and release times are programmed separately.

SYSTEM LEVELS OF A COMPLETE COMPANDING SYSTEM

Figure 10 demonstrates the compressing and expanding functions:

Point A represents a wide dynamic range signal with a maximum amplitude of +16dB and minimum amplitude of –80dB.

Point B represents the compressor output showing a 2:1 reduction in dynamic range (–40dB is increased to –20dB, for example). Point B can also be seen as the dynamic range of a transmission medium. Transmission noise is present at the –60dB level from Point B to Point C.

Point C represents the input signal to the expandor.

Point D represents the output of the expandor. The signal transformation from Point C to D represents a 1:2 expansion.

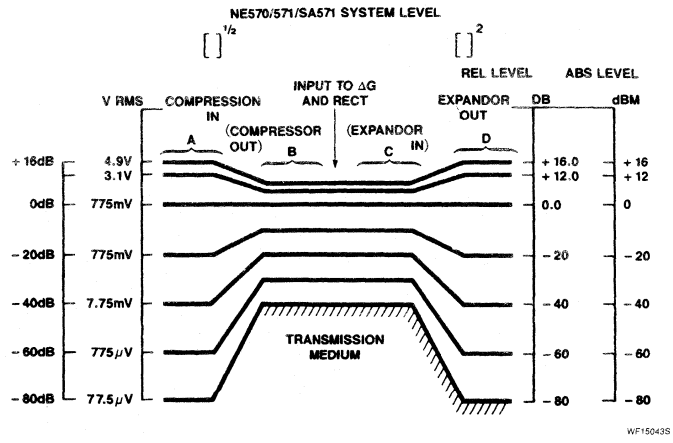
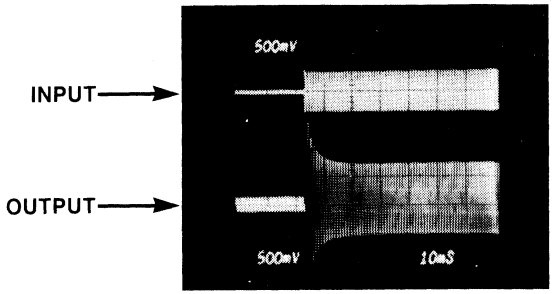


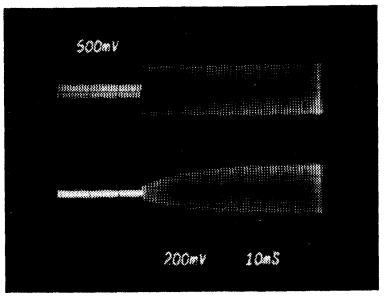
Figure 10. System Levels of a Complete Companding System

WHAT IS COMPANDING??

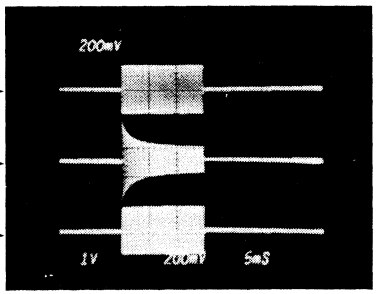
Shown here are some scope pictures of what three functions of the compandor look like in the kitchen, responding to tone bursts of varying amplitudes.



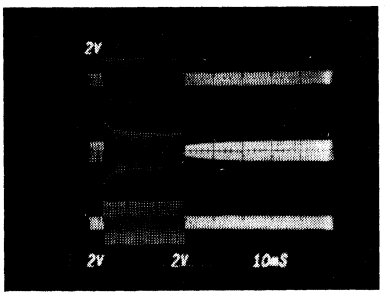
COMPRESSION 1kHz



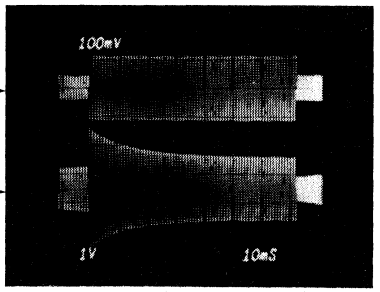
EXPANSION 1kHz



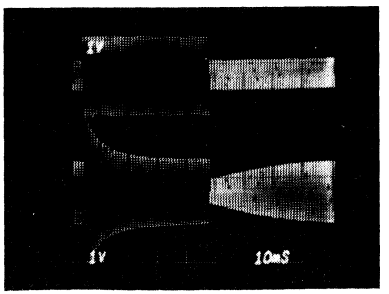
COMPANDOR SYSTEM 15kHz



COMPANDOR SYSTEM 1kHz



AUTOMATIC LEVEL CONTROL
(SMALL SIGNAL INPUT)



AUTOMATIC LEVEL CONTROL
(LARGE SIGNAL INPUT)

Figure 11

APPLICATION BOARD

Shown below is the schematic (Figure 12) for Signetics' NE570/571 evaluation/demo board. This board provides one channel of Expansion and one channel of Compression (which can be switched to Automatic Level Control).

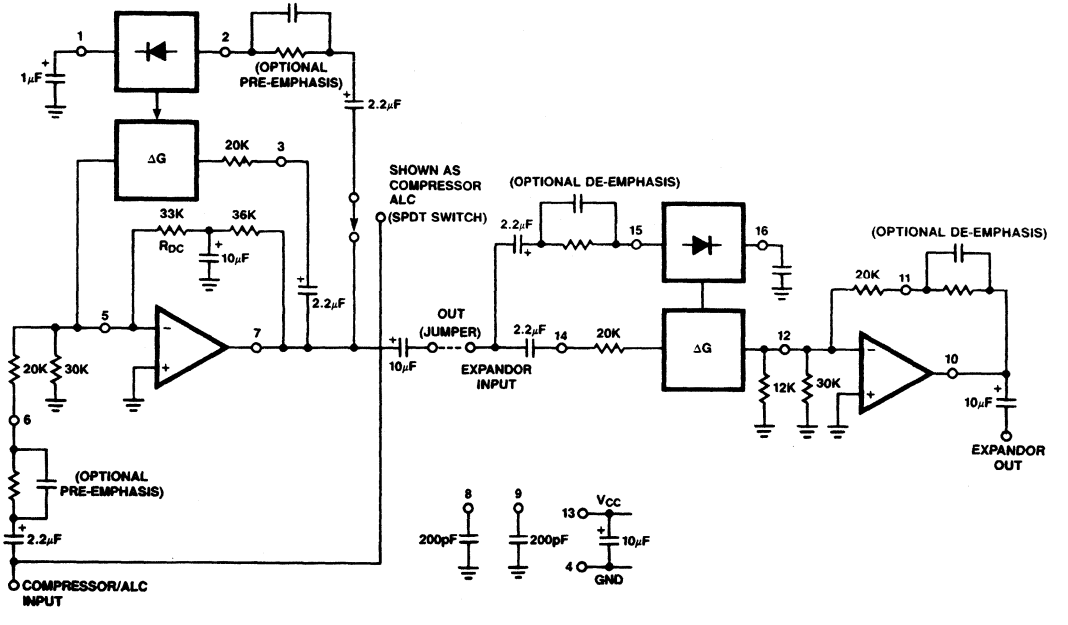


Figure 12

NE570/571/SA571
Compandor

Product Specification

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{avg}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{avg}}{R_1}$$

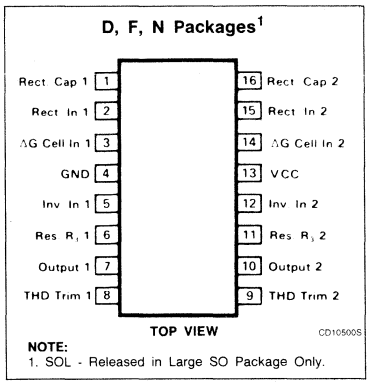
FEATURES

- **Complete compressor and expandor in one IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to $6V_{DC}$**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Cellular radio**
- **Telephone trunk compandor — 570**
- **Telephone subscriber compandor — 571**
- **High level limiter**
- **Low level expandor — noise gate**
- **Dynamic noise reduction systems**
- **Voltage-controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

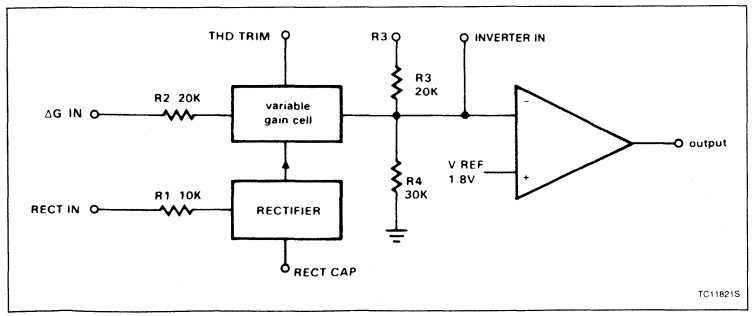


NOTE:
1. SOL - Released in Large SO Package Only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE570F
16-Pin Plastic DIP	0 to +70°C	NE570N
16-Pin Plastic SOL	0 to +70°C	NE571D
16-Pin Cerdip	0 to +70°C	NE571F
16-Pin Plastic Cerdip	0 to +70°C	NE571N
16-Pin Cerdip	−40°C to +85°C	SA571F
16-Pin Plastic DIP	−40°C to +85°C	SA571N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Positive supply 570 571	 24 18	V_{DC}
T_A	Operating ambient temperature range NE SA	 0 to +70 −40 to +85	 °C °C
P_D	Power dissipation	400	mW

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 15V$. Except where indicated, the 571 specifications are identical to those of the 570.

SYMBOL	PARAMETER	TEST CONDITIONS	NE570			NE/SA571[5]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		24	6		18	V
I_{CC}	Supply current	No signal		3.2	4.8		3.2	4.8	mA
I_{OUT}	Output current capability		±20			±20			mA
SR	Output slew rate			±.5			±.5		V/μs
	Gain cell distortion[2]	Untrimmed Trimmed		0.3 0.05	1.0		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15		±5	±15	%
	Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±20	±50		±30	±100	mV
	Expandor output noise	No signal, 15Hz − 20kHz[1]		20	45		20	60	μV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dBm
	Gain change[2, 4]	−40°C < T < 70°C 0°C < T < 70°C		±0.1 ±0.1	 ±0.2		±0.1 ±0.1	 ±0.4	dB
	Reference drift[4]	−40°C < T < 70°C 0°C < T < 70°C		+2, −25 ±5	+10, −40 ±10		+2, −25 ±5	+20, −50 ±20	mV
	Resistor drift[4]	−40°C < T < 70°C 0°C < T < 70°C		+8, −0 +1.−0					%
	Tracking error (measured relative to value at unity gain) equals [$V_O - V_O$ (unity gain)] dB − V_2dBm	Rectifier input, V_2 = +6dBm, V_1 = 0dB V_2 = −30dBm, V_1 = 0dB		±0.2 +0.2	 −0.5, +1		 +0.2	 −1, +1.5	dB
	Channel separation			60			60		dB

NOTES:
1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at $T_A = 25°C$.
5. Electrical characteristics for the SA571 only are specified over −40 to +85°C temperature range.

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\, e^{-t/\tau} + G_{final};\ \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

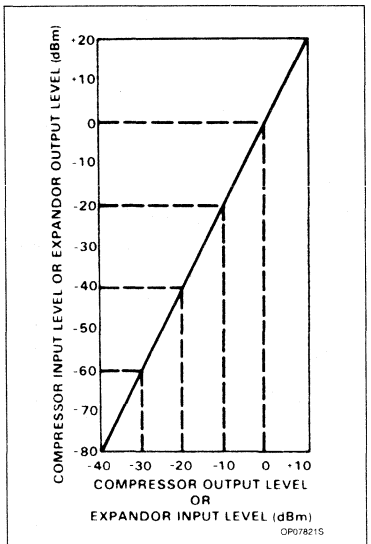
The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

The output stage is capable of ± 20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

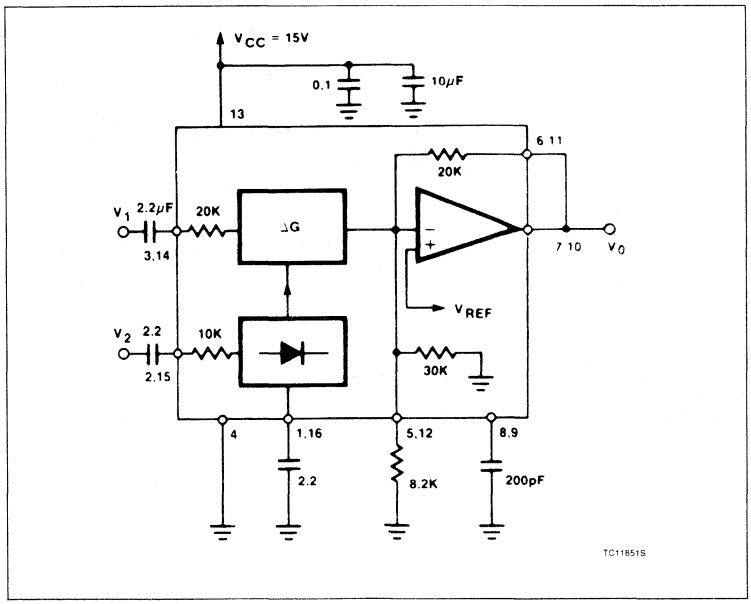
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS



Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT



INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components. This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (< 0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to −80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expandor are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

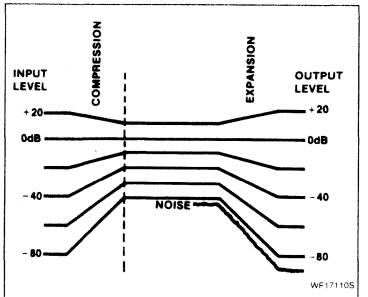


Figure 1. Restricted Dynamic Range Channel

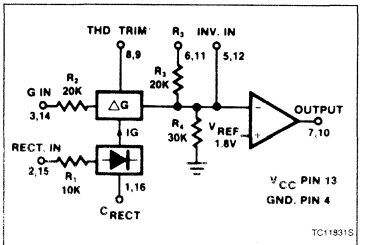


Figure 2. Chip Block Diagram (1 of 2 Channels)

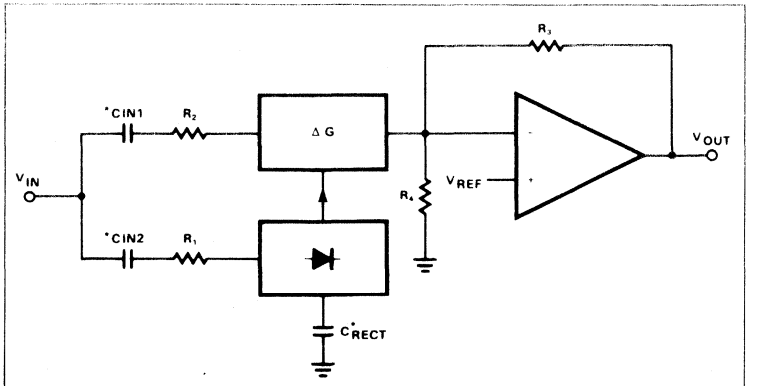
The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 4 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\ DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

$$V_{REF} = \left(1 + \frac{R_{DC\ TOT}}{30k}\right) 1.8V$$



NOTES:

$$\text{GAIN} = \frac{2\ R_3\ V_{IN}\ (\text{avg.})}{R_1\ R_2\ I_B}$$

$I_B = 140\mu A$

*External components

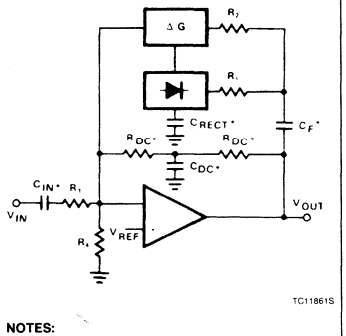
Figure 3. Basic Expandor

The output of the expandor will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4}\ V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k} \right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.



NOTES:

$$GAIN = \left(\frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (avg)} \right)^{1/2}$$

$I_B = 140\mu A$

*external components

Figure 4. Basic Compressor

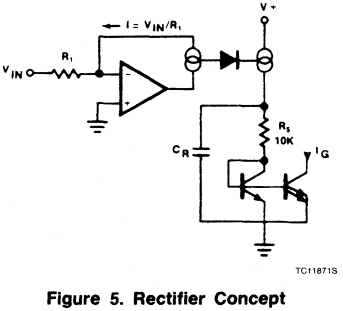
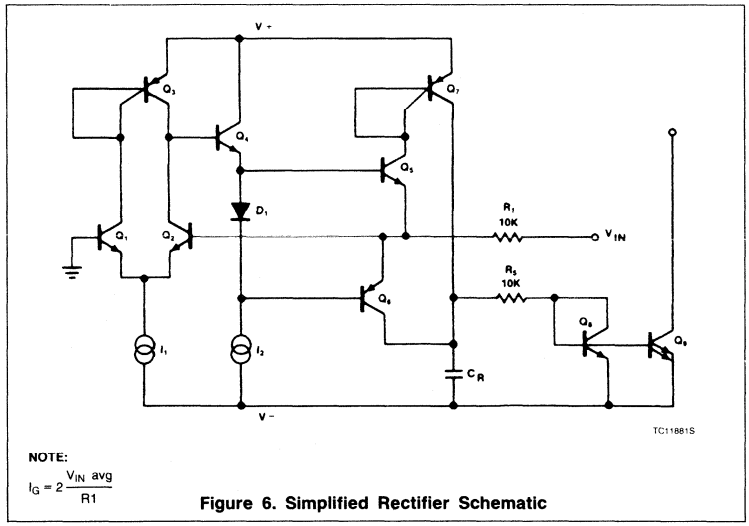


Figure 5. Rectifier Concept

CIRCUIT DETAILS — RECTIFIER

Figure 5 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and



NOTE:

$$I_G = 2\frac{V_{IN}\ avg}{R1}$$

Figure 6. Simplified Rectifier Schematic

then mirrored with a gain of 2 to become I_G, the gain control current.

Figure 6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The α's of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

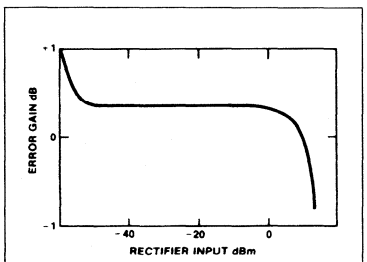


Figure 7. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, −20dBm, and −40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

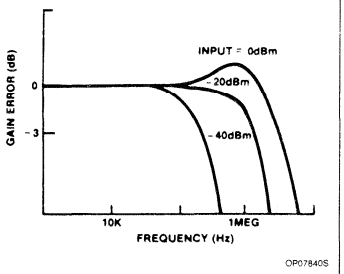


Figure 8. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linerarized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} ($= V_{IN}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

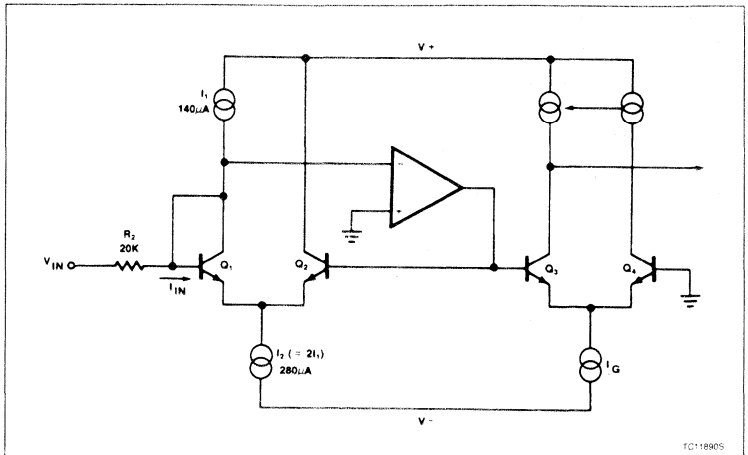
$$I_2 - (I_1 + I_{IN}) = I_1 - I_{IN} = I_{C2}.$$

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G = I_{C3} + I_{C4}$ and $I_{OUT} = I_{C4} - I_{C3}$ will yield the multiplier transfer function,



NOTE:

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{I_G\ V_{IN}}{I_2\ R_2}$$

Figure 9. Simplified ΔG Cell Schematic

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN}}{R_2} \frac{I_G}{I_1}.$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

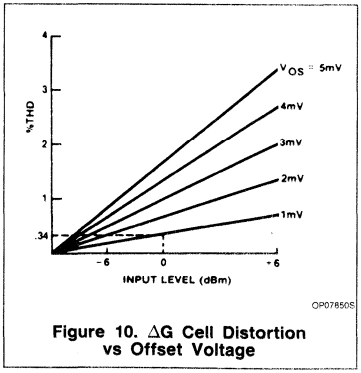


Figure 10. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about ½mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

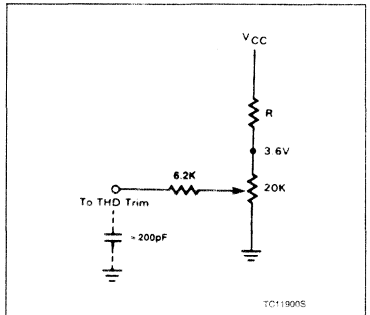


Figure 11. THD Trim Network

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 13 shows such a trim network.

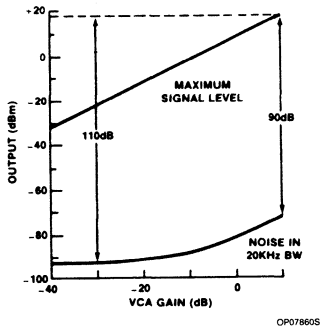


Figure 12. Dynamic Range of NE570

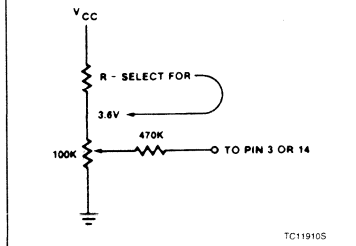


Figure 13. Control Signal Feedthrough Trim

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

RESISTORS

Inspection of the gain equations in Figures 3 and 4 will show that the basic compressor and expandor circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made 1/7 the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

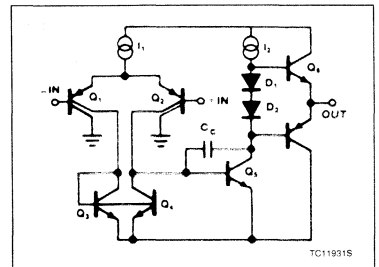


Figure 14. Operational Amplifier

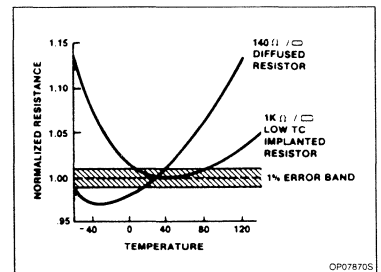


Figure 15. Resistance vs Temperature

NE/SA572
Programmable Analog Compandor

Product Specification

DESCRIPTION

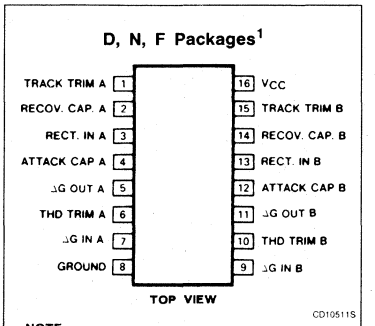
The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- **Independent control of attack and recovery time**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external op amp**
- **Wide dynamic range — greater than 110dB**
- **Temperature-compensated gain control**
- **Low distortion gain cell**
- **Low noise — 6μV typical**
- **Wide supply voltage range — 6V – 22V**
- **System level adjustable with external components**

PIN CONFIGURATION



NOTE:
1. D package released in large SO (SOL) package only.

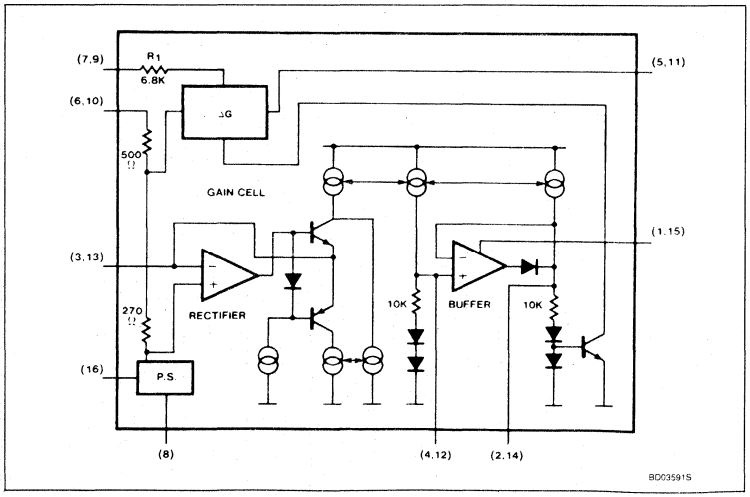
APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High-level limiter**
- **Low-level noise gate**
- **State variable filter**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE572D
16-Pin Plastic DIP	0 to +70°C	NE572N
16-Pin Plastic SO	−40°C to +85°C	SA572D
16-Pin Cerdip	−40°C to +85°C	SA572F
16-Pin Plastic DIP	−40°C to +85°C	SA572N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

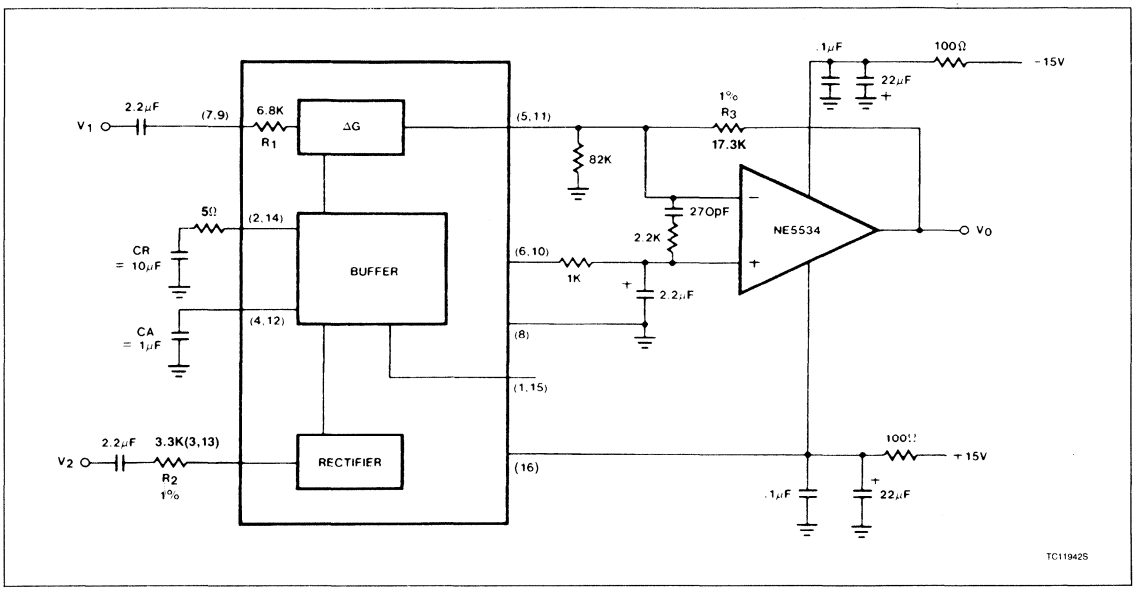
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	V_{DC}
T_A	Operating temperature range NE572 SA572	 0 to +70 −40 to +85	 °C
P_D	Power dissipation	500	mW

DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) V_{CC} = 15V, T_A = 25°C; Expandor mode (see Test Circuit). Input signals at unity gain level (0dB) = 100mV_{RMS} at 1kHz; $V_1 = V_2$; R_2 = 3.3kΩ; R_3 = 17.3kΩ.

SYMBOL	PARAMETER	TEST CONDITIONS	NE572			SA572			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		22	6		22	V_{DC}
I_{CC}	Supply current	No signal			6			6.3	mA
V_R	Internal voltage reference		2.3	2.5	2.7	2.3	2.5	2.7	V_{DC}
THD	Total harmonic distortion (untrimmed)	1kHz C_A = 1.0μF		0.2	1.0		0.2	1.0	%
THD	Total harmonic distortion (trimmed)	1kHz C_R = 10μF		0.05			0.05		%
THD	Total harmonic distortion (trimmed)	100Hz		0.25			0.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20 − 20kHz)		6	25		6	25	μV
	DC level shift (untrimmed)	Input change from no signal to 100mV_{RMS}		±20	±50		±20	±50	mV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dB
	Large-signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0		0.7	3	%
	Tracking error (measured relative to value at unity gain) = [$V_O - V_O$ (unity gain)]dB − V_2dB	Rectifier input V_2 = +6dB V_1 = 0dB V_2 = −30dB V_1 = 0dB		 ±0.2 ±0.5	 −1.5 +0.8		 ±0.2 ±0.5	 −2.5 +1.6	dB
	Channel crosstalk	200mV_{RMS} into channel A, measured output on channel B	60			60			dB
PSRR	Power supply rejection ratio	120Hz		70			70		dB

TEST CIRCUIT



AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10k resistor R_A defines the attack time t_A. The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10k resistor R_R. Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1μF and 1.0μF attack capacitors, respectively. Recovery time of 200ms can be obtained with a 4.7μF external capacitor. With the recovery capacitor added in the level sensor, the gain control ripple for low frequency signals is much lower than that of a simple RC ripple filter. As a result, the residual third harmonic distortion of low frequency signal in a two quad transconductance amplifier is greatly improved. With the 1.0μF attack capacitor and 4.7μF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0 – 70°C. The SA572 is intended for applications from –40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of $Q_1 - Q_2$ and the V_{BE} of $Q_3 - Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\triangle V_{BE_{Q3-Q4}} = \triangle_{BE_{Q1-Q2}}$$

$(V_{BE} = V_T \ln IC/IS)$

$$V_T \ln\left(\frac{\frac{1}{2}I_G + \frac{1}{2}I_O}{I_S}\right) - V_T \ln\left(\frac{\frac{1}{2}I_G - \frac{1}{2}I_O}{I_S}\right)$$

$$= V_T \ln\left(\frac{I_1 + I_{IN}}{I_S}\right) - V_T \ln\left(\frac{I_2 - I_1 - I_{IN}}{I_S}\right) \quad (2)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$

$I_1 = 140\mu A$

$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \quad (3)$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within $\pm 25\mu A$ into the THD trim pin.

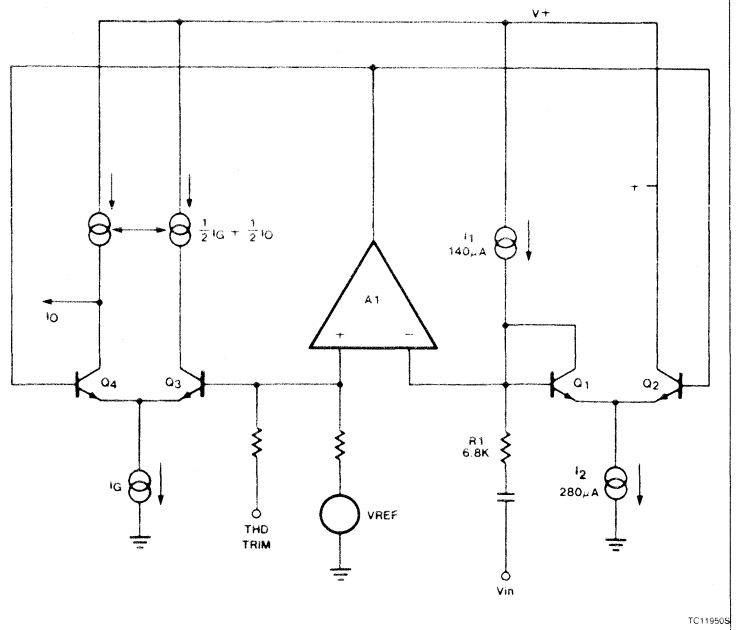


Figure 1. Basic Gain Cell Schematic

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only $6\mu V$ in the audio spectrum (10Hz – 20kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (4)$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN(AVG)}}{R_2}$$

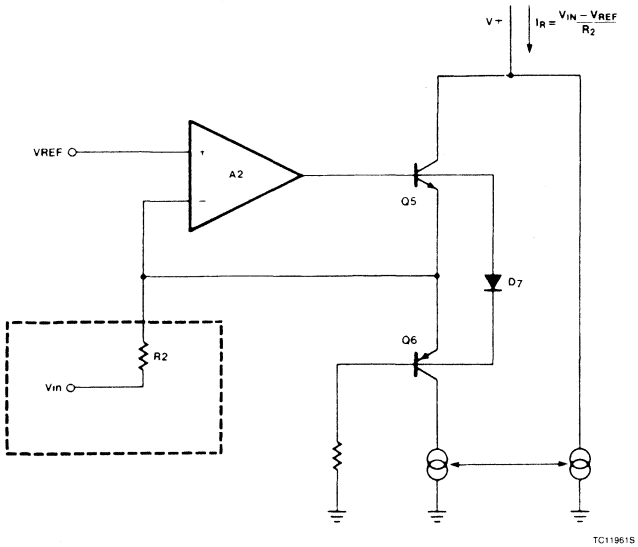


Figure 2. Simplified Rectifier Schematic

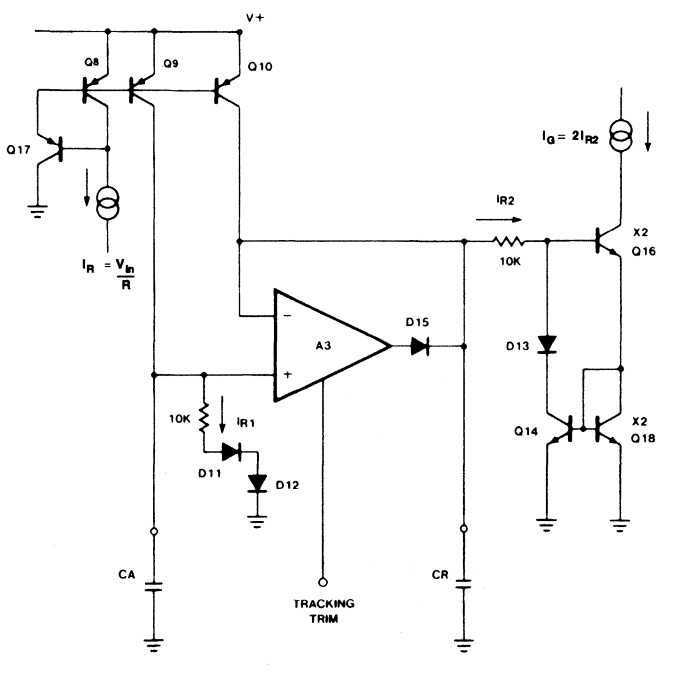


Figure 3. Buffer Amplifier Schematic

The internal bias scheme limits the maximum output current I_R to be around 300μA. Within a ±1dB error band the input range of the rectifier is about 52dB.

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\ e^{\frac{-t}{\tau_A}} + Ga_{FNL}$$

Ga_{INT} = Initial Gain

Ga_{FNL} = Final Gain

$\tau_A = R_A \cdot CA = 10k \cdot CA$

where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR · R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{R\ INT} - G_{R\ FNL})\ e^{\frac{-t}{\tau_R}} + G_{R\ FNL}$$

$\tau R = R_R \cdot CR = 10k \cdot CR$

where τR is the recovery time constant and R_R is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of ±3μA.

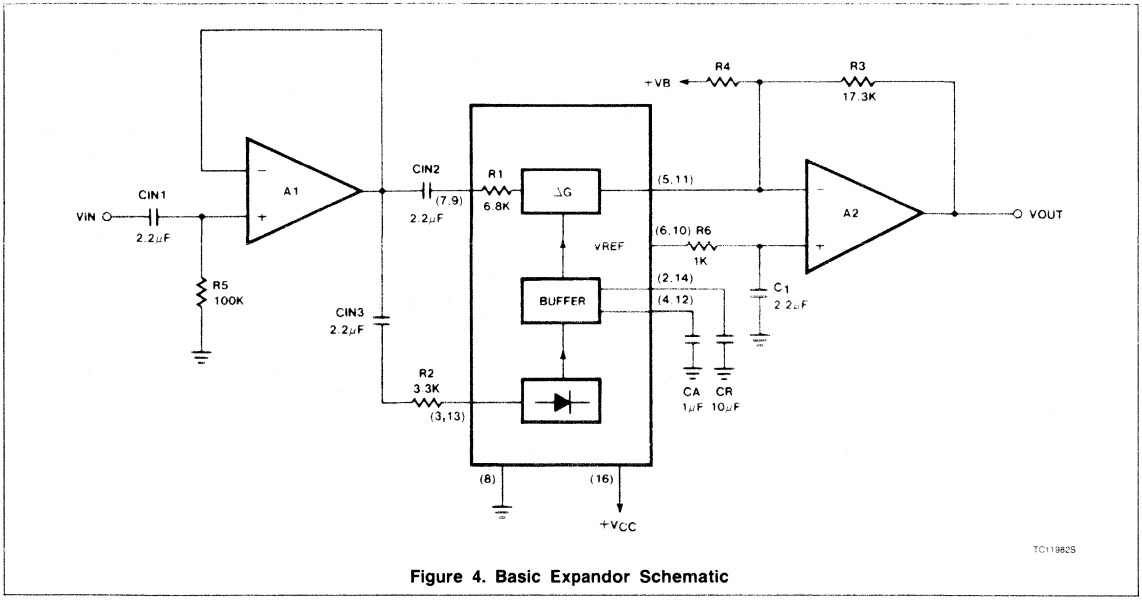


Figure 4. Basic Expandor Schematic

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \qquad (5)$$

($I_1 = 140\mu A$)

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA · 6.8k = 952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B\frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}} \right)^{1/2} \quad (7)$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF} \left(1 + \frac{R_{DC1} + R_{DC2}}{R_4} \right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4} \right) \quad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

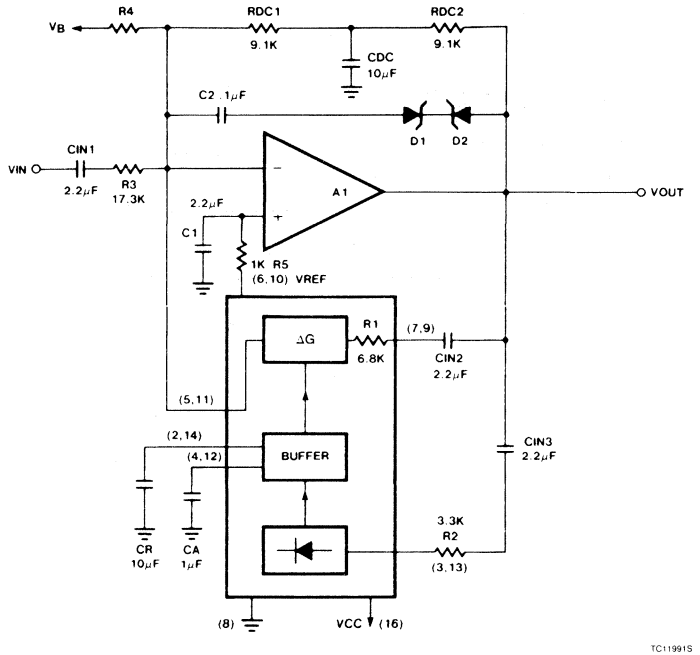


Figure 5. Basic Compressor Schematic

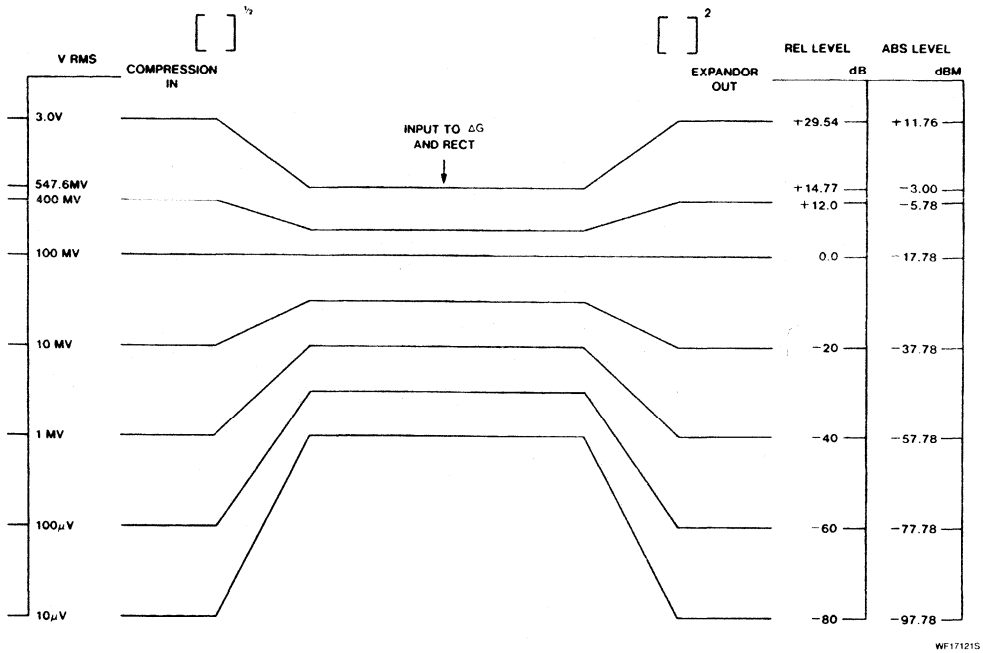


Figure 6. NE572 System Level

NE575
Low Voltage Compandor

Preliminary Specification

DESCRIPTION

The NE575 is a dual gain-control circuit designed for low voltage applications. The NE575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

FEATURES

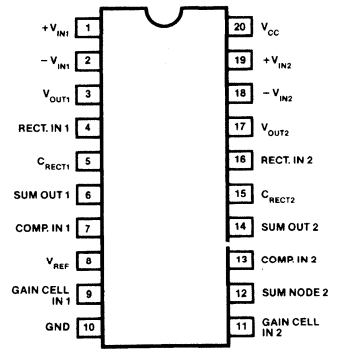
- **Operating voltage range from 3 to 7V**
- **Reference voltage of 100mV_{RMS} = 0dB**
- **One dedicated summing op amp per channel and two extra uncommitted op amps**
- **600Ω drive capability**
- **Single or split supply operation**
- **Wide input/output swing capability.**

APPLICATIONS

- **Portable communications**
- **Cellular radio**
- **Cordless telephone**
- **Consumer audio**
- **Portable broadcast mixers**
- **Wireless microphones**
- **Modems**
- **Electric organs**

PIN CONFIGURATION

NE575 D, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE575N
20-Pin Plastic SO	0 to +70°C	NE575D

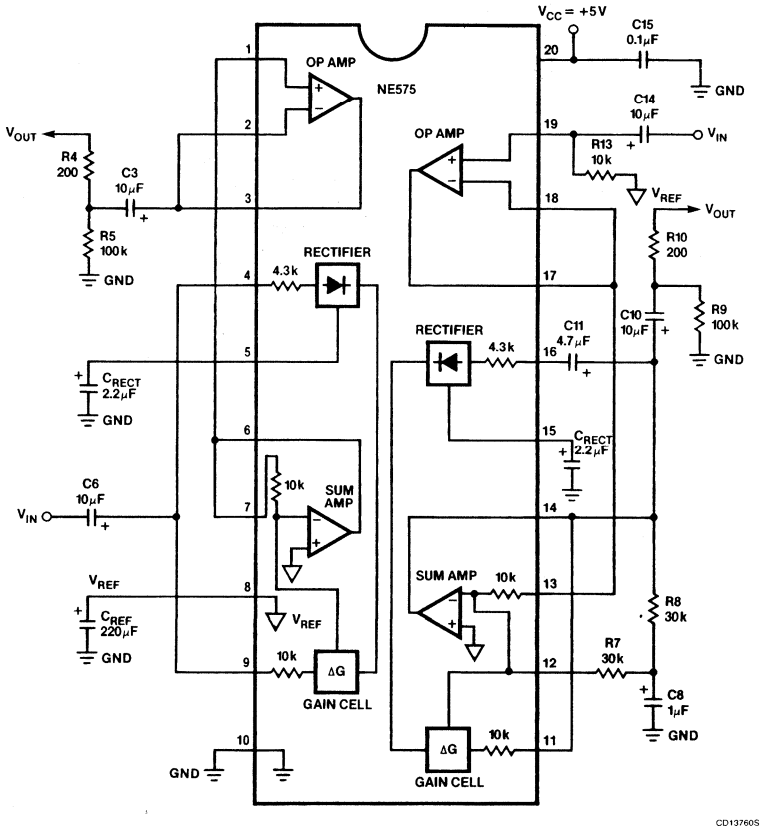
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	8	V
T_A	Operating temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, 0dB = 100mV, expander mode, V_{CC} = 5V, Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
For compandor, including summing amplifier						
V_{CC}	Supply voltage[1]		3	5	7	V
I_{CC}	Supply current	No signal	3	4	5.5	mA
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.13	1.0	%
eno	Output voltage noise	BW = 20kHz, R_S = 0Ω		6	20	μV
0dB	Unity gain level	1kHz	−1.0		1.0	dB
V_{OS}	Output voltage offset	no signal	−100		100	mV
	Output DC shift	no signal to 0dB	−50	10	50	mV
	Tracking error	1kHz, +6dB to −30dB	−0.5		+0.5	dB
	Crosstalk	1kHz, 0dB, C_{REF} = 220μF		−80	−65	dB
For operational amplifier						
V_O	Output swing	V_{P-P}, R_L = 10kΩ	V_{CC}−0.4	V_{CC}−0.2		V
R_L	Output load	1kHz	600			Ω
CMR	Input common-mode range		0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		dB
I_B	Input bias current	V_{IN} = 0.5V − 4.5V	−0.3		0.3	μA
V_{OS}	Input offset voltage		−10	3	10	mV
A_{VOL}	Open-loop gain	R_L = 10kΩ	80	90		dB
SR	Slew rate	unity gain		1		V/μs
GBW	Bandwidth	unity gain		3		MHz
eni	Input voltage noise	BW = 20kHz		2.5		μV
PSRR	Power supply rejection ratio	1kHz, 250mV		60		dB

NOTE:
1. The IC remains functional down to 2V.



NOTE:
Left channel in expander mode; right channel in compressor mode.
For additional information, call the factory.

Figure 1. Typical Application

AN174
Applications for Compandors: NE570/571/SA571

Application Note

APPLICATIONS

The following circuits will illustrate some of the wide variety of applications for the NE570.

BASIC EXPANDOR

Figure 1 shows how the circuit would be hooked up for use as an expandor. Both the rectifier and ΔG cell inputs are tied to V_{IN} so that the gain is proportional to the average value of (V_{IN}). Thus, when V_{IN} falls 6dB, the gain drops 6dB and the output drops 12dB. The exact expression for the gain is

$$\text{Gain exp.} = \left[\frac{2\ R_3\ V_{IN}\ (\text{avg})}{R_1\ R_2\ I_B};\right]^2$$

$I_B = 140\mu A$

The maximum input that can be handled by the circuit in Figure 1 is a peak of 3V. The rectifier input current can be as large as $I = 3V/R_1 = 3V/10k = 300\mu A$. The ΔG cell input current should be limited to $I = 2.8V/R_2 = 2.8V/20k = 140\mu A$. If it is necessary to handle larger input voltages than 0 ±2.8V peak, external resistors should be placed in series with R_1 and R_2 to limit the input current to the above values.

Figure 1 shows a pair of input capacitors C_{IN1} and C_{IN2}. It is now necessary to use both capacitors if low level tracking accuracy is not important. If R_1 and R_2 are tied together and share a common capacitor, a small current will flow between the ΔG cell summing node and the rectifier summing node due to offset voltages. This current will produce an error in the gain control signal at low levels, degrading tracking accuracy.

The output of the expandor is biased up to 3V by the DC gain provided by R_3, R_4. The output will bias up to

$$V_{OUT\ DC} = (1+\frac{R_3}{R_4})\ V_{REF}$$

For supply voltages higher than 6V, R_4 can be shunted with an external resistor to bias the output up to $\frac{1}{2}V_{CC}$.

Note that it is possible to externally increase R_1, R_2, and R_3, and to decrease R_3 and R_4. This allows a great deal of flexibility in setting up system levels. If larger input signals are to be handled, R_1 and R_2 may be increased; if a larger output is required, R_3 may be increased. To obtain the largest dynamic range out of this circuit, the rectifier input should always be as large as possible (subject to the ±300μA peak current restriction).

BASIC COMPRESSOR

Figure 2 shows how to use the NE570/571 as a compressor. It functions as an expandor in the feedback loop of an op amp. If the input rises 6dB, the output can rise only 3dB. The 3dB increase in output level produces a 3dB increase in gain in the ΔG cell, yielding a 6dB increase in feedback current to the summing node. Exact expression for gain is

$$\text{Gain comp.} = \left[\frac{R_1\ R_2\ I_B}{2\ R_3 V_{IN}\ (\text{avg})}\right]^{1/2}$$

The same restrictions for the rectifier and ΔG cell maximum input current still hold, which place a limit on the maximum compressor output. As in the expandor, the rectifier and ΔG cell inputs could be made common to save a capacitor, but low level tracking accuracy would suffer. Since there is no DC feedback path around the op amp through the ΔG cell, one must be provided externally. The pair of resistors R_{DC} and the capacitor C_{DC} must be provided. The op amp output will bias up to

$$V_{OUT\ DC} = (1 + \frac{2R_{DC}}{R4})\ V_{REF}$$

For the largest dynamic range, the compressor output should be as large as possible so that the rectifier input is as large as possible (subject to the ±300μA peak current restriction). If the input signal is small, a large output can be produced by reducing R_3 with the attendant decrease in input impedance, or by increasing R_1 or R_2. It would be best to increase R_2 rather than R_1 so that the rectifier input current is not reduced.

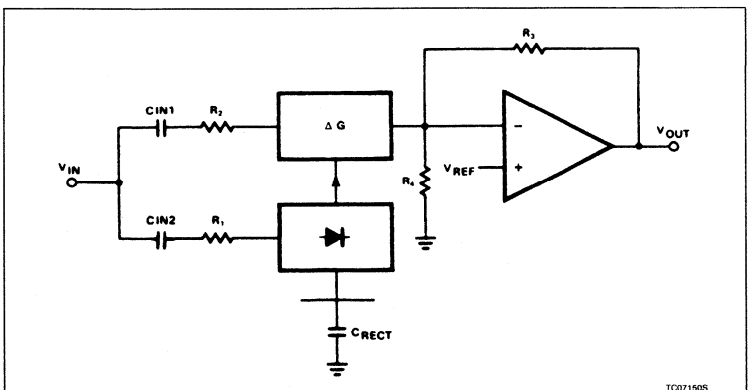


Figure 1. Basic Expandor

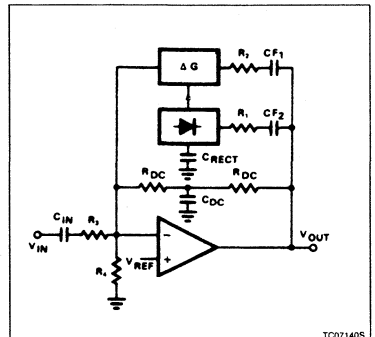


Figure 2. Basic Compressor

DISTORTION TRIM

Distortion can be produced by voltage offsets in the ΔG cell. The distortion is mainly even harmonics, and drops with decreasing input signal (input signal meaning the current into the ΔG cell). The THD trim terminal provides

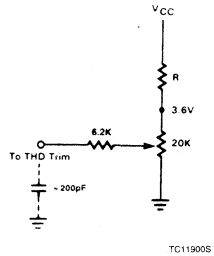


Figure 3. THD Trim Network

a means for trimming out the offset voltages and thus trimming out the distortion. The circuit shown in Figure 3 is suitable, as would be any other capable of delivering $\pm 30\mu A$ into 100Ω resistor tied to 1.8V.

LOW LEVEL MISTRACKING

The compandor will follow a 2-to-1 tracking ratio down to very low levels. The rectifier is responsible for errors in gain, and it is the rectifier input bias current of $< 100nA$ that produces errors at low levels. The magnitude of the error can be estimated. For a full-scale rectifier input signal of $\pm 200\mu A$, the average input current will be $127\mu A$. When the input signal level drops to a $1\mu A$ average, the bias current will produce a 10% or 1dB error in gain. This will occur at 42dB below the maximum input level.

It is possible to deviate from the 2-to-1 transfer characteristic at low levels as shown in the circuit of Figure 4. Either R_A or R_B, (but not both), is required. The voltage on C_{RECT} is $2 \times V_{BE}$ plus V_{IN} avg. For low level inputs V_{IN} avg is negligible, so we can assume 1.3V as the bias on C_{RECT}. If R_A is placed from C_{RECT} to AND we will bleed off a current

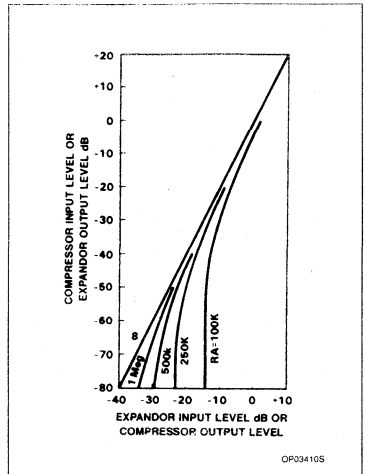


Figure 5. Mistracking With R_A

$I = 1.3V/R_A$. If the rectifier average input current is less than this value, there will be no gain control input to the ΔG cell so that its gain will be zero and the expandor output will be zero. As the input level is raised, the input current will exceed $1.3V/R_A$ and the expandor output will become active. For large input signals, R_A will have little effect. The result of this is that we will deviate from the 2-to-1 expansion, present at high levels, to an infinite expansion at low levels where the output shuts off completely. Figure 5 shows some examples of tracking curves which can be obtained. Complementary curves would be obtained for a compressor, where at low level signals the result would be infinite compression. The bleed current through R_A will be a function of temperature because of the two V_{BE} drops, so the low level tracking will drift with temperature. If a negative supply is available, if would be desirable to tie R_A to that, rather than ground, and to increase its value accordingly. The bleed current will then be less sensitive to the V_{BE} temperature drift.

R_B will supply an extra current to the rectifier equal to $(V_{CC} - 1.3V)R_B$. In this case, the expandor transfer characteristic will deviate towards 1-to-1 at low levels. At low levels the expandor gain will stop dropping and the expansion will cease. In a compressor, this would lead to a lack of compression at low levels. Figure 6 shows some typical transfer curves. An R_B value of approximately 2.5M would trim the low level tracking so as to match the Bell system N2 trunk compandor characteristic.

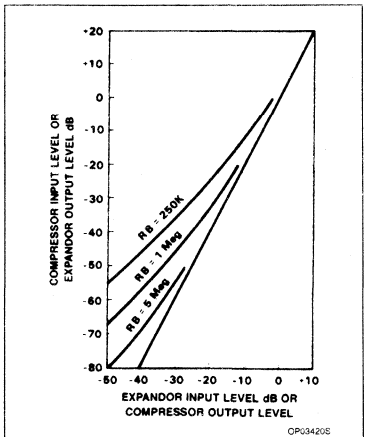


Figure 6. Mistracking With R_B

RECTIFIER BIAS CURRENT CANCELLATION

The rectifier has an input bias current of between 50 and 100nA. This limits the dynamic range of the rectifier to about 60dB. It also limits the amount of attenuation of the ΔG cell. The rectifier dynamic range may be increased by about 20dB by the bias current trim network shown in Figure 7. Figure 8 shows the rectifier performance with and without bias current cancellation.

ATTACK AND DECAY TIME

The attack and decay times of the compandor are determined by the rectifier filter time constant $10k \times C_{RECT}$. Figure 9 shows how the gain will change when the input signal undergoes a 10, 20, or 30dB change in level.

The attack time is much faster than the decay, which is desirable in most applications. Figure 10 shows the compressor attack envelope for a +12dB step in input level. The initial output level of 1 unit instantaneously rises to 4 units, and then starts to fall towards

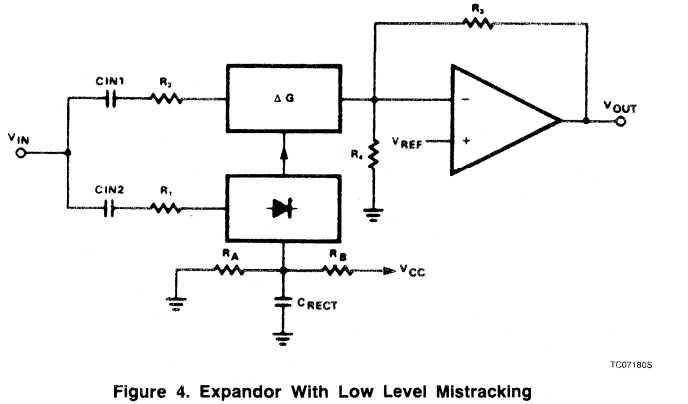


Figure 4. Expandor With Low Level Mistracking

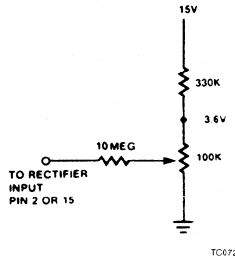


Figure 7. Rectifier Bias Current Compensation

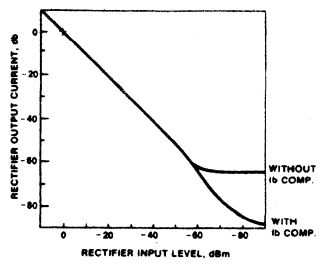


Figure 8. Rectifier Performance With Bias Current Compensation

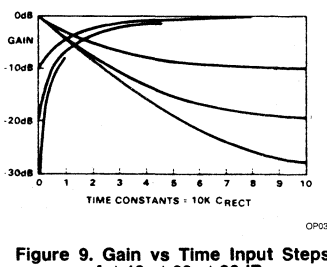


Figure 9. Gain vs Time Input Steps of ± 10, ± 20, ± 30dB

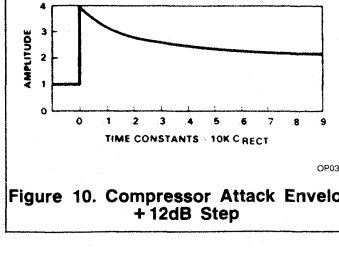


Figure 10. Compressor Attack Envelope +12dB Step

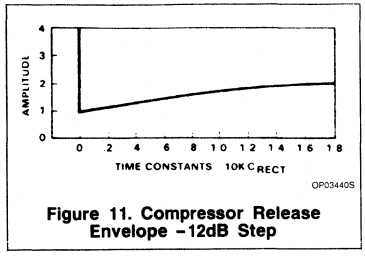


Figure 11. Compressor Release Envelope -12dB Step

its final value of 2 units. The CCITT recommendation on attack and decay times for telephone system compandors defines the attack time as when the envelope has fallen to a level of 3 units, corresponding to t = 0.15 in the figure. The CCITT recommends an attack time of 3 ± 2ms, which suggests an RC product of 20ms. Figure 11 shows the compressor output envelope when the input level is suddenly reduced 12dB. The output, initially at a level of 4 units, drops 12dB to 1 unit and then rises to its final value of 2 units. The CCITT defines release time as when the output has risen to 1.5 units, and suggests a value of 13.5 ± 9ms. This corresponds to t = 0.675 in the figure, which again suggests a 20ms RC product. Since R_1 = 10k, the CCITT recommendations will be met if C_{RECT} = 2μF.

There is a trade-off between fast response and low distortion. If a small C_{RECT} is used to get very fast attack and decay, some ripple will appear on the gain control line and produce distortion. As a rule, a 1μF C_{RECT} will produce 0.2% distortion at 1kHz. The distortion is inversely proportional to both frequency and capacitance. Thus, for telephone applications where C_{RECT} = 2μF, the ripple would cause 0.1% distortion at 1kHz and 0.33% at 800Hz. The low frequency distortion generated by a compressor would be cancelled (or undistorted) by an expandor, providing that they have the same value of C_{RECT}.

FAST ATTACK, SLOW RELEASE HARD LIMITER

The NE570/571 can be easily used to make an excellent limiter. Figure 12 shows a typical circuit which requires ½ of an NE570/571, ½ of an LM339 quad comparator, and a PNP transistor. For small signals, the ΔG cell is nearly off, and the circuit runs at unity gain as set by R_8, R_7. When the output signal tries to exceed a + or −1V peak, a comparator threshold is exceeded. The PNP is turned on and rapidly charges C_4 which activates the ΔG cell. Negative feedback through the ΔG cell reduces the gain and the output signal level. The attack time is set by the RC product of R_{18} and C_4, and the release time is determined by C_4 and the internal rectifier resistor, which is 10k. The circuit shown attacks in less than 1ms and has a release time constant of 100ms. R_9 trickles about 0.7μA through the rectifier to prevent C_4 from becoming completely discharged. The gain cell is activated when the voltage on Pin 1 or 16 exceeds two diode drops. If C_4 were allowed to become completely discharged, there would be a slight delay before it recharged to > 1.2V and activated limiting action.

A stereo limiter can be built out of 1 NE570/571, 1 LM339 and two PNP transistors. The resistor networks R_{12}, R_{13} and R_{14}, R_{15}, which set the limiting thresholds, could be common between channels. To gang the stereo channels together (limiting in one channel will produce a corresponding gain change in the second channel to maintain the balance of the stereo image), then Pins 1 and 16 should be jumpered together. The outputs of all 4 comparators may then be tied together, and only one PNP transistor and one capacitor C_4 need be used. The release time will then be the product 5k × C_4 since two channels are being supplied current from C_4.

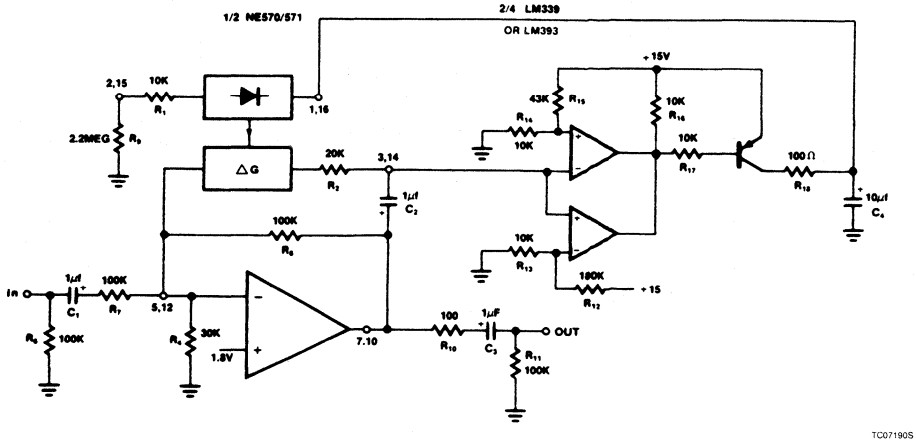
USE OF EXTERNAL OP AMP

The operational amplifiers in the NE570/571 are not adequate for some applications. The slew rate, bandwidth, noise, and output drive capability can limit performance in many systems. For best performance, an external op amp can be used. The external op amp may be powered by bipolar supplies for a larger output swing.

Figure 13 shows how an external op amp may be connected. The non-inverting input must be biased at about 1.8V. This is easily accomplished by tying it to either Pin 8 or 9, the THD trim pins, since these pins sit at 1.8V. An optional RC decoupling network is shown which will filter out the noise from the NE570/571 reference (typically about 10μV in 20kHz BW). The inverting input of the external op amp is tied to the inverting input of the internal op amp. The output of the external op amp is then used, with the internal op amp output left to float. If the external op amp is used single supply (+V_{CC} and ground), it must have an input common-mode range down to less than 1.8V.

N2 COMPANDOR

There are four primary considerations involved in the application of the NE570/571 in an N2 compandor. These are matching of input and output levels, accurate 600Ω input and output impedances, conformance to the Bell system low level tracking curve, and proper attack and release times.



+15V Pin 13
GND Pin 4
R_1, R_2, R_4 are internal to the NE570/571.

Figure 12. Fast Attack, Slow Release Hard Limiter

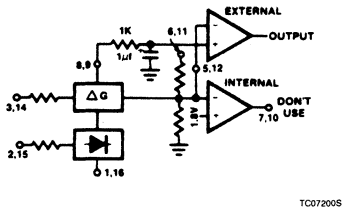


Figure 13. Use of External Op Amp

Figure 14 shows the implementation of an N2 compressor. The input level of $0.245V_{RMS}$ is stepped up to $1.41V_{RMS}$ by the 600Ω: 20kΩ matching transformer. The 20k input resistor properly terminates the transformer. An internal 20kΩ resistor (R_3) is provided, but for accurate impedance termination an external resistor should be used. The output impedance is provided by the 4kΩ output resistor and the 4kΩ: 600Ω output transformer. The $0.275V_{RMS}$ output level requires a 1.4V op amp output level. This can be provided by increasing the value of R_2 with an external resistor, which can be selected to fine trim the gain. A rearrangement of the compressor gain equation (6) allows us to determine the value for R_2.

$$R_2 = \frac{\text{Gain}^2 \times 2\ R_3\ V_{IN\ avg}}{R_1\ I_B}$$

$$= \frac{1^2 \times 2 \times 20k \times 1.27}{10k \times 140\mu A}$$

$$= 36.3k$$

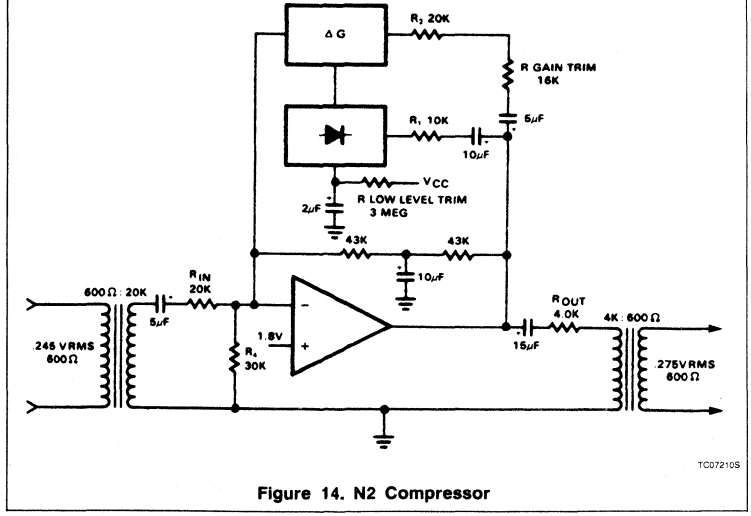


Figure 14. N2 Compressor

The external resistance required will thus be 36.3k – 20k = 16.3k.

The Bell-compatible low level tracking characteristic is provided by the low level trim resistor from C_{RECT} to V_{CC}. As shown in Figure 6, this will skew the system to a 1:1 transfer characteristic at low levels. The 2μF rectifier capacitor provides attack and release times of 3ms and 13.5ms, respectively, as shown in Figures 10 and 11. The R-C-R network around the op amp provides DC feedback to bias the output at DC.

An N2 expandor is shown in Figure 15. The input level of $3.27V_{RMS}$ is stepped down to 1.33V by the 600Ω:100Ω transformer, which is terminated with a 100Ω resistor for accurate impedance matching. The output impedance is accurately set by the 150Ω output resistor and the 150Ω:600Ω output transformer. With this configuration, the 3.46V transformer output requires a 3.46V op amp

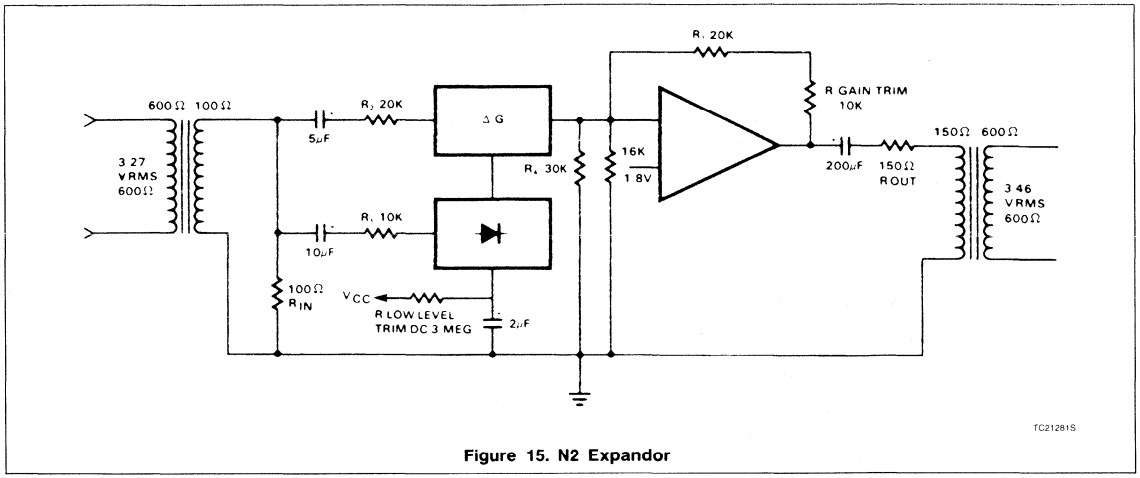


Figure 15. N2 Expandor

output. To obtain this output level, it is necessary to increase the value of R_3 with an external trim resistor. The new value of R_3 can be found with the expandor gain equation

$$R_3 = \frac{R_1\ R_2\ I_B\ \text{Gain}}{2\ V_{IN}\ \text{avg}}$$

$$= \frac{10k \times 20k \times 140\mu A \times 2.6}{2 \times 1.20}$$

$$= 30.3k$$

An external addition to R_3 of 10k is required, and this value can be selected to accurately set the high level gain.

A low level trim resistor from C_{RECT} to V_{CC} of about 3M provides matching of the Bell low-level tracking curve, and the 2μF value of C_{RECT} provides the proper attack and release times. A 16k resistor from the summing node to ground biases the output to $7V_{DC}$.

VOLTAGE-CONTROLLED ATTENUATOR

The variable gain cell in the NE570/571 may be used as the heart of a high quality voltage-controlled amplifier (VCA). Figure 16 shows a typical circuit which uses an external op amp for better performance, and an exponential converter to get a control characteristic of −6dB/V. Trim networks are shown to null out distortion and DC shift, and to fine trim gain to 0dB with 0V of control voltage.

Op amp A_2 and transistors Q_1 and Q_2 form the exponential converter generating an exponential gain control current, which is fed into the rectifier. A reference current of 150μA, (15V and R_{20} = 100k), is attenuated a factor of two (6dB) for every volt increase in the control voltage. Capacitor C_6 slows down gain changes to a 20ms time constant ($C_6 \times R_1$) so that an abrupt change in the control voltage will produce a smooth sounding gain change. R_{18} assures that for large control voltages the circuit will go to full attenuation. The rectifier bias current would normally limit the gain reduction to about 70dB. R_{18} draws excess current out of the rectifier. After approximately 50dB of attenuation at a −6dB/V slope, the slope steepens and attenuation becomes much more rapid until the circuit totally shuts off at about 9V of control voltage. A_1 should be a low noise high slew rate op amp. R_{13} and R_{14} establish approximately a 0V bias at A_1's output.

With a 0V control voltage, R_{19} should be adjusted for 0dB gain. At 1V(−6dB gain) R_9 should be adjusted for minimum distortion with a large (+10dBm) input signal. The output DC bias (A_1 output) should be measured at full attenuation (+10V control voltage) and then R_8 is adjusted to give the same value at 0dB gain. Properly adjusted, the circuit will give typically less than 0.1% distortion at any gain with a DC output voltage variation of only a few millivolts. The clipping level (140μA into Pin 3, 14) is ± 10V peak. A signal-to-noise ratio of 90dB can be obtained.

If several VCAs must track each other, a common exponential converter can be used. Transistors can simply be added in parallel with Q_2 to control the other channels. The transistors should be maintained at the same temperature for best tracking.

AUTOMATIC LEVEL CONTROL

The NE570 can be used to make a very high performance ALC as shown in Figure 17. This circuit hook-up is very similar to the basic compressor shown in Figure 2 except that the rectifier input is tied to the input rather than the output. This makes gain inversely proportional to input level so that a 20dB drop in input level will produce a 20dB increase in gain. The output will remain fixed at a constant level. As shown, the circuit will maintain an output level of ± 1dB for an input range of +14 to −43dB at 1kHz. Additional external components will allow the output level to be adjusted. Some relevant design equations are:

$$\text{Output level} = \frac{R_1\ R_2\ I_B}{2\ R_3}\left(\frac{V_{IN}}{V_{IN}\ (\text{avg})}\right);$$

$$I_B = 140\mu A$$

$$\text{Gain} = \frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (\text{avg})} \text{ where}$$

$$\frac{V_{IN}}{V_{IN}\ (\text{avg})} = \frac{\pi}{2\sqrt{2}} = 1.11 \text{ (for sine wave)}$$

If ALC action at very low input levels is not desired, the addition of resistor R_X will limit the maximum gain of the circuit.

$$\text{Gain max} = \frac{\frac{R_1 + R_X}{1.8V} \times R_2 \times I_B}{2\ R_3}$$

The time constant of the circuit is determined by the rectifier capacitor, C_{RECT}, and an internal 10k resistor.

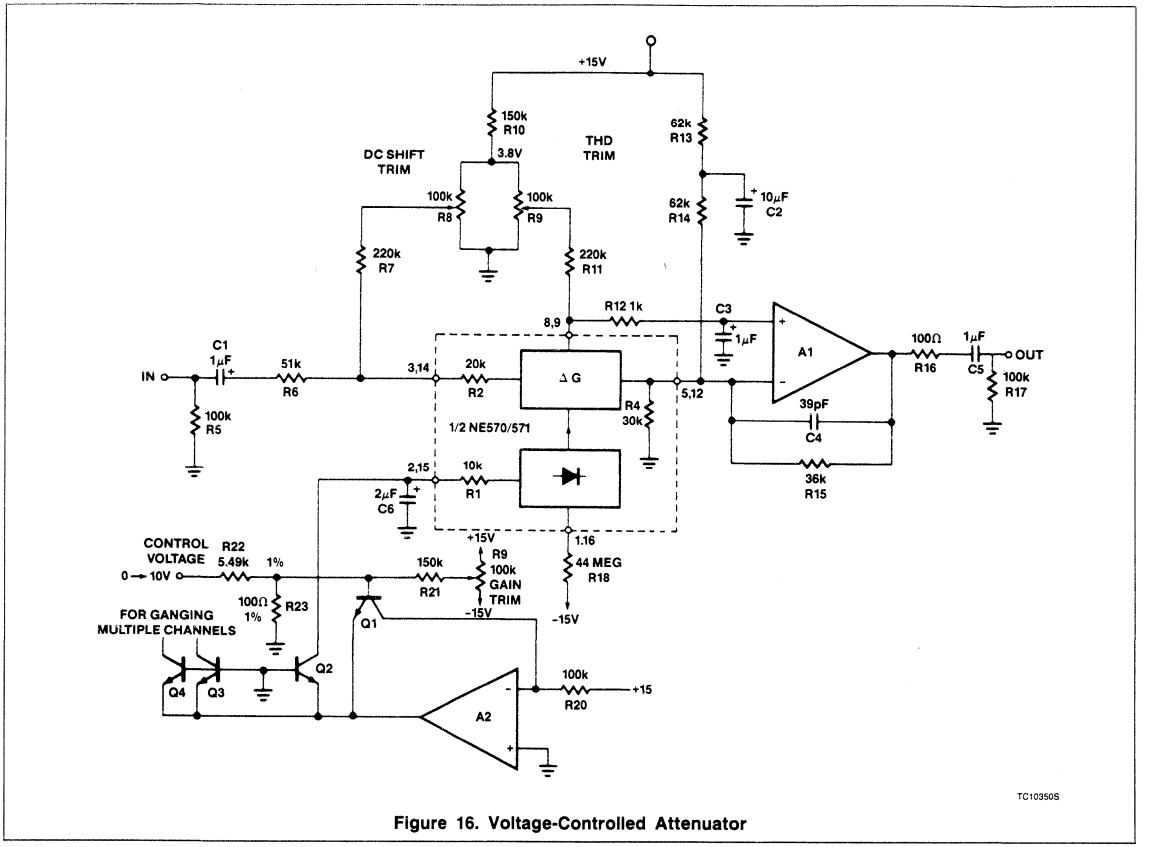


Figure 16. Voltage-Controlled Attenuator

$\tau = 10k\ C_{RECT}$

Response time can be made faster at the expense of distortion. Distortion can be approximated by the equation:

$$THD = \left(\frac{1\mu F}{C_{RECT}}\right)\left(\frac{1kHz}{freq.}\right) \times 0.2\%$$

VARIABLE SLOPE COMPRESSOR-EXPANDOR

Compression and expansion ratios other than 2:1 can be achieved by the circuit shown in Figure 18. Rotation of the dual potentiometer causes the circuit hook-up to change from a basic compressor to a basic expandor. In the center of rotation, the circuit is 1:1, has neither compression nor expansion. The (input) output transfer characteristic is thus continuously variable from 2:1 compression, through 1:1 up to 1:2 expansion. If a fixed compression or expansion ratio is desired, proper selection of fixed resistors can be used instead of the potentiometer. The optional threshold resistor will make the compression or expansion ratio deviate towards 1:1 at low levels. A wide variety of (input) output characteristics can be created with this circuit, some of which are shown in Figure 18.

HI-FI COMPANDOR

The NE570 can be used to construct a high performance compandor suitable for use with music. This type of system can be used for noise reduction in tape recorders, transmission systems, bucket brigade delay lines, and digital audio systems. The circuits to be described contain features which improve performance, but are not required for all applications.

A major problem with the simple NE570 compressor (Figure 2) is the limited op amp gain at high frequencies. For weak input signals, the compressor circuit operates at high gain and the 570 op amp simply runs out of loop gain. Another problem with the 570 op amp is its limited slew rate of about 0.6V/μs. This is a limitation of the expandor, since the expandor is more likely to produce large output signals than a compressor.

Figure 20 is a circuit for a high fidelity compressor which uses an external op amp and has a high gain and wide bandwidth. An input compensation network is required for stability.

Another feature of the circuit in Figure 20 is that the rectifier capacitor (C_9) is not grounded, but is tied to the output of an op amp circuit. This circuit, built around an LM324, speeds up the compressor attack time at low signal levels. The response times of the simple expandor and compressor (Figures 1 and 2) become longer at low signal levels. The time constant is not simply $10k \times C_{RECT}$, but is really:

$$\left(10k + 2\left(\frac{0.026V}{I_{RECT}}\right)\right) \times C_{RECT}$$

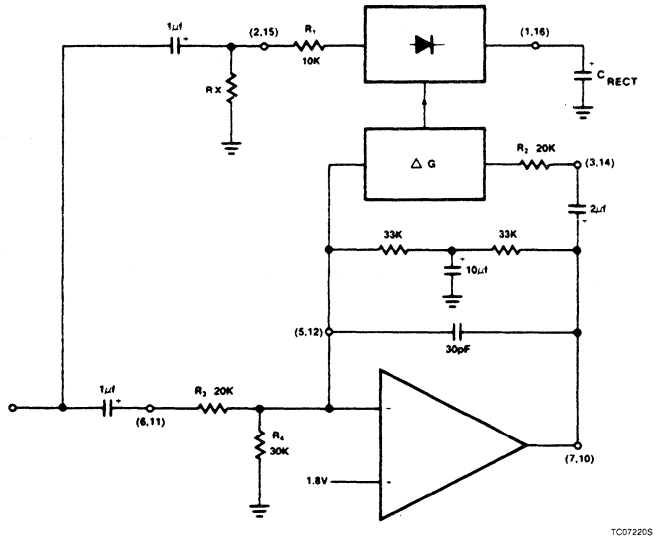


Figure 17. Automatic Level Control

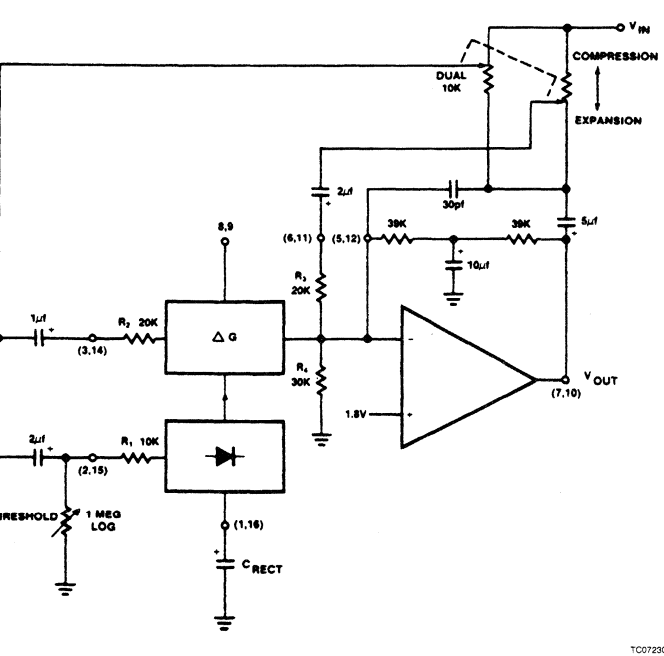


Figure 18. Variable Slope Compressor-Expandor

When the rectifier input level drops from 0dBm to −30dBm, the time constant increases from $10.7k \times C_{RECT}$ to $32.6k \times C_{RECT}$. In systems where there is unity gain between the compressor and expandor, this will cause no overall error. Gain or loss between the compressor and expandor will be a mistracking of low signal dynamics. The circuit with the LM324 will greatly reduce this problem for systems which cannot guarantee the unity gain.

When a compressor is operating at high gain, (small input signal), and is suddenly hit with a signal, it will overload until it can reduce its gain. Overloaded, the output will attempt to swing rail to rail. This compressor is limited to approximately a $7V_{P-P}$ output swing by the brute force clamp diodes D_3 and D_4. The diodes cannot be placed in the feedback loop because their capacitance would limit high frequency gain. The purpose of limiting the output swing is to avoid overloading any succeeding circuit such as a tape recorder input.

The time it takes for the compressor to recover from overload is determined by the rectifier capacitor C_9. A smaller capacitor will allow faster response to transients, but will produce more low frequency third harmonic distortion due to gain modulation. A value of 1μF seems to be a good compromise value and yields good subjective results. Of course, the expandor should have exactly the same value rectifier capacitor for proper transient response. Systems which have good low frequency amplitude and phase response can use compandors with smaller rectifier capacitors, since the third harmonic distortion which is generated by the compressor will be undistorted by the expandor.

Simple compandor systems are subject to a problem known as breathing. As the system

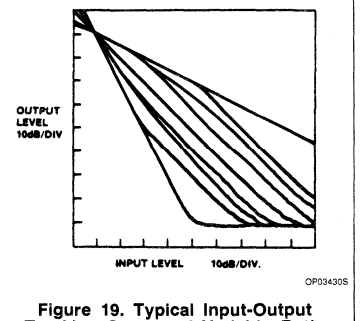


Figure 19. Typical Input-Output Tracking Curves of Variable Ratio Compressor-Expandor

is changing gain, the change in the background noise level can sometimes be heard.

The compressor in Figure 20 contains a high frequency pre-emphasis circuit (C_2, R_5 and C_8, R_{14}), which helps solve this problem. Matching de-emphasis on the expandor is required. More complex designs could make the pre-emphasis variable and further reduce breathing.

The expandor to complement the compressor is shown in Figure 21. Here an external op amp is used for high slew rate. Both the compressor and expandor have unity gain levels of 0dB. Trim networks are shown for distortion (THD) and DC shift. The distortion trim should be done first, with an input of 0dB at 10kHz. The DC shift should be adjusted for minimum envelope bounce with tone bursts. When applied to consumer tape recorders, the subjective performance of this system is excellent.

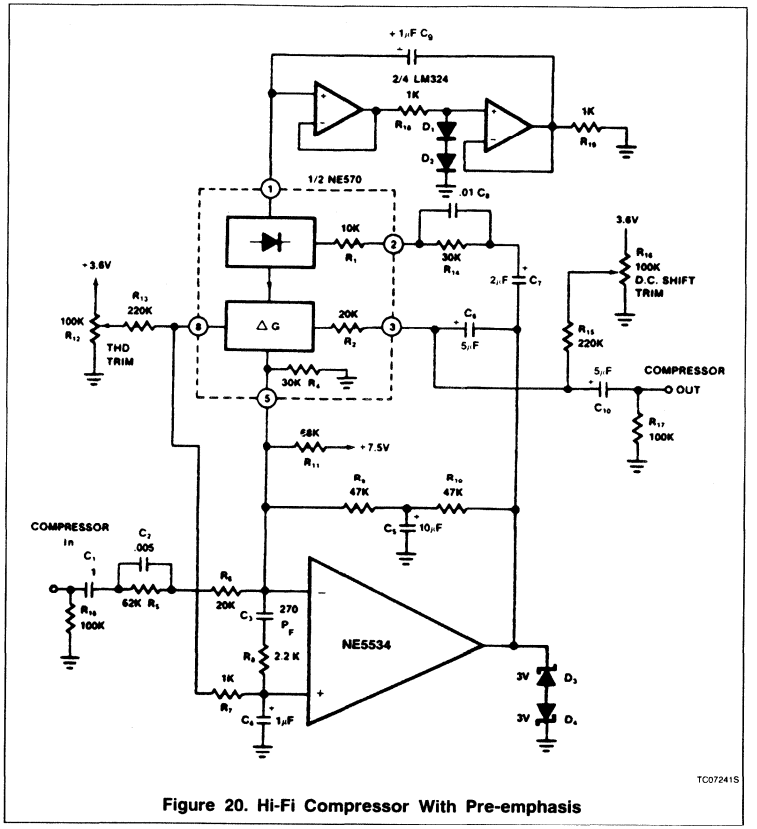


Figure 20. Hi-Fi Compressor With Pre-emphasis

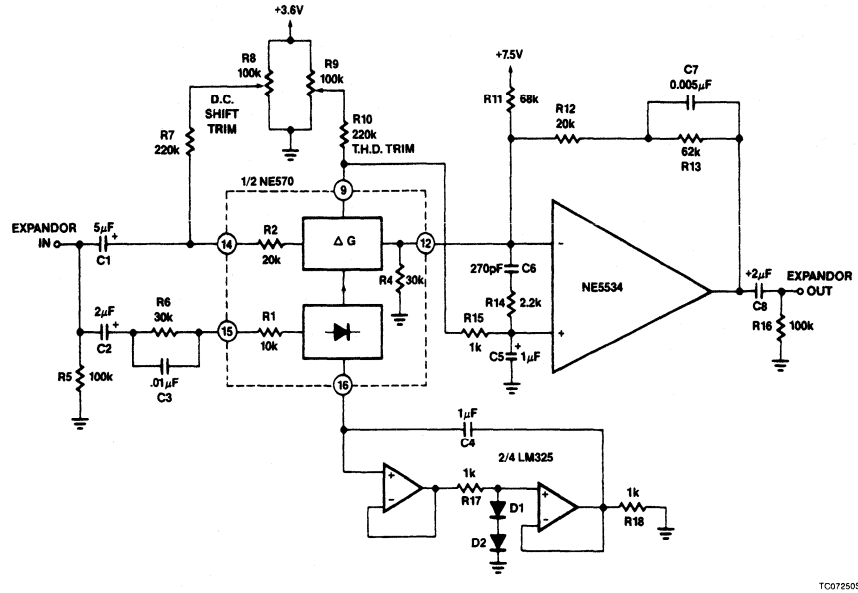
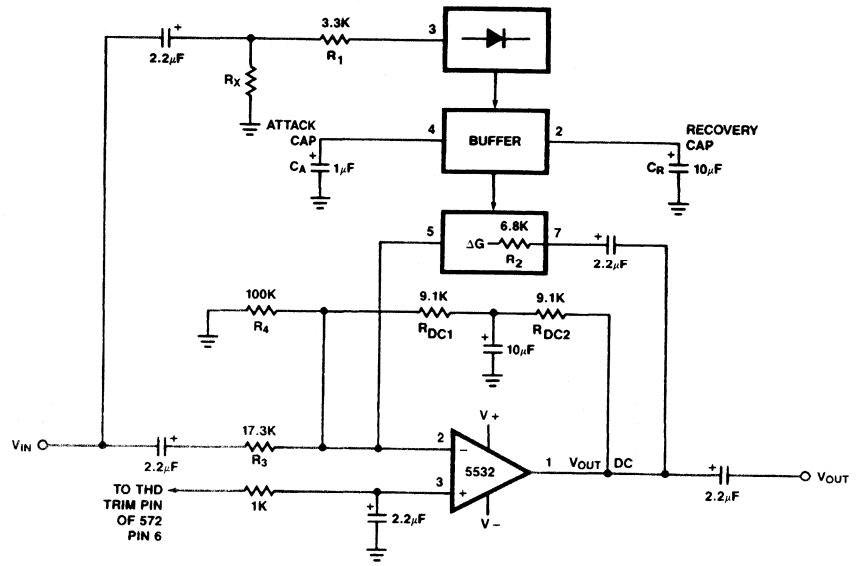


Figure 21. Hi-Fi Expandor With De-emphasis

AN175
Automatic Level Control Using the NE572

Application Note

NE572 AUTOMATIC LEVEL CONTROL



$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right)$$

WHERE: $R_4 = 100k$
$R_{DC1} = R_{DC2} = 9.1k$
$V_{REF} = 2.5V$

$$\text{OUTPUT LEVEL} = \left(\frac{R_1 R_2 I_B}{2R_3}\right)\left(\frac{V_{IN}}{V_{IN(avg)}}\right)$$

$$\text{GAIN} = \frac{R_1 R_2 I_B}{2R_3 V_{IN}\ (avg)}$$

WHERE: $R_1 = 6.8k$ (Internal)
$R_2 = 3.3k$
$R_3 = 17.3k$
$I_B = 140\mu A$

ATTACK TIME = (10k) C_A

RECOVERY TIME = (10k) C_R

TO LIMIT THE GAIN AT VERY LOW INPUT LEVELS, ADD R_X:

$$\text{GAIN MAX.} = \frac{\frac{R_1 + R_X}{2.5V} \times R_2 \times I_B}{2R_3}$$

$$\frac{V_{IN}}{V_{IN(avg)}} = \frac{\pi}{2\sqrt{2}} = 1.11$$
(FOR SINE WAVES)

NOTE:
Pin numbers are for side A of the NE572.

DATA COMMUNICATIONS

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Line drivers/receivers 1423

Modems 1467

Data transmission 1523

Line drivers/receivers

		page
AM26LS30	dual differential RS-422 party-line/quad single-ended RS-423 line driver	1425
AM26LS31	quad high-speed differential line driver	1433
AM26LS32	quad high-speed differential line receiver	1439
AM26LS33	quad high-speed differential line receiver	1439
MC1488	quad line driver	1443
MC1489	quad line receiver	1447
MC1489A	quad line receiver	1447
NE5170	octal line driver	1450
NE5180	octal differential line receiver	1457
NE5181	octal differential line receiver	1457
AN113	using MC1488/1489 line drivers and receivers	1463

AM26LS30

Dual Differential RS-422 Party Line/ Quad Single-Ended RS-423 Line Driver

Preliminary Specification

DESCRIPTION

The AM26LS30 is a line driver designed for digital data transmission. A mode control input provides a choice of operation either as two differential line drivers which meet all the requirements of EIA Standard RS-422 or as four independent single-ended RS-423 line drivers.

In the differential mode, the outputs have individual 3-State controls. In the high impedance state, these outputs will not clamp the line over a common mode transmission line voltage of ±10V. A typical full duplex system consists of the AM26LS30 differential line driver and up to twelve AM26LS32 line receivers, or the AM26LS32 line receiver and up to thirty-two AM26LS30 differential drivers.

A slew control pin allows the use of an external capacitor to control slew rate for suppression of near-end cross talk to receivers in the cable.

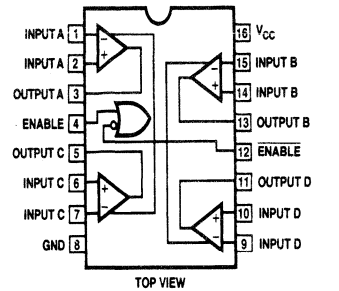
The AM26LS30 is constructed using high speed oxide isolated bipolar processing.

FEATURES

- **Dual RS-422 line driver or quad RS-423 line driver**
- **Driver outputs do not clamp line with power off or in high impedance state**
- **Individual 3-State controls when used in differential mode**
- **Low I_{CC} and I_{EE} power consumption**
  - **RS-422 differential mode: 35mW/driver typ**
  - **RS-423 single-ended mode: 26mW/driver typ**
- **Individual slew rate control for each output**
- **50Ω transmission line drive capability (RS-422 into virtual ground)**
- **Low current PNP inputs compatible with TTL, MOS and CMOS**
- **High capacitive load drive capability**
- **Exact replacement for DS16/3691**
- **High speed oxide isolated bipolar processing**

PIN CONFIGURATION

D, F and N Packages



FUNCTION TABLE

MODE	INPUTS		OUTPUTS	
	A (D)	B (C)	A (D)	B (C)
0	0	0	0	1
0	0	1	Z	Z
0	1	0	1	0
0	1	1	Z	Z
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

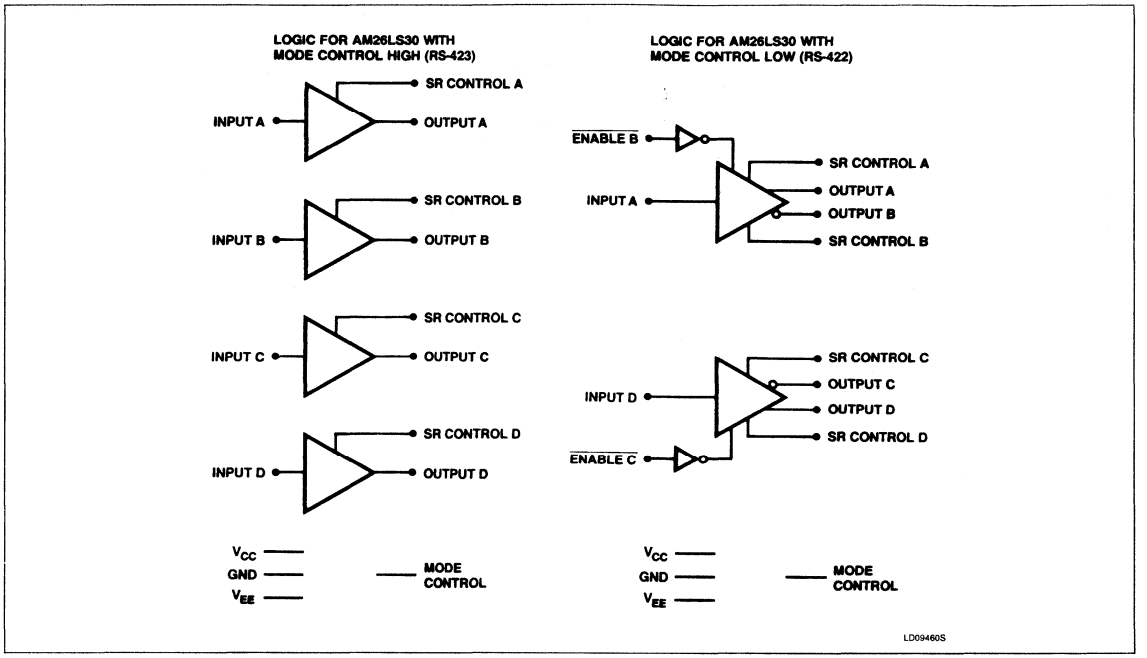
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	AM26LS30CN
16-Pin Plastic SO	0 to +70°C	AM26LS30CD
16-Pin Plastic DIP	-40°C to +85°C	AM26LS30IN
16-Pin Plastic SO	-40°C to +85°C	AM26LS30ID
16-Pin Plastic DIP	-55°C to +125°C	AM26LS30MN
16-Pin Ceramic DIP	-55°C to +125°C	AM26LS30MF

Dual Differential RS-422 Party Line/ Quad Single-Ended RS-423 Line Driver

AM26LS30

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage V+	7	V
V_{EE}	V–	–7	V
V_{IN}	Input voltage	–.5V to V_{CC}	V
V_{OUT}	Output voltage (Power Off)	±13.5	V
P_D	Power dissipation	600	mW
T_A	Ambient temperature range AM26LS31C	0 to +70	°C
	AM26LS31I	–40 to +85	°C
	AM26LS32M	–55 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

POWER DISSIPATION TABLE

PACKAGE	POWER DISSIPATION	DERATING FACTOR	ABOVE T_A
N	1,488mW	11.9mW/°C	25°C
D	1,262mW	10.1mW/°C	25°C
F	1,250mW	10.0mW/°C	25°C

Dual Differential RS-422 Party Line/ Quad Single-Ended RS-423 Line Driver

AM26LS30

DC ELECTRICAL CHARACTERISTICS over the operating temperature range. The following conditions apply unless otherwise specified: AM26LS30M, $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = GND$; AM26LS30C, $T_A = 0$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{EE} = GND$; AM26LS30I, $T_A = -40$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{EE} = GND$ **RS-422 Connection**, Mode Voltage $\leq$ 0.8V.

SYMBOL[2]	PARAMETER	TEST CONDITIONS[3]		LIMITS			UNITS
				Min	Typ[1]	Max	
V_O	Differential output	$R_L = \infty$	$V_{IN} = 2.0V$		3.6	6.0	V
$\overline{V_O}$	Voltage, $V_{A, B}$		$V_{IN} = 0.8V$		−3.6	−6.0	V
V_T	Differential output	$R_L = 100\Omega$	$V_{IN} = 2.0V$	2.0	2.4		V
$\overline{V_T}$	Voltage, $V_{A, B}$		$V_{IN} = 0.8V$	−2.0	−2.4		V
V_{OS} , $\overline{V_{OS}}$	Common mode offset voltage	$R_L = 100\Omega$			2.5	0.4	V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in differential output voltage	$R_L = 100\Omega$			0.005	0.4	V
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in common mode offset voltage	$R_L = 100\Omega$			0.005	3.0	V
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	$R_L = 100\Omega$		4.0	4.8		V
V_{CMR}	Output voltage common mode range	$V_{\overline{ENABLE}} = 2.4V$		±10			V
I_{XA}	Output leakage	$V_{CC} = 0V$	$V_{CMR} = 10V$			20	μA
I_{XB}	current		$V_{CMR} = -10V$			−20	μA
I_{OX}	Off state (high Z)	$V_{CC} = Max$	$V_{CMR} \leq 10V$			20	μA
	output current		$V_{CMR} > -10V$			−20	μA
I_{SA}, I_{SB}	Output short circuit	$V_{IN} = 2.4V$	$V_{OA} = 0V$		−80	−150	mA
	current		$V_{OB} = 6V$		80	150	mA
		$V_{IN} = 0.4V$	$V_{OA} = 6V$		80	150	mA
			$V_{OB} = 0V$		−80	−150	mA
I_{CC}	Supply current				18	30	mA
V_{IH}	High level input voltage			2.0			V
V_{IL}	Low level input voltage					0.8	V
I_{IH}	High level input current	$V_{IN} = 2.4V$			1.0	40	μA
		$V_{IN} \leq V_{CC}$			10	100	μA
I_{IL}	Low level input current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input clamp voltage	$I_{IN} = -12mA$				−1.5	V

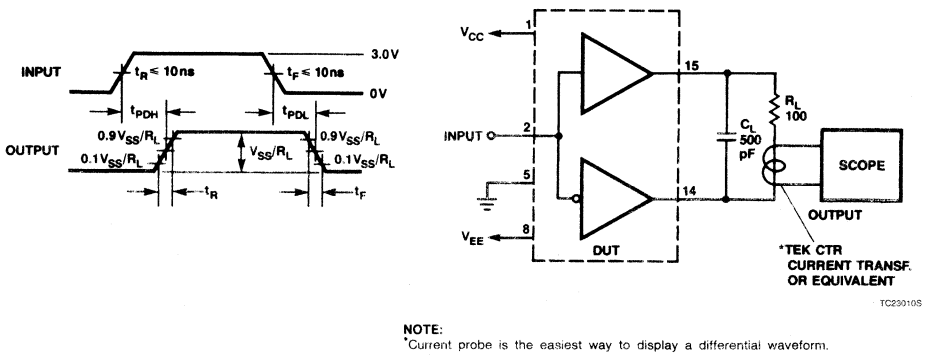
Dual Differential RS-422 Party Line/ Quad Single-Ended RS-423 Line Driver

AM26LS30

AC ELECTRICAL CHARACTERISTICS EIA RS-422 Connection, V_{CC} = 5.0V, V_{EE} = GND, Mode = 0.4V, T_A = 25°C.

SYMBOL[2]	PARAMETER	TEST CONDITIONS[3]	LIMITS			UNIT
			Min	Typ[1]	Max	
t_r	Rise time	R_L = 100Ω, C_L = 500pF, Figure 1		120	200	ns
t_f	Fall time	R_L = 100Ω, C_L = 500pF, Figure 1		120	200	ns
t_{PDH}	Output propagation delay	R_L = 100Ω, C_L = 500pF, Figure 1		120	200	ns
t_{PDL}	Output propagation delay	R_L = 100Ω, C_L = 500pF, Figure 1		120	200	ns
t_{PLZ}	Output enable to output	R_L = 450Ω, C_L = 500pF, Figure 2		180	300	ns
t_{PHZ}				250	350	ns
t_{PZL}	Output enable to output	R_L = 450Ω, C_L = 500pF, Figure 2		250	350	ns
t_{PZH}				180	300	ns

NOTES:
1. Typical limits are at V_{CC} = 5V, V_{EE} = GND, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-422 where applicable.
3. RL connected between each output and its complement.



NOTE:
*Current probe is the easiest way to display a differential waveform.

Figure 1. Switching Time Waveforms and AC Test Circuits for EIA RS-422 Connection

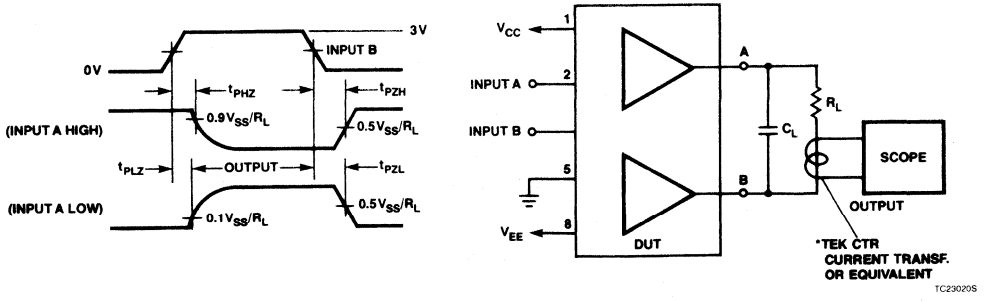


Figure 2. 3-State Delays

Dual Differential RS-422 Party Line/ Quad Single-Ended RS-423 Line Driver

AM26LS30

DC ELECTRICAL CHARACTERISTICS

over the operating temperature range. The following conditions apply unless otherwise specified: AM26LS30 $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = -5.0V \pm 10\%$; AM26LS30 $T_A = 0$ to $+70°C$, $V_{CC} = 5.0V \pm 5.0\%$, $V_{EE} = -5.0V \pm \%5$; **RS-423 Connection**, Mode Voltage $\geq 2.0V$.

SYMBOL[2]	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ[1]	Max	
V_O	Output voltage	$R_L = \infty$ Note 3	$V_{IN} = 2.4V$	4.0	4.4	6.0	V
$\overline{V_O}$		$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert = 4.75V$	$V_{IN} = 0.4V$	-4.0	-4.4	-6.0	V
V_T	Output voltage	$R_L = 450\Omega$	$V_{IN} = 2.4V$	3.6	4.1		V
$\overline{V_T}$		$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert = 4.75V$	$V_{IN} = 0.4V$	-3.6	-4.1		V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Output unbalance	$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$, $R_L = 450\Omega$			0.02	0.4	V
I_{X+}	Output leakage power off	$V_{CC} = V_{EE} = 0V$	$V_O = 6V$		2.0	20	μA
I_{X-}			$V_O = -6V$		-2.0	-20	μA
I_{S+}	Output short circuit current	$V_O = 0V$	$V_{IN} = 2.4V$		-80	-150	mA
I_{S-}			$V_{IN} = 0.4V$		80	150	mA
I_{SLEW}	Slew control current	$V_{SLEW} = V_{EE} + 0.9V$			±140		μA
I_{CC}	Positive supply current	$V_{IN} = 0.4V$, $R_L = \infty$			18	30	mA
I_{EE}	Negative supply current	$V_{IN} = 0.4V$, $R_L = \infty$			-10	-22	mA
V_{IH}	High level input voltage			2.0			V
V_{IL}	Low level input voltage					0.8	V
I_{IH}	High level input current		$V_{IN} = 2.4V$		1.0	40	μA
			$V_{IN} \leq V_{CC}$		10	100	μA
I_{IL}	Low level input current	$V_{IN} = 0.4V$			=nl30	-200	μA
V_I	Input clamp voltage	$I_{IN} = -12mA$				-1.5	V

AC ELECTRICAL CHARACTERISTICS

EIA RS-423 Connection, $V_{CC} = 5.0V$, $V_{EE} = -5V$, Mode = 2.4V, $T_A = 25°C$.

SYMBOL[2]	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ[1]	Max	
t_r	Rise time	$R_L = 450\Omega$, $C_L = 500pF$	$C_C = 0pF$		120	300	ns
		Figure 3	$C_C = 50pF$		3.0		μs
t_f	Fall time	$R_L = 450\Omega$, $C_L = 500pF$	$C_C = 0pF$		120	300	ns
		Figure 3	$C_C = 50pF$		3.0		μs
S_{RC}	Slew rate coefficient	$R_L = 450\Omega$, $C_L = 500pF$, Figure 3			0.06		μs/pF
t_{PDH}	Output propagation delay	$R_L = 450\Omega$, $C_L = 500pF$, Figure 3 $C_C = 0pF$			180	300	ns
t_{PDL}	Output propagation delay	$R_L = 450\Omega$, $C_L = 500pF$, Figure 3 $C_C = 0pF$			180	300	ns

NOTES:
1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = -5V$, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.
3. Output voltage is +3.9V minimum and -3.9V minimum at -55°C.

Dual Differential RS-422 Party Line/ Quad Single-Ended RS-423 Line Driver

AM26LS30

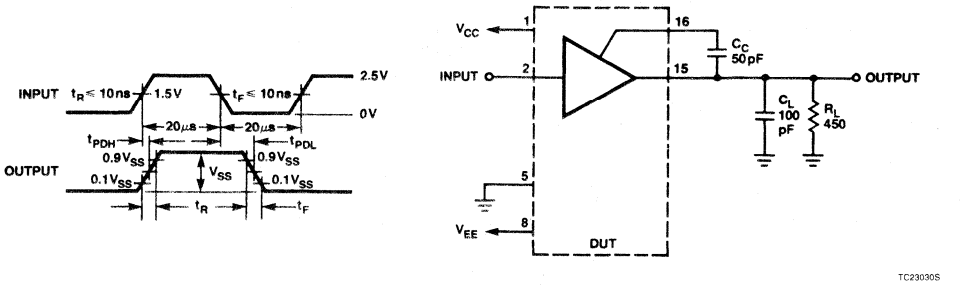


Figure 3. Switching Time Waveforms and AC Test Circuits for EIA RS-423 Connection

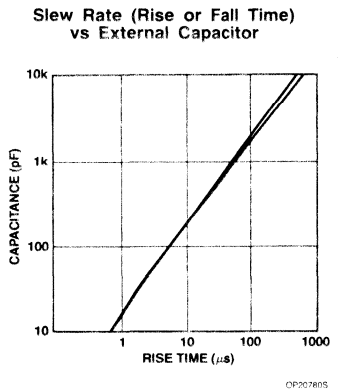


Figure 4

Dual Differential RS-422 Party Line/ Quad Single-Ended RS-423 Line Driver

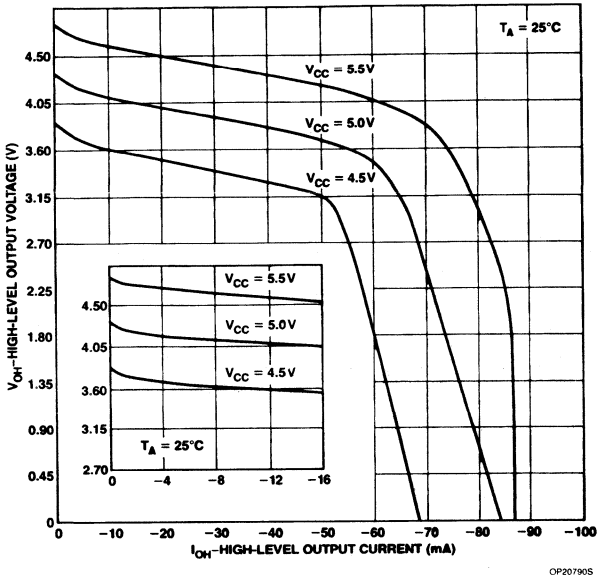


Figure 5

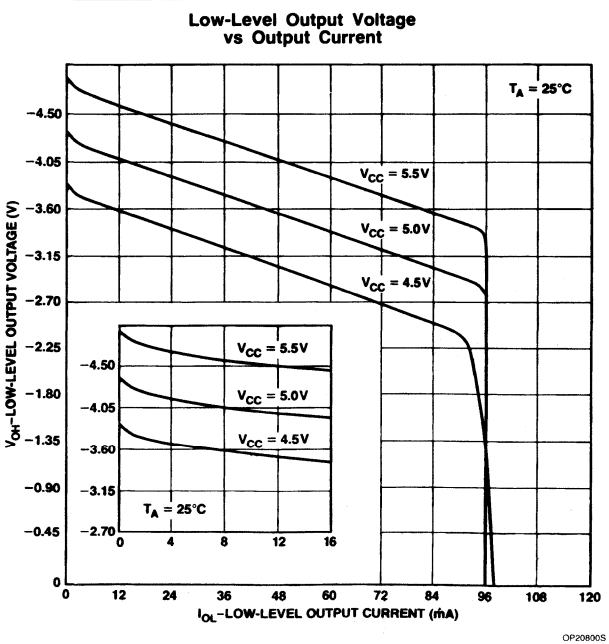


Figure 6

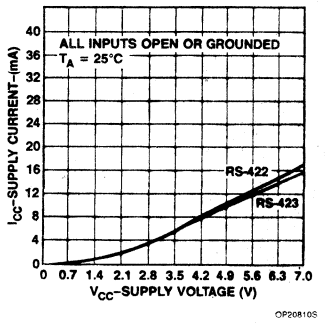

Supply Current
vs Supply Voltage
ALL INPUTS OPEN OR GROUNDED
T_A = 25°C
I_{CC}–SUPPLY CURRENT–(mA)
40
36
32
28
24
20
16
12
8
4
0
RS-422
RS-423
0 0.7 1.4 2.1 2.8 3.5 4.2 4.9 5.6 6.3 7.0
V_{CC}–SUPPLY VOLTAGE (V)
OP20810S

Figure 7

AM26LS31
Quad High-Speed Differential Line Driver

Product Specification

DESCRIPTION

The AM26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The AM26LS31 meets all the requirements of EIA standard RS-422 and Federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines. The circuit provides an enable and disable function common to all four drivers. The AM26LS31 features 3-state outputs and logical ORed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The AM26LS31 is constructed using advanced Low Power Schottky processing.

FEATURES

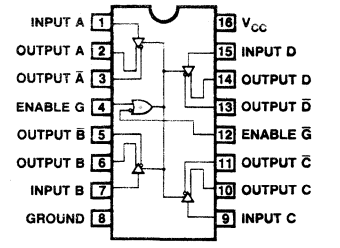
- **Output skew of 2.0ns typical**
- **Input to output delay: 12ns**
- **Operation from single +5V**
- **16-pin DIP and SO packages**
- **Four line drivers in one package**
- **Output short-circuit protection**
- **Complementary outputs**
- **Meets EIA standard RS-422**
- **High output drive capability for 100Ω terminated transmission lines**
- **Available in military and commercial temperature range**
- **Advanced low power Schottky processing**
- **Outputs won't load line when V_{CC} = 0V**

APPLICATIONS

- **Data communications equipment**
- **Computer peripherals**
- **Workstations**
- **Automatic test equipment**

PIN CONFIGURATION

D, F, and N Packages



TOP VIEW

CD14751S

FUNCTION TABLE (Each Driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	A	$\overline{A}$
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

NOTES:
H = High level
L = Low level
X = Irrelevant
Z = High-impedance (OFF)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	AM26LS31CN
16-Pin SO	0 to +70°C	AM26LS31CD
16-Pin Plastic DIP	-40°C to +85°C	AM26LS31IN
16-Pin SO	-40°C to +85°C	AM26LS31ID
16-Pin Cerdip	-55°C to +125°C	AM26LS31MF
16-Pin Plastic DIP	-55°C to +125°C	AM26LS31MN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7	V
V_{IN}	Input voltage	7	V
	Output off-state voltage	5.5	V
T_A	Operating temperature range		
	AM26LS31MF	−55 to +125	°C
	AM26LS31MN	−55 to +125	°C
	AM26LS31IN	−40 to +85	°C
	AM26LS31ID	−40 to +85	°C
	AM26LS31CN	0 to +70	°C
	AM26LS31CD	0 to +70	°C
T_{STG}	Storage temperature range	−55 to +150	°C
T_{SOLD}	Lead temperature (soldering 10sec max.)	300	°C

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
F	1250mW	10mW/°C	25°C
N	1488mW	11.9mW/°C	25°C
D	1126mW	9mW/°C	25°C

DC AND AC ELECTRICAL CHARACTERISTICS

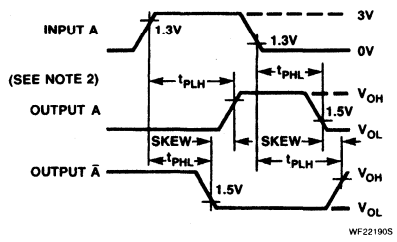
V_{CC} = 5V± 10%, T_A = −55 to +125°C for AM26LS31MF and AM26LS31MN;
V_{CC} = 5V± 5%, T_A = −40 to +85°C for AM26LS31IN and AM26LS31ID;
V_{CC} = 5V± 5%, T_A = 0 to +70°C for AM26LS31CN and AM26LS31CD,
unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
V_{OH}	Output High voltage	V_{CC} = Min., I_{OH} = −20mA	2.5	3.0		V
V_{OL}	Output Low voltage	V_{CC} = Min., I_{OL} = 20mA		0.3	0.5	V
V_{IH}	Input High voltage	V_{CC} = Min.	2.0			V
V_{IL}	Input Low voltage	V_{CC} = Max.			0.8	V
I_{IL}	Input Low current	V_{CC} = Max., V_{IN} = 0.4V		−0.26	−0.36	mA
I_{IH}	Input High current	V_{CC} = Max., V_{IN} = 2.7V		0.001	20	μA
I_I	Input reverse current	V_{CC} = Max., V_{IN} = 7.0V		0.001	0.1	mA
I_O	OFF-state (high-impedance) output current	V_{CC} = Max., V_O = 5.5V V_O = 0.5V		0.6 −0.050	20 −20	μA μA
V_I	Input clamp voltage	V_{CC} = Min., I_{IN} = −18mA		−0.8	−1.5	V
I_{SC}	Output short-circuit current	V_{CC} = Max.	−30		−150	mA
I_{CC}	Power supply current	V_{CC} = Max; all outputs disabled		40	80	mA
t_{PLH}	Input to output	T_A = 25°C, load[2]		9	20	ns
t_{PHL}	Input to output	T_A = 25°C, load[2]		9	20	ns
SKEW	Output to output	T_A = 25°C, load[2]		2	6	ns
t_{LZ}	Enable to output	T_A = 25°C, C_L = 10pF		17	35	ns
t_{HZ}	Enable to output	T_A = 25°C, C_L = 10pF		12	30	ns
t_{ZL}	Enable to output	T_A = 25°C, load[2]		14	45	ns
t_{ZH}	Enable to output	T_A=25°C, load[2]		12	40	ns

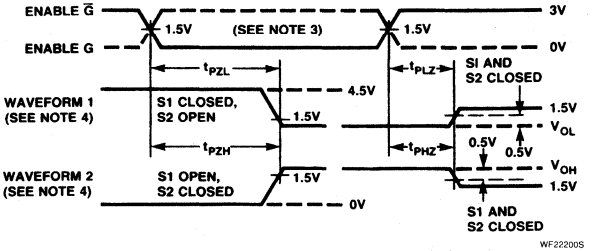
NOTES:
1. All typical values are T_A = +25°C; V_{CC} = 5.0V.
2. C_L = 30pF; V_{IN} = 1.3V to V_{OUT} = 1.3V; V_{PULSE} = 0V to 3.0V.

TIMING DIAGRAMS

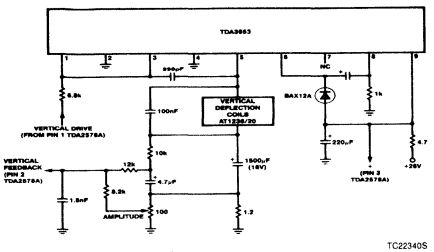
PARAMETER MEASUREMENT INFORMATION



Propagation Delay Times and Skew



Enable and Disable Times



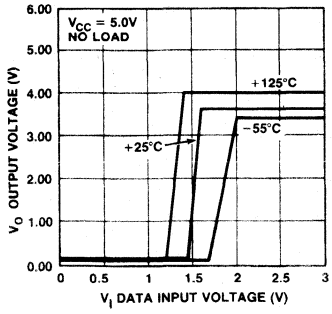
Test Circuit

NOTES:

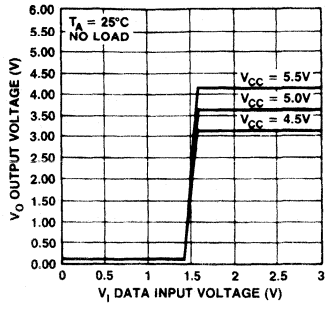
1. All pauses are supplied by generators having the following characteristics: PRR ⩽ 1MHz, Z_{OUT} = 50Ω, 1R ⩽ 15ns, 1F ⩽ 6ns
2. When measuring propagation delay times and skew, switches S1 and S2 are open.
3. Each enable is tested separately.
4. Waveform 1 is for an output with internal condition such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
5. C_L includes probe and jig capacitance.

TYPICAL PERFORMANCE CHARACTERISTICS

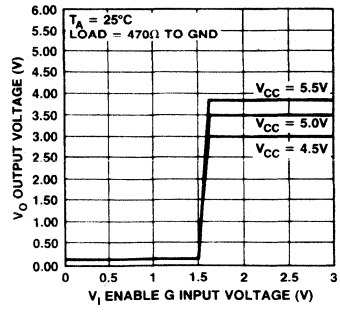
Output Voltage vs Data Input Voltage



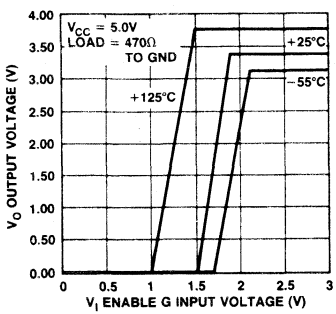
Output Voltage vs Data Input Voltage



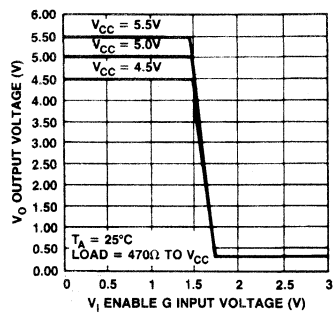
Output Voltage vs Enable G Input Voltage



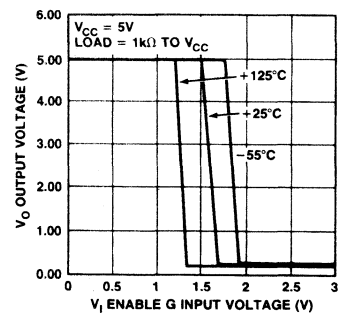
Output Voltage vs Enable G Input Voltage



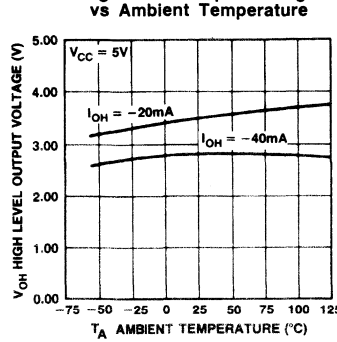
Output Voltage vs Enable G Input Voltage



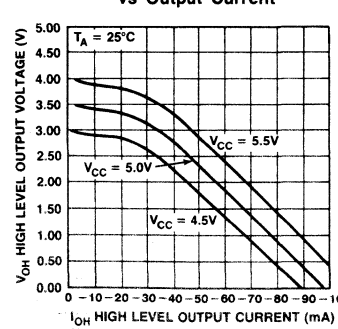
Output Voltage vs Enable G Input Voltage



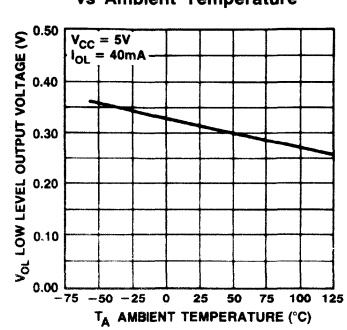
High Level Output Voltage vs Ambient Temperature



High Level Output Voltage vs Output Current

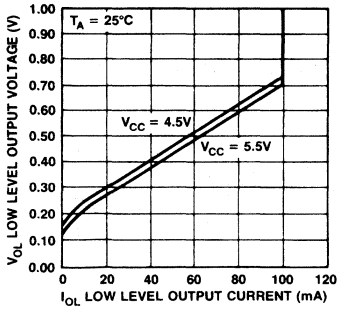


Low Level Output Voltage vs Ambient Temperature

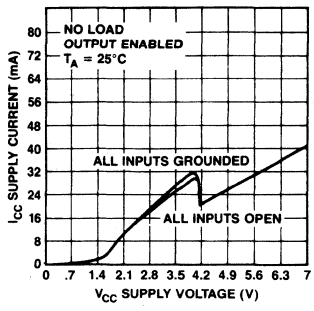


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

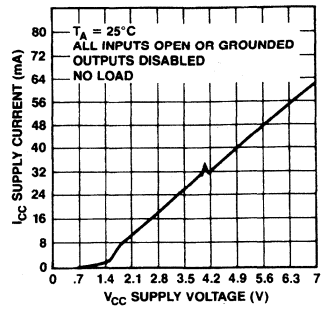
Low Level Output Voltage vs Output Current



Supply Current vs Supply Voltage



Supply Current vs Supply Voltage



AM26LS32/33
Quad High Speed Differential Line Receivers

Objective Specification

DESCRIPTION

The AM26LS32 and AM26LS33 are quad line receivers with the AM26LS32 designed to meet all of the requirements of RS-422 and RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The AM26LS32 features an input sensitivity of ±200mV over the common mode input range of ±7V.

The AM26LS33 features an input sensitivity of ±500mV over the common mode input voltage range of ±15V.

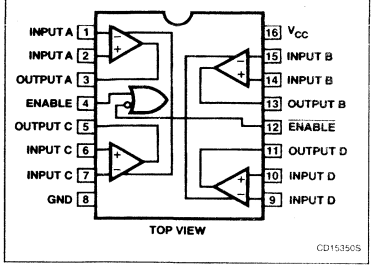
The AM26LS32 and AM26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-State outputs with 8mA sink capability and incorporate a fail-safe input-output relationship which forces the outputs high when the inputs are open.

FEATURES

- **Input voltage range of 15V (differential or common mode) on AM26LS33; 7V (differential or common mode) on AM26LS32**
- **±0.2V sensitivity over the input voltage range on AM26LS32**
- **±0.5V sensitivity on AM26LS33**
- **6k minimum input impedance**
- **60mV input hysteresis**
- **The AM26LS32 meets all the requirements of RS-422 and RS-423**
- **Operation from single +5V supply**
- **Fail safe input-output relationship. Output always high when inputs are open**
- **3-State drive, with choice of complementary output enables, for receiving directly onto a data bus**
- **3-State outputs disabled during power up and power down**

PIN CONFIGURATION

F, D and N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	AM26LS32CN
16-Pin SO	0 to +70°C	AM26LS32CD
16-Pin Plastic DIP	−40°C to +85°C	AM26LS32IN
16-Pin SO	−40°C to +85°C	AM26LS32ID
16-Pin Cerdip	−55°C to +125°C	AM26LS32MF
16-Pin Plastic DIP	−55°C to +125°C	AM26LS32MN
16-Pin Plastic DIP	0 to +70°C	AM26LS33CN
16-Pin SO	0 to +70°C	AM26LS33CD
16-Pin Plastic DIP	−40°C to +85°C	AM26LS33IN
16-Pin SO	−40°C to +85°C	AM26LS33ID
16-Pin Cerdip	−55°C to +125°C	AM26LS33MF
16-Pin Plastic DIP	−55°C to +125°C	AM26LS33MN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	7	V
V_{IN}	Power supply	7	V
	Output sink current	50	mA
	Common mode range	±25	V
V_{TH}	Differential input voltage	±25	V
T_{STG}	Storage temperature range	−65 to +150	°C

DISSIPATION OPERATING TABLE

PACKAGE	POWER DISSIPATION	DERATING FACTOR	ABOVE T_A
F	1,524mW	12.19mW/°C	25°C
N	1,275mW	10.2mW/°C	25°C
D	1,262W	10.1mW/°C	25°C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V± 10% for AM26LS32/33MX, V_{CC} = 5.0V± 5% for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS AM26LS32/33 Min	Typ[1]	Max	UNIT
V_{TH}	Differential input voltage	$V_{OUT} = V_{OL}$ or V_{OH} AM26LS32, $-7V \leq V_{CM} \leq +7V$		0.2	0.06	0.2	V
		AM26LS33, $-15V \leq V_{CM} \leq +15V$		0.5	0.06	0.5	V
R_{IN}	Input resistance	$-15V \leq V_{CM} \leq +15V$ (One input AC ground)		6.0	9.8		kΩ
I_{IN}	Input current (under test)	$V_{IN} = +15V$ Other input $-10V \leq V_{IN} \leq +15V$				2.3	mA
I_{IN}	Input current (under test)	$V_{IN} = -15V$ Other input $+10V \leq V_{IN} \leq -15V$				−2.8	mA
V_{OH}	Output HIGH voltage	V_{CC} = min., I_{OH} = −440μA ΔV_{IN} = +1.0V $V_{\overline{ENABLE}}$ = 0.8V	Com'l	2.7	3.4		V
			Mil	2.5	3.4		V
V_{OL}	Output LOW voltage	V_{CC} = min., $V_{\overline{ENABLE}}$ = 0.8V, ΔV_{IN} = +1.0V	I_{OL} = 4.0mA		0.3	0.4	V
			I_{OL} = 8.0mA			0.45	V
V_{IL}	Enable LOW voltage					0.8	V
V_{IH}	Enable HIGH voltage			2.0			V
V_I	Enable clamp voltage	V_{CC} = min., I_{IN} = −18mA				−1.5	V
I_O	Off state (high impedance) output current	V_{CC} = max.	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	μA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 5.0V± 10% for AM26LS32/33MX, V_{CC} = 5.0V± 5% for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

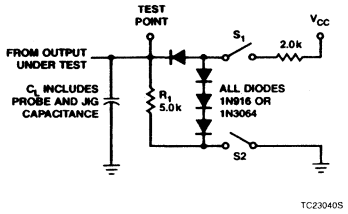
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS AM26LS32/33 Min	LIMITS AM26LS32/33 Typ[1]	LIMITS AM26LS32/33 Max	UNIT
I_{IL}	Enable LOW current	V_{IN} = 0.4V			-0.2	-0.36	mA
I_{IH}	Enable HIGH current	V_{IN} = 2.7V			0.5	20	µA
I_I	Enable input HIGH current	V_{IN} = 5.5V			1	100	µA
I_{SC}	Output short circuit current	V_{CC} = max. ΔV_{IN} = +1V, V_{OUT} = 0V		-15	-60	-85	mA
I_{CC}	Power supply current	V_{CC} = max.; All V_{IN} = GND outputs disabled			52	70	mA
V_{HYST}	Input hysteresis	T_A = 25°C, V_{CC} = 5.0V, V_{CM} = 0V	AM26LS32		60		mV
			AM26LS33		120		mV
t_{PLH}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pf (see test condition)			TBD	25	ns
t_{PHL}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pf (see test condition)			TBD	25	ns
t_{LZ}	Enable to output	T_A = 25 = C, V_{CC} = 5.0V C_L = 5pF (see test condition)			TBD	30	ns
t_{HZ}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 5pF (see test condition)			TBD	22	ns
t_{ZL}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			TBD	22	ns
t_{ZH}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF			TBD	22	ns

NOTE:
1. All typical values are T_A = 25°C, V_{CC} = 5.0V.

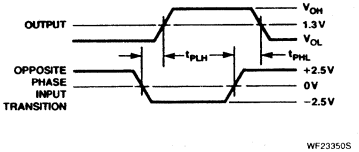
FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES E	ENABLES $\overline{E}$	OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$VTL \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	X	L	L
X	L	H	Z

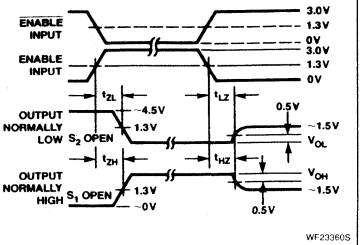
NOTES:
H = high level, L = low level, X = irrelevant
Z = high impedance (off), ? = indeterminate
E = enable, $\overline{E}$ = $\overline{\text{enable}}$



Load Test Circuit for 3-State Outputs



Propagation Delay[1, 4]



Enable and Disable Times[2, 3, 4]

NOTES:
1. Diagram shown for $\overline{\text{Enable}}$ Low.
2. Enable is tested with $\overline{\text{Enable}}$ High; $\overline{\text{Enable}}$ is tested with Enable Low.
3. S_1 and S_2 of Load Circuit are closed except where shown.
4. Pulse Generator for All Pulses: Rate $\leq$ 1.0MHz; $Z_O = 50\Omega$; $t_r \leq 15$ns; $t_f \leq 6.0$ns.

MC1488
Quad Line Driver

Product Specification

DESCRIPTION

The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

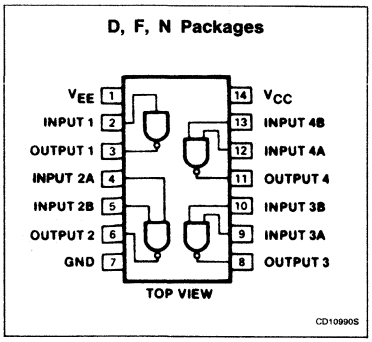
FEATURES

- **Current limited output: ± 10mA Typ**
- **Power-off source impedance: 300Ω min**
- **Simple slew rate control with external capacitor**
- **Flexible operating supply range**
- **Inputs are DTL/TTL compatible**

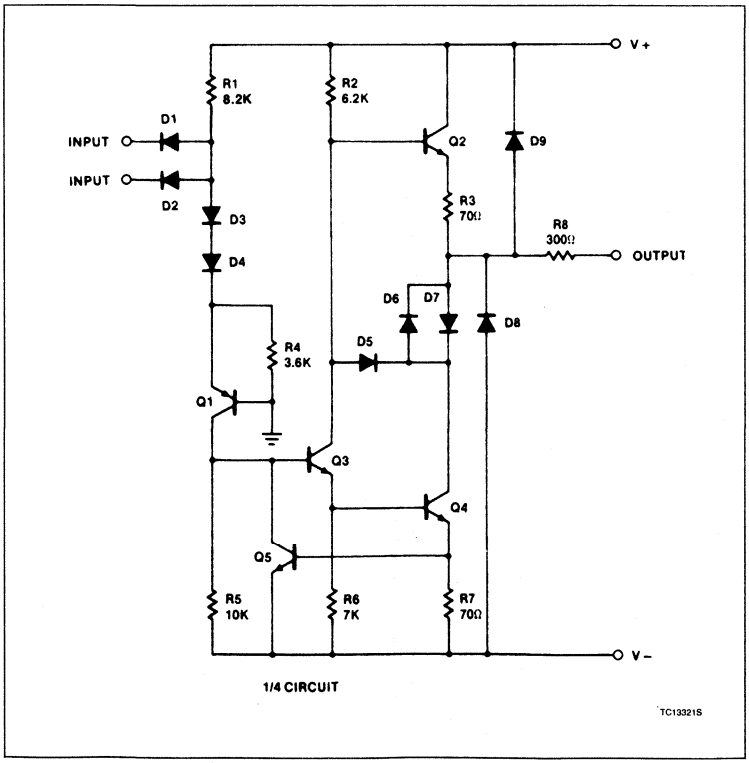
APPLICATIONS

- **Computer port driver**
- **Digital transmission over long lines**
- **Slew rate control**
- **TTL/DTL to MOS translation**

PIN CONFIGURATION



CIRCUIT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +75°C	MC1488D
14-Pin Plastic DIP	0 to +75°C	MC1488N
14-Pin Ceramic DIP	0 to +75°C	MC1488F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage V+	+15	V
	V–	–15	V
V_{IN}	Input voltage	$-15 \leqslant V_{IN} \leqslant 7.0$	V
V_{OUT}	Output voltage	±15	V
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating ambient temperature range	0 to +75	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C.
   N package at 11.4mW/°C.
   D package at 8.3mW/°C.

DC AND AC ELECTRICAL CHARACTERISTICS

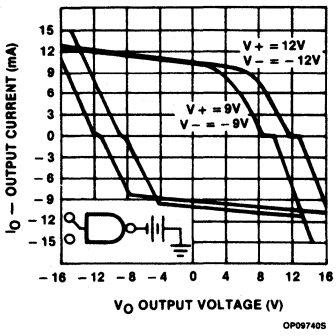
$V+ = +9.0V \pm 1\%$, $V- = -9.0V \pm 1\%$, $T_A = 0°C$ to $+75°C$, unless otherwise specifed. All typicals are for $V+ = 9.0V$, $V- = -9.0V$, and $T_A = 25°C$[1].

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ	Max	
I_{IH} I_{IL}	Logic "0" input current Logic "1" input current	$V_{IN} = 0V$ $V_{IN} = +5.0V$			−1.0 0.005	−1.6 10.0	mA μA
V_{OH}	High level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 0.8V$	V+ = 9.0V V− = −9.0V	6.0	7.0		V
			V+ = 13.2V V− = −13.2V	9.0	10.5		V
V_{OL}	Low level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 1.9V$	V+ = 9.0V V− = −9.0V	−6.0	−6.8		V
			V+ = 13.2V V− = −13.2V	−9.0	−10.5		V
I_{SC+}	High level output short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 0.8V$		−6.0	−10.0	−12.0	mA
I_{SC-}	Low level output short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 1.9V$		5.0	10.0	12.0	mA
R_{OUT}	Output resistance	$V+ = V- = 0V$ $V_{OUT} = \pm 2V$		300			Ω
I+	Positive supply current (output open)	$V_{IN} = 1.9V$	V+ = 9.0V, V− = −9.0V V+ = 12V, V− = −12V V+ = 15V, V− = −15V		15.0 19.0 25.0	20.0 25.0 34.0	mA mA mA
		$V_{IN} = 0.8V$	V+ = 9.0V, V− = −9.0V V+ = 12V, V− = −12V V+ = 15V, V− = −15V		4.5 5.5 8.0	6.0 7.0 12.0	mA mA mA
I−	Negative supply current (output open)	$V_{IN} = 1.9V$	V+ = 9.0V, V− = −9.0V V+ = 12V, V− = −12V V+ = 15V, V− = −15V		−13.0 −18.0 −25.0	−17.0 −23.0 −34.0	mA mA mA
		$V_{IN} = 0.8V$	V+ = 9.0V, V− = −9.0V V+ = 12V, V− = −12V V+ = 15V, V− = −15V		−1 −1 −0.01	−15 −15 −2.5	μA μA mA
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[2] F package N package D package					1190 1420 1040	mW mW mW
t_{PD1}	Propagation delay to "1"	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			275	560	ns
t_{PD0}	Propagation delay to "0"	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			70	175	ns
t_R	Rise time	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			75	100	ns
t_F	Fall time	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			40	75	ns

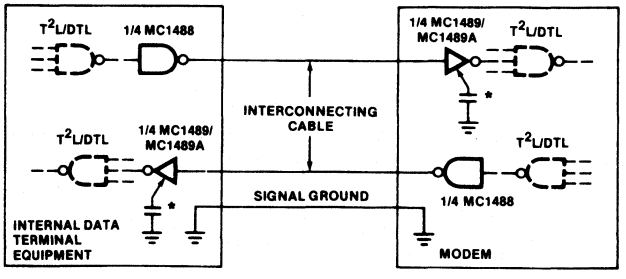
NOTES:

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C.
   N package at 11.4mW/°C.
   D package at 8.3mW/°C.

TYPICAL PERFORMANCE CHARACTERISTICS



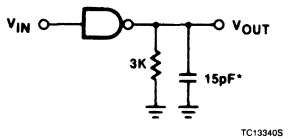
Output Voltage and Current-Limiting Characteristics



NOTE:
*Optional for noise filtering

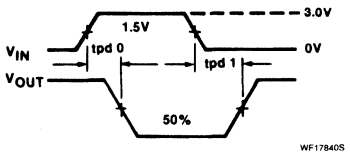
RS-232C Data Transmission

AC LOAD CIRCUIT



NOTE:
*C_L includes probe and jig capacitance.

SWITCHING WAVEFORMS



NOTE:
t_R and t_F are measured between 10% and 90% of the output waveform.

APPLICATIONS

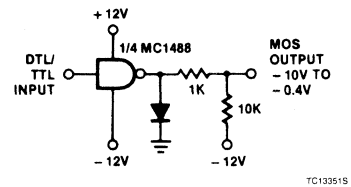
By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current-limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{SC}(\Delta T/\Delta V)$$

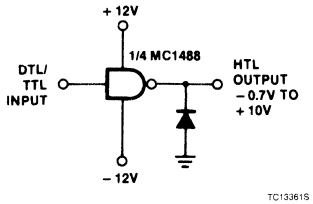
where C is the required capacitor, I_{SC} is the short-circuit current value, and $\Delta V/\Delta T$ is the slew rate.

RS-232C specifies that the output slew rate must not exceed 30V/μs. Using the worst-case output short-circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

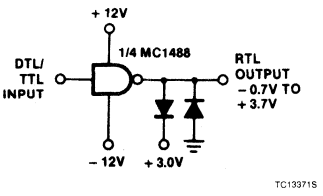
TYPICAL APPLICATIONS



DTL/TTL-to-MOS Translator



DTL/TTL-to-HTL Translator



DTL/TTL-to-RTL Translator

MC1489/MC1489A
Quad Line Receivers

Product Specification

DESCRIPTION

The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS-232C.

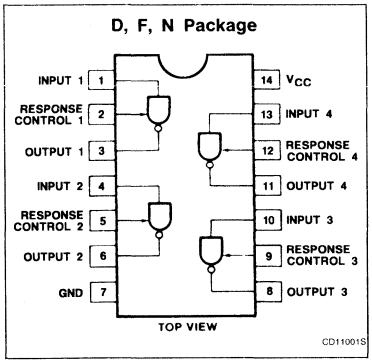
FEATURES

- **Four totally separate receivers per package**
- **Programmable threshold**
- **Built-in input threshold hysteresis**
- **"Fail safe" operating mode**
- **Inputs withstand ±30V**

APPLICATIONS

- **Computer port inputs**
- **Modems**
- **Eliminating noise in digital circuitry**
- **MOS-to-TTL/DTL translation**

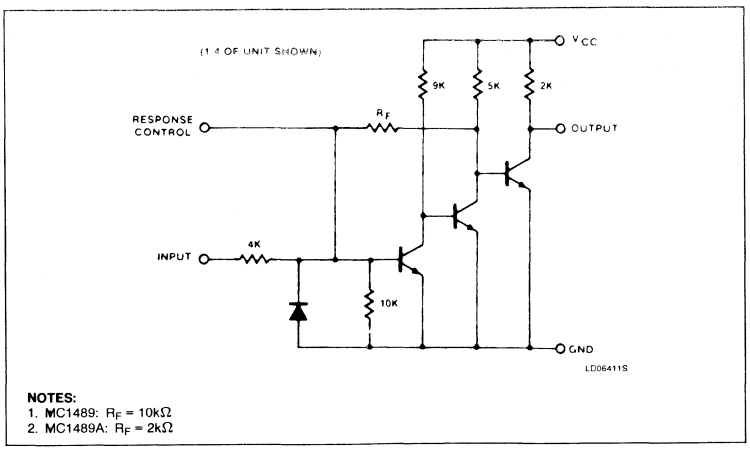
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	MC1489N
14-Pin Plastic DIP	0 to +70°C	MC1489AN
14-Pin Cerdip	0 to +70°C	MC1489F
14-Pin Cerdip	0 to +70°C	MC1489AF
14-Pin Plastic SO	0 to +70°C	MC1489D
14-Pin Plastic SO	0 to +70°C	MC1489AD

EQUIVALENT SCHEMATIC



NOTES:
1. MC1489: $R_F = 10k\Omega$
2. MC1489A: $R_F = 2k\Omega$

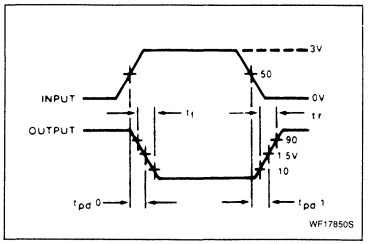
Quad Line Receivers | MC1489/MC1489A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	10	V
V_{IN}	Input voltage range	±30	V
I_{OUT}	Output load current	20	mA
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1] F package N package D package	 1190 1420 1040	 mW mW mW
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:
1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C

VOLTAGE WAVEFORMS



DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±1%, 0°C ≤ T_A ≤ +75°C, unless otherwise specified.[1, 2]

SYMBOL	PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input high threshold voltage	T_A = 25°C, V_{OUT} ≤ 0.45V, I_{OUT} = 10mA	1.0		1.5	1.75		2.25	V
V_{IL}	Input low threshold voltage	T_A = 25°C, V_{OUT} ≥ 2.5V, I_{OUT} = −0.5mA	0.75		1.25	0.75		1.25	V
I_{IN}	Input current	V_{IN} = +25V V_{IN} = −25V V_{IN} = +3V V_{IN} = −3V	+3.6 −3.6 +0.43 −0.43	+5.6 −5.6 +0.53 −0.53	+8.3 −8.3	+3.6 −3.6 +0.43 −0.43	+5.6 −5.6 +0.53 −0.53	+8.3 −8.3	mA
V_{OH}	Output high voltage	V_{IN} = 0.75V, I_{OUT} = −0.5mA Input = Open, I_{OUT} = −0.5mA	2.6 2.6	3.8 3.8	5.0 5.0	2.6 2.6	3.8 3.8	5.0 5.0	V V
V_{OL}	Output low voltage	V_{IN} = 3.0V, I_{OUT} = 10mA		0.33	0.45		0.33	0.45	V
I_{SC}	Output short-circuit current	V_{IN} = 0.75V		3.0			3.0		mA
I_{CC}	Supply current	V_{IN} = 5.0V		20	26		20	26	mA
P_D	Power dissipation	V_{IN} = 5.0V		100	130		100	130	mW

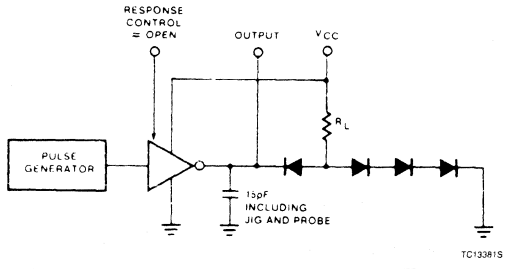
NOTES:
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±1%, T_A = 25°C, unless otherwise specified.[1, 2]

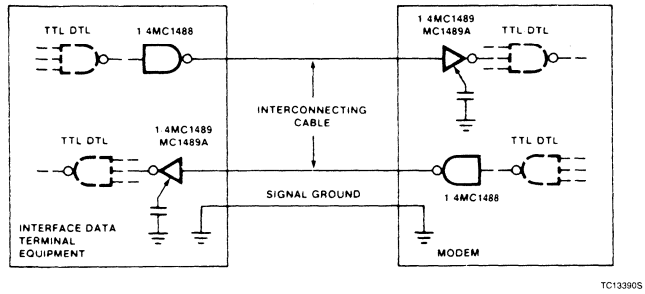
SYMBOL	PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{PD1}	Input to output "high" Propagation delay	R_L = 3.9kΩ (AC test circuit)		25	85		25	85	ns
t_{PD0}	Input to output "low" Propagation delay	R_L = 390Ω (AC test circuit)		20	50		20	50	ns
t_R	Output rise time	R_L = 3.9kΩ (AC test circuit)		110	175		110	175	ns
t_F	Output fall time	R_L = 390Ω (AC test circuit)		9	20		9	20	ns

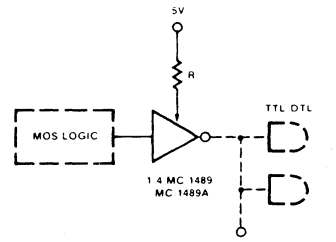
NOTES:
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

AC TEST CIRCUIT



TYPICAL APPLICATIONS





NOTE:
*Optional for noise filtering

RS-232C Data Transmission **MOS-to-TTL/DTL Translator**

NE5170
Octal Line Driver

Preliminary Specification

DESCRIPTION

The NE5170 is an octal line driver which is designed for digital communications with data rates up to 100kb/s. This device meets all the requirements of EIA standards RS-232C/RS-423A and CCITT recommendations V.10/X.26. Three programmable features: (1) output slew rate, (2) output voltage level, and (3) 3-State control (high-impedance) are provided so that output characteristics may be modified to meet the requirements of specific applications.

FEATURES

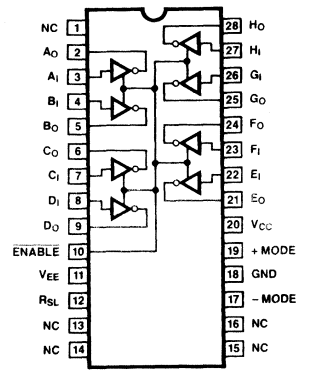
- **Meets EIA RS-232C/423A and CCITT V.10/X.26**
- **Simple slew rate programming with a single external resistor**
- **0.1 to 10V/μs slew rate range**
- **High/Low programmable voltage output modes**
- **TTL compatible inputs**

APPLICATIONS

- **High-speed modems**
- **High-speed parallel communications**
- **Computer I/O ports**
- **Logic level translation**

PIN CONFIGURATIONS

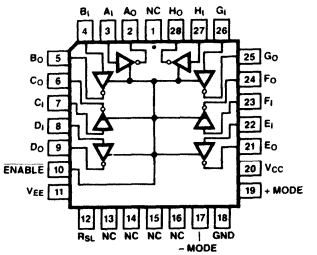
N Package



CD10240S

TOP VIEW

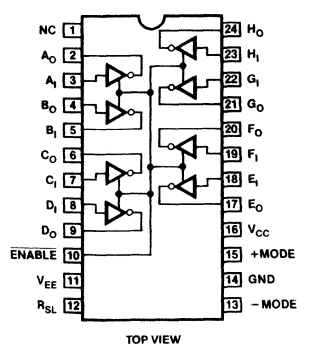
A Package



CD10250S

TOP VIEW

D Package



TOP VIEW

CD12300S

FUNCTION TABLE

$\overline{\text{ENABLE}}$	LOGIC INPUT	OUTPUT VOLTAGE (V)		
		RS-423A[1]	RS-232C	
			Low Output Mode[1]	High Output Mode[2]
L	L	5 to 6V	5 to 6V	$\geqslant$9V
L	H	−5 to −6V	−5 to −6V	$\leqslant$−9V
H	X	Hi-Z	Hi-Z	Hi-Z

NOTES:
1. V_{CC} = +10V and V_{EE} = −10V; R_L = 3kΩ
2. V_{CC} = +12V and V_{EE} = −12V; R_L = 3kΩ

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	0 to +70°C	NE5170N
28-Pin PLCC	0 to +70°C	NE5170A
24-Pin SO package	0 to +70°C	NE5170D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage and + MODE	15	V
V_{EE}	Supply voltage and – MODE	–15	V
I_{OUT}	Output current[1]	±150	mA
V_{IN}	Input voltage ($\overline{\text{ENABLE}}$, Data)	–1.5 to +7	V
V_{OUT}	Output voltage[2]	±15	V
	Minimum slew resistor[3]	1	kΩ
P_D	Power dissipation	1200	mW

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ±10%; V_{EE} = –10V ±10%; ±MODES = 0V; R_{SL} = 2kΩ, 0°C ≤ T_A ≤ 70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{OH}	Output High voltage	V_{IN} = 0.8V, R_L = 3kΩ[4]	5	6	V
		R_L = 450Ω[4]	4.5	6	
		R_L = 3kΩ[5], C_L = 2500pF	V_{CC} – 3		
V_{OL}	Output Low voltage	V_{IN} = 2.0V, R_L = 3kΩ[4]	–6	–5	V
		R_L = 450Ω[4]	–6	–4.5	
		R_L = 3kΩ[5], C_L = 2500pF		V_{EE}+3	
V_{OU}	Output unbalance voltage	V_{CC} = $\lvert V_{EE} \rvert$, R_L = 450Ω[4]		0.4	V
I_{CEX}	Output leakage current	$\lvert V_O \rvert$ = 6V, ENABLE = 2V or V_{CC} = V_{EE} = 0V	–100	100	μA
V_{IH}	Input High voltage		2.0		V
V_{IL}	Input Low voltage			0.8	V
I_{IL}	Logic "0" input current	V_{IN} = 0.4V	–400	0	μA
I_{IH}	Logic "1" input current	V_{IN} = 2.4V	0	40	μA
I_{OS}	Output short circuit current[1]	V_O = 0V	–150	150	mA
V_{CL}	Input clamp voltage	I_{IN} = –15mA	–1.5		V
I_{CC}	Supply current	No Load		35	mA
I_{EE}		No Load	–45		mA

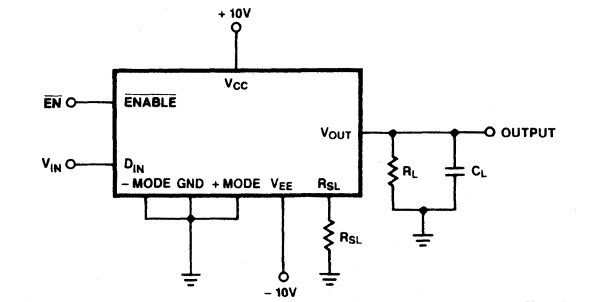
NOTES:
1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. High-impedance mode.
3. Minimum value of the resistor used to set the slew rate.
4. V_{OH}, V_{OL} at R_L = 450Ω will be ≥ ≥90% of V_{OH}, V_{OL} at R_L = ∞.
5. High Output Mode; +MODE pin = V_{CC}; –MODE pin = V_{EE}; 9V ≤ V_{CC} ≤ 13V; –9V ≥ V_{EE} ≥ –13V.

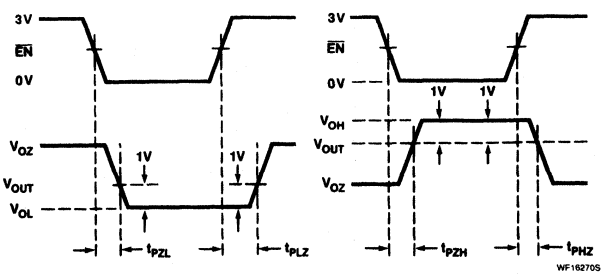
AC ELECTRICAL CHARACTERISTICS V_{CC} = +10V; V_{EE} = −10V; Mode = GND, 0°C ≤ T_A ≤ 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_{PHZ}	Propagation delay output high to high-impedance	R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		5	μs
t_{PLZ}	Propagation delay output low to high-impedance	R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		5	μs
t_{PZH}	Propagation delay high-impedance to high output	R_{SL} = 200k R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		150	μs
t_{PZL}	Propagation delay high-impedance to low output	R_{SL} = 200k R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		150	μs
SR	Output slew rate[1]	R_{SL} = 2k	8	12	V/μs
		R_{SL} = 20k	0.8	1.2	
		R_{SL} = 200k	0.06	0.14	

NOTE:
SR: Load condition. (A) For R_{SL} < 4kΩ use R_L = 450Ω; C_L = 50pF; (B) for R_{SL} > 4kΩ use either R_L = 450Ω, C_L = 50pF or R_L = 3kΩ, C_L = 2500pF.

AC PARAMETER TEST CIRCUIT AND WAVEFORMS





NOTES:
1. See AC electrical characteristics table for values of R_{SL}, R_L and C_L.
2. V_{IN} pulse: Frequency = 1kHz, duty cycle = 50%, Z_{OUT} = 50Ω, $t_r = t_f \leq 10$ns.

SLEW RATE PROGRAMMING

Slew rate for the NE5170 is set using a single external resistor connected between the R_{SL} pin and ground. Adjustment is made according to the formula:

$$R_{SL}\ (\text{in } k\Omega) = \frac{20}{\text{Slew Rate}}$$

where the slew rate is in $V/\mu s$. The slew resistor can vary between 2 and 200kΩ which gives a slew rate range of 10 to $0.1V/\mu s$. This adjustment of the slew rate allows tailoring output characteristics to recommendations for cable length and data rate found in EIA standard RS-423A. Approximations for cable length and data rate are given by:

Max. data rate (in kb/s) = 300/t

Cable length (in feet) = 100 × t

where t is the rise time in microseconds. The absolute maximum data rate is 100kb/s and the absolute maximum cable length is 4000 feet.

OUTPUT MODE PROGRAMMING

The NE5170 has two programmable output modes which provide different output voltage levels. The low output mode meets the specifications of EIA standards RS-423A and RS-232C. The high output mode meets the specifications of RS-232C only, since higher output voltages result from programming this mode. The high output mode provides the greater output voltages where higher attenuation levels must be tolerated. Programming the high output mode is accomplished by connecting the +MODE pin to V_{CC} and the −MODE pin to V_{EE}. The low output mode results when both of these pins are connected to ground.

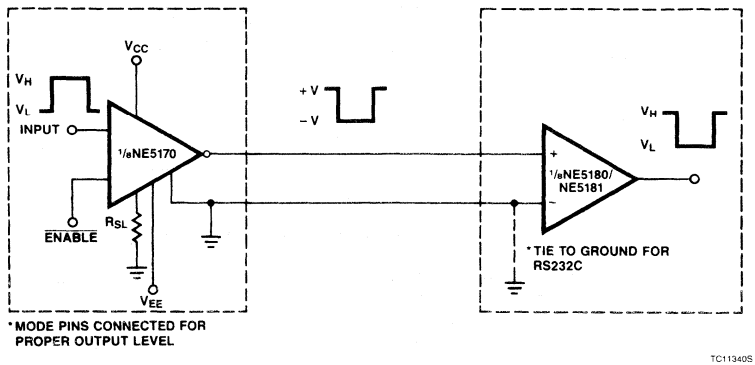


Figure 1. RS-232C/RS-423A Data Transmission

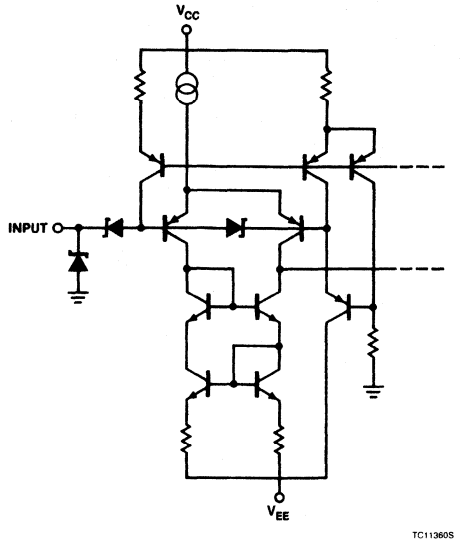


Figure 2. Input Stage Schematic

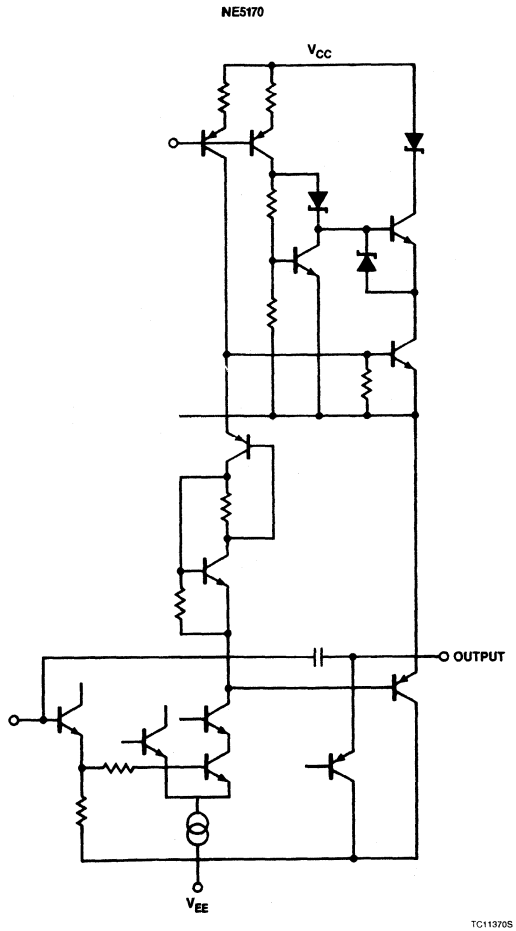


Figure 3. Output Stage Schematic

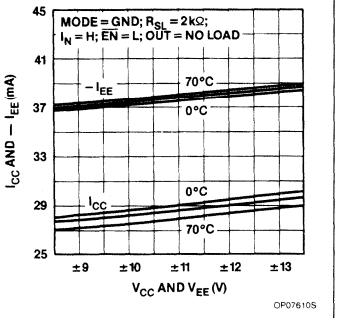


Figure 4. Typical I_{CC} and I_{EE} vs Supply Voltages

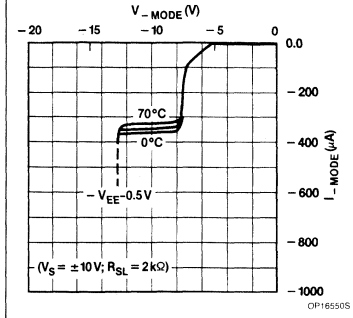


Figure 7. Typical −MODE Current vs −MODE Voltage

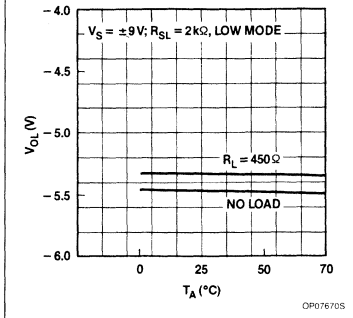


Figure 10. Typical Output Low Voltage vs Temperature

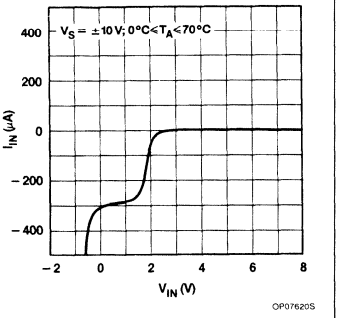


Figure 5. Typical Input Current vs Input Voltage

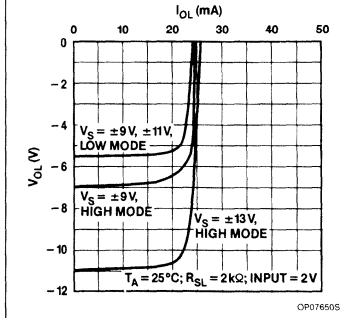


Figure 8. Typical Output Low Voltage vs Load Current

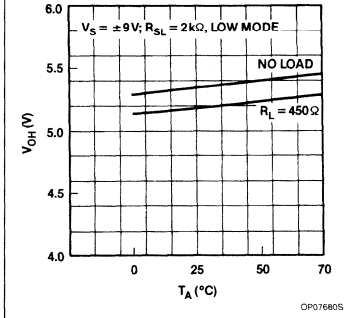


Figure 11. Typical Output High Voltage vs Temperature

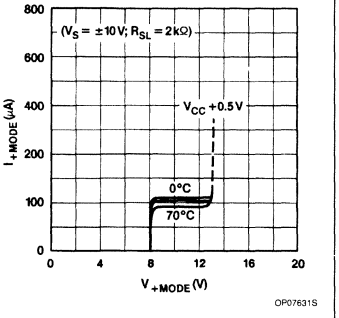


Figure 6. Typical +MODE Current vs +MODE Voltage

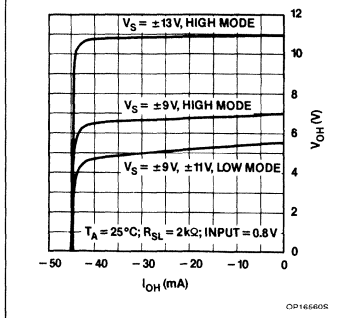


Figure 9. Typical Output High Voltage vs Load Current

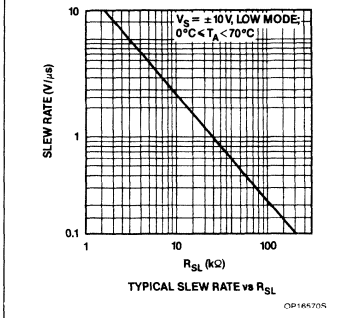


Figure 12. Typical Slew Rate vs R_{SL}

NE5180/NE5181
Octal Differential Line Receivers

Preliminary Specification

DESCRIPTION

The NE5180 and NE5181 are octal line receivers designed to interface data terminal equipment with data communications equipment. These devices meet the requirements of EIA standards RS-232C, RS-423A, RS-422A, and CCITT V.10, V.11, V.28, X.26 and X.27. The NE5180 is intended for use where the data transmission rate is up to 200 kb/s. The NE5181 covers the entire range of data rates up to 10 Mb/s. The difference in data rates for the two devices results from the input filtering of the NE5180. These devices also provide a failsafe feature which protects against certain input fault conditions.

FEATURES

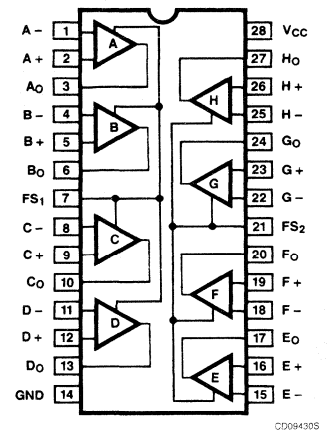
- **Meets EIA RS-232C/423A/422A and CCITT V.10, V.11, V.28**
- **Single +5V supply — TTL compatible outputs**
- **Differential inputs withstand ±25V**
- **Failsafe feature**
- **Input noise filter (NE5180 only)**
- **Internal hysteresis**
- **Available in SMD PLCC**

APPLICATIONS

- **High-speed modems**
- **High-speed parallel communications**
- **Computer I/O ports**
- **Logic level translation**

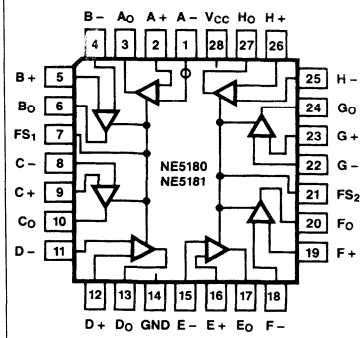
PIN CONFIGURATIONS

N Package



TOP VIEW

A Package



TOP VIEW

FUNCTION TABLE

INPUT	FAILSAFE INPUT	LOGIC OUTPUT
$V_{ID} > 200mV^1$	X	H
$V_{ID} < -200mV^1$	X	L
Both inputs open or grounded	0V	L
	V_{CC}	H

NOTE:
1. V_{ID} is defined as the non-inverting terminal input voltage minus the inverting terminal input voltage.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	0 to +70°C	NE5180N
28-Pin Plastic DIP	0 to +70°C	NE5181N
28-Pin PLCC	0 to +70°C	NE5180A
28-Pin PLCC	0 to +70°C	NE5181A

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$

SYMBOL	PARAMETER	RATING	UNIT
P_D	Power dissipation	800	mW
V_{CC}	Supply voltage	7	V
V_{CM}	Common-mode range	±15	V
V_{ID}	Differential input voltage	±25	V
I_{SINK}	Output sink current	50	mA
V_{FS}	Failsafe voltage	−0.3 to V_{CC}	V
I_{OS}	Output short-circuit time	1	sec

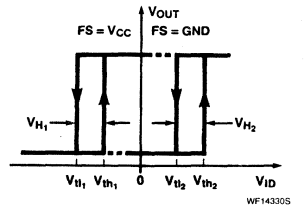


Figure 1. V_{tl}, V_{th}, V_H Definitions

DC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V \pm 5\%$, $0°C \leq T_A \leq +70°C$, input common-mode range ±7V

SYMBOL	PARAMETER	TEST CONDITIONS		NE5180		NE5181		UNIT
				Min	Max	Min	Max	
R_{IN}	DC input resistance	$3V \leq \lvert V_{IN} \rvert \leq 25V$		3	7	3	7	kΩ
V_{OFS}	Failsafe output voltage	Inputs open or shorted to GND	$0 \leq I_{OUT} \leq 8mA$, $V_{failsafe} = 0V$		0.45		0.45	V
			$0 \geq I_{OUT} \geq -400\mu A$, $V_{failsafe} = V_{CC}$	2.7		2.7		
V_{TH}	Differential input high[4] threshold	$V_{OUT} \geq 2.7V$, $I_{OUT} = -440\mu A$	$R_S = 0$[1]		0.2		0.2	V
			$R_S = 500$[1]		0.4		0.4	
V_{tl}	Differential input low[4] threshold	$V_{OUT} \leq 0.45V$, $I_{OUT} = 8mA$	$R_S = 0$[1]	−0.2		−0.2		V
			$R_S = 500$[1]	−0.4		−0.4		
V_H	Hysteresis[4]	FS = 0V or V_{CC} (See Figure 1)		50	140	50	140	mV
V_{IOC}	Open-circuit input voltage				2		2	V
C_I	Input capacitance				30		30	pF
V_{OH}	High level output voltage	$V_{ID} = 1V$, $I_{OUT} = -440\mu A$		2.7		2.7		V
V_{OL}	Low level output voltage	$V_{ID} = -1V$	$I_{OUT} = 4mA$[2]		0.4		0.4	V
			$I_{OUT} = 8mA$[2]		0.45		0.45	
I_{OS}	Short-circuit output current	$V_{ID} = 1V$, Note 3		20	100	20	100	mA
I_{CC}	Supply current	$4.75V \leq V_{CC} \leq 5.25V$, $V_{ID} = -1V$; FS = 0V			100		100	mA
I_{IN}	Input current	Other inputs grounded	$V_{IN} = +10V$		3.25		3.25	mA
			$V_{IN} = -10V$	−3.25		−3.25		

NOTES
1. R_S is a resistor in series with each input.
2. Measured after 100ms warm-up (at 0°C).
3. Only 1 output may be shorted at a time and then only for a maximum of 1 second.
4. See Figure 1 for threshold and hysteresis definitions.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V \pm 5\%$, $0°C \leq T_A \leq +70°C$

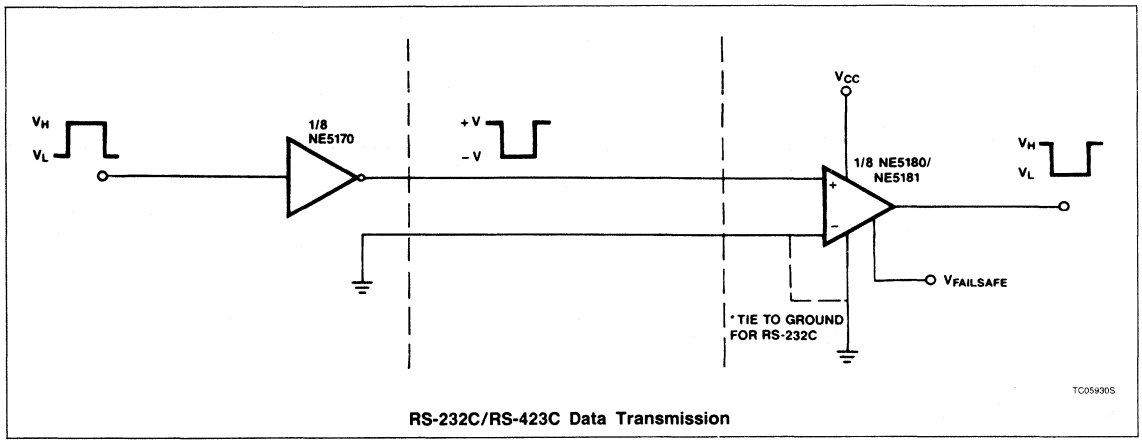
SYMBOL	PARAMETER	TEST CONDITIONS	NE5180		NE5181		UNIT
			Min	Max	Min	Max	
t_{PLH}	Propagation delay — low to high	$C_L = 50pF$, $V_{ID} = \pm 1V$		500		100	ns
t_{PHL}	Propagation delay — high to low	$C_L = 50pF$, $V_{ID} = \pm 1V$		500		100	ns
f_a	Acceptable input frequency	Unused input grounded, $V_{ID} = \pm 200mV$[1]		0.1		5.0	MHz
f_r	Rejectable input frequency	Unused input grounded, $V_{ID} = \pm 500mV$	5.5		NA		MHz

NOTE:
1. $V_{ID} = \pm 1V$ for NE5181.

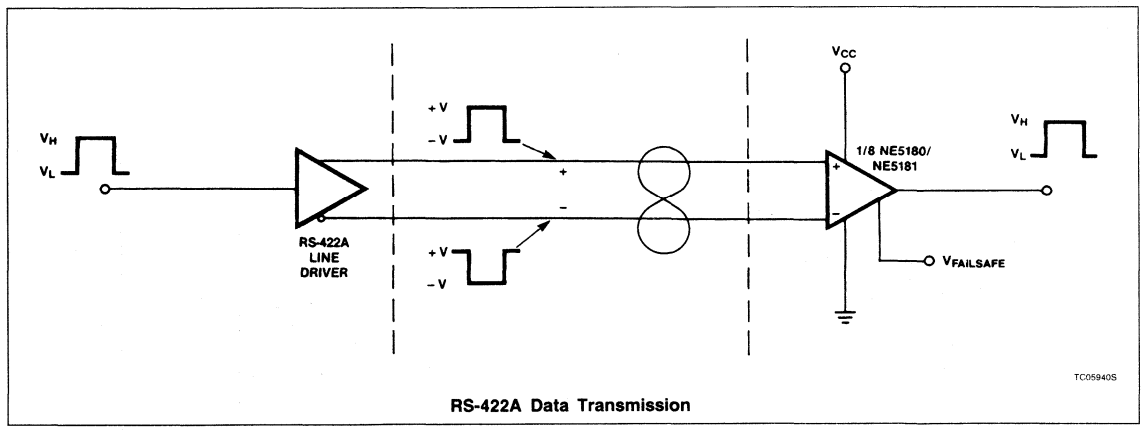
FAILSAFE OPERATION

These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS-422A and RS-423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to V_{CC} provides

APPLICATIONS

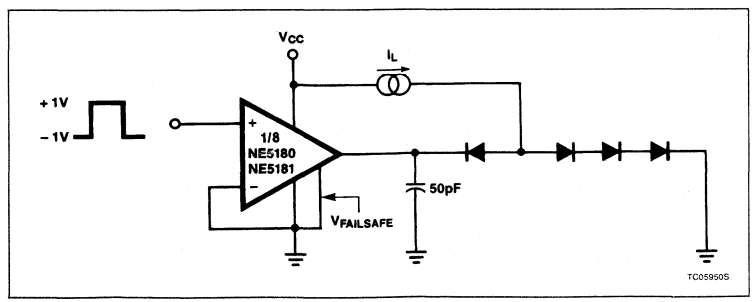


RS-232C/RS-423C Data Transmission

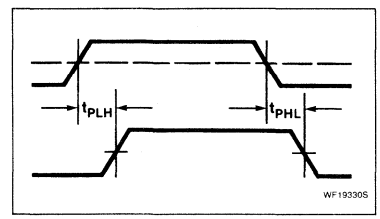


RS-422A Data Transmission

AC TEST CIRCUIT



VOLTAGE WAVEFORMS



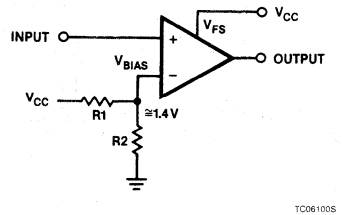
a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the NE5180 or NE5181 where each provides common failsafe control for four receivers.

RS-232 FAILSAFING

The internal failsafe circuitry works by providing a small input offset voltage which can be polarity-switched by using the failsafe control pins. This offset is kept small (approximately 80mV) to avoid degradation of the ± 200mV input threshold for RS-423 or RS-422 operation. If the positive and negative inputs to any receiver are both shorted to ground or open circuited, the internal offset drives that output to the programmed failsafe state. If only one input open circuits (as may be the case for RS-232 operation), that input will rise to the "input open circuit voltage" (approximately 700mV). Since this is much greater than the 200mV threshold, the output will be driven to a state that is independent of the failsafe programming. Failsafe programming can be achieved for non-inverting single-ended applications by raising or lowering the unused input bias voltage as shown in Figure 2. For $V_{BIAS} \cong 1.4$, an open (or grounded) INPUT line will be approximately 700mV (0V) and the output will failsafe low. If the resistor divider is not used and V_{BIAS} is connected to ground, the output will failsafe high due to the internal failsafe offset for the INPUT grounded and the 700mV "open circuit input voltage" for the INPUT open circuited. Similar operation holds for an inverting configuration, with V_{BIAS} applied to the positive input and V_{FS} = ground.

INPUT FILTERING (NE5180)

The NE5180 has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5MHz at ± 500mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output. As the signal amplitude decreases (increases) the rejected frequency decreases (increases).



NOTE:
Two silicon diodes may be used in place of R2.

Figure 2. Single-Input Failsafe Programming

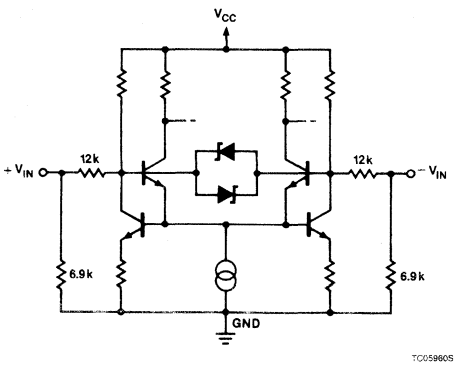


Figure 3. Differential Input Stage

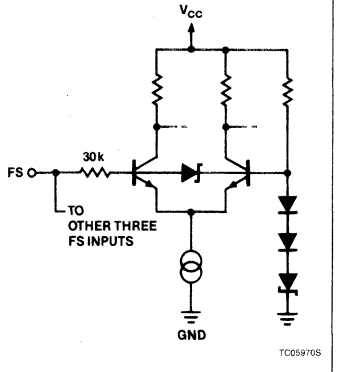


Figure 4. Failsafe Input Stage

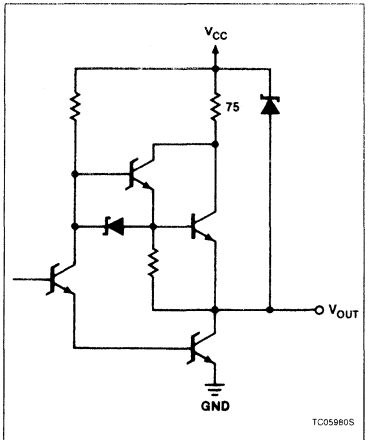


Figure 5. Output Stage

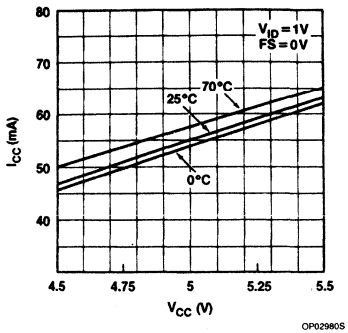


Figure 6. Typical Supply Current vs Supply Voltage

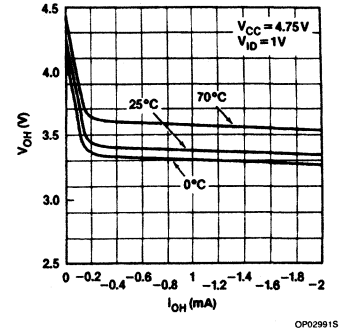


Figure 7. Typical High Level Output Voltage vs Output Current

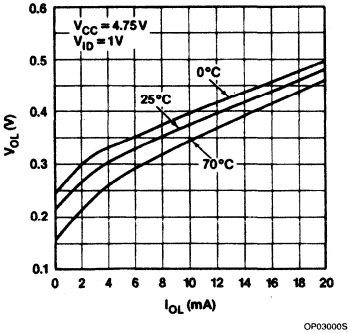
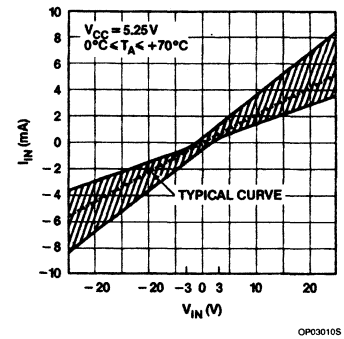


Figure 8. Typical Low Level Output Voltage vs Output Current



*This graph applies for all receiver inputs, provided that the opposite polarity input of the amplifier being measured is grounded.

Figure 9. Input Current vs Input Applied Voltage*

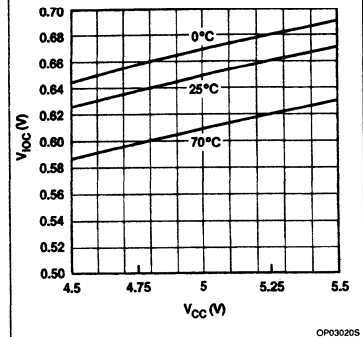


Figure 10. Typical V_{IOC} vs V_{CC}

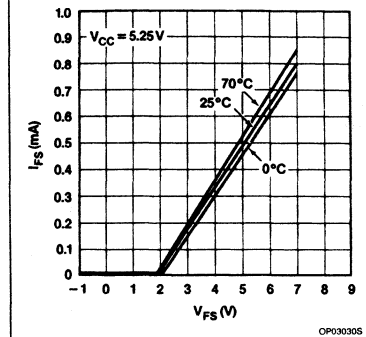


Figure 11. Typical FS Input Current vs FS Applied Voltage

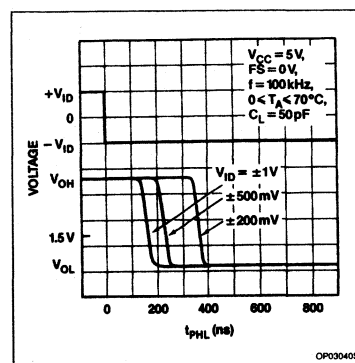


Figure 12. NE5180: Propagation Delay at Various Input Amplitudes

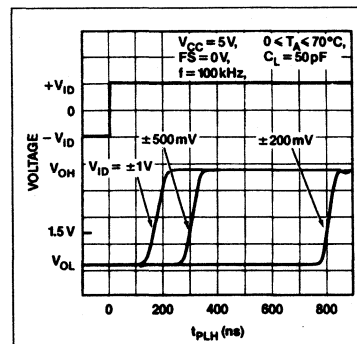


Figure 13. NE5180: Propagation Delay at Various Input Amplitudes



AN113
Using the MC1488/1489 Line Drivers and Receivers

Application Note

LINE DRIVERS AND RECEIVERS

Many types of line drivers and receivers are available today. Each device has been designed to meet specific criteria. For instance, the device may be extremely wide-band or be intended for use in party line systems. Some include built-in hysteresis in the receiver while others do not.

The EIA Standard

The Electronic Industries Association (EIA) has produced a number of specifications dealing with the transmission of data between data terminal and communications equipment. One of these is EIA Standard RS-232C, which delineates much information about signal levels and hardware configurations in data systems.

MC1488/1489

As line driver and receiver, the MC1488 and MC1489 meet or exceed the RS-232C specification.

Standard RS-232C defines, the voltage level as being from 5 to 15V with positive voltage representing a logic 0. The MC1488 meets these requirements when loaded with resistors from 3k to 7kΩ.

Output slew rates are limited by RS-232C to 30V/μs. To accomplish this specification, the MC1488 is loaded at its output by capacitance as shown by the typical hook-up diagram of Figure 1. A graph of slew rate vs output capacitance is given in Figure 2. For the standard 30V/μs, a capacitance of 400pF is selected.

The short-circuit current charges the capacitance with the relationship

$$C = \frac{I_{SC}\Delta T}{\Delta V}$$

Where C is the required capacitor, I_{SC} is the short-circuit current value, and $\Delta V/\Delta T$ is the slew rate.

Using the worst-case output short-circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output to limit the output slew rate to 30V/μs in accordance with the EIA standard.

The EIA standard also states that output shorts to any other conductor of the cable must not damage the driver. Thus, the MC1488 is designed such that the output will withstand shorts to other conductors indefinitely even if these conductors are at worst-case voltage levels. In addition to output protection, the MC1488 includes a 300Ω, resistor to ensure that the output impedance of the driver will be at least 300Ω, even if the power supply is turned off. In cases where power supply malfunction produces a low impedance to ground, the 300Ω resistors are shorted to ground also. Output shorts then can cause excessive power dissipation. To prevent this, series diodes should be included in both supply lines as pictured in Figure 3.

The companion receiver, MC1489, is also designed to meet RS-232C specifications for receivers. It must detect a voltage from ± 3 to ± 25V as logic signals but cannot generate an input differential voltage of greater than 2V should its inputs become open circuited. Noise and spurious signals are rejected by incorporating positive feedback internally to produce hysteresis. Featured also in the receiver is an external response node so that the threshold may be externally varied to fit the application. Figure 4 shows the shift in high and low trip points as a function of the programming resistance.

APPLICATIONS

The design of the MC1488 and MC1489 makes them very versatile with many possible applications. The MC1488 output current limiting enables the user to define the output voltage levels independent of supply voltages. Figure 5 shows the MC1488 as a TTL-to-MOS Translator, while Figures 6 and 7 illustrate TTL-to-HTL and TTL-to-MOS Translators.

The MC1489 response control node allows the user to modify the input threshold voltage levels. This is accomplished by adding a resistor between the response control pin and an external power supply. Figure 4 shows the shift thus provided. This feature and the fact that the inputs are designed to withstand ± 30V permit the use of the MC1489 for level translation as shown in the MOS-to-TTL Translator of Figure 8. This feature is also useful for level shifting, as illustrated in Figure 9.

The response control node can also be used to filter out high frequency, high energy noise pulses. Figures 10 and 11 give typical noise pulse rejection curves for various sized external capacitors.

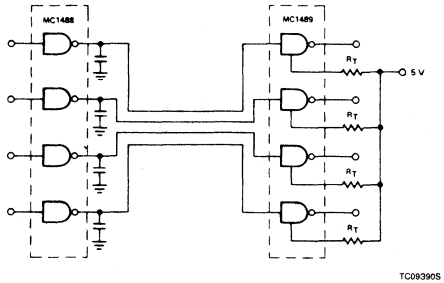


Figure 1. Typical Line Driver-Receiver Application

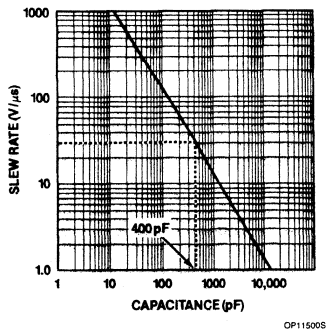


Figure 2. Output Slew Rate vs Load Capacitance

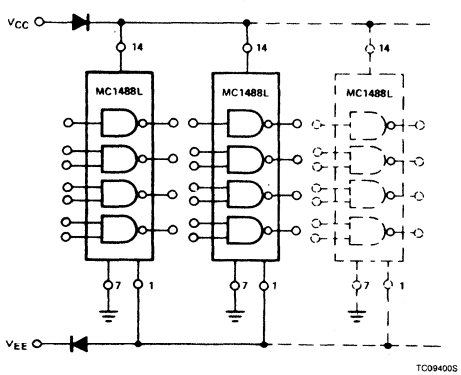
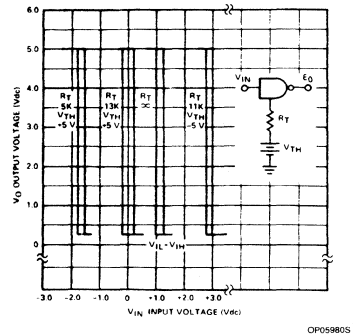
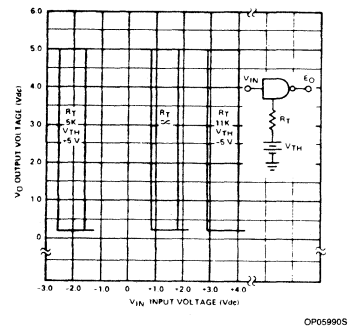


Figure 3. Protection From Power Supply Malfunction



a. MC1489



b. MC1489A

Figure 4. Hysteresis as a Function of Programming Resistance

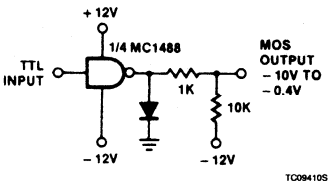


Figure 5. TTL-to-MOS Translator

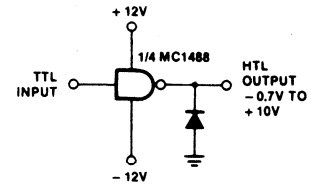


Figure 6. TTL-to-HTL Translator

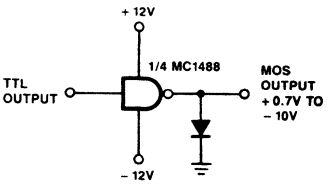


Figure 7. TTL-to-MOS Translator

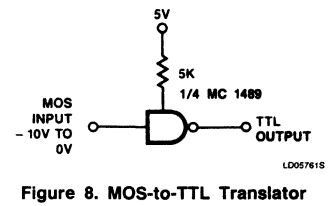


Figure 8. MOS-to-TTL Translator

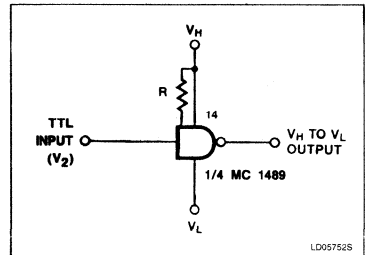


Figure 9. Level Shifter[1]

NOTE:
1. $V_2 \leq 5V$; $3V \leq V_H - V_L \leq 10V$.

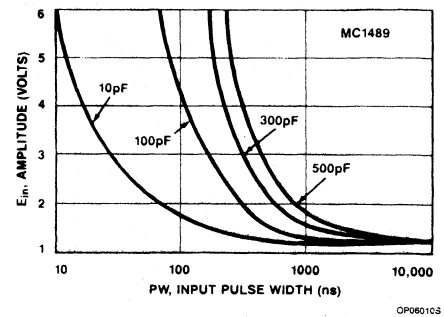


Figure 10. Turn-on Threshold vs Capacitance From Response Control Pin to GND

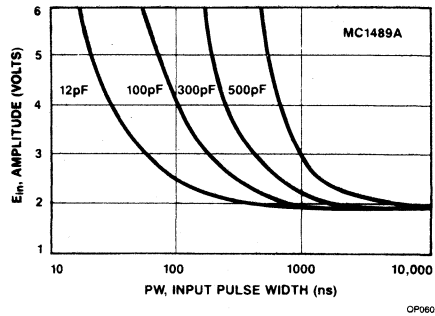


Figure 11. Turn-on Threshold vs Capacitance From Response Control Pin to GND

Modems

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NE5050	power line modem	1469
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NE5081	high-speed FSK modem receiver	1479
AN195	applications using the NE5080, NE5081	1483
AN1950	application of the NE5080 and NE5081 with frequency deviation reduction	1491
AN1951	NE5050: power line modem application board cookbook	1494

NE5050
Power Line Modem

Product Specification

DESCRIPTION

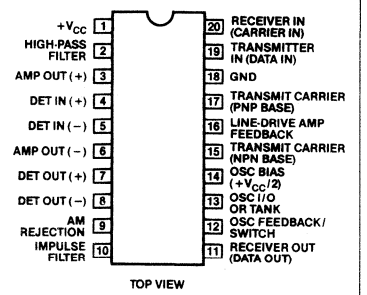
The NE5050 is a modem for power line, coaxial cable, and twisted-pair communications. The modem incorporates features to overcome line impulse noise and line impedance modulation. The modem's transmitter incorporates a Colpitts oscillator, positive logic, carrier-on/-off switch, and a line driver. The receiver has an amplifier, a limiter, an amplitude detector, an amplitude modulation cancelling stage, an impulse filter, and an SR flip-flop. One NE5050 can be used to transmit and receive with Amplitude Shift Key (ASK) carrier-on/-off modulation. With two NE5050s, Frequency Shift Key (FSK) modulation can be implemented. The transmitter input and the receiver output accept TTL or CMOS serial data.

FEATURES

- **High receiver sensitivity — typ. 1.5mV$_{RMS}$**
- **Receiver input overload protected for signals up to 70V$_{P-P}$**
- **High data rates — 300kbit/s ASK NRZ over twisted-pair**
- **The modem reaches the Nyquist limit of 1 bit per carrier cycle**
- **Has listen-while-talking for carrier sense multiple access/collision detect (CSMA/CD) networking capability**
- **Increased noise immunity with balance interstage ports for bandpass filtering**
- **Flexible oscillator can be made with LC tank (Colpitts), with crystal (Pierce), or accept external clock**

PIN CONFIGURATION

D[1] and N Packages



TOP VIEW

CD14970S

NOTE:
1. SOL — Released in large SO package only.

- **Signals are processed in real-time making this modem suitable for repeater/carrier translation applications**

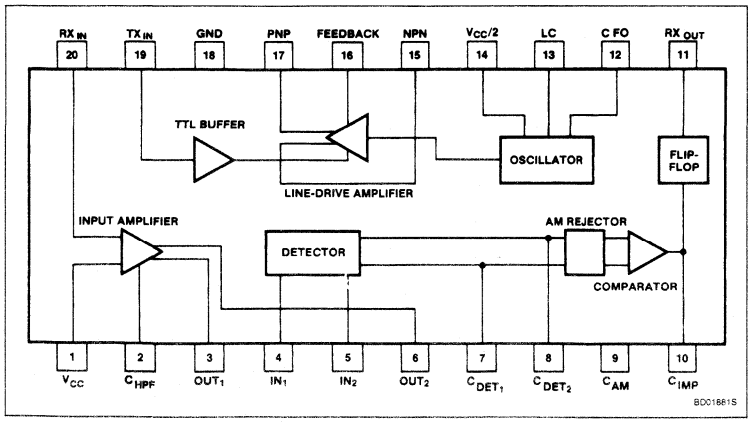
APPLICATIONS

- **Twisted-pair communications**
- **Coaxial cable communications**
- **120/277V$_{RMS}$, 50 or 60Hz, power line communications**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE5050N
20-Pin Plastic SOL	0 to +70°C	NE5050D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
V_{LOGIC}	Logic supply voltage	18	V
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature range	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{DMAX}	Maximum power dissipation[1]	700	mW

NOTE:

1. The power dissipation is based on V_{CC} = 12V, T_J = +150°C, TX_{OFF}: I_{CC} = 20mA, TX_{ON}: I_{CC} = 50mA, θ_{JA} = 61°C/W 20-pin plastic package.

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_{CC} = 12V, F carrier = 120kHz, data = NRZ, 50% duty cycle unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		10	12	16	V
I_{CC}	Supply current	TX_{OFF}	5	8	11	mA
I_{CC}	Supply current	TX_{ON}[1]	18	24	30	mA
V_{LOGIC}	Logic voltage			5	16	V
P_D	Power dissipation	RX_{OFF}, TX_{OFF} RX_{ON}, TX_{ON}, 100Ω load		100 300	220 660	mW mW
V_{IHMIN}	TX TTL input	TX_{ON}, Pin 19	2.4			V
V_{ILMAX}	TX TTL input	TX_{OFF}, Pin 19			0.8	V
V_{OLMAX}	RX open-collector output	I_{OL} = 5mA, Pin 11			0.4	V
I_{OLMAX}	RX open-collector output	Pin 11			5	mA
	TX data rate[2]	f_{CXR}=120kHz, 500kHz	DC	1k	300k	bit/s
	RX data rate[2]	f_{CXR}=120kHz, 500kHz	0.1	1k	300k	bit/s
	Carrier cycles per bit, TX and RX[2]		1			cycle
Broadband I/O ports, carrier						
	RX input sensitivity	1:1 input transformer	3.5	1.5		mV_{RMS}
	RX input signal level	V_{CC} ± 35V = −25V, +51V			70	V_{P-P}
	RX input impedance	Pin 20		9		kΩ
	RX line impedance modulation rejection	120HzAM 2V/20mV, 1kbit/s	40			dB
	RX carrier frequency[2]		0.1	120	500	kHz
	RX detector differential input impedance	Pin 4, Pin 5, each		27		kΩ
PSRR	RX power supply rejection ratio	60Hz and 120Hz		80		dB
	Broadband port impedance	RX_{OFF} and TX_{OFF}		7.3		kΩ
	TX output signal level	TX_{ON}, 100Ω load		8		V_{P-P}
	TX driver output impedance	TX_{OFF}		40		kΩ
	TX driver output impedance	TX_{ON}		1.2		Ω
	TX amplitude temperature drift	External oscillator		+140		ppm/°C
	TX amplitude temperature drift	LC oscillator		+0.23		%/°C
	TX output current capability	TX_{ON}, Pins 15, 17		40		mA peak

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = +25°C$, $V_{CC} = 12V$, F carrier = 120kHz, data = NRZ, 50% duty cycle unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	TX output THD (total harmonic distortion)	TX_{ON}, LC oscillator		1	2	%
	TX line drive amplifier BW	At 6dB gain		500		kHz
	TX carrier frequency[2]		DC	120	500	kHz
	TX oscillator temperature drift	Temperature range		+60		ppm/°C
	TX oscillator initial frequency accuracy	Same LC tank		±1		%
	TX carrier feedthrough (leakage)	TX_{OFF}		−90		dBmΩ

ABBREVIATIONS:
TX = transmitter
RX = receiver

NOTES:
1. TX looped back to RX, data = 1kbit/s TTL, NRZ, 50% duty cycle ASK.
2. The NE5050 modem reaches the theoretical maximum data density for a given (fixed) carrier frequency. This limit is set by the maximum data bandwidth required before intersymbol interference occurs. The minimum specified limits are not tested in production. They are guaranteed by design and by characterization.

PIN FUNCTION DESCRIPTION

Pin 1: $+V_{CC}$
For decoupling V_{CC} to ground a 0.1μF capacitor must be placed close to Pin 1 and Pin 18.

Pin 2: C_{HPF}
High-pass filter, rejects 60Hz and its harmonics, rejects low frequencies, directing them to ground. Capacitor to ground: C_{HPF} = 10nF for f_{CXR} = 120kHz and C_{HPF} = 4.7nF for f_{CXR} = 300kHz. The input amplifier provides a high-pass function: a +20dB/decade frequency response, with a DC attenuation of −50dB. A frequency of 100kHz is amplified by +24dB. The −3dB point of this high-pass filter is given by the equation:

$$10^9/C_{HPF}\ (F) = f_{-3dB}\ (Hz)$$

Pin 3: OUT_1
RX amplifier differential (+) output. Low impedance output. See Pin 6. Pin 3 can be connected to Pin 4 directly. A differential, bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{-3dB} is controlled by the series resistors R_1 and R_2. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 4, Pin 5: IN_1, IN_2
AM detector (±) inputs. High-impedance inputs = 27kΩ each. They require DC bias voltage from Pins 3 and 6 or around 4.5V. Pin 3 can be connected to Pin 4 directly. Pin 6 can be connected to Pin 5 directly. A differential bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{-3dB} is controlled by series resistors. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 6: OUT_2
RX amplifier differential (−) output. Low impedance output. See Pin 3. Pin 6 can be connected to Pin 5 directly. A differential bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{-3dB} is controlled by the series resistors R_1 and R_2. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 7, Pin 8: C_{DET}
Amplitude detector (±) output capacitor between Pins 7 and 8. t_{DET} is the time it takes for C_{DET} to charge from 0mV to 50mV, where 50mV is the detection threshold. The detector delay time, t_{DET}, affects the receiver's jitter. t_{DET} is a term in a sum of delays, the sum being the total receiver delay, t_D. See below in 'Receiver Delays' the relation between t_D and the maximum bit rate. The C_{DET} capacitor value is given by:

$$C_{DET}\ (F) = t_{DET}\ (sec)/10^5$$

Pin 9: C_{AM}
Line impedance modulation rejection capacitor. A 0.1μF capacitor to ground provides about 4s of delay for the transition from receive data to standby. The C_{AM} value is determined in function of the bit rate, or, more precisely, minimum bit time, to assure proper capture of leading bits in a bit string or in the preamble. It is a measure of the "readiness" of the receiver to switch from the "standby" mode to the "receive data mode" with no loss of leading bits. A low C_{AM} value will make the modem react faster (shorter delays) in both transition directions: from "standby" to "receive data" (incoming or departing messages) and from "receive data" to "standby" (absence of data traffic). Its value should be:

$$C_{AM}\ (F) = 10^{-4}/\text{bit rate [bits/s]}$$

Pin 10: C_{IMP}
Impulse noise rejection capacitor. At 1kbit/s a 10nF capacitor to ground provides 350μs of delay and impulse rejection. This capacitor determines the receiver impulse noise immunity (transmission channel with non-Gaussian noise). t_{IMP} is the time it takes to ramp up or down the C_{IMP} voltage (the beginning of the ramp is delayed by t_{DET}). The shortest bit should last longer than the widest impulse. t_{IMP} is a term in a sum of delays, the sum being the total receiver delay, t_D. See 'Receiver Delays' for the relation between t_D and the maximum bit rate. The C_{IMP} capacitor value is determined by the equation:

$$C_{IMP}\ (F) = t_{IMP}\ (s)/85k\Omega$$

The following equation determines t_{IMP}:

Maximum rejected or expected impulse noise width (s) < t_{IMP} (s)

Pin 11: RX Data Output
Open-collector RX output. RX data output.

$$I_{OLMAX} = 5mA = V_{LOGIC}/R_{PULL\text{-}UP}$$

Pin 12: C_{F0}
Oscillator feedback input. C_{FO} = 27 to 51pF capacitor between Pins 12 and 13. C_{F1} = capacitor between Pins 12 and GND. If the on-chip oscillator is used, C_{F1} may be omitted. If external oscillations are injected at Pin 13, C_{F0} must be removed and C_{F1} must be connected to GND. Grounding Pin 12 disables the oscillator.

Pin 13: Oscillator I/O
Colpitts LC oscillator tank, Pierce crystal oscillator, or external oscillator input.

On-chip LC oscillator — oscillator output. External oscillator tank present. Parallel LC components attached between Pins 13 and 14. C_{F0} attached between Pin 12 and Pin 13. A resistor between Pins 13 and 14 can decrease the oscillation amplitude to the desired level. Amplitudes above 2V peak may have THD > 2%. C_{F1} is not used. The amplitude varies with temperature; thermistor compensation recommended at Pin 16.

On-chip crystal oscillator — oscillator output. Two external capacitors in series, C_{13} and C_{14}. C_{13} is connected to Pin 13 and C_{14} is connected to Pin 14. The external crystal is attached between Pin 13 and the connection of C_{13} and C_{14}. An optional inductor L, attached between Pins 13 and 14, tuned at the oscillation frequency by C_{13} and C_{14} prevents oscillations at the crystal overtones. C_{F0} and C_{F1} are not used.

External oscillator — oscillator input. Parallel LC components attached between Pins 13 and 14 provide bias to Pin 13 and perform bandpass filtering. If a square wave is generated from a microprocessor by clock division, a series LC from the divider output to Pin 13 will perform additional bandpass filtering. $C_{F1} = 0.1\mu F$ is connected to ground. C_{F0} is not used. If a sinusoidal wave is available, a 50Ω resistor may replace the parallel LC bandpass filter and a 0.1μF capacitor may replace the series LC bandpass filter. The amplitude is constant over temperature.

Pin 14: $+V_{CC}/2$
Oscillator bias at $+V_{CC}/2$. A 0.1μF decoupling capacitor to GND is optional. Parallel LC components attached between Pins 13 and 14.

Pin 15: TX Carrier Output (NPN Transistor Base)
Transmitter broadband output. Can drive 40mA peak (80mA peak non-repetitive).

NPN external Darlington transistor — Drives 1Ω loads.

NPN external transistor drive — $1\Omega - 0.5W - R_{E1}$ to Pin 16 for 10Ω loads.

On-chip driver — 10Ω R_{E1} between Pins 15 and 16 for 50Ω loads.

Pin 16: TX Line Driver Feedback
$R_{FEEDBACK}$ adjusts the driver amplifier gain. Minimum gain ($R_{FEEDBACK} = 0$) is 2 (6dB). A thermistor can compensate the LC oscillator amplitude variation. R_{E1} resistor (and NPN EB junction) to Pin 15. R_{E2} resistor (and PNP EB junction) to Pin 17. The C_{DRIVE} coupling capacitor is in series with the R_{DRIVE} resistor from Pin 16 to Pin 20. The R_{DRIVE} value is the assumed line impedance. The C_{DRIVE} impedance is $1/(2 \times f_{CXR}\ C_{DRIVE})$.

Pin 17: TX Carrier Output (PNP Transistor Base)
Transmitter broadband output. Can drive 40mA peak (80mA peak non-repetitive).

PNP external Darlington transistor — Drives 1Ω loads.

PNP external transistor drive — $1\Omega - 5.0W - R_{E2}$ to Pin 16 for 10Ω loads.

On-chip driver — 10Ω R_{E2} between Pins 16 and 17 for 50Ω loads.

Pin 18: Ground

Pin 19: TX Data Input
Transmitter TTL data input. Logic 1 will turn the transmit driver on, and sinusoidal carrier will be sent to the line from a low impedance source. Logic 0 will turn the driver off, to high output impedance.

Pin 20: RX Carrier Input
Receiver carrier input. Withstands an overvoltage of $+V_{CC} \pm 35V$. DC bias connected through the line coupling transformer secondary to $+V_{CC}$ (Pin 1). The C_{DRIVE} coupling capacitor is in series with the R_{DRIVE} resistor from Pin 16 to Pin 20.

DESCRIPTION OF OPERATION

The NE5050 modem has been designed for transmitting and receiving control and data signals over the AC power lines, coaxial cables and twisted-pair cables. The modem overcomes line impulse noise and line impedance modulation. Two carrier modulation methods can be used: carrier on/off ASK, NRZ data and non-coherent FSK.

The power line is not an ideal medium for communication. The line noise, interference, and losses are caused by: impulse noise, CW interference, line impedance modulation, and distribution transformer attenuation. NE5050 was designed to support both ASK and non-coherent FSK communications in this environment.

Listen-While-Talk

The IC modem is always in the receive mode, even when transmitting (it receives its own carrier). This capability permits remote RX and TX functionality testing for each system node. In the receive mode, the modem receives carrier signals from other transmitters. In the transmit mode, the modem transmits carrier to other receivers and receives its own carrier.

On-Chip Collision Detection

The listen-while-talk capability enables this IC to perform CSMA/CD (carrier-sense, multiple-access/collision detect) networks. Collision is detected when the local TX intends to transmit and the line is not clear.

In Dense Data Traffic

The RX data output (RX_{OUT}) does not have time to go into the standby (lower power consumption, inverted logic) mode. In this case the RX_{OUT} is in positive logic (carrier-on = 1, carrier-off = 0). A collision is detected at the local node when the local TX is off and the local $RX_{OUT} = 1$. Collision: remote carrier present and detected. Abort local transmission. If, however, standby occurs (bursts of high-speed data) a proper value of C_{AN} will insure capture of all leading bits except for the first "10" transition.

In Rare Data Traffic

The RX_{OUT} is in standby most of the time. In this case the RX_{OUT} logic mode is inverted due to a designed-in offset present in the AM rejection and impulse filter circuits. A logic sequence from the local TX insures proper RX offset adjustment (preamble, the first "10" bits). The collision detection proceeds as in the dense data traffic case. The transition time from the last received bit "1" to the standby mode is proportional to the value of the AM rejection capacitor at Pin 9. For C_{AM} = 10nF, the "receive data" to "standby" transition occurs after 4 seconds from the last "1". Therefore, long strings of "0"s can be transmitted and received. The standby function may be disabled with proper bias at Pin 9 (external components).

TX-to-RX and RX-to-TX Switching Times

With the listen-while-talk capability the TX-to-RX and the RX-to-TX switching times have the meaning of TX_{ON}-to-TX_{OFF} and TX_{OFF}-to-TX_{ON} switching times, respectively. The TX-to-RX and RX-to-TX minimum switching times can be calculated from the maximum data rate. Since one bit can last a minimum of 3μs (NRZ ASK data), this may be considered the minimum switching time.

Data Rate

The maximum data rate is 300kbit/s NRZ ASK. This data rate was achieved on a twisted-pair cable with a 150kHz, 50% duty cycle square wave for data. The data rate depends on the BPF (between Pins 3 – 4 and 5 – 6), on the AM detector capacitor for delay, C_{DET} (between Pins 7 and 8), on C_{AM} (Pin 9) for capture of leading bits, and on the desired impulse noise immunity for delay, C_{IMP} (Pin 10).

AC Line Coupling Network

One or two (120V or 240V and 277V AC RMS) coupling capacitors rated 600V are connected in series with the primary of a 1:1 transformer and connected to the AC line. The transformer secondary may be tuned to the carrier frequency by a capacitor (TOKO

transformer, low data rates) or no secondary tuning capacitor for higher data rates (AIE Magnetics transformer). Two back-to-back zener diodes must be placed between Pins 1 and 20 for the IC transient protection (1N4744 or 1N6275). The transformer secondary carries DC bias current between Pins 1 and 20 of the IC. This coupling network itself attenuates to below the RX input sensitivity the 50 or 60Hz and their harmonic frequencies. In a coaxial cable application the transformer can be replaced with a coupling capacitor.

Receiver (RX)

The typical RX sensitivity is $1.5mV_{RMS}$. For less sensitivity, adjust the turn ratio of the coupling transformer or insert loss in the bandpass filter. The RX-only function can be implemented by not using the oscillator and by grounding the TX input. The maximum data rate is 300kbit/s. The power supply rejection ratio (PSRR) is 80dB for 60Hz and 120Hz. The RX is composed of the following blocks:

The Input Amplifier/Limiter limits its output signals to $1.2V_{P-P}$. The maximum input carrier signal can be $70V_{P-P}$. The gain is 24dB. The input amplifier bandpass characteristic has the upper −3dB frequency internally fixed at 300kHz. The lower −3dB frequency is adjustable with the C_{HPF} capacitor from Pin 2 to GND. For maximum RX sensitivity C_{HPF} = 10nF at f_{CXR} = 120kHz. A $C_{HPF} = 0.1\mu F$ value attenuates 60Hz by 50dB and 120Hz by 45dB.

The Bandpass Filter is differential RLC bandpass filter which can be connected from Pins 3, 6 to Pins 4, 5. The LC values are the same as the oscillator LC values (see Pins 13 and 14). The formulae relating the BW_{-3dB} to the RLC values are:

$$BW_{-3dB} / \omega_{CXR} = (\omega_{CXR} * L) / (2 * R) = 1 / Q$$

$$BW_{-3dB} / \omega_{CXR} = 1 / (\omega_{CXR} * 2 * C * R) = 1 / Q$$

$$BW_{-3dB} = (\omega_{CXR} * \omega_{CXR} * L) / (2 * R)$$

$$BW_{-3dB} = 1 / (2 * C * R) \text{ and } \omega_{CXR} = 2 \times f_{CXR}.$$

If no bandpass filter is required, connect Pin 3 to 4 and Pin 5 to 6 ($R_1 = R_2 = 0\Omega$).

The Amplitude Detector is a Gilbert phase detector with a single differential input. The compared signals are always in phase and the demodulated output is a full rectified wave, function of the bias current, the carrier amplitude, and the collector load. The detected voltage is developed across a differential capacitive load between Pin 7(+) and Pin 8(−). DC offset is caused by line impedance modulation.

The AM Rejection Circuit stabilizes the DC average value of the envelope by adding or subtracting a series voltage to the voltage of the detector capacitor. The AM rejection is 40dB at a modulation rate of 120Hz. The value of the AM rejection capacitor C_{AM} (Pin 9 to GND) determines the transition times to and from receive data and standby.

The Slicing Comparator has current output and a fixed threshold of 50mV.

The Impulse Filter consists of a capacitor, C_{IMP}, at the output of the comparator, from Pin 10 to GND. This capacitor is charged or discharged with constant current from the comparator, causing the voltage variation to be a constant slope in time. Narrow current impulses will not last long enough to fully charge or discharge the capacitor.

$2V_{BE}$ Voltage Hysteresis provides a voltage interval in which the C_{IMP} voltage ramps and in which both inputs to the SR flip-flop are zero.

The Flip-Flop is an SR type, with an open-collector transistor output at Pin 11. The transistor can switch a maximum load of 5mA.

Receiver Delays and Maximum Data Rate

The total receiver delay is a sum of delays, where t_{DET} (sec) is the detector delay, t_{IMP} (sec) is the impulse filter delay, and $2\mu s$ is the approximate receiver delay with no C_{DET} and no C_{IMP}:

t_D (sec) = total receiver delay
$= t_{DET}$ (sec) $+ t_{IMP}$ (sec) $+ 2\mu s$

The maximum bit rate, in the no-return-to-zero, amplitude shift keying data format is determined by: Maximum bit rate MRZ ASK (bit/sec) $< 1/t_D$ (sec^{-1})

NOTE:
The C_{DET} and C_{IMP} values so calculated are for guidance and the user shall determine the optimal performance values in a range between 0.1 times to 10 times the calculated values (power line environment assumed). For twisted-pair or coaxial cables the calculated values are close to optimal. Based on power line applications made at 100 bits/sec and at 50 kbits/sec, the C_{IMP} / C_{DET} capacitor ratio ranges from 100:1 to 1:1.

Transmitter, TX

The transmitter includes an oscillator, a line driver, and a drive switch.

The TTL Switch is a low power TTL gate that switches on/off the bias current for the line driver. A logic "1" at Pin 19 (TX_{IN}) enables the line driver and carrier is being sent on the line. A logic "0" disables the driver.

The Oscillator is a differential transistor pair. It can be configured as a Colpitts LC oscillator, as a Pierce crystal oscillator, or used with external input (microprocessor clock divided to the carrier frequency). When the TX drive is off, the carrier leak is less than −90dBmO. Pin 18 can be used as input for an external oscillator. Grounding Pin 12 disables the oscillation process.

The Line Driver is a class AB push-pull stage with optional external complementary transistor pair for increased current capability. The TX output impedance is 40Ω in the off-state (receive mode) and less than 2Ω in the on-state (transmit mode). Note that in the transmit mode one receives its own signal. To increase the amplitude of the transmitter, add a feedback resistor in the driver amplifier feedback path at Pin 16.

By itself the NE5050 is capable of driving a consumer line impedance of 50Ω (40mA peak/80mA peak non-repetitive), the THD being less than 2%. With complementary transistors, 10Ω industrial loads can be driven. With complementary Darlington transistors, 1Ω industrial loads can be driven.

One design objective was to provide the user with a flexible IC modem for residential as well as for industrial AC lines, for twisted-pair, and for coaxial cables. The IC modem can be used for control functions and data applications. Practical observations of power line noise point to a data rate upper boundary of 1kbit/sec. The main sources of interference are the light dimmers. Software for error correction can be used for improved error rates. Two system configurations can be implemented: an ASK system and a non-coherent FSK system. The non-coherent FSK system can continue to transmit ASK data if the other channel is made unusable by CW interference. High-voltage transient protection and filtering are accomplished with user-selected external components.

Additional flexibility is provided by the chip architecture: one-IC real-time repeater, one-IC dual-frequency gateway, external oscillator input port, the listen-while-talk capability (CSMA/CD), immediate TX-to-RX switching, ASK and FSK, and ASK-multinode single-frequency network.

The modem can be used for control systems and data applications in homes and other consumer environments and in industry.

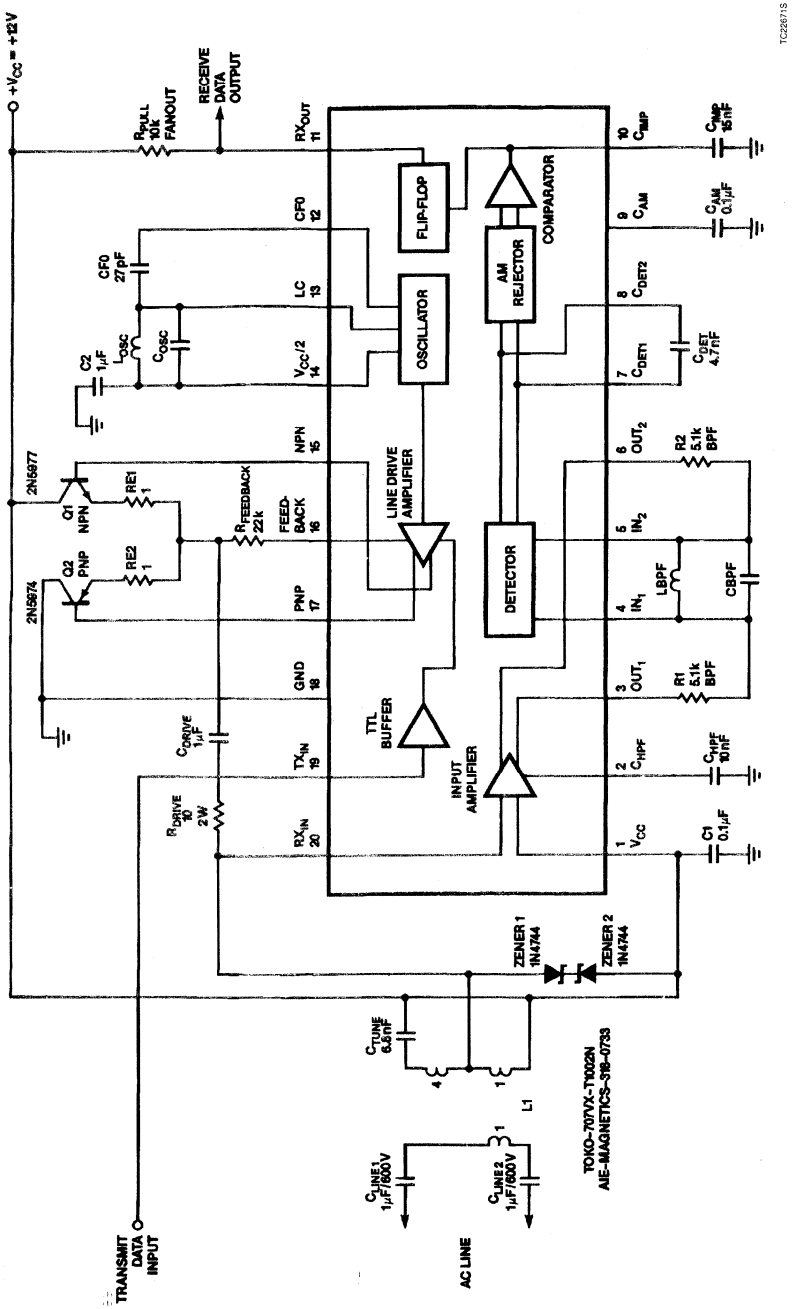


Figure 1. Typical Application Circuit for 1kbit/s on the 120/277V AC Line

NE5080
High-Speed FSK Modem Transmitter

Preliminary Specification

DESCRIPTION

The NE5080 is the transmitter chip, of a two-chip set, designed to be the heart of an FSK modem. (The NE5081 is the receiver chip.) The chips are compatible with the IEEE 802.4 standard for a "Single-Channel Phase-Continuous-FSK Token Bus." The specifications shown in this data sheet are those guaranteed when the transmitter is tuned for the frequencies given in the 802 standard. However, both the NE5080 and the NE5081 may be used at other frequencies. The ratio of logic high to logic low frequencies is normally at 1.67 to 1.00 at any center frequency; however, it can be varied externally. (See AN1950.)

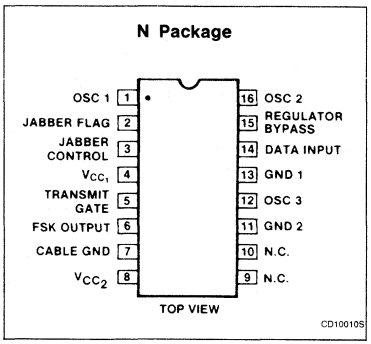
FEATURES

- **Meets IEEE 802.4 standard**
- **Data rates to several Megabaud**
- **Half- or full-duplex operation**
- **Jabber function on-chip**

APPLICATIONS

- **Local Area Networks**
- **Point-to-point communications**
- **Factory automation**
- **Process control**
- **Office automation**

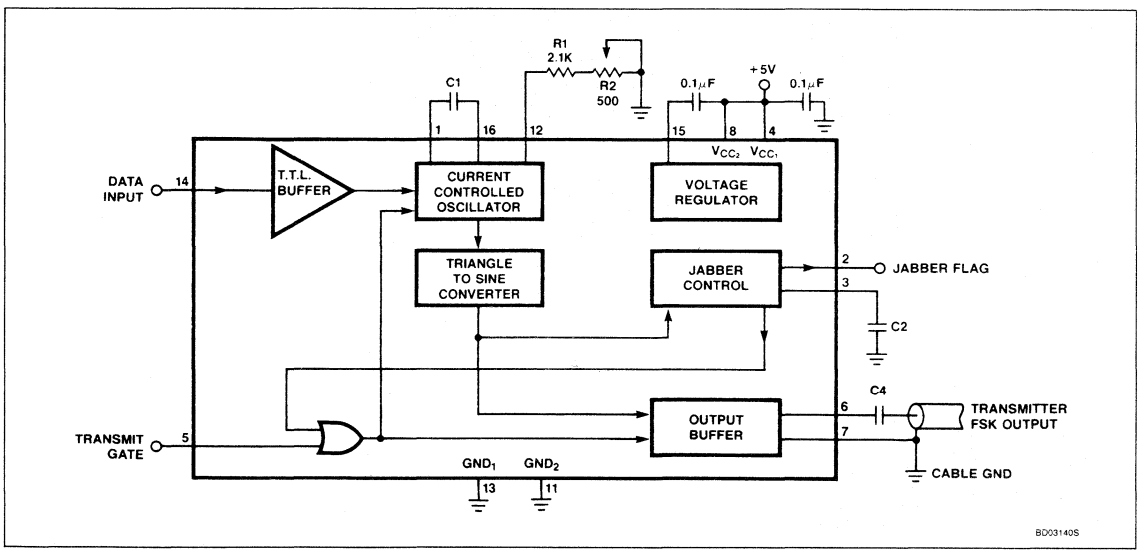
PIN CONFIGURATION



ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	NE5080N

BLOCK DIAGRAM



High-Speed FSK Modem Transmitter NE5080

GENERAL DESCRIPTION

The NE5080 is designed to transmit high frequency asynchronous data on coaxial cable, at rates from DC to 2M baud (see Note 1). The chip accepts serial data and transmits it as a periodic signal whose frequency depends on whether the data is high or low.

The device is meant to operate at a frequency of 6.25MHz for a logic high and 3.75MHz for a logic low (see Note 2). The frequency is set up by external trimming components; however, the ratio of the high and low frequencies is set internally and cannot be altered.

The FSK output can be turned off by use of the transmit gate pin. When turned off, the transmitter has a high output impedance and the oscillator is disabled.

The length of time a transmitter can transmit can be controlled by the use of the Jabber control pin (see description of Jabber Control Pin).

Jabber Control Pin

During the time the transmitter is transmitting, this pin sources a current. This current can be used to set the maximum time that the transmitter can be on. There are three options that can be used:

1. Use the current to charge a capacitor. When the voltage across the cap gets to approximately 1.4V, the transmitter will turn off. A logic low applied to Pin 3 will reset the Jabber function; an open collector output should be used for this purpose. A logic high applied to the pin will disable the transmitter.
2. Use to externally sense the current and have external circuitry to control the length of time the transmitter is on.
3. The pin can be tied to ground and is then not active. Transmission is then controlled solely by the signal at the transmit gate pin.

Jabber Flag Pin

This pin will go to a logic high when the Jabber Control pin is used to shut off the transmitter. It will latch and can be reset by applying a logic low to the Jabber Control pin.

NOTES:

1. The NE5080 is capable of transmitting up to 1M baud of differential Manchester code at a center frequency of 5MHz.
2. Although the chip is designed to meet the requirements of IEEE standard 802.4 (Token-Passing Single-Channel Phase-Continuous-FSK Bus), it can be used at other frequencies. See "Determining Component Values."

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply voltage	+6	V
V_{IN}	Input voltage range (Data, Gate)	−0.3 to $+V_{CC}$	V
P_D	Power dissipation	800	mW
T_A	Operating temperature range	0 to +70	°C
T_J	Max junction temperature	+150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C

NE5080 PIN FUNCTION

PIN	FUNCTION
1	**OSC 1:** One end of the external capacitor used to set the carrier frequency.
2	**Jabber Flag:** This pin goes to a logic high if the transmitter attempts to transmit for a longer time than allowed by the Jabber control function.
3	**Jabber Control:** Used to control transmit time. See note on Jabber function.
4	**V_{CC1}:** Voltage supply.
5	**Transmit Gate:** A logic flow on this pin will enable the transmitter; a logic high will disable it.
6	**Transmitter FSK Output**
7	**Cable Ground:** The shield of the coax cable should be connected to this pin and to Pin 11.
8	**V_{CC2}:** Connect to Pin 4 close to device.
9	**No Connection**
10	**No Connection**
11	**Ground 2:** Connect to Analog ground close to device.
12	**OSC 3:** A variable resistor between this point and ground is used to set the carrier frequencies.
13	**Ground 1:** Connect to Analog close to device.
14	**Data Input**
15	**Regulator Bypass:** A bypass capacitor between this pin and V_{CC1} is required for the internal voltage regulator function.
16	**OSC 2:** One end of a capacitor that is between Pin 1 and Pin 16 and is used to set the carrier frequency.

DC ELECTRICAL CHARACTERISTICS $V_{CC1,\ 2} = 4.75 - 5.25V$, $T_A = 0°C$ to $+70°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_1	Output frequency (Logic high)	Data input $\geq 2.0V$ (See Note 1)	6.17	6.25	6.33	MHz
f_0	Output frequency (Logic low)	Data input $\leq 0.8V$ (See Note 1)	3.67	3.75	3.83	MHz
V_O	Output amplitude	Data input $\geq 2.0V$ or $\leq 0.8V$ Output Load = 37.5Ω	0.5		1.0	V_{RMS}
R_{OFF}	Output impedance (gated off)	Transmit gate $\geq 2.0V$	100			$k\Omega$
R_{ON}	Output impedance (gated on)	Transmit gate $\leq 0.8V$			37.5	Ω
C_O	Output capacitance	Transmit gate $\geq 2.0V$ or $\leq 0.8V$			10	pF
V_F	Feedthrough	Transmit gate $\geq 2.0V$ 2.0MHz sq. wave (TTL levels) input			1	mV_{RMS}
I_J	Jabber current	Transmit gate $\leq 0.8V$ Input $\geq 2.0V$ or $\leq 0.8V$		1.25		μA
I_{CC}	Supply current	V_{CC1} connected to V_{CC2}		75	100	mA
Logic levels						
	Data Input					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	$V_{IN} = 2.4V$			40	μA
I_{IL}	Input current	$V_{IN} = 0.4V$			−1.6	mA
	Transmit gate					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	VG = 2.4V			40	μA
I_{IL}	Input current	VG = 0.4V			−1.6	mA
	Jabber flag					
V_{OH}	Logic high	$I_{OH} = -400\mu A$	2.4			V
V_{OL}	Logic low	$I_{OL} = 4.0mA$			0.4	V
	Jabber control					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V

NOTE:
1. Tuned per instructions in AN195.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_S	Setup time	Data in	Gate on	Figure 1	2	0.1		μs
t_A	Delay time	Output freq. change	Data transition	Figure 2			150	ns
t_B	Delay time	Output disabled	Gate off	Figure 3		0.4	2	μs
t_C	Delay time	Output disabled	Jabber control	Figure 4			100	ns
t_D	Delay time	Jabber flag	Jabber control	Figure 5			100	ns
	Jabber control reset Pulse width (Logic low)				100			ns

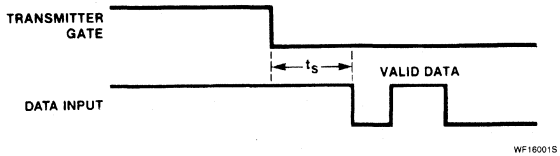


Figure 1. Setup Time, t_S

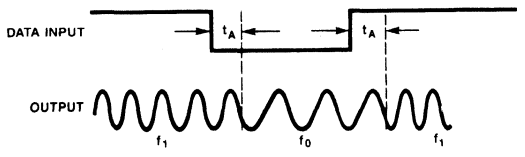


Figure 2. Delay Time, t_A

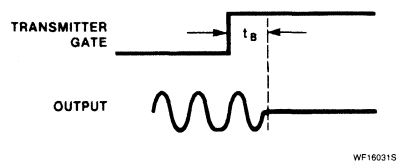


Figure 3. Delay Time, t_B

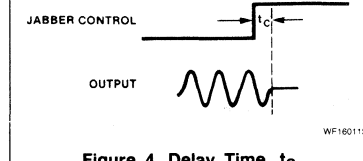


Figure 4. Delay Time, t_C

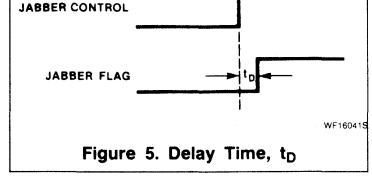


Figure 5. Delay Time, t_D

NE5081
High-Speed FSK Modem Receiver

Preliminary Specification

DESCRIPTION

The NE5081 is the receiver chip of a two-chip set designed to operate as an FSK modem (the NE5080 is the transmitter chip). The chips are compatible with the IEEE 802.4 standard for a "Single-Channel Phase-Continuous-FSK Token Bus." The specifications given in this data sheet are those guaranteed when the receiver is tuned to the frequencies in the 802 standard. However, the receiver will work at other frequencies.

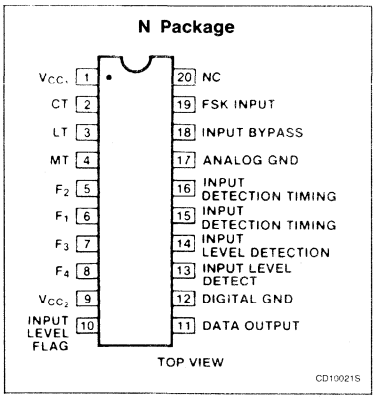
FEATURES

- **Meets IEEE 802.4 standard**
- **Data rates to several Megabaud**
- **Half- or full-duplex operation**
- **Low bit rate error (10^{-12} typical)**

APPLICATIONS

- **Local Area Networks**
- **Point-to-point communications**
- **Factory automation**
- **Process control**
- **Office automation**

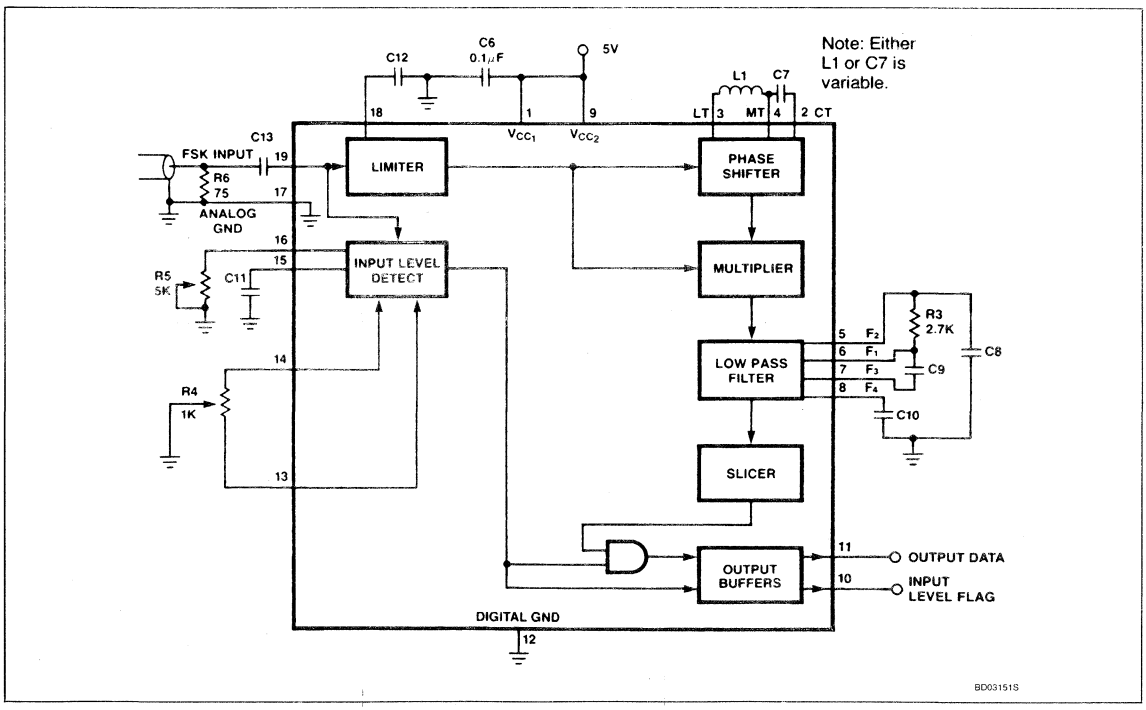
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE5081N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply voltage	+6	V
V_{IN}	Input voltage range	−0.3 to $+V_{CC}$	V
I_{DO}	Output (Data, Level detect) Max sink current	20	mA
P_D	Maximum power dissipation, $T_A = 25°C$, (still-air)[1] N package	1690	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C
	Max differential voltage between analog and digital grounds	100	mV

NOTE:
1. Derate above 25°C as follows:
   N package at 13.5mW/°C.

DC ELECTRICAL CHARACTERISTICS $V_{CC1, 2} = 4.75 - 5.25V$. External LC circuit tuned to 5MHz. Input level detect set at $16mV_{RMS}$, $T_A = 0°C$ +70°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_0	Logic Low Frequency	External LC tuned to 5MHz	3.67	3.75	3.83	MHz
f_1	Logic High Frequency	External LC tuned to 5MHz	6.17	6.25	6.33	MHz
IN_{DL}	Minimum Input Detect Level	Minimum input level that is detected as carrier (See Note 2 in General Description)	5		50	mV_{RMS}
	Logic Levels:					
V_{OL}	Data Output	$I_{OL} = 4.0mA$ $V_{IN} > 16mV_{RMS}$ Freq = f_0			0.4	V
V_{OH}	Data Output	$I_{OH} = -400\mu A$ $V_{IN} > 16mV_{RMS}$ Freq = f_1	2.4			V
V_{OH}	Data Output	$I_{OH} = -400\mu A$ $V_{IN} < 5mV_{RMS}$ Freq = f_0	2.4			V
V_{OL}	Input Detect Flag	$I_{OL} = 4.0mA$ $V_{IN} = 0V_{RMS}$			0.4	V
V_{OH}		$I_{OH} = -400\mu A$ $V_{IN} > 16mV$	2.4			V
I_{CC}	Supply Current	$V_{CC} = 5.25V$ (V_{CC1} connected to V_{CC2}) $V_{IN} = 1.0V_{RMS}$ Freq = f_1 or f_0			50	mA
BER	Bit Error Rate	Input Signal > $16mV_{RMS}$ maximum in-band noise = $1.6mV_{RMS}$		10^{-12}	10^{-9}	

AC ELECTRICAL CHARACTERISTICS (AN195, Figure 5 with a 100KHz $1V_{P-P}$)

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_B	Delay Time	Input Level Detect Flag	Input On	Figure 1		0.05	1	μs
t_C	Delay Time	Input Level Detect Flag	Input Off	Figure 1	0.5	1.5	2.5	μs
t_D	Delay Time	Output Enabled	Input On	Figure 2			2	μs
t_E	Delay Time	Output Disabled	Input Off	Figure 2	0.5	1.5	2.5	μs
	Required Delay	Carrier Turn Off	Valid Data End		2			μs

GENERAL DESCRIPTION

The NE5081 will accept an FSK-encoded signal and provide the demodulated digital data at the output. It is optimized to work at frequencies specified in IEEE 802.4 — Token-Passing Single-Channel Phase-Continuous-FSK Bus — (i.e., 3.75MHz and 6.25MHz). However, it will work at other frequencies.[1]

Its normal acceptable input signal level range is from $16mV_{RMS}$ to $1V_{RMS}$. This can be adjusted.[3]

The receiver will yield an undetected "Bit Error Rate" of 10^{-9} or lower when receiving signals with a 20dB signal-to-noise ratio. It has a maximum output Jitter of ± 40ns.[3]

NOTES:

1. The receiver can be tuned to accept different frequencies by adjustment of the LC circuit shown in Figure 7. However, the external components have been optimized for 3.75MHz and 6.25MHz. See "Determining Component Values" for use at other frequencies.
2. Input Level Detect
   This is a method of turning off the output of the receiver when the input signal falls below an acceptable level. This level is adjustable within the range given in the electrical specification section. The purpose of this function is to minimize the effect of noise on receiver performance and to indicate when there is an acceptable signal present at the input. All specifications given in this data sheet are with the input level detection set at $16mV_{RMS}$.
3. Jitter (Definition)
   This is a measure of the ability of the receiver to accurately reproduce the timing of its FSK-coded digital input. The spec indicates the error band in the timing of a logic level change.

NE5081 PIN FUNCTION

PIN	FUNCTION
1	**V_{CC1}:** Should be connected to the 5V supply and Pin 9
2	**CT:** One end of an external capacitor that is used to tune the receiver
3	**LT:** One end of an indicator that is used to tune the receiver
4	**MT:** The junction of the capacitor and inductor used for tuning the receiver
5	**F2**
6	**F1** Pins 5, 6, 7, 8 are used for a low-pass filter to remove carrier
7	**F3** harmonics from the data output
8	**F4**
9	**V_{CC2}:** Connect to Pin 1 (see Pin 1 function) close to the device
10	**Input Level Flag:** This pin is used to indicate when there is a signal at the input that is greater than the level set by the input level detection circuitry. A logic high indicates an input greater than the set level
11	**Data Output:** Supplies T^2L level data that corresponds to the FSK input received
12	**Digital Ground:** Should be connected to digital ground
13 and 14	**Input Level Detect:** These pins are used to set the level of input signal that the device will accept as valid
15	**Input Detection Timing:** An external capacitor between this pin and ground is used to determine the time from carrier turn-off to output disable
16	**Input Detection Timing:** Same as Pin 15, except that a resistor goes between this pin and ground. The values of the C and R depend on the carrier frequency. The values given in this data sheet are for a 5MHz carrier center frequency
17	**Analog Ground:** Connect to analog ground close to the device
18	**Input Bypass:** A capacitor between this pin and ground is used to bypass the input bias circuitry
19	**Input:** The FSK signal from the cable goes to this pin
20	**No Connection**

TIMING DIAGRAMS

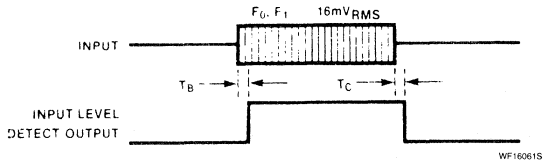


Figure 1. Delay Time, t_B, t_C

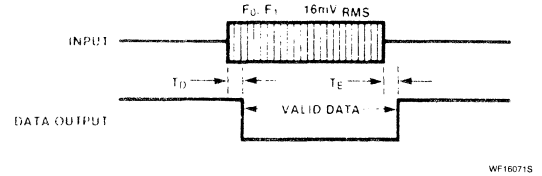


Figure 2. Delay Time, t_D, t_E

AN195
Applications Using the NE5080, NE5081

Application Note

APPLICATIONS

Figure 1 shows a block diagram of the NE5080 and NE5081 in a simple point-to-point communications scheme. Pin 5 of the NE5080 is grounded to permanently enable transmission; grounding Pin 3 disables the jabber function.

An example of a communications system block diagram using the NE5080 and the NE5081 (as in a modem) is shown in Figure 2.

The jabber function is active in this system. The NE5080 Jabber Flag (Pin 2) goes high when the capacitor at Pin 3 of the NE5080 charges to about 1.4V. This fault condition will interrupt the Transmission Controller, which will cease transmitting and write to the proper address for the decoder to put out a signal to discharge the capacitor. The Controller will then pass the token to the next node.

The transmission medium can be anything from a twisted pair to a fiber optic link. The NE5081 receives the FSK signal and converts it to a digital data stream corresponding to the data sent by the NE5080. Pin 10 of the NE5081 goes high when the signal at its input is above the threshold set by the potentiometer between Pins 13 and 14 of the NE5081.

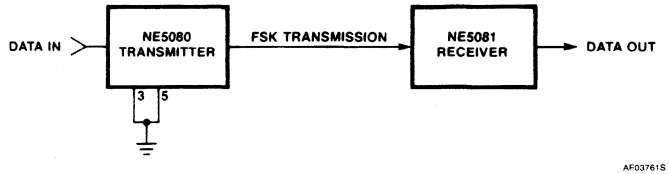


Figure 1. Point-to-Point Communications

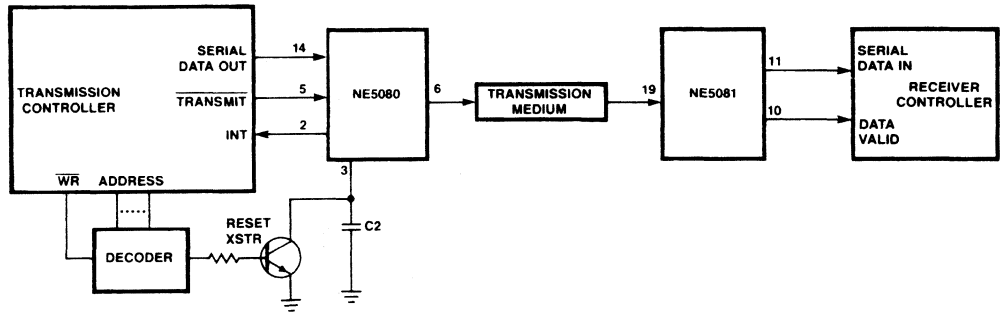
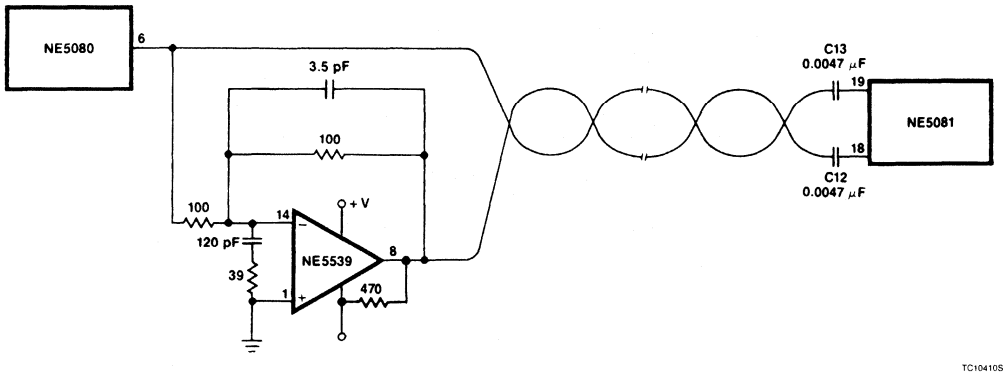


Figure 2. Communications System Block Diagram



NOTE:
In applications using twisted-pair lines where noise pick-up may be excessive, it is recommended that the twisted-pair be driven differentially.

Figure 3. Modem Using a Twisted-Pair Transmission Line

DC-to-2 Megabaud Modem Using the NE5080 and NE5081

The NE5080 and NE5081 are designed to be used together as an asynchronous modem. They employ FSK modulation at high carrier frequencies, plus filtering to reject EMI and RFI noise that is frequently encountered in industrial and commercial environments. Figures 4 and 5 show full- and half-duplex modems.

The carrier frequency is externally adjustable and can range from 50kHz to over 20MHz.

The modem can be used in a number of ways:

1. Multidrop party line of data transmitting and receiving devices (local area networks).
2. Point-to-point operation connecting just two transmitting/receiving devices.
3. Either of the above operated on one cable in the half-duplex mode.
4. Either 1 or 2 above operated on two cables in the full-duplex mode.

The 30dB dynamic range of modems built using the NE5080 and NE5081 makes it possible to attach them at any point on the cable without any gain adjustment. There is no problem with proximity to other similar modems.

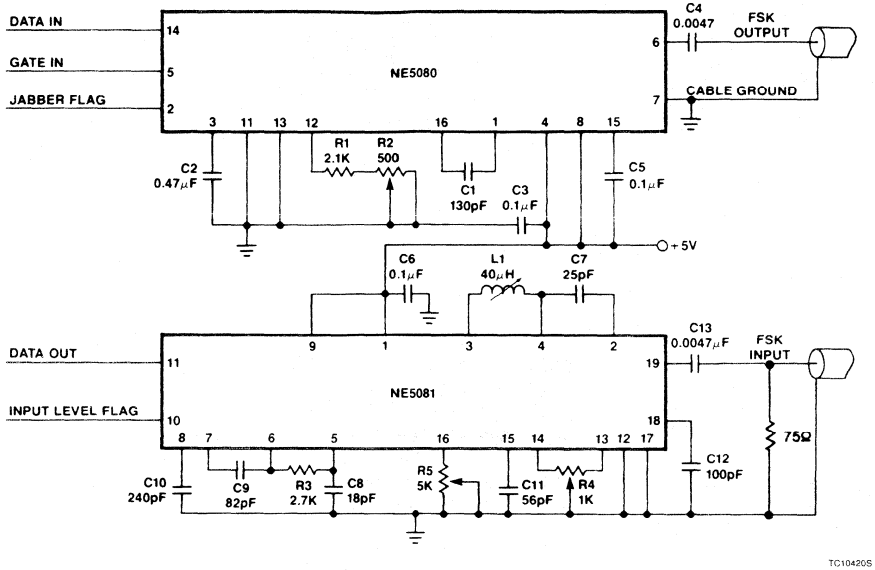
The distance that can be driven varies with the type of cables used, the number of modems attached to the cable, and the carrier frequency.

Typical operation can be 100 modems randomly spaced on up to 2000 meters of RG-11 (foam) cable with a center frequency of 5MHz.

In point-to-point operation, one can drive further. Table 1 gives obtainable distances when different carrier frequencies and cables are used.

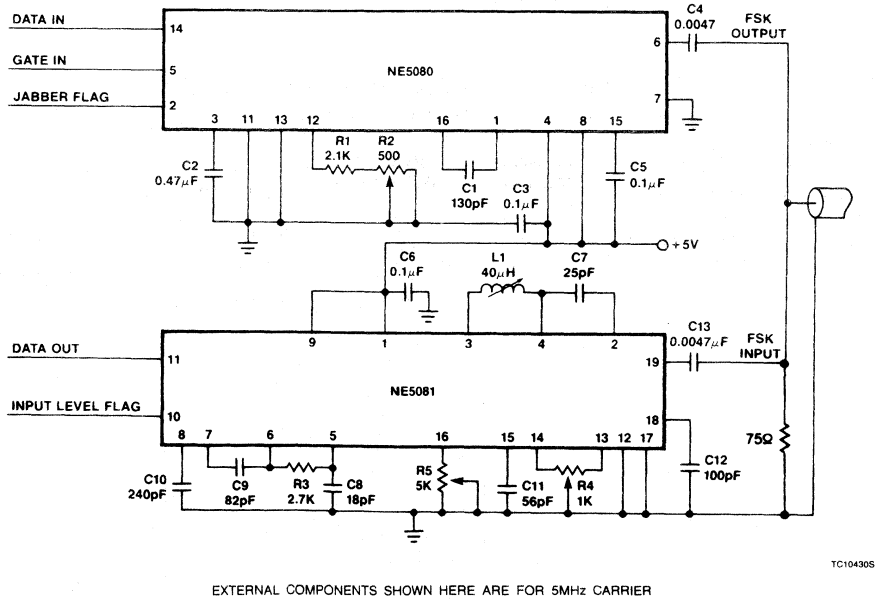
Table 1. Transmission Distance for a Single Receiver as a Function of Center Frequency and Cable Type

CARRIER FREQUENCY	MAXIMUM DATA RATE	CABLE			
		RG-59	RG-11 (Foam)	T4412J	T4750J
1MHz	0.5 Megabaud	6000 Ft	21000 Ft	33000 Ft	50000 Ft
3MHz	1.0 Megabaud	5000 Ft	12000 Ft	20000 Ft	32000 Ft
5MHz	2.0 Megabaud	4200 Ft	9500 Ft	15000 Ft	25000 Ft



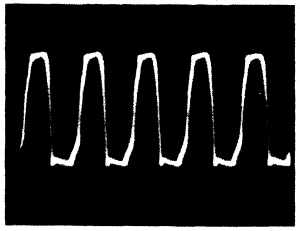
EXTERNAL COMPONENTS SHOWN HERE ARE FOR 5MHz CARRIER

Figure 4. NE5080 and NE5081 Connected as a Full-Duplex Modem



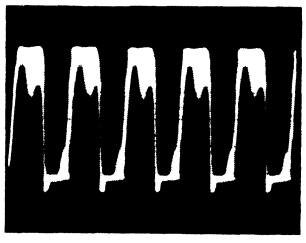
EXTERNAL COMPONENTS SHOWN HERE ARE FOR 5MHz CARRIER

Figure 5. NE5080 and NE5081 Connected as a Half-Duplex Modem



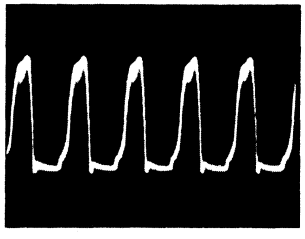
OP06580S

Figure 6. NE5081 Data Output When Correctly Tuned to Incoming 5MHz Carrier



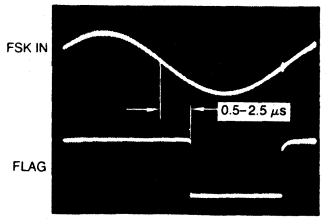
OP06590S

Figure 7. NE5081 Data Output When Tuned Just Below 5MHz Carrier



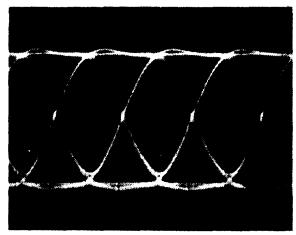
OP06600S

Figure 8. NE5081 Data Output Tuned Just Above 5MHz Carrier



OP06610S

Figure 9. Correct Adjustment of Input Level Detection Timing



OP06620S

Figure 10. 'Eye' Pattern at NE5081 Pin 8

FSK MODEM SETUP PROCEDURES

To set up the modem per IEEE 802.4 specifications, the following sequence should be followed at 25 ±2°C ambient.

TRANSMITTER SETUP:

1. Ground Jabber Control (Pin 3) and the transmit gate (Pin 5) of the NE5080.
2. Turn on the power and allow the circuit to warm up for 3 minutes.
3. Hold the Data Input (Pin 14) of the NE5080 at a logic high.
4. Measure the frequency at the FSK output of the transmitter (cable should be properly terminated) and adjust R2 for a frequency reading of 6.250MHz ±5kHz.
5. Apply a logic low to the Data Input and check the output frequency. If the reading is not 3.750MHz ±40kHz, readjust R1 until the high frequency is 6.250MHz ±25kHz and the low frequency is 3.750MHz ±40kHz.

Transmitter setup is now complete.

RECEIVER SETUP:

6. Set Detection Timing pot R5 and Input Level Detect pot R4 at the NE5081 to mid range.
7. Apply a 5.000MHz $1V_{P-P}$ sine wave to the receiver FSK Input.
8. Attach an oscilloscope probe to the Data Output pin of the NE5081 and adjust L1 or C7 (whichever is adjustable) until the output state alternates between high and low levels. Figure 7 and 8 indicate examples of improper tuning.
9. Set the generator to 3.750MHz, $35mV_{P-P}$.
10. Adjust Input Level Detect pot R4 until the Data Output pin is alternating between high and low levels.
11. Increase the generator output to $45mV_{P-P}$ and verify that the data output is low.
12. Decrease the generator output to $25mV_{P-P}$ and verify that the data output is high.
13. Apply a 100kHz $1V_{P-P}$ signal to the FSK Input and connect a scope probe to the Input Level Flag and another probe to the FSK Input. Adjust Detection Timing pot R5 so that the delay from the time the FSK Input signal goes through 0 volts on the Positive to negative transition, to the time when the Input Level Flag goes from high to low, is between 0.5 and 2.5µs. See Figure 9.
14. For final adjustment to the tuning of L1/C7 use an adjusted transmitter to transmit pseudo random data and tune the receiver L1/C7 tank circuit for minimum jitter and symmetrical eye pattern observed on the receiver Pin 8 (see Figure 10).

This concludes the receiver setup procedure.

DETERMINING COMPONENT VALUES

Power supply pins of both devices should be bypassed with high quality 0.1µF capacitors close to the devices. Additionally, the NE5081 V_{CC2} (Pin 9) should be well-decoupled from the power supply by a small inductor (about 10µH) and another 0.1µF capacitor as the NE5081 exhibits large changes in power supply current during switching.

The coupling capacitors C4 and C13 are needed to maintain input bias when a low DC impedance line is connected to the FSK Input. Too small a value for these capacitors could result in excessive signal attenuation. If these capacitors are too large, the receiver Input Level Flag may remain high for an excessive amount of time after the input signal is removed. Each transmitter and each receiver should have its own coupling capacitor. This is necessary to prevent any DC terminations from altering biases.

The external resistance at the NE5080 Pin 12 should always be about 2.4kΩ, with some adjustment allowable to compensate for the tolerance of C1 and slight differences between individual ICs.

C11 and R5 are the Carrier Detect timing components and determine how long after the FSK input signal is discontinued before the Input Level Flag goes low. R5 should not exceed 5kΩ. With C11 set at 56pF, a 5kΩ R5 will allow Carrier Detect Timing adjustment to 2μs. R5 can be a fixed resistor if this timing is not critical (perhaps because of the use of an "end of data" signal). This delay is required to allow the signal to propagate through the receiver. Carrier Detect Timing should be adjusted for different center frequencies by choosing C11 according to the relationship:

$$C11 = \frac{1}{3572\ f_C}$$

The Input Level Detect function can be disabled and the receiver be made to hold the Carrier Detect Flag high by removing R5 and C11 and tying Pins 15 and 16 together and pulling them up to V_{CC} with a 10kΩ resistor.

If the Jabber function is not to be used, Jabber control Pin 3 of NE5080 should be grounded. If the Jabber function is to be used, a capacitor, C2, should be connected between Pin 3 and ground. The value of this capacitor is determined as indicated below:

$$C2 = (0.95 \times 10^{-6})t$$

where t is the maximum allowable transmit time in seconds.

The resistance R1, together with capacitor C1, set the transmit frequencies. The logic high frequency is fixed at about 1.67 times the logic low frequency, meaning that the logic low frequency is 0.75 times the center frequency f_C, and the logic high frequency is 1.25 times the center frequency. Note that this center frequency is never transmitted in normal operation and is sometimes referred to as the "carrier frequency."

C1 is chosen by the relationship for f_C at or below 7MHz:

$$C1 = \frac{6.5 \times 10^4}{f_C}$$

Above 7MHz center frequency, this capacitor is found by modifying this equation to:

$$C1 = \frac{5.5 \times 10^{-4}}{f_C}$$

To get the characteristics that are needed for proper operation of the NE5081, it is important to keep the proper relationship between L1 and C7:

$$C7 = \frac{1}{7885\ f_C}$$

$$L1 = \frac{200}{f_C}$$

Capacitor values of the filter are dependent upon operating frequencies to maintain proper characteristics:

$$C8 = \frac{9.0 \times 10^{-5}}{f_C}$$

$$C9 = \frac{4.1 \times 10^{-4}}{f_C}$$

$$C10 = \frac{1.2 \times 10^{-3}}{f_C}$$

$$C12 = \frac{5 \times 10^{-4}}{f_C}$$

Coupling capacitor values also depend upon center frequency:

$$C4 = C13 = \frac{2.5 \times 10^{-2}}{f_C}$$

In all of the above equations, capacitances are in Farads, inductances in Henrys, and frequencies in Hertz.

SOME COMMON BAUD RATES

Although intended to be used with a center frequency of 5MHz, the NE5080 and NE5081 can be used at other center frequencies. Table 2 gives minimum center frequency (f_C) for some common baud rates, together with external component values for those center frequencies. Note that it is not recommended that these devices be operated at center frequencies below 50kHz.

USING THE NE5080/NE5081 WITH A FIBER-OPTIC LINK

The NE5080/NE5081 chip set is highly suitable for use in low cost fiber-optic links. There are many advantages to fiber links over open-wire or coaxial cable links. These advantages include:

1. Cost savings in conductor weight and size.
2. Immunity to EMI/RFI.
3. Low crosstalk.
4. High communications security; cannot be tapped by electromagnetic induction or surface conduction.
5. Fiber-optic cable does not radiate electromagnetic energy nor disturb other communications media.
6. Extremely wide bandwidth (high channel per conductor density).
7. Low attenuation.
8. No ground loops or shifts caused by common grounds.
9. Complete electrical isolation between transmitter and receiver.
10. Cable breaks cause no shorts, making this technology useful in hazardous environments, e.g., explosive chemical facilities.
11. No damage to equipment is expected due to current surges on adjacent lines.
12. Fiber cable does not act as an antenna to pick up high electromagnetic pulses such as those caused by electrical storms.
13. Low BER (Bit Error Rate).

The circuit of Figure 11 shows a simplex fiber link between the NE5080 transmitter and the NE5081 receiver. The components shown are for a center frequency of 5MHz, although this frequency can be increased to 20MHz with proper selection of external component values. The NE5539 has a 350MHz unity gain bandwidth which may limit maximum operating frequencies in some systems.

Since the NE5081 can adequately accept signals below 10mV at 5MHz carrier, the gain stage (within the dashed lines of Figure 11) may be eliminated if the attenuation in the link is low. If the gain stage is used, be mindful of the bandwidth trade-off at higher gains. Refer to the NE5539 data sheet for details.

The transmitter and receiver are set up as described under FSK Modem Setup Procedure.

LAYOUT PRECAUTIONS

As is the case with any components using high frequencies, good layout practice is essential; poor layout can adversely affect performance. All lead lengths should be as short as is practical for all lines which carry RF, including the tuning capacitor and resistors (C1, R1, R2) of the NE5080. Lead length is especially critical with C1, which should be mounted as close to the NE5080 as is possible. A printed circuit board with a good ground plane, both top and bottom, is also recommended (wire-wrap is NOT recommended). The ground plane should extend below tuning capacitor C1 on both top and bottom of the board, with no other trace coming between the leads of this capacitor.

Because of the high speed switching, Pin 9 (V_{CC2}) of the NE5081 can exhibit a large current swing, causing vertical output jitter which may be eliminated by decoupling Pin 9 with a small (10μH) RF choke and a 0.05μF capacitor.

See Figure 12 for an example of a working layout.

Table 2. Recommended Minimum Center Frequency and Component Values for Various Baud Rates

BAUD RATE (kBaud)	f_C (kHz)	C1	L1	C4 C13	C7	C8	C9	C10	C11	C12
9.6	50	13nF	4mH	0.50μF	2.4nF	1.8nF	8.2nF	24nF	5.6nF	10nF
19.2	50	13nF	4mH	0.50μF	2.4nF	1.8nF	8.2nF	24nF	5.6nF	10nF
38.4	100	6.8nF	2mH	0.27μF	1.3nF	0.9nF	3.9nF	12nF	2.7nF	5nF
50.1	125	5.1nF	1.6mH	0.20μF	1.0nF	750nF	3.3nF	10nF	2.2nF	3.9nF
64.0	160	3.9nF	1.3mH	0.15μF	800pF	560pF	2.5nF	7.5nF	1.8nF	3nF
128	320	2nF	625μH	0.075μF	390pF	270pF	1.3nF	3.9nF	860pF	1.6nF
256	640	1nF	312μH	0.039μF	200pF	150pF	640pF	1.8nF	430pF	750pF
512	1250	510pF	160μH	0.02μF	100pF	75pF	330pF	1.0nF	220pF	390pF
1500	3750	180pF	53μH	6.8nF	33pF	25pF	110pF	330pF	75pF	130pF
1544	4000	160pF	50μH	6.8nF	33pF	22pF	100pF	300pF	68pF	125pF
2000	5k	130pF	40μH	5.0nF	25pF	18pF	82pF	240pF	56pF	100pF
8000	20k	33pF	10μH	1.2nF	6pF	5pF	20pF	62pF	15pF	25pF

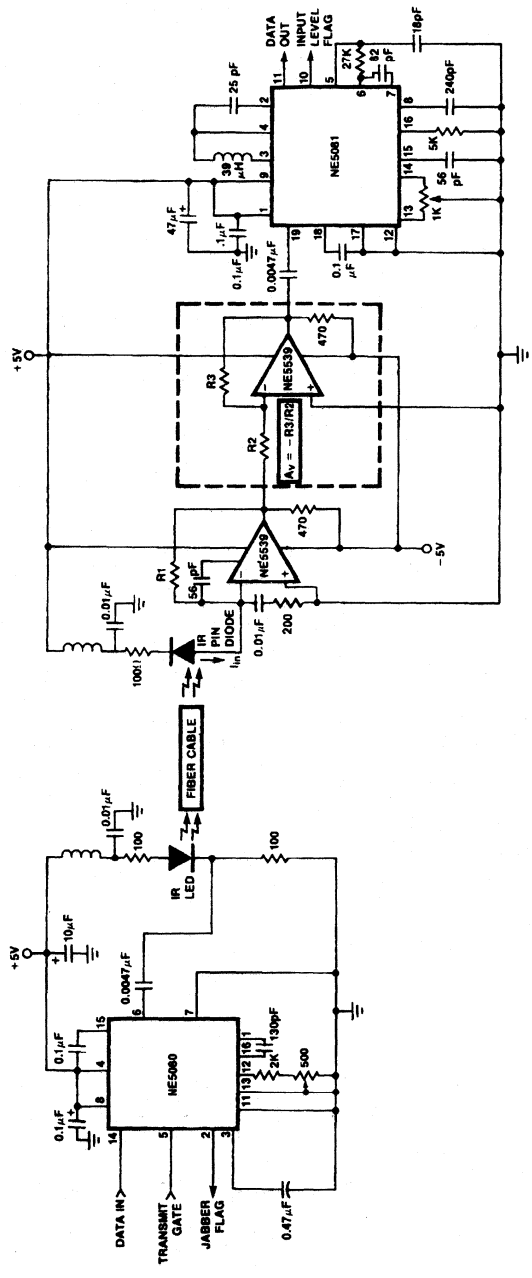
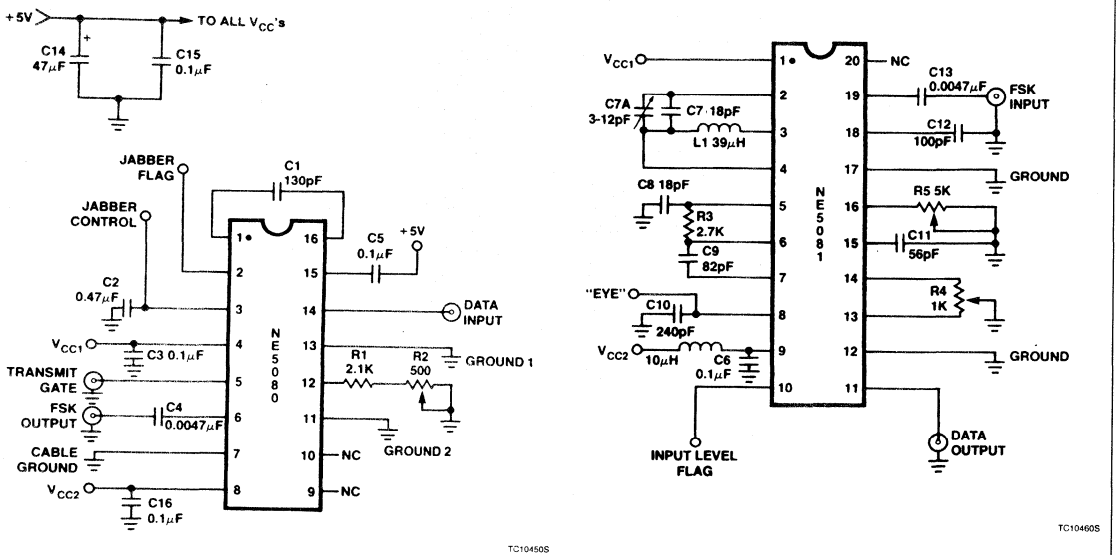
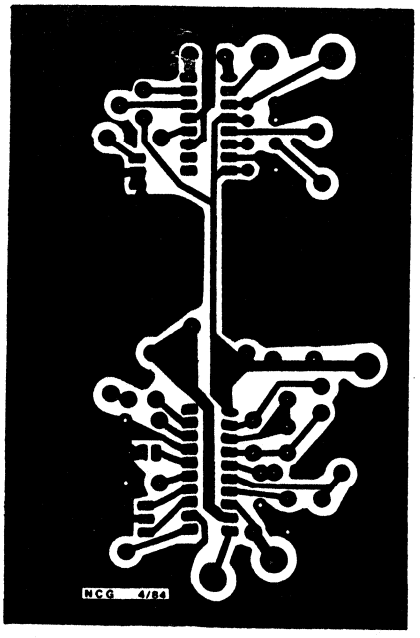


Figure 11. Simplex Fiber-Optic System



NOTE:
See NE5080 and NE5081 Block Diagram(s)

NOTE:
Signetics NE5080/NE5081 Evaluation Board



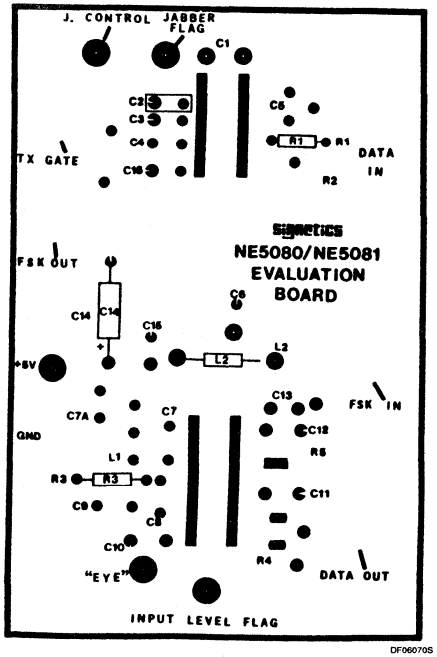


Figure 12. Components and Layout Used for Evaluation Board

AN1950
Application of NE5080 and NE5081 With Frequency Deviation Reduction

Application Note

INTRODUCTION

Application note AN195 discusses numerous applications of NE5080 and NE5081 in point-to-point, half-duplex and full-duplex communications using coaxial, twisted-wire pair, and fiber optic cables. It also discusses several aspects about tuning the transmitter and receiver at various center frequencies and board layout precautions. In this application note, the transmitter and receiver chips themselves are discussed. Following the brief circuit description, a few novel application ideas are discussed.

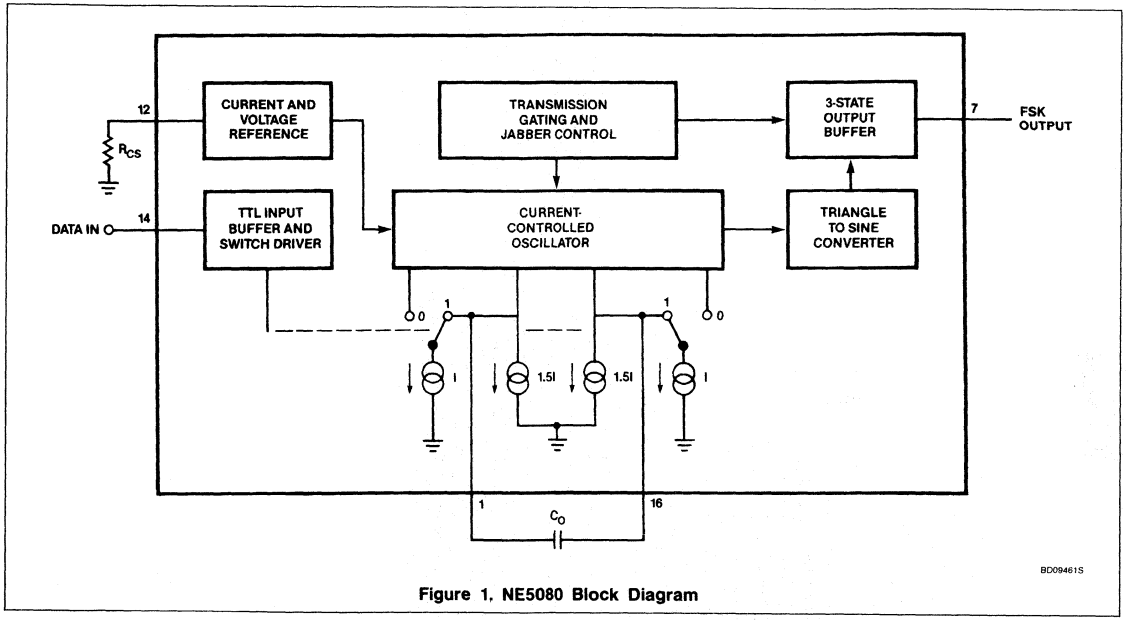


Figure 1. NE5080 Block Diagram

TRANSMITTER

The block diagram of the transmitter NE5080 is shown in Figure 1. The transmitter is composed of the following six major building blocks: a TTL input buffer and switch driver, a current controller oscillator, a triangle-to-sine wave converter, a 3-state output buffer, and transmission gating and jabber control circuitry. It also has an on-chip voltage regulator that provides current and voltage references to the various building blocks of the circuit.

The transmitter center frequency can be adjusted by selecting the values of the tuning capacitor, C_O. The switch driver circuitry switches the current sources I in and out of Pins 1 and 16. This effectively changes the total average charging and discharging current into C_O from 1.5I to 2.5I, which causes the output to shift from one frequency to another. This soft switching action keeps the output phase continuous and eliminates discontinuities. The ratio of the two output frequencies is equal to the ratio of the total average current charging and discharging C_O. Since the values of the internal current sources are fixed, it produces a constant frequency ratio of 1.66. An external modification for changing this ratio through extra components is discussed later.

The triangle-to-sine wave converter circuitry converts the output of the current-controlled oscillator into a sine wave with about 2% distortion. The transmission gating and jabber control circuitry controls the FSK output through the 3-state output buffer. The transmit gate, when held high, will inhibit the transmission by putting the output buffer into the high impedance state. It also turns off the current-controlled oscillator, thus minimizing any feedthrough to the output.

The jabber control function is similar to the transmit gate, but the transmission time can be programmed through an external capacitor. There is a small current sourced to the jabber control pin, which charges up the capacitor. When the voltage on the capacitor reaches a preset threshold level, the transmission is stopped. This is a failsafe feature provided to restrict an errant transmitter or the NE5080 itself from tying up the network. In point-to-point communications, the jabber control can be disabled by connecting the jabber control pin to ground.

Application of NE5080 and NE5081 With Frequency Deviation Reduction

AN1950

RECEIVER

The receiver block diagram shown in Figure 2 is composed of the following seven major building blocks: an input limiter, a phase shifter, an analog multiplier, a low-pass filter, a comparator, an input level detector, and a TTL output buffer. The input limiter limits the FSK input signal eliminating any amplitude variations.

The L and C tank circuit of the phase shifter is tuned to resonate with the incoming carrier center frequency. A quadrature detection scheme is used to demodulate the data. The balanced analog multiplier processes the incoming signal with its phase-shifted carrier frequency and generates signals with baseband data and other higher order harmonics.

The low-pass filter is a simple second-order Butterworth filter which eliminates the carrier frequency and higher-order intermodulation frequencies, and gives the baseband data which is equivalent to the signal modulated by the transmitter. The comparator makes the decision based on the output of the low-pass filter with reference to a threshold voltage. The TTL buffers provide the output data at TTL levels. The input detection level can be adjusted through the external resistor to set the threshold for minimum input level. If the input level falls below the set threshold, the output buffers are disabled, preventing the noise from being interpreted as data.

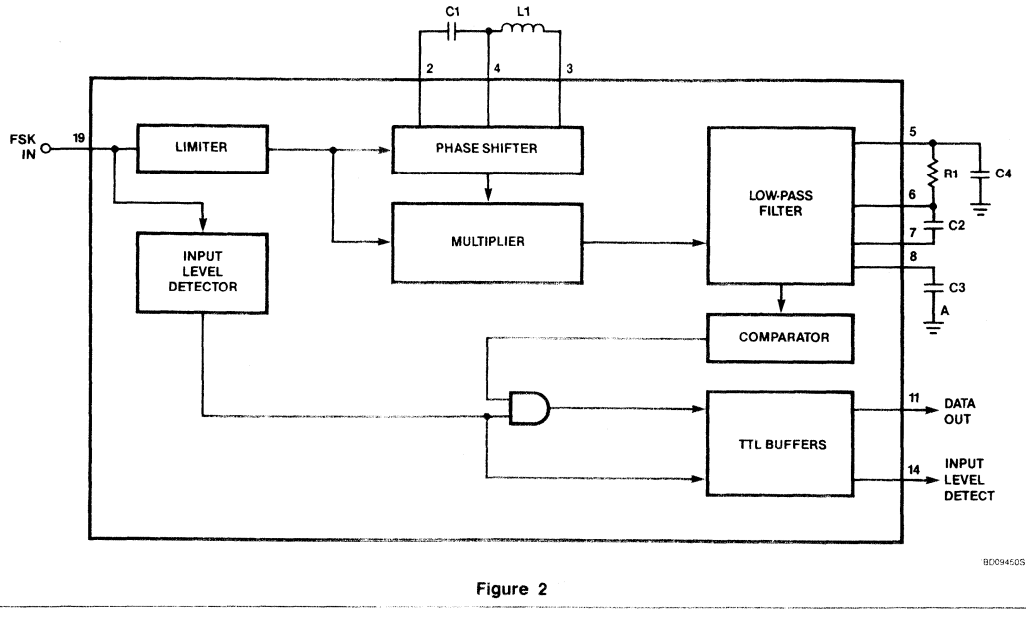


Figure 2

Application of NE5080 and NE5081 With Frequency Deviation Reduction

AN1950

APPLICATIONS

NE5080 AND NE5081 chip set encompasses a broad spectrum of data rates and facilitates economical modem design for various applications. The transmitter can be tuned to various center frequencies for different data rates. The wide dynamic range of the receiver and the excellent drive capability of the transmitter make it possible to drive long distances without any signal repeaters. The transmitter is not limited to transmitting on coaxial cable only; it can also drive a twisted-wire pair and optical fibers. All these salient features are discussed in greater detail in AN195.

The major focus of this application note is on reducing the frequency deviation. The reduction in frequency ratio can be achieved by bringing the two frequencies f_0 and f_1 closer together. This will reduce the overall bandwidth utilized by the modem because the main lobe in the spectrum becomes narrower. This gain in bandwidth reduction is offset by a slight increase in the probability of a bit error due to poor noise margin. As explained in the transmitter block diagram section of this application note, the frequency of the oscillator is controlled by the charging and discharging current into C_O. The two oscillating frequencies can be brought close together either by lowering the higher frequency f_1 or by raising the lower frequency f_0. Figure 3 shows the technique for raising the lower frequency f_0. When the logic input is a '1', the two diodes are reversed biased. In this situation, the capacitor is charged and discharged by the current from the internal current sources. As the logic input changes to a '0', the two diodes are forward biased. This will increase the available current from the internal current sources that are charging and discharging the capacitor C_O, thus resulting in a higher frequency of oscillation than would be obtained otherwise. The value of resistor R will determine the amount of excess current available, which will affect the ratio of the higher frequency to the lower frequency (f_1/f_0).

Figure 4 gives a graph of the deviation ratio versus the resistor value R for different values of oscillator capacitor C_O. It can be seen from the graph that the deviation ratio remains constant for a fixed value of resistor R over a wide range of capacitor values C_O. It should be noted that the effective data rates will be lower when the frequency deviation is reduced. A similar scheme can also be applied to increase the frequency ratio and thereby increase the data rate, but this will be done at the cost of extra bandwidth. Using appropriate filters for the transmitters and receivers, a frequency division multiplexing (FDM) can be achieved for more efficient usage of the most expensive resource, namely the coaxial cable.

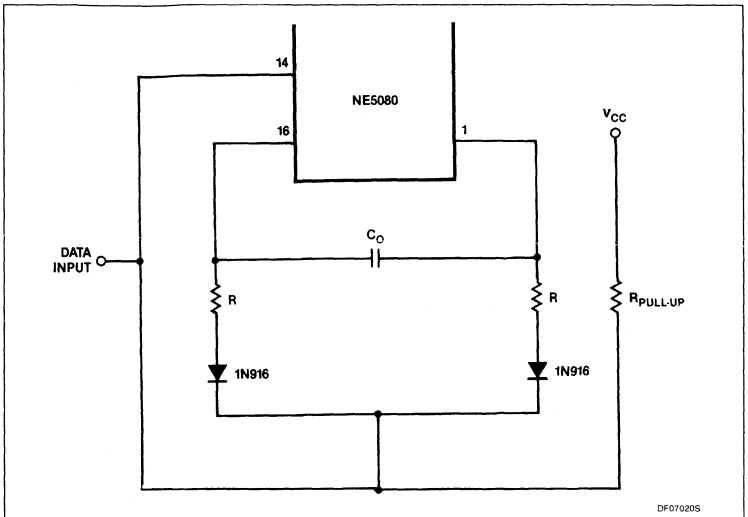


Figure 3

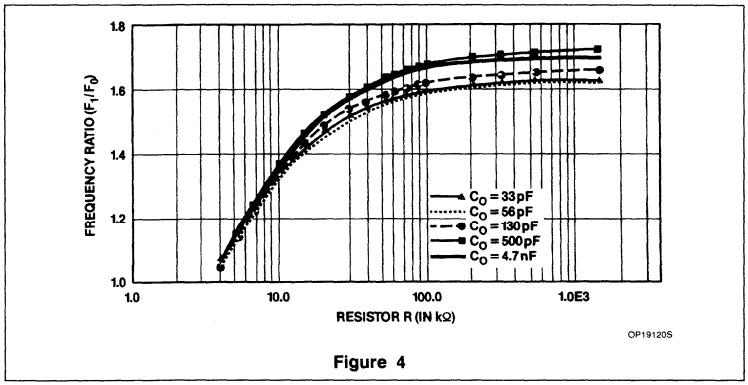


Figure 4

AN1951

NE5050: Power Line Modem Application Board Cookbook

Application Note

INTRODUCTION

Applications Disclaimer

The applications outlined within this cookbook in no way specify the absolute maximum performance of the NE5050 Power Line Modem. They are merely examples given to show the flexibility of the part. In general, the external components used for each application tend to be the limiting factors in each application. For example, the component drift for capacitors that provide a load on the oscillator would cause a corresponding drift in the oscillator frequency, although there is nothing wrong with the chip itself. On the other hand, external drive transistors provide a larger transmitter voltage than what would normally be available from direct drive with the chip.

Only careful characterization of the operating environment (whether it is the power line, twisted pair, or coaxial cable) coupled with a knowledge of the external component limitations, can ensure reliable operation for a given application. Often, operating problems originate with an applications fault rather than with the chip itself.

One reason that the part may not always work in every situation is the same reason that it can work in so many situations — the part is extremely flexible. Operation is dependent on the values of the external components. For instance:

- To change the carrier frequency, change the oscillator capacitor and inductor. To receive the same signal, however, the BPF values must also be changed to the same values. Active filters or no filters can be used. The tuning capacitor must also be changed so that the transformer secondary locks onto the carrier. The oscillator can also be driven with an external source.
- To adjust the limiting of the data rate, the detection capacitor has to be changed. If the data rate is increased without adjusting this capacitor, the bit rate will be RC-filtered out.
- Adjusting the impulse capacitor will provide protection from transients of a certain duration, but leaves a vulnerability to longer ones or a succession of smaller ones.

Each of these cases should illustrate the fact that the performance of the board is extremely application and environment dependent. The environmental parameters and goals of data transmission should be determined before specifying component values. Proper operation depends on it.

Summary of Operation

The AC power line is, in general, not ideal for data communication. Impulse noise, large magnitude voltage transients (> 1kV typical), line impedance modulation, and other factors, have prohibited its use as an effective medium for transmitting data and control signals.

The NE5050 Power Line Modem (PLM) has been designed to overcome these problems while affording the user the flexibility of tailoring the design to his/her own needs. The PLM can be used to transmit over power lines or twisted-pair cables using two forms of modulation — carrier on/off ASK (Amplitude Shift-Keying) and non-coherent FSK (Frequency Shift-Keying). To use it in the FSK mode, two devices will be required for each transceiver in order to bandpass and generate the two different frequencies representing logical 0 and 1. If one of the two frequencies used fails, the remaining frequency can be used in the ASK mode. The applications referred to in this cookbook only refer to the single-carrier ASK form. Some of the features of the IC include:

Listen-While-Talk

The modem is always in the receive mode, even when transmitting (it receives its own signal). This capability permits RX and TX remote functionality testing for each system node since it requires no other transceivers. In the receive mode, the modem receives carrier signals from other transmitters. In the transmit mode, the IC transmits an ASK carrier to the other receivers, including its own. It is up to the user to design protocol to arbitrate ownership of the line. In some protocols, such as in General Electric's HOMENET®, the listen-while-talk feature is not desired and so the receiver is disabled during transmission mode.

On-Chip Collision Detection

The listen-while-talk capability enables a controller to perform CSMA/CD (Carrier Sense, Multiple Access/Collision Detect) functions. To summarize (for further information, the reader is referred to IEEE 802.3 and to general articles describing ETHERNET or other probabilistic network protocols), any node can access the line to transmit signals at any time provided the line is not being used. The procedure is as follows. A receiver listens to the line to see if there are any carriers present (Carrier Sense). Every receiver is also listening to the line (hence, Multiple Access). If a transmitter is on, each node waits until the line is free before transmitting. Priorities may be established by the controller. A collision is detected if, while transmitting a message, an incoming transmission originating from another node is detected.

The PLM performs a similar operation for both dense and rare data traffic situations. In dense data traffic, the RX data output (RX_{OUT}) does not have time to go into the standby (low power consumption, inverted logic mode). In this case, the RX_{OUT} is in positive logic (carrier on = 1, carrier off = 0). A collision is detected at the local node when the local TX is off and the local $RX_{OUT} = 1$. Therefore, a remote carrier is present and has been detected, so abort local transmission. The line is busy. Wait until the line is clear.

In rare data traffic, the RX_{OUT} is usually in the standby mode. In this case, the RX_{OUT} logic mode is inverted due to a designed-in offset present in the AM rejection and impulse filter circuits. A "10" logic sequence from the local TX insures proper RX offset adjustment (the preamble contains the first two "10" bits) and collision detection can be performed with the next "10" bits. The collision detection proceeds as in the dense data traffic case. The transition time from the last received bit "1" to the standby mode is typically 4 seconds and this time is independent of the data rate. This enables long strings of "0's" to be transmitted and received.

To eliminate the standby mode and to have the modem in the receive-data mode at all times, the bias at Pin 9 should be altered. A 10MΩ resistor from Pin 9 to a potential of $2.2V_{DC}$ will perform this change. The 2.2V potential may be generated between two resistors: 1MΩ from V_{CC} = 12V and 220kΩ to ground.

Power Supply Decoupling (C1 and C2)

Capacitor $C_1 = 0.1\mu F$ at Pin 1 decouples the supply voltage, V_{CC}. The capacitor $C_2 = 0.1\mu F$ at Pin 14 is optional and decouples the supply for the oscillator section. This

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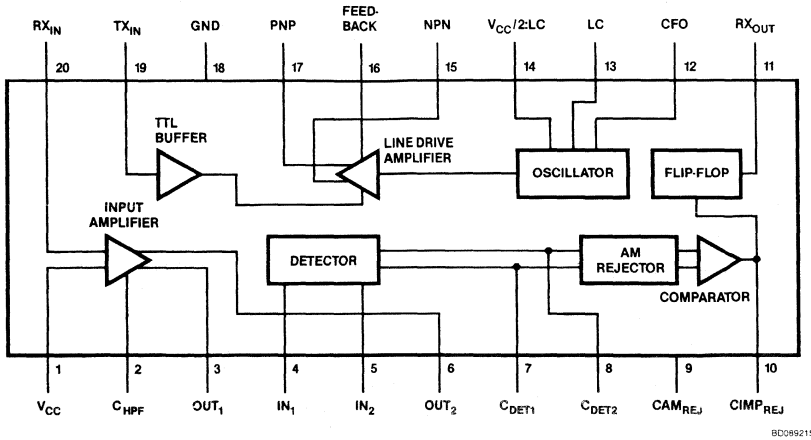


Figure 1. Block Diagram

supply, $V_{CC}/2$, is internally generated. C_1 is essential for clean operation and should be placed as close as possible to the IC, between Pins 1 and 18.

AC Line Coupling

The line transformer, a Toko America 707VX-T1002N, has a primary-to-secondary coil ratio, L_1:L_2, of 1:1. One end of coil L_1 goes to the power line via line capacitor C_{LINE}. The secondary signal is tapped off between L_2 and L_3 and then goes to the receive input (Pin 20.) The other turn ratio is L_1:L_3 at 1:4. The L_2 secondary is connected between Pins 1 (V_{CC}) and 20 (RX_{IN}). It carries about $1mA_{DC}$ current into Pin 20 for biasing. The $L_2 + L_3$ secondary is tuned to the carrier frequency by a tuning capacitor C_{TUNE} = 6.8pF. This transformer is suitable *only* for data rates up to 10kBits/sec because of envelope distortion.

To tune the transformer for maximum sensitivity, connect a BNC "T" connector to the output of the waveform generator. One output should go to an oscilloscope and the other should be connected to the prongs of the power cord of the board (make sure ground is also connected to one prong). Then send the 100% AM modulated pulse train (ASK) to the board. The carrier envelope is a square-wave pattern. Tune the transformer for maximum carrier amplitude. To do this take a jewelhead screwdriver and adjust the transformer core. Maximum sensitivity is reached at maximum amplitude at the carrier frequency.

Another manufacturer that provides good transformers for both power line and twisted-pair communication is AIE Magnetics (Address and telephone numbers for TOKO and AIE Magnetics are listed in the External Components Section).

Line and Tuning Capacitors (C_{LINE} and C_{TUNE})

C_{LINE} = 1μF AC-couples the transformer to the power line and is rated to withstand 600V. Its main function is to filter out the 60 and 120Hz signals from the line power and to pass only the higher frequency carrier signals. C_{LINE} and the primary inductance of the transformer act as a voltage divider that attenuates 60Hz signals by 100dB. Line voltage signals are less than a millivolt on the secondary of the coupling transformer. Remember to discharge this capacitor before removing the insulating backplane and changing components.

C_{TUNE} = 6.8nF tunes the transformer secondary winding to the carrier frequency (100kHz). Make sure to change this capacitor in addition to the LCs of the oscillator and bandpass filter sections when changing the carrier frequency.

TRANSCEIVER EXTERNAL COMPONENTS

Figure 1 is a block diagram of the NE5050. It comes in a 20-pin DIP (Dual In-Place package) in both plastic and SO (Small Outline). This section describes the external components that must be added and the characteristics to expect at those pins.

Receiver

Input Filter C_{HPF} (Pin 2)

The input amplifier limits its output signals to $1.2V_{P-P}$ differential. On Pin 20, the maximum input carrier signal can be $70V_{P-P}$, centered at V_{CC}. The amplifier gain is 24dB at the carrier frequency. The input amplifier bandpass characteristic has an upper –3dB frequency internally fixed. The lower –3dB frequency is set by C_{HPF}. C_{HPF} actually suppresses the lower order harmonics. With C_{HPF} = 100nF, 60 and 120Hz are rejected more than 40dB (see Figure 2). For lower values of C_{HPF}, this rejection increases along the frequency spectrum. For a 1nF capacitor, amplifier response has large peaking near 500kHz. Response for values of 10, 100, and 1000nF are also shown over the frequency range 0.01 – 100MHz.

C_{HPF} is connected from Pin 2 to ground. For carrier frequencies above 100kHz, typical values for C_{HPF} are between 2 and 20nF. The amplifier has differential outputs (Pins 3 and 6). The DC voltage at these pins is 4.6V.

Inter-Stage Bandpass Filter R1, R2, C_{BPF}, L_{BPF} (Pins 3, 4, 5, 6)

If all necessary bandpass filtering is performed in the line-coupling network, then the BPF between input amplifier output and AM detector input is not needed. It is also possible to bypass use of the filter in most twisted-pair applications. Otherwise, for ASK operation, L_{BPF} and C_{BPF} should match the LC tank components L_{OSC} and C_{OSC} of the oscillator in order to have effective carrier sense. The carrier frequency is simply defined as

$$\omega_{CXR} = \frac{1}{\sqrt{L_{BPF} \times C_{BPF}}}$$

The bandpass characteristics are governed by the following equations relating 3dB band-

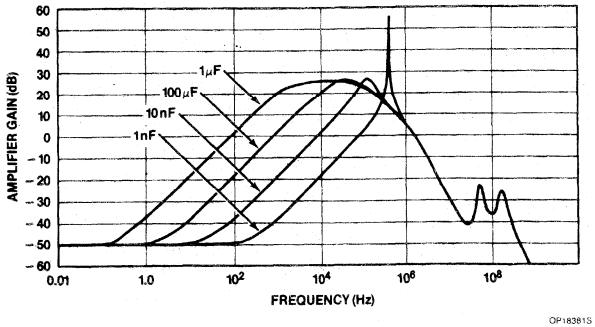


Figure 2. Receiver Amplifier Gain vs Frequency for Different Values of C_{HPF}

width to carrier frequency ω_{CXR} and components R_1, $R_2 = R$, L_{BPF}, and C_{BPF}.

$$BW_{-3dB} = \frac{(\omega_{CXR}{}^2 \times L_{BPF})}{(2 \times R)}$$

$$BW_{-3dB} = \frac{1}{(C_{BPF} \times 2 \times R)}$$

These equations can easily be manipulated to express the Quality factor, Q:

$$\frac{BW_{-3dB}}{\omega_{CXR}} = \frac{(\omega_{CXR} \times L_{BPF})}{(2 \times R)} = \frac{1}{Q}$$

$$\frac{BW_{-3dB}}{\omega_{CXR}} = \frac{1}{(\omega_{CXR} \times C_{BPF} \times 2 \times R)} = \frac{1}{Q}$$

Since this is a passive filter, a good deal of signal attenuation should be expected. If there is trouble getting signals through, consider shorting out the bandpass by shorting Pin 3 to Pin 4 and Pin 5 to Pin 6. If this does not work, trace signal from RX_{IN} (Pin 20) and follow through.

Depending on the filtering configuration, Pins 4 and 5, the AM detection input requires DC biasing. If no DC path is provided from Pin 3 to 4 and from 6 to 5 (series capacitors present for DC open-circuit), then the network in Figure 3 can be used.

Active bandpass filters may be used if gain is desired in the signal. This allows more room for tweaking. Remember, the goal is to bandpass the broadband signal (ω_{CXR} = 100kHz for the industrial operation) and *not* the baseband signal (1kBits/s for the same application) as can be seen from the above equations. For more details on alternative BPFs, see the section on High Performance Industrial Operation.

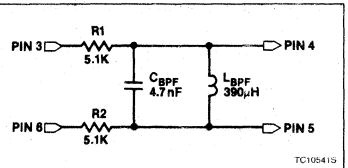


Figure 3. Single-Pole Bandpass Filter for 118kHz Operation

AM Detection C_{DET} (Pins 7 and 8)

The capacitor C_{DET} is the load across the collectors of a Gilbert multiplier cell (Pins 7 and 8) that is being multiplied by itself. So compared signals are always in phase and demodulated output is a function of carrier amplitude (hence, detects AM signals), bias current, and collector load. (Internally there are resistors in the collectors of the cell so the part *will* run without C_{DET} included.) Since it is the load, it has to be charged and discharged, and thus delays the transition of the signal. C_{DET} introduces a delay in signal transmission because of its integrating action. The combination of C_{DET} and the collector resistors provides an RC low-pass filtering action on the received signal. The carrier (broadband) is filtered out and only the envelope (baseband) is passed. Consequently, C_{DET} provides the limiting value for the data rate. The 4.7nF value is fine for 1kBit/sec operation, but, if an increased data rate is desired, the value of the capacitor should be reduced. Similarly, for a longer delay and reduced data rate, increase C_{DET} (see Figure 4).

If C_{DET} is removed altogether, a reduction in signal delay should be observed (full-wave rectification). There will still be a signal if the impulse capacitor is connected. Removing both C_{DET} and C_{IMP} should eliminate signal delay entirely.

Probing at this point (Pins 7 and 8) should reveal a square wave with rising edges following a $1 - \exp(-t/RC_{DET})$ type of curve. Similarly, the falling edge should show an $(\exp(-t/RC_{DET}))$ type of characteristic. Probing on the complementary pin will just show the inversion of the signal. This should be expected since just the charging and discharging of the detection capacitor are being observed.

AM Rejection C_{AM} (Pin 9)

The AM rejection circuit tracks the average DC value of the envelope by adding or subtracting a series voltage to the voltage on the C_{DET}. (It operates as a negative feedback voltage mechanism for changes on the AM detector load by the additional DC components on the line.) AM rejection is better than 40dB. $C_{AM} = 0.1\mu F$ typical for 40dB rejection for 120Hz AM. This value will suffice for most power line applications. For a different case, look at the Twisted-Pair Applications.

If the received signal remains at the zero state after a 1-to-0 (on-to-off) transition for more than 4 seconds, the RX_{OUT} pin will drift to the logic High level and stay there until the signal changes state again. This is known as the standby mode. This feature can be defeated by externally applying a $2.2V_{DC}$ signal (see HOMENET application). Any protocol should take this feature into account if it does not externally defeat the feature through the hardware.

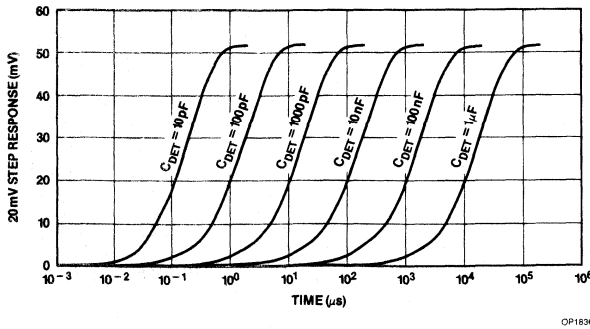


Figure 4. Comparative Delay of AM Detector for Different Values of C_{DET}

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Impulse Rejection C_{IMP} (Pin 10)
This capacitor allows the device to absorb the line transients that sometimes reach peak values of several thousand volts. It also reduces the effect of the glitches caused by different line loads. C_{IMP} is charged or discharged with constant current from the comparator which causes the voltage variation at Pin 10 to be of constant slope versus time. Narrow current impulses will not last long enough to fully charge or discharge C_{IMP} ($I_{CIMP} = C_{IMP} \times (\Delta V/\Delta T)$.) The baud rate depends on the size of C_{IMP}. Typically, rejected impulse width $\leq C_{IMP} \times 35k\Omega$ (sec) $\leq$ minimum data width.

The delay in recovering data that is introduced by this stage is

$$t_{DELAY} = C_{IMP} \times 35k\Omega.$$

If this point is probed, a square wave with a well-defined slope on the rising and falling edges should be seen. The slope is a function of the output current of the comparator and the capacitance on this pin (I_{CIMP} and C_{IMP}).

Logic Output R_{PULL} (Pin 11)
This is an open-collector output and needs a pull-up resistor to let it swing to a High value. The listed value of 10kΩ is fine. It can be decreased for a maximum $I_{OL} = 10mA$. Also shown in the diagram is an optional supply $V_{LOGIC} = +5V$ provided by the user to give TTL-level compatibility. Otherwise, the output should swing all the way to +12V and all the way down to ground.

The point can be probed while the signal is transmitted to see if the IC is receiving its own transmission. Carrier feedthrough may be seen on the output signal.

Transmitter

The transmitter input (TX_{IN}) is at Pin 19. A logic "1" enables the line driver and sends the carrier on the line. A logic "0" disables the carrier, which constitutes the on/off Amplitude Shift-Keying. When in the receive mode, this pin should be grounded. Make sure that the TX_{IN} levels are TTL compatible. Signals that are more than one V_{BE} (0.7V) below ground turn on a diode that disables the transmitter. External components to be set for the transmitter are as follows:

Carrier Frequency (R_{OSC}, C_{OSC}, L_{OSC}, C_{F0}, C_{F1})
The carrier frequency is set internally by a differential-pair Colpitts Oscillator. To set the frequency externally, apply the signal to LC (Pin 13). Pin 13 is the input for external operation and the load for use of the on-board oscillator.

If an external carrier is not desired, set the oscillator frequency by the 5 external components listed above. (Note: $C_{F1} = 0$ in this application. Increasing it merely raises the level of AC feedback to the oscillator. It would only be important in the wideband operation since it provides a reference for the other end of the differential pair.) The design equation for the ω_0 is (ω_0 should equal ω_{CXR}):

$$\omega_0 = \frac{1}{\sqrt{L_{OSC} \times C_{EQ}}}$$

$$(\omega_0 = 2\pi f_0)$$

where C_{EQ} is given by

$$C_{EQ} = C_{OSC} + \frac{C_{F0} \times C_{F1}}{C_{F0} + C_{F1}}$$

Since $C_{F0} >> C_{F1}$, then

$$C_{EQ} = C_{OSC} + C_{F0}$$

Carrier leakage in the off state is minimal and should have no effect on the receive input, RX_{IH} (Pin 20).

Output Stage (Q1, Q2, R_{E1}, R_{E2})
The line driver is a class AB push-pull output stage with optional external complementary transistor pair for increased current drive capability. The TX output impedance is 40kΩ in the off state (RX_{ON}, receive mode) and less than 2Ω in the on state (TX_{ON}, transmit mode).

By itself, the NE5050 is capable of driving a *consumer* line impedance of 50Ω *without* the drive transistors Q1 and Q2. To do this, set $R_{E1} = R_{E2} = 10\Omega$, placing R_{E1} between Pins 15 and 16, and R_{E2} between Pins 16 and 17; select $R_{DRIVE} = 50\Omega$. The voltage divider effect is evident.

With the external drive transistors, however, the PLM is capable of driving an *industrial* line impedance of 10Ω. Merely set $R_{E1} = R_{E2} = 1\Omega$ and set $R_{DRIVE} = 10\Omega$.

Feedback ($R_{FEEDBACK}$)
To increase the amplitude of the transmitter, add a feedback resistor in the driver amplifier feedback path at Pin 16. $R_{FEEDBACK} \approx 75k\Omega$ is fine for $V_{CC} = +15V$ operation. For $V_{CC} = +12V$, use a 22kΩ resistor. If you are not using external drive transistors and are using $V_{CC} = +12V$, then use a 56kΩ resistor.

Transmitter Drive (R_{DRIVE}, C_{DRIVE})
R_{DRIVE} and C_{DRIVE} provide impedance matching for the output of the driver for coupling back through the transformer. R_{DRIVE} provides the real component and C_{DRIVE} the complex. R_{DRIVE} should be set to 50Ω for consumer applications; with no external transistors needed (set R_{E1} and R_{E2} as above), or for industrial applications, use $R_{DRIVE} = 10\Omega$ with the drive transistors, setting R_{E1} and R_{E2} as indicated.

INDUSTRIAL APPLICATION

Electrical Hazards to the User

WARNING: ELECTRICAL SHOCK HAZARD! DO NOT PROCEED UNTIL YOU HAVE READ THIS SECTION !

In addition to being a supply of $110V_{AC}$, the power line is a near-infinite source of current and it only takes 100mA to kill a human being. (It takes about 80mA to fibrillate the heart and give a serious shock. Approach the board testing as though you were going to repair a television set.) So remember, 110V of AC line voltage is present on the line cord, the line coupling capacitor (C_{LINE}), and on the transformer primary. Please exercise extreme caution when using these boards. Even if the cord is not plugged into the AC power line, C_{LINE} can retain charge. After being unplugged, if touched before discharged, it can give a severe electric shock.

Certain measures have been made to protect the user from being exposed to the power line. A silicone resin has been applied to the line cord on the top of the board and a mylar plate has been attached via four nuts to the bottom of the board. Before changing components, please use the following procedure:

1. Unplug the cord from the AC line. Always use one hand when plugging or unplugging the cord. A good procedure to follow would be to set the board down first and then plug it in with the same hand, keeping the other in your pocket. Holding the board in one hand (exposed AC) and the plug in the other could turn *you* into the load if you are careless.
2. Discharge the coupling capacitor by holding the unplugged cord by the insulated portion of the plug and then short the plug prongs with an insulated screwdriver. Be sure to hold the screwdriver by its insulated handle. As you touch the screwdriver to the prongs, you should hear a slight 'pop' from the discharge. If you don't hear the pop, it could be an indication that the line capacitor is bad.

   NOTE:
   Transient protection must be incorporated between Pins 1 and 20 when following this procedure (i.e. Back-to-Back zeners or transient absorbers).
3. Remove the plastic nuts, screws, and the mylar plate.
4. After changing components and soldering, *replace* the nuts and mylar plate. *NEVER* operate the board or plug it into the AC line without the cover. It is very easy to leave a wire or a piece of solder on the bench and short the AC line when you set the board down. This is a possible fire hazard and will usually trip the

circuit breaker for your area, killing the power in the area. (This actually happened while testing application boards.)

Do not attempt to remove the silicone from the line cord on the top of the board. This isolates you from the line while probing the component side. Do not defeat this safety feature.

Do not operate on metallic or other types of conductive surfaces. Always operate with the mylar plate on the backplane of the board. Refer to #4 above for what can happen if you leave the board off.

Do not keep drinks or liquids in the area. A spilled drink can be disastrous.

NOTE:
Signetics provides these NE5050 Power Line Modem Application Boards for design and development purposes only. Signetics assumes no liability and makes no guarantees regarding the performance of these boards. By acceptance of these demo boards, the user agrees to follow the instructions described in this manual and releases Signetics from any liability and claims resulting from use of these boards including but not limited to third party claims.

OBSERVING THE NE5050 DEMONSTRATION BOARD PERFORMANCE

Operation of the NE5050 Demonstration Board

Figure 5 is the schematic for the NE5050 demonstration board. The demo board is designed to operate at a carrier frequency of 118kHz. From left to right on the schematic, the board is coupled to the power line via a 1-1 ratio Toko brand transformer. Two high voltage 47μF capacitors provide blocking of the 50/60Hz high voltage from the power line (and pass the high-frequency carrier). The presence of a times-4 wound secondary coil is used in series with C_{TUNE} to set up a secondary which is resonant with the carrier frequency. This resonance should be tuned via the transformer core to provide minimum attenuation of the carrier frequency.

The signal (and whatever line noise is present) is then presented differentially to the input amplifier (Pins 1 and 20). Two 15V, 1W zener diodes are connected between these pins to protect the IC from high voltage spikes (note that this can happen, for example, when discharging the line capacitors by shorting the plug). The input amplifier is also configured as a high-pass filter whose characteristics are determined by the value of the capacitor on Pin 2 (C_{LPF}). See Figure 3 for bode plots. The input amplifier/filter will provide about a 20dB boost of the carrier frequency. The signal is then output to Pins 3 and 6 to an externally-connected band-pass filter. On the demonstration board this is a single-pole RCL filter tuned to approximately 118kHz.

Pins 4 and 5 form the input to the amplitude detector which performs signal decoding via amplitude detection and amplitude modulation cancellation. This detector will trigger at the presence of a signal at a level of 20 – 30mV_{RMS}. The amplitude modulation cancellation stage allows for continuous amplitude modulation of the carrier frequency without loss of data (as long as the amplitude fluctuations are above the detector threshold).

The final stage is the impulse filter which rejects short-duration impulses of a duration determined by the value of the impulse capacitor (C_{IMP}) connected at Pin 10. Pin 11 is the open-collector output which provides a TTL-level demodulated output. This output is connected to a 10k resistor pull-up which is tied to the output post labeled "V_{LOGIC}". The TTL level signal appears at the post labeled "REC". An NPN transistor forms an open-collector inverted output at the post labeled "REC OC."

The transmitter section consists of an oscillator whose frequency is determined by the externally connected LC tank at Pins 13 and 14. These are of the same value as the LC tank used for the band-pass filter at Pins 4 and 5. This oscillator is internally connected to a line-drive amplifier which drives an external class AB amplifier consisting of a power NPN and PNP transistor. The line drive amplifier is turned off and on by the presence of a logic "0" or logic "1" level appearing at the transmit input, Pin 19. This results in the ASK encoding; digital information is transmitted via the presence or absence of the carrier frequency. $R_{FEEDBACK}$ is used to improve harmonic distortion; R_{DRIVE} is matched to the anticipated average load. The high-frequency carrier is transmitted to the transformer for induction to the power line.

Some additional features of the demonstration board are:

JMPR-Standby Defeat

This jumper, when connected, inhibits the NE5050 from going into "standby mode". As a power-saving feature, the NE5050's output transistor (driving Pin 11) will deactivate after approximately 4 seconds of no-data traffic (go into "standby"). This will result in a logic "1" level at the open-collector output, Pin 11. By closing this jumper, this feature will be defeated by introducing a DC voltage at Pin 9.

JMPR-RCV Suppress (Receiver Suppress)

This jumper, when connected, will force Pin 11 to a Low state during transmission of a logic "1" level. This feature is provided to prevent "echoes" of transmitted messages from feeding back to the receiver. This can occur because of the time delay of transmitted signals traveling back through the receiver filters (primarily the impulse filter). In multiple transceiver networks, this echo may be undesirable because it can simulate the presence of another transmitter on the line during the short duration between the end of a transmission and the presence of the "echo". Because collision (and hence arbitration) can only occur during the transmission of a logic "0" (absence of carrier) condition, suppressing the receiver will not eliminate any useful information regarding the line status. Note that closing this jumper will result in a low state at the output (Pin 11) during transmissions of a logic "1".

Inputs/Outputs

Inputs to the NE5050 demonstration board consist of a V_{LOGIC} input, and a XMIT input. The V_{LOGIC} input is simply the voltage level that will appear at the output pin (marked REC) during a logic "1" condition. For most TTL interfaces, this will be + 5V. This is to be externally applied. A DC power supply of + 12 to + 18V is required to power the board.

The XMIT input is a TTL-level input which either activates or deactivates the line-drive amplifier which drives the power line (or selected medium) with a carrier. A logic "1" will activate the transmitter, resulting in a presence-of-carrier condition. A logic "0" will deactivate the transmitter resulting in an absence-of-carrier. Be sure that the levels are TTL and have a common ground with the demo board.

Outputs of the demo board consist of a REC OC (Receive, Open-Collector), a REC (Receive), and an LED visual output. The REC OC is an inverted, open-collector output, appropriate for interfaces requiring an inverted logic, open-collector output (such as GE's HOMENET). REC is a positive logic output which will provide output voltage levels according to the V_{LOGIC} voltage level which is externally applied. The LED provides an inverted-logic visual indicator, activated during the presence of a "0" at the output, and turned off during the presence of a "1".

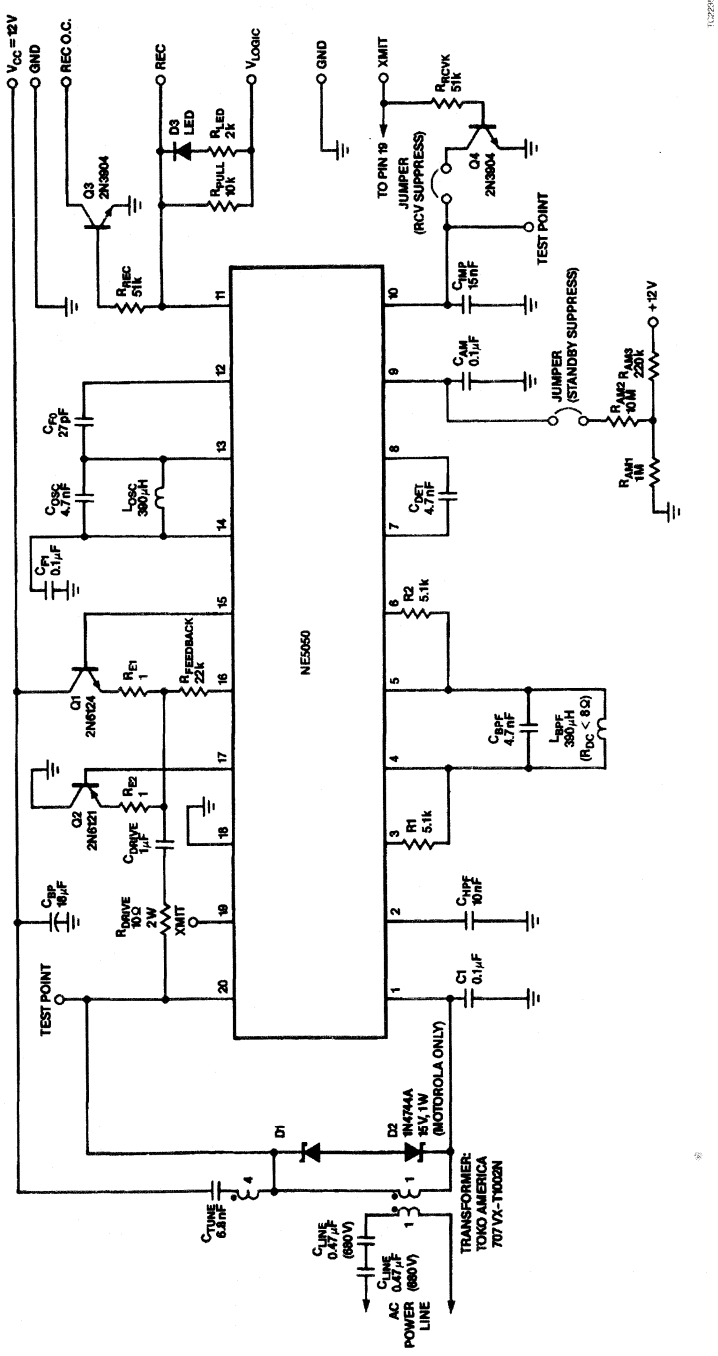


Figure 5. NE5050 Demonstration Board Schematic

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Transient Protection

The latest revision of the NE5050 demo board incorporates two back-to-back zener diodes (Motorola 1N4744A) which provide 15V overvoltage protection for the NE5050. The NE5050 has been designed to endure ± 35V transients, but for additional protection during worst-case conditions (such as the sudden discharge of the line capacitor by shorting the prongs of the plug), these devices have been added. The diodes are connected between Pins 1 and 20 of the IC. Other devices may be used instead (such as surge protectors), as long as they are fast enough to prevent fast-rising high voltage impulses from reaching plus or minus 35V.

120/240V_{AC} Compatibility

This incorporates two series line capacitors, each rated for 680V. This makes the new demo boards compatible with both 120 and 240V_{AC} power line.

BENCH TUNING AND TESTING

Testing and tuning of the NE5050 demonstration boards can be accomplished safely without plugging the boards into the power line. This test procedure is, therefore, done in the absence of the line voltage. Note that the boards are configured to a receiver threshold of 20mV peak-to-peak, with an impulse rejection time of approximately 570μs. The carrier frequency has been set to 118kHz (± 10% due to component variations).

Receiver Testing:

1. Make sure to ground the XMIT input to deactivate the local oscillator.
2. Apply V_{CC} = 12V at the input pin marked "V_{CC}", and 0V at "GND".
3. Measure V_{CC} = 12V at Pins 1 and 20.
4. Make sure the voltage at Pin 3 equals the voltage at Pin 6.
5. With an external frequency source (either another NE5050 demonstration board or a generator), create a 100kHz carrier frequency modulated with a 500Hz envelope (see Figure 6a).
6. Apply this ASK signal to the plug-input of the demonstration board.
7. View this signal with an oscilloscope at Pin 3 or 6. It should appear as illustrated in Figure 6b.
8. Next, view the signal after the band-pass filter, at Pin 4 or 5. It will appear as is shown in Figure 6c.
9. While viewing the ASK signal at Pin 4, adjust the frequency of the source until a maximum amplitude is observed. This should occur at near 118kHz. (See Figure 6d.)
10. Further maximize the carrier amplitude by tuning the core of the Toko transformer with a small screwdriver. (See Figure 6e.)
11. Next, probe Pins 7 and 8, the detector output. It will look like Figure 6f.
12. Next, look at how the impulse filter affects the output signal. This is done by probing Pin 10. You will see a trapezoidal trace with ramps of duration of about 570μs. This rise time is determined by C_{IMP} at Pin 10.
13. The Pin 10 signals are photographed in Figure 6g.
14. Apply at V_{LOGIC} a 5V_{DC} supply. View the recovered TTL level square wave at the output marked REC (Figure 6h). Note that any pulse of less than about 570μs will be removed by the impulse filter.

Transmitter Testing:

- Power the board and test as covered above (see Figure 6i)
- Connect a 10Ω, 2W resistor to simulate a load across the plug
- Apply a 500Hz TTL-level square-wave to the pin marked "XMIT"
- The corresponding ASK signal will appear across the 10Ω load at the plug
- Disconnect the resistor and the amplitude should double
- Tune the transformer core to obtain maximum signal amplitude at the plug output

Experiment with the NE5050 board before plugging it into the power line. Here are some additional procedures for observing each section.

Receiver— Turn the transmitter, TX, off by grounding TX_{IN} (Pin 19.) If this is not done, the signal coming is the local oscillator. Remove the line coupling transformer and the bandpass filter to permit broadband operation (the filtering action of the transformer with C_{TUNE} is no longer needed). Replace the line coupling transformer secondary with a 50Ω resistor. Connect Pin 20 of the IC to the line coupling capacitor, C_{TUNE}. Inject ASK input signals at the cord prongs from a 50Ω generator. Connect the signal side to one prong and the ground side to the other. Now run the following checks:

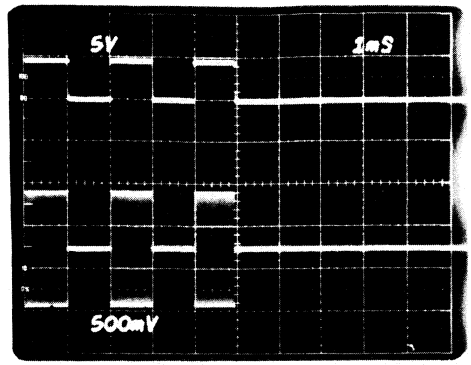
- Sweep the carrier frequency
- Change the carrier amplitude (sensitivity specified to 1.5mV_{RMS} typical, guaranteed minimum 3.5mV_{RMS} over 0 to + 70°C, the consumer temperature range).
- Change the data rate; observe the theoretical maximum: Data rate ratio to carrier frequency (1 Bit/cycle). Note that the data rate is limited directly by the value of the impulse capacitor C_{IMP}.
- Sweep V_{CC} from 12 to 18V
- Remove and replace C_{DET} (AM detector cap) and C_{IMP} (impulse filter cap) and observe RX_{OUT} (Pin 11)
- Decrease C_{LPF} (changing the input high-pass filter characteristics) to 1nF for maximum sensitivity at f_C = 300kHz
- Sweep the carrier frequency from 100Hz to 500kHz
- Increase C_{LPF} to 0.1μF; use low carrier frequencies and low data rates
- Sweep the carrier down to DC
- Decrease the ASK data rate
- Observe the general limitations of the IC modem with the given external components

TRANSMITTER— Replace the 50Ω resistor, R_{DRIVE}, with a 10Ω, ½W resistor. Monitor prongs of cord on the oscilloscope. Similar tests to those done in the receiver can now be done:

- Inject TTL and CMOS data at TX_{IN} (Pin 19)
- Sweep V_{CC}
- Observe the TX output (4V_{P-P} into a 10Ω load, R_L, connected between R_{DRIVE} and ground)
- Open TX_{IN} and observe the THD (total harmonic distortion) of the unmodulated carrier
- Ground TX_{IN} and observe the −90dB carrier suppression at TX_{OUT} and at the prongs
- Check the RX_{OUT} Pin to make sure that it is always receiving what it is sending

Should you have any recommendations or questions in the course of your development, please call Mike Sedayao at (408) 991-4637 or Dan Hariton at (408) 991-4730. We would be glad to assist you.

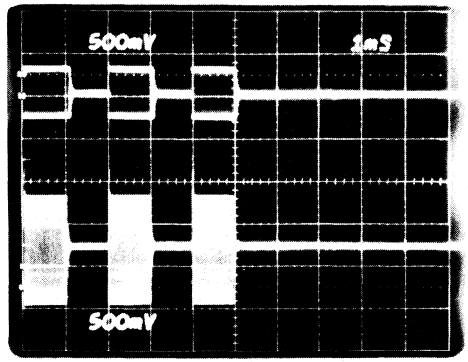
The NE5050 demonstration board kits are available from your local Signetics distributor (order # NE5050 EVN MSC). These kits are for typical power line performance. Each kit contains 2 samples, 2 demonstration boards with samples, and this application note. Each kit has an estimated cost of $266.00.



EXTERNAL 500Hz

EXTERNAL ASK INTO PCB PLUG (RX INPUT) f_{CXR} = 100kHz

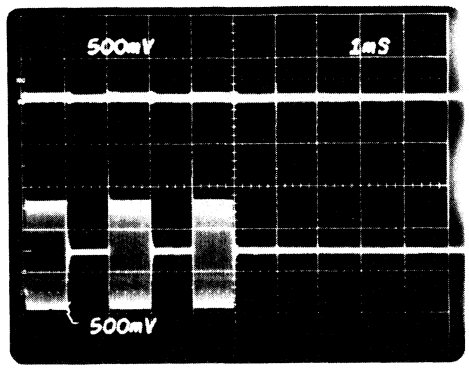
a.



PIN 3 OR PIN 6 (RX AMPLIFIER OUTPUT)

EXTERNAL ASK AT THE PCB PLUG (RX_{IN}) f_{CXR} = 100kHz

b.

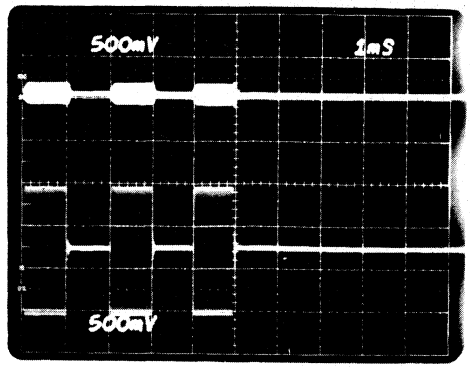


PIN 4 OR PIN 5 (DETECTOR INPUT)

EXTERNAL ASK AT THE PCB PLUG (RX_{IN}) f_{CXR} = 100kHz

c.

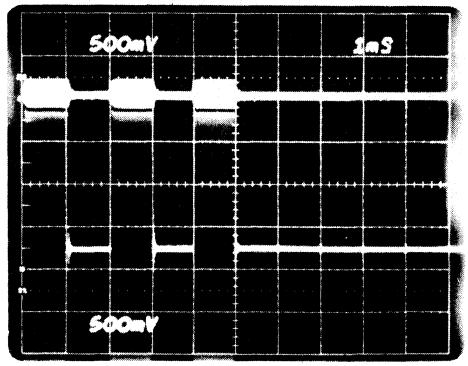
Figure 6. Oscilloscope Plots of NE5050 PCB Bench Testing



PIN 4
(DETECTOR IN)

RX_{IN}
f_{CXR} = 125kHz

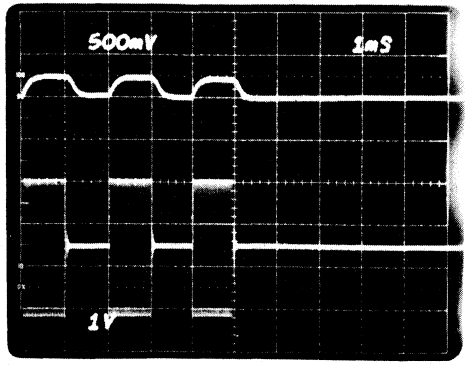
d.



PIN 4
(DETECTOR IN)

RX_{IN}
f_{CXR} = 125kHz
(TRANSFORMER TUNED)

e.

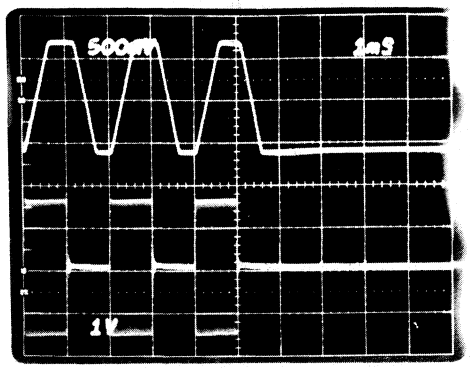


PIN 7 OR PIN 8
(DETECTOR OUTPUT)

RX_{IN}

f.

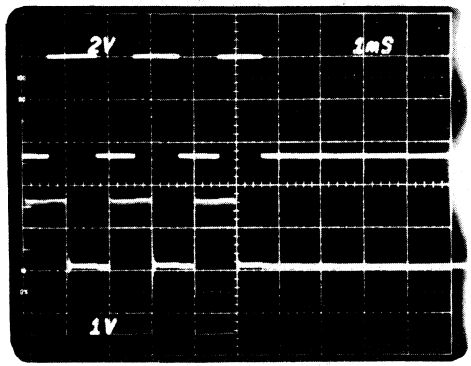
Figure 6. Oscilloscope Plots of NE5050 PCB Bench Testing (Continued)



PIN 10
(IMPULSE FILTER)
DELAY ~ 500μs

RX_{IN}

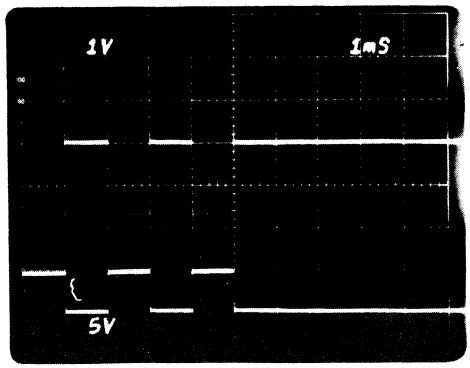
g.



RX_{OUT} "REC"
(PIN 11)

RX_{IN}

h.



PCB PLUG
(ACROSS 10Ω LOAD)

'XMIT' (PIN 19)
(TX_{IN})

i.

Figure 6. Oscilloscope Plots of NE5050 PCB Bench Testing (Continued)

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GUIDE FOR NE5050 CAPACITOR SELECTION

The NE5050 is connected to several external capacitors which must be optimized for different noise environments. Here is how to select the approximate values:

- **C_{LPF}: For rejection of low frequencies**

The input amplifier also provides a fixed high-pass function. The low −3dB point of this filter is given by the equation:

$$10^{-3}/C_{LPF}\ [F] = f_{-3dB}\ [Hz].$$

This provides a + 20dB/decade response, with a DC attenuation of −50dB. A carrier around 100kHz is boosted by + 24dB. See Figure 2.

- **C_{AM}: AM Rejection Capacitor**

This capacitor must be adjusted as a function of the bit rate (or more precisely, minimum-bit time). Its value should be:

$$C_{AM}\ [F] = 10^{-4}/\text{bit rate}\ [bits/sec].$$

This is to assure proper capture of leading bits in a bit string or in the preamble. It is a measure of the "readiness" of the receiver to switch from the "standby" mode to the "receive data mode" with no loss of leading bits. A low C_{AM} value will make the modem react faster (shorter delays) in both transition directions: from "standby" to "receive data" (incoming or departing messages) and from "receive data" to "standby" (absence of data traffic).

- **C_{DET}: AM Detector Capacitor**

Its value is given by:

$$C_{DET}\ [F] = t_{DET}\ [sec]/10^5;\ \text{see Figure 4.}$$

t_{DET} is the time it takes for C_{DET} to charge from 0 to 50mV, where 50mV is the detection threshold. The detector delay time, t_{DET}, affects the receiver's jitter. This delay is a term in a sum of delays, the sum being the total receiver delay, t_D [sec]. See below in "Receiver Delays" the relation between t_D and the maximum bit rate.

- **C_{IMP}: Impulse Filter Capacitor**

This capacitor determines the receiver impulse-noise immunity (transmission channel with non-Gaussian noise). This capacitor is determined by the equation:

$$C_{IMP}\ [F] = t_{IMP}\ [sec]/35k\Omega\ [ohm].$$

t_{IMP} is the time it takes to ramp up or down the C_{IMP} voltage (the beginning of the ramp is delayed by t_{DET}). The shortest bit should last longer than the widest impulse. The following equation determines t_{IMP}:

Maximum rejected or expected impulse-noise width [sec] < t_{IMP} [sec].

This delay is a term in a sum of delays, the sum being the total receiver delay, t_D [sec]. See 'Receiver Delays' the relation between t_D and the maximum bit rate.

- **Receiver Delays: Maximum bit rate**

The total receiver delay is a sum of delays, where t_{DET} [sec] is the detector delay, t_{IMP} [sec] is the impulse-filter delay, and 2μs is the receiver delay with no C_{DET} and no C_{IMP}:

t_D [sec] = total receiver delay = t_{DET} [sec] + t_{IMP} [sec] + 2μs.

The maximum bit rate, in the no-return-to-zero, amplitude-shift keying data format is determined by:

Maximum bit rate NRZ ASK [bit/sec] < $1/t_D$ [sec^{-1}]

NOTE:
The C_{DET} and C_{IMP} values so calculated are for guidance and the user shall determine the optimal performance values in a range between 0.1 times to 10 times the calculated values (power line environment assumed). For twisted-pair or coaxial cables the calculated values are close to optimal. Based on power line applications made at 100Bit/sec and at 50kBit/sec. the C_{IMP}/C_{DET} capacitor ratio ranged from 100:1 to 1:1.

Observing AC Line Transmission

To observe full data transmission, reconnect the line-coupling transformer, bandpass filter, and the initial values for capacitors C_{IPF}, C_{IMP}, and C_{AM}.

Take two boards, setting one up as the transmitter and the other as the receiver. Supply + 12V to + 15V and ground to each of them. On the receiver, short the TX_{IN} to ground. Attach a pulse generator to the TX_{IN} of the transmitter, remembering to connect the ground of the generator to the ground of the board. Review safety precautions before plugging into AC line.

Receiver sensitivity is $1mV_{RMS}$. It's recommended to start with about $4V_{P-P}$ to ensure a strong square wave for transmission. To center the bandpass of the transformer to the incoming carrier frequency, adjust the transformer coupling with a jewel head screwdriver.

To monitor the receiver, connect oscilloscope probes to the following circuit points:

- RX_{IN} (Pin 20, AC line signal with noise)
- OUT1 and OUT2 differentially (Pins 3 and 6, RX amplifier output)
- C_{DET1} and C_{DET2} differentially (Pins 7 and 8, AM detector output; the device can also be operated with this capacitor removed. Observe reduction in delay.)
- C_{AMREJ} (Pin 9, AM rejection)
- C_{IMPREJ} (Pin 10, impulse filter; as with the detector capacitor, the device can be operated without this part. There will also be a reduction in the delay.)
- RX_{OUT} (Pin 11, receive data output)

Loud, high power-consuming electrical equipment could be set up nearby to produce in-band disturbances, such as impulses. Also, switch fluorescent lights on and off to see the effect of the transients on the data transmission. To transmit the data, inject TTL signals (CMOS signals are fine because they typically swing from positive to negative rails. TTL thresholds are typically 0.8V for logic 0 and 2.0V for logic 1) into the TX_{IN} (Pin 19) of the other modem located nearby. Make sure that the signals do not go below ground; if they go more than one diode drop below ground, an internal diode turns on and redirects any signal from TX_{IN} into the substrate of the device. So if just injecting a pulse train is desired, choose a pulse generator that has TTL output rather than the symmetrical output that swings both positive and negative. After observing these signals, gradually separate the distance between the TX modem and the RX modem, trying different electrical outlets on the same floor, different floors, and different buildings.

Potential Sources of Interference

There are several sources of signal interference to consider. Among the most important and most likely to occur are the following:

Impulse noise — This form of interference is caused by electrical impulses present on the line. It is present in the baseband and in the frequency interval ($\omega_{CARRIER} \pm 2 \times \omega_{DATA}$) used for data communications. Because the frequency spectrum of a delta (Dirac) impulse is continuous, it would be present in any band. (A delta Dirac impulse is defined to be of infinite amplitude and zero time duration. Thus, its Fourier transform would give it an infinite bandwidth with value unity.)

This translates into a carrier of short duration in the receiver. If data carrier bursts are longer than the impulse bursts, it is possible to filter out narrow data by low-pass filtering (integrating) or by the constant charging and discharging of a capacitor (time domain filtering). Observe the waveform at Pin 10 to see this.

Distributor transformer attenuation — The transformers that separate domestic dwellings or different floors in a factory offer safety features for the people in the buildings, but can also attenuate signals trying to pass through. The maximum attenuation between any two locations within the same house is around 50dB in the 10 − 550kHz range. House-to-house attenuation could be from 10dB for the same distribution transformer to 30dB for separate transformers.

In residential areas, the power line network should not extend beyond the building. High-frequency blocking may be necessary to implement this separation. Consult the EIA (Electrical Industries Association) for up-to-

date information on how to implement the blocking. The consensus is that the blocking should be done at the electric power meter.

CW (Continuous Wave) interference — This type of interference is usually caused by tones present on the AC line. They can be generated by mercury-vapor fluorescent lamps. If in the frequency band of the receiver, they may affect the received data and can cause bit errors. The CW interference has spectral components at multiples of 60kHz. It is amplitude-modulated by a 120Hz envelope.

Line impedance modulation — The impedance of the AC power line varies according to the number and power consumption requirements of the various equipment connected to the line. 120Hz impedance modulation also occurs as a result of rectification at 60Hz. Different conditions exist, of course, for the residential and the industrial environments.

The effect of the impedance modulation is best illustrated by observing the waveforms on Pins 7 and 8 (AM detection) and on Pin 9 (AM rejection). The data signal varies in amplitude because of the varying impedance on the line. The AM rejection circuit forces the comparator to track the DC average of the demodulated data and keeps the comparator from changing states. This can be envisioned as a 50mV "window" (comparator threshold) "surfing" on the input waveform.

A good example of the kinds of noise on the power line and how the NE5050 eliminates them is shown in Figure 5.

The top trace shows the signal at Pin 20, RX_{IN}. The signal has already come from the line, and gone through the line capacitor and coupling transformer. If the trace is followed from left to right, three squares over show the effects of Continuous Wave interference. These signals start to produce an amplitude variation where the signal should clearly be cut off. It also starts to distort the logic 1-to-0 and 0-to-1 transitions. At about the seventh block, the effects of impedance modulation on the signal can be seen. What should clearly be a square-shaped signal is now distorted into jagged edges of increasing magnitude.

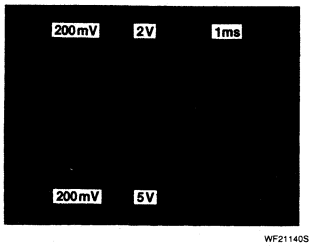


Figure 7. Oscilloscope Traces of RX_{IN}, Output of Bandpass Filter, Impulse Rejection, and RX_{OUT}

The second trace is the output of the single-pole bandpass filter and the input of the AM detector (Pins 4 and 5). After RX_{IN}, the signal was amplified and then filtered before coming out of Pins 3 and 6 and going into the bandpass filter. At the end of the signal there is some ringing, and in the third block the effects of the impedance modulation still show slight amplitude variations.

Trace three shows the output of the slicing comparator at the impulse rejection range. The slope of the signal is directly related to C_{IMP}. At this point the signal has now gone through the AM detector and the AM rejector. AM rejection was successful since the impedance modulation effects do not show up on the third block.

The bottom trace shows the output, RX_{OUT}, at Pin 11. Resistor R_{PULL} connects Pin 11 to the logic High voltage. This signal is a square wave, just the output of the flip-flop that was fed internally by the comparator. Comparing the top and bottom traces, a delay is evident. This is caused by the charging of the AM detection and the impulse rejection capacitors.

Troubleshooting Board Problems

Because all components, discrete or integrated, are not exactly the same, always expect to see a difference in performance as different components are used. Not every application board is the same in the sense that the frequency, filter Q, transmitted power, etc., vary ± 10%; otherwise, they are all fully functional. To help solve eventual problems, a list of cures has been accumulated for different situations. Short of doing a pin-for-pin, part-for-part test, these are some of the things that can be done to get the system running prior to identifying the specific problem.

Assuming that the setup is configured in the send/receive mode and connected to the power line, there are three possible solutions to use to get the signal through.

Increase power supply — Bringing the power supply of the part to about +15V may reduce the total harmonic distortion (THD) of the transmitter if the driver swings more than $8V_{P-P}$. For higher voltage swing, increase $R_{FEEDBACK}$ for lower negative feedback. This also increases the swing of the voltage output of the transmitter. Sending out a larger signal over the power lines increases the signal-to-noise ratio.

[To operate the board at supply voltages in excess of +15V (but not beyond +18V), connect an 82kΩ resistor between Pin 1 (V_{CC}) and Pin 15 (feedback) to create a DC bias at this point so that the upper drive transistor will not break down. This is a process limitation.]

Reducing or shorting output resistor R_{DRIVE} — This 10Ω resistor drops the transmit voltage by a little. Reducing or bypassing this resistor increases the voltage sent over the AC lines. The overall effect is similar to solution #1.

Bypassing the bandpass filter — Although this is usually done only in wideband applications, it is possible that the loss of signal occurs because the signal is being filtered out. That may occur because of BPF or oscillator component skew. The carrier may be filtered out instead of the noise. In removing the BPF, more noise is introduced because of the wider frequency band, but, once the signal is identified, the BPF can be reconfigured to pass the carrier frequency in the center of its bandwidth.

NE5050 DEMONSTRATION BOARD ADJUSTMENTS

Summary

The demonstration board comes configured in a particular mode of operation (i.e., carrier frequency, filter parameters, impulse filtering, etc.) but is easily modifiable. BE SURE TO DISCONNECT THE BOARD FROM THE POWER LINE AND DISCHARGE THE LINE CAPACITORS BEFORE REMOVING THE BACKING OR CHANGING COMPONENTS. Here are some basic adjustments that can be made:

1. Carrier Frequency
   Both transmitter and receiver are tuned to approximately 118kHz. This may be altered by changing C_{BPF}, L_{BPF}, C_{OSC}, and L_{OSC}. Center frequency is determined by the equation $f(Hertz) = 1/[2*pi*\{(LC)^{1/2}\}]$.

2. Impulse Filter
   The impulse filter consists of a capacitor tied to Pin 10. This capacitor results in a rejection of impulses (short-duration, high-bandwidth noise) that can appear after the bandpass filter. This filter will ignore short pulses of duration determined by the equation Impulse Rejection Time (in seconds) = 38k $*C_{IMP}$. The demonstration board comes with a 15nF impulse capacitor, resulting in an impulse rejection time of 570μs. This means that any pulse or state-change that is shorter than 570μs will be ignored by the IC. This impulse rejection time may be changed by altering this capacitor value. Note that the value of this capacitor subsequently places a ceiling on the maximum baud rate by placing a minimum allowable time for symbol encoding.

3. Input High-Pass Filter
   The input stage of the NE5050 consists of a gain/high-pass filter stage. The transfer function of this filter can be modified by changing the value of the capacitor at Pin 2. See Figure 3 for this filter's characteristics.
4. Receiver Bandpass Filter
   The receiver bandpass filter consists of a differential single-pole LC stage connected to Pins 3, 4, 5, and 6. The center frequency is given in Part 1 above. The sharpness of this filter is determined by the value of the R1 and R2. By increasing the value of these resistors, we may increase the filter Q (which also increases insertion loss). Figure 8 shows some typical performance curves of this filter with different values of resistors.
5. The demonstration board is designed to deliver maximum power into a 10Ω load. This may be changed by simply matching the value of R_{DRIVE} to the equivalent impedance of the transmission medium. Be sure to use at least a 2W resistor.
6. Transformer Tuning
   The Toko transformer provided has an adjustable core which should be tuned to provide minimum carrier attenuation at the desired carrier frequency. This can be accomplished by observing the envelope of a continuous carrier (generated by another transmitter and applied through the power line side of the transformer) and turning the core to a point of maximum carrier amplitude.

The value for C_{TUNE}, 6.8nF, was found to be the best tuning possible for the secondary of the TOKO transformer. One could also try to tune the primary of the transformer.

The TOKO transformer is not recommended in networks with a large number of nodes, and is not recommended for high bit rates, for two reasons:

a) In the receive mode the NE5050 IC input impedance is 9kΩ at the carrier frequency (Pin 20). The TOKO transformer lowers the receive-mode input impedance of the printed circuit board to 200Ω. This is OK for few nodes. This TOKO transformer design does not facilitate the use of many nodes in a single network. A possible substitute transformer is the AIE Magnetics transformer which has 2kΩ at the carrier frequency.

b) The TOKO transformer has limited capability for high-speed data transmission rates (to 10kbit/sec) while the AIE transformer enables data rates in excess of 100kbit/sec. The AIE transformer is broadband and does not require tuning.

7. Transient Protection

Note that no guaranties are given regarding the breakdown voltage of either transformer. For transient protection, the user is directed to the following standard:

IEEE Standard 587 (ANSI C62.41 – 1981)
Condition:
Long Branch Circuits — 0.5μs – 100kHz oscillatory wave 6kV.
Short Branch Circuits — 1.2 × 50μs impulse wave 6kV.

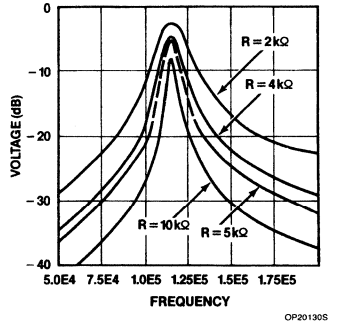


Figure 8. Typical Response for One-Pole BPF and Different Resistor Values

LAYOUT OF BOARD

Shown in Figure 9 is a copy of the layout. Imagine looking from the top and actually seeing "through" the board to the metallization layer (solder side). Look on the back and the pattern will be reversed. This has been done so that the engineer may look at the components on top (component side) and see how they are interconnected on the back side (solder side).

List of External Components

These component values reflect the NE5050 demonstration board which has been designed for 118kHz operation into a line impedance of 10Ω.

Component	Value
Capacitors	
C_{LINE}	0.47μF/680V (2)
C_{TUNE}	6.8nF
C_{PS}	10uF
C_{DRIVE}	1μF
C_1	0.1μF
C_{LPF}	10nF
C_{BPF}	4.7nF
C_{OSC}	4.7nF
C_{DET}	4.7nF
C_{F0}	27pF
C_{F1}	.1μF
C_{AM}	.1μF
C_{IMP}	15nF
Resistors	
R_{DRIVE}	10Ω/2W
R_1	5.1kΩ
R_2	5.1kΩ
R_{E2}	1Ω
R_{E1}	1Ω
$R_{FEEDBACK}$	22kΩ
R_{AM1}	1MΩ
R_{AM2}	20MΩ
R_{AM3}	220kΩ
R_{OC}	51kΩ
R_{PULL}	10kΩ
R_{LED}	2kΩ
R_{RCVS}	51kΩ
Inductors	
L_{OSC}	390μH
L_{BPF}	390μH
Transistors	
Q1	2N6124 (NPN)
Q2	2N6121 (PNP)
Q3	2N3904
Q4	2N3904
Miscellaneous	
Transformer: Toko America* #707VX – T1002N Diodes: Motorola 1N4744A 1 LED	

*Toko America, Inc.
5520 West Touhy Avenue
Skokie, IL 60077
(312) 677-3640
In California (408) 996-7575

AIE Magnetics
A Division of Vernitron Corporation
701 Murfreesboro Road
Nashville, TN 37210
(615) 244-9024

Advance Transformer Company
2950 Northwestern Avenue
Chicago, IL 60618
(312) 267-8100

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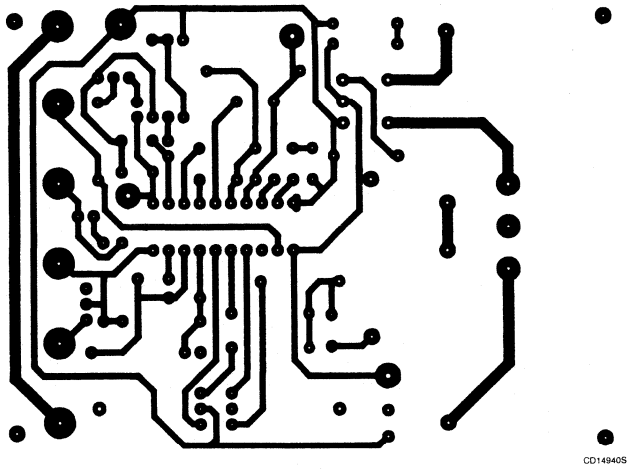
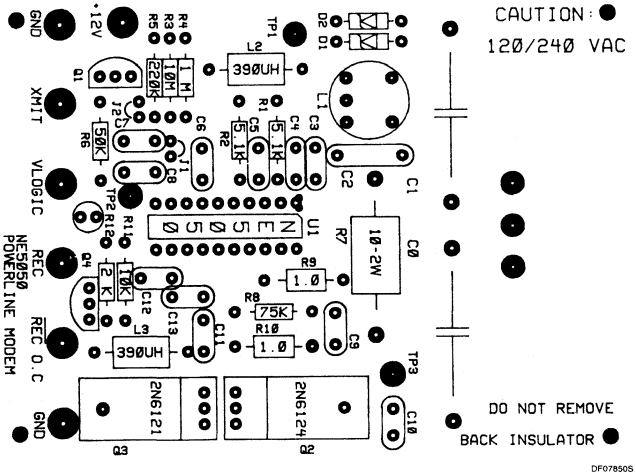


Figure 9. Layout of Application Board



*J1: JMPR – Standby suppress
J2: JMPR – Receive suppress

Figure 10. Component Reference on Layout of Board (Top View)

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HIGH-PERFORMANCE INDUSTRIAL APPLICATION

In a hostile environment, the carrier frequency and filtering scheme must be judiciously chosen. This is usually done over the frequency domain and after a thorough characterization of the environment it is designed for. The carrier frequency is then chosen to be in the range of least interference. To ensure the suppression of out-of-band signals, whether it is noise or other carrier frequencies (for a multicarrier system, see the Multicarrier Operation section), a high Q filter with large stopband suppression is desirable. This suggests the use of multipole passive filters or active filters. The problem in using multipole passive filters is that the passive elements tend to overattenuate the signal.

The configuration shown in Figure 7 illustrates one alternative to the single-pole filter given in the normal 100kHz industrial operation. The problem presented was that certain fluorescent light bulbs added significant interference to line transmission and caused bit-error-rate problems. The light bulbs produce spectral components at 60 and 120kHz that contribute to impedance modulation effects in that range. With a carrier near 100kHz, the single-pole passive bandpass filter with its 6dB/octave roll-off did not provide sufficient stopband suppression to get around the spikes at 120kHz. The solution was to move the carrier to a higher frequency (260kHz) beyond the effect of the lights and to select a filter with a much higher Q in order to eliminate as much noise as possible in the spectrum near the carrier.

The outputs of the input amplifier are Pins 3 and 6 which feed into the high-Q ceramic filters. The ones used are Toko 262Cs with a center frequency of 262kHz. These filters have a BW of greater than 8kHz and an insertion loss of 6dB. Given the center frequency and BW, the Q is approximately 32. The outputs of the ceramic filters then feed into the two-pole LC filter on the right part of the diagram. C1, L1, C4, and L2 provide the center frequency.

Resistors R1, R2, R3A, R4A, R5A, R6A, R3, and R4 provide DC biasing to the middle of the supply range, 6V. Resistors R3 and R4 buffer the NE592 Differential Amplifier, and C2 and C3 AC-couple the signal to the second LC tank which is buffered by R7 and R8. The NE592 is used to amplify the signal which has been attenuated by the ceramic filter and the input resistors. The NE592 has an adjustable gain, in this case, the gain (differential) has been set to 200. (This is the middle of the gain range and should be adjusted to give the desired signal.) The output is then sent to the input of the AM detector, Pins 4 and 5.

There are additional changes to be made for the high-performance application. C_{OSC} and L_{OSC} have been changed to 1nF and 390μH to match the change made in the bandpass filter. C_{TUNE} has been changed to 1nF for the same reason. C_{IMP} has been raised to 12nF to provide a suppression of impulses with duration under 450μs.

The filter shown in this example should by no means be taken as the best possible example. It was only tailored for the application and environmental conditions in Signetics' laboratory. Any conventional filter with a differential input and output can be used. In most cases, the cost of external components to the user and the amount of available space on the board will be the limiting factors.

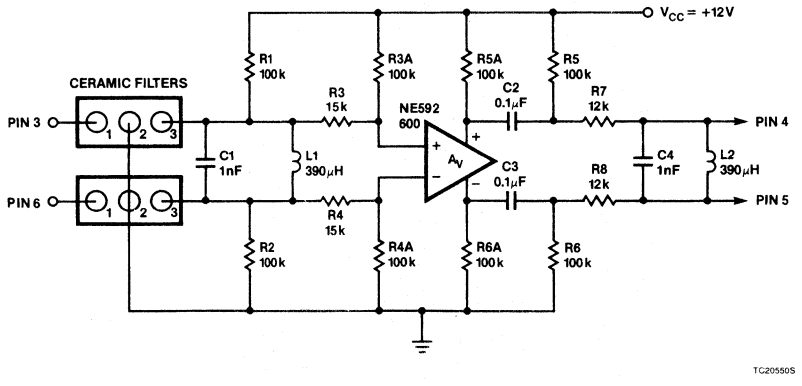


Figure 11. Ceramic Filter with Two-Pole Filter for High-Performance Industrial Operation (F_C = 260kHz)

OTHER APPLICATIONS

On the following pages are several applications for the NE5050 that demonstrate its flexibility. As mentioned in the disclaimer, these do not denote the maximum performance of the part, they just describe potential applications.

CONSUMER OPERATION

The consumer application is similar to the industrial operation outlined earlier, except that it uses a drive resistor of 50Ω instead of 10Ω. Use the same safety precautions, outlined under Electrical Hazards to the User.

A major difference between this application and that of the industrial environment is the lack of external drive transistors for the transmitter.

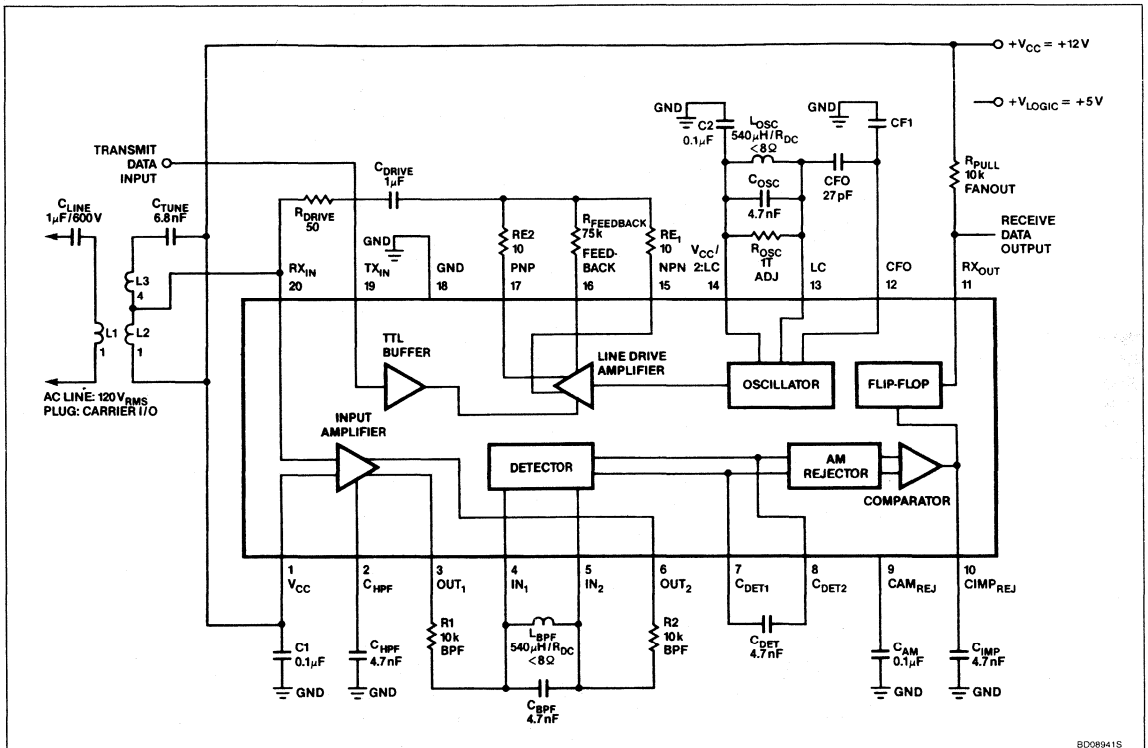


Figure 12. 100kHz Consumer Operation

SPLIT-SECONDARY OPERATION

This operation is similar to the industrial operation except that the transmitted signal is sent on a separate secondary winding. Note that the turns ratios are 10:40 for the received signal. The turns ratio for the transmitted signal back to the line is 1:10. For this application, the transmitted input is not being received back into the device, so collision detection is not used. This is to be expected since TX_{OUT} and RX_{IN} are transmitted and received on different secondaries.

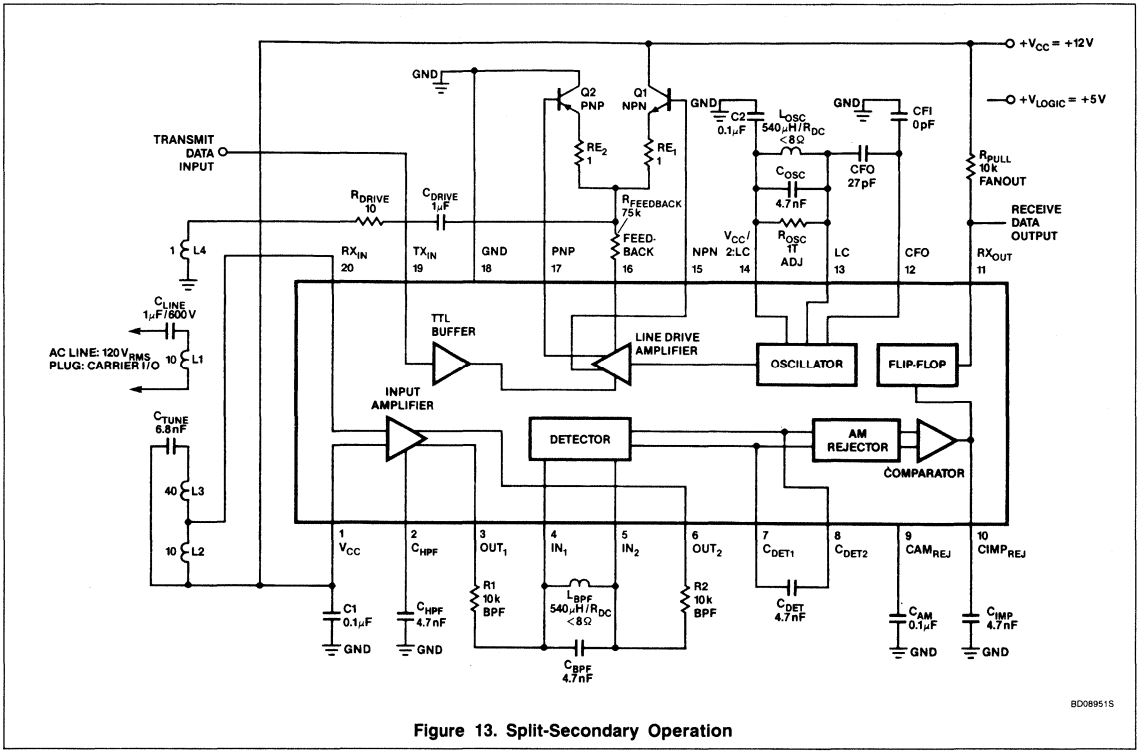


Figure 13. Split-Secondary Operation

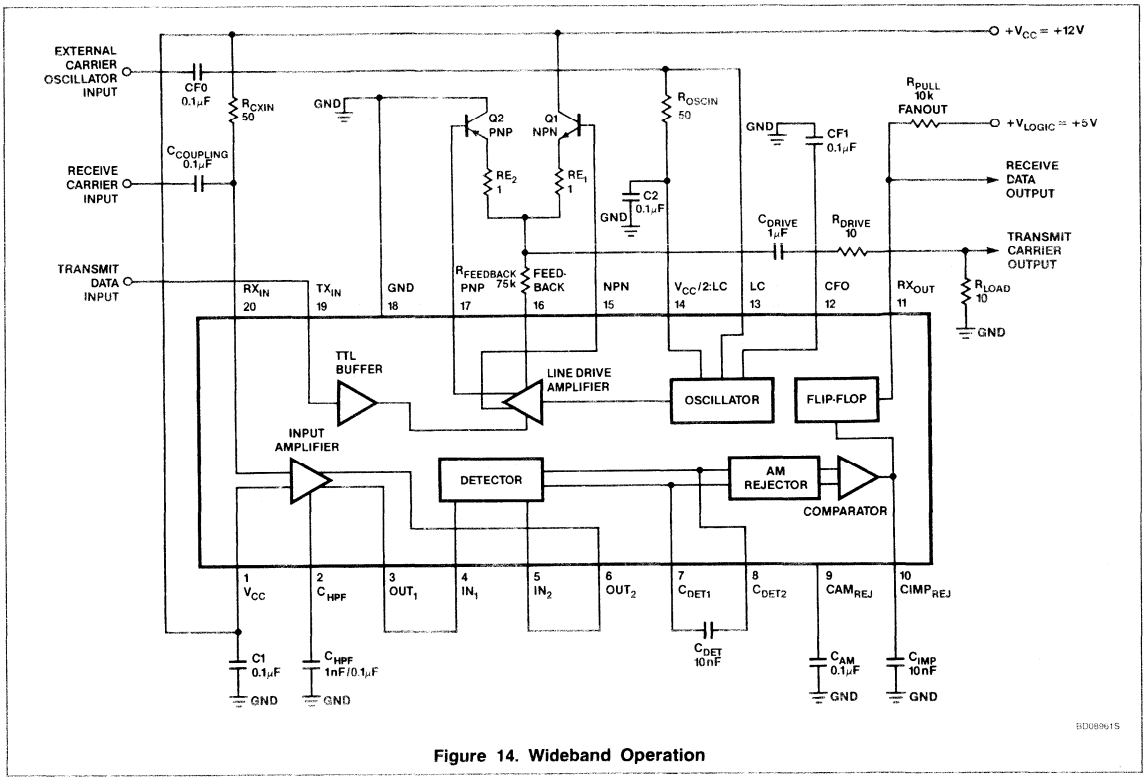


Figure 14. Wideband Operation

WIDEBAND OPERATION

For wideband operation, note in Figure 10 that the bandpass filter is not utilized and the output of the input amplifier is shorted directly to the AM detector to permit all frequencies to pass through. Also note the absence of any transformer coils. The receive input and the transmit output are just AC-coupled to their respective sources and destinations. The external carrier oscillator input is AC-coupled directly to Pin 13 to the LC tank input. It goes through a 50Ω resistor to Pin 14. Pin 12 has a capacitor to ground to prevent the Colpitts oscillator from building up oscillations itself.

This application is ideal for testing the frequency response of the receiver and transmitter. For single frequencies, the 50Ω resistor between Pin 13 and Pin 14 can be replaced with a tuned LC tank circuit.

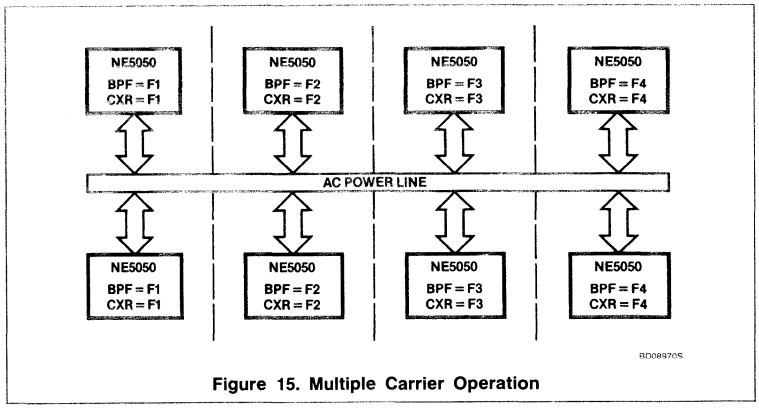


Figure 15. Multiple Carrier Operation

MULTICARRIER OPERATION

This application enables use of multiple points on the network without interference from adjacent transceivers using the same medium. Set up the boards as in the consumer or industrial applications, but use different values for the carrier frequency and the bandpass filter. It is suggested that each carrier be separated as much as possible over the working range of the NE5050. The frequencies should not be multiple integers of each other. This ensures that any harmonics will be suppressed far enough not to interfere with other carriers in the spectrum of operation.

In this type of application, the stopband suppression of the bandpass filters plays a large role in the efficiency of carrier transmission, so active filters should be considered.

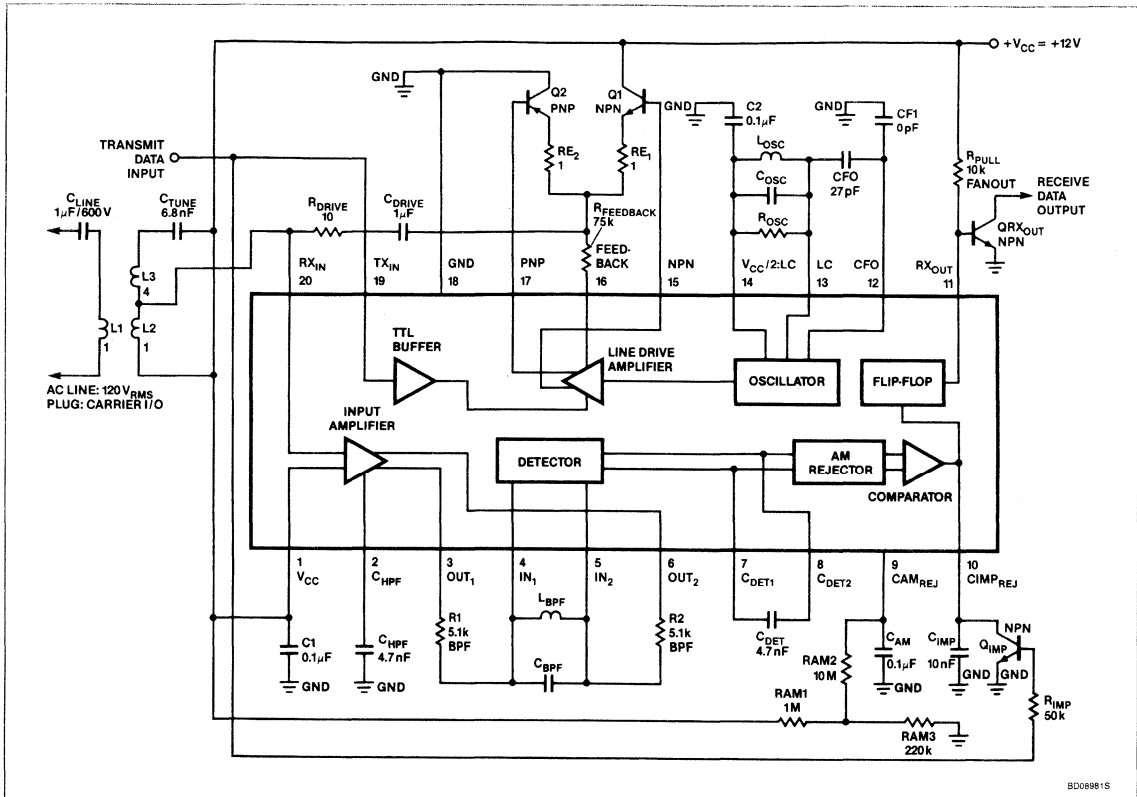


Figure 16. HOMENET Operation at 120kHz

GENERAL ELECTRIC'S HOMENET OPERATION[1]

HOMENET is a software package copyrighted by General Electric Company for the purposes of power line and twisted-pair communication in a residential environment. The software package is called the HOMENET Link Layer and is compatible with the X-10 Home Control System manufactured by BSR and GE.

A working diagram is shown in Figure 12. Technical highlights are as follows:

1. The receiver is disabled while in the transmit mode. This is done by having the transmit input drive an NPN transistor. When turned on, it discharges the impulse capacitor and pulls the comparator output Low (Pin 10). The flip-flop cannot change state. When the data is Low, the oscillator is suppressed and no carrier is detected.
2. HOMENET wants the signal inverted and with an open collector so the user can pick the logic voltage for the receive output (typically +5V).
3. In order to prevent the receive output from going into the standby mode (typically 4 seconds after a TX_{IN} 1-to-0 transition, the RX_{OUT} pin will drift High), the AM rejection pin is externally biased to 2.2V DC with the resistors shown to prevent the comparator from triggering.

NOTE:

1. The HOMENET Link Layer is available as a software package with the Commodore 64 Personal Computer. Current version number available by contacting: The Industry Standards Staff, General Electric Corporation, Fairfield, CT 06431.

TWISTED-PAIR APPLICATIONS

Data transmission over twisted-pair cable enables much higher data rates because the media is usually free of the noise and impedance modulation problems of the power line. Transmission over longer distances is also possible. Many of the same reasons can be applied to coaxial cable. The NE5050 provides an easy interface for twisted-pair operation.

Figure 13 shows the characteristics of the cable used. Four rolls of cable were used. Each roll had over a kilometer of cable which was linked together to create about 15,000 feet of media. The operation is straightforward and is shown in the schematic in Figure 14.

This version has no external drive transistors and has no drive resistor. The receive input comes directly from the end of the secondary (no tuning capacitor); the tap is left unconnected. The other end of the secondary is biased to the power supply. The transformer made by AIE Magnetics connects itself to the twisted-pair wire. The center tap is grounded to the shield of the cable. Only a single-pole filter is used. The AIE transformer was chosen because it enabled the high transmission rates.

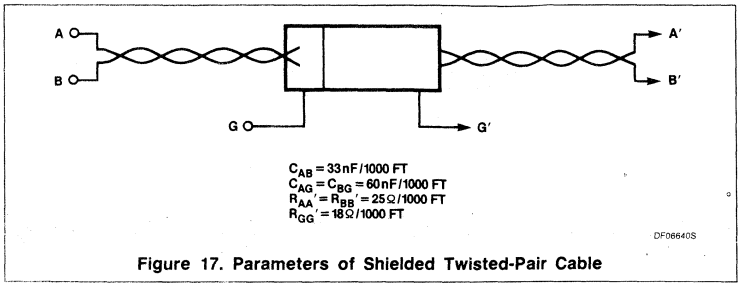


Figure 17. Parameters of Shielded Twisted-Pair Cable

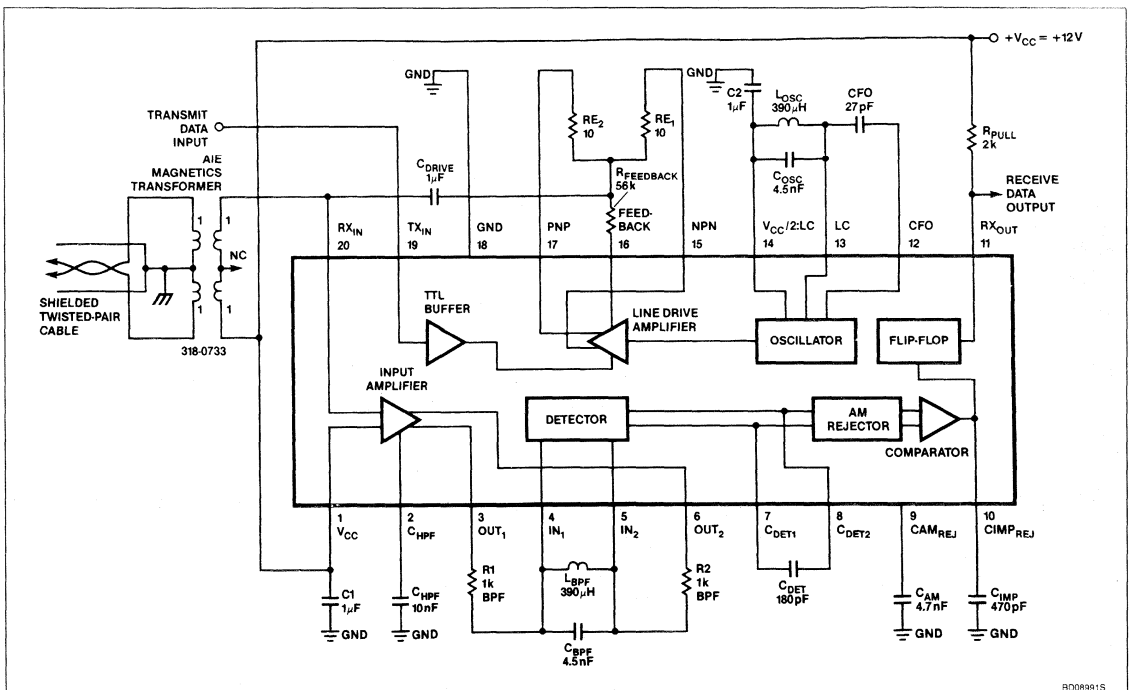


Figure 18. Twisted-Pair Operation: 15,000ft Unequalized Cable at 20kBits/sec

Faster transmission is possible if the cable lengths are shortened. As a rule of thumb, shortening the cable enables a doubling of the transmission rates provided it doesn't exceed the part's (or the transformer's) broadband limitations. Remember, when changing the data rate, C_{AM} has to be adjusted accordingly. Because of the less noisy environment, high voltage transients are absent and C_{IMP} plays less of a role in maintaining a lower bit-error-rate. It will, however, keep the rate-limiting effect outlined earlier.

An additional case was performed in the lab incorporating the following changes:

1. Pin 2 has a 10μF capacitor in series with a 2.2kΩ resistor. The resistor was added to reduce the ringing effects on the RX_{IN}, Pin 20, due to the response of components at higher data rates and higher carrier frequencies. The components will cause the parts to ring. (The transformer is a potential source. The IC will not ring unaided.)
2. R1 = R2 = .1kΩ, C_{BPF} = C_{OSC} = 470pF, L_{BPF} = L_{OSC} = 390μH
3. C_{DET} = 68pF
4. C_{AM} = 1.5nF
5. C_{IMP} = 12pF
6. Connect a 10Ω resistor between the ends of the primary of the transformer (AIE Magnetics 318-0733). This resistor shunts the two twisted wires.

Performance under these changes resulted in a 100kbits/sec data rate over 3,000 feet of shielded twisted-pair wire using a carrier frequency of 370kHz.

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Twisted-Pair Cable Operation at 20kbit/sec

The Belden cable used was 2-conductor, 24 gauge, shielded; trade # is 9452. Fifteen spools were connected in series, 1000 feet each. Longer transmission distance can be achieved if the cable is not shielded (less capacitive loss). The cable is unequalized.

Cable measurements:

Conductor-to-conductor capacitance = 33nF/1000 ft.

Conductor resistance = 25Ω/1000 ft., one conductor

Conductor-to-shield capacitance = 62nF/1000 ft.

Shield resistance = 18Ω/1000 ft.

The carrier frequency is about 125kHz.
The transmitted bit pattern is 1101 0100 1000 0000.
One bit lasts 50μs; therefore, the NRZ data rate is 20kbit/sec.

In Figure 20A the oscillator in the receiver modem is turned off; this prevents crosstalk to the local receiver (possible crosstalk cause: usage of unshielded inductors). This crosstalk creates a first type of jitter in the receiver. In the transmitter there is synchronization between the data and the carrier zero-crossings. The absence of data-to-carrier synchronization creates a second type of jitter in the receiver. From top to bottom: Trace 1 is the transmitter input data, trace 2 is the carrier signal at the transmitter, trace 3 is the carrier at the receiver input, and trace 4 is the demodulated data at the receiver output.

A D-type edge-triggered flip-flop is used to achieve transmitter data-to-carrier synchronization. In the transmitter, the oscillator carrier from Pin 13 is amplified, shaped, and injected as clock signal into the flip-flop. The data is applied at the D input of the flip-flop. The flip-flop output, Q, is connected to the transmitter data input, Pin 19.

Figure 20b illustrates the effect of the two types of jitter upon received data. The oscillator in the receiver is on, and in the transmitter data is applied directly to Pin 19 (data-to-carrier not synchronized). From top to bottom: Trace 1 is the transmitter input data, trace 2 is the carrier signal at the transmitter, trace 3 is the carrier at the receiver input, and trace 4 is the demodulated data at the receiver output. Notice the jitter present in trace 4.

Figure 20c shows data transmission at 25kbit/sec. From top to bottom: Trace 1 is the transmitter input data, trace 2 is the carrier signal at the transmitter, trace 3 is the carrier at the receiver input, and trace 4 is the demodulated data at the receiver output. Notice the absence of jitter in trace 4.

LINE IMPEDANCE MODULATION

The NE5050 receiver has 40dB of AM rejection. To test this, the NE5050 transmitter can be configured to generate 40dB of AM that looks like line impedance modulation. Therefore, an NE5050 can be used to test itself (see Figure 4).

The following are oscilloscope plots of receiver waveforms which demonstrate the effect of impedance modulation on the carrier.

Notice in photographs Figures 20B and C that the AM occurs in the middle of the pulse.

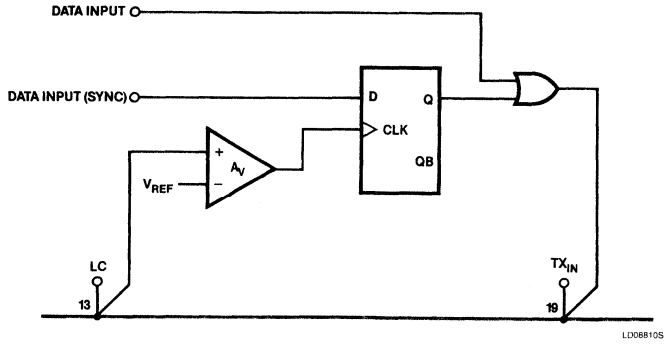
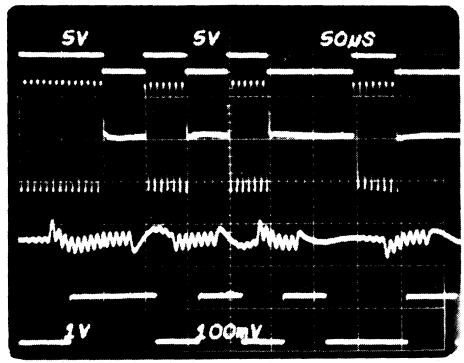
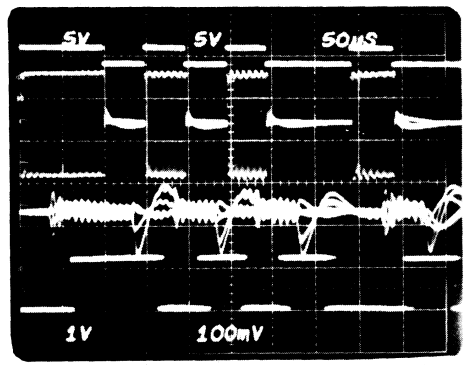


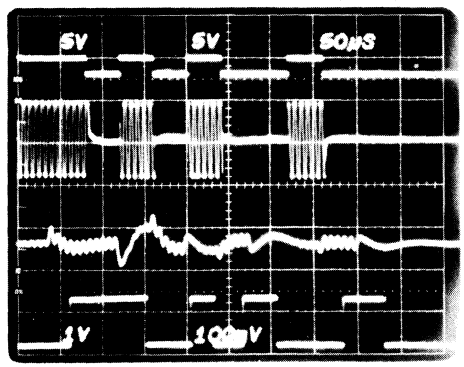
Figure 19. NE5050 Transmitter Data-to-Carrier Synchronization



a.



b.



c.

Figure 20. Twisted-Pair

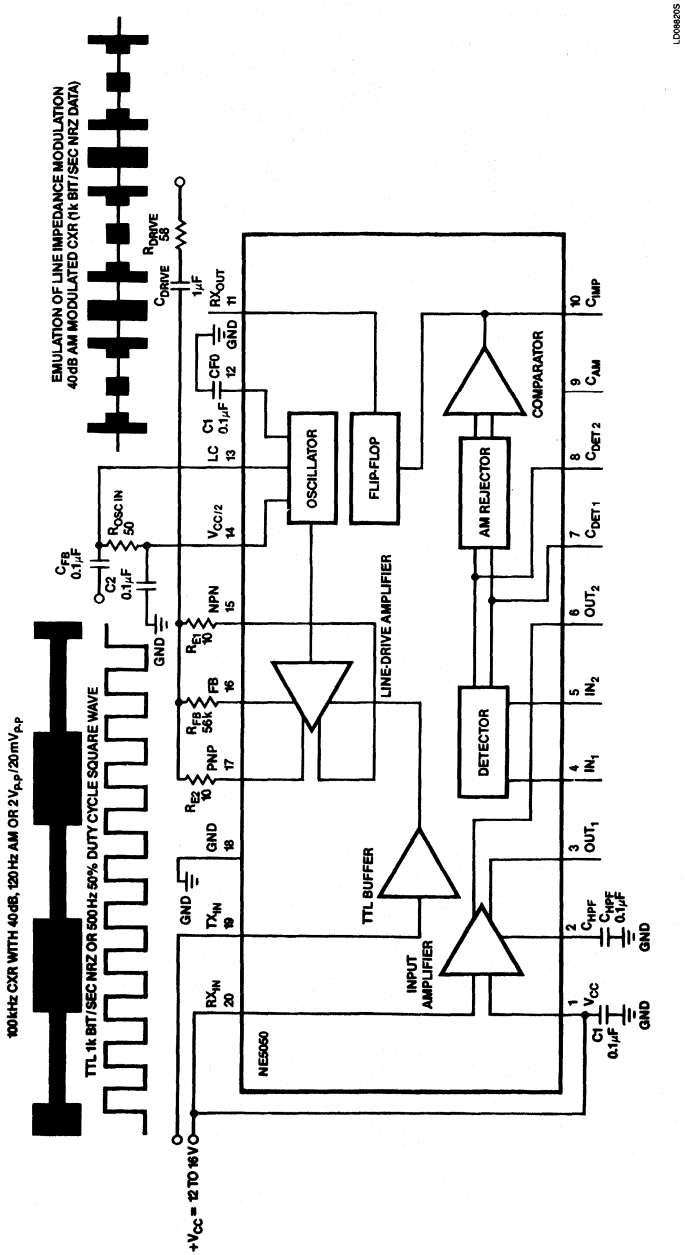
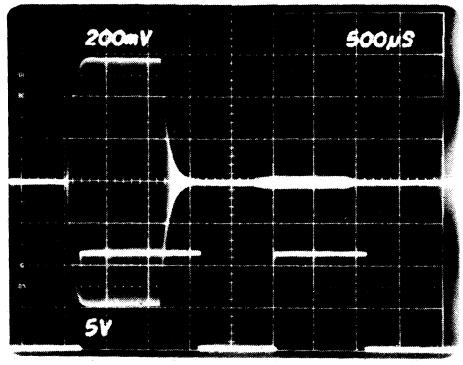
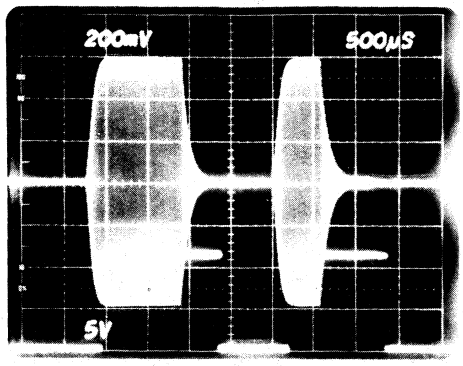


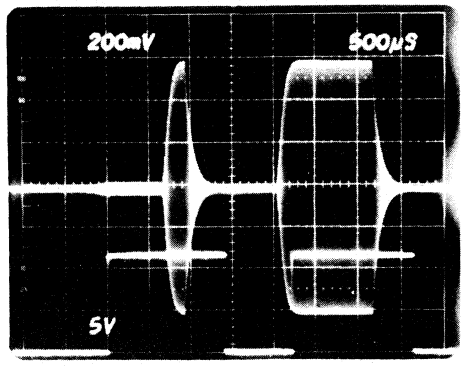
Figure 21. NE5050 Emulation of AC Line Impedance Modulation



a.

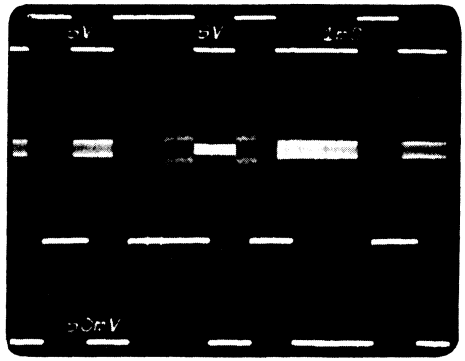


b.



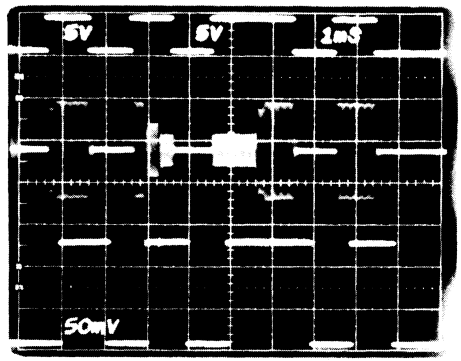
c.

Figure 22. Receiver AM Rejection: General Aspect



OUT-OF-BAND CW INTERFERENCE FROM THE RADIO SHACK POWER LINE TELEPHONE SET

d.



VISIBLE LINE IMPEDANCE MODULATION CAUSED BY 2 LIGHT DIMMERS (IMPULSES PRESENT)

e.

Figure 22. Receiver AM Rejection: General Aspect (Continued)

NE5050 at 50kbit/sec NRZ Data Over the 277V_{RMS} Power Line

50kbit/sec NRZ data was transmitted in the laboratory environment over 20 meters, with 277V_{RMS} AC voltage present and the fluorescent ceiling lights on. A first requirement was to reject the 0 to 100kHz frequency band using a high-pass filter. A 1.5V_{P-P} 10kHz, CW interference had to be filtered out. The AIE Magnetics transformer is used.

The carrier frequency is set around 475kHz using the following components, either in series or in parallel: L = 390μH/8Ω and C = 390pF. In parallel to the LC oscillator tank a 20kΩ potentiometer is used to adjust the transmitted amplitude.

The bit width is 20μs and the observed jitter is < 4μs peak-to-peak. The carrier amplitude at the receiver is between 0.75 to 2V_{P-P}

No external transistors were used. For external transistors the following complementary

NPN-PNP pairs can be used:

2N4401 – 2N4403 or 2N4400 – 2N4402.

For transient protection two back-to-back 1N4744 zener diodes were used.

A 1010 1110 0000 0000 repetitive bit pattern was transmitted.

The BPF resistors are 100Ω, C_{DET} = 390pF, C_{AM} = 2200pF, C_{IMP} = 270pF.

Figure 24a illustrates the transmitted bit pattern (top trace) and the line carrier amplitude (bottom trace).

Figure 24b illustrates the received ASK carrier (top) and the demodulated data (bottom).

Figure 24c illustrates received ASK carrier (top) and the jitter increase in the received data (bottom: jitter < 4μs). Additional noise was deliberately added. Notice the drop in carrier amplitude caused by the low impedance of the noise source.

Over the 20 meters a 6dB carrier attenuation was observed.

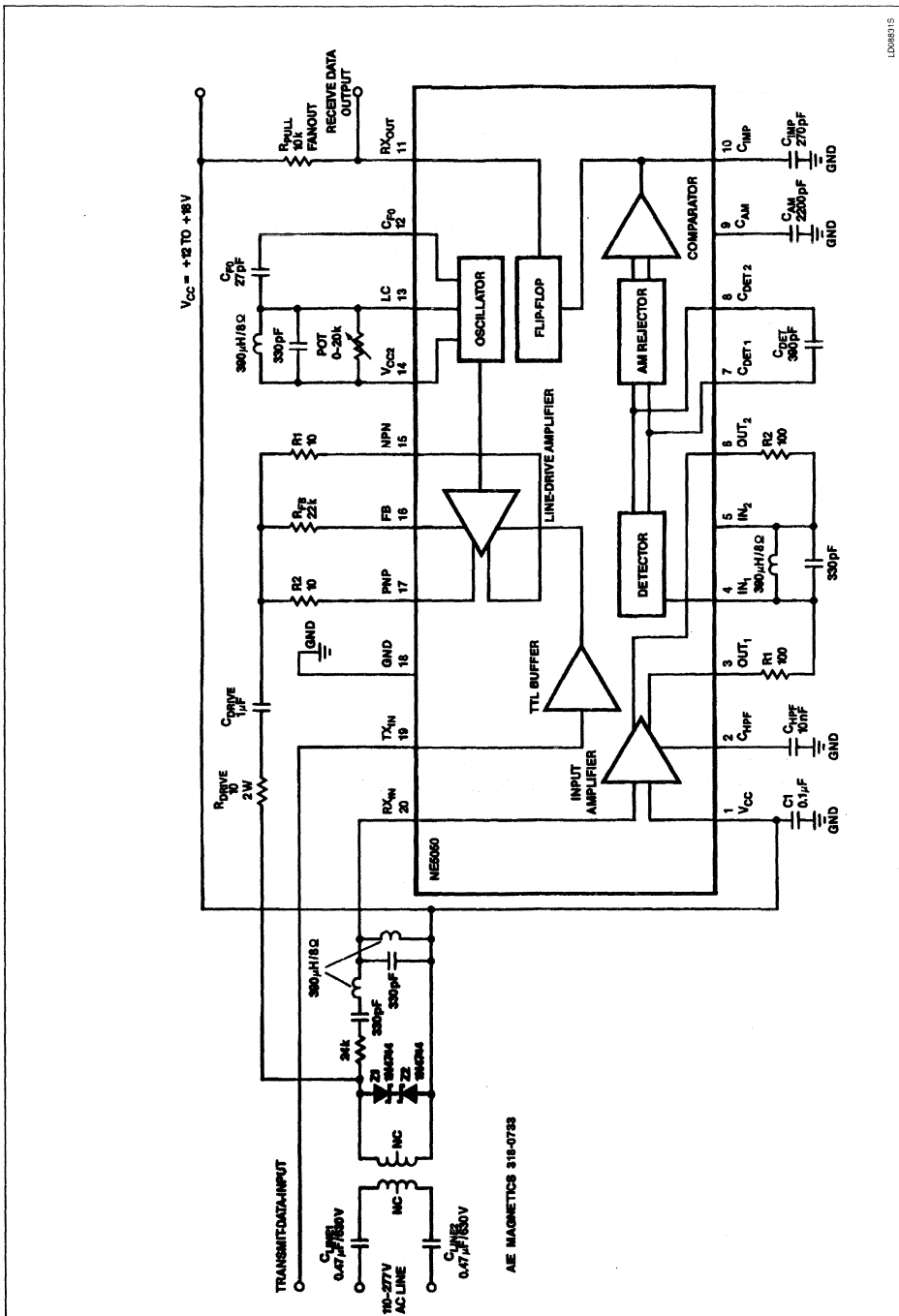
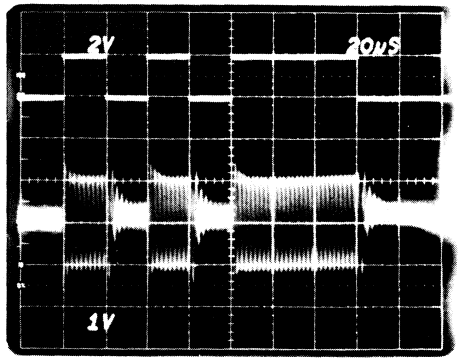
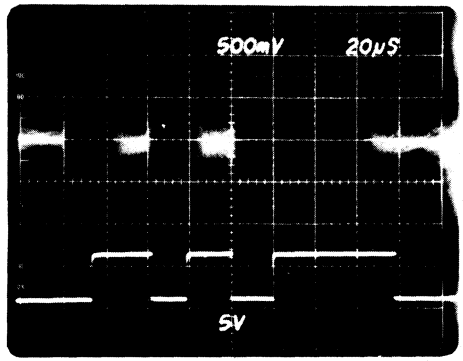


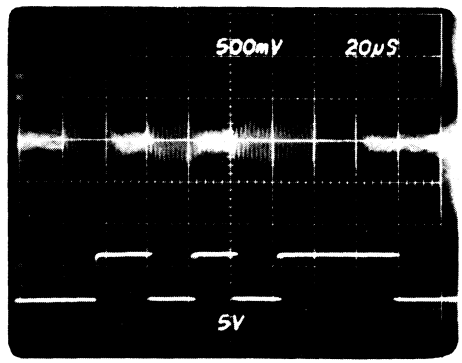
Figure 23. 50kBit/sec on the 277V_{RMS}, Neon Lighting, Ceiling Wires



a.



b.



c.

Figure 24. 50kBits/sec

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Data transmission

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PDV BUS CONTROLLER (DLC)

1. INTRODUCTION

The MEB3000 is a VLSI NMOS device for serial data communication using PDV bus control.

This serial data link controller (DLC) handles serial data communication between devices in industrial control systems. Data is transformed into a serial message format with a redundant check code. The DLC transmits and receives serial data both in NRZ code with additional frame and clock signals, and in Manchester code with intrinsic clock and frame information. Communication with the user device is accomplished via a parallel interface with bus capability.

1.1 Features

- Serial data communication
- Transmits and receives following the "call-reply" principle
- Serial digital interface (SDI) or line interface (LI) for Manchester code on the line system
- 8-bit parallel interface with the processing unit
- Message formatting and cyclic redundancy check (CRC, HD = 4)
- Address recognition
- Interpretation of control fields in data messages
- Central master with "pass mastership" capability
- Independent command acknowledge
- Call retry in case of transmission errors
- Block transfer in DMA mode
- NMOS technology
- TTL compatible I/O levels
- Supply voltage 5 V ± 10%
- Transmission speed 0 to 312.5 kbits/s
- Operating ambient temperature range 0 to + 70 °C

PACKAGE OUTLINE

28-lead DIL; metal ceramic (CERDIL) (SOT87B).

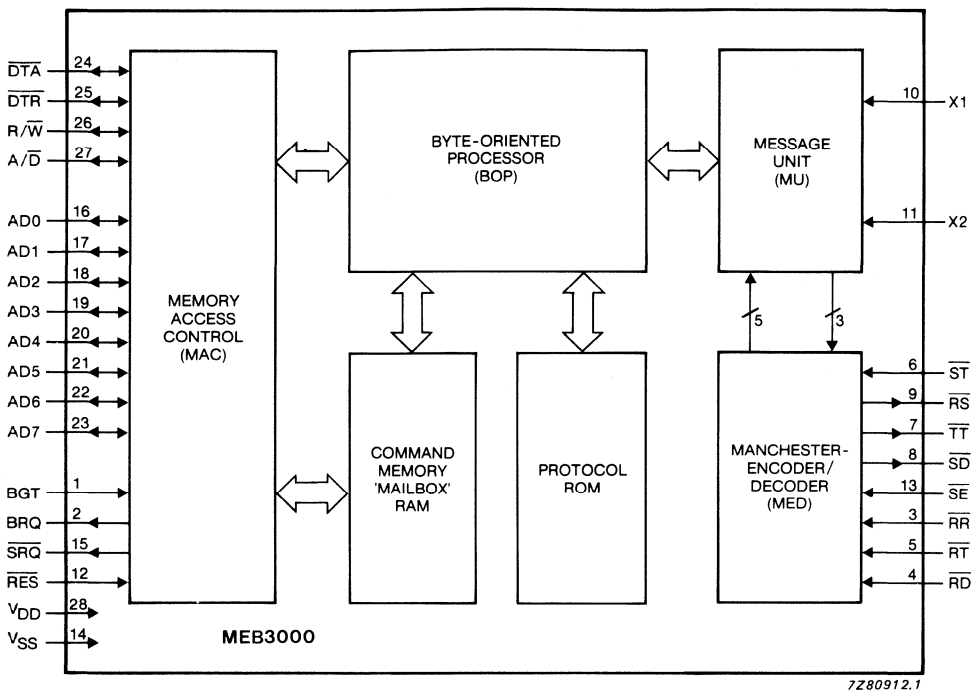


Fig. 1.1 Block diagram.

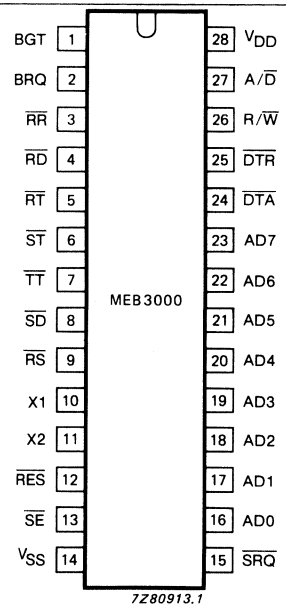


Fig. 1.2 Pinning diagram.

Table 1.1 Pin description

mnemonic	input/ output	pin(s)	function
BGT	I	1	Bus grant. This signal is a response to a bus request (BRQ). During BGT = HIGH, the parallel bus is controlled by the DLC
BRQ	O	2	Bus request. When BRQ is HIGH, the DLC requests control of the parallel bus for a DMA transfer
$\overline{RR}$*	I	3	Receive ready: SDI: receive window, $\overline{RD}$ is valid when $\overline{RR}$ = LOW LI : $\overline{RR}$ must be HIGH
$\overline{RD}$*	I	4	Receive data: SDI: NRZ-coded data LI : Manchester-coded data
$\overline{RT}$*	I	5	Receive timing: SDI: receive clock, the $\overline{RD}$ line is sampled at the positive-going edge of $\overline{RT}$ LI : input for inverse Manchester-coded data
$\overline{ST}$*	I	6	Send timing: SDI: clock information for NRZ-coded data. $\overline{ST}$ controls transmission speed LI : $\overline{ST}$ must be 8-times the transmission bit-rate
$\overline{TT}$*	O	7	Terminal timing: SDI: reflected send clock for $\overline{SD}$ derived from $\overline{ST}$ LI : inverted Manchester-coded data output (3-state output, define via a 5.6 kΩ pull-up resistor)
$\overline{SD}$*	O	8	Send data: SDI: NRZ-coded data LI : Manchester-coded data output (3-state output, define via a 5.6 kΩ pull-up resistor)
$\overline{RS}$*	O	9	Request to send: SDI: valid window for NRZ-coded data LI : oscillator output (3-state output, define via a 5.6 kΩ pull-up resistor)
X1	I	10	External clock, or crystal connection for use with internal oscillator circuit
X2	I	11	Crystal connection
$\overline{RES}$	I	12	Reset. If $\overline{RES}$ = LOW, the DLC is reset to the power-on state and internal registers are cleared
$\overline{SE}$*	I	13	Signal error: SDI: if both $\overline{SE}$ and $\overline{RR}$ are LOW, an error has occurred in the serial data stream LI : $\overline{SE}$ must be LOW
V_{SS}	I	14	Negative supply voltage (ground)
$\overline{SRQ}$	O	15	Service request. $\overline{SRQ}$ becomes LOW whenever a user command is completed. The signal is reset when the processing unit reads the status register
AD0 to AD7	I/O	16 to 23	Parallel interface: bidirectional address/data bus

* These pins are used for serial bus communication. The function of the pins depends on the serial mode selected by the user. The serial mode can be serial digital interface (SDI) or line interface (LI).

DEVELOPMENT DATA

Table 1.1 (continued)

mnemonic	input/ output	pin(s)	function
$\overline{DTA}$	I/O	24	Data transfer acknowledge. This signal terminates a handshake cycle: Read cycle: $\overline{DTA}$ = LOW for data valid Write cycle: $\overline{DTA}$ = LOW for data accepted
$\overline{DTR}$	I/O	25	Data transfer request. Together with DTA (pin 24), this signal synchronizes the data transfer: Read cycle: $\overline{DTR}$ = LOW for data request Write cycle: $\overline{DTR}$ = LOW for data valid
R/$\overline{W}$	I/O	26	Read/write select. This pin, in conjunction with BGT (pin 1), determines the direction of data transfer via the parallel interface: BGT = LOW, parallel interface controlled by processing unit: R/$\overline{W}$ = LOW, A0 to A7 are inputs R/$\overline{W}$ = HIGH, A0 to A7 are outputs BGT = HIGH, parallel interface controlled by DLC: R/$\overline{W}$ = LOW, A0 to A7 are outputs R/$\overline{W}$ = HIGH, A0 to A7 are inputs
A/$\overline{D}$	I/O	27	Address/data select: A/$\overline{D}$ = LOW for data transfer A/$\overline{D}$ = HIGH for address
V_{DD}	I	28	Positive supply voltage

2. GENERAL DESCRIPTION

2.1 Functional description

The DLC is a cost-effective serial bus controller for linking up to 255 stations in a distributed production processing environment. It is a building block that can be used as a "mailbox" for control and data communication.

The DLC is designed in such a way that the bus protocol is rigorously transparent to the user, it will automatically send the appropriate reply message when it receives a message containing its programmed address. Depending on the received function code, this reply message is generated by the DLC itself or taken from a special, user-prepared area in the internal RAM. The internal RAM is the interface between user and DLC, through which messages are passed. If the size of a message exceeds the capacity of the internal RAM, then the DLC can perform DMA to an external memory.

The DLC is always responsible for the assembly of the serial messages and generates check characters and frame signals. When a message is received it is passed to the user without the check characters and frame marks. If an error is detected by the DLC, the user will not be informed of this message but the transmitting DLC will retry the message automatically, by a user-defined number of repetitions.

Two serial modes are possible with the DLC; the serial digital interface (SDI) and the line interface (LI). If SDI is selected, messages are transmitted in NRZ-code and clock and frame information is carried by separate lines. When LI is used, the data is transmitted in Manchester code and the clock and frame signals, together with the information bits, are contained in one serial line only. The inverted signal for LI is available on a separate pin to facilitate a symmetrical line driver.

The parallel interface is compatible with both synchronous and asynchronous microprocessors.

DEVELOPMENT DATA

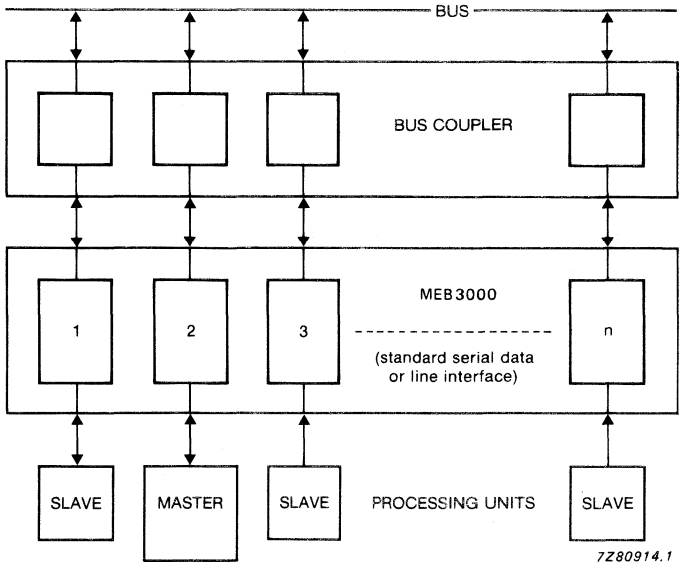


Fig. 2.1 The bus is adapted to the MEB3000 with a bus coupler (the coupler can be omitted from small-area applications).

2.2 Byte-oriented processor (BOP)

The BOP is the central control unit of the DLC and takes care of bus protocol. It communicates with the user via the internal command RAM. If a DLC is programmed to be the master station, then its BOP takes user-prepared call commands from the command RAM and passes the call to the message unit (MU) for transmission. The corresponding reply message is placed in the command RAM by the BOP.

A slave station receives a transmitted message and compares the message address with its own address. When a match is found, the call is placed into the slave's command RAM and a reply message is sent.

The command RAM is divided into 8 fields of 8 bytes each. A field can contain one of the following commands:

- Initialize command
  contains the station type (master station, slave station, listen station), the station address, the maximum number of retries in case of error, and the time-out constants for bus activity.
- Receive command
  contains a complete reply message, prepared by the user. If the station gets a call, it can answer with this message.
- Call command
  contains a call (with addres, function code and data, if any) for another station. A call command is only executed if the station is the bus master or has been granted permission for subtraffic.

All of the 8 command fields are available for user commands to the DLC. For instance, in a master station the command RAM could be filled with one initialize command and 7 call commands. Similarly, in a slave station the 8 fields could be filled with one initialize command, a reply command and 6 receive commands.

In the simplest case, the DLC needs only its own address to communicate with others. Therefore, after a power-on reset, the BOP tries to read the station address via a special DMA from an external register. After the address is known, the DLC can perform simple communication directly through DMA, without control from the command RAM. In this way, non-intelligent devices (i.e. D/A or A/D converters) can be connected directly to the bus system.

Data transfer via the serial bus and management of the complete bus system is accomplished by the use of the following bus control commands coded into the function byte of a message.

- Write call
  causes the BOP to put the received message into a receive command field in the command RAM.
- Read call
  invites the BOP to send a reply message (i.e. execution of a reply command).
- Normalize call
  establishes the termination of initialize command field(s) and requires a new initialization in the slave station(s).
- Status read
  is a call to a station to request a status message. The status message response informs the master of existing reply and call commands in the slave station. For a fast status transfer of multiple slave stations, a quick polling mode is available. In this event, no check characters are sent.
- Quick poll
  is a fast way of reading the status of multiple stations. A quick poll sequence is started by the broadcast of bus command message: START QUICK POLL. After the start, the bus master addresses a number of stations by sending only their address (no function code or check character is sent). An addressed station that does not need service responds only with its address, otherwise the station responds with its address, function code and check character to indicate that it has a reply or call command pending.
- Grant subtraffic
  permits the called station to execute a call and reply sequence, with retries if needed.
- Pass control call
  causes the addressed station to assume bus mastership, while the calling station becomes a slave.

2.3 Memory access control (MAC)

The MAC communicates both with the user and the BOP, and controls the parallel I/O bus. It therefore has two principle tasks:

- Control of read/write cycles between user and internal command RAM.
  In this type of transfer, the handshake lines $\overline{DTR}$, $\overline{DTA}$ and the control lines R/$\overline{W}$ and A/$\overline{D}$ are used. Fig. 2.3 is an example of such read/write cycles.
- The handling of a DMA cycle by command of the BOP.
  In this task the MAC uses the handshake and control lines much in the same way as the user in Fig. 2.3. Before any DMA can be done, the MAC has to gain control of the parallel bus by the use of the signals BRQ and BGT. Every DMA transfer starts with the MAC writing a memory address. This address information is handled by external address counter hardware, so microprocessor types to be used with the DLC are not restricted to specific data/address bus widths.

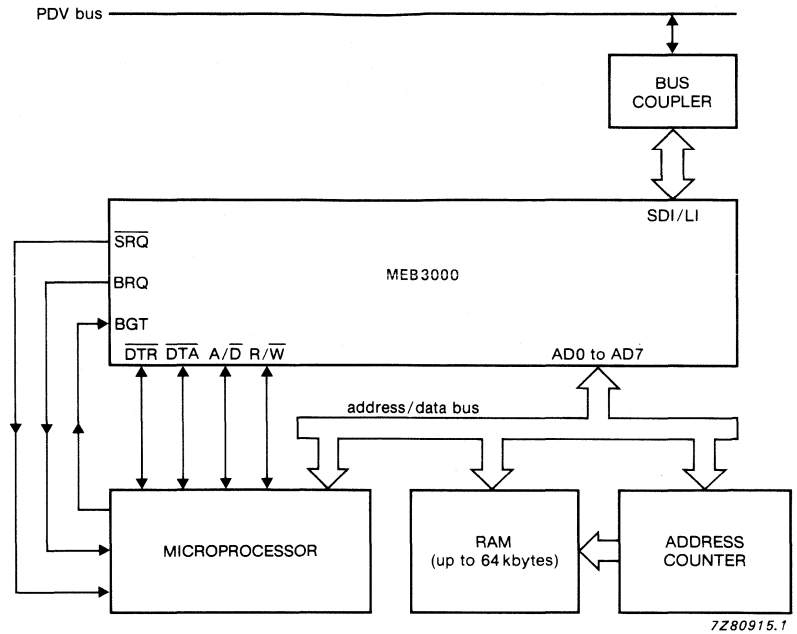


Fig. 2.2 Configuration example: for DMA, BRQ = HIGH for bus request; BGT = HIGH when bus is available; SRQ = LOW indicates command done. The handshake lines are DTR and DTA.

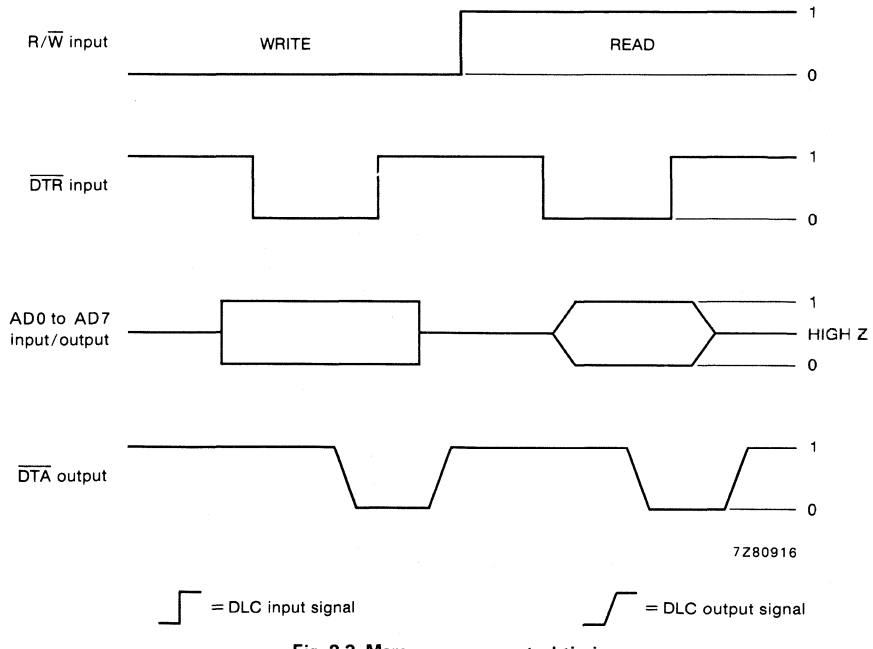


Fig. 2.3 Memory access control timing.

2.4 Message unit (MU)

When the message unit is in transmitting mode it is responsible for formatting the data (the MU assembles the data from the BOP into messages). All signals at the message unit output to the serial data interface are generated as shown in Fig. 2.4 and assembled into a message in the format shown in Fig. 2.5. Every two information bytes are protected with a 1-byte CRC according to the polynomial:

$$X^8 + X^2 + X + 1;\ \text{Code BCH (24,16)}$$

The CRC characters are sent inverted as a protection against jitter.

When the MU receives a message the data bytes are parallel-transferred to the BOP. At the same time, CRC characters are generated and checked with the sent CRC characters and any errors are reported to the BOP.

2.5 Manchester encoder/decoder (MED)

The MED transforms serial data from the MU into Manchester-coded signals with unique start and stop bits added. The Manchester signal is available in true and inverted polarity ($\overline{SD}$ and $\overline{TT}$). The MED requires a clock ($\overline{ST}$) at 8-times the transmission bit-rate.

After recognition of a start bit, the MED receiver continuously synchronizes to polarity changes of the data input. The received data is converted into NRZ code and passed to the MU.

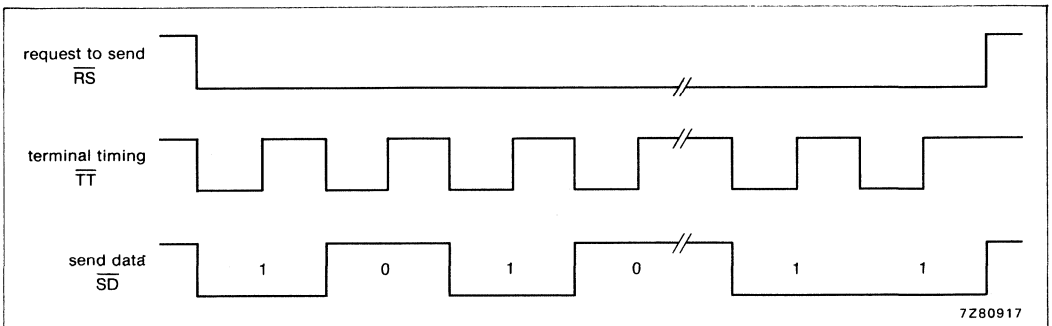


Fig. 2.4 SDI output signals.

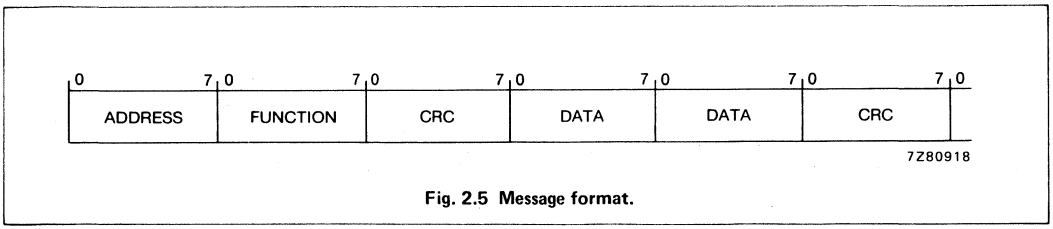


Fig. 2.5 Message format.

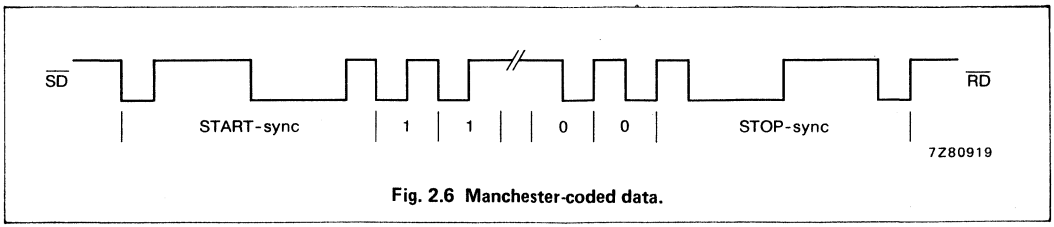


Fig. 2.6 Manchester-coded data.

3. PROGRAMMING AND OPERATION

3.1 Command memory

From the user's point of view, the DLC is comparable to a mailbox. It accepts messages that are to be sent to other stations on the bus and passes messages coming from them. The interface between the user and the DLC is the command memory, a 64 x 8-bit RAM, which both user and DLC can read from or write to.

The command memory is divided into 8 fields of 8 bytes each (command fields) in which the user puts his commands. Any of these fields can contain a PDV-bus message.

This structure requires command-oriented operation of the DLC.

The command memory is addressed indirectly, i.e. the applied addres is stored within an address-latch. After each access the address-latch automatically increments the three least-significant bits of the stored address.

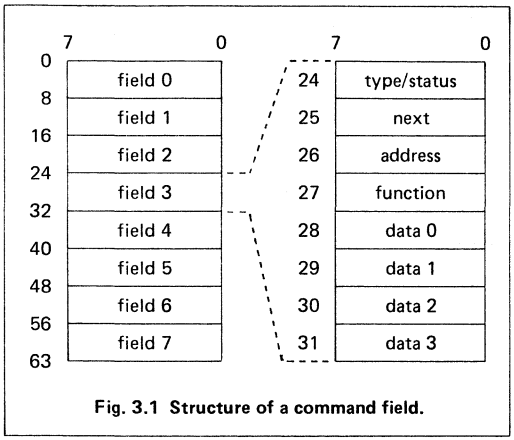


Fig. 3.1 Structure of a command field.

3.1.1 Command types

The first two bytes of each command field contain information about:

- the type of command (type)
- status of the command (status)
- the next command field (next)

Four types of commands exist:

type nibble:

a)	0	0	0	0	initialize command
b)	1	0	0	1	call command
c)	1	0	1	0	reply command
d)	1	0	1	1	receive command

a) Initialize command
this command contains all parameters that a station needs for active participation in the bus traffic.

b) Call command
can only be executed by the bus master and by stations that have permission from the master to execute a call command (subtraffic).

c) Reply command
this command is needed for answering a call from a station at any time a call READ INDIRECT is received by the station.

d) Receive call
this command is needed for storing a message from a station at any time a call WRITE INDIRECT is received by the station.

3.1.2 Command status

The status of a command field determines whether the field is accessible by the user or by the DLC. It also indicates the "ready" or "done" status of a command and the successfulness of a completed command.

The various status can be:

a) Status "normalized"
After a reset, all 8 command fields are cleared and the user has access to the fields.

b) Status "ready"
If the user has completed preparing a command, he can set the status of this field to "ready" which gives the right of access to the DLC for execution.

c) Status "done"
After successful execution of a command, the DLC sets status "done" and this returns access to the user.

d) Status "error"
When an error occurs during execution of a command, the DLC sets status "error". The type of error is encoded in the field and access is given back to the user.

e) Status "rejected"
There are two conditions under which the DLC rejects a command:
- when the command would cause a bus protocol violation if it were executed;
- when the actual length of a data transmission is greater than the expected maximum data length.

When the status "rejected" is present, the right of access is returned to the user.

Table 3.1 Status of command fields

command type	code in byte 0	description
initialization	0 0 0 0 0 0 0 0	normalized (hardware reset)
	0 0 0 0 0 0 0 1	ready
	0 0 0 0 0 0 1 0	command terminated by NORMALIZE call (software reset)
	0 0 0 0 0 1 1 0	TLN time-out
	0 0 0 0 1 0 1 0	PASS CONTROL call received
	0 0 0 0 1 1 1 0	reception hinders transmission of the call
call	1 0 0 1 0 0 0 0	normalized (cleared)
	1 0 0 1 0 0 0 1	ready
	1 0 0 1 0 0 1 0	done
	1 0 0 1 1 0 0 0	error, NMAX retries
	1 0 0 1 1 1 0 0	error, CRC or bit error
	1 0 0 1 1 0 1 0	error, handshake
	1 0 0 1 0 1 0 0	rejected, actual length greater than expected length
	1 0 0 1 0 1 1 0	rejected, protocol violation (see 3.3.2)
reply	1 0 1 0 0 0 0 0	normalized
	1 0 1 0 0 0 0 1	ready
	1 0 1 0 0 0 1 0	done
receive	1 0 1 1 0 0 0 0	normalized
	1 0 1 1 0 0 0 1	ready
	1 0 1 1 0 0 1 0	done
	1 0 1 1 0 1 0 0	rejected, actual length greater than expected length

3.1.3 Command sequencing

The second byte of a command field points to the next command field of the same type. By using this "next" field, the user can create a chain of commands that are automatically executed in the given order. The chain length can be chosen freely but two restrictions apply:

- the initialize command always occupies field 0;
- immediately after initialization, the DLC expects
  the first call command in field 1,
  the first reply command in field 2,
  the first receive command in field 3.

As an example of command sequencing, if the "next" field indicates "field 5" then the DLC will take the field with byte address 40 as the next command field of this type (see Fig. 3.2).

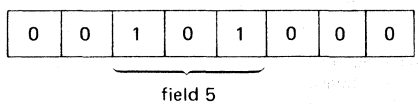


Fig. 3.2 Example of command sequencing.

If the current field is the last to be required, the "next" field should be written with the user's own address and the DLC then waits for a new "ready" message from the processing unit. The "next" field should never be written with zeros as this would destroy the initialize command.

3.1.4 The information part of a command field

Bytes 2 to 7 of a command field contain information for PDV-bus messages. If these messages exceed a data length of four bytes, all bytes are read or written by DMA to external memory, rather than from or to the command field. In DMA mode, the bytes 4 to 7 of the command field serve to indicate the length and start address of the DMA transfer (see Fig. 3.3).

Two length parameters (byte 4) are defined:

- length "A", the actual data length of a message as determined by the transmitter command field; and
- length "E", the expected data length of a message as determined by the receiver command field.

The actual length "A" may never exceed the expected length "E". The data length of a message can vary between 1 and 256 bytes; the code for 256 bytes is 0.

0	type	status
1	next	
2	address	
3	function	
4	length	
5	data (1)	
6	external address (2)	
7	external address (3)	

(1) Byte 5 is an available single data byte.
(2) lower byte.
(3) higher byte.

Fig. 3.3 Command field for DMA mode; data size > 4 bytes.

3.2.2 Initialization by command

initialize	status
station type	
station address	
NMAX	TAB
TAN	
TST	
TLN0 (1)	
TLN1 (2)	

(1) lower byte.
(2) higher byte.

Fig. 3.4 Initialization command field.

3.2 Initialization

During initialization of the DLC, the parameters necessary for each participant in the bus traffic are loaded. An initialization can be caused by a RESET command, by reception of the message "normalize" and by reception of a "pass control" call. After TLN time units, the initialization field is terminated with status "TLN expired" and the DLC waits to receive parameters from the user and the setting "ready" call from the processing unit.

3.2.1 Self-initialization

Self-initialization is a "stand alone" mode in which the DLC can be used for simple I/O operation. The DLC itself controls the handling of the complete bus protocol and addresses the attached peripherals (e.g. D/A and/or A/D converters) for read/write operations.

Every participant in the bus system needs at least its own address so that it is able to receive messages. At the start of an initialization, the DLC tries to read its address from an external register and uses the $\overline{SRQ}$ line as a handshake line. The DLC tests the BGT line for a HIGH without requesting DMA with BRQ. This condition means that the DMA permission has been granted without a request and, if this condition is true, the DLC reads a byte via the parallel data lines by pulling $\overline{SRQ}$ "LOW". ($\overline{SRQ}$ can be used to enable a 3-state buffer.)

If self-initialization is successful, the DLC does not expect more parameters and is now in a mode in which the command memory is not used but only direct I/O transfers are possible. The DLC responds to all correct PDV-protocol calls, however, the bus commands with function code WRITE INDIRECT or READ INDIRECT are not acknowledged. The call NORMALIZE causes a new self-initialization.

If the self-initialization could not be carried out because BGT was LOW, the DLC waits for the initialization command field to be set to ready. This command is used once and is located at position 0 in the command field.

The bytes of the initialization command field are loaded with the necessary operational parameters. The DLC supports all station types that are defined in the PDV bus (see also 3.3). The station type is coded in the byte "station type" as follows:

station type

'FF'H	1	1	1	1	1	1	1	1	master station
'01'H	X	X	X	X	X	X	0	1	slave station
'00'H	X	X	X	X	X	X	0	0	listen station
'02'H	X	X	X	X	X	X	1	0	monitor station

The "station address" byte (Fig. 3.4) can contain the address for any of 255 stations. The address 255 is the "broadcast" address to which all stations respond.

The nibble "NMAX" contains the number of retries caused by an error in a received message. After NMAX retries, the call command field is marked "terminated with error".

The various time-out constants for guarding the call-reply cycles are also stored in the initialization command field. The unit of time is the time needed for transmission of 32 bits. The DLC always records the time elapsed between a call being sent and the reply being received.

The time-out parameters and the limits imposed on them are as follows; the expression DMAX represents the maximum number of bytes in a message.

3.2.2 Initialization by command (continued)

TAB $15 > TAB > 2$	maximum time between call and reply for quick poll and status read
TAN $255 > TAN > 3/8*DMAX + 2$	maximum time between call and reply in normal call-reply cycle
TST $255 > TST > TAN*(NMAX + 2) + 4$	maximum time between grant subtraffic and the status read that closes the subtraffic
TLN $2^{16} > TLN > 4*TAN$	TAN guards the bus master activity. The bus master becomes active within TLN time units. All guarding stations have different TLN values. In this scheme, the station with the smallest TLN value will replace a malfunctioning master

A time-out parameter having a value 0 causes the DLC to disable the corresponding counter start.

The initialization command is terminated after one of the following events:

- a normal message is received;
- time-out on TLN;
- a pass control message is received;
- reception hinders transmission of the call.

Note: If the initialization command is terminated by one of the above events, the other command fields of the DLC remain unchanged. However, it is for the user to correct the "next" parameter of the fields because the DLC expects the first commands of each type to be located as indicated in 3.1.3.

3.3 Station types

A PDV system contains one or more master stations (only one of which is active at a time), slave stations, and listen stations. The monitor station functions only as a safeguard for the bus traffic.

The DLC supports all station types. The amount of extra hardware needed depends upon the complexity of the performance demanded of a station. A simple example is a station with just one DLC and D/A or A/D converter, but a station could also be a complex microprocessor-based system. As described in 3.2.2, the type of station that the DLC performs is determined during the initialization command.

3.3.1 Master station

In the master station mode, the DLC executes its call commands without checking the contents. The user should take care of useful command parameters. The initialization command for a master station must contain:

- the station address;
- the station type;
- TAN, NMAX;
- TAB, if the quick poll or status read is used in the system;
- TST, if the system employs subtraffic.

3.3.2 Slave station

A slave station cannot initiate a message directly but it responds to all calls that contain either its address or the general call address (the broadcast address 255).

The user should supply the necessary reply commands. An exception to this rule is for calls that contain only bus management function codes as the DLC can handle these without user involvement.

If the command memory contains a call, the DLC requests permission for subtraffic from the bus master. This request can be transmitted as part of any reply message. After subtraffic permission is granted, the call is transmitted and the reply is taken into the call command field. The end of subtraffic is signalled to the bus master by the status reply from the station that carried out the subtraffic.

The reception of a message containing the function code NORMALIZE or PASS CONTROL causes the DLC to re-enter its initialization routine after it has marked the initialization command field accordingly.

If the TLN parameter is different from zero, the DLC will guard the activity of the master station. If the master fails to send any call within the time limit, the DLC marks its initialize command, and waits for user instructions (a new initialization). Normally the station will take over the master function.

The DLC of a slave station checks each command for validity. In subtraffic, all messages without data are forbidden, i.e. the bus management messages START QUICK POLL and NORMALIZE are inhibited, and also messages with function code READ INDIRECT (to avoid loss of data) and WRITE INDIRECT WITHOUT TERMINATION. If a forbidden command code is set "ready", the DLC sets "rejected" in the command status nibble.

The DLC also inhibits the use of a reply field for a call, any reply message is automatically marked as such by the DLC.

The initialize command for a slave must contain:

- the station address;
- the station type;
- TAN, NMAX if subtraffic is required for the slave station;
- TLN if the slave station should guard the bus master.

3.3.3 Listen station

A listen station behaves like a slave station but it also receives all replies from all other bus stations. These messages are overheard and delivered into the ready receive command fields; they are treated like WRITE INDIRECT but not replied to.

This station supports the broadcasting of data to a group of stations. A station of this kind can easily replace a bus master as it keeps a list of participating stations.

3.3.4 Monitor station

A monitor has no address and is never active on the bus. Only receive commands and initialization are given in the command fields. Every message received without errors by a monitor station is delivered to a ready command field.

A monitor station can only be re-initialized by a RESET. After a reset, the DLC clears its command memory and starts initialization. The initialization command for a monitor station requires only one parameter: the station type.

3.4 Status word and service request

3.4.1 Status of the DLC

Information about the progress of command processing can be read in compact form by means of a status word. This feature is provided to avoid unnecessary command memory scanning. The status word is a read-only register at address (01xxxxxx).

status word

REP	CALL	P2	P1	P0	0	ERR	WAT

REP — At least one reply field ready.

CALL — At least one call field ready.

P2, P1, P0 — Number of the most-recently terminated field.

ERR — Summing error message, set if a call command has been concluded with errors.

WAT — Write attempt. This bit is set when the DLC receives a message with function code WRITE INDIRECT and has no receive command ready for it.

3.4.2 Service request ($\overline{SRQ}$)

The $\overline{SRQ}$ pin is active as follows:

- after an update of the status word (i.e. after termination of a command);
- after normalization of the command memory. In this event $\overline{SRQ}$ indicates "waiting for initialization".

The service request is removed after a status word read.

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4. FUNCTION CODES IN PDV-BUS PROTOCOL

(See also Chapter 5, Error List)

There are seven function codes to control the bus system and data transfer. The bus system control codes are NORMALIZATION, STATUS READ, QUICK POLL, SUBTRAFFIC and PASS CONTROL, and those for data transfer are WRITE and READ. The five bus control codes and the 'write indirect without termination' and 'read indirect' parts of the data transfer codes are only allowed for the bus master station, the DLC of a slave station will reject these functions.

4.1 Normalization

Normalization is used as a software reset. If the master station ceases to receive messages it either normalizes each station separately or globally (all together). A station that is not accessible after this procedure must be faulty.

Transmission of a message with function code NORMALIZE causes termination of the initialization command, after which the stations enter a new initialization phase. In order to normalize just one station, its address is given in the command field. All stations are normalized if the address field contains the global address (FFH). The call is transmitted only once and is then marked "done". In the addressed station(s) the initialization field is marked "normalized" and commands that had not been executed remain unchanged in the command memory. Normalized station(s) expect subsequent commands to conform to the command sequencing (3.1.3).

There is no reply to the normalization command.

Example

Before command execution NORMALIZE:

	master station call field		slave station initialization field	
0	call	ready	init.	ready
1	next		station type	
2	address		address	
3	NORM.		(NMAX)	(TAB)
4	---		(TAN)	
5	---		(TST)	
6	---		(TLN0)	
7	---		(TLN1)	

() = only when needed.

After command execution:

	master station call field		slave station initialization field	
0	call	done	init.	norm.
1	next		station type	
2	address		address	
3	NORM.		(NMAX)	(TAB)
4	---		(TAN)	
5	---		(TST)	
6	---		(TLN0)	
7	---		(TLN1)	

() = only when needed.

4.2 Status read

Transmission of a call with function code STATUS READ causes the addressed slave to reply with a status word as the function code of its reply message. With this status word the slave can signal to the master that a call command or a reply command is ready in the command memory of the slave.

If the status reply is received with error, the read status call is retried NMAX times. If no error-free status reply can be obtained, the call command is marked "error".

If the reply message was received correctly, the command is marked "done" and the status word function code of the reply is placed in the command field at position 3. Every time a DLC sends a reply message the status is automatically entered into the function code field (see 4.8).

Example

Master station call field:

	Before command execution		After command execution: no error		After command execution: error	
0	call	ready	call	done	call	error
1	next		next		next	
2	address		address		address	
3	STAT		function		function	
4	---		---		---	
5	---		---		---	
6	---		---		---	
7	---		---		---	

4.3 Quick poll

Quick poll allows a fast status read of several stations. All stations are prepared for a quick poll sequence by a general call (bytes 2 and 3 of the call command field). The general call is transmitted only once and there are no replies.

In byte 4 of the same message, the first slave station is addressed for its status. The addressed slave responds with a status function code (see 4.2), but if the slave does not have a call field and a reply field ready, it responds only with its address (function code = 0).

The response of the addressed station is written in the quick poll command field (byte 5) as follows:

byte = "0" if the addressed station responds with only its address; or

byte = "FFH" if the addressed station does not respond; or

byte = "function" if the addressed station replies with a status function code.

After this the next station is addressed (byte 6) and the result is written in byte 7. If the next command field also contains the function code QUICK POLL, the polling continues without the requirement for a new general call. In this way any number of stations can be polled, provided that the user supplies new QUICK POLL commands in time. After execution the command field is marked "done".

Example

Station (A) does not reply, stations (B) and (D) send their status and station (C) replies but without a service request.

Master station call field:

	before command execution		after command execution	
20H + 0	call | ready		0	call | done
1	next (e.g. 28H)		1	next (e.g. 28H)
2	global address (≙ FFH)		2	global address (≙ FFH)
3	STQP		3	STQP
4	address (A)		4	address (A)
5	0		5	'FFH'
6	address (B)		6	address (B)
7	0		7	function (B)

	before next command execution		after next command execution	
28H + 0	call | ready		0	call | done
1	next (e.g. 20H)		1	next (e.g. 20H)
2	global address		2	global address
3	STQP		3	STQP
4	address (C)		4	address (C)
5	0		5	0
6	address (D)		6	address (D)
7	0		7	function (D)

4.4 Subtraffic

With the call START SUBTRAFFIC (STST) an addressed station (A) is granted permission to execute a call command to a station (B), to receive the reply and, in case of errors, to retry the call.

The subtraffic is terminated by a status reply from the executing station (A) to the bus master. If the bus master does not receive a status reply within the subtraffic time limit (TST), the call START SUBTRAFFIC is retried. If the master does not receive a status reply within NMAX retries, the call command field is marked "terminated with error".*

When the master receives a status reply from station (A), the command is marked "done" and the function byte of the reply is placed in position 3 of the command field.

If the addressed station (A) has no call field reply, it replies immediately with a status reply.

* In subsequent text this is referred to as "error".

Example

A receive command is ready at station (B) and the WRITE INDIRECT call of station (A) is executed. Following the write message, station (B) replies with a message containing the function code "command executed" and this is placed in the command field of station (A).

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4.4 Subtraffic (continued)

Before command execution:

	master station call field		slave station (A) call field		slave station (B) receive field	
0	call	ready	call	ready	receive	ready
1	next		next		next	
2	address (A)		address (B)		----	
3	STST		WRITE INDIRECT 4		----	
4	----		data 0		length (E)	
5	----		data 1		----	
6	----		data 2		external receive address 0	
7	----		data 3		external receive address 1	

After execution of master call and slave commands:

	master station call field		slave station (A) call field		slave station (B) receive field	
0	call	done	call	done	receive	done
1	next		next		next	
2	address (A)		address (B)		address (B)	
3	function (A)		function (B)		WRITE INDIRECT 4	
4	----		data 0		data 0	
5	----		data 1		data 1	
6	----		data 2		data 2	
7	----		data 3		data 3	

Example

Before command execution PASS CONTROL:

	master station call field		slave station initialization field	
0	call	ready	init.	ready
1	next		station type	
2	address		address	
3	PCT		NMAX	TAB
4	----		TAN	
5	----		TST	
6	----		TLN0	
7	----		TLN1	

After command execution:

	master station call field		slave station initialization field	
0	call	done	init.	1010*
1	next		station type	
2	address		address	
3	PCT		NMAX	TAB
4	----		TAN	
5	----		TST	
6	----		TLN0	
7	----		TLN1	

* Terminated by PASS CONTROL.

4.5 Pass control

The bus master passes "mastership" to the addressed station by sending the call PASS CONTROL (PCT). The call is sent only once and there is no reply. The calling station marks its command field with "done" and switches to slave operation, i.e. it calls only in subtraffic. The addressed station marks its initialization command field with "pass control" (= 'OAH') and awaits initialization as a master by the user. All other command fields are unaffected; the station expecting its next commands in the field as described in 3.1.3.

4.6 Write

Write calls are used to send data to slave stations. The following calls are possible:

- WRITE DIRECT, fixed data format and without use of command field memory;
- WRITE INDIRECT, several data formats;
- WRITE INDIRECT WITHOUT TERMINATION, several data formats.

4.6.1 Write direct

When the call WRITE DIRECT is sent, the receiving DLC writes two data bytes via DMA preceded by a two-byte DMA address, without using any receiving command field.

The following parameters must be supplied in the command field of the master:

- address of the slave;
- function code WRITE DIRECT;
- DMA address (address = 0 for LOW byte, address = 1 for HIGH byte);
- the two data bytes (data 1 is the LOW byte, data 2 is the HIGH byte).

The called station writes the DMA address directly to the processing unit interface and transmits a status reply as in 4.2. No reply will be sent if any errors occur in reception or in the handshake with the processing unit.

If an error occurs the calling station will retry NMAX times.

After the call command is executed successfully, the call command field is marked "done" and the function byte of the status reply is placed in position 3. If there is no reply the field is marked "error".

Example

Master station call field:

	before command execution		after command execution	
0	call	ready	call	done
1	next		next	
2	address		address	
3	WRITE DIRECT		function byte of called station	
4	address 0		address 0	
5	address 1		address 1	
6	data 1		data 1	
7	data 2		data 2	

4.6.2 Write indirect

Transmission of the call WRITE INDIRECT causes placing of the sent data into a prepared receive command field.

Basically, calls with 2 or 4 data bytes can be distinguished from calls with a variable number of data bytes. If the data length is 2 or 4 bytes, the data bytes put in the receiving field are merely a copy of the data bytes in the calling field. When the data length is variable, the DLC first transmits the bytes 2 to 5 from the command field and then data from an external memory, starting at the address given by positions 5 and 6 of the command field.

The actual data length (A) field determines the length of the transmitted data string (1 to 256 bytes can be sent, (A) is coded 0 for a 256-byte data length). The receiving station tests that the length (A) is within the foreseen maximum length (E) in the receive command field. If it is, then the data stream is directed to the external memory of the slave, starting at the address given by bytes 5 and 6 of the receive command field. If (E) $<$ (A), the receive command field is marked "error" and a status reply containing a function code indicating "command not executed" will be transmitted to the master station.

If the number of data bytes is odd, the data are extended with a dummy byte (this is necessary for assembling the check character). This byte is stripped-off in the receiver.

If the call is received without error, the slave sends a status reply as in 4.2. The call is retried NMAX times when errors occur. If no receiving command is set ready, the addressed station replies with a status function code in which bit 4 is set (command not executed).

When the addressed station answers, the call field is marked "done" and the function code of the reply is put in byte 3. If errors occur and the retries are not successful the call field is marked "error". Nothing is written in the receive command field when errors occur and the field is saved for other use.

Example

Call WRITE INDIRECT with two bytes.

Before command execution WRITE INDIRECT:

	calling station call field		slave station receive field	
0	call	ready	receive	ready
1	next		next	
2	address		---	
3	WRITE INDIRECT 2		---	
4	data 1		length (E)	
5	data 2		---	
6	---		external receive address 0	
7	---		external receive address 1	

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4.6.2 (continued)

After command execution:

	calling station call field	slave station receive field
0	call / done	receive / done
1	next	next
2	address	address
3	function	WRITE INDIRECT 2
4	data 1	data 1
5	data 2	data 2
6	---	external receive address 0
7	---	external receive address 1

After command execution:

	calling station call field	slave station receive field
0	call / done	receive / done
1	next	next
2	address	address
3	function	WRITE INDIR. VAR.
4	length (A)	length (A)
5	data	data
6	external call address 0	external receive address 0
7	external call address 1	external receive address 1

Example

Call WRITE INDIRECT with variable data length: the reception is actuated only if length (A) $\leqslant$ length (E).

Before command execution WRITE INDIRECT:

	calling station call field	slave station receive field
0	call / ready	receive / ready
1	next	next
2	address	---
3	WRITE INDIR. VAR.	---
4	length (A)	length (E)
5	data*	---
6	external call address 0	external receive address 0
7	external call address 'f'	external receive address 0

* The byte "data" in position 5 is an available single data byte.

4.6.3 Write indirect without termination

If a reply message is received with error, the call WRITE INDIRECT can cause multiple transmissions of the same data with the retry (retries) of the calling station. These calls will occupy consequent receiving fields in the slave and all are terminated with the status "done". If this situation is inadmissible, the call WRITE INDIRECT WITHOUT TERMINATION can be used. With this, the receiving command is not terminated immediately after the reception and, in the case of unwanted retries, the data is overwritten in the same data area.

The receive command field is marked "done" only after an explicit read status call from the master station.

The call WRITE INDIRECT WITHOUT TERMINATION is not allowed in subtraffic. This is because a status read call should never be executed by a slave and such a call will not be accepted by the DLC.

4.6.3 (continued)

Example

Call WRITE INDIRECT WITHOUT TERMINATION. In this example, four data bytes have been placed in bytes 4 to 7 of the receive command field but the command field has not been terminated with status "done". After the reply, the function code of the reply message is placed in position 3 of the call field. The current write call must be terminated by a read status call before the next write command can be executed.

Before command execution WRITE INDIRECT WITHOUT TERMINATION:

	calling station call field		slave station receive field	
0	call	ready	receive	ready
1	next		next	
2	address		———	
3	WRITE IND. 4 WT		———	
4	data 1		length (E)	
5	data 2		———	
6	data 3		external receive address 0	
7	data 4		external receive address 0	

After command execution:

	calling station call field		slave station receive field	
0	call	done	receive	done
1	next		next	
2	address		address	
3	function		WRITE IND. 4 WT	
4	data 1		data 1	
5	data 2		data 2	
6	data 3		data 3	
7	data 4		data 4	

Before command execution STATUS:

	calling station call field		slave station receive field	
0	call	ready	receive	ready
1	next		next	
2	address		address	
3	STAT		WRITE IND. 4 WT	
4	———		data 1	
5	———		data 2	
6	———		data 3	
7	———		data 4	

After command execution:

	calling station call field		slave station receive field	
0	call	done	receive	done
1	next		next	
2	address		address	
3	function		WRITE IND. 4 WT	
4	———		data 1	
5	———		data 2	
6	———		data 3	
7	———		data 4	

DEVELOPMENT DATA

4.7 Read

Read calls cause data to be transferred from a slave station to a calling station. Two types of read call exist:

- READ DIRECT, fixed data format and without use of command field memory;
- READ INDIRECT, several data formats.

4.7.1 Read direct

The call READ DIRECT permits reading of two bytes from a given 16-bit location in an external slave memory. Before execution of the call, the command field contains the address of the selected slave, the function code READ DIRECT and the DMA address (secondary address). After execution, the command field contains the reply function code and the two data bytes. If errors occur, the call is retried NMAX times. When a successful transfer is made the call field is marked "done"; if there is no successful transfer it is marked "error".

Example

Call READ DIRECT.

Calling station call field:

	Before command execution		After command execution: no error		After command execution: error	
0	call	ready	call	done	call	error
1	next		next		next	
2	address		address		address	
3	READ DIRECT		function		READ DIRECT	
4	sec. address 0		data 1		sec. address 0	
5	sec. address 1		data 2		sec. address 1	
6	---		---		---	
7	---		---		---	

4.7.2 Read indirect

The call READ INDIRECT causes a data read via a prepared reply command in the slave. The reply command field of the addressed station contains information about the data format in its function byte (see 4.8). Data formats can comprise 2, 4 or a variable number of bytes.

If the data length is 2 or 4 bytes, data is fetched from the reply command field, i.e. station address is sent and the bytes 3 to 5 (including two data bytes) or bytes 3 to 7 (including four data bytes) are transferred.

With a variable data length transfer the call command field includes a DMA address and the maximum length (E) of the data in the external memory of the slave. The slave station address, bytes 3 to 5 of the reply command field and the data from the external memory are sent via DMA.

The function byte in the reply field is automatically completed with status information before transmission. In the examples, the completed byte is called "function A".

After reception, the actual data length (A) is compared with the expected data length (E). If (A) > (E) the call field is marked "error".

The call is retried NMAX times if there is an error in reception. The slave knows from the function code of the retry message that the transfer is a retry; it does not terminate the reply field but again delivers the same data. The reply command field is not marked "done" until a new message is received which is not a retry.

After a correctly received reply, the call field is marked "done". If no error-free reply can be obtained after NMAX retries, the call field is marked "error".

The call READ INDIRECT is not allowed in subtraffic, and is rejected by the DLC. This is to avoid another station 'stealing' data intended for the master.

Example

Call READ INDIRECT in which the slave has two bytes ready.

Before command execution READ INDIRECT:

	calling station call field		slave station reply field	
0	call	ready	reply	ready
1	next		next	
2	address		---	
3	READ INDIRECT		function (2)*	
4	length (E)		data 1	
5	---		data 2	
6	ext. rec. addr. 0		---	
7	ext. rec. addr. 1		---	

* Function (2): function code indicates a 2-byte data length (see 4.8.1).

After command execution:

	calling station call field		slave station reply field	
0	call	done	reply	ready
1	next		next	
2	address		———	
3	function A (2)		function (2)	
4	data 1		data 1	
5	data 2		data 2	
6	ext. rec. addr. 0		———	
7	ext. rec. addr. 1		———	

After command execution:

	calling station call field		slave station reply field	
0	call	done	reply	ready
1	next		next	
2	address		———	
3	function A (V)		function (V)	
4	length (A)		length (A)	
5	———		data	
6	ext. rec. addr. 0		ext. rep. addr. 0	
7	ext. rec. addr. 1		ext. rep. addr. 1	

After reception of another call that is not a retry message:

	slave station reply field	
0	reply	done
1	next	
2	———	
3	function (2)	
4	data 1	
5	data 2	
6	———	
7	———	

Example

Call READ INDIRECT in which the slave has variable data length.

Before command execution READ INDIRECT:

	calling station call field		slave station reply field	
0	call	ready	reply	ready
1	next		next	
2	address		———	
3	READ INDIRECT		function (V)*	
4	length (E)		length (A)	
5	———		data	
6	ext. rec. addr. 0		ext. rep. addr. 0	
7	ext. rec. addr. 1		ext. rep. addr. 1	

* Function (V): function code indicates variable length (see 4.8.1).

4.8 Function code field

4.8.1 Function codes in call messages

The function code characterizes the type of message in the transmission channel as shown in Tables 4.1 and 4.2.

Function bits:	7	6	5	4	3	2	1	0

Call messages are denoted by Bit 0 = 1. If a call is transmitted with Bit 0 = 0, it is treated as a WRITE INDIRECT and no reply message is sent.

Bits 1 and 2 indicate the length of data:

bit 2	bit 1	indication
0	0	no data*
0	1	2 bytes
1	0	4 bytes
1	1	variable; length given in next field

* With Bit 1 = Bit 2 = 0, no function codes with odd values are allowed in subtraffic.

DEVELOPMENT DATA

Table 4.1 Bus command mnemonics, codes and functions used in call messages

bus command mnemonic	function bits 7 6 5 4 3 2 1 0	hex code	function
NORM	0 0 0 0 0 0 0 1	0 1	normalize
STAT	0 0 0 1 0 0 0 1	1 1	status read
STST	0 0 1 0 0 0 0 1	2 1	start subtraffic
STQP	1 0 0 0 0 0 0 1	8 1	start quick poll
PCT	1 0 0 1 0 0 0 1	9 1	pass control
WD	0 0 1 0 1 1 0 1	2 D	write direct
WI 0	0 1 1 0 1 0 0 1	6 9	write indirect; length = 0
WI 2	0 1 1 0 1 0 1 1	6 B	write indirect; length = 2 bytes
WI 4	0 1 1 0 1 1 0 1	6 D	write indirect; length = 4 bytes
WI V	0 1 1 0 1 1 1 1	6 F	write indirect; length variable
WI 0 WT	1 1 0 0 0 0 0 1	C 1	write indirect without termination; length = 0
WI 2 WT	1 1 0 0 0 0 1 1	C 3	write indirect without termination; length = 2 bytes
WI 4 WT	1 1 0 0 0 1 0 1	C 5	write indirect without termination; length = 4 bytes
WI V WT	1 1 0 0 0 1 1 1	C 7	write indirect without termination; length variable
RD	0 1 0 0 1 0 1 1	4 B	read direct
RI	1 0 0 0 1 0 0 1	8 9	read indirect
RI R	1 0 0 1 1 0 0 1	9 9	read indirect, retry message. Used only by the DLC in retry messages following a READ INDIRECT call

Table 4.2 Function codes in call messages

bit 0	1	1	1	1	1	1	1	1
bits 1 2	0 0	0 1	1 0	1 1	0 0	0 1	1 0	1 1
bit 3	0	0	0	0	1	1	1	1

bits 7 6 5 4								
0 0 0 0	NORM	WI 2	WI 4	WI V	WI 0	WI 2	WI 4	WI V
0 0 0 1	STAT	WI 2	WI 4	WI V	WI 0	WI 2	WI 4	WI V
0 0 1 0	STST	WI 2	WI 4	WI V	WI 0	WI 2	WD	WI V
0 0 1 1	WI 0	WI 2	WI 4	WI V	WI 0	WI 2	WD	WI V
0 1 0 0	WI 0	WI 2	WI 4	WI V	WI 0	RD	WI 4	WI V
0 1 0 1	WI 0	WI 2	WI 4	WI V	WI 0	RD	WI 4	WI V
0 1 1 0	WI 0	WI 2	WI 4	WI V	WI 0	WI 2	WI 4	WI V
0 1 1 1	WI 0	WI 2	WI 4	WI V	WI 0	WI 2	WI 4	WI V
1 0 0 0	STQP	WI 2	WI 4	WI V	RI	WI 2	WI 4	WI V
1 0 0 1	PCT	WI 2	wi 4	WI V	(RI R)	WI 2	WI 4	WI V
1 0 1 0	WI 0	WI 2	WI 4	WI V	RI	WI 2	WI 4	WI V
1 0 1 1	WI 0	WI 2	WI 4	WI V	(RI R)	WI 2	WI 4	WI V
1 1 0 0	WI 0 WT	WI 2 WT	WI 4 WT	WI V WT	RI	WI 2 WT	WI 4 WT	WI V WT
1 1 0 1	WI 0 WT	WI 2 WT	WI 4 WT	WI V WT	(RI R)	WI 2 WT	WI 4 WT	WI V WT
1 1 1 0	WI 0 WT	WI 2 WT	WI 4 WT	WI V WT	RI	WI 2 WT	WI 4 WT	WI V WT
1 1 1 1	WI 0 WT	WI 2 WT	WI 4 WT	WI V WT	(RI R)	WI 2 WT	WI 4 WT	WI V WT

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4.8.2 Function codes in reply messages

As explained in section 3, certain calls are automatically answered by the DLC. The meanings of the function byte in these reply messages are given below. The coding shown must be used if reply messages are prepared by the user and put in the reply command fields.

Function bits:	7	6	5	4	3	2	1	0

Bit 0 is always zero in reply messages.

Bits 1 and 2 indicate the length of data:

bit 2	bit 1	indication
0	0	no data
0	1	2 bytes
1	0	4 bytes
1	1	variable; length given in next field

Bits 3 and 5 are zero when the reply function byte is generated by the DLC. In user-given function bytes, bits 3 and 5 are free for use.

Bit 4 = 0: command executed
Bit 4 = 1: command not executed

Bit 6 = 0: no subtraffic request
Bit 6 = 1: subtraffic request (a call command field is ready)

Bit 7 = 0: no reply field ready
Bit 7 = 1: reply field ready

The bits 6 and 7 are automatically set/reset by the DLC, according to the DLC status byte.

5. ERROR LIST

5.1 Call retry in the event of errors (master stations only)

If a CRC error occurs during the transmission of the fourth byte of a reply message, the DLC will overwrite bytes 4 to 7 of the Command Field. During 'Read Direct' and 'Read Indirect' operations, retry message data will be changing so the 'Call Retry in case of transmission errors' feature is not useful and the NMAX parameter of the Initialization Field must be zero.

5.2 Wrong access to Receive Fields (Slave, Listen, and Monitor Stations)

If a CRC error occurs during the transmission of the fourth byte of a message, the DLC will change bytes 4 to 7 of the Receive Field. Byte 0 of the Command Field is not affected and the status of the Receive Field is still 'ready'.

6. ELECTRICAL SPECIFICATIONS

6.1 Ratings

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C
Voltage range at any pin	V_I, V_O	−0.5	+ 7	V
Total power dissipation	P_{tot}	–	1.5	W

6.2 DC characteristics

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = 0 to + 70 °C.

parameter	conditions	symbol	min.	max.	unit
Power supply current		I_{DD}	–	150	mA
LOW level input voltage		V_{IL}	−0.5	0.8	V
HIGH level input voltage (except X1)		V_{IH}	2.0	V_{DD}	V
HIGH level input voltage (X1 only)		V_{IHO}	3.0	V_{DD}	V
LOW level output voltage (except X2)	I_{OL} = 1.6 mA	V_{OL}	–	0.4	V
HIGH level output voltage	I_{OH} = −20 μA	V_{OH}	2.4	–	V
Input leakage current ($\overline{RR}$, $\overline{RD}$, $\overline{RT}$, $\overline{ST}$, BGT, $\overline{RES}$, $\overline{SE}$)	V_{DD} = 5.5 V	I_{IL}	–	10	μA
Logic 0 input current (AD0 to AD7, $\overline{DTA}$, $\overline{DTR}$, R/$\overline{W}$, A/$\overline{D}$)	V_i = 0.4 V	I_{ILL}	–	−500	μA

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7. AC CHARACTERISTICS

7.1 Timing

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = 0 to + 70 °C. Load: 80 pF; 2.2 kΩ to V_{SS}, 4.3 kΩ to V_{DD}. f_{OSC} = 0.1 to 2.5 MHz.

parameter	symbol	min.	max.	f_{OSC} = 2.5 MHz min.	max.
DLC passive					
$1/f_{OSC}$	t_{OSC}	400 ns	10 µs	400 ns	–
R/$\overline{W}$ set-up to $\overline{DTR}$	T_{SRWN}	100 ns	–	100 ns	–
A/$\overline{D}$ set-up to $\overline{DTR}$	T_{SADN}	100 ns	–	100 ns	–
Address/data set-up to $\overline{DTR}$	T_{SAD}	100 ns	–	100 ns	–
R/$\overline{W}$ hold after $\overline{DTR}$	T_{HRWN}	0 ns	–	0 ns	
A/$\overline{D}$ hold after $\overline{DTR}$	T_{HADN}	0 ns	–	0 ns	–
Address/data hold after $\overline{DTR}$	T_{HAD}	0 ns	–	0 ns	–
$\overline{DTR}$ to $\overline{DTA}$ acknowledge pulse:	T_{ADTA}				
1. Write address		3 t_{OSC} + 100 ns	5 t_{OSC} + 200 ns	1.3 µs	2.2 µs
2. Read status		3 t_{OSC} + 100 ns	5 t_{OSC} + 200 ns	1.3 µs	2.2 µs
3. Write data		7 t_{OSC} + 100 ns	17 t_{OSC} + 200 ns	2.9 µs	7 µs
4. Read data		7 t_{OSC} + 100 ns	17 t_{OSC} + 200 ns	2.9 µs	7 µs
$\overline{DTA}$ to rising edge of $\overline{DTR}$ (1)	T_{RDTR}	–	$t_{OSC}/2$	–	200 ns
$\overline{DTA}$ pulse duration	T_{WDTA}	2 t_{OSC}	–	800 ns	–
Address/data valid to $\overline{DTA}$	T_{AAD}	–	2 t_{OSC} – 100 ns	–	700 ns
Address/data valid after $\overline{DTA}$	T_{IAD}	2 t_{OSC} + 100 ns	–	800 ns	–
$\overline{SRQ}$ to $\overline{DTA}$ acknowledge pulse	T_{ASRQ}	–	t_{OSC}	–	400 ns

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parameter	symbol	min.	max.	f_{OSC} = 2.5 MHz min.	f_{OSC} = 2.5 MHz max.
DLC active					
$1/f_{OSC}$	t_{OSC}	400 ns	10 µs	400 ns	10 µs
Address/data set-up to $\overline{DTA}$	T_{SAD}	100 ns	–	100 ns	–
$\overline{DTA}$ hold after $\overline{DTR}$	T_{HDTA}	0 ns	–	0 ns	–
Address/data hold after $\overline{DTA}$	T_{HAD}	0 ns	–	0 ns	–
BRQ to rising edge of BGT (1)	T_{RBGT}	–	$t_{OSC}/2$	–	200 ns
$\overline{DTR}$ to falling edge of $\overline{DTA}$ (1)	T_{RBGT}	–	$t_{OSC}/2$	–	200 ns
BRQ to A/$\overline{D}$ valid	T_{AADN}	–	3 t_{OSC}	–	1.2 µs
BRQ to R/$\overline{W}$ valid	T_{ARWN}	–	3 t_{OSC}	–	1.2 µs
BRQ to D0 valid	T_{AD0}	–	3 t_{OSC}	–	1.2 µs
$\overline{DTR}$ to D1 valid	T_{AD1}	–	4 t_{OSC}	–	1.6 µs
BRQ to first $\overline{DTR}$ pulse	T_{ADTR0}	–	5 t_{OSC} – 100 ns	–	1.9 µs
DTR0 to second $\overline{DTR}$ pulse	T_{ADTR1}	–	6 t_{OSC}	–	2.4 µs
$\overline{DTR}$ pulse duration	T_{WDTR}	2 t_{OSC}	–	800 ns	–
A/$\overline{D}$ valid after second $\overline{DTR}$	T_{IADN}	2 t_{OSC}	–	800 ns	–
R/W valid after second $\overline{DTR}$	T_{IRWN}	2 t_{OSC}	–	800 ns	–
D1 valid after second $\overline{DTR}$	T_{ID1}	2 t_{OSC}	–	800 ns	–
BRQ high after second $\overline{DTR}$	T_{IBRQ}	3 t_{OSC}	–	1.2 µs	–

Note to the timing characteristics

1. If the $T_{R__}$ parameters exceed the specified limits, then the corresponding $T_{A__}$, $T_{W__}$, and $T_{W__}$ parameters will increase by 2 t_{OSC}.

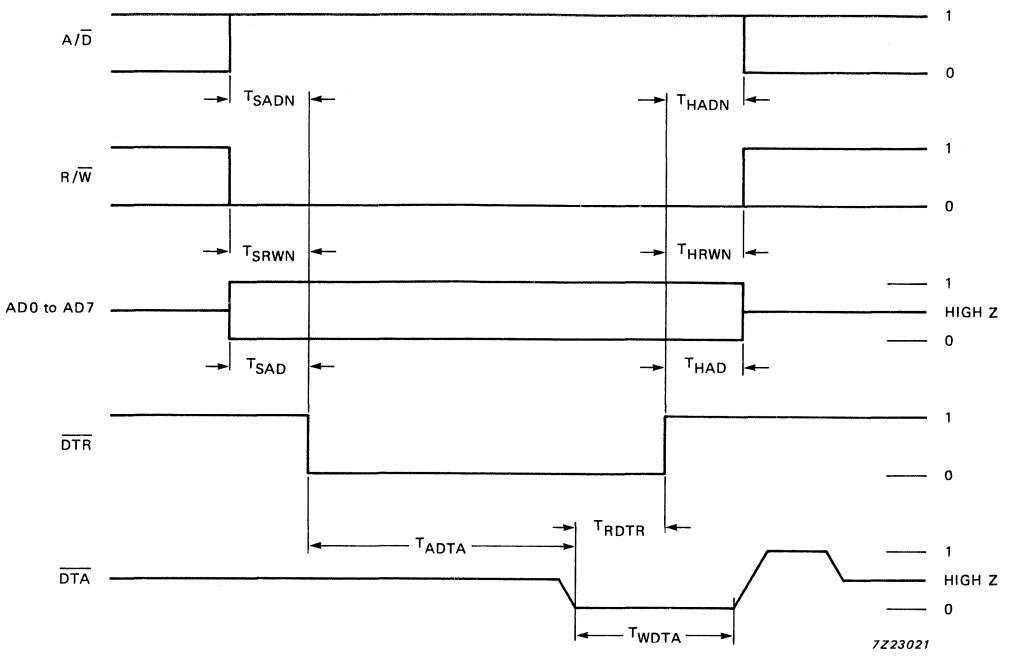


Fig. 7.1 Write address into DLC.

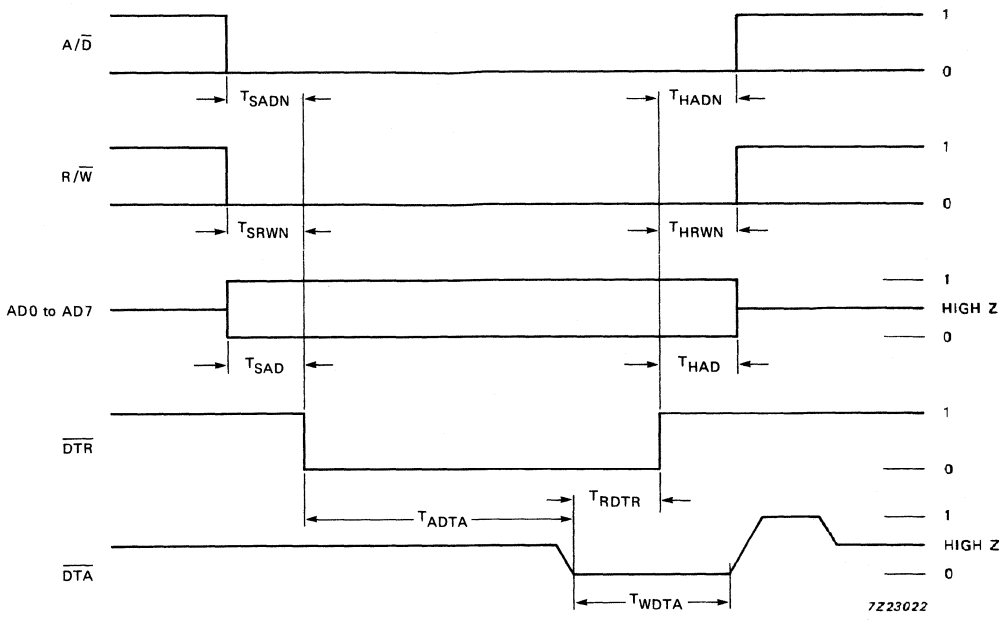


Fig. 7.2 Write data into DLC; the waiting time of about 4 TKM cycles is due to competing access to the command memory.

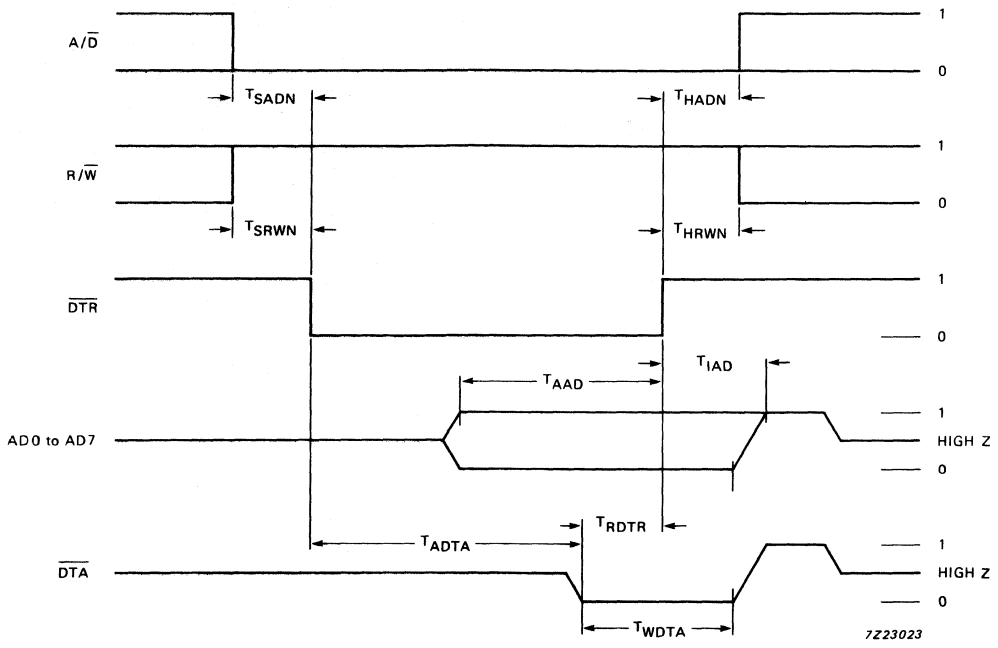


Fig. 7.3 Read data from DLC; the waiting time of about 4 TKM cycles is due to competing access to the command memory.

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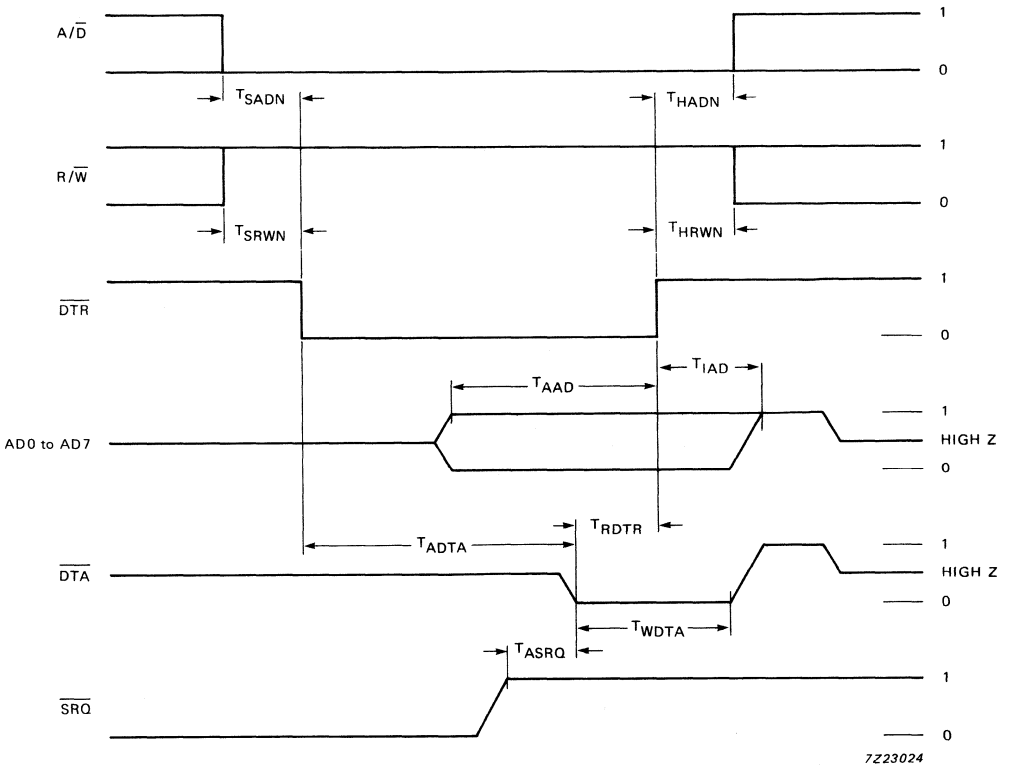


Fig. 7.4 Read status timing.

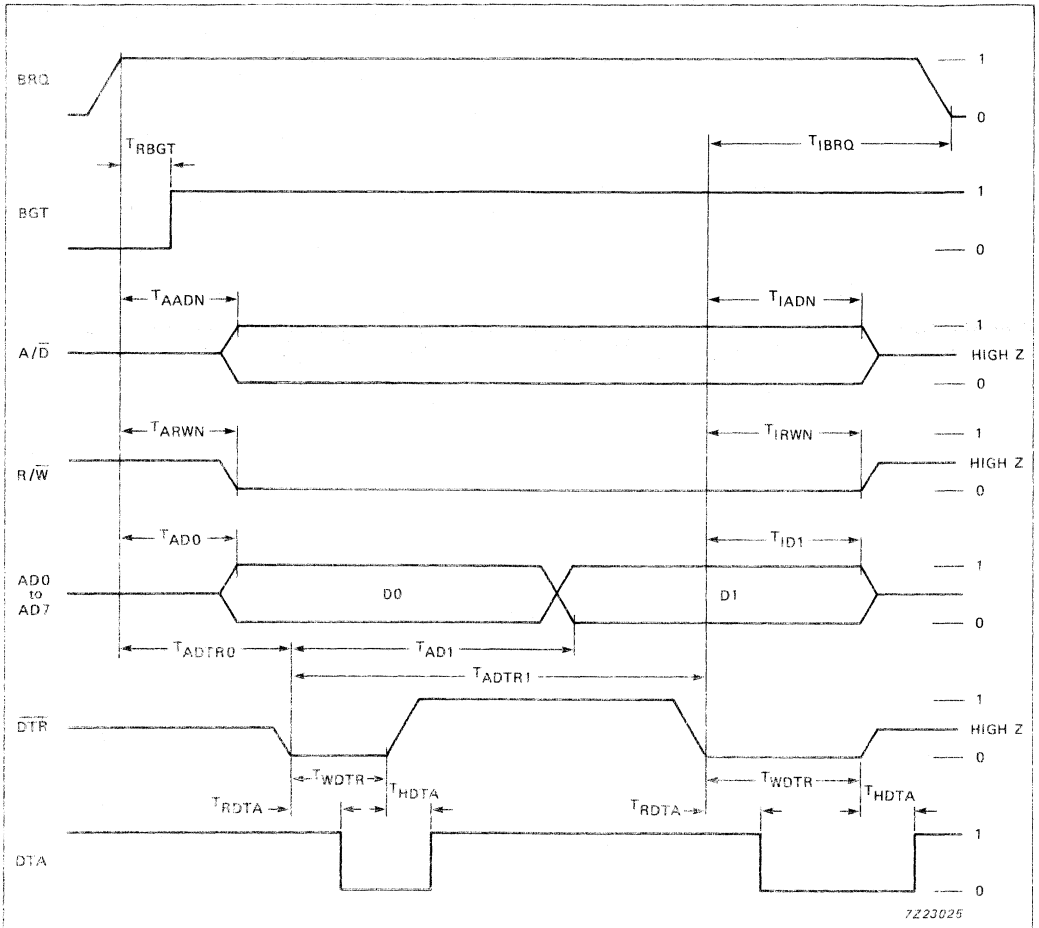


Fig. 7.5 Write data to external RAM; DLC active.

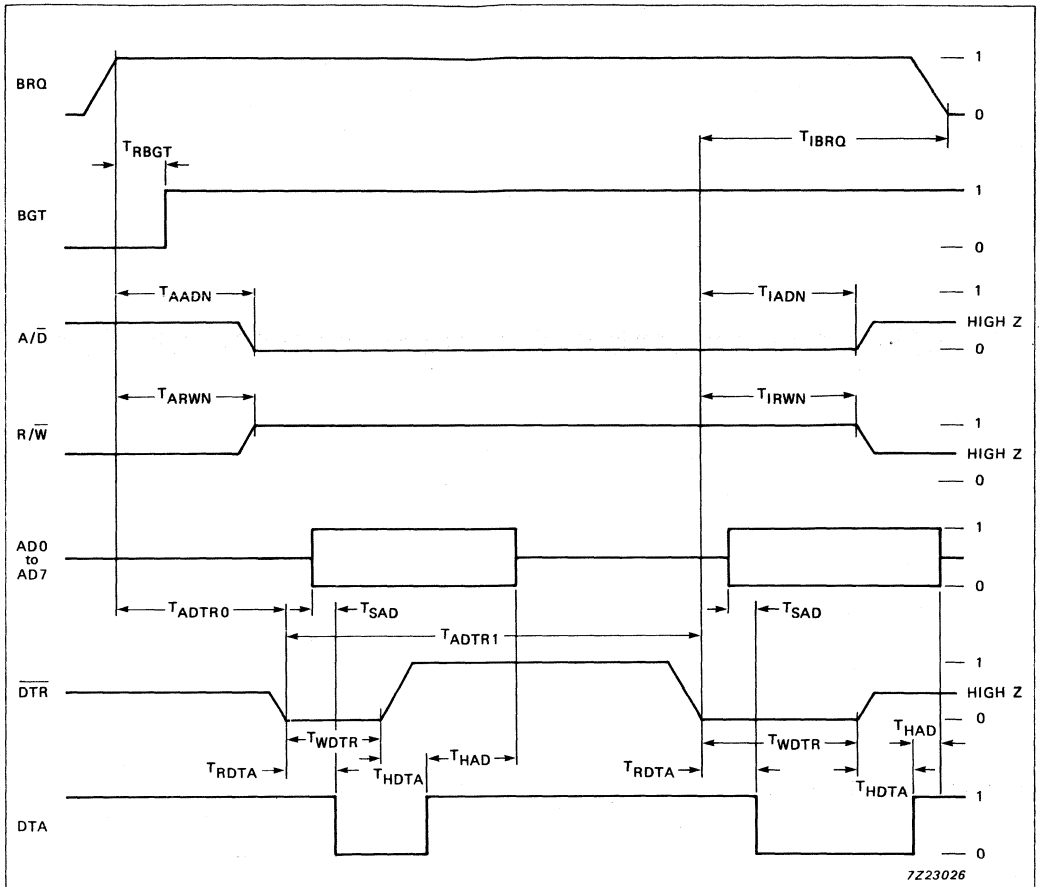
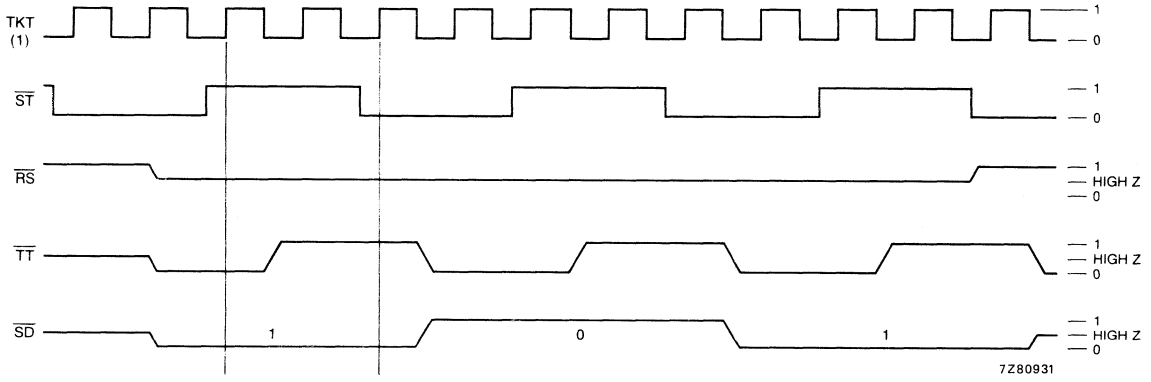


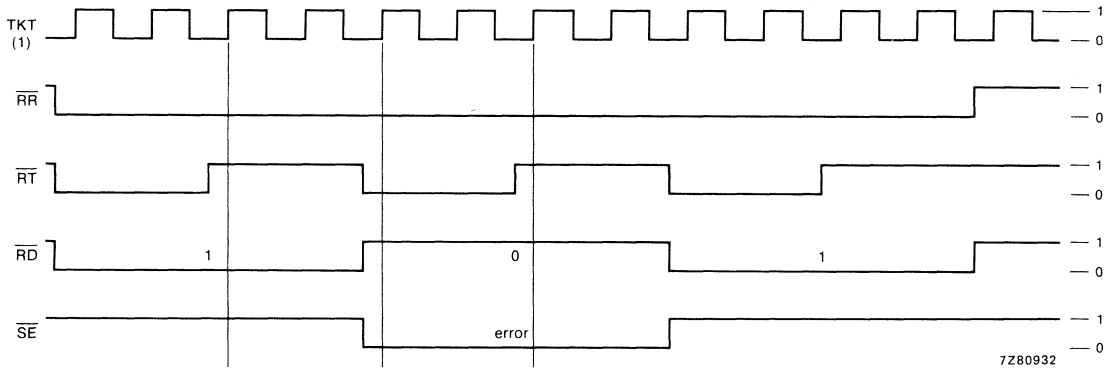
Fig. 7.6 Read data from external RAM; DLC active.

7.2 Data transfer via the message unit



(1) The waveform TKT is an internal clock generated in the message unit (MU) stage and is not available externally.

Fig. 7.7 Sending NRZ-coded data; serial data interface.



(1) The waveform TKT is an internal clock generated in the message unit (MU) stage and is not available externally.

Fig. 7.8 Receiving NRZ-coded data; serial data interface.

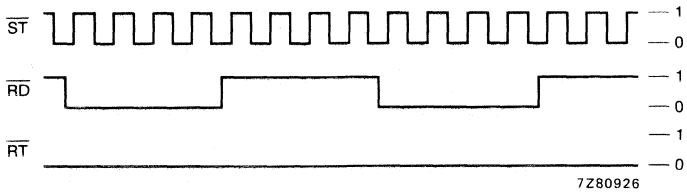


Fig. 7.9 Receiving Manchester-coded data; line interface with one active line.

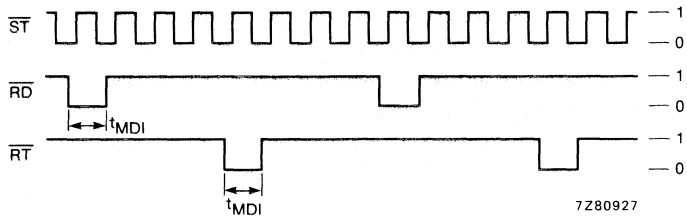


Fig. 7.10 Receiving Manchester-coded data; line interface with two active lines.

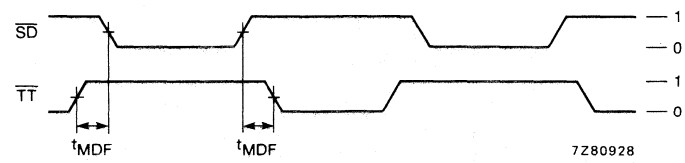


Fig. 7.11 Sending Manchester-coded data; line interface.

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7.3 Data transmission example

Command field in the master station:

0	call	ready
1	next	
2	address	
3	write ind., var.	
4	length (A)	
5	----	
6	ext. call addr. 0	
7	ext. call addr. 1	

The DLC sequence starts with a bus request. When the parallel bus is requested, BRQ goes HIGH a short time after status "ready" has been set.

In the examples shown in Fig. 7.12, the oscillator frequency (X1) = 2 MHz and the send frequency ($\overline{ST}$ or $\overline{TT}$) = 250 kHz. (The time taken for a two-byte transfer will increase with a decrease in $\overline{ST}$ frequency.)

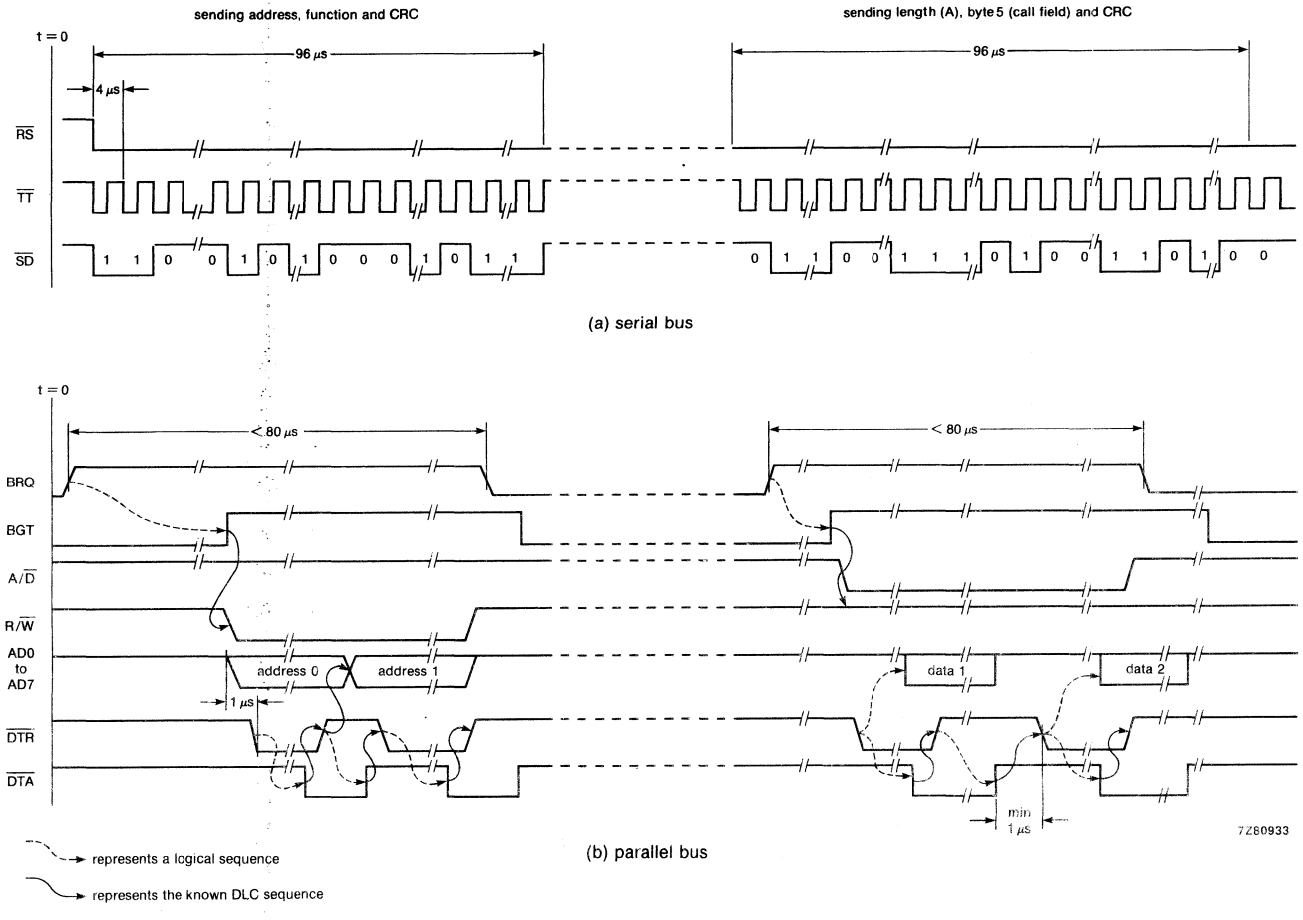


Fig. 7.12 Examples of serial bus and parallel bus data transfer: oscillator frequency = 2 MHz; send frequency = 250 kHz; at t = 0 "ready" has been set.

7.4 Oscillator circuit

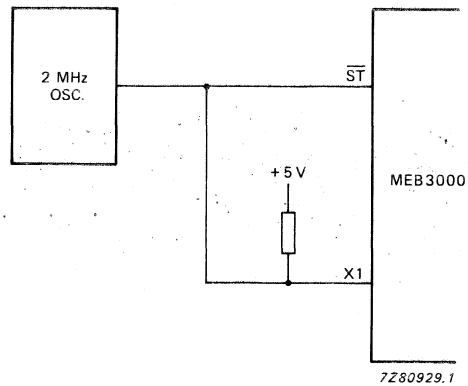
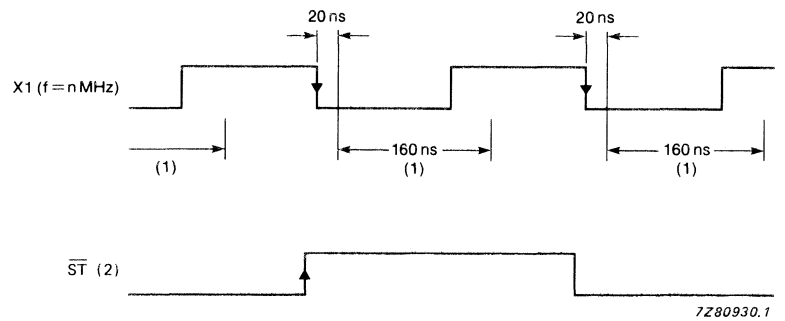


Fig. 7.13 Example of oscillator circuit using a 2 MHz crystal oscillator: the delay time of the delay element equals the rated delay of the toggle flip-flop; X2 (pin 11) is not connected.



(1) Positive-going edges of $\overline{ST}$ are not allowed during these periods.
(2) f = n/a MHz; a = 1, 2, 4, 8, – – – – – –

Fig. 7.14 Waveforms showing the relationship between clock X1 and send timing $\overline{ST}$.

7.5 Distance between messages

The spacing of messages is a function of clock X1 and send timing $\overline{ST}$. An allowance has to be made due to uncertainties of one $\overline{ST}$ period for the serial digital interface and of eight $\overline{ST}$ periods for the line interface.

The following equations can be used to calculate worst-case examples of the time allowances required (typical values will be less). In the equations:

t = 1 X1 period;

T = 1 $\overline{ST}$ period for SDI or 8 $\overline{ST}$ periods for LI.

Time for initialization of $\overline{RES}$ rising edge to SRQ falling edge:

$t_I = 172t$.

Calling time (master station) from "message ready" to "start message":

$t_A = 34t + T$.

Time for reaction of slave station from the end of calling message to the end of reply message:

minimum time for write direct = $t_{u\ dir(min)} = 60\ t + T$;

maximum time for write indirect = $t_{u\ ind(max)} = 164t + T$.

Time for reaction of master station from the end of reply message to the beginning of a new call message:

minimum time during quick poll = $t_{LQP(min)} = 106t + T$;

maximum time during normal calling sequence = $t_{Lnorm(max)} = 196t + T$.

7.6 Illegal operation

The following situations are regarded as illegal operations as they result in the station entering the TEST mode and exit from this can only be made by a RESET:

the input combination A/$\overline{D}$ = HIGH, R/$\overline{W}$ = HIGH and $\overline{DTR}$ = LOW; and

the global self-initialization address "FFH".

8. APPLICATION NOTES

8.1 Parallel interface

The bidirectional I/O pins (AD0 to AD7, A/$\overline{D}$, R/$\overline{W}$, $\overline{DTR}$ and $\overline{DTA}$) have internal pull-ups which can source up to 20 μA (I_{OH} = 20 μA). For additional current, external pull-ups should be used (R = 4.3 kΩ).

8.2 Reception hinders transmission

Noise on the serial input of a master station can result in the rejection of the Initialization Field. A hardware reset is required to re-initialize a master station. A bus coupler should be used to avoid this problem.

8.3 Timeout parameters

The following values are possible:

TAB: $15 > TAB > 3$

TAN: $255 > TAN > 4$

TLN: $2*16 > TLN > 4*(3/8*DMAX + 2)$

TQV: $255 > TQV > (3/8*DMAX + 2)*(1 + NMAX) + 4$

Note: the complete subtraffic sequence of the slave stations (call, reply, and call retry in case of errors) has to be completed within TQV – Time; otherwise the master station terminates the Initialization Field with 'reception hinders transmission' (because the slaves are still transmitting).

DEVELOPMENT DATA

9. LIST OF ABBREVIATIONS

A/D	analogue-to-digital
A/$\overline{D}$	address/$\overline{data}$ select
BGT	bus grant
BOP	byte-oriented processor
BRQ	bus request
CRC	cyclic redundancy check
D/A	digital-to-analogue
DIL	dual-in-line
DLC	data link controller
DMA	direct memory access
DTA	data transfer acknowledge
DTR	data transfer request
ERR	error
ext. rec. addr.	external receive address
ext. rep. addr.	external reply address
ind.	indirect
I/O	input/output
LI	line interface
MAC	memory access control
MED	Manchester encoder/decoder
MU	message unit
NMOS	n-channel metal oxide semiconductor
NMAX	maximum number
NORM	normalize
NRZ	non-return to zero
PDV-bus	process-control data bus
PCT	pass control
R	retry
RAM	random access memory
RD	receive data
REP	reply
RD	read direct
RI	read indirect
RR	receive ready
RS	ready to send
RT	receive timing
SD	send data
SDI	serial digital interface
SE	signal error
sec.	secondary
SRQ	service request
ST	send timing
STAT	status read
STQP	start quick poll
STST	start subtraffic
TAB	maximum call/reply time (quick poll and status read)
TAN	maximum call/reply time (normal cycle)
TLN	call-to-response time limit
TST	subtraffic time limit
TT	terminal timing
var.	variable length
VLSI	very-large-scale integration
WAT	write attempt
WD	write direct
WI	write indirect
WT	without termination

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Substrate Design Guidelines for Surface-Mounted Devices

INTRODUCTION

SMD technology embodies a totally new automated circuit assembly process using a new generation of electronic components: surface-mounted devices (SMDs). Smaller than conventional components, SMDs are placed onto the surface of the substrate, not through it like leaded components. And from this, the fundamental difference between SMD assembly and conventional through-hole component assembly arises; SMD component positioning is relative, not absolute.

When a through-hole (leaded) component is inserted into a PCB, either the leads go through the holes, or they don't. An SMD, however, is placed onto the substrate surface, its position only relative to the solder-lands, and placement accuracy is therefore influenced by variations in the substrate track pattern, component size, and placement machine accuracy.

Other factors influence the layout of SMD substrates. For example, will the board be a mixed-print (a combination of through-hole components and SMDs) or an all-SMD design? Will SMDs be on one side of the substrate or both? And there are process considerations, such as: what type of machine will place the components and how will they be soldered?

Using our expertise in the world of SMD technology, this section draws upon applied research in the area of substrate design and manufacture, and presents the basic guidelines to assist the designer in making the transition from conventional through-hole PCB assembly to SMD substrate manufacture.

Designing With SMD

SMD technology is penetrating rapidly into all areas of modern electronic equipment manufacture — in professional, industrial, and consumer applications. Boards are made with conventional print-and-etch PCBs, multilayer boards with thick film ceramic substrates, and with a host of new materials specially developed for SMD assembly.

However, before substrate layout can be attempted, footprints for all components must be defined. Such a footprint will include the combination of patterns for the copper solder-lands, the solder resist, and, possibly, the solder paste. So the design of a substrate breaks down into two distinct areas: the SMD footprint definition, and the layout and track routing for SMDs on the substrate.

Each of these areas is treated individually; first, the general aspects of SMD technology, including substrate configurations, placement machines, and soldering techniques, are discussed.

Substrate Configurations

SMD substrate assembly configurations are classified as:

Type I — Total surface mount (all-SMD); substrates with no through-hole components at all. SMDs of all types (SM integrated circuits, discrete semiconductors, and passive devices) can be mounted either on one side, or both sides, of the substrate. See Figure 1a.

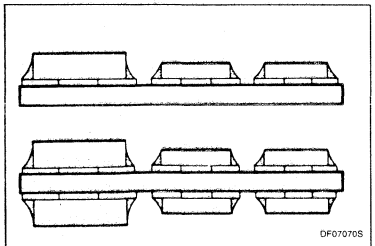
Type IIA — Double-sided mixed-print; substrates with both through-hole components and SMDs of all types on the top, and smaller SMDs (transistors and passives) on the bottom. See Figure 1b.

Type IIB — Underside attachment mixed-print; the top of the substrate is dedicated exclusively to through-hole components, with smaller SMDs (transistor and passives) on the bottom. See Figure 1c.

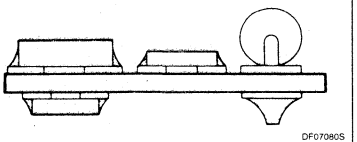
Although the all-SMD substrate will ultimately be the cheapest and smallest variation as there are no through-hole components, it's the mixed-print substrate that many manufacturers will be looking to in the immediate future, for this technique enjoys most of the advantages of SMD assembly and overcomes the problem of non-availability of some components in surface-mounted form.

The underside attachment variation of the mixed-print (type IIB — which can be thought of as a conventional through-hole assembly with SMDs on the solder side) has the added advantages of only requiring a single-sided, print-and-etch PCB and of using the established wave soldering technique. The all-SMD and mixed-print assembly with SMDs on both sides require reflow or combination wave/reflow soldering, and, in most cases, a double-sided or multilayer substrate.

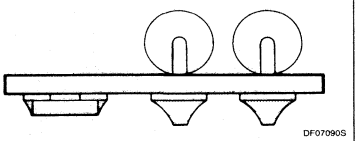
The relatively small size of most SMD assemblies compared with equivalent through-hole designs means that circuits can often be repeated several times on a single substrate. This multiple-circuit substrate technique (shown in Figure 2) further increases production efficiency.



a. Type I — Total Surface-Mount (all-SMD) Substrates



b. Type IIA — Mixed-Print (Double-Sided) Substrate



c. Type IIB — Mixed-Print (Underside Attachment) Substrate

Figure 1

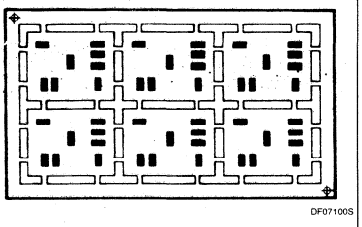


Figure 2. Multiple-Circuit Substrate

Mixed Prints

The possibility of using a partitioned design should be investigated when considering the mixed-print substrate option. For this, part of the circuit would be an all-SMD substrate, and the remainder a conventional through-hole

PCB or mixed-print substrate. This allows the circuit to be broken down into, for example, high and low power sections, or high and low frequency sections.

Automated SMD Placement Machines

The selection of automated SMD placement machines for manufacturing requirements is an issue reaching far beyond the scope of this section. However, as a guide, the four main placement techniques are outlined. They are:

In-Line Placement — a system with a series of dedicated pick-and-place units, each placing a single SMD in a preset position on the substrate. Generally used for small circuits with few components. See Figure 3a.

Sequential Placement — a single pick-and-place unit sequentially places SMDs onto the substrate. The substrate is positioned below the pick-and-place unit using a computer-controlled X-Y moving table (a "software programmable" machine). See Figure 3b.

Simultaneous Placement — places all SMDs in a single operation. A placement module (or station), with a number of pick-and-place units, takes an array of SMDs from the packaging medium and simultaneously places them on the substrate. The pick and place units are guided to their substrate location by a program plate (a "hardware programmable" machine), or by software-controlled X-Y movement of substrate and/or pick-and-place units. See Figure 3c.

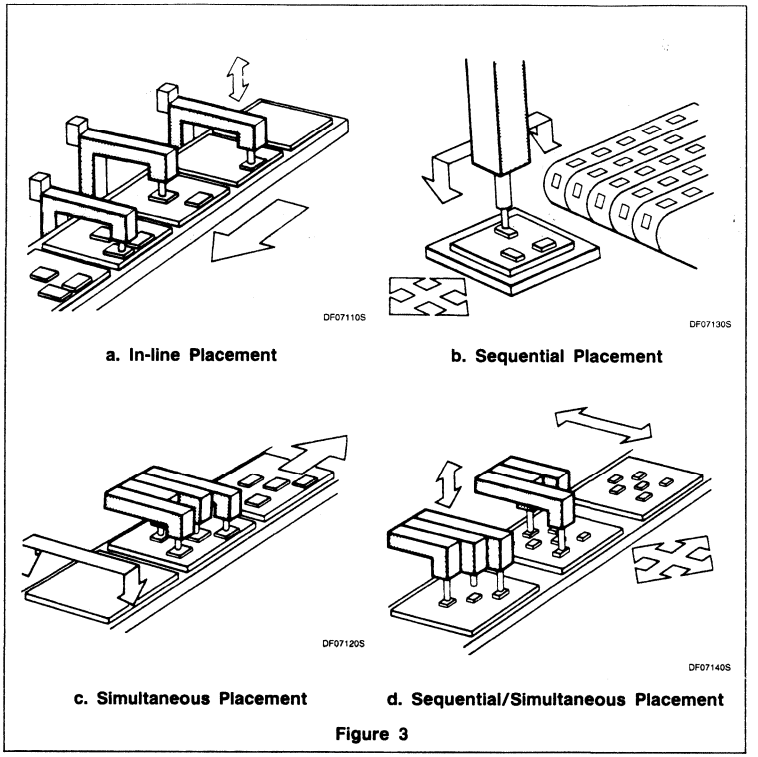
Sequential/Simultaneous Placement — a complete array of SMDs is transferred in a single operation, but the pick-and-place units within each placement module can place all devices simultaneously, or individually (sequentially). Positioning of the SMDs is software-controlled by moving the substrate on an X-Y moving table, by X-Y movement of the pick-and-place units, or by a combination of both. See Figure 3d.

All four techniques, although differing in detail, use the same two basic steps: picking the SMD from the packaging medium (tape, magazine, or hopper) and placing it on the substrate. In all cases, the exact location of each SMD must be programmed into the automated placement machine.

Soldering Techniques

The SMD-populated substrate is soldered by conventional wave soldering, reflow soldering, or a combination of both wave and reflow soldering. These techniques are covered at length in another publication entitled *SMD Soldering Techniques*, but, briefly, they can be described as follows:

Wave Soldering — the conventional method of soldering through-hole component assemblies where the substrate passes over a wave (or more often, two waves) of molten solder. This technique is favored for mixed-print assemblies with through-hole components on the top of the substrate, and SMDs on the bottom.



a. In-line Placement

b. Sequential Placement

c. Simultaneous Placement

d. Sequential/Simultaneous Placement

Figure 3

Reflow Soldering — a technique originally developed for thick-film hybrid circuits using a solder paste or cream (a suspension of fine solder particles in a sticky resin-flux base) applied to the substrate which, after component placement, is heated and causes the solder to melt and coalesce. This method is predominantly used for Type I (all-SMD) assemblies.

Combination Wave/Reflow Soldering — a sequential process using both the foregoing techniques to overcome the problems of soldering a double-sided mixed-print substrate with SMDs and through-hole components on the top, and SMDs only on the bottom. (Type IIB).

Footprint Definition

An SMD footprint, as shown in Figure 4, consists of:

- A pattern for the (copper) solderlands
- A pattern for the solder resist
- If applicable, a pattern for the solder cream.

The design for the footprint can be represented as a set of nominal coordinates and dimensions. In practice, the actual coordinates of each pattern will be distributed around these nominal values due to positioning and processing tolerances. Therefore, the coordinates are stochastic; the actual values form a probability distribution, with a mean value (the nominal value) and a standard deviation.

The coordinates of the SMD are also stochastic. This is due to the tolerances of the actual component dimensions and the positional errors of the automated placement machine.

The relative positions of solderland, solder resist pattern, and SMD, are not arbitrary. A number of requirements may be formulated concerning clearances and overlaps. These include:

- Limiting factors in the production of the patterns (for example, the spacing between solderlands or tracks has a minimum value)

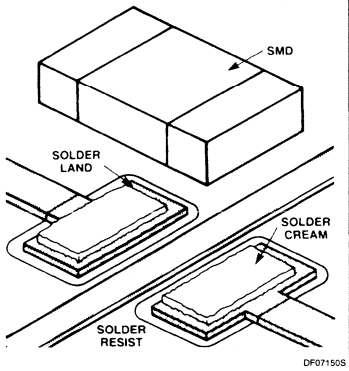


Figure 4. Component Lead, Solder Land, Solder Resist, and Solder Cream "Footprint"

- Requirements concerning the soldering process (for example, the solderlands must be free of solder resist)
- Requirements concerning the quality of the solder joint (for example, the solderland must protrude from the SMD metallization to allow an appropriate solder meniscus)

Mathematical elaboration of these requirements and substitution of values for all tolerances and other parameters lead to a set of inequalities that have to be solved simultaneously. To do this manually using worst-case design is not considered realistic. A better approach is to use a statistical analysis; although this requires a complex computer program, it can be done.

Such an approach may deliver more than one solution, and, if this is so, then the optimal solution must be determined. Optimization is achieved by setting the following objective — find the solution that:

- Minimizes the area occupied by the footprint
- Maximizes the number of tracks between adjacent solderlands.

The final SMD footprint design also depends on the soldering process to be used. The requirements for a wave-soldered substrate differ from those for a reflow-soldered substrate, so each is discussed individually.

Footprints for Wave Soldering

To determine the footprint of an SMD for a wave-soldered substrate, consider four main interactive factors:

- The component dimensions plus tolerances — determined by the component manufacturer
- The substrate metallization — positional tolerance of the solderland with respect to a reference point on the substrate
- The solder resist — positional tolerance of the solder resist pattern with respect to the same reference point
- The placement tolerance — the ability of an automated placement machine to accurately position the SMD on the substrate.

The coordinates of patterns and SMDs have to meet a number of requirements. Some of these have a general validity (the minimum overlap of SMD metallization and solderland) and available space for solder meniscus. Others are specifically required to allow successful wave soldering. One has to take into account factors like the "shadow effect" (missing of joints due to high component bodies), the risk of solder bridging, and the available space for a dot of adhesive.

The "Shadow Effect"

In wave soldering, the way in which the substrate addresses the wave is important. Unlike wave soldering of conventional printed boards where there are no component bodies to restrict the wave's freedom to traverse across the whole surface, wave soldering of SMD substrates is inhibited by the presence of SMDs on the solder-side of the board. The solder is forced around and over the SMDs as shown in Figure 5a, and the surface tension of the molten solder prevents its reaching the far end of the component, resulting in a dry-joint downstream of the solder flow. This is known as the "shadow effect."

The shadow effect becomes critical with high component bodies. However, wetting of the solderlands during wave soldering can be improved by enlarging each land as shown in Figure 5b. The extended substrate metallization makes contact with the solder and allows it to flow back and around the component metallization to form the joint.

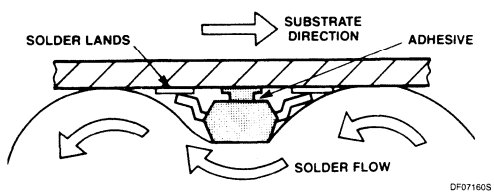
The use of the dual-wave soldering technique also partially alleviates this problem because the first, turbulent wave has sufficient upward pressure to force solder onto the component metallization, and the second, smooth wave "washes" the substrate to form good fillets of solder. Similarly, oil on the surface of the solder wave lowers the surface tension, (which lessens the shadow effect), but this technique introduces problems of contaminants in the solder when the oil decomposes.

Footprint Orientation

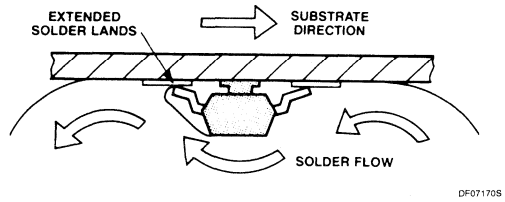
The orientation of SO (small outline) and VSO (very small outline) ICs is critical on wave-soldered substrates for the prevention of solder bridge formation. Optimum solder penetration is achieved when the central axis of the IC is parallel to the flow of solder as shown in Figure 6a. The SO package may also be transversely oriented, as shown in Figure 6b, but this is totally unacceptable for the VSO package.

Solder Thieves

Even with parallel mounted SO and VSO packages, solder bridges have a tendency to form on the leads downstream of the solder flow. The use of solder thieves (small squares of substrate metallization), shown in Figure 7 for a 40-pin VSO, further reduces the likelihood of solder-bridge formation.

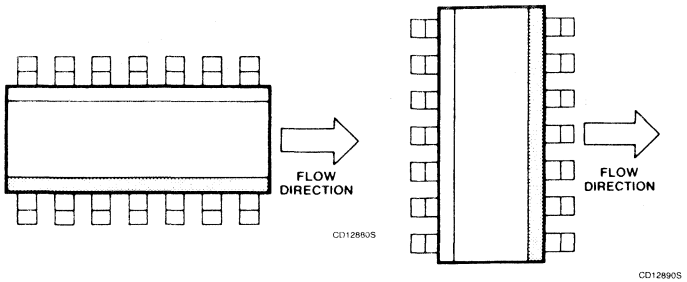


a. Surface Tension Can Prevent the Molten Solder From Reaching the Downstream End of the SMD, Known as the "Shadow Effect"



b. Extending the Solder Lands to Overcome the Shadow Effect

Figure 5



a. Parallel Orientation for SO and VSO Packages

b. Transverse Orientation for SO Packages Only

Figure 6

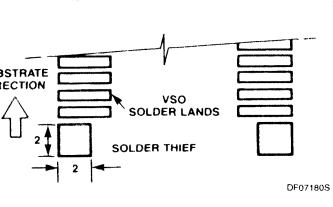


Figure 7. Example of Solder Thieves for VSO-40 Footprints (Dims in mm)

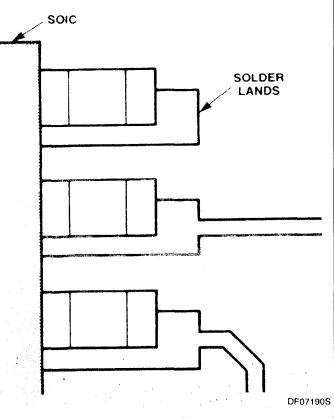


Figure 8. Misaligned Placement of SO Package Increases the Possibility of Solder Bridging

Placement Inaccuracy

Another major cause of solder bridges on SO ICs and plastic leaded chip carriers (PLCCs) is a slight misalignment as shown in Figure 8. The close spacing of the leads on these devices means that any inaccuracy in placement drastically reduces the space between adjacent pins and solderlands, thus increasing the chance of solder bridges forming.

Dummy Tracks for Adhesive Application

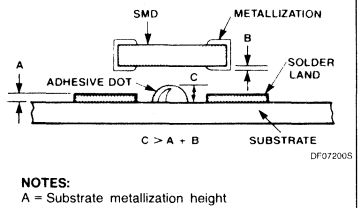
For wave soldering, an adhesive to affix components to the substrate is required. This is necessary to hold the SMDs in place between the placement operation and the soldering process (this technique is covered at length in another publication entitled *Adhesive Application and Curing*).

The amount of adhesive applied is critical for two reasons: first, the adhesive dot must be high enough to reach the SMD, and, second, there mustn't be too much adhesive which could foul the solderland and prevent the formation of a solder joint. The three parameters governing the height of the adhesive dot are shown in Figure 9. Although this diagram illustrates that the minimum requirement is $C > A + B$, in practice, $C > 2(A + B)$ is more realistic for the formation of a good strong bond.

Taking these parameters in turn, the substrate metallization height (A) can range from about 35μm for a normal print-and-etch PCB to 135μm for a plated through-hole board. And the component metallization height (B) (on 1206-size passive devices, for example) may differ by several tens of microns. Therefore, A + B can vary considerably, but it is desirable to keep the dot height (C) constant for any one substrate.

The solution to this apparent problem is to route a track under the device as shown in Figure 10. This will eliminate the substrate metallization height (A) from the adhesive dot-height criteria. Quite often, the high component density of SMD substrates necessitates the routing of tracks between solderlands, and, where it does not, a short dummy track should be introduced.

For bonding small outline (SO) ICs to the substrate, two dots of adhesive are sufficient for SO-8, -14, and -16 packages, but the SOL-20, -24, -28, and VSO-40 packages need three dots. The through-tracks (or dummy tracks) must be positioned beneath the IC accordingly to support the adhesive dots.



NOTES:
A = Substrate metallization height
B = SMD metallization height
C = Height of adhesive dot

Figure 9. Adhesive Dot Height Criteria

Footprints for Reflow Soldering

To determine the footprint of an SMD for a reflow-soldered substrate, there are now five interactive factors to consider: the four that affect the wave solder footprints (although the solder resist may be omitted), plus an additional factor relating to the solder cream application (the positional tolerance of the screen-printed solder cream with respect to the solderlands).

Solder Cream Application

In reflow soldering, the solder cream (or paste) is applied by pressure syringe dispensing or by screen printing. For industrial purposes, screen printing is the favored technique because it is much faster than dispensing.

Screen Printing

A stainless steel mesh coated with emulsion (except for the solderland pattern where cream is required) is placed over the substrate. A squeegee passes across the screen and forces solder cream through the uncoated areas of the mesh and onto the solderland. As a result, dots of solder cream of a given height and density (in mg/mm^2) are produced.

There is an optimum amount of solder cream for each joint. For example, the solder cream requirements for the C1206 SM capacitor are around 1.5mg per end; the SO IC requires between 0.5 and 0.75mg per lead.

The solder cream density, combined with the required amount of solder, makes a demand upon the area of the solderland (in mm^2). The footprint dimensions for the solder cream pattern are typically identical to those for the solderlands.

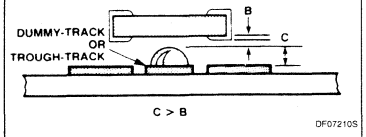


Figure 10. Through-Track or Dummy Track to Modify Dot Height Criteria

Floating

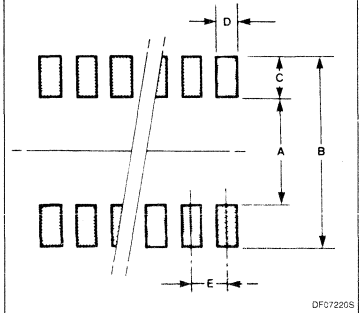
One phenomenon sometimes observed on reflow-soldered substrates is that known as "floating" (or "swimming"). This occurs when the solder paste reflows, and the force exerted by the surface tension of the now molten solder "pulls" the SMD to the center of the solderland.

When the solder reflows at both ends simultaneously, the swimming phenomenon results in the SMD self-centering on the footprint as the forces of surface tension fight for equilibrium. Although this effect can remove minor positional errors, it's not a dependable feature and cannot be relied upon. Components must always be positioned as accurately as possible.

Footprint Dimensions

The following diagrams (Fig. 11 to 19) show footprint dimensions for SO ICs, the VSO-40 package, PLCC packages, and the range of surface-mounted transistors, diodes, resistors, and capacitors. All dimensions given are based on the criteria discussed in these guidelines.

Please note — these footprints are based on our experience with both experimental and actual production substrates and are reproduced for guidance only. Research is constantly going on to cover all SMDs currently available and those planned for in the future, and data will be published when in it becomes available.



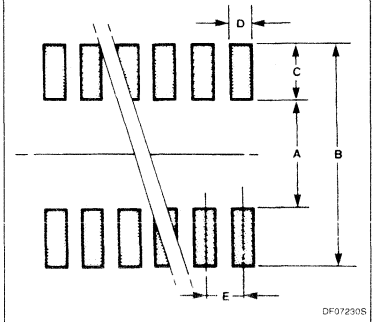
PACKAGE OUTLINE	INCHES A	B	C	D	E
SO-8, 14, 16	.155	.275	.060	.024	.050
SOL-16, 20, 24, 28	.310	.450	.070	.024	.050

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E
SO SMALL	4.0	7.0	1.5	.6	1.27
SO LARGE	7.8	11.4	1.8	.6	1.27

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E
SOL-8	9.0	13.2	2.1	.6	1.27

PACKAGE OUTLINE	INCHES A	B	C	D	E
SOL-8	.36	.528	.084	.024	.050

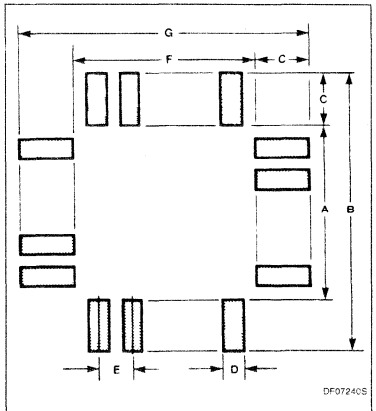
Figure 11. Footprints for SO ICs



PACKAGE OUTLINE	INCHES A	B	C	D	E
VSO-40	.32	.536	.108	.02	.030
VSO-56	.46	.676	.108	.02	.030

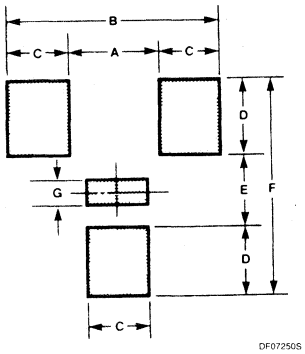
PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E
VSO-40	8.0	13.4	2.7	.5	.762
VSO-56	11.5	16.9	2.7	.5	.75

Figure 12. Footprints for VSO ICs



PACKAGE OUTLINE	INCHES A	B	C	D	E	F	G
PLCC-20	.260	.440	.090	.024	.050	.260	.440
PLCC-28	.360	.540	.090	.024	.050	.360	.540
PLCC-44	.560	.740	.090	.024	.050	.560	.740
PLCC-52	.660	.840	.090	.024	.050	.660	.840
PLCC-68	.860	1.040	.090	.024	.050	.860	1.040
PLCC-84	1.060	1.240	.090	.024	.050	1.060	1.240
PLCC-32	.360	.540	.090	.024	.050	.460	.640

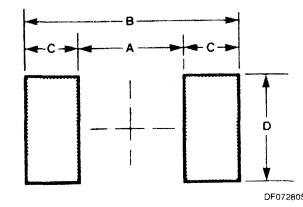
Figure 13. Footprints for PLCCs



	INCHES					
SOT-23	A	B	C	D	E	F
Reflow	0.048	0.104	0.028	0.044	0.104	—
Wave	0.032	0.136	0.052	0.052	0.048	0.152

	METRIC (mm)					
SOT-23	A	B	C	D	E	F
Reflow	1.2	2.6	0.7	1.1	2.6	—
Wave	0.8	3.4	1.3	1.3	1.2	3.8

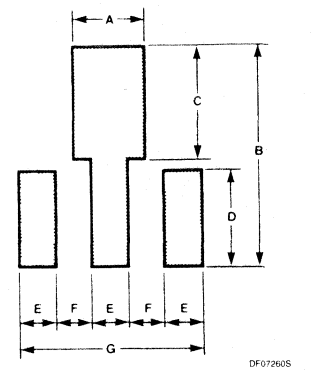
Figure 14. Footprints for SOT-23 Transistors



	INCHES			
SOD-80	A	B	C	D
Reflow	0.096	0.208	0.056	0.056
Wave	0.10	0.2	0.05	0.08

	METRIC (mm)			
SOD-80	A	B	C	D
Reflow	2.4	5.2	1.4	1.4
Wave	2.5	5.0	1.25	2.0

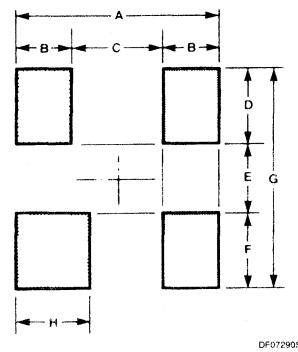
Figure 15. Footprints for SOD-80 Diodes



PACKAGE	INCHES						
OUTLINE	A	B	C	D	E	F	G
SOT-89	0.08	0.184	0.104	0.048	0.032	0.028	0.152

PACKAGE	METRIC (mm)						
OUTLINE	A	B	C	D	E	F	G
SOT-89	2.0	4.6	2.6	1.2	0.8	0.7	3.8

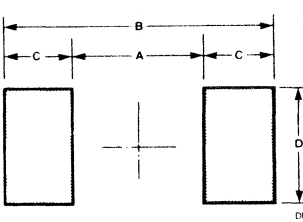
Figure 16. Footprints for Reflow-Soldered SOT-89 Transistors



PACKAGE	INCHES							
OUTLINE	A	B	C	D	E	F	G	H
SOT-143	0.104	0.028	0.048	0.036	0.044	0.036	0.116	0.044

PACKAGE	METRIC (mm)							
OUTLINE	A	B	C	D	E	F	G	H
SOT-143	2.6	0.7	1.2	0.9	1.1	0.9	2.0	1.1

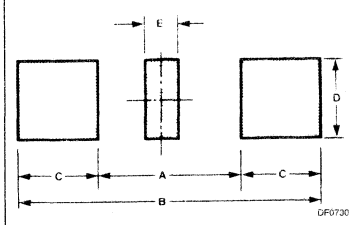
Figure 17. Footprints for Reflow-Soldered SOT-143 Transistors



		INCHES			
CODE	SIZE	A	B	C	D
C0805	0.08 × 0.05	0.032	0.136	0.052	0.056
R/C1206	0.128 × 0.064	0.072	0.184	0.056	0.068
C1210	0.128 × 0.1	0.072	0.184	0.056	0.104
C1808	0.18 × 0.08	0.112	0.248	0.068	0.084
C1812	0.18 × 0.128	0.112	0.248	0.068	0.132
C2220	0.228 × 0.2	0.16	0.296	0.068	0.204

		METRIC (mm)			
CODE	SIZE	A	B	C	D
C0805	2.0 × 1.25	0.8	3.4	1.3	1.4
R/C1206	3.2 × 1.6	1.8	4.6	1.4	1.7
C1210	3.2 × 2.5	1.8	4.6	1.4	2.6
C1808	4.5 × 2.0	2.8	6.2	1.7	2.1
C1812	4.5 × 3.2	2.8	6.2	1.7	3.3
C2220	5.7 × 5.0	4.0	7.4	1.7	5.1

Figure 18. Footprints for Reflow-Soldered Surface-Mounted Resistors and Ceramic Multilayer Capacitors



		INCHES				
	SIZE	A	B	C	D	E
C0805	0.08 × 1.05	0.048	0.144	0.048	0.048	0.016
R/C1206	0.128 × .0640.08		0.192	0.056	0.056	0.020

		METRIC (mm)				
CODE	SIZE	A	B	C	D	E
C0805	2.0 × 1.25	1.2	3.6	1.2	1.2	0.4
R/C1206	3.2 × .6	2.0	4.8	1.4	1.4	0.5

Figure 19. Footprints for Wave-Soldered Surface-Mounted Resistors and Ceramic Multilayer Capacitors

Layout Considerations

Component orientation plays an important role in obtaining consistent solder-joint quality. The substrate layout shown in Figure 20 will result in significantly better solder joints than a substrate with SMD resistors and capacitors positioned parallel to the solder flow.

Component Pitch

The minimum component pitch is governed by the maximum width of the component and the minimum distance between adjacent components. When defining the maximum component width, the rotational accuracy of the placement machine must also be considered. Figure 21 shows how the effective width of the SMD is increased when the component is rotated with respect to the footprint by angle $\phi°$. (For clarity, the rotation is exaggerated in the illustration.)

The minimum permissible distance between adjacent SMDs is a figure based upon the gap required to avoid solder-bridging during the wave soldering process. Figure 22 shows how this distance and the maximum component width are combined to derive the basic expression for calculating the minimum pitch (F_{MIN}).

As a guide, the recommended minimum pitches for various combinations of two sizes of SMDs, the R/C1206 and C0805 (R or C designating resistor or capacitor respectively; the number referring to the component size), are given in Table 1. These figures are statistically derived under certain assumed boundary conditions as follows:

- Positioning error (Δp)± 0.3mm; (± 0.012")
- Pattern accuracy (Δq)± 0.3mm; (± 0.012")
- Rotational accuracy (ϕ)± 3°
- Component metallization/solderland overlap (M_{MIN}) 0.1mm (0.004") (Note this figure is only valid for wave soldering)
- The figure for the minimum permissible gap between adjacent components (G_{MIN}) is taken to be 0.5mm (0.020").

As these calculations are not based on worst-case conditions, but on a statistical analysis of all boundary conditions, there is a certain flexibility in the given data.

For example, it is possible to position R/C1206 SMDs on a 2.5mm pitch, but the probability of component placements occurring with G_{MIN} smaller than 0.5mm will increase; hence, the likelihood of solder-bridging also increases. Each application must be assessed on individual merit with regard to acceptable levels of rework, and so on.

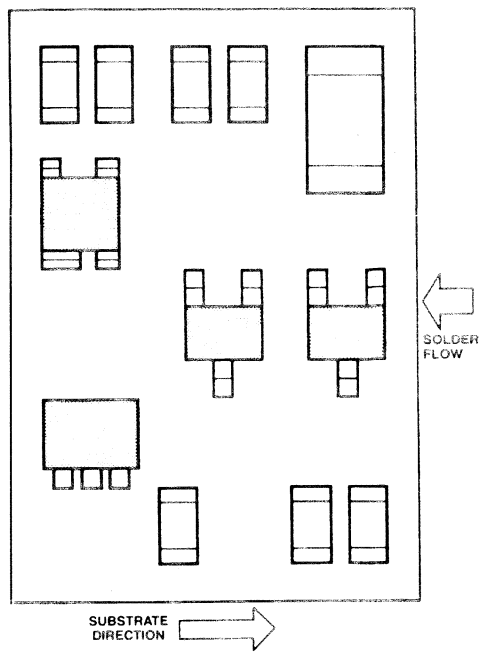
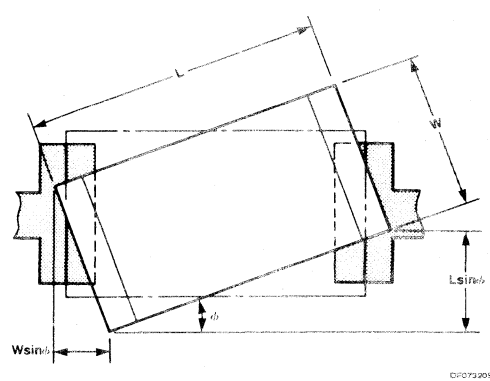


Figure 20. Recommended Component Orientation for Wave-Soldered Substrates

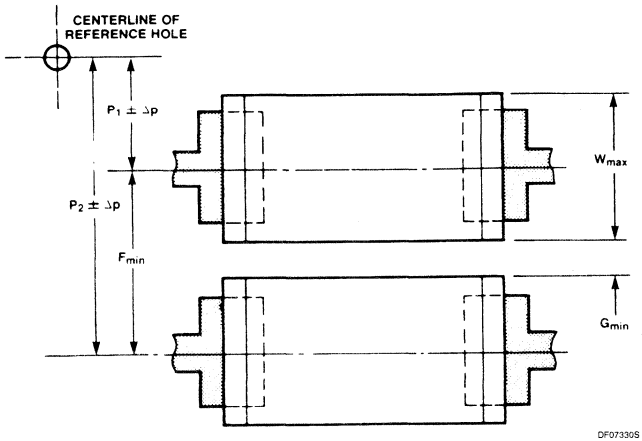


NOTES:
ϕ = Component rotation with respect to footprint
L sin ϕ = Effective increase in width
W sin ϕ = Effective increase in length

Figure 21. The Influence of Rotation of the SMD With Respect to the Footprint

Solderland/Via Hole Relationship

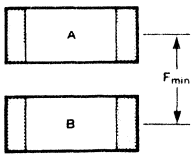
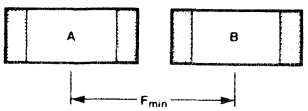
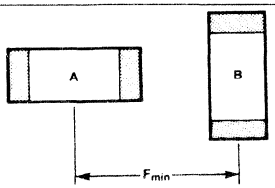
With reflow-soldered multilayer and double-sided, plated through-hole substrates, there must be sufficient separation between the via holes and the solderlands to prevent a solder well from forming. If too close to a solder joint, the via hole may suck the molten solder away from the component by capillary action; this results in insufficient wetting of the joint.



NOTES:
W_{MAX} = Maximum width of component
G_{MIN} = Minimum permissible gap
F_{MIN} = Minimum pitch
P_1 = Nominal position of component 1 (tolerance Δp)
P_2 = Nominal position of component 2 (tolerance Δp)
$F_{MIN} = W_{MAX} + 2\Delta p + G_{MIN}$

Figure 22. Criteria for Determining the Minimum Pitch of SMDs

Table 1. Recommended Pitch For R/C1206 and C0805 SMDs

Combination	Component A	Component B	
		R/C1206	C0805
	R/C1206 C0805	3.0(0.12") 2.8(0.112")	2.8(0.112") 2.6(0.0104")
	R/C1206 C0805	5.8(0.232") 5.3(0.212")	5.3(0.212") 4.8(0.192")
	R/C1206 C0805	4.1(0.164") 3.6(0.144")	3.7(0.148") 3.0(0.12")

Solderland/Component Lead Relationship

Of special consideration for mixed-print substrate layout is the location of leaded components with respect to the SMD footprints and the minimum distance between a protruding clinched lead and a conductor or SMD. Figure 23 shows typical configurations for R/C1206 SMDs mounted on the underside of a substrate with respect to the clinched leads of a leaded component. Minimum distances between the clinched lead ends and the SMDs or substrate conductors are 1mm (0.04") and 0.5 (0.02") respectively.

Placement Machine Restrictions

There are two ways of looking at the distribution of SMDs on the substrate: uniform SMD placement and non-uniform SMD placement. With nonuniform placement, center-to-center dimensions of SMDs are not exact multiples of a predetermined dimension as shown in Figure 24a, so the location of each is difficult to program into the machine.

Uniform placement uses a modular grid system with devices placed on a uniform center-to-center spacing. (For example, 2.5 (0.1") or 5mm (0.2") as shown in Figure 24b.) This placement has the distinct advantage of establishing a standard and enables the use of other automated placement machines for future production requirements without having to redesign boards.

Substrate Population

Population density of SMDs over the total area of the substrate must also be carefully considered, as placement machine limitations can create a "lane" or "zone" that restricts the total number of components which can be placed within that area on the substrate.

For example, on a hardware-programmable simultaneous placement machine (see Figure 3c), each pick-and-place unit within the placement module can only place a component on the substrate in a restricted lane (owing to

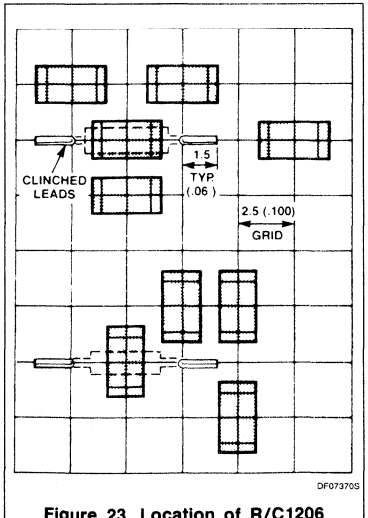
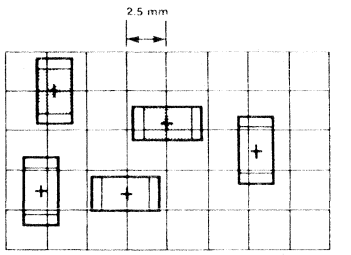
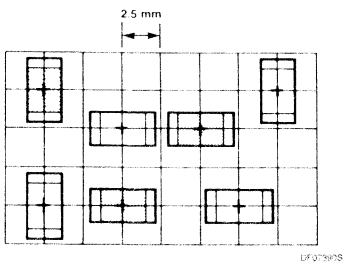


Figure 23. Location of R/C1206 SMDs on the Underside of a Mixed-Print Substrate with Respect to the Clinched Leads of Through-Hole Components (Dimensions in mm)



a. Non-Uniform Component Placement



b. Uniform Component Placement

Figure 24

adjacent pick-and-place units), typically 10 to 12mm (0.4" to 0.48") wide, as shown in Figure 25.

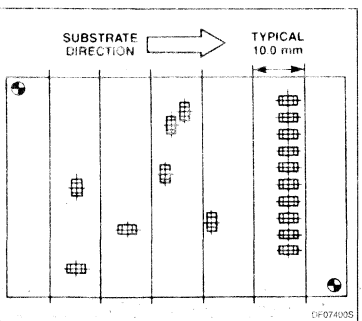


Figure 25. Substrate "Lanes" From Use of a Simultaneous Placement Machine

Placement of the 10 components in the lane on the right of the substrate shown will require a machine with 10 placement modules (or ten passes beneath a single placement module), an inefficient process considering that there are no more than three SMDs in any other lane.

Test Points

Siting of test points for in-circuit testing of SMD substrates presents problems owing to the fewer via holes, higher component densities, and components on both sides of SMD substrates. On conventional double-sided PCBs, the via holes and plated-through component lead-holes mean that most test-points are accessible from one side of the board. However, on SMD substrates, extra provision for test-points may have to be made on both sides of the substrate.

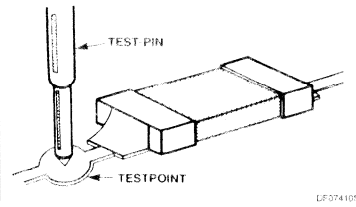
Figure 26a shows the recommended approach for positioning test-points in tracks close to components, and Figure 26b shows an acceptable (though not recommended) alternative where the solderland is extended to accommodate the test pin. This latter method avoids sacrificing too much board space, thus maintaining a high-density layout, but can introduce the problem of components moving ("floating") when reflow-soldered. The approach shown in Figure 26c is totally unacceptable since the pressure applied by the test pin can make an open-circuit soldered joint appear to be good, and, more importantly, the test pin can damage the metallization on the component, particularly with small SMDs.

CAD Systems for SMD Substrate Layout

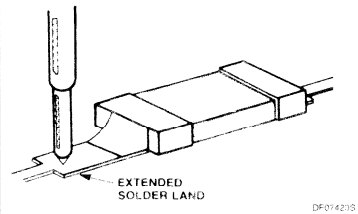
At present, about half of all PCBs are laid out using computer-aided design (CAD) techniques, and this proportion is expected to rise to over 90% by 1988. Of the many current CAD systems available for designing PCB layouts for conventional through-hole components and ICs in DIL packages, few are SMD-compatible, and systems dedicated exclusively to SMD substrate layout are still comparatively rare. There are two main reasons for this: some CAD suppliers are waiting for SMD technology to fully mature before updating their systems to cater to SMD-loaded substrates, and others are holding back until standard package outlines are fully defined.

However, updating CAD systems used for through-hole printed boards is not simply a case of substituting SMD footprints for conventional component footprints, since SMD-populated substrates impose far tougher restraints on PCB layout and require a total rethink of the layout programs. For example, systems must deal with higher component densities, finer track widths, devices on both sides of the substrate (possibly occupying corresponding positions on opposite sides), and even SMDs under conventional DILs on the same side of the substrate.

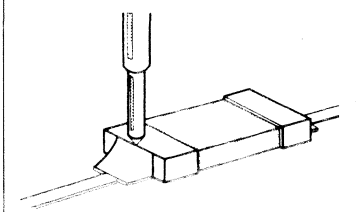
The amount of reworking that a program requires depends on whether it's an interactive (manual) system, or one with fully automatic routing and placement capabilities. For



a. RECOMMENDED Test Point Location Close to an SMD



b. Acceptable Test Point Location



c. UNACCEPTABLE Test Point Location

Figure 26

interactive systems, where the user positions the components and routes the tracks manually on-screen, program modifications will be minimal. Automatic systems, however, must contend with the stricter design rules for SMD substrate layout. For example, many autorouting programs assume that every solderland is a plated through-hole and, therefore, can be used as a via hole. This is not applicable for SMD-populated substrates.

CAD programs base the substrate layout on a regular grid. This method, analogous to drawing the layout on graph paper, must have the grid lines on a pitch that is no larger than the smallest component or feature (track width, pitch, and so on). For conventional DIL boards, this is typically 0.635mm (0.025"), but with the much smaller SMDs, a grid spacing of 0.0254mm (0.001") is required. Consequently, for the same area of substrate, a CAD system based on this finer grid requires

a resolution more than 600 times greater than that required for conventional-layout CAD systems.

To handle this, extra memory capacity can be added, or the allowable substrate area can be limited. In fact, the small size of SMDs, and the high-density layouts possible, generally result in a smaller substrate. However, high-density layout gives rise to additional complications not directly related to the SMD substrate design guidelines. Most CAD systems, for instance, cannot always completely route all interconnects, and some traces have to be routed manually. This can be particularly difficult with the fewer via holes and smaller component spacing of SMD boards.

Ideally, the CAD program should have a "tear-up and start again" algorithm that allows it to restart autorouting if a previous attempt reaches a position where no further traces can be routed before an acceptable percentage of interconnects (and this percentage must first be determined) have been made. This minimizes the manual reworking required.

CAE/CAD/CAM Interaction

Computer-aided production of printed boards has evolved from what was initially only a computer-aided manufacturing process (CAM — digitizing a manually-generated layout and using a photoplotter to produce the artwork) to fully-interactive computer-aided engineering, design, and manufacture using a common database. Figure 27 illustrates how this multi-dimensional interaction is particularly well-suited to SMD-populated substrate manufacture in its highly-automated environment of pick-and-place assembly machines and test equipment.

Using a fully-integrated system, linked by local area network to a central database, will make it possible to use the initial computer-aided engineering (CAE — schematic design, logic verification, and fault simulation) in the generation of the final test patterns at the end of the development process. These test patterns can then be used with the automatic test equipment (ATE) for functional testing of the finished substrates.

Such a system is particularly useful for testing SMD-populated substrates, as their high component density and fewer via-holes make in-circuit testing ("bed of nails" approach) difficult. Consequently, manufacturers are turning to functional testing as an alternative. These aspects are covered in another publication entitled *Functional Testing and Repair*.

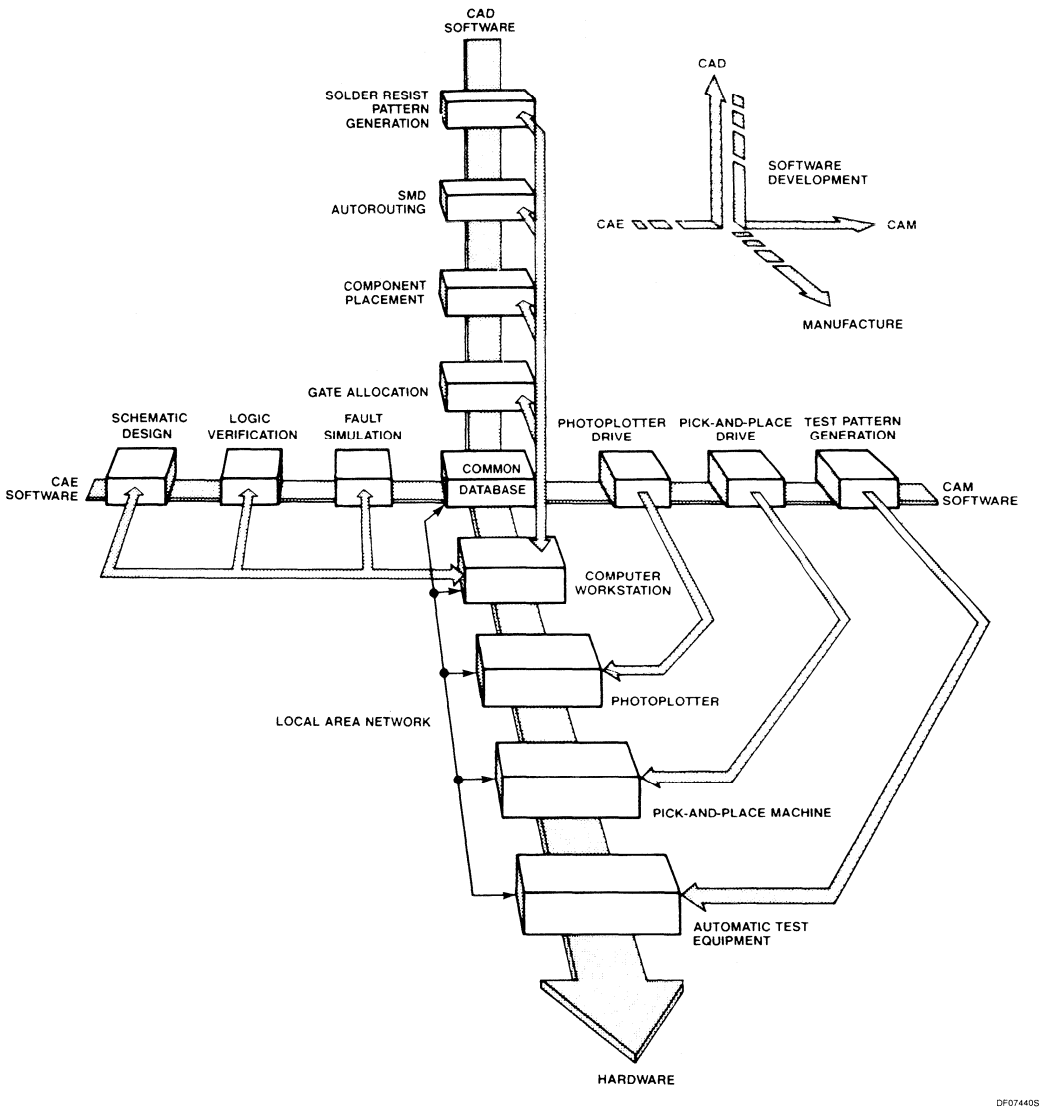


Figure 27. The Software-Hardware Interaction for the Computer-Aided Engineering, Design, and Manufacture of SMD Substrates

AN INTRODUCTION

The key questions that must be asked of any electronic circuit are "does it work, and will it continue to do so over a specified period of time?" Until zero-defect soldering is achieved, and all components are guaranteed serviceable by the vendors, manufacturers can only answer these questions by carrying out some form of test on the finished product.

The types of tests, and the depth to which they are carried out, are determined by the complexity of the circuit and the customer's requirements. The amount of rework to be performed on the circuit will depend on the results of these tests and the degree of reliability demanded. The criteria are true of all electronic assemblies, and the test engineer must formulate test schedules accordingly.

Substrates loaded with surface mounted devices (SMDs), however, pose additional problems to the test engineer. The devices are much smaller, and substrate population density is greater, leading to difficulty in accessing all circuit nodes and test points. Also SMD substrate layout designs often have fewer via and component lead holes, so test points may not all be on one side of the substrate and double-sided test fixtures become necessary.

To achieve the high throughput rates made possible by using highly automated SMD placement machines and volume soldering techniques, automatic testing becomes a necessity. Visual inspection of the finished substrate by trained inspectors can normally detect about 90% of defects. With the correct combination of automatic test equipment, the remainder can be eliminated. In this publication, we hope to provide the manufacturer with information to enable him to evaluate and select the best combination of test equipment and the most effective test methods for his product.

BARE-BOARD TESTING

Although SMD substrates will undoubtedly be smaller than conventional through-hole substrates and have less space between conductors, the principles of bare-board testing remain the same. Many of the testers already in use can, with little or no modification, be used for SMD substrates. As this is already a well-established and well-documented practice, it will not be discussed further in this publication, but it is recommended that bare-board testing always be used as the first step in assuring board integrity.

POST-ASSEMBLY TESTING

Testing densely populated substrates is no easy task, as the components may occupy both sides of the board and cover many of the circuit nodes (see Figure 1 for the three main types of SMD-populated substrates). Unlike conventional substrates, on which all test points are usually accessible from the bottom, SMD assemblies must be designed from the start with the siting of test points in mind. Probing SMD substrates is particularly difficult owing to the very close spacing of components and conductors.

Mixed print or all-SMD assemblies with components on both sides further aggravate the testing problems, as not all test points are present on the same side of the board. Although two-sided test fixtures are feasible, they are expensive and require considerable time to build.

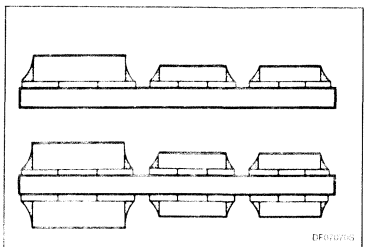
The application of a test probe to the top of an SMD termination could damage it, and probe pressure on a poor or open solder joint can force contact and thus allow a defective joint to be assessed as good. Figure 2a illustrates the recommended siting of test points close to SMD terminations, and Figure 2b shows an alternative, though not recommended, option. Here, problems could arise from reflow soldering (solder migrating from the joint) unless the test point area is separated from the solder land area with a stripe of solder resist. Excessive mechanical pressure caused by too many probes concentrated in a small area may also result in substrate damage.

It is good practice for substrates to have test points on a regular grid so that conventional, rather than custom, testers may be used. If the substrate has tall components or heatsinks, the test points must be located far enough away to allow the probes to make good contact. All test points should be solder coated to provide good electrical contact. Via holes may also be used as test points, but the holes must be filled with solder to prevent the probe from sticking.

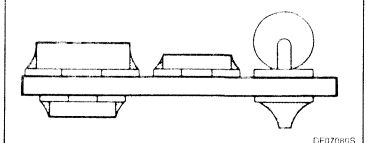
AUTOMATIC TEST EQUIPMENT (ATE)

As manufacturers strive to increase production, the question becomes not whether to use automatic test engineering (ATE), but which ATE system to use and how much to spend on it. Because of the rapid fall in price of computers, memories, and peripherals, today's low-cost ATE equals the performance of the high-cost equipment of just two or three years ago. For factory automation, manufacturers must consider many factors, such as production volume, product complexity, and availability of skilled personnel.

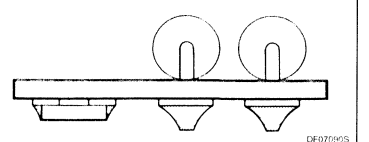
One question is whether the ATE system can be used not only for production testing but also for service and repair to reduce the high cost of keeping a substrate inventory in the field. Another is whether assembly and process-induced faults represent a significant percentage of production defects, rather than out-of-tolerance components. These questions need to be answered before deciding on the type of ATE system required.



a. Type I — Total Surface Mount (All-SMD) Substrates

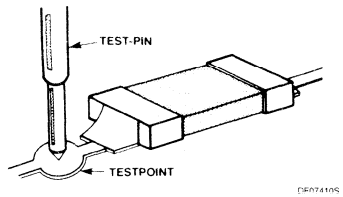


b. Type IIA — Mixed Print (Double-Sided) Substrate

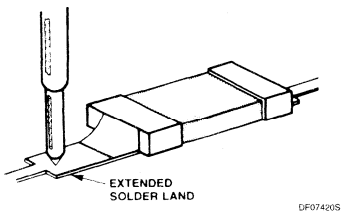


c. Type IIB — Mixed Print (Underside Attachment) Substrate

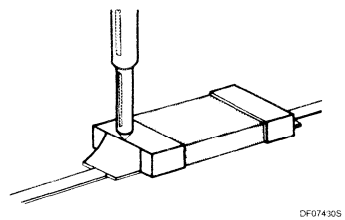
Figure 1



a. Recommended Location of Test Points Close to SMDs



b. Acceptable, Though Not Recommended, Location of Test Points Close to SMDs



c. Unacceptable Location of Test Points Close to SMDs

Figure 2

Several systems are currently available to the manufacturer, including short-circuit testers, in-circuit testers, in-circuit analyzers, and functional testers. Figure 3 shows a bar-chart giving a comparison of percent fault detection and programming time for various ATE systems.

A loaded-board, short-circuit tester takes from two to six hours to program and its effective fault coverage is between 35% and 65%. It has the advantage of being operationally fast and comparatively inexpensive. On the negative side, however, it is limited to the detection of short-circuits and may require a double-sided, bed-of-nails test fixture (see Figure 4), which for SMD substrates may be expensive and take time to produce. Careful

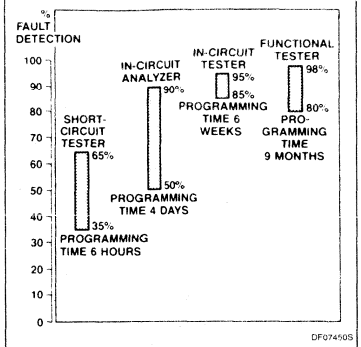


Figure 3. Bar Chart Showing a Comparison of Percent Fault Detection and Programming Time for Various ATE Systems

design can, however, often eliminate the need for double-sided test probe fixtures.

In-circuit testers power the assembly and check for open or short-circuits, circuit parameters, and can pinpoint defective components. They can provide around 90% fault coverage, but are more expensive than short-circuit testers and programming can take more than six weeks.

In-circuit analyzers are relatively simple to program and can detect manufacturing-induced faults in one third of the time required by an in-circuit tester. Fault coverage is between 50% and 90%. Because they do not power the assembly, they cannot detect digital logic faults, unlike an in-circuit tester or functional tester.

Functional testers, on the other hand, check the assembly's performance and simply make a go or no-go decision. Either the assembly performs its required function or it does not. They are much more expensive, but their fault coverage is between 80% and 98%. Their major disadvantages, apart from cost, are that they cannot locate defective components, and programming for a high-capacity system can take as long as nine months.

ATE Systems

An analysis of defects on a finished substrate will determine which combination of ATE will best meet the test requirements with regard to fault coverage and throughput rate.

If most defects are short-circuits, a loaded-board short-circuit tester, in tandem with an in-circuit tester, will pre-screen the substrate for short-circuits twice as fast as the in-circuit tester. This allows more time for the in-circuit tester to handle the more complex test requirements. This combination of ATE, instead of an in-circuit tester alone, improves the throughput rate.

Combining a short-circuit tester with a functional tester produces even more dramatic results. If most defects are manufacturing-produced shorts, the use of a short-circuit tester to relieve the functional tester of this task can increase throughput five-fold while maintaining a fault coverage of up to 98%.

If manufacturing faults and analog component defects are responsible for the majority of failures, a relatively low-cost, in-circuit analyzer can be used in tandem with an in-circuit tester or functional tester to reduce testing costs and improve throughput. The in-circuit analyzer is three times faster than an in-circuit tester in detecting manufacturing-induced faults, offers test and diagnostics usually within 10 seconds each, and is relatively simple to program. But because it is unpowered, an in-circuit analyzer cannot test digital logic faults; either an in-circuit tester or functional tester following the in-circuit analyzer must be used to locate this type of defect.

POLLUTED POWER SUPPLIES

Today's electronic components and the equipment used to test them are susceptible to electrical noise. Erroneous measurements on pass-or-fail tests could lower test throughput or, even more seriously, allow defective products to pass inspection. Semiconductor chips under test can also be damaged or destroyed as high-energy pulses or line-voltage surges stress the fine-line geometrics separating individual cells.

Noise pulses can be either in the normal (line-to-line) mode or common (line-to-ground) mode. Common-mode electrical noise poses a special threat to modern electronic circuitry since the safety ground line to which common-mode noise is referenced is often used as the system's logic reference point. Since parasitic capacitance exists between safety ground and the reference point, at high frequencies these points are essentially tied together, allowing noise to directly enter the system's logic.

MANUAL REPAIR

The repair of SMD-populated substrates will entail either the resoldering of individual joints and the removal of shorts or the replacement of defective components.

The reworking of defective joints will invariably involve the use of a manual soldering iron. Bits are commercially available in a variety of shapes, including special hollow bits used for desoldering and for the removal of solder bridges. The criteria for the inspec-

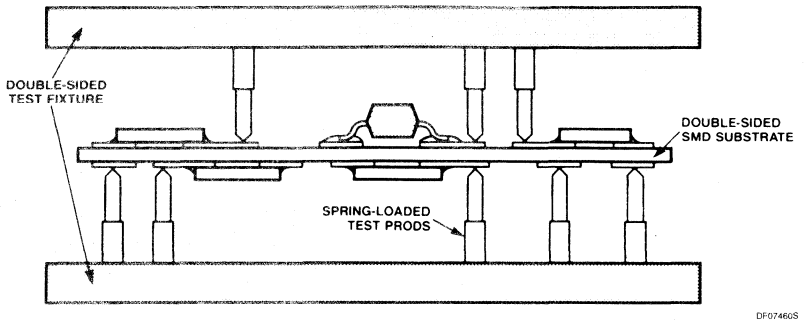


Figure 4. Double-Sided, Bed-of-Nails Test Fixture

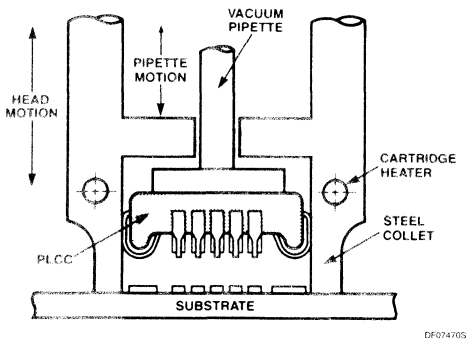


Figure 5. Heated Collet for the Removal and Replacement of Multi-Leaded SMDs (a PLCC is Shown Here)

tion of reworked soldered joints are the same as those for machine soldering.

Special care must be taken when reworking or replacing electrostatic sensitive devices. Soldering irons should be well grounded via a safety resistor of minimum 100kΩ. The ground connection to the soldering iron should be welded rather than clamped. This is because oxidation occurs beneath the clamp, thus isolating the ground connection. Voltage spikes caused by the switching of the iron can be avoided by using either continuously-powered irons, or irons that switch only at zero voltage on the AC sine curve.

To remove defective leadless SMDs, a variety of soldering iron bits are available that will apply the correct amount of heat to both ends of the component simultaneously and allow it to be removed from the substrate. If the substrate has been wave soldered, an adhesive will have been used, and the bond can be broken by twisting the bit. Any adhesive residue must then be removed. The same tool is then used to place and solder the new component, using either solder cream or resin-cored solder.

When a multi-leaded component, such as a plastic leaded chip carrier (PLCC), has to be removed, a heated collet can be used (see Figure 5). The collet is positioned over the PLCC, heat is applied to the leads and solder lands automatically until the solder reflows. The collet, complete with the PLCC, is then raised by vacuum. Solder cream is then re-applied to the solder lands by hand. No adhesive is required in this operation.

The collet is positioned over the replacement PLCC, which is held in place by the slight spring pressure of the PLCC leads against the walls of the collet. The collet, complete with PLCC, is then raised pneumatically and positioned over the solder lands.

Using air pressure, the center pin of the collet then pushes the PLCC into contact with the substrate where it is maintained with the correct amount of force. Heat is then applied through the walls of the collet to reflow the solder paste. The center pin maintains pressure on the PLCC until the solder has solidified, then the center pin is raised and the replacement is complete.

Another method, well-suited to densely populated SMD substrates, uses a stream of heated air, directed onto the SMD terminations. Once the solder has been reflowed, the component can be removed with the aid of tweezers. While the hot air is being directed onto the component, cooler air is played onto the bottom of the substrate to protect it from heat damage. During removal, the component should be twisted sideways slightly in order to break the surface tension of the solder and any adhesive bond between the component and the substrate. This prevents damage to the substrate when the component is lifted.

To fit a new component, the solder lands are first retinned and fluxed, the new component accurately placed, and the solder reflowed with hot air. Substituting superheated argon, nitrogen, or a mixture of nitrogen and hydrogen for the hot air stream removes any risk of contaminating or oxidizing the solder.

Focused infrared light has also been used successfully to reflow the solder on densely populated substrates.

In general, the equipment and procedures used for the replacement of PLCCs can be used for leadless ceramic chip carriers (LCCCs) and small-outline packages (SO ICs). SO ICs are somewhat easier to replace, as the leads are more accessible and only on two sides of the component.

Fluxing and Cleaning

INTRODUCTION

The adoption of mass soldering techniques by the electronics industry was prompted not only by economics, and a requirement for high throughput levels, but also by the need for a consistent standard of quality and reliability in the finished product unattainable by using manual methods. With surface-mounted device (SMD) assembly, this need is even greater.

The quality of the end-product depends on the measures taken during the design and manufacturing stages. The foundations of a high-quality electronic circuit are laid with good design, and with correct choice of components and substrate configuration. It is, however, at the manufacturing stage where the greatest number of variables, both with respect to materials and techniques, have to be optimized to produce high-quality soldering, a prerequisite for reliability.

Of the two most commonly-used soldering techniques, wave and reflow, wave soldering is by far the most widely used and understood. Many factors influence the outcome of the soldering operation, some relating to the soldering process itself, and others to the condition of components and substrate to which they are to be attached. These must be collectively assessed to ensure high-quality soldering.

One of the most important, most neglected, and least understood of these processes is the choice and application of flux. This section outlines the fluxing options available, and discusses the various cleaning techniques that may be required, for SMD substrate assembly.

FLUXES

Populating a substrate involves the soldering of a variety of terminations simultaneously. In one operation, a mixture of tinned copper, tin/lead-or gold-plated nickel-iron, palladium-silver, tin/lead-plated nickel-barrier, and even materials like Kovar, each possessing varying degrees of solderability, must be attached to a common substrate using a single solder alloy.

It is for this reason that the choice of the flux is so important. The correct flux will remove surface oxides, prevent reoxidization, help to transfer heat from source to joint area, and leave non-corrosive, or easily removable corrosive residues on the substrate. It will also improve wettability of the solder joint surfaces.

The wettability of a metal surface is its ability to promote the formation of an alloy at its interface with the solder to ensure a strong, low-resistance joint.

However, the use of flux does not eliminate the need for adequate surface preparation. This is very important in the soldering of SMD substrates, where any temptation to use a highly-active flux in order to promote rapid wetting of ill-prepared surfaces should be avoided because it can cause serious problems later when the corrosive flux residues have to be removed. Consequently, optimum solderability is an essential factor for SMD substrate assembly.

Flux is applied before the wave soldering process, and during the reflow soldering process (where flux and solder are combined in a solder cream). By coating both bare metal and solder, flux retards atmospheric oxidization which would otherwise be intensified at soldering temperature. In the areas where the oxide film has been removed, a direct metal-to-metal contact is established with one low-energy interface. It is from this point of contact that the solder will flow.

Types of Flux

There are two main characteristics of flux. The first is efficacy—its ability to promote wetting of surfaces by solder within a specified time. Closely related to this is the activity of the flux, that is, its ability to chemically clean the surfaces.

The second is the corrosivity of the flux, or rather the corrosivity of its residues remaining on the substrate after soldering. This is again linked to the activity; the more active the flux, the more corrosive are its residues.

Although there are many different fluxes available, and many more being developed, they fall into two basic categories; those with residues soluble in organic liquids, and those with residues soluble in water.

Organic Soluble Fluxes

Most of the fluxes soluble in organic liquids are based on colophony or rosin (a natural product obtained from pine sap that has been distilled to remove the turpentine content). Solid colophony is difficult to apply to a substrate during machine soldering, so it is dissolved in a thinning agent, usually an alcohol. It has a very low efficacy, and hence limited cleaning power, so activators are added in varying quantities to increase it. These take the form of either organic acids, or organic salts that are chemically active at soldering temperatures. It is therefore convenient to classify the colophony-based fluxes by their activator content.

Non-Activated Rosin (R) Flux

These fluxes are formed from pure colophony in a suitable solvent, usually isopropanol or ethyl alcohol. Efficacy is low and cleaning action is weak. Their uses in electronic soldering are limited to easily-wettable materials with a high level of solderability. They are used mainly on circuits where no risk of corrosion can be tolerated, even after prolonged use (implanted cardiac pacemakers, for example). Their flux residues are noncorrosive and can remain on the substrate, where they will provide good insulation.

Rosin, Mildly-Activated (RMA) Flux

These fluxes are also composed of colophony in a solvent, but with the addition of activators, either in the form of di-basic organic acids (such as succinc acid), or organic salts (such as dimethylammonium chloride or diethylammonium chloride). It is customary to express

the amount of added activator as mass percent of the chlorine ion on the colophony content, as the activator-to-colophony ratio determines the activity, and, hence, the corrosivity. In the case of RMA activated with organic salts, this is only some tenths of one percent.

When organic acids are used, a higher percentage of activator must be added to produce the same efficacy as organic salts, so frequently both salts and acids are added. The cleaning action of RMA fluxes is stronger than that of the R type, although the corrosivity of the residues is usually acceptable. These residues may be left on the substrate as they form a useful insulating layer on the metal surfaces. This layer can, however, impede the penetration of test probes at a later stage.

Rosin, Activated (RA) Flux

The RA fluxes are similar to the RMA fluxes, but contain a higher proportion of activators. They are used mainly when component or substrate solderability is poor and corrosion-risk requirements are less stringent. However, as good solderability is considered essential for SMD assembly, highly-activated rosin fluxes should not be necessary. The removal of

flux residues is optional and usually dependent upon the working environment of the finished product and the customer's requirements.

Water-Soluble Fluxes

The water-soluble fluxes are generally used to provide high fluxing activity. Their residues are more corrosive and more conductive than the rosin-based fluxes, and, consequently, must always be removed from the finished substrate. Although termed water soluble, this does not necessarily imply that they contain water; they may also contain alcohols or glycols. It is the flux residues that are water soluble. The usual composition of a water-soluble flux is shown below.

1. A chemically-active component for cleaning the surfaces.
2. A wetting agent to promote the spreading of flux constituents.
3. A solvent to provide even distribution.
4. Substances such as glycols or water-soluble polymers to keep the activator in close contact with the metal surfaces.

Although these substances can be dissolved in water, other solvents are generally used, as water has a tendency to spatter during soldering. Solvents with higher boiling points, such as ethylene glycol or polyethylene glycol are preferred.

Water-Soluble Fluxes With Inorganic Salts

These are based on inorganic salts such as zinc chloride, or ammonium chloride, or inorganic acids such as hydrochloric. Those with zinc or ammonium chloride must be followed by very stringent cleaning procedures as any halide salts remaining on the substrate will cause severe corrosion. These fluxes are generally used for non-electrical soldering. Although the hydrazine halides are among the best active fluxing agents known, they are highly suspect from a health point of view and are therefore no longer used by flux manufacturers.

Water-Soluble Fluxes With Organic Salts

These fluxes are based on organic hydrohalides such as dimethylammonium chloride, cyclo hexalamine hydrochloride, and aniline hydrochloride, and also on the hydrohalides of organic acids. Fluxes with organic halides usually contain vehicles such as glycerol or polyethylene glycol, and non-ionic surface-active agents such as nonylphenol polyoxyethylene. Some of the vehicles, such as the polyethylene glycols, can degrade the insulation resistance of epoxy substrate material and, by rendering the substrate hydrophilic, make it susceptible to electrical leakage in high-humidity environments.

Water-Soluble Fluxes With Organic Acids

Based on acids such as lactic, melonic, or citric, these fluxes are used when the presence of any halide is prohibited. However, their fluxing action is weak, and high acid concentrations have to be used. On the other hand, they have the advantage that the flux residues can be left on the substrate for some time before washing without the risk of severe corrosion.

Solder Creams

For reflow soldering, both the solder and the flux are applied to the substrate before soldering and can be in the form of solder creams (or pastes), preforms, electro-deposit, or a layer of solder applied to the conductors by dipping. For SMD reflow soldering, solder cream is generally used.

Solder cream is a suspension of solder particles in flux to which special compounds have been added to improve the rheological properties. The shape of the particles is important and normally spherical particles are used, although non-spherical particles are now being added, particularly in very fine-line soldering.

In principle, the same fluxes are used in solder creams as for wave soldering. However, due to the relatively large surface area of the solder particles (which can oxidize), more effective fluxing is required and, in general, solder creams contain a higher percentage of activators than the liquid fluxes. The drying of the solder paste during preheating (after component placement) is an important stage as it reduces any tendency for components to become displaced during soldering.

Flux Selection

Choosing an appropriate flux is of prime importance to the soldering system for the production of high-quality, reliable joints. When solderability is good, a mildly-activated flux will be adequate, but when solderability is poorer, a more effective, more active flux will be required. The choice of flux, moreover, will be influenced by the cleaning facilities available, and if, in fact, cleaning is even feasible.

With water-soluble fluxes, aqueous cleaning of the substrate after soldering is mandatory. If thorough cleaning is not carried out, severe problems may arise in the field, due to corrosion or short circuits caused by too low a surface resistance of the conductive residues.

For rosin-based fluxes, the need for cleaning will depend on the activity of the flux. Mildly-activated rosin residues can, in most cases, remain on the substrate where they will afford protection and insulation. In practice, for the great majority of electronic circuits, the choice will be between an RA or an RMA rosin-based flux.

Application of Flux

Three basic factors determine the method of applying flux: the soldering process (wave or reflow), the type of substrate being processed (all-SMD or mixed print), and the type of flux.

For wave soldering, the flux must be applied in liquid form before soldering. While it is possible to apply the flux at a separate fluxing station, with the high throughput rates demanded to maximize the benefits of SMD technology, today's wave-soldering machines incorporate an integral fluxing station prior to the preheat stage. This enables the preheat stage to be used to dry the flux as well as preheat the substrate to minimize thermal shock.

The most commonly-used methods of applying flux for wave soldering are by foam, wave, or spray.

Foam Fluxing

Foam flux is generated by forcing low-pressure clean air through an aerator immersed in liquid flux (see Figure 1). The fine bubbles produced by the aerator are guided to the surface by a chimney-shaped nozzle. The substrates are passed across the top of the nozzle so that the solder side comes in contact with the foam and an even layer of flux is applied. As the bubbles burst, flux penetrates any plated-through holes in the substrate.

Wave Fluxing

A double-sided wave can also be used to apply flux, where the washing action of the wave deposits a layer of flux on the solder side of the substrate (see Figure 2). Wave-height control is essential and a soft, wipe-off brush should be incorporated on the exit side of the fluxing station to remove excess flux from the substrate.

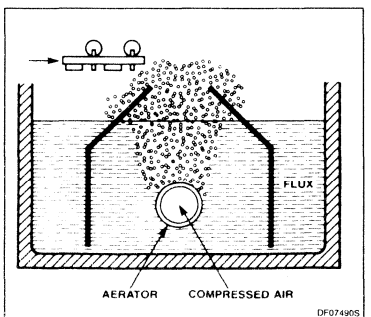


Figure 1. Schematic Diagram of Foam Fluxer

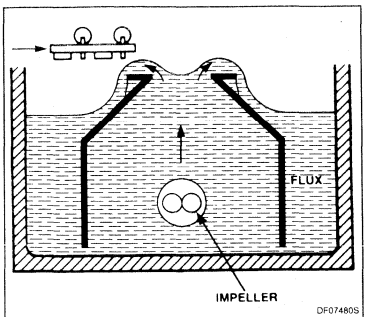


Figure 2. Schematic Diagram of Wave Fluxer

Spray Fluxing

Several methods of spray fluxing exist; the most common involves a mesh drum rotating in liquid flux. Air is blown into the drum which, when passing through the fine mesh, directs a spray of flux onto the underside of the substrate (see Figure 3). Four parameters affect the amount of flux deposited: conveyor speed, drum rotation, air pressure, and flux density. The thickness of the flux layer can be controlled using these parameters, and can vary between 1 and 10μm.

The advantages and disadvantages of these three flux application techniques are outlined in Table 1.

Flux Density

One of the main control factors for fluxes used in machine soldering is the flux density. This provides an indication of the solids content of the flux, and is dependent on the nature of the solvents used. Automatic control systems, which monitor flux density and inject more solvent as required, are commercially available, and it is relatively simple to incorporate them into the fluxing system.

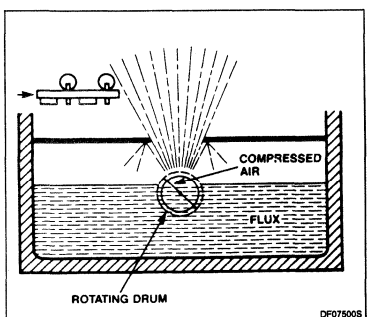


Figure 3. Schematic Diagram of Spray Fluxer

PREHEATING

Preheating the substrate before soldering serves several purposes. It dries the flux to evaporate most of the solvent, thus increasing the viscosity. If the viscosity is too low, the flux may be prematurely expelled from the substrate by the molten solder. This can result in poor wetting of the surfaces, and solder spatter.

Drying the flux also accelerates the chemical action of the flux on the surfaces, and so speeds up the soldering process. During the preheating stage, substrate and components are heated to between 80°C and 90°C (solvent-based fluxes) or to between 100°C and 110°C (water-based systems). This reduces the thermal shock when the substrate makes contact with the molten solder, and minimizes any likelihood of the substrate warping.

The most common methods of preheating are: convection heating with forced air, radiation heating using coils, infrared quartz lamps or heated panels, or a combination of both convection and radiation. The use of forced air has the added advantage of being more effective for the removal of evaporated solvent. Optimum preheat temperature and duration will depend on the nature and design of the substrate and the composition of the flux.

Figure 4 shows a typical method of preheat temperature control. The desired temperature is set on the control panel, and the microprocessor regulates preheater No. 1 to provide approximately 60% of the required heat. The IR detector scans the substrate immediately following No. 1 heater and reads the surface temperature. By taking into account the surface temperature, conveyor speed, and the thermal characteristics of the substrate, the microprocessor then calculates the amount of additional heat required to be provided by heater No. 2 in order to attain the preset temperature. In this way, each substrate will have the same surface temperature on reaching the solder bath.

POSTSOLDERING CLEANING

Now that worldwide efforts in both commercial and industrial electronics are converting old designs from conventional assembly to surface mounting, or a combination of both, it can also be expected that high-volume cleaning systems will convert from in-line aqueous cleaners to in-line solvent cleaners or in-line saponification systems (a technique that uses an alkaline material in water to react with the rosin so that it becomes water soluble). These systems may, however, become subject to environmental objections, and new governmental restrictions on the use of halogenated hydrocarbons.

The major reason for this is that the water-soluble flux residues, containing a higher concentration of activators, or showing hygroscopic behavior, are much more difficult to remove from SMD-populated substrates than rosin-based flux residues. This is primarily because the higher surface tension of water, compared to solvents, makes it difficult for the cleaning agents to penetrate beneath SMDs, especially the larger ones, with their greatly reduced off-contact distance (the distance between component and substrate).

Postsoldering cleaning removes any contamination, such as surface deposits, inclusions, occlusions, or absorbed matter which may degrade to an unacceptable level the chemical, physical, or electrical properties of the assembly. The types of contaminant on substrates that can produce either electrical or mechanical failure over short or prolonged periods are shown in Table 2.

All these contaminants, regardless of their origin, fall into one of two groups: polar and non-polar.

Polar Contaminants

Polar contaminants are compounds that dissociate into free ions which are very good conductors in water, quite capable of causing circuit failures. They are also very reactive with metals and produce corrosive reactions. It is essential that polar contaminants be removed from the substrates.

Non-Polar Contaminants

Non-polar contaminants are compounds that do not dissociate into free ions or carry an electrical current and are generally good insulators. Rosin is a typical example of a non-polar contaminant. In most cases, non-polar contamination does not contribute to corrosion or electrical failure and may be left on the substrate. It may, however, impede functional testing by probes and prevent good conformal coat adhesion.

Solvents

The solvents currently used for the post-soldering cleaning of substrates are normally organic based and are covered by three classifications: hydrophobic, hydrophillic, and azeotropes of hydrophobic/hydrophillic blends.

Azeotropic solvents are mixtures of two or more different solvents which behave like a single liquid insomuch that the vapor produced by evaporation has the same composition as the liquid, which has a constant boiling point between the boiling points of the two solvents that form the azeotrope. The basic ingredients of the azeotropic solvents are combined with alcohols and stabilizers. These stabilizers, such as nitromethane, are included to prevent corrosive reaction be-

Table 1. Advantages and Disadvantages of Flux Application Methods

Method	Advantages	Disadvantages
Foam Fluxing	• Compatible with continuous soldering process • Foam crest height not critical • Suitable for mixed-print substrates	• Not all fluxes have good foaming capabilities • Losses throught evaporation may be appreciable • Prolonged preheating because of high boiling point of solvents
Wave Fluxing	• Can be used with any liquid flux • Compatible with continuous soldering process • Suitable for densely-populated mixed print	• Wave crest height is critical to ensure good contact with bottom of substrate without contaminating the top
Spray fluxing	• Can be used with most liquid fluxes • Short preheat time if appropriate alcohol solvents are used • Layer thickness is controllable	• High flux losses due to non-recoverable spray • System requires frequent cleaning

tween the metallization of the substrate and the basic solvents.

Hydrophobic solvents do not mix with water at concentrations exceeding 0.2%, and consequently have little effect on ionic contamination. They can be used to remove non-polar contaminants such as rosin, oils, and greases.

Hydrophillic solvents do mix with water and can dissolve both polar and non-polar contamination, but at different rates. To overcome these differences, azeotropes of the various solvents are formulated to maximize the dissolving action for all types of contamination.

Solvent Cleaning

Two types of solvent cleaning systems are in use today: batch and conveyorized systems, either of which can be used for high-volume production. In both systems, the contaminated substrates are immersed in the boiling solvents, and ultrasonic baths or brushes may also be used to further improve the cleaning capabilities.

The washing of rosin-based fluxes offers advantages and disadvantages. Washed substrates can usually be inserted into racks easier, as there will be no residues on their edges; test probes can make better contact without a rosin layer on the test points, and the removal of the residues makes it easier to visually examine the soldered joints. On the other hand, washing equipment is expensive, and so are the solvents, and some solvents present a health or environmental hazard if not correctly dealt with.

Aqueous Cleaning

For high-volume production, special machines have been developed in which the substrates are conveyor-fed through the various stages of spraying, washing, rinsing, and drying. The final rinse water is blown from the substrates to prevent any deposits from the water being left on the substrate.

Where water-soluble fluxes have been used in the soldering process, substrate cleaning is mandatory. For the rosin-based fluxes, it is optional, and is often at the discretion of the customer.

Conformal Coatings

A conformal, or protective coating on the substrate, applied at the end of processing, prevents or minimizes the effects of humidity and protects the substrate from contamination by airborne dust particles. Substrates that are to be provided with a conformal coating (dependent on the environmental conditions to which the substrate will be subjected) must first be washed.

Environmental and Ecological Aspects of Fluxes and Solvents

Fumes and vapors produced during soldering processes, or during cleaning, will not, under normal circumstances, present a health hazard, if relevant health and safety regulations are observed.

Fumes originating from colophony can cause respiratory problems, so an efficient fume-extraction system is essential. The extraction system must cover the fluxing, preheating, and soldering stations, remain operational for at least one hour after machine shutdown, and conform to local regulations. Today, the problem of noxious fumes is unlikely to concern the cleaning station, as all commercial systems are equipped to condense the vapors back into the system. In the future, however, it can be expected that a much lower degree of escape of noxious fumes from any system will be allowed, and all systems may have to be reviewed.

Certain fluxes, particularly some water-soluble ones, contain highly aggressive substances, and must not be allowed to come into contact with the skin or eyes. Any contamination should immediately be removed with plenty of clean, fresh water. Deionized water should also be readily available as an eye-wash. Should contamination occur, a qualified medical practitioner should be consulted. Protective clothing should be worn during cleaning or maintenance of the fluxing station.

Conclusion

SMD technology imposes tougher restraints on fluxing and cleaning of substrate assemblies. Traditionally, rosin-based fluxes have been used in electronic soldering where residues were considered "safe" and could be left on the board. However, increased SMD packing density, fine-line tracks, and more rigid specifications have resulted in changes to this basic philosophy.

There is now a demand for surfaces free from residues; test probes are more efficient when they do not have to penetrate rosin flux residues, and conformal coating and board inspection benefit from the absence of such residues.

Cleaning also poses problems for SMD substrates. The close proximity of component and substrate means that solvents cannot effectively clean beneath devices. Components must also be compatible with the cleaning process. They must, for example, be resistant to the solvents used and to the temperatures of the cleaning process. They must also be sealed to prevent cleaning fluids from entering the devices and degrading performance.

So, eliminating the need for cleaning is better than poor or incomplete cleaning. And in a well-balanced system, mildly-activated rosin-based fluxes, leaving only non-corrosive residues, can be successfully used for SMD substrate soldering without subsequent cleaning.

Much research into fluxes and solder creams is presently being done — for example, the production of synthetic resin, with qualities superior to colophony at a lower cost. Another area of research is that of solder creams with non-melting additives, such as lead or ceramic spheres, that increase the distance

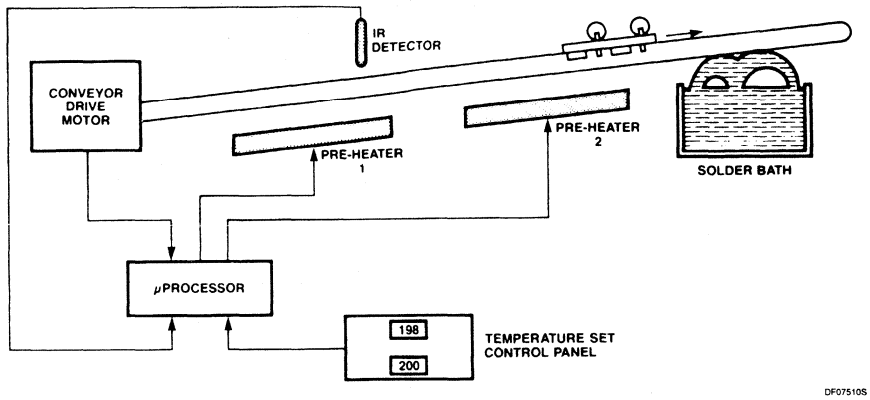


Figure 4. Schematic Diagram of a Typical Controlled Preheat System

Table 2. Substrate Contaminants

Contaminant	Origin
Organic compounds	Fluxes, solder mask
Inorganic insoluble compounds	Photo-resists, substrate processing
Organo-metallic compounds	Fluxes, substrate processing
Inorganic soluble compounds	Fluxes
Particle matter	Dust, fingerprints

between component and substrate, thus making it easier for cleaning fluids to penetrate beneath the component. It also increases the joint's ability to withstand thermal cycling.

Rosin-free and halide-free fluxes are also being developed with similar activities to conventional rosin-based fluxes. These new types will combine the "safety" of rosin fluxes with easier removal in conventional solvents. Using non-polar materials, ionizable or corrosive residues are eliminated, and the need for cleaning immediately after soldering is avoided.

Thermal Considerations for Surface-Mounted Devices

INTRODUCTION

Thermal characteristics of integrated circuit (IC) packages have always been a major consideration to both producers and users of electronics products. This is because an increase in junction temperature (T_J) can have an adverse effect on the long-term operating life of an IC. As will be shown in this section, the advantages realized by miniaturization can often have trade-offs in terms of increased junction temperatures. **Some of the VARIABLES affecting T_J are controlled by the PRODUCER of the IC, while others are controlled by the USER and the ENVIRONMENT in which the device is used.**

With the increased use of Surface-Mount Device (SMD) technology, management of thermal characteristics remains a valid concern, not only because the SMD packages are much smaller, but also because the thermal energy is concentrated more densely on the printed wiring board (PWB). For these reasons, the designer and manufacturer of surface-mount assemblies (SMAs) must be more aware of all the variables affecting T_J.

POWER DISSIPATION

Power dissipation (P_D), varies from one device to another and can be obtained by multiplying V_{CC} Max by typical I_{CC}. Since I_{CC} decreases with an increase in temperature, maximum I_{CC} values are not used.

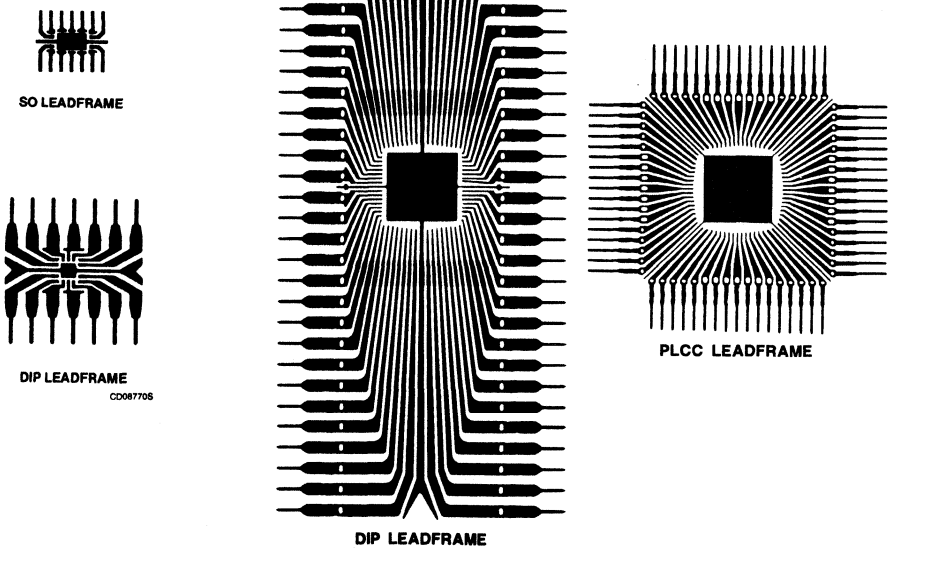
THERMAL RESISTANCE

The ability of the package to conduct this heat from the chip to the environment is expressed in terms of thermal resistance. The term normally used is Theta JA (θ_{JA}). θ_{JA} is often separated into two components: thermal resistance from the junction to case, and the thermal resistance from the case to ambient. θ_{JA} represents the total resistance to heat flow from the chip to ambient and is expressed as follows:

$$\theta_{JC} + \theta_{CA} = \theta_{JA}$$

JUNCTION TEMPERATURE (T_J)

Junction temperature (T_J) is the temperature of a powered IC measured by Signetics at the



a. SO-14 Leadframe Compared to a 14-Pin DIP Leadframe

b. PLCC-68 Leadframe Compared to a 64-Pin DIP Leadframe

Figure 1

substrate diode. When the chip is powered, the heat generated causes the T_J to rise above the ambient temperature (T_A). T_J is calculated by multiplying the power dissipation of the device by the thermal resistance of the package and adding the ambient temperature to the result.

$$T_J = (P_D \times \theta_{JA}) + T_A$$

FACTORS AFFECTING θ_{JA}

There are several factors which affect the thermal resistance of any IC package. Effective thermal management demands a sound understanding of all these variables. Package variables include the leadframe design and materials, the plastic used to encapsulate the device, and, to a lesser extent, other variables such as the die size and die attach methods. Other factors that have a significant impact on the θ_{JA} include the substrate upon which the IC is mounted, the density of the layout, the air-gap between the package and the substrate, the number and length of traces on the board, the use of thermally-conductive epoxies, and external cooling methods.

PACKAGE CONSIDERATIONS

Studies with dual in-line plastic (DIP) packages over the years have shown the value of proper leadframe design in achieving minimum thermal resistance. SMD leadframes are smaller than their DIP counterparts (see Figures 1a and 1b). Because the same die is used in each of the packages, the die-pad, or flag, must be at least as large in the SO as in the DIP.

While the size and shape of the leads have a measurable effect on θ_{JA}, the design factors that have the most significant effect are the die-pad size and the tie-bar size. With design constraints caused by both miniaturization and the need to assemble packages in an automated environment, the internal design of an SMD is much different than in a DIP. However, the design is one that strikes a balance between the need to miniaturize, the need to automate the assembly of the package, and the need to obtain optimum thermal characteristics.

LEAD FRAME MATERIAL is one of the more important factors in thermal management. For years, the DIP leadframes were constructed out of Alloy-42. These leadframes met the producers' and users' specifications in quality and reliability. However, three to five years ago the leadframe material of DIPs was changed from Alloy-42 to Copper (CLF) in order to provide reduced θ_{JA} and extend the reliable temperature-operating range. While this change has already taken place for the DIP, it is still taking place for the SO package. Signetics began making 14-pin SO packages with CLF in April 1984 and completed conversion to CLF for all SO packages by 1985. As is shown in Figures 10 through 14, the change to CLF is producing dramatic results in the θ_{JA} of SO packages. All PLCCs are assembled with copper leadframes.

The MOLDING COMPOUND is another factor in thermal management. The compound used by Signetics and Philips is the same high purity epoxy used in DIP packages (at present, HC-10, Type II). This reduces corrosion caused by impurities and moisture.

OTHER FACTORS often considered are the die-size, die-attach methods, and wire bonding. Tests have shown that die size has a minor effect on θ_{JA} (see Figures 10 through 14).

While there is a difference between the thermal resistance of the silver-filled adhesive used for die attach and a gold silicon eutectic die attach, the thickness of this layer (1 – 2 mils) is so small it makes the difference insignificant.

Gold-wire bonding in the range of 1.0 to 1.3 mils does not provide a significant thermal path in any package.

In summary, the SMD leadframe is much smaller than in a DIP and, out of necessity, is designed differently; however, the SMD package offers an adequate θ_{JA} for all moderate power devices. Further, the change to CLF will reduce the θ_{JA} even more, lowering the T_J and providing an even greater margin of reliability.

SIGNETICS' THERMAL RESISTANCE MEASUREMENTS — SMD PACKAGES

The graphs illustrated in this application note show the thermal resistance of Signetics' SMD devices. These graphs give the relationship between θ_{JA} (junction-to-ambient) or θ_{JC} (junction-to-case) and the device die size. Data is also provided showing the difference between still air (natural convection cooling) and air flow (forced cooling) ambients. All θ_{JA} tests were run with the SMD device soldered to test boards. It is important to recognize that the test board is an essential part of the test environment and that boards of different sizes, trace layouts, or compositions may give different results from this data. Each SMD user should compare his system to the Signetics test system and determine if the data is appropriate or needs adjustment for his application.

Test Method

Signetics uses what is commonly called the TSP (temperature-sensitive parameter) method. This method meets MIL-STD 883C, Method 1012.1. The basic idea of this method is to use the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power dissipation. The thermal resistance can be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{T_J - T_A}{P_D}$$

Test Procedure

TSP Calibration

The TSP diode is calibrated using a constant-temperature oil bath and constant-current power supply. The calibration temperatures used are typically 25°C and 75°C and are measured to an accuracy of ±0.1°C. The calibration current must be kept low to avoid significant junction heating; data given here used constant currents of either 1.0mA or 3.0mA. The temperature coefficient (K-Factor) is calculated using the following equation:

$$K = \frac{T_2 - T_1}{V_{F2} - V_{F1}} \Bigg| \; I_F = \text{Constant}$$

Where: K = Temperature Coefficient (°C/mV)
T_2 = Higher Test Temperature (°C)
T_1 = Lower Test Temperature (°C)
V_{F2} = Forward Voltage at I_F and T_2
V_{F1} = Forward Voltage at I_F and T_1
I_F = Constant Forward Measurement Current
(See Figure 2)

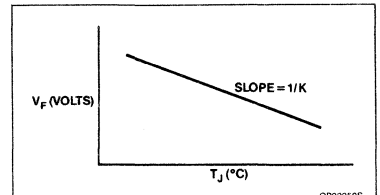


Figure 2. Forward Voltage — Junction Temperature Characteristics of a Semiconductor Junction Operating at a Constant Current. The K Factor is the Reciprocal of the Slope

Thermal Resistance Measurement

The thermal resistance is measured by applying a sequence of constant current and constant voltage pulses to the device under test. The constant current pulse (same current at which the TSP was calibrated) is used to measure the forward voltage of the TSP. The constant voltage pulse is used to heat the part. The measurement pulse is very short

(less than 1% of cycle) compared to the heating pulse (greater than 99% of cycle) to minimize junction cooling during measurement. This cycle starts at ambient temperature and continues until steady-state conditions are reached. The thermal resistance can then be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{K(V_{FA} - V_{FS})}{V_H \times I_H}$$

Where: V_{FA} = Forward Voltage of TSP at Ambient Temperature (mV)

V_{FS} = Forward Voltage of TSP at Steady-State Temperature (mV)

V_H = Heating Voltage (V)

I_H = Heating Current (A)

Test Ambient

θ_{JA} Tests

All θ_{JA} test data collected in this application note was obtained with the SMD devices soldered to either Philips SO Thermal Resistance Test Boards or Signetics PLCC Thermal Resistance Test Boards with the following parameters:

Board size — SO Small
1.12" × 0.75" × 0.059"
— SO Large:
1.58" × 0.75" × 0.059"
— PLCC:
2.24" × 2.24" × 0.062"

Board Material — Glass epoxy, FR-4 type with 1oz. sq.ft. copper solder coated

Board Trace Configuration — See Figure 3.

SO devices are set at 8 - 9mil stand-off and SO boards use one connection pin per device lead. PLCC boards generally use 2 - 4 connection pins regardless of device lead count. Figure 5 shows a cross-section of an SO part soldered to test board, and Figure 4 shows typical board/device assemblies ready for θ_{JA} Test.

The still-air tests were run in a box having a volume of 1 cubic foot of air at room temperature. The air-flow tests were run in a 4" × 4" cross-section by 26" long wind tunnel with air at room temperature. All devices were soldered on test boards and held in a horizontal test position. The test boards were held in a Textool ZIF socket with 0.16" stand-off. Figure 6 shows the air-flow test setup.

θ_{JC} Tests

The θ_{JC} test is run by holding the test device against an "infinite" heat sink (water-cooled block approximately 4" × 7" × 0.75") to give a θ_{CA} (case-to-ambient) approaching zero. The copper heat sink is held at a constant temperature (≈20°C) and monitored with a thermocouple (0.040" diameter sheath, grounded junction type K) mounted flush with heat-sink surface and centered below die in the test device. Figure 7 shows the θ_{JC} test mounting for a PLCC device.

SO devices are mounted with the bottom of the package held against the heat sink. This is achieved by bending the device leads straight out from the package body. Two small wires are soldered to the appropriate leads for tester connection. Thermal grease is used between the test device and heat sink to assure good thermal coupling.

PLCC devices are mounted with the top of the package held against the heat sink. A small spacer is used between the hold-down mechanism and PLCC bottom pedestal. Small hook-up wires and thermal grease are used as with the SO setup. Figure 7 shows the PLCC mounting.

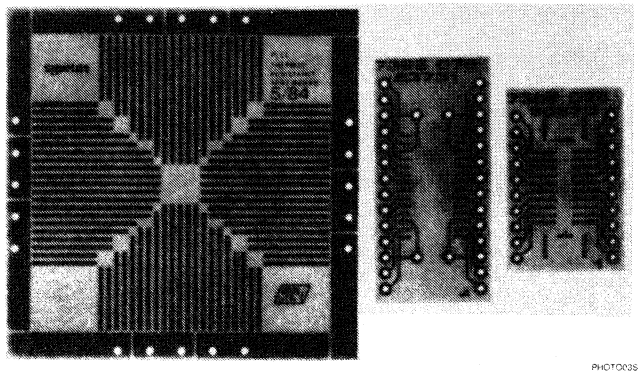


Figure 3. Board Trace Configuration for Thermal Resistance Test Boards

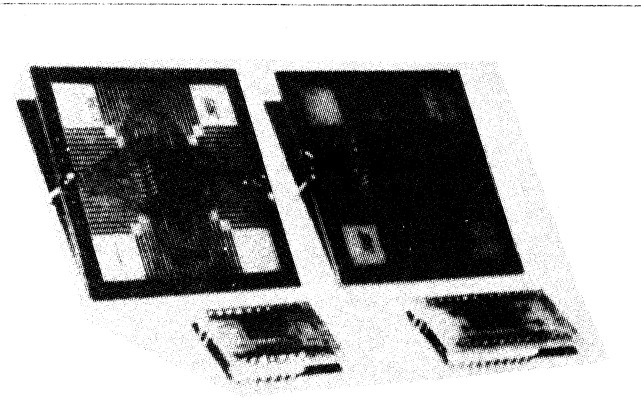


Figure 4. Device/Board Assemblies

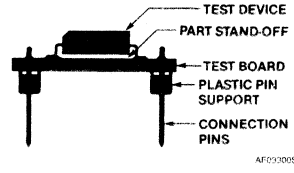
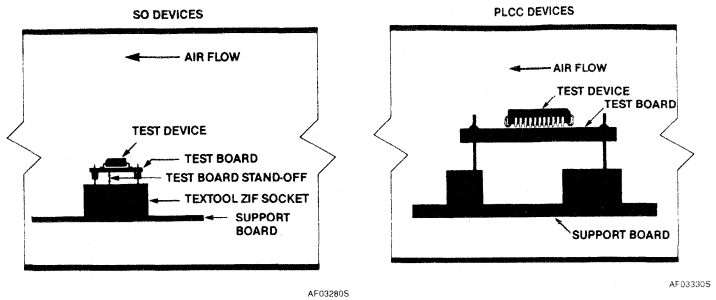


Figure 5. Cross-Section of Test Device Soldered to Test Board



SO Devices PLCC Devices

Figure 6. Air-Flow Test Setup

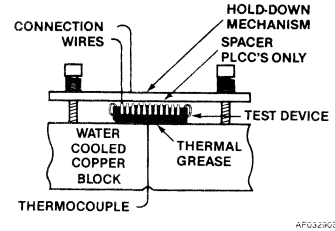


Figure 7. θ_{JC} Test Setup With PLCC Device

DATA PRESENTATION

The data presented in this application note was run at constant power dissipation for each package type. The power dissipation used is given under Test Conditions for each graph. Higher or lower power dissipation will have a slight effect on thermal resistance. The general trend of thermal resistance decreasing with increasing power is common to all packages. Figure 8 shows the average effect of power dissipation on SMD θ_{JA}.

Thermal resistance can also be affected by slight variations in internal leadframe design such as pad size. Larger pads give slightly lower thermal resistance for the same size die. The data presented represents the typical Signetics leadframe/die combinations with large die on large pads and small die on small pads. The effect of leadframe design is within the ±15% accuracy of these graphs.

SO devices are currently available in both copper or alloy 42 leadframes; however, Signetics is converting to copper only. PLCC devices are only available using copper leadframes.

The average lowering effect of air flow on SMD θ_{JA} is shown in Figure 9.

Thermal Calculations

The approximate junction temperature can be calculated using the following equation:

$$T_J = (\theta_{JA} \times P_D) + T_A$$

Where: T_J = Junction Temperature (°C)

θ_{JA} = Thermal Resistance Junction-to-Ambient (°C/W)

P_D = Power Dissipation at a T_J ($V_{CC} \times I_{CC}$) (W)

T_A = Temperature of Ambient (°C)

Example: Determine approximate junction temperature of SOL-20 at 0.5W dissipation using 10,000 sq. mil die and copper leadframe in still air and 200 LFPM air-flow ambients. Given T_A = 30°C,

1. Find θ_{JA} for SOL-20 using 10,000 sq. mil die and copper leadframe from typical θ_{JA} data — SOL-20 graph.

   Answer: 88°C/W @ 0.7W

2. Determine θ_{JA} @ 0.5W using Average Effect of Power Dissipation on AMD θ_{JA}, Figure 8.

   Percent change in Power

   $$= \frac{0.5W - 0.7W}{0.7W} \times 100$$

   $$= -28.6\%$$

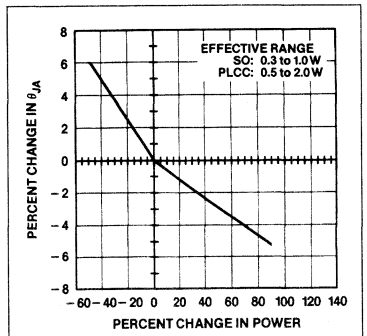


Figure 8. Average Effect of Power Dissipation on SMD θ_{JA}

From Figure 8:
28.6% change in power gives 3.5% increase in θ_{JA}

Answer:
88°C/W + (88 × 0.035)
= 91°C/W @ 0.5W

3. Determine θ_{JA} @ 0.5W in 200 LFPM air flow from Average Effect of Air Flow on SMD θ_{JA}, Figure 9.

From Figure 9: 200 LFPM air flow gives 14% decrease in θ_{JA}

Answer:
91°C/W – (91 × 0.14) = 78°C/W

4. Calculate approximate junction temperature

Answer:
T_J (still-air)
= (91°C/W × 0.5W) + 30
= 76°C
T_J (200 LFPM)
= (78°C/W × 0.5W) + 30
= 69°C

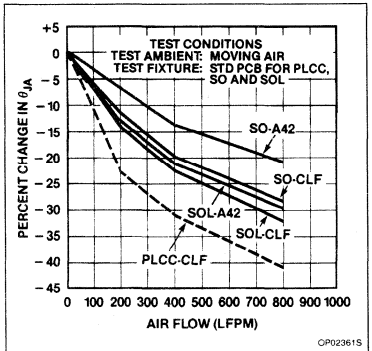
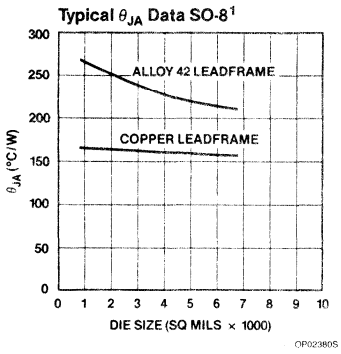
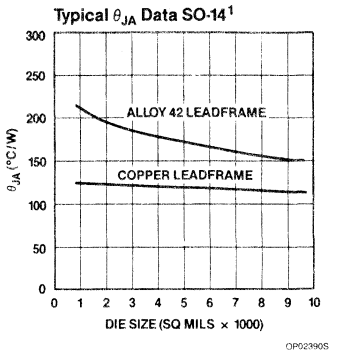
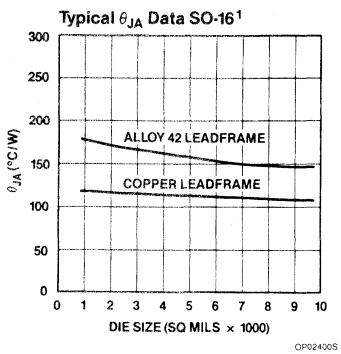
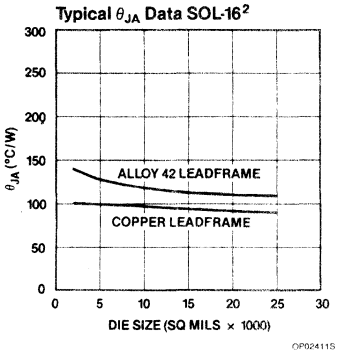


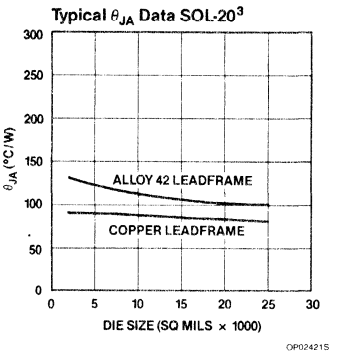
Figure 9. Average Effect of Air Flow on SMD θ_{JA}

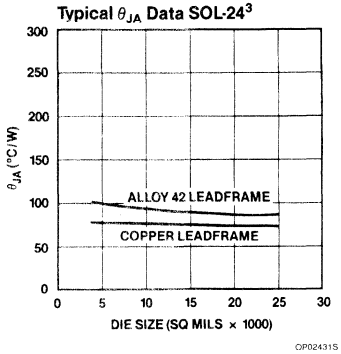


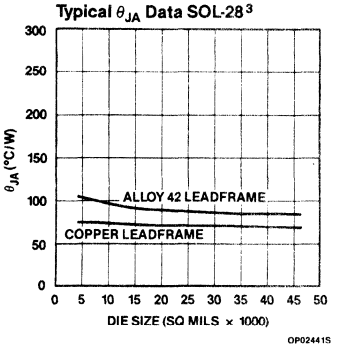












NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.12″ × 0.75″ × 0.059″)
Accuracy:	±15%

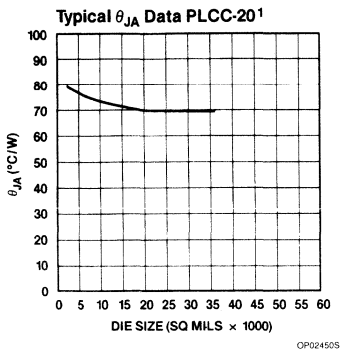
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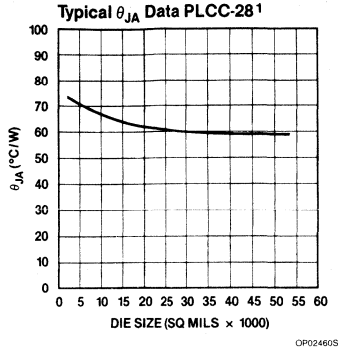
Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.58″ × 0.75″ × 0.059″)
Accuracy:	±15%

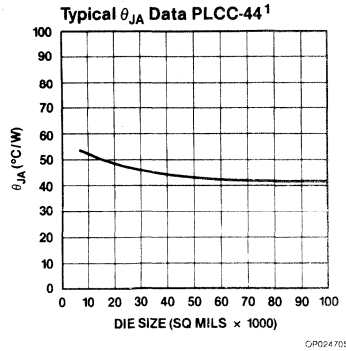
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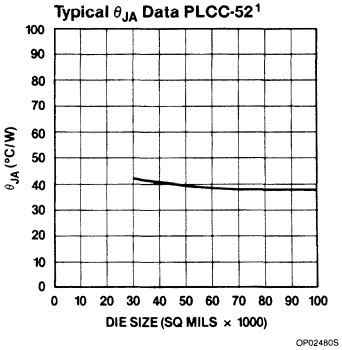
Test ambient:	Still air
Power dissipation:	0.7W
Test fixture:	Philips PCB (1.58″ × 0.75″ × 0.059″)
Accuracy:	±15%

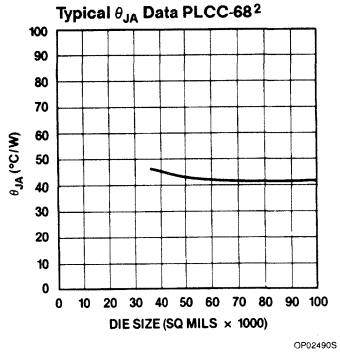
Figure 10. Typical SMD Thermal (θ_{JA}) Characteristics

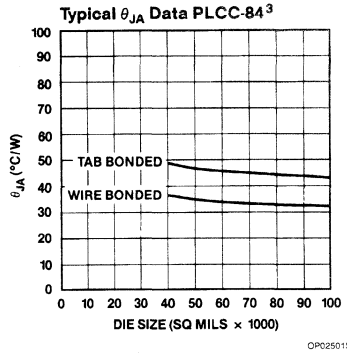












NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.75W
Test fixture:	Signetics PCB (2.24″ × 2.24″ × 0.062″)
Accuracy:	±15%

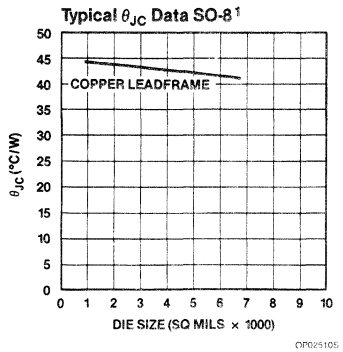
2. TEST CONDITIONS:

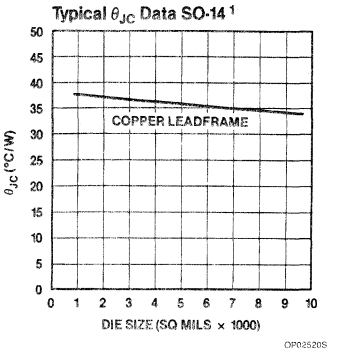
Test ambient:	Still air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24″ × 2.24″ × 0.062″)
Accuracy:	±15%

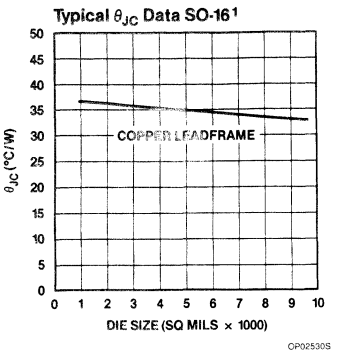
3. TEST CONDITIONS:

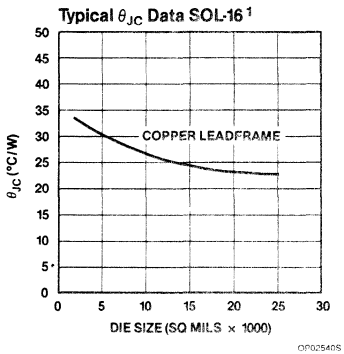
Test ambient	Still air
Power dissipation:	1.5W
Test fixture:	Signetics PCB (2.24″ × 2.24″ × 0.062″)
Accuracy:	±15%

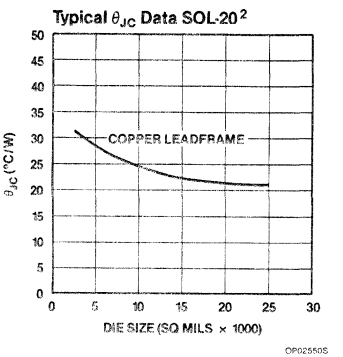
Figure 11. Typical SMD Thermal (θ_{JA}) Characteristics

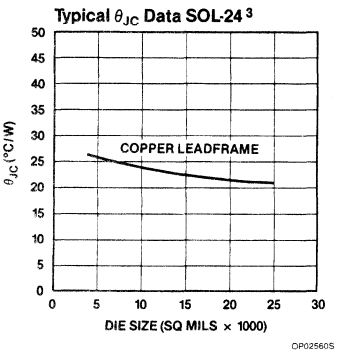


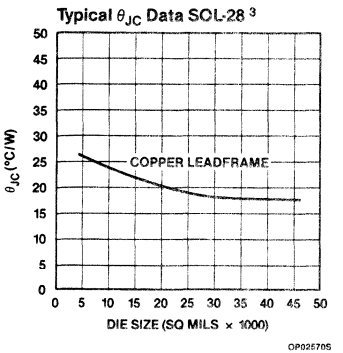












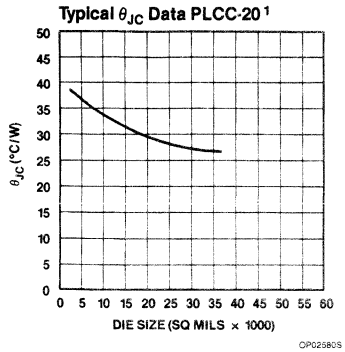
NOTES:

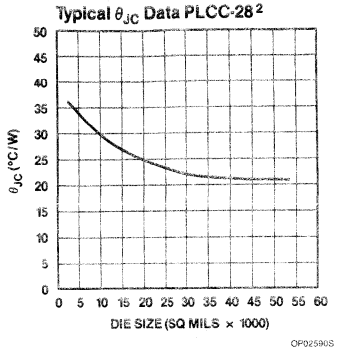
1. TEST CONDITIONS:
Power dissipation: 0.5W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

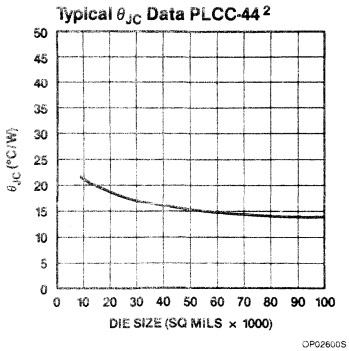
2. TEST CONDITIONS:
Power dissipation: 0.7W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

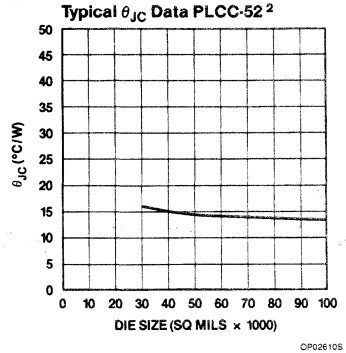
3. TEST CONDITIONS:
Power dissipation: 1.0W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

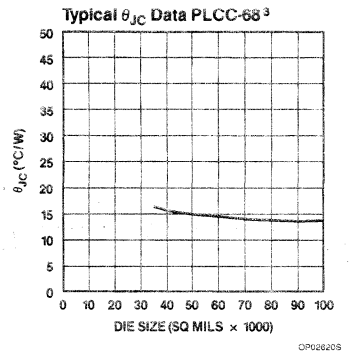
Figure 12. Typical SMD Thermal (θ_{JC}) Characteristics

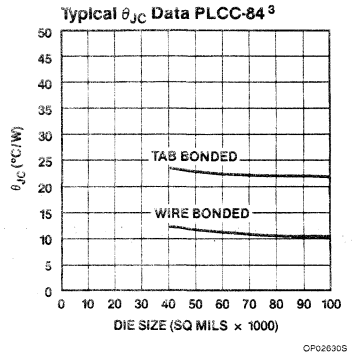












NOTES:

1. TEST CONDITIONS:

Power dissipation:	0.75W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

2. TEST CONDITIONS:

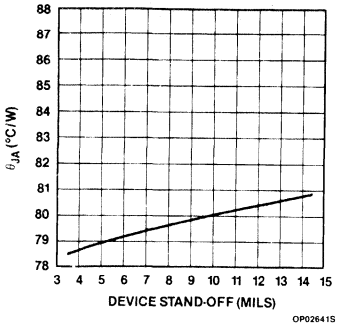
Power dissipation:	1.0W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

3. TEST CONDITIONS:

Power dissipation:	2.0W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

Figure 13. Typical SMD Thermal (θ_{JC}) Characteristics

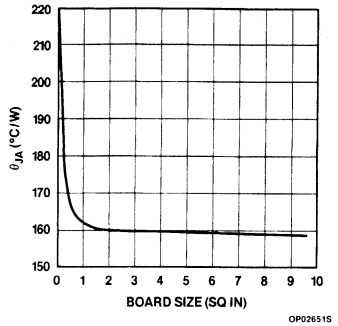
Effect of Device Stand-Off on SO θ_{JA} [1]



NOTES:
1. TEST CONDITIONS

Package type:	SOL-20 CLF
Die size:	11,322sq.mils
Test Ambient:	Still-air
Power dissipation:	0.75W
Test fixture:	Phillips PCB (1.58" × 0.75" × 0.059")

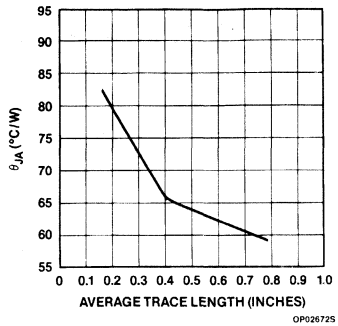
Effect of Board Size on SO θ_{JA} [2]



NOTES:
2. TEST CONDITIONS

Package type:	SOL-14 CLF
Die size:	5,040sq.mils
Test Ambient:	Still-air
Power dissipation:	0.6W
Test fixture:	0.062" thick PCB with "no traces" 8 – 9mil stand-off

Effect of Trace Length on 28-Lead PLCC θ_{JA} [3]



NOTES:
3. TEST CONDITIONS

Package type:	PLCC-28 CLF
Die size:	10,445sq.mils
Test Ambient:	Still-air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062") trace 27mil-wide 1oz sq.ft copper

Figure 14

SYSTEM CONSIDERATIONS

With the increases in layout density resulting from surface mounting with much smaller packages, other factors become even more important. THE USER IS IN CONTROL OF THESE FACTORS.

One of the most obvious factors is the substrate material on which the parts are mounted. Environmental constraints, cost considerations, and other factors come into play when choosing a substrate. The choice is expanding rapidly, from the standard glass epoxy PWB materials and ceramic substrates to flexible circuits, injection-molded plastics, and coated metals. Each of these has its own thermal characteristics which must be considered when choosing a substrate material.

Studies have shown that the air gap between the bottom of the package and the substrate has an effect on θ_{JA}. The larger the gap, the higher the θ_{JA}. Using thermally conductive epoxies in this gap can slightly reduce the θ_{JA}.

It has long been recognized that external cooling can reduce the junction temperatures of devices by carrying heat away from both the devices and the board itself. Signetics has done several studies on the effects of external cooling on boards with SO packages. The results are shown in Figures 15 through 18.

The designer should avoid close spacing of high power devices so that the heat load is spread over as large an area as possible. Locate components with a higher junction temperature in the cooler locations on the PCBs.

The number and size of traces on a PWB can affect θ_{JA} since these metal lines can act as radiators, carrying heat away from the package and radiating it to the ambient. Although the chips themselves use the same amount of energy in either a DIP or an SO package, the increased density of a surface-mounted assembly concentrates the thermal energy into a smaller area.

It is evident that nothing is free in PWB layout. More heat concentrated into a smaller area makes it incumbent on the system designer to provide for the removal of thermal energy from his system.

Large conductor traces on the PCB conduct heat away from the package faster than small traces. Thermal vias from the mounting surface of the PCB to a large area ground plane in the PCB reduce the heat buildup at the package.

In addition to the package's thermal considerations, thermal management requires one to at least be aware of potential problems caused by mismatch in thermal expansion.

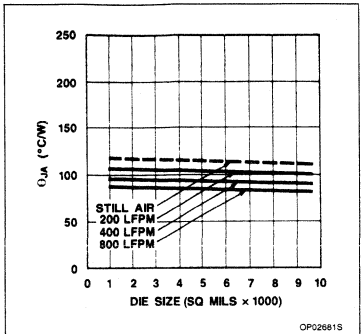


Figure 15. Results of Air Flow on θ_{JA} on SO-14 With Copper Leadframe

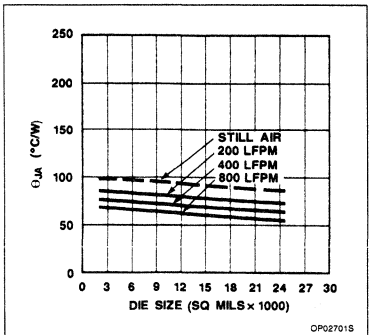


Figure 16. Results of Air Flow on θ_{JA} on SOL-16 With Copper Leadframe

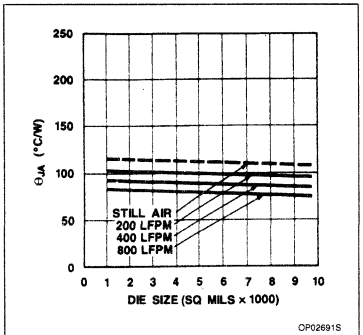


Figure 17. Results of Air Flow on θ_{JA} on SO-16 With Copper Leadframe

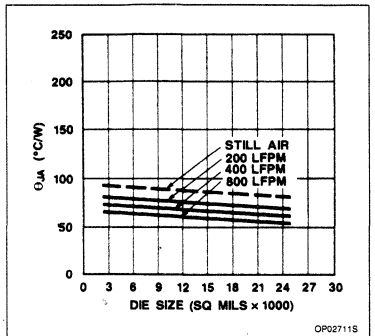


Figure 18. Results of Air Flow on θ_{JA} on SOL-20 With Copper Leadframe

The very nature of the SMD assembly, where the devices are soldered directly onto the surface, not through it, results in a very rigid structure. If the substrate material exhibits a different thermal coefficient of expansion (TCE) than the IC package, stresses can be set up in the solder joints when they are subjected to temperature cycling (and during the soldering process itself) that may ultimately result in failure.

Because some of the boards assembled will require the use of Leadless Ceramic Chip Carriers (LCCCs), TCE must be understood. As will be seen below, TCE is less of a problem with the commercial SMD packages with leads.

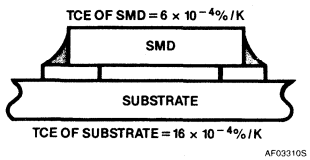
Take the example of a leadless ceramic chip carrier with a TCE of about 6×10^{-6}/°C soldered to a conventional glass-epoxy laminate with a TCE in the region of 16×10^{-6}/°C. This thermal expansion mismatch has been shown to fracture the solder joints during thermal cycling. Substrate materials with matched TCEs should be evaluated for these SMD assemblies to avoid problems caused by thermal expansion mismatch.

The stress level associated with thermal expansion and contraction of small SMDs such as capacitors and resistors, where the actual change in length is small, is normally rather low. However, as component sizes increase, stresses can increase substantially.

Thermal expansion mismatch is unlikely to cause too many problems in systems operating in benign environments; but, in harsher conditions, such as thermal cycling in military or avionic applications, the mechanical stresses set up in solder joints due to the different TCEs of the substrate and the component are likely to cause failure.

The basic problem is outlined in Figure 19. The leadless SMD is soldered to the substrate as shown, resulting in a very rigid structure. If the substrate material exhibits a different TCE from that of the SMD material, the amount of expansion for each will differ for any given increase in temperature. The soldered joint will have to accommodate this difference, and failure can ultimately result. The larger the component size, the higher the stress levels so that this phenomenon is at its

most critical in applications requiring large LCCCs with high pin counts.



NOTE:
Data provided by N.V. Philips

Figure 19. The Basic Problem of Thermal Expansion Mismatch Is That the Substrate and Component May Each Have Different Thermal Coefficients of Expansion

To address this problem, three basic solutions are emerging. First, the use of leadless ceramic chip carriers can sometimes be avoided by using leaded devices; the leads can flex and absorb the stress. Second, when this solution is not feasible, the stresses can be taken up by inserting a compliant elastomeric layer between the ceramic package and the epoxy glass substrate. Third, TCE values of component and substrate can be matched.

USING LEADED DEVICES (SO, SOL, and PLCC)

The current evolution in commercial electronics includes the adoption of the commercial SMD packages, i.e., SO with gull-wing leads or the PLCC with rolled-under J-leads, rely on the compliance of the leads themselves to avoid any serious problems of thermal expansion mismatch. At elevated temperatures, the leads flex slightly and absorb most of the mechanical stress resulting from the thermal expansion differentials.

Similarly, leaded holders can be used with LCCCs to attach them to the substrate and thus absorb the stress.

Unfortunately, using a lead does not always ensure sufficient compliancy. The material from which the lead is made, and the way it is formed and soldered can adversely affect it. For example, improper soldering techniques, which cause excess solder to over-fill the bend of the gull-wing lead of an SO, can significantly reduce the lead's compliancy.

COMPLIANT LAYER

This approach introduces a compliant layer onto the interface surface of the substrate to absorb some of the stresses. A 50μm thick elastomeric layer is bonded to the laminate. To make contacts, carbon or metallic powders are introduced to form conductive stripes in the nonconductive elastomer material. Unfortunately, substrates using this technique are substantially more expensive than standard uncoated boards.

Another solution is to increase the compliancy of the solder joint. This is done by increasing the stand-off height between the underside of the component and the substrate. To do this, a solder paste containing lead or ceramic spheres which do not melt when the surrounding solder reflows, thus keeping the component above the substrate, can be used.

MATCHING TCE

There are two ways to approach this solution. The TCE of the substrate laminate material can be matched to that of the LCCC either by replacing the glass fibers with fibers exhibiting a lower TCE (composites such as epoxy-Kevlar®or polyimide-Kevlar and polyimide-quartz), or by using low TCE metals (such as Invar®, Kovar, or molybdenum).

This latter approach involves bonding a glass-polyimide or a glass-epoxy multilayer to the low TCE restraining core material. Typical of such materials are copper-Invar-copper, Alloy-42, copper-molybdenum-copper, and copper-graphite. These restraining-core constructions usually require that the laminate be bonded to both sides to form a balanced structure so that they will not warp or twist.

This inevitably means an increase in weight, which has always been a negative factor in this approach. However, the SMD substrate can be smaller and the components more densely packed, in many cases overcoming the weight disadvantages. On the positive side, the material's high thermal conductivity helps to keep the components cool. Moreover, copper-clad Invar lends itself readily to moisture-proof multilayering for the creation of ground and power planes and for providing good inherent EMI/RFI shielding.

Kevlar is lighter and widely used for substrates in military applications; but, it suffers from a serious drawback which, although overcome to a certain extent by careful attention to detail, can cause problems. The material, when laminated, can absorb moisture and chemical processing fluids around the edges. Thermal conductivity, machinability, and cost are not as attractive as for copper-clad Invar.

For the majority of commercial substrates, however, where the use of ceramic chip carriers in any quantity is the exception rather than the rule, and when adequate cooling is available, the mismatch of TCEs poses little or no problem. For these substrates, traditional FR-4 glass-epoxy and phenolic-paper will no doubt remain the most widely-used materials.

Although FR-4 epoxy-glass has been the traditional material for plated-through professional substrates, it is phenolic-paper laminate (FR-2) which finds the widest use in consumer electronics. While it is the cheapest material, it unfortunately has the lowest dimensional stability, rendering it unsuitable for the mounting of LCCCs.

SUBSTRATE TYPES

FR-4 glass-epoxy substrates are the most commonly used for commercial electronic circuits. They have the advantage of being cheap, machinable, and lightweight. Substrate size is not limited. On the negative side, they have poor thermal conductivity and a high TCE, between 13 and 17 $\times$ 10^{-6}/°C. This means they are a poor match to ceramic.

Glass polyimide substrates have a similar TCE range to glass-epoxy boards, but better thermal conductivity. They are, however, three to four times more expensive.

Polyimide Kevlar substrates have the advantage of being lightweight and not restricted in size. Conventional substrate processing methods can be used and its TCE (between 4 and 8), matches that of ceramic. Its disadvantages are that it is expensive, difficult to drill, and is prone to resin microcracking and water absorption.

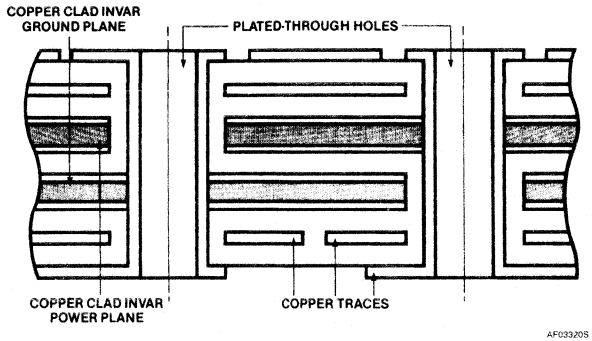
Polyimide quartz substrates have a TCE between 6 and 12, making them a good match for LCCCs. They can be processed using conventional techniques, although drilling vias can be difficult. They have good dielectric properties and compare favorably with FR-4 for substrate size and weight.

Alumina (ceramic) substrates are used extensively for high-reliability military applications and thick-film hybrids. The weight, cost, limited substrate size and inherent brittleness of alumina means that its use as a substrate material is limited to applications where these disadvantages are outweighed by the advantage of good thermal conductivity and a TCE that exactly matches that of LCCCs. A further limitation is that they require thick-film screening processing.

Copper-clad Invar substrates are the leading contenders for TCE control at present. It can be tailored to provide a selected TCE by varying the copper-to-Invar ratio. Figure 20 shows the construction of a typical multilayer substrate employing two cores providing the power and ground planes. Plated-through holes provide an integral board-to-board interconnection. The low TCE of the core dominates the TCE of the overall substrate,

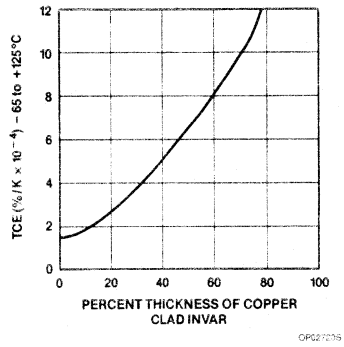
making it possible to mount LCCCs with confidence.

Because the TCE of copper is high, and that of Invar is low, the overall TCE of the substrate can be adjusted by varying the thickness of the copper layers. Figure 21 plots the TCE range of the copper-clad Invar as a function of copper thickness and shows the TCE range of each of several other materials to which the clad material can be matched. For example, if the TCE of Alumina is to be matched, then the core should have about 46% thickness of copper. When this material is used as a thermal mounting plane, it also acts as a heatsink.



NOTE:
Data provided by N.V. Philips

Figure 20. Section Through a Typical Multilayer Substrate Incorporating Copper-Clad Invar Ground and Power Planes, Interconnected via Plated-Through Holes



NOTE:
Data provided by N.V. Philips

Figure 21. The TCE Range of Copper-Clad Invar as a Function of Copper Thickness

Table 1. Substrate Material Properties

SUBSTRATE MATERIAL	TCE (10^{-6}/°C)	THERMAL CONDUCTIVITY (W/m^{3}K)
Glass-epoxy (FR-4)	13 – 17	0.15
Glass polyimide	12 – 16	0.35
Polyimide Kevlar	4 – 8	0.12
Polyimide quartz	6 – 12	TBD
Copper-clad Invar	6.4 (typical)	165 (lateral) 16 (transverse)
Alumina	5 – 7	21
Compliant layer Substrate	See Notes	0.15 – 0.3

NOTES:
Compliant layer conforms to TCE of the LCCC and to base substrate material.
Data provided by N.V. Philips
KEVLAR® is a registered trademark of DU PONT.
INVAR® is a registered trademark of TEXAS INSTRUMENTS.

CONCLUSION

Thermal management remains a major concern of producers and users of ICs. The advent of SMD technology has made a thorough understanding of the thermal characteristics of both the devices and the systems they are used in mandatory. The SMD package, being smaller, does have a higher θ_{JA} than its standard DIP counterpart . . . even with copper leadframes. That is the major trade-off one accepts for package miniaturization. However, consideration of all the variables affecting IC junction temperatures will allow the user to take maximum advantage of the benefits derived from use of this technology.

Package Outlines
For Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC

INTRODUCTION
The following information applies to all packages unless otherwise specified on individual package outline drawings.

GENERAL
1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120mils square die for plastic packages and a 90mils square die in the smallest available cavity for hermetic packages. All units were solder-mounted to PC boards, with standard stand-off, for measurement.

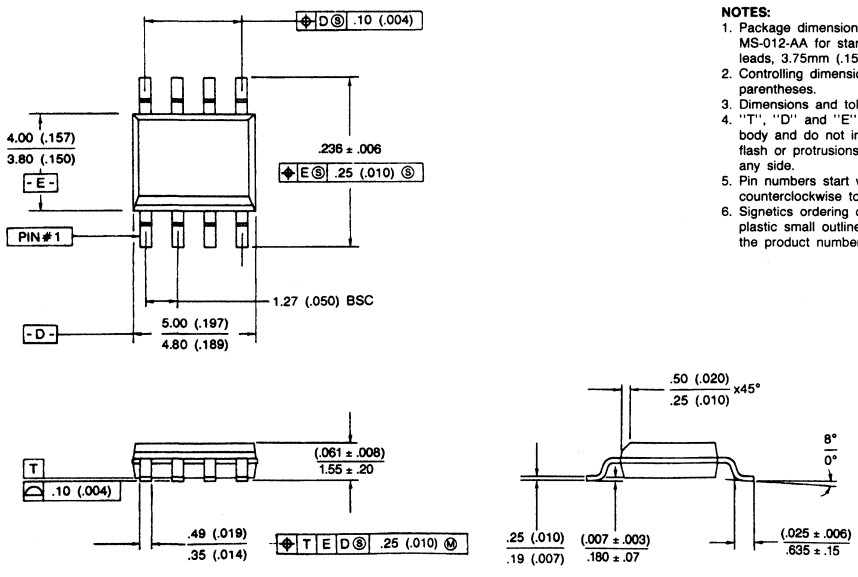
PLASTIC ONLY
5. Lead material: Alloy 42 (Nickel/Iron Alloy), Olin 194 (Copper Alloy), or equivalents, solder-dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO packages/microminiature packages:
   a. Lead material: Alloy-42.
   b. Body material: Plastic (Epoxy).

HERMETIC ONLY
10. Lead material
    a. ASTM alloy F-15 (KOVAR) or equivalent — gold-plated, tin-plated, or solder-dipped.
    b. ASTM alloy F-30 (Alloy 42) or equivalent — tin-plated, gold-plated or solder-dipped.
    c. ASTM alloy F-15 (KOVAR) or equivalent — gold-plated.
11. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent — gold- or tin-plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
12. Lid Material
    a. Nickel- or tin-plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold-plated, alloy seal.
    d. BeO ceramic with glass seal.
13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
14. Recommended minimum offset before lead bend.
15. Maximum glass climb 0.010 inches.
16. Maximum glass climb or lid skew is 0.010 inches.
17. Typical four places.
18. Dimension also applies to seating plane.

PLASTIC PACKAGES

DESCRIPTION	PACKAGE CODE	θ_{JA}/θ_{JC} (°C/W)	PACKAGE TYPE
Standard Dual-in-Line Packages			
8-Pin	N	110/49	
14-Pin	N	90/46	TO-116/MO-001
16-Pin	N	90/46	MO-001
18-Pin	N	79/36	
20-Pin	N	79/35	
22-Pin	N	56/23	
24-Pin	N	58/30	MO-015
28-Pin	N	56/30	MO-015
Metal Headers			
4-Pin	E	100/20	TO-46 Header
4-Pin	E	150/25	TO-72 Header
8-Pin	H	150/25	TO-5 Header
10-Pin	H	150/25	TO-5/TO-100 Header, Short Can
10-Pin	H	150/25	TO-5/TO-100 Header, Tall Can
Cerdip Family			
8-Pin	FE	162/26	Dual-in-Line Ceramic
14-Pin	F	109/26	Dual-in-Line Ceramic
16-Pin	F	105/26	Dual-in-Line Ceramic
18-Pin	F	88/22	Dual-in-Line Ceramic
20-Pin	F	85/22	Dual-in-Line Ceramic
22-Pin	F	75/13	Dual-in-Line Ceramic
24-Pin	F	65/16	Dual-in-Line Ceramic
28-Pin	F	62/16	Dual-in-Line Ceramic
Laminated Ceramic, Side-Brazed Lead			
16-Pin	I	90/25	DIP Laminate

8-PIN PLASTIC SO (D PACKAGE)

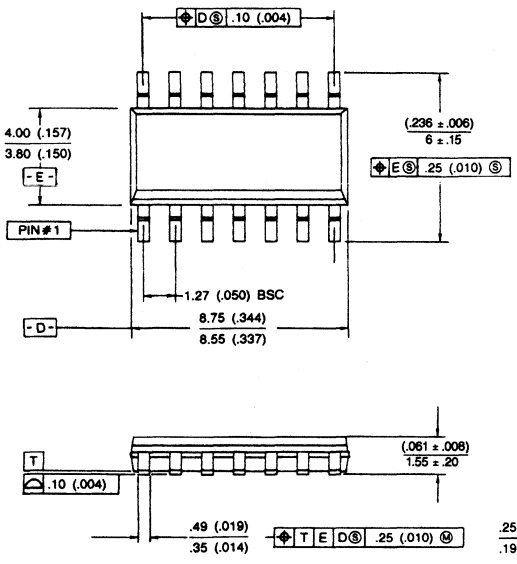


NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

853-0174 88070

PO00273S

14-PIN PLASTIC SO (D PACKAGE)

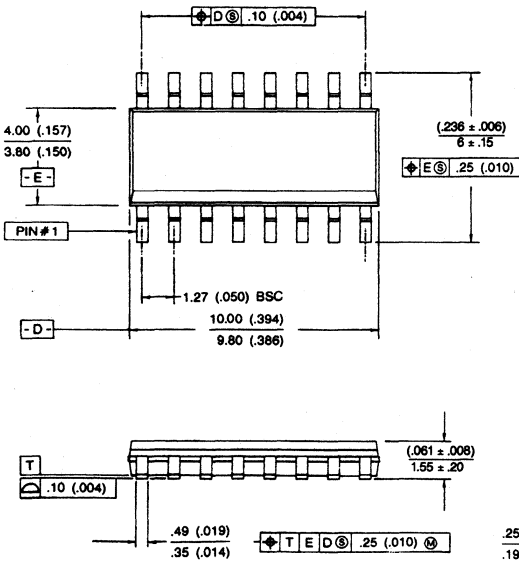


853-0175 88068

PO00263S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SO (D PACKAGE)

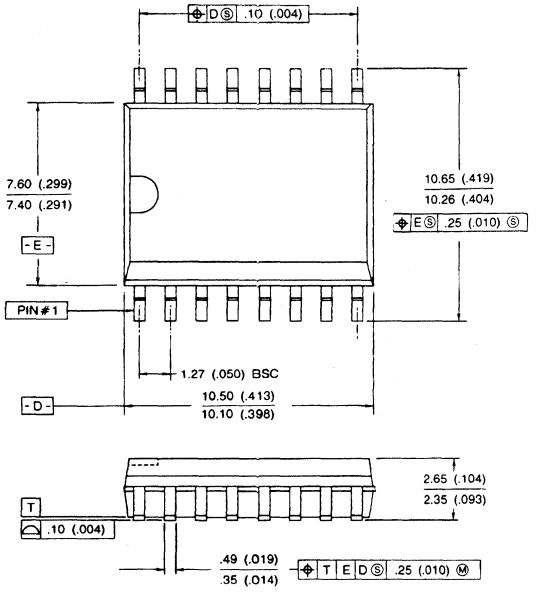


853-0005 88069

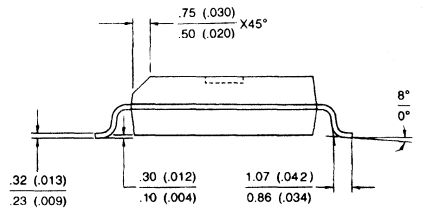
PO00252S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SOL (D PACKAGE)



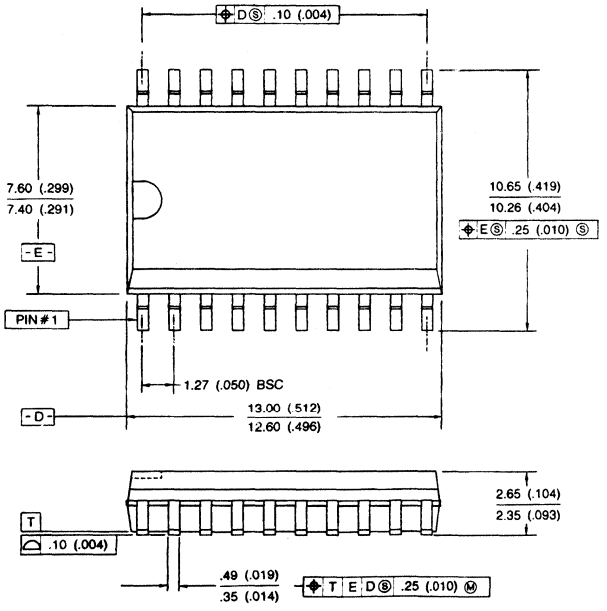
853-0171 81218



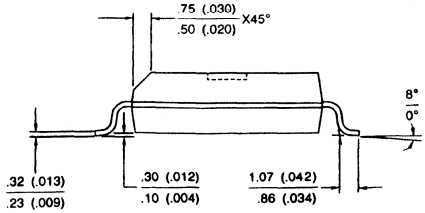
PO00241S

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

20-PIN PLASTIC SOL (D PACKAGE)



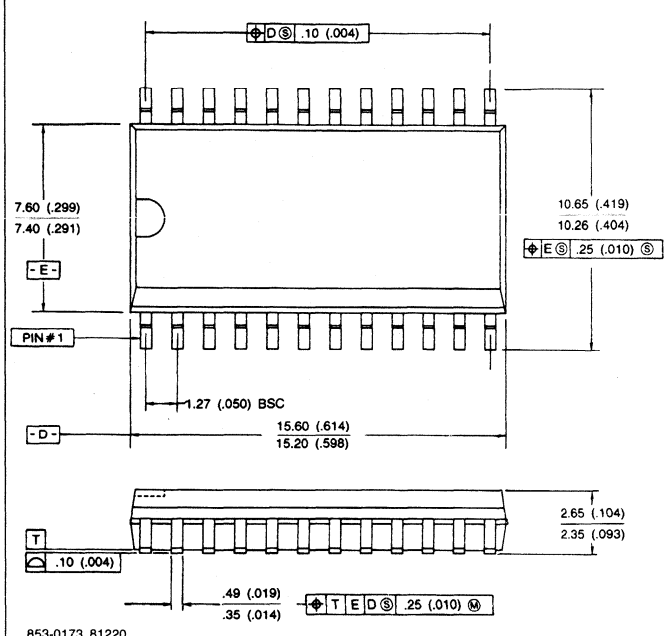
853-0172 81219

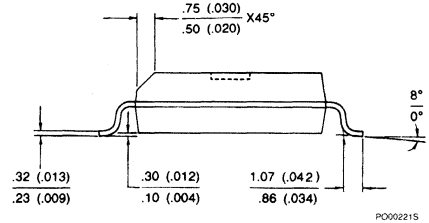


PO00231S

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

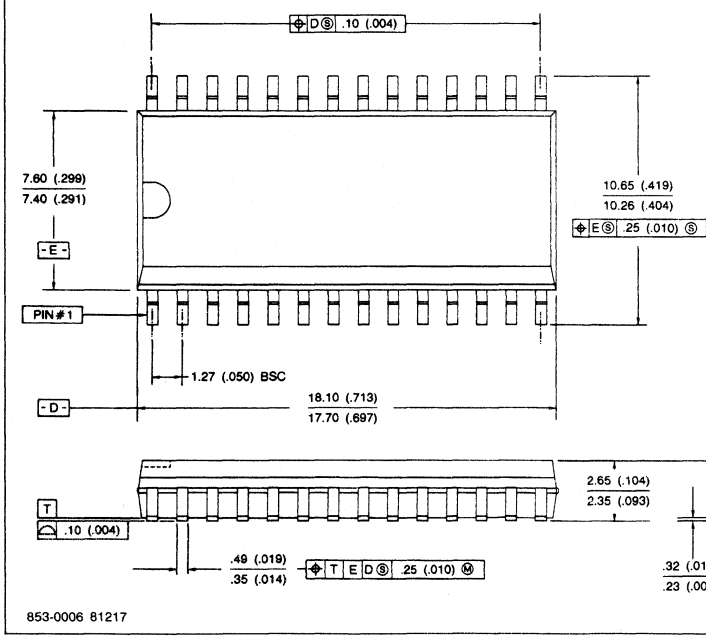
24-PIN PLASTIC SOL (D PACKAGE)

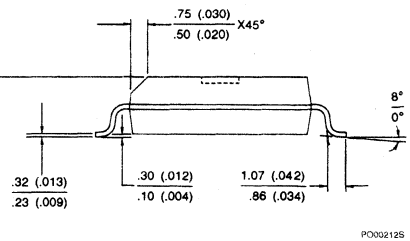




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

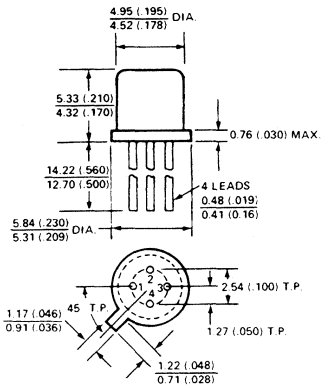
28-PIN PLASTIC SOL (D PACKAGE)



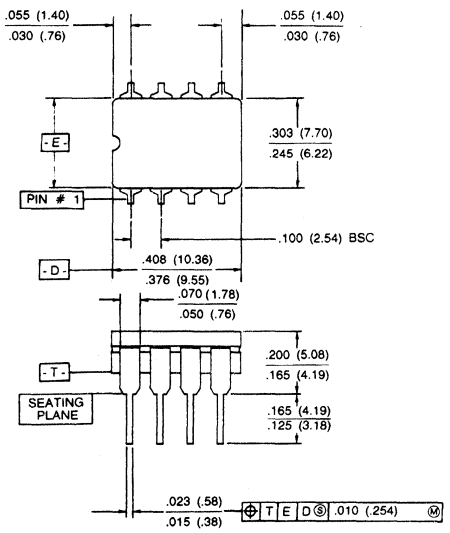


NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

4-PIN HERMETIC TO-72 HEADER (E PACKAGE)

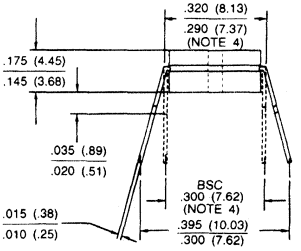


8-PIN CERDIP (FE PACKAGE)



NOTES:

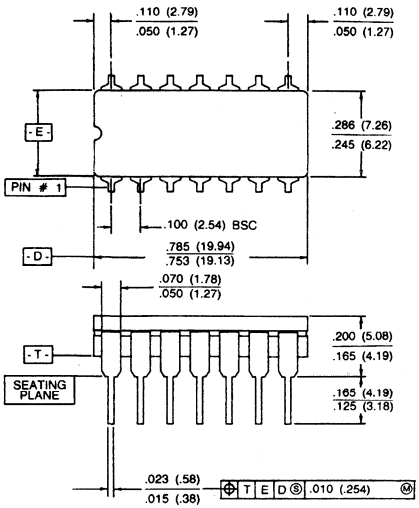
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

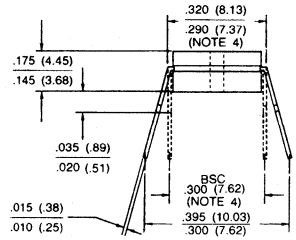


853-0580 81594

PO00480S

14-PIN CERDIP (F PACKAGE)



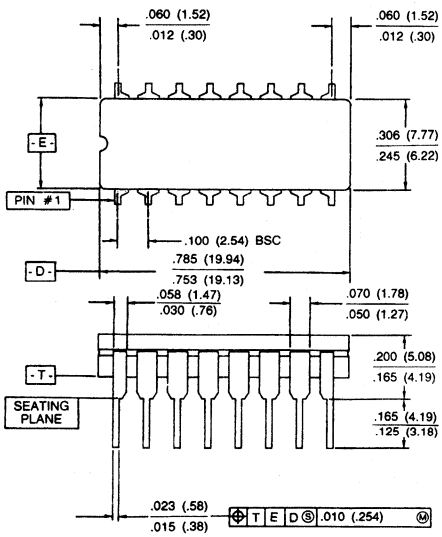


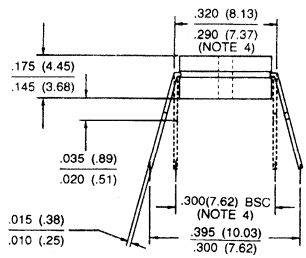
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

853-0581 81594

PO00440S

16-PIN CERDIP (F PACKAGE)



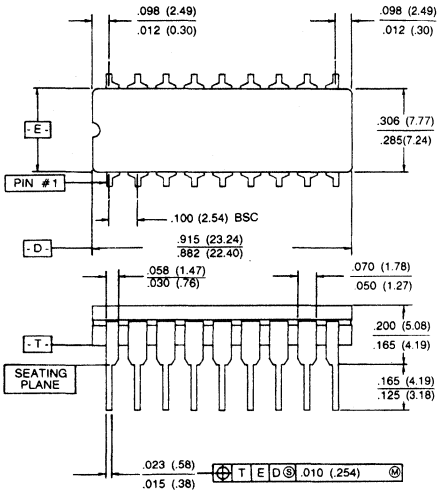


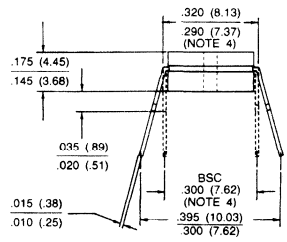
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0582 81594

PO00490S

18-PIN CERDIP (F PACKAGE)



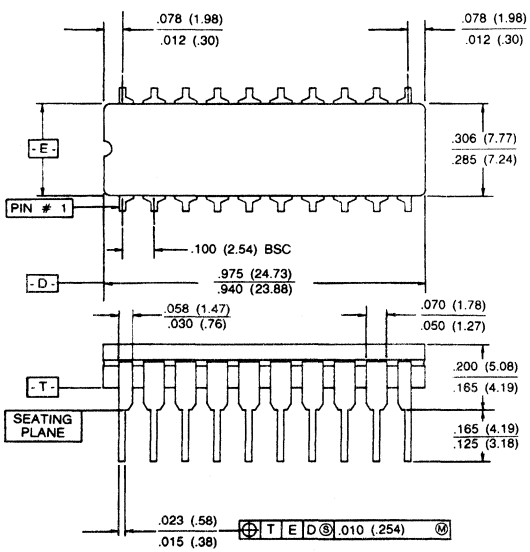


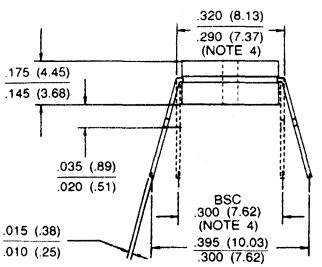
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top.

853-0583 81594

PO00470S

20-PIN CERDIP (F PACKAGE)



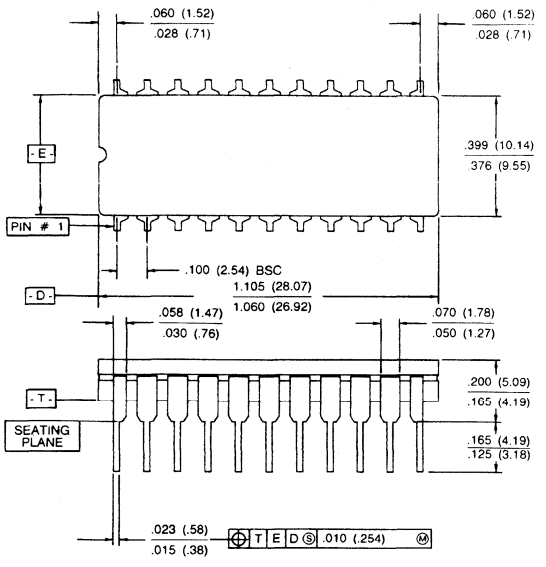


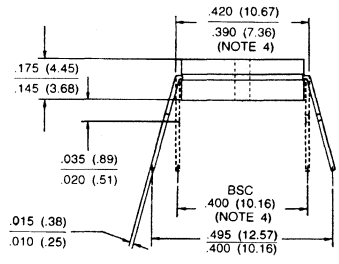
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

853-0584 81594

PO00430S

22-PIN CERDIP (F PACKAGE)



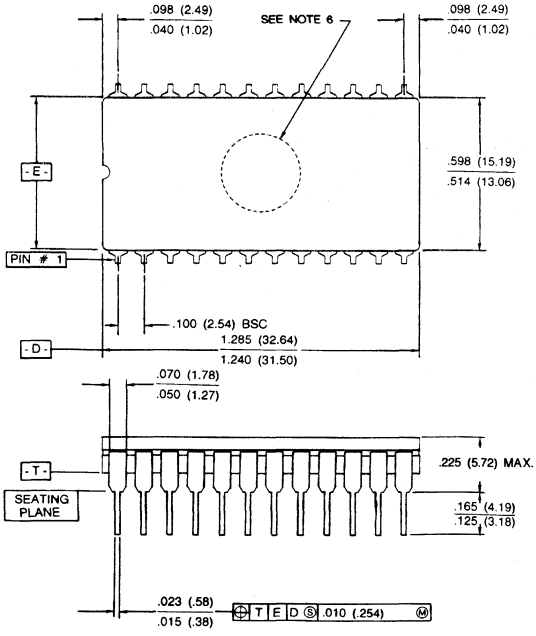


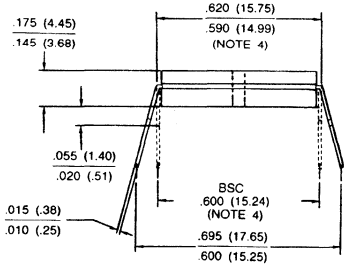
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #22 when viewed from the top.

853-0585 81594

PO00420S

24-PIN CERDIP (F PACKAGE)



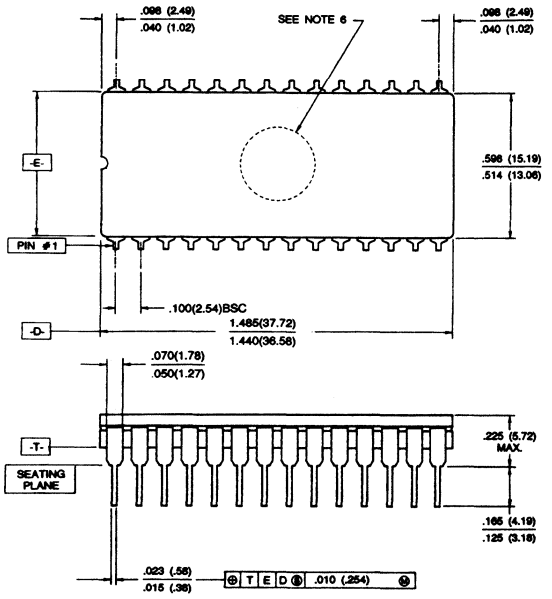


NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0588 84221

PO00464S

28-PIN CERDIP (F PACKAGE)

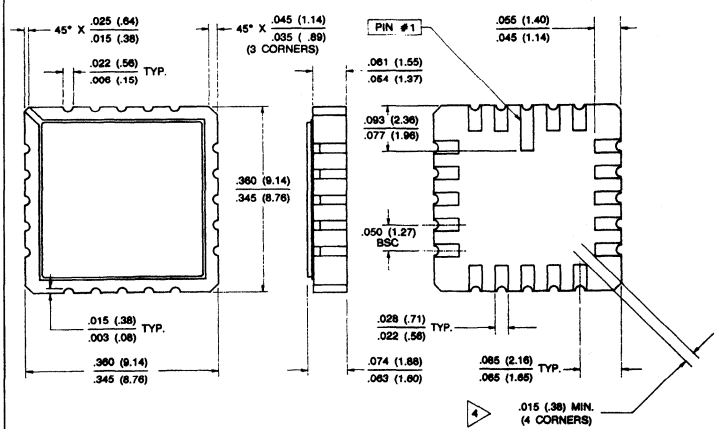


853-0589 84000

PO00660S

NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.
6. Denotes window location for EPROM Products.

20-PIN PGA (G PACKAGE)

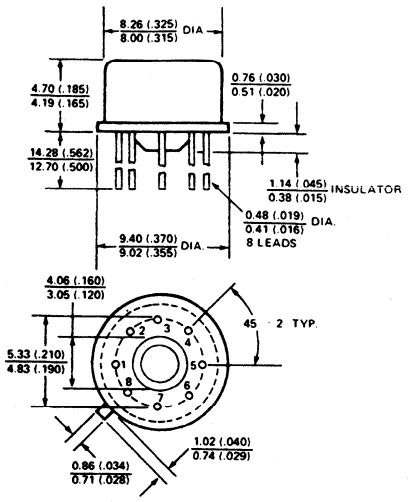


853-0063 82276

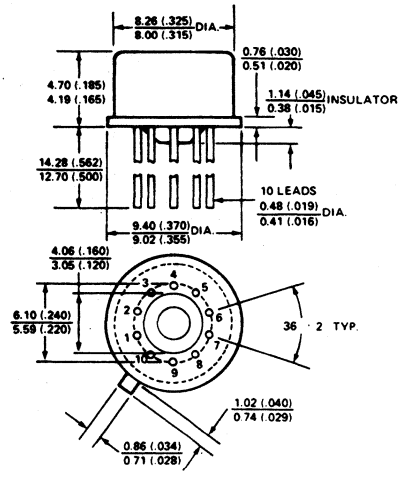
PO00670S

NOTES:
1. Package dimensions conform to Mil-M-38510, outline NO. C – 2, 20 leads, square ceramic leadless chip carrier.
2. Controlling dimension: inches, millimeters are shown in parenthesis.
3. Dimension and tolerancing per ANSI Y14.5M – 1982.
4. This dimension represents the minimum spacing between the corner contact pads. These corner pads may have a .020 inch by 45 degree maximum chamfer to accomplish the .015 minimum spacing.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.
6. Signetics order code for product packaged in a CCCL is the suffix "G" after the product number.

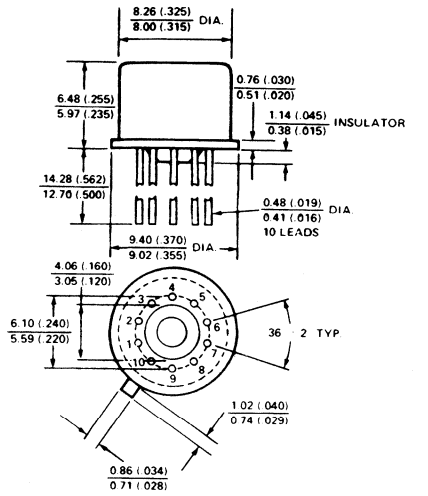
8-PIN HERMETIC TO-5 HEADER (H PACKAGE)



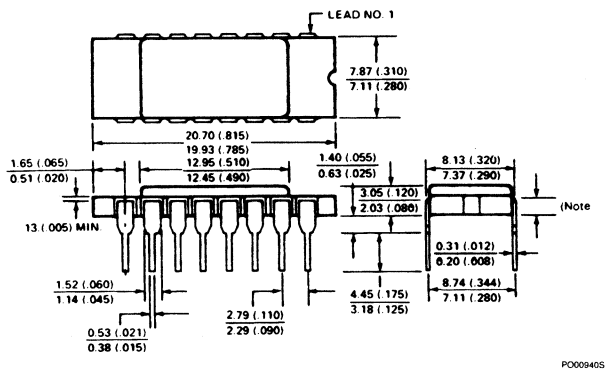
10-PIN HERMETIC TO-5/100 HEADER SHORT CAN (H PACKAGE)



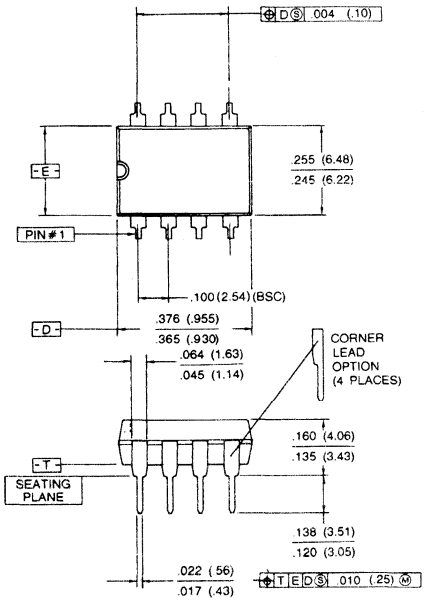
10-PIN HERMETIC TO-5/100 HEADER TALL CAN (H PACKAGE)

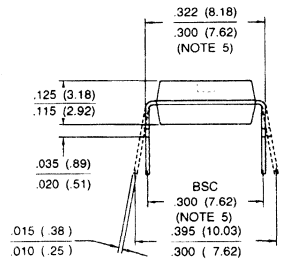


16-PIN HERMETIC SDIP (I PACKAGE)



8-PIN PLASTIC PDIP (N PACKAGE)



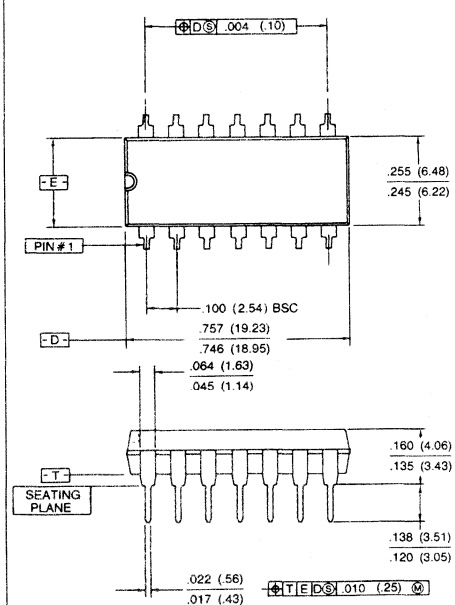


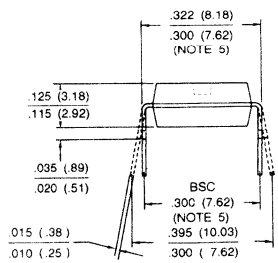
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

853-0404 81230

PO00312S

14-PIN PLASTIC DIP (N PACKAGE)



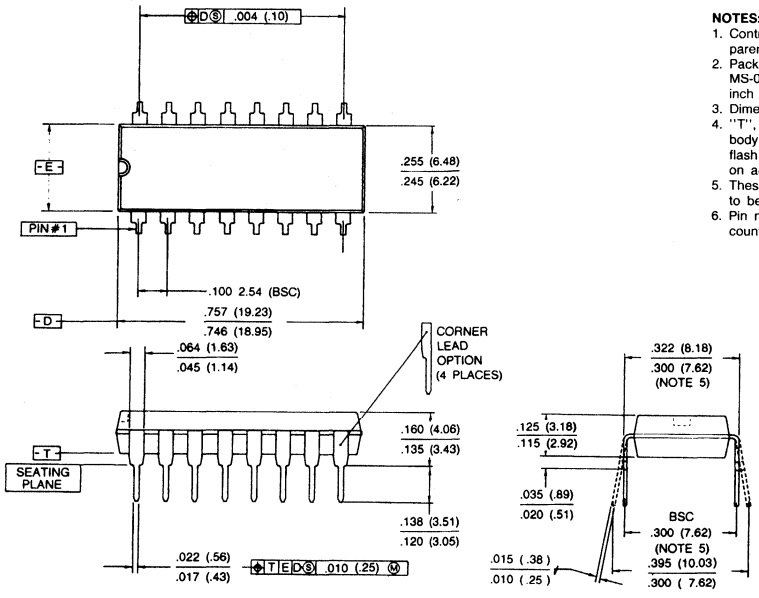


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

853-0405 81231

PO00330S

16-PIN PLASTIC DIP (N PACKAGE)

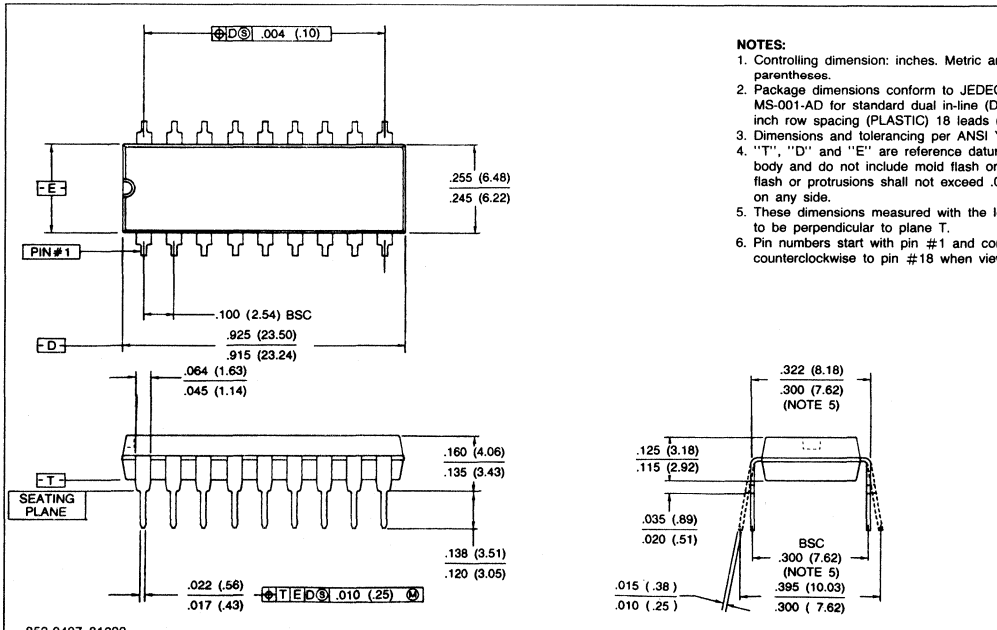


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0406 81232

PO00280S

18-PIN PLASTIC DIP (N PACKAGE)

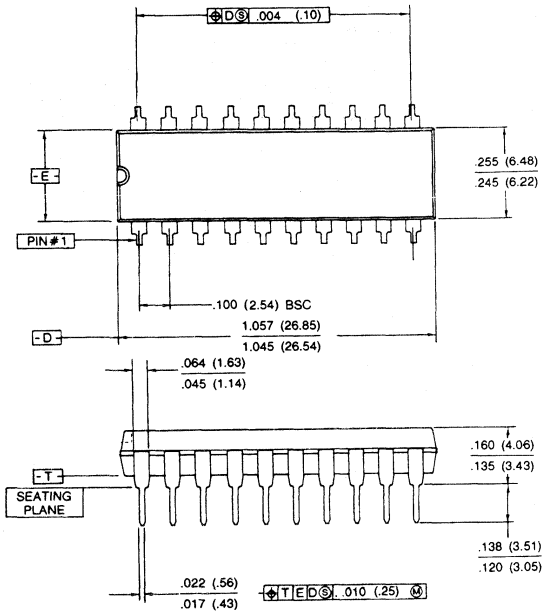


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AD for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 18 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top.

853-0407 81233

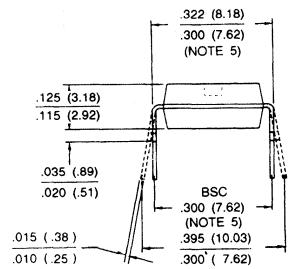
PO00300S

20-PIN PLASTIC DIP (N PACKAGE)



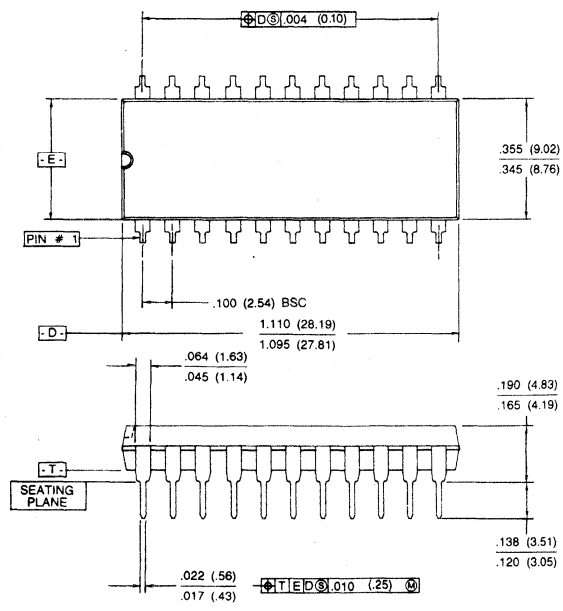
853-0408 81234

NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.



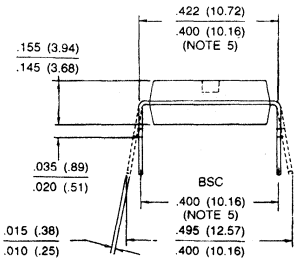
PO00290S

22-PIN PLASTIC DIP (N PACKAGE)



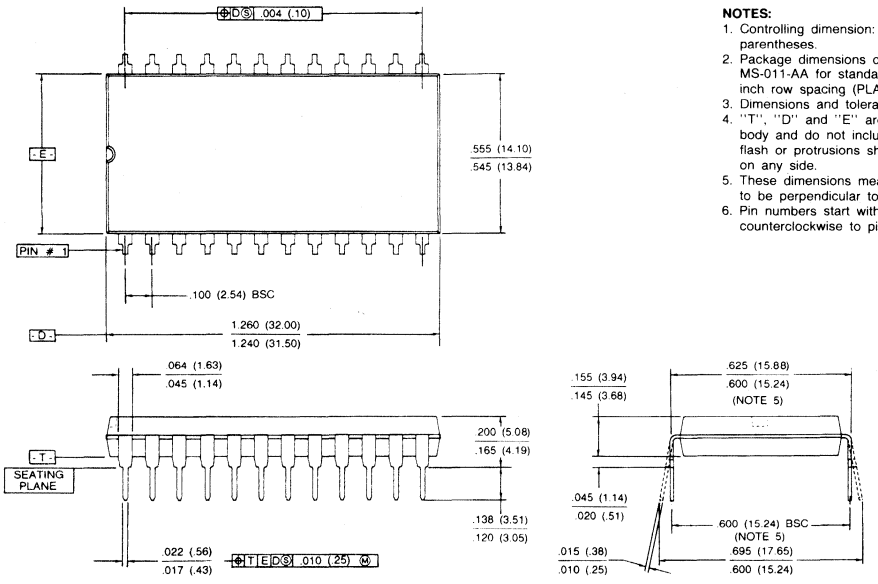
853-0409 81235

NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-010-AA for standard dual in-line (DIP) package .400 inch row spacing (PLASTIC) 22 leads (issue A. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #22 when viewed from the top.



PO00341S

24-PIN PLASTIC DIP (N PACKAGE)

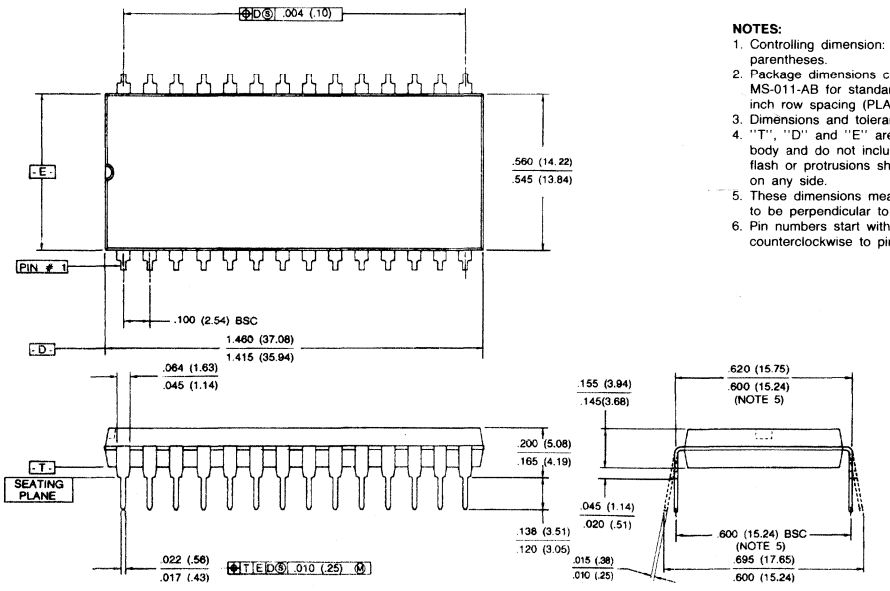


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AA for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0412 81238

PO00361S

28-PIN PLASTIC DIP (N PACKAGE)



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

853-0413 84099

PO00372S

Package Outlines

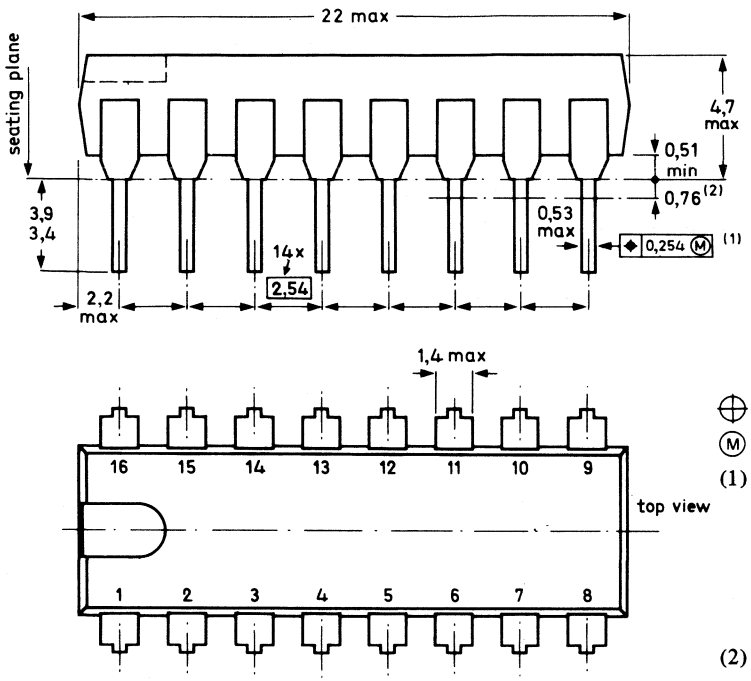
page

Index
for prefixes: MEB, SAA, TCA, TDA and TEA 1615

The package information for each type number is given below:

type number	description and package code	page
MEB3000	28-lead dual in-line; metal ceramic (cerdil) (SOT87B)	1619
SAA1029	16-lead dual in-line; plastic (SOT38)	1617
TCA520B	8-lead dual in-line; plastic (SOT97)	1621
TCA520D	8-lead mini-pack; plastic (SO8; SOT96A)	1620
TDA1023	16-lead dual in-line; plastic (SOT38)	1617
TDA1060	16-lead dual in-line; plastic (SOT38)	1617
TDA1060A	16-lead dual in-line; plastic (SOT38)	1617
TDA1060B	16-lead dual in-line; ceramic (cerdip) (SOT74)	1618
TDA1060T	16-lead mini-pack; plastic (SO16; SOT109A)	1623
TDA5030A	18-lead dual in-line; plastic (SOT102)	1622
TDA5030AT	20-lead mini-pack; plastic (SO20; SOT163A)	1626
TEA1017	18-lead dual in-line; plastic (SOT102)	1622
TEA1039	9-lead single in-line; plastic (SOT110B)	1624
TEA5500	16-lead dual in-line; plastic (SOT38)	1617
TEA5500T	16-lead mini-pack; plastic (SO16L; SOT162A)	1625

16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT38)



Dimensions in mm

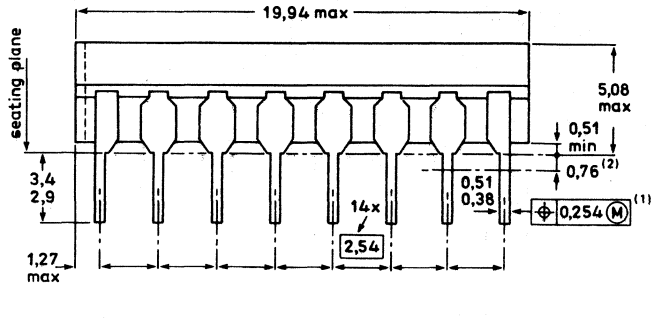
⊕ Positional accuracy.

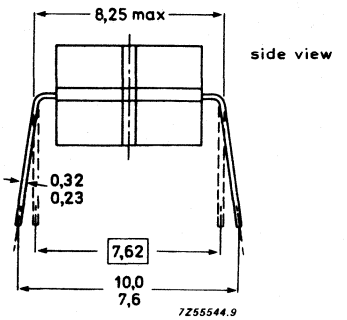
Ⓜ Maximum Material Condition.

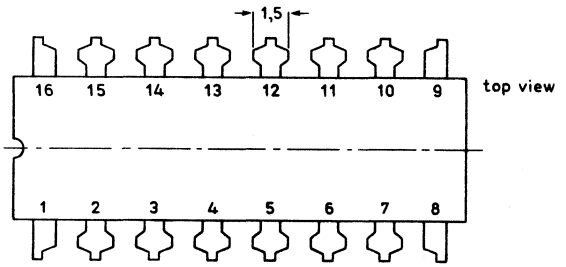
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT74)







Dimensions in mm

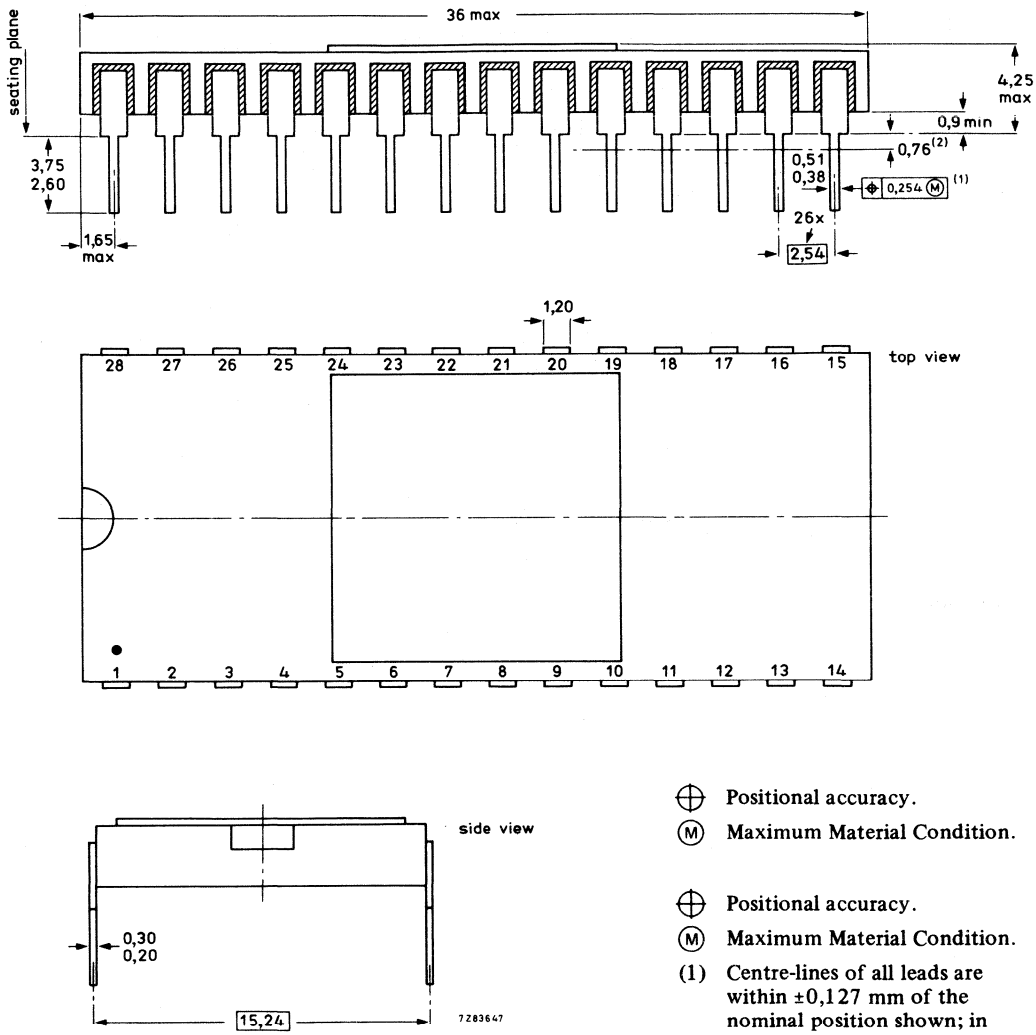
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

28-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT87B)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

⊕ Positional accuracy.

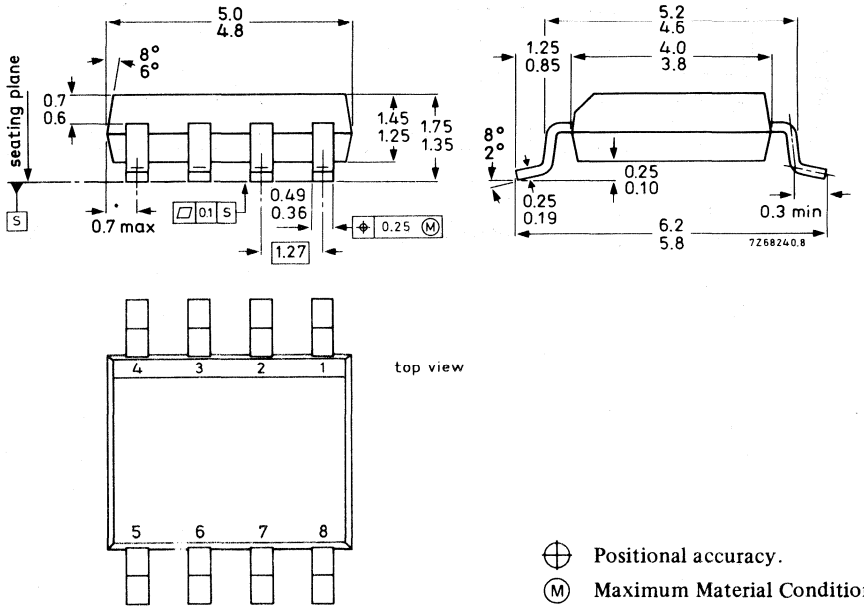
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8; SOT96A)

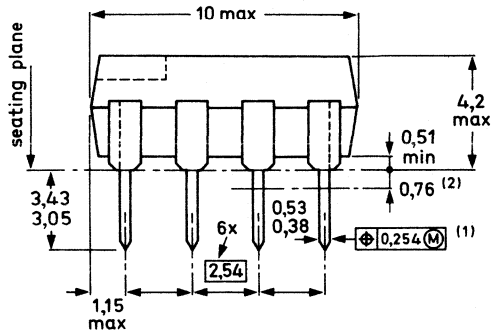


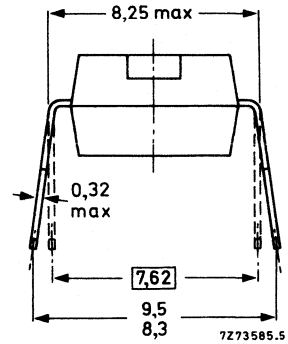
⊕ Positional accuracy.

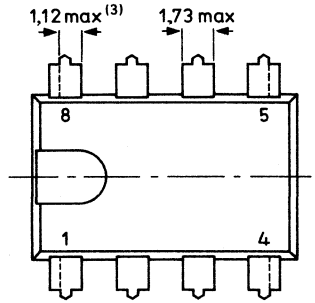
Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)







⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

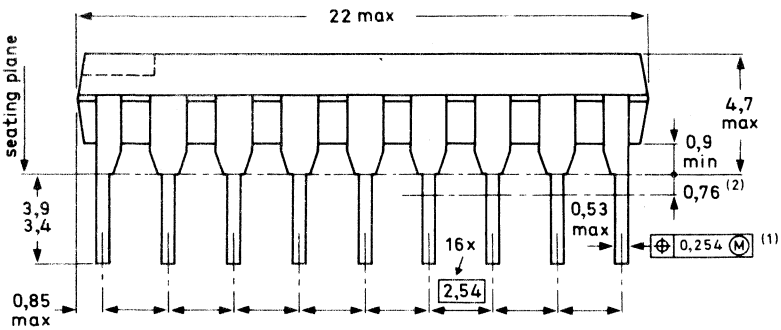
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

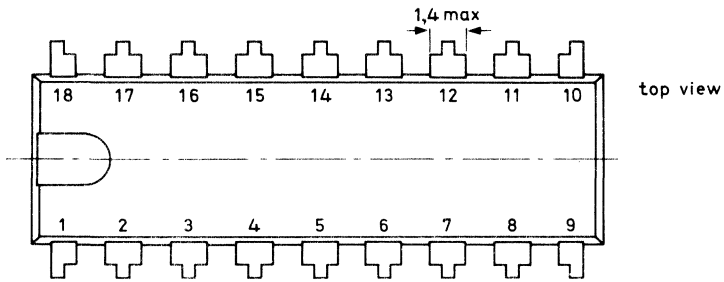
(2) Lead spacing tolerances apply from seating plane to the line indicated.

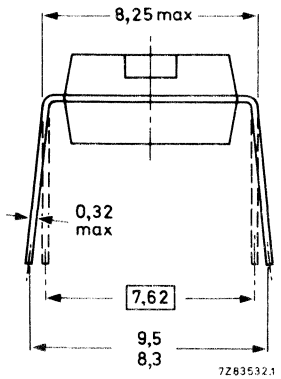
(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT102)







⊕ Positional accuracy.

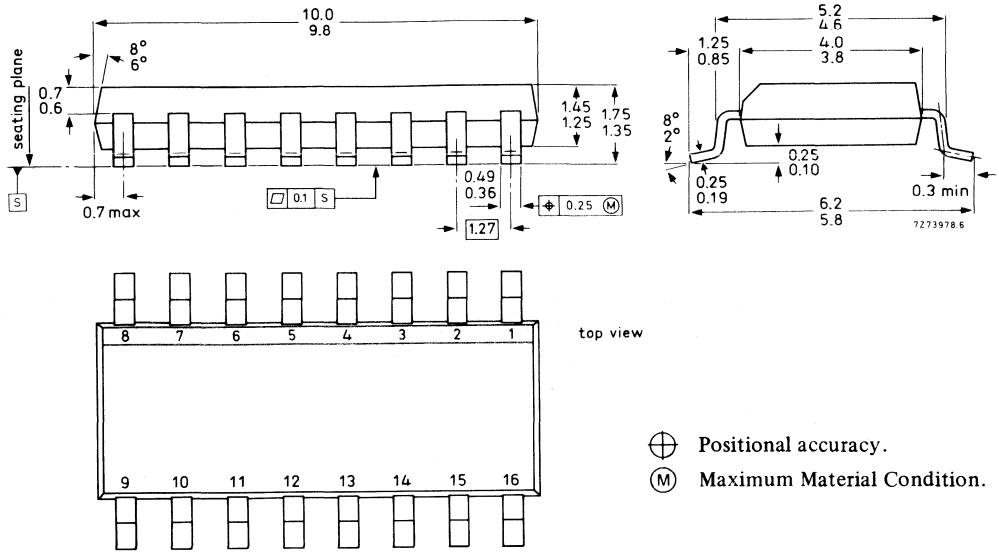
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

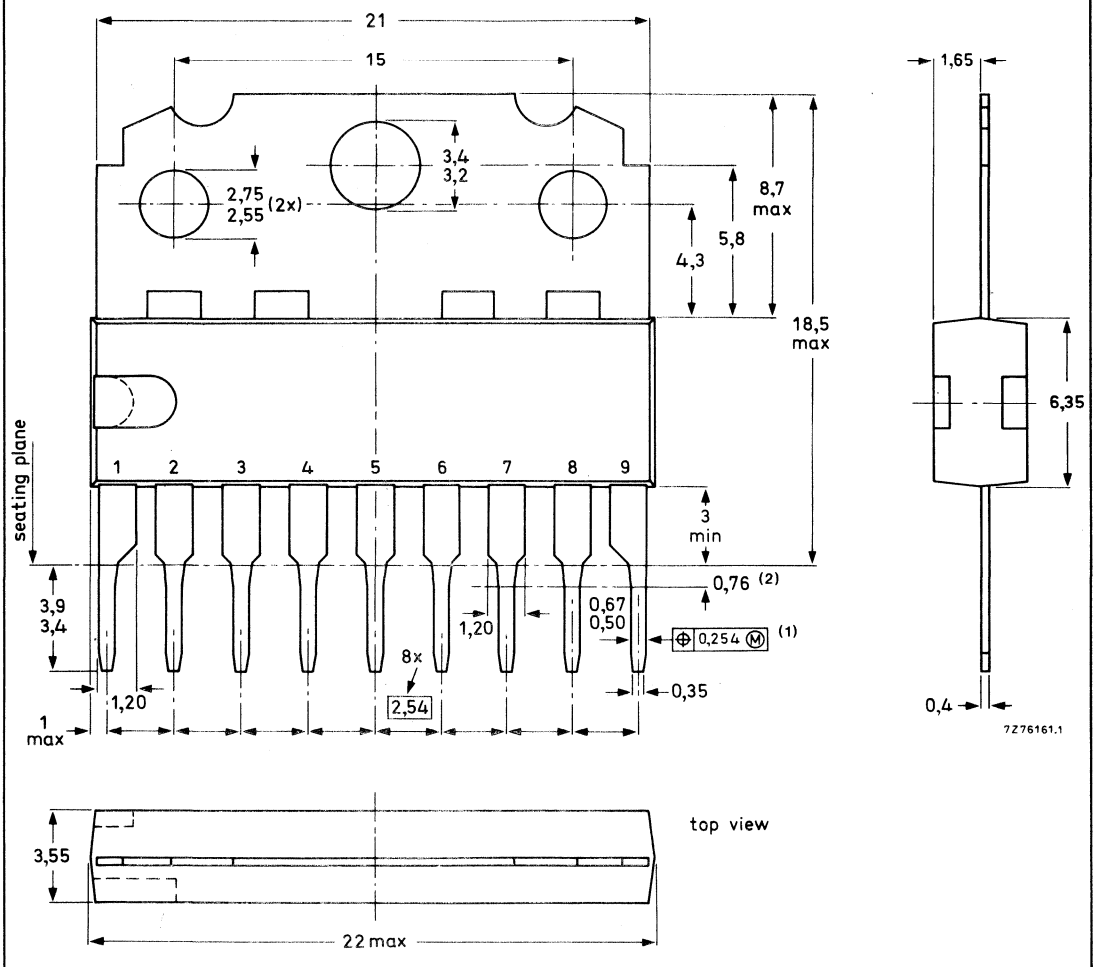
Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16; SOT109A)



Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC (SOT110B)



⊕ Positional accuracy.

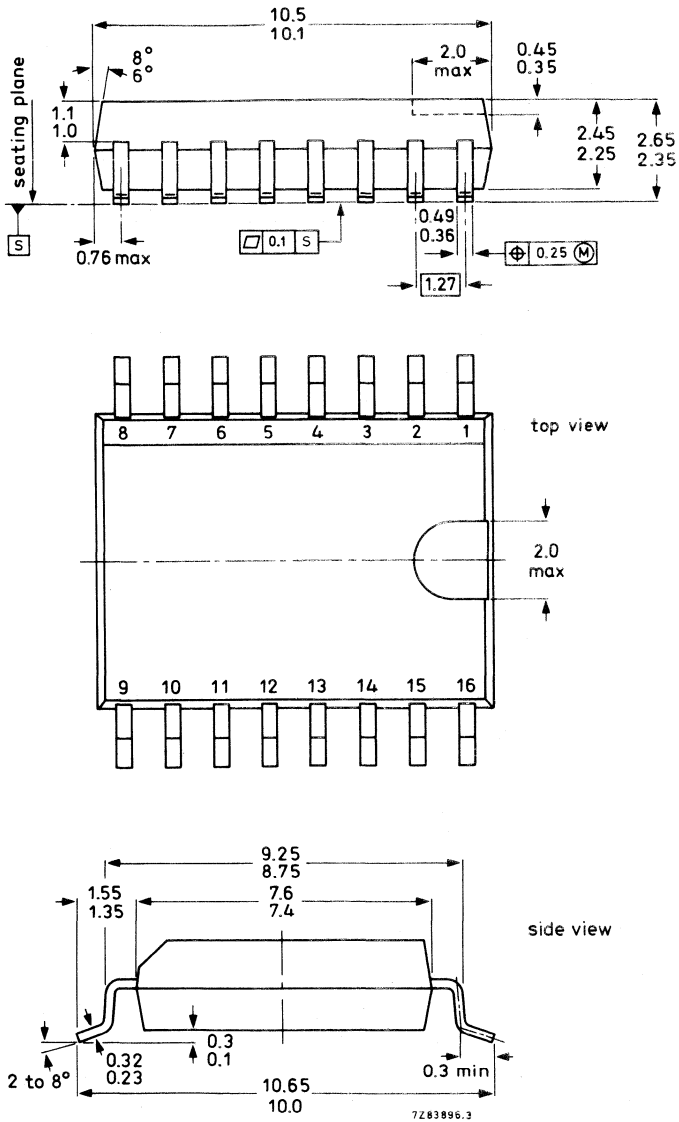
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)

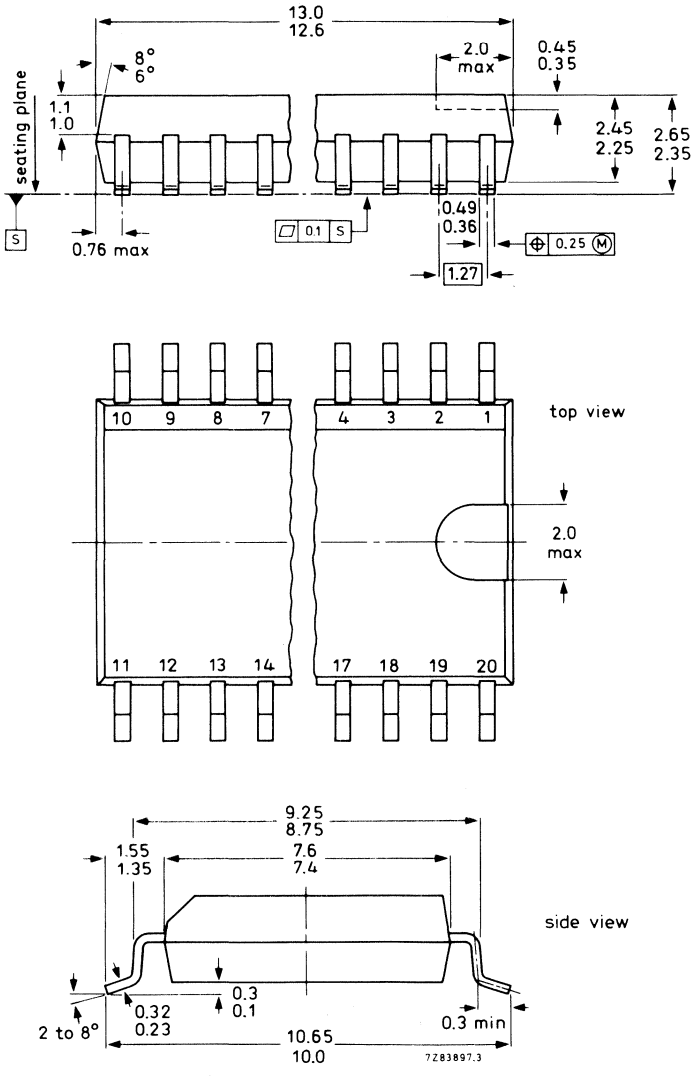


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

20-LEAD MINI-PACK; PLASTIC (SO20; SOT163A)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

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for Prefixes: MEB, SAA, TCA, TDA, and TEA 1627

Plastic dual in-line (DIL) packages 1629
Plastic mini-pack (SO) packages 1629

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of six series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MATERIALS*

The contents of each series are listed on pages iii to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom** Bipolar, MOS Subscriber sets, Cordless Telephones
IC04	**HE4000B logic family** CMOS
IC05	**Advanced Low-power Schottky (ALS) Logic Series**
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
IC08	**ECL 10K and 100K logic families**
IC09N	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
IC12	**I^2C-bus compatible ICs**
IC13	**Semi-custom** Programmable Logic Devices (PLD)
IC14	**Microcontrollers** NMOS, CMOS
IC15	**FAST TTL logic series**
Supplement to IC15	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom** Bipolar, MOS Radio pagers Mobile telephones ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**

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This series of data handbooks comprises:

current code	new code	handbook title
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S2a	**SC02***	**Power diodes**
S2b	**SC03***	**Thyristors and triacs**
S3	**SC04**	**Small-signal transistors**
S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07**	**Small-signal field-effect transistors**
S6	**SC08** **SC09**	**RF power transistors** **RF power modules**
S7	**SC10**	**Surface mounted semiconductors**
S8a	**SC11***	**Light emitting diodes**
S8b	**SC12**	**Optocouplers**
S9	**SC13***	**PowerMOS transistors**
S10	**SC14**	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S15**	**SC16**	**Laser diodes**
S13	**SC17**	**Semiconductor sensors**
S14	**SC18***	**Liquid crystal displays and driver ICs for LCDs**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

DISPLAY COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T8	**DC01**	**Colour display components**
T16	**DC02**	**Monochrome monitor tubes and deflection units**
C2	**DC03***	**Television tuners, coaxial aerial input assemblies**
C3	**DC04***	**Loudspeakers**
C20	**DC05***	**Wire-wound components for TVs and monitors**

* These handbooks are currently issued in another series; they are not yet issued in the Display Components series of handbooks.

PASSIVE COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
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C11	**PA02***	**Varistors, thermistors and sensors**
C12	**PA03**	**Potentiometers and switches**
C7	**PA04***	**Variable capacitors**
C22	**PA05***	**Film capacitors**
C15	**PA06***	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08***	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T1	*	**Power tubes for RF heating and communications**
T2a	*	**Transmitting tubes for communications, glass types**
T2b	*	**Transmitting tubes for communications, ceramic types**
T3	**PC01****	**High-power klystrons**
T4	*	**Magnetrons for microwave heating**
T5	**PC02****	**Cathode-ray tubes**
T6	**PC03****	**Geiger-Müller tubes**
T9	**PC04****	**Photo and electron multipliers**
T10	**PC05**	**Plumbicon camera tubes and accessories**
T11	**PC06**	**Circulators and Isolators**
T12	**PC07**	**Vidicon and Newvicon camera tubes and deflection units**
T13	**PC08**	**Image intensifiers**
T15	**PC09****	**Dry reed switches**
C8	**PC10**	**Variable mains transformers; annular fixed transformers**
	PC11	**Solid state image sensors and peripheral integrated circuits**

* These handbooks will not be reissued.

** Not yet issued with the new code in this series of handbooks.

MATERIALS

This series of data handbooks comprises:

current code	new code	handbook title
C4 C5	MA01*	**Soft Ferrites**
C16	MA02**	**Permanent magnet materials**
C19	MA03**	**Piezoelectric ceramics**

* Handbooks C4 and C5 will be reissued as one handbook having the new code MA01.

** Not yet issued with the new code in this series of handbooks.

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